Stefan Nikolić

Updated September 26, 2024

Email: stefan.nikolic@dmi.uns.ac.rs **Phone**: +381 (0) 65 4222 697

About me:

I am an Assistant Professor at the Department of Mathematics and Informatics, Faculty of Sciences, University of Novi Sad. Previously, I was a PhD student at EPFL, where I worked at the Processor Architecture Laboratory (LAP), under the supervision of Professor Paolo Ienne. My research currently focuses on developing new algorithms for automating various aspects of designing reconfigurable architectures, as well as for mapping user designs onto reconfigurable architectures.

Education

École Polytechnique Fédérale de Lausanne Lausanne, Switzerland
PhD in Computer Science 09.2017–07.2023
Thesis Title: "Automating the Design of Programmable Interconnect for Reconfigurable Architectures"
Thesis Advisor: Paolo Ienne

University of Novi Sad Novi Sad, Serbia
BEng (Hons) in Electrical and Computer Engineering 09.2013–07.2017
GPA: 9.98/10.00
Thesis Title : "On the Problem of FPGA Realization of Asynchronous Circuits"
Thesis Advisor: Ivan Mezei

Awards and Honors

2024 European Design and Automation Association (EDAA) Outstanding Dissertation Award for the best thesis in the fields of *new directions in systems design methods and tools, simulation and validation, embedded software design and optimization for embedded, cyber-physical, secure and learning systems.*

2023 EDIC Patrick Denantes Memorial Prize for the best PhD thesis defended at the School of Computer and Communication Sciences of EPFL between 01.09.2022 and 31.08.2023.

Michal Servit Best Paper Memorial Award at FPL'21, for *the most outstanding paper in the area of design algorithms, methods, and CAD tools for FPGAs and self-aware systems.*

Michal Servit Best Paper Memorial Award at FPL'20

EPFL EDIC Doctoral Fellowship (2017)

Languages

Serbian (native), English (fluent), French (basic), Russian (basic)

Publications

Runtime efficient multi-stage router flow for circuit designs (*USPTO*)
Dinesh Gaitonde, Chirag Ravishankar, and Stefan Nikolić
(Patent application published, pending approval)

Exploring FPGA Switch-Blocks without Explicit Pattern Listing (*TRETS'24*)
Stefan Nikolić and Paolo Ienne

IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck (*ICCAD'23*)
Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar,
Dinesh Gaitonde, and Mirjana Stojilović

Regularity Matters: Designing Practical FPGA Switch-Blocks (*FPGA'23*)
Stefan Nikolić and Paolo Ienne

Mitigating the Last-Mile Bottleneck: A Two-Step Approach For Faster Commercial FPGA Routing (*FPGA'23*)
Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar,
Dinesh Gaitonde, and Mirjana Stojilović
(Abstract only)

Detailed Placement for Dedicated LUT-Level FPGA Interconnect (*TRETS'22*)
Stefan Nikolić, Grace Zgheib, and Paolo Ienne

Turning PathFinder Upside-Down: Exploring FPGA Switch-Blocks by Negotiating Switch Presence (*FPL'21*)
Stefan Nikolić and Paolo Ienne
(Michal Servit Best Paper Award)

Global Is the New Local: FPGA Architecture at 5nm and Beyond (*FPGA'21*)
Stefan Nikolić, Francky Catthoor, Zsolt Tőkei, and Paolo Ienne

NetCracker: A Peek into the Routing Architecture of Xilinx 7-Series FPGAs (*FPGA'21*)
Morten B. Petersen, Stefan Nikolić, and Mirjana Stojilović

Timing-Driven Placement for FPGA Architectures with Dedicated Routing Paths (*FPL'20*)
Stefan Nikolić, Grace Zgheib, and Paolo Ienne
(Michal Servit Best Paper Award)

Straight to the Point: Intra- and Intercluster LUT Connections to Mitigate the Delay of Programmable Routing (*FPGA'20*)
Stefan Nikolić, Grace Zgheib, and Paolo Ienne

Finding a Needle in the Haystack of Hardened Interconnect Patterns (*FPL'19*)
Stefan Nikolić, Grace Zgheib, and Paolo Ienne
(Short paper)

On Feasibility of FPGAs without a Dedicated Programmable Interconnect Structure (*FPGA'19*)
Anastasiia Kucherenko, Stefan Nikolić, and Paolo Ienne
(Abstract only)

All publications can be found at the LAP's website: epfl.ch/labs/lap/pubs.
The corresponding artifacts are available at github.com/EPFL-LAP.

Invited Talks

Algorithms for Automated FPGA Interconnect Design (2023)
CUNY Graduate Center, City University of New York

Automating the Design of FPGA Switch-Blocks (2023)
University of Pennsylvania

Systematic Exploration of FPGA Interconnect (2022)
EDIC Open House, EPFL

Straight to the Point: Intra- and Intercluster LUT Connections to Mitigate the Delay of Programmable Routing (2020)
Xilinx, San Jose

Internships

Xilinx, Inc., Longmont, CO, USA
Architecture Engineer Intern, 09.2021–02.2022

I worked in Xilinx's (now part of AMD) FPGA architecture team under the supervision of Chirag Ravishankar and Dinesh Gaitonde, exploring novel FPGA interconnect ideas, including reproducing some of my work from EPFL in industrial context. Most of the work focused on architectural modifications aimed at increasing performance of implemented circuits, but some algorithmic improvements were also made, both in terms of increasing the quality of results produced by the CAD tools and reducing their runtime.

Frobas d.o.o Novi Sad, Novi Sad, Serbia
Hardware Design Intern 11.2016–02.2017

I worked on preliminary architecture design of a Support-vector machine accelerator. I also wrote most of the RTL description for the first prototype and performed initial functional verification. The project was a joint effort between Frobas d.o.o and the Chair of Electronics of the Faculty of Technical Sciences, headed by Professor Rastislav Struharik and Dr. Mihajlo Katona.

EPFL, LAP, Lausanne, Switzerland
Research Intern 07.2016–09.2016

I worked on transistor-level design and optimization of *And-Inverter Cones* (AICs) for use in FPGA logic clusters, under the supervision of Grace Zgheib.

Teaching experience

Algorithms in Hardware Design (Seminar), University of Novi Sad Fall 2024

This seminar introduces computer science students to the fundamental EDA algorithms and strives to prepare them for conducting research in this area.

Advanced Programming for Mathematicians, University of Novi Sad Fall 2024

This course is given to MSc students of the Data Science program at the mathematics section, with an intention of enabling them to write high-performance programs in C++.

Software Processes, University of Novi Sad Spring 2024

This course introduces third and fourth year computer science students to the fundamental concepts of software development methodologies, team organization, and project management

Programming 2, University of Novi Sad Spring 2024

This is the second programming course given to MSc mathematics students, introducing them to object-oriented programming in C++.

CS-173 Digital System Design, Computer Science, EPFL Spring 2019, 2020, 2021, 2022

This is the first hardware-related course in the computer science bachelor degree programs at EPFL, taught by Professor Theo Kluter. It covers basic topics in logic design, as well as hardware description languages, and some FPGA architecture. Apart from designing and organizing the labs, my tasks also covered writing grading automation scripts, maintaining submission servers, and developing a system for remote access to FPGA boards. For several years, I served as the head TA for the course, coordinating a team of about ten other assistants.

CS-119(h) Information, Computation, Communication, Civil Engineering, EPFL Fall 2019

This is a general culture course introducing fundamental concepts of computer science to students at other departments. My duties were related to practical labs, which covered programming in Python. The course instructor was Dr. Jean-Philippe Pellet.

CS-208 Computer Architecture, Computer Science, EPFL Fall 2018

This is the first computer architecture course in the computer science bachelor degree programs at EPFL, taught by Dr. Mirjana Stojilović. As part of the practical labs that I was involved in, the students learned about the principles of microarchitecture design, implementing a Nios II processor on an FPGA, writing the RTL from scratch. They also learned the principles of assembly programming. Apart from designing the labs, I was responsible for designing some of the exam questions.

CS-111(f) Programming, Chemistry, EPFL Spring 2018

This course is very similar to CS-119(h) apart from the language of instruction being C and the course contents being tailored to the needs of chemistry students. The instructor at the time was Dr. Mirjana Stojilović.

Supervising

I had a chance to supervise several incredible interns through the Summer@EPFL program, starting from 2018. Continued cooperation with two of them also allowed me to cosupervise one bachelor thesis at the Taras Shevchenko National University of Kyiv and one master thesis at École Polytechnique.

Service

As a secondary reviewer to Professor Ienne, I reviewed papers submitted to FPGA, FPL, FCCM, IWLS, ASAP, and TCAD. As the primary reveiwer, I reviewed papers submitted to CSUR, TRETS, TCAD, FPGA, FPL, IWLS, and HEART. I also helped in organization of FPL'16 in Lausanne, FPGA'21 and '22 as virtual events, and FPGA'23 in Monterey, California, and I chaired poster sessions at FPGA'22, IWLS'23, and regular sessions at IWLS'24. In 2021 and 2022, I served as one of the EDIC Ambassadors, helping to promote the computer science PhD program of EPFL. During my entire stay at EPFL as a PhD student, I participated in organization of Summer@EFPL, not only as a mentor, but also by organizing events for the interns, such as hikes and visits to the CROCUS research reactor.