UNIVERSITY OF DUBLIN

TRINITY COLLEGE

Faculty of Engineering, Mathematics and Science
School of Computer Science and Statistics

Integrated Computer Science Programme
B.A.I. Engineering
Annual Examinations

Trinity Term 2014

CS2022 – Computer Architecture I

Wednesday 7th May, 2014 Regent House 14:00 – 16:00

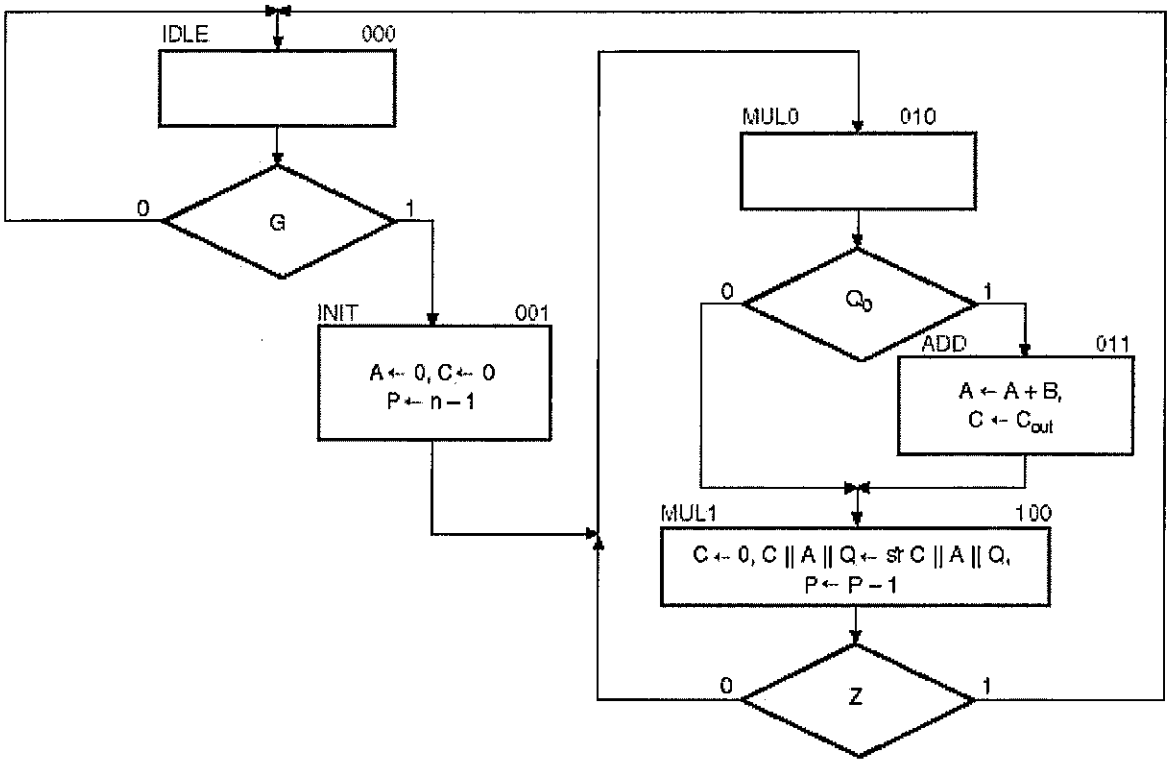
Dr. Michael Manzke

Answer **three** questions.

The use of non-programmable calculators is permitted.

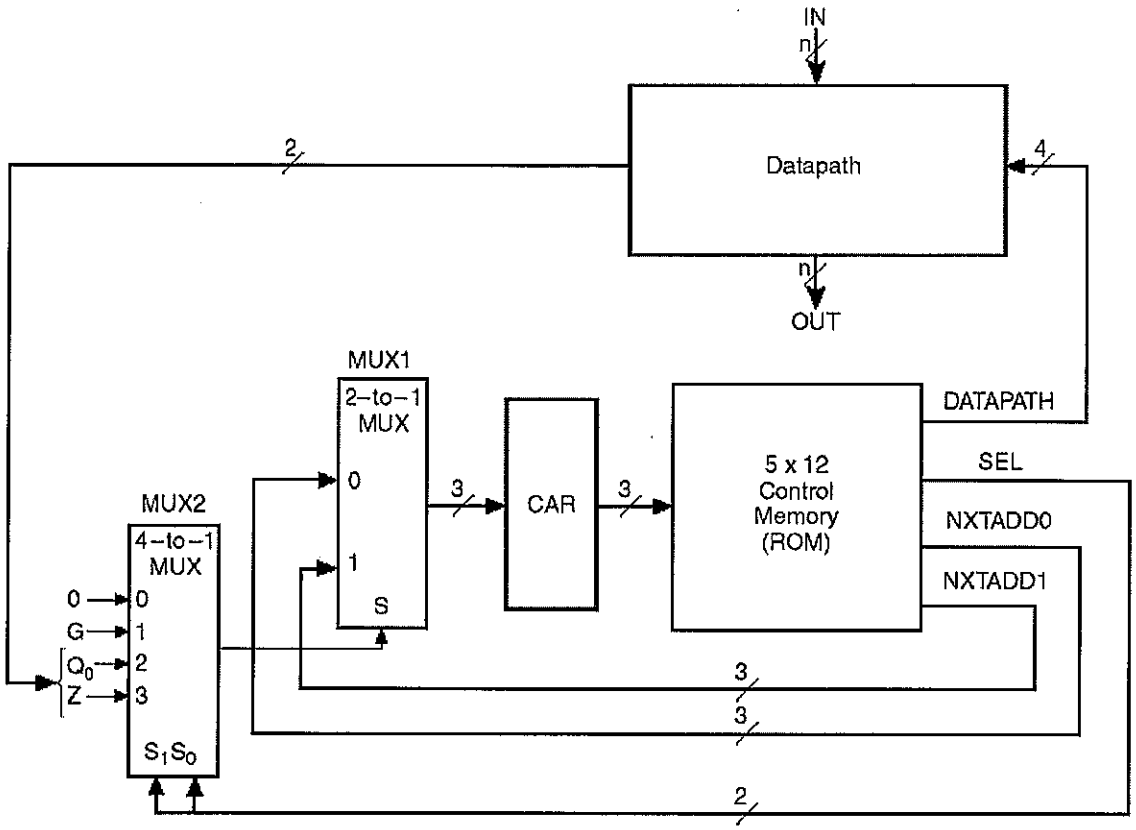
1.

The following ASM Chart describes the sequential operations of a Binary Multiplier:



a) The above ASM Chart is suitable for a microcoded control implementation. What would you need to change in order to make the ASM suitable for a hardwired solution? Why is this modification necessary?

[5 marks]



Control Signal	Register Transfers	States in Which Signal is Active	Micro-instruction Bit Position	Symbolic Notation
Initialize	$A \leftarrow 0, P \leftarrow n-1$	INIT	0	IT
Load	$A \leftarrow A+B, C \leftarrow C_{out}$	ADD	1	LD
Clear_C	$C \leftarrow 0$	INIT, MUL1	2	CC
Shift_dec	$C\|A\|Q \leftarrow \text{sr } C\|A\|Q, P \leftarrow P-1$	MUL1	3	SD

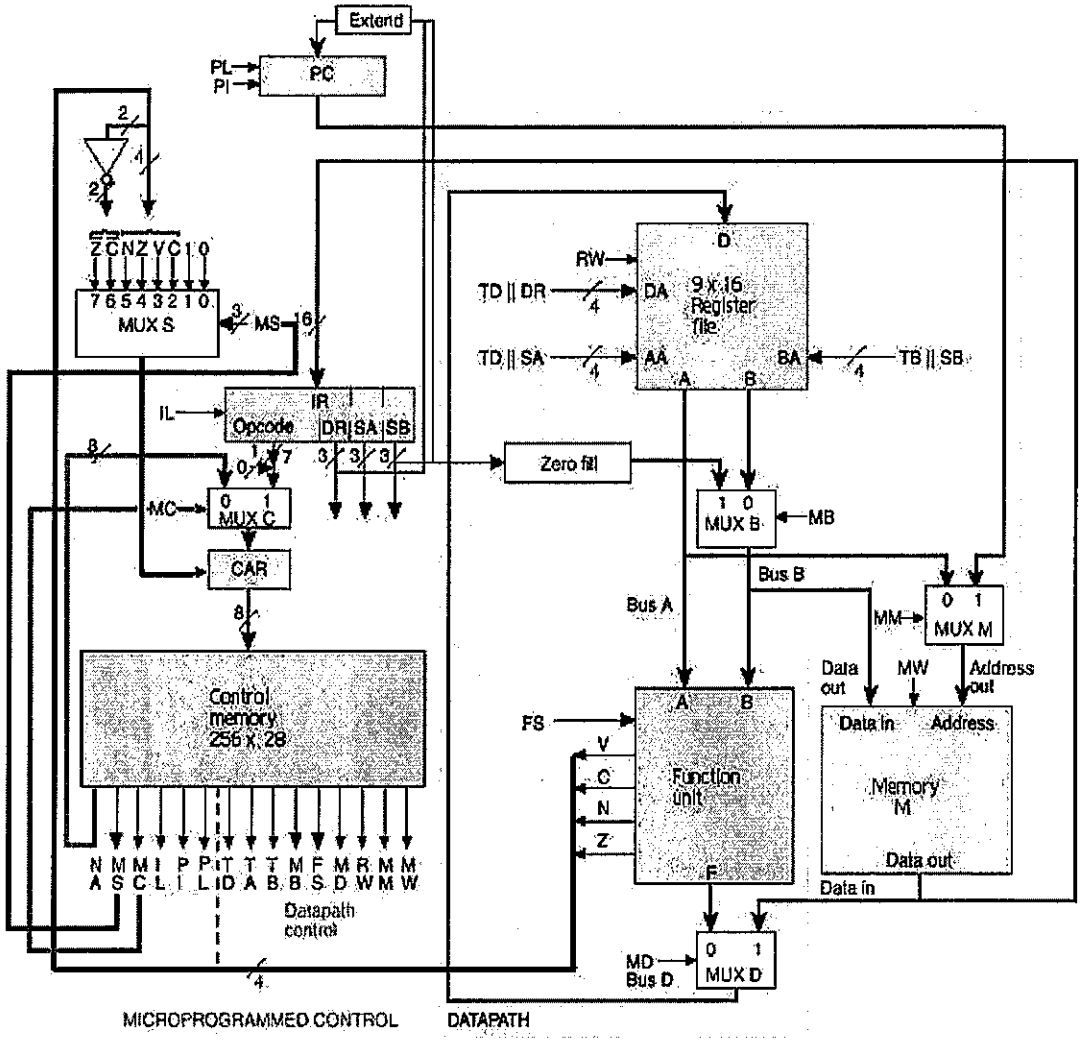
b) Please provide microcode for the above Control Memory (5x12) that implements the above ASM Chart. Discuss how the control hardware executes your microcode.

[15 marks]

2.

a) Explain in detail the operations that take place when the following multiple-cycle microprogrammed instruction set processor executes machine instructions.

[10 marks]



b) Expand on your discussion from Question 2.a) by explaining how the following instruction is executed. In particular discuss all operations in the microprogrammed control:

Subtraction followed by a branch on negative. Explain what happens when the branch is taken and when it is not taken.

[10 marks]

3.

a) Provide a detailed schematic for a *Function Unit* that implements the following *micro-operations*:

[10 marks]

Table 1: FS code definition

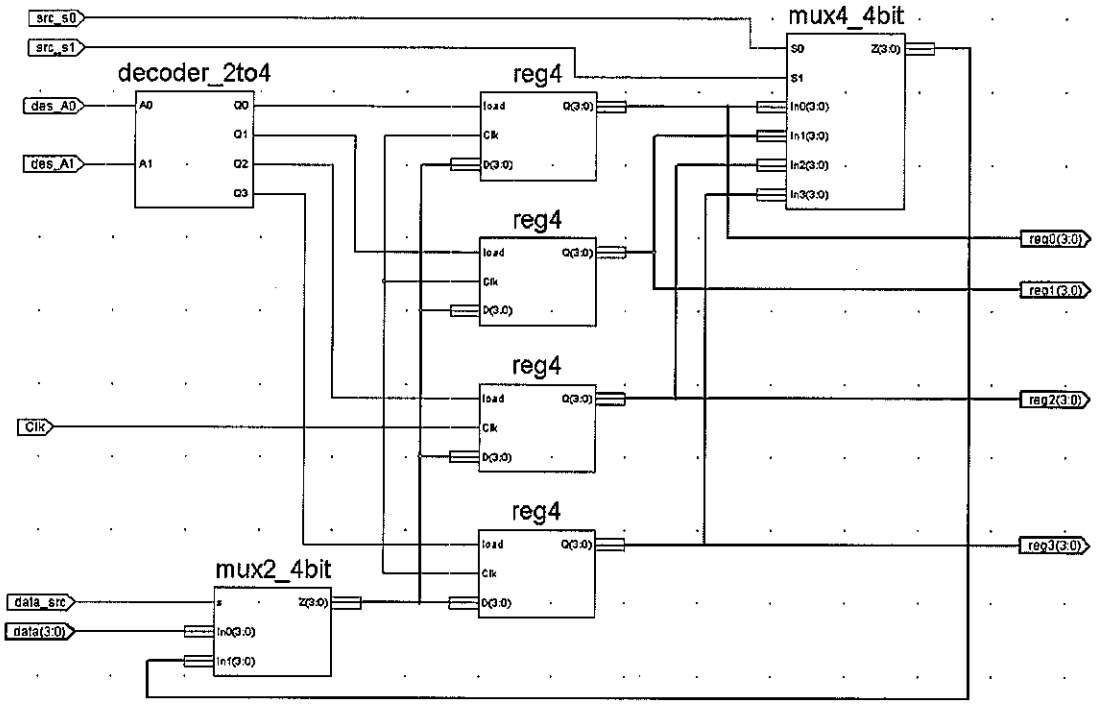
FS	Micro-operation
00000	$F = A$
00001	$F = A + 1$
00010	$F = A + B$
00011	$F = A + B + 1$
00100	$F = A + \bar{B}$
00101	$F = A + \bar{B} + 1$
00110	$F = A - 1$
00111	$F = A$
01000	$F = A \wedge B$
01010	$F = A \vee B$
01100	$F = A \oplus B$
01110	$F = \bar{A}$
10000	$F = B$
10100	$F = srB$
11000	$F = slB$

b) Provide VHDL code for a 4bit barrel shifter.

[10 marks]

4 a) Write VHDL code that implements the following *Register-file*:

[12 marks]



b) Provide a VHDL Test Bench for the Register-file code.

[8 marks]