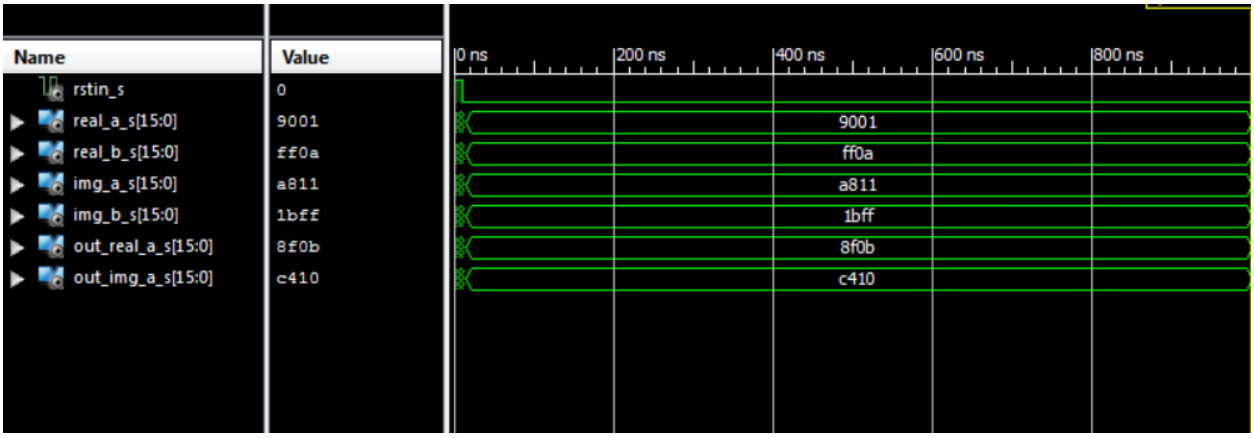
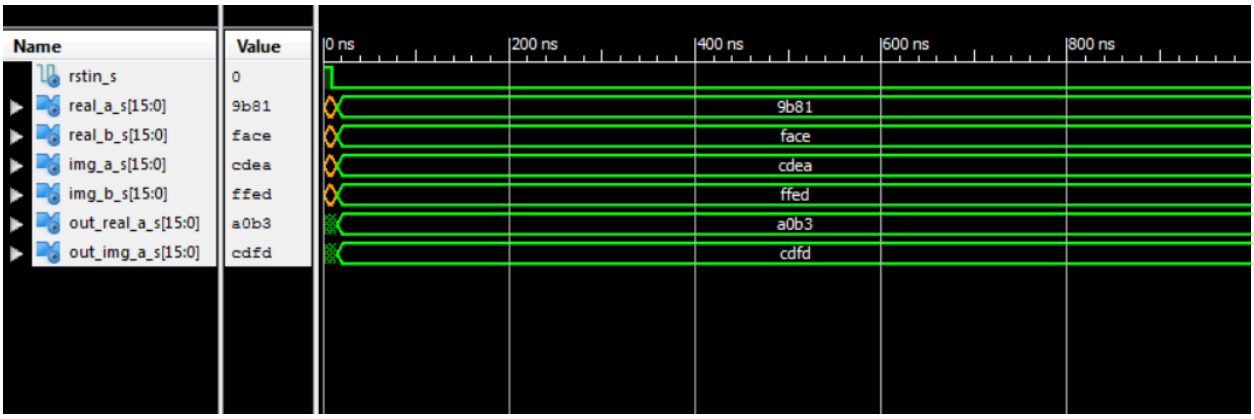
VHDL Simulations

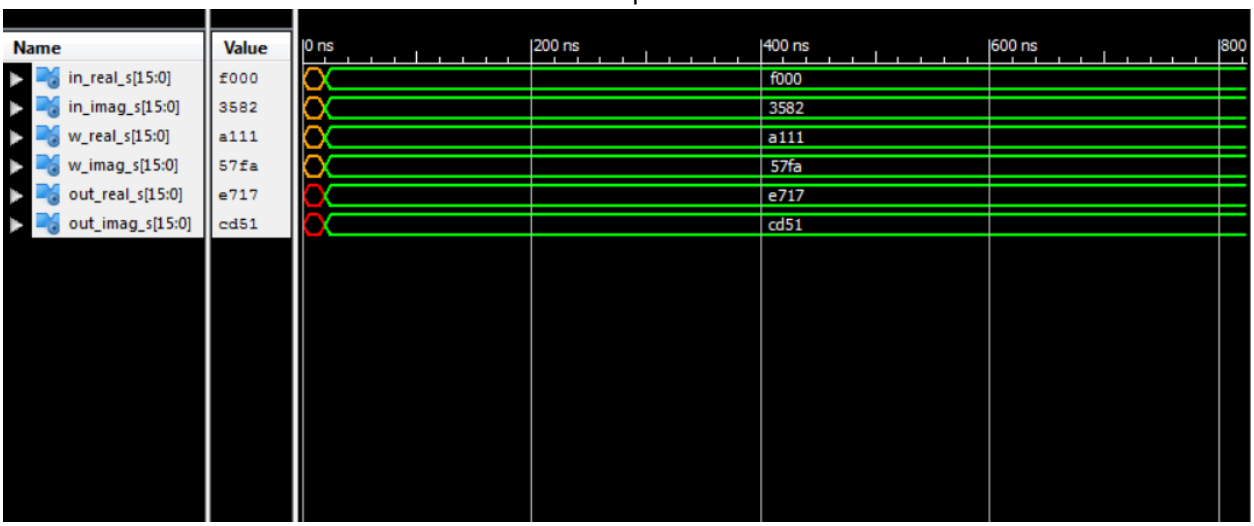
Adder



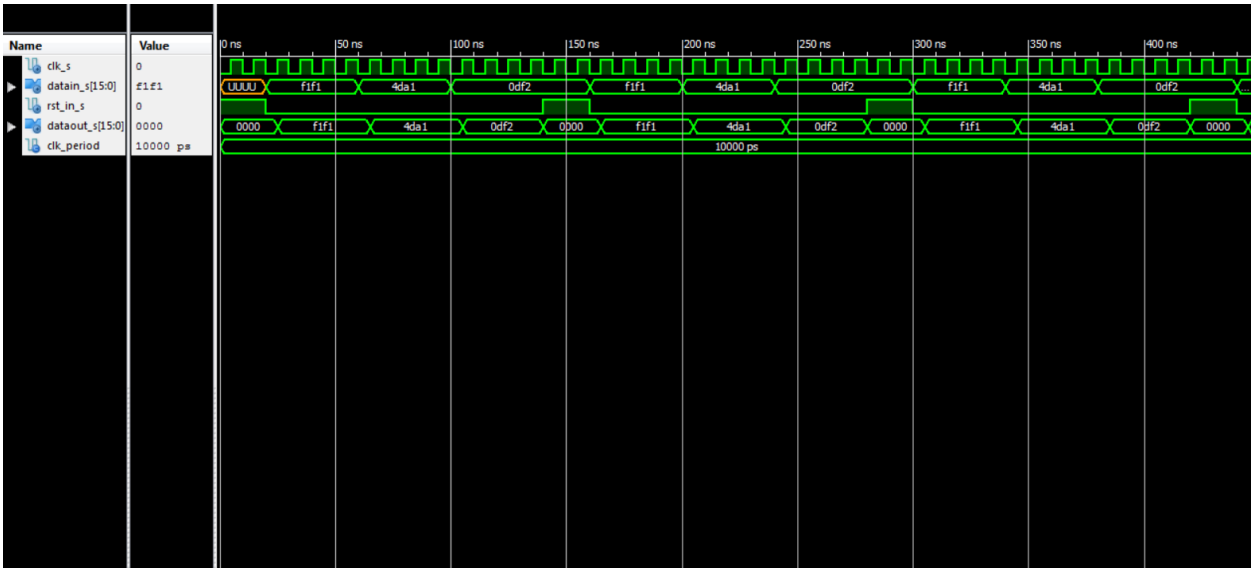

Subtractor



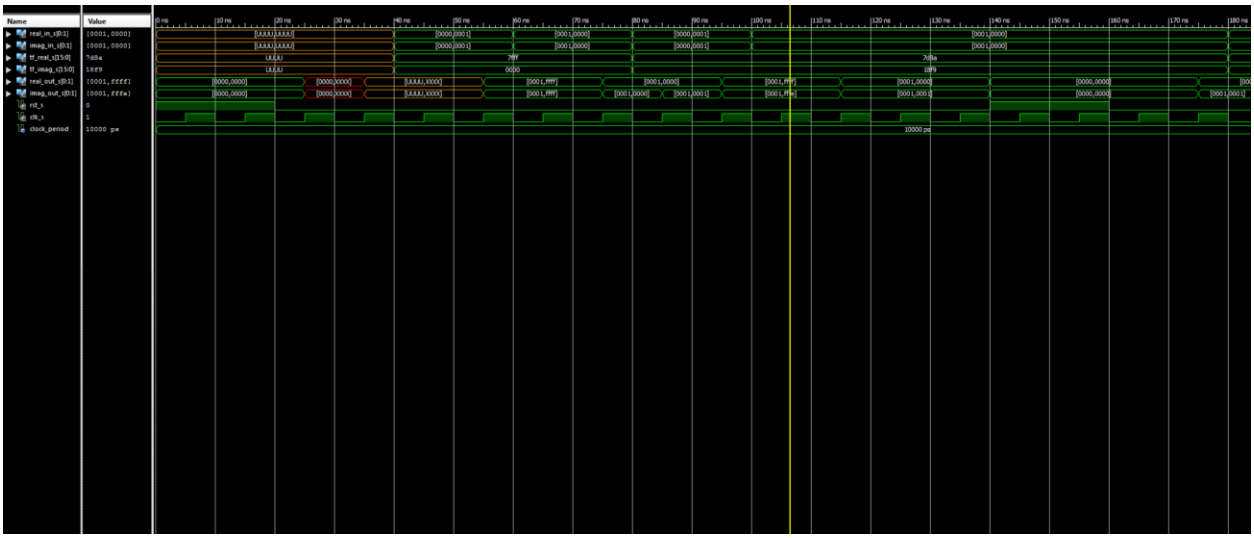

Multiplier



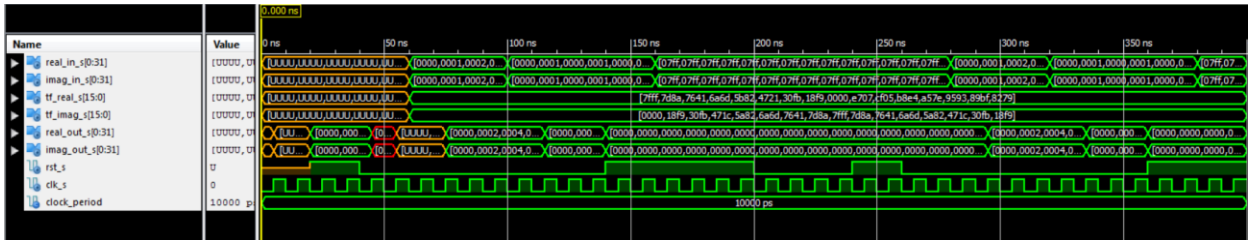
Register

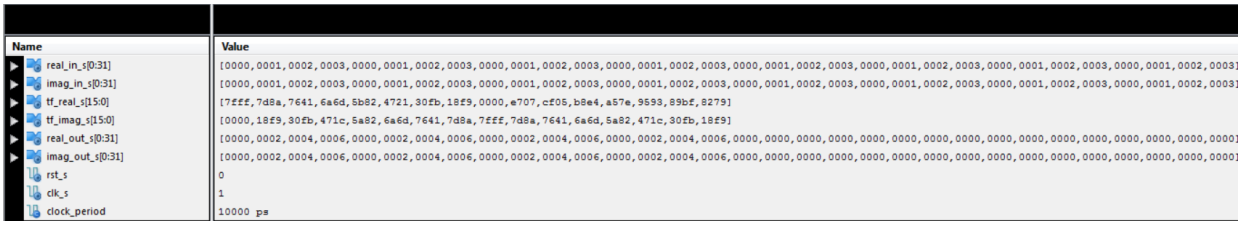



Single_DFT

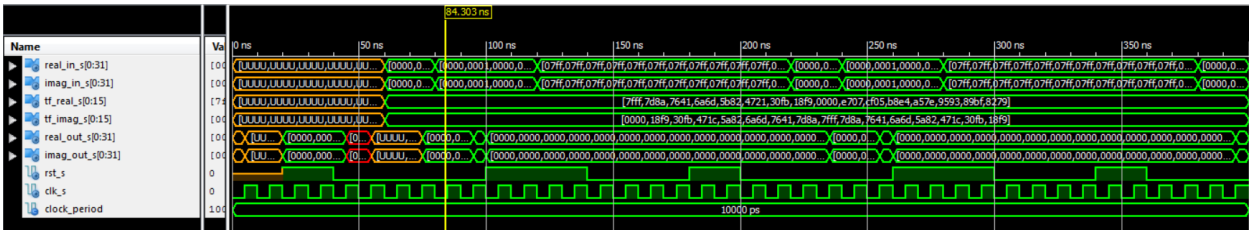


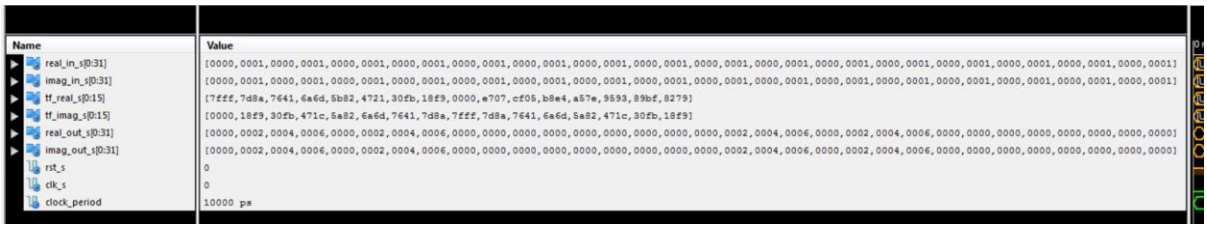
Stage 1



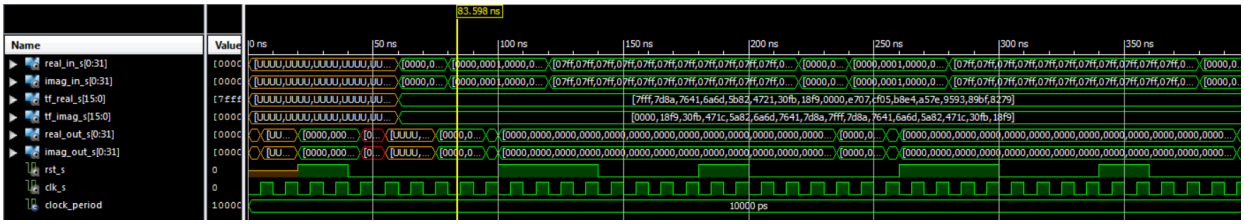



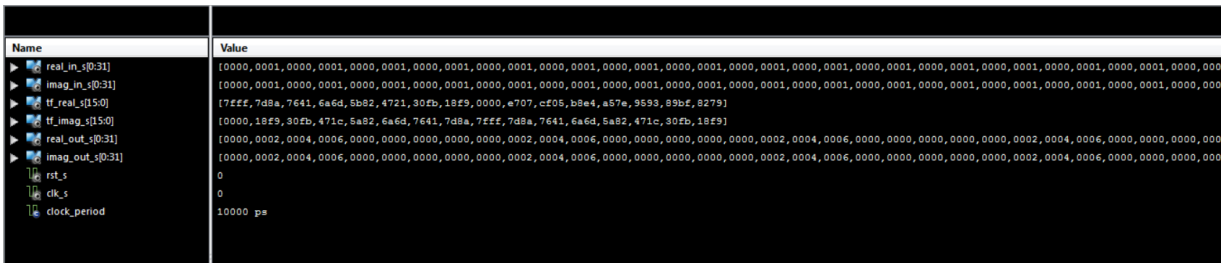

Stage 2



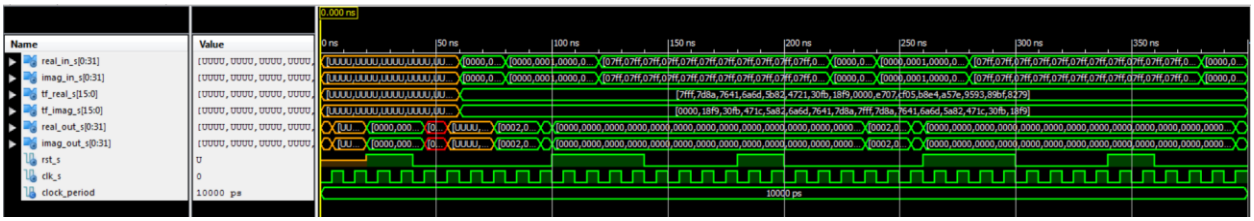



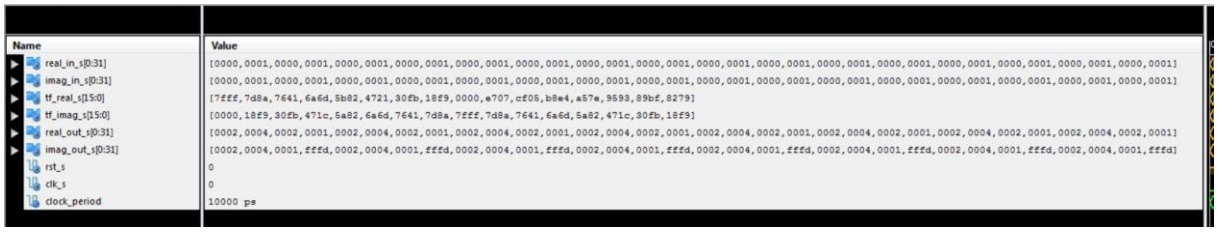
## Stage 3



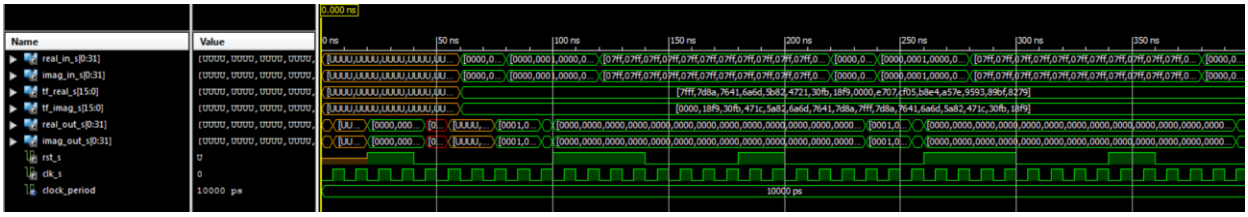



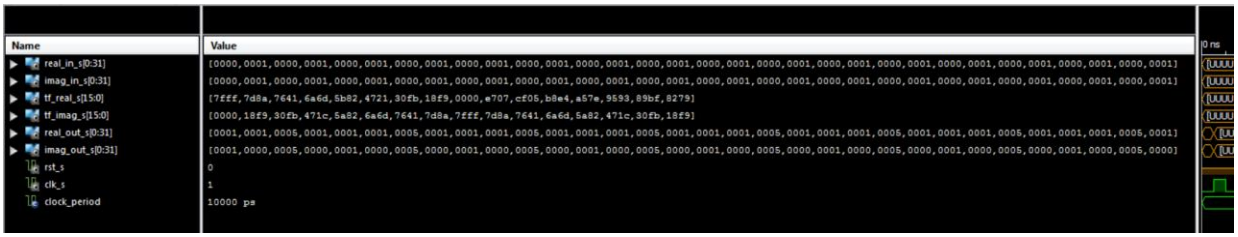

## Stage 4



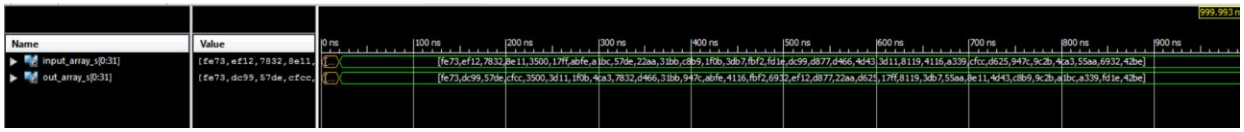




## Stage 5

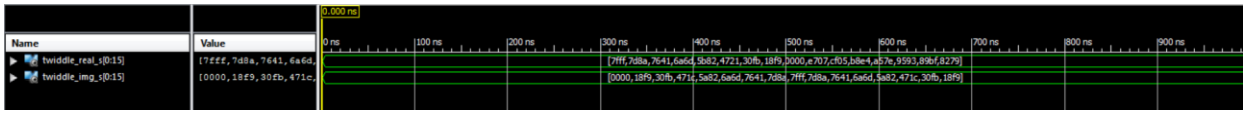


Swapper




Twiddle




Full FFT – With Working Output, but unverified accuracy