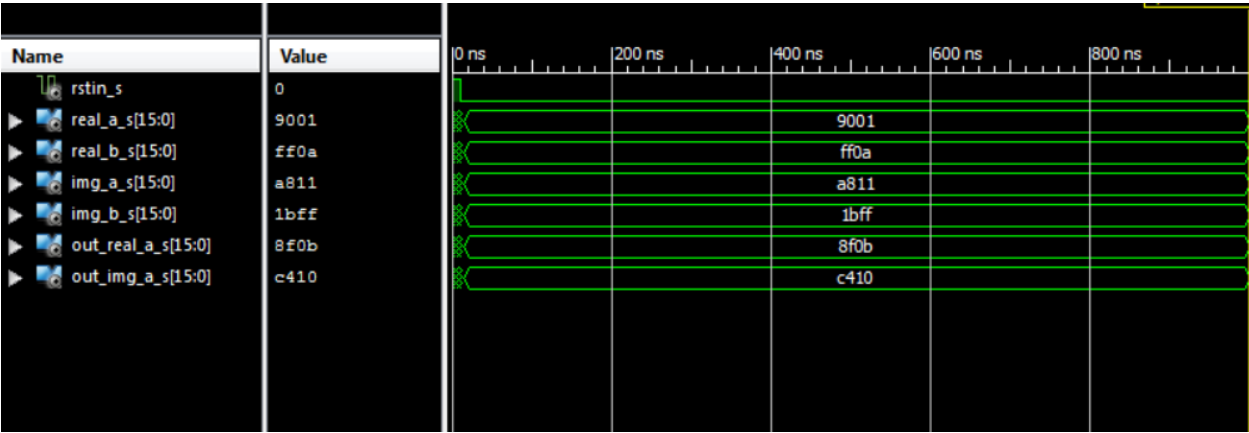
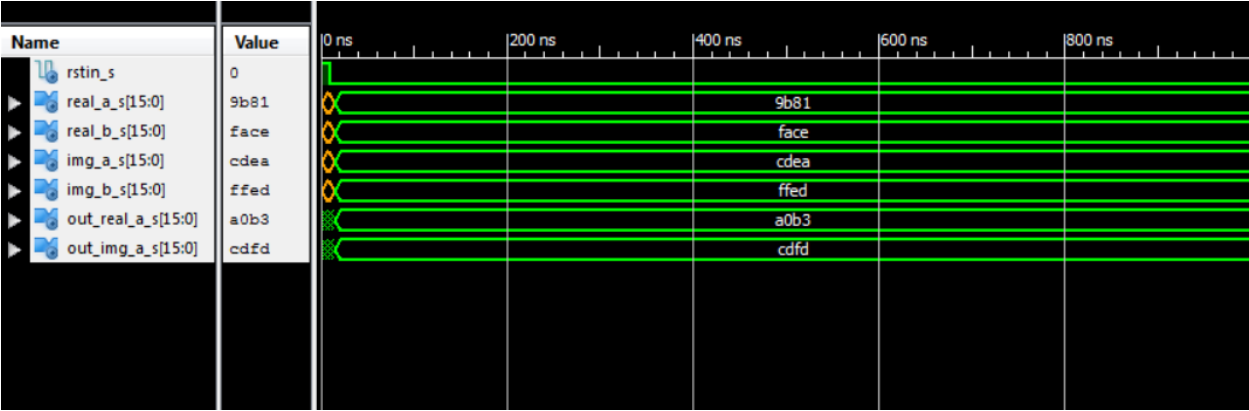


VHDL Simulations

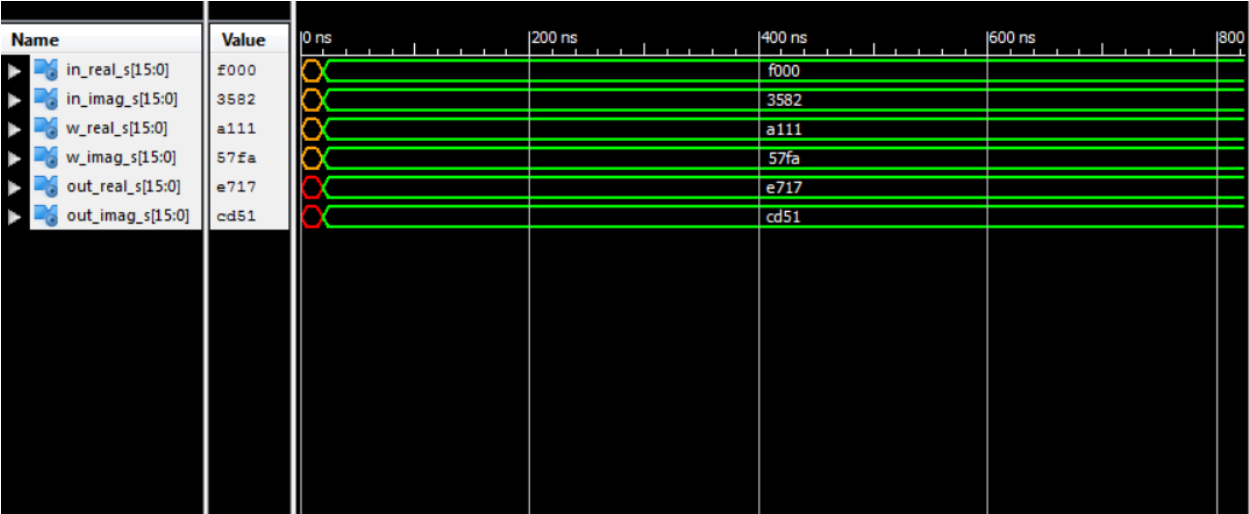
Adder



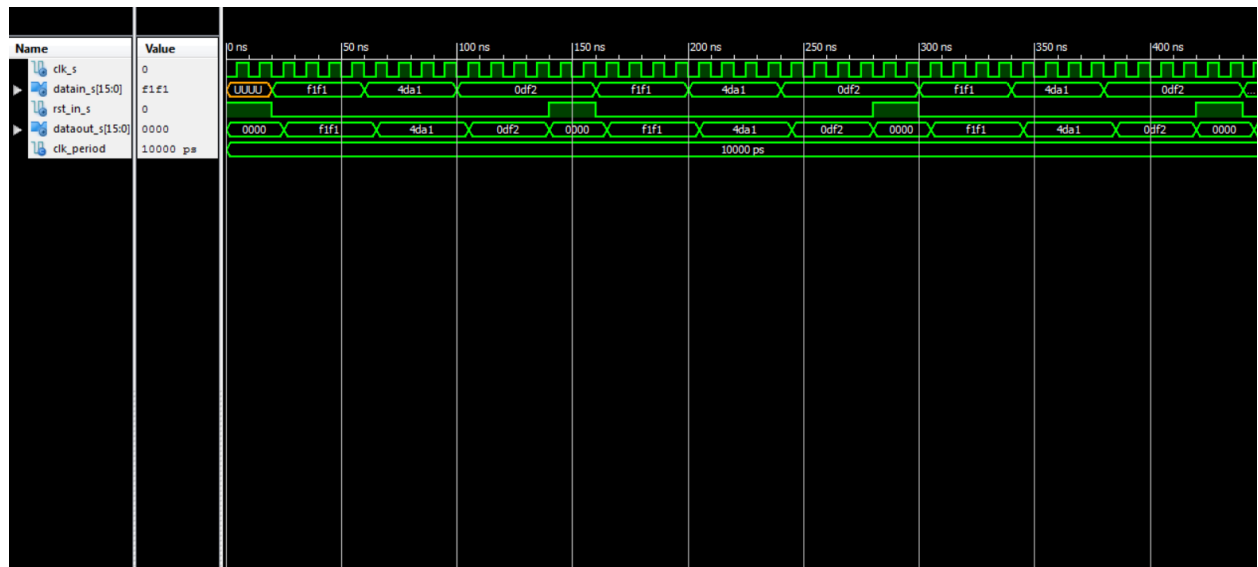
Subtractor



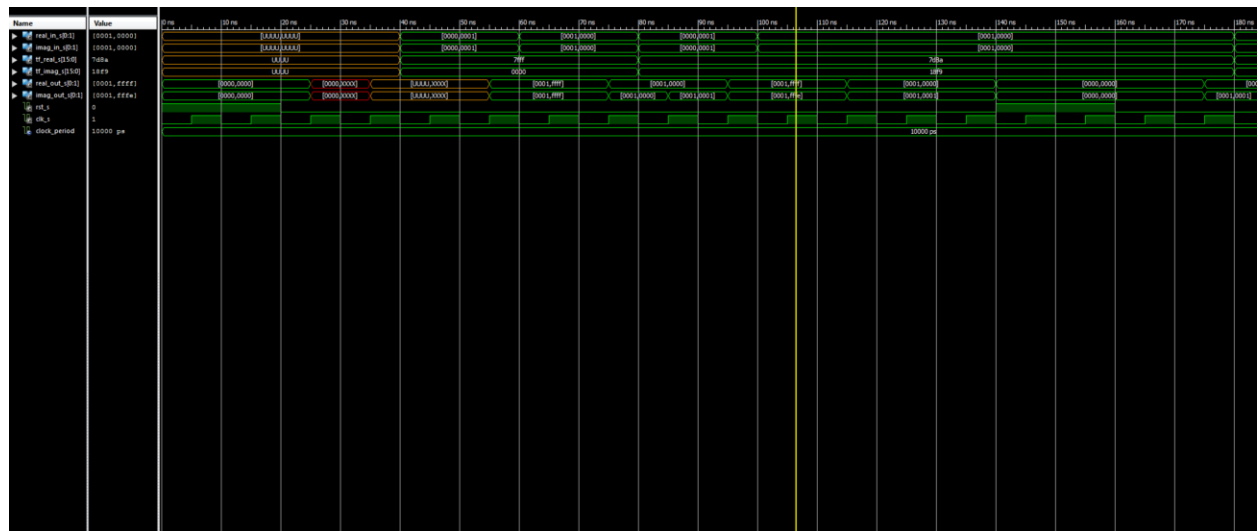
Multiplier



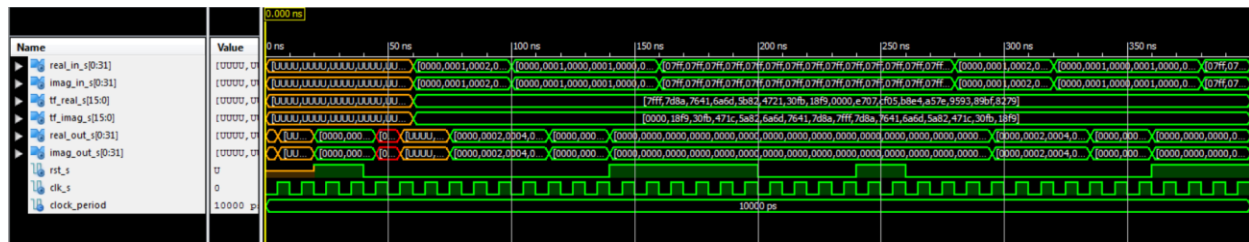
Register



Single_DFT

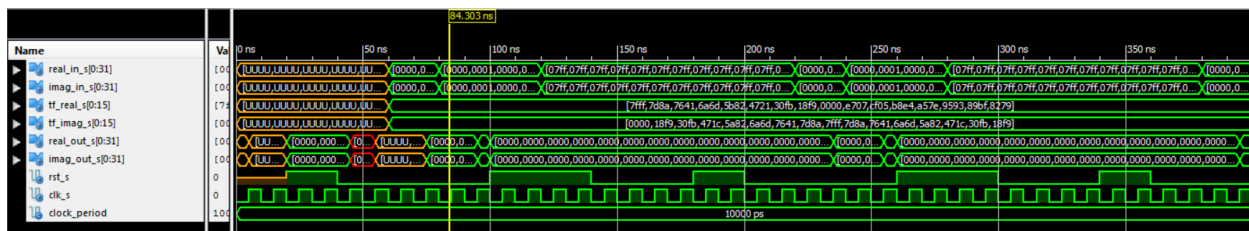


Stage 1

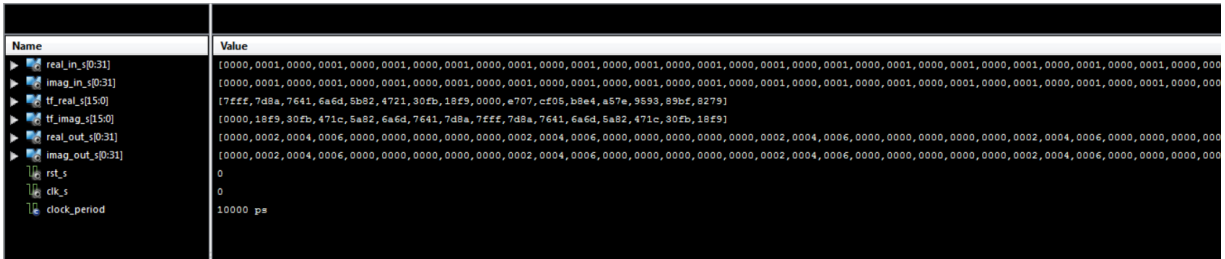
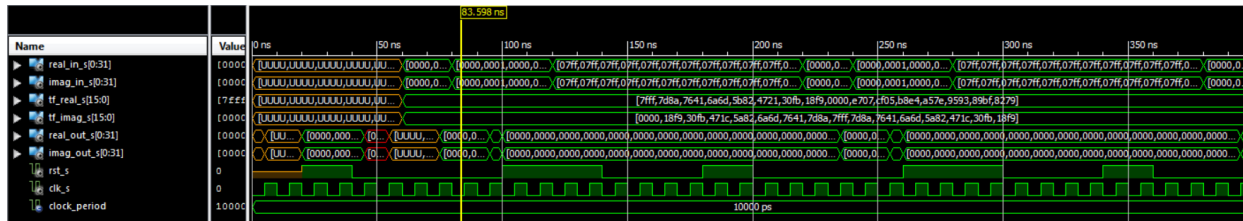


Name	Value
real_in_s[0:31]	{0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003}
imag_in_s[0:31]	{0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003, 0000, 0001, 0002, 0003}
tf_real_s[5:0]	{7fff, 7d8a, 7641, 6aed, 5b82, 4721, 30fb, 18f9, 0000, e707, c705, b9e4, a57e, 9593, 89bf, 8279}
tf_imag_s[5:0]	{0000, 18f9, 30fb, 471c, 5a82, 6aed, 7641, 7d8a, 7fff, 7d8a, 7641, 6aed, 5a82, 471c, 30fb, 18f9}
real_out_s[0:31]	{0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000}
imag_out_s[0:31]	{0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0002, 0004, 0006, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000, 0000}
rst_s	0
clk_s	1
clock_period	10000 ps

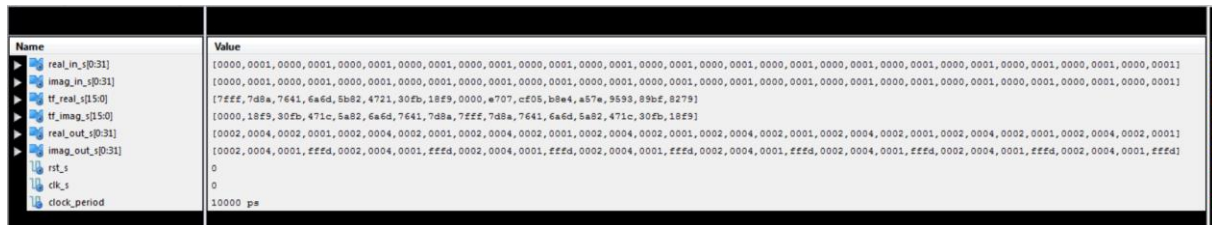
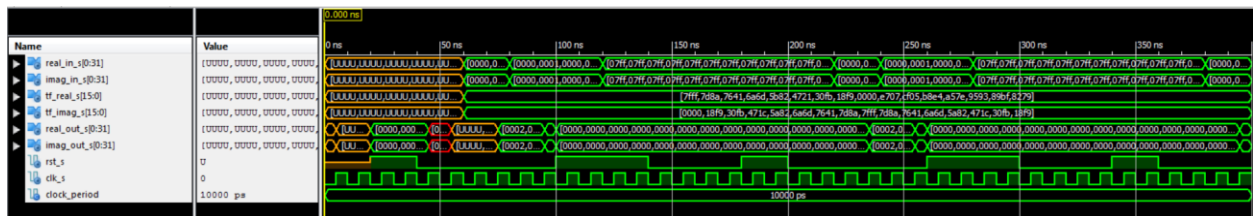
Stage 2

[illegible]

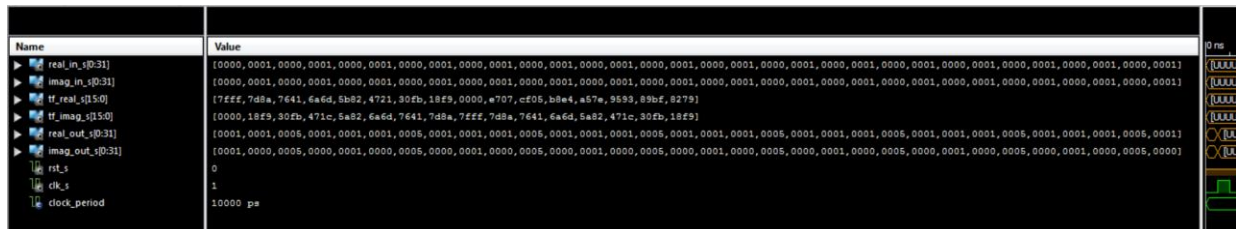
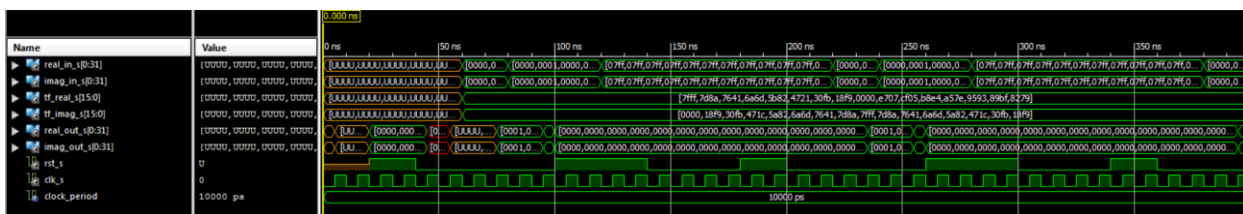
Stage 3



Stage 4



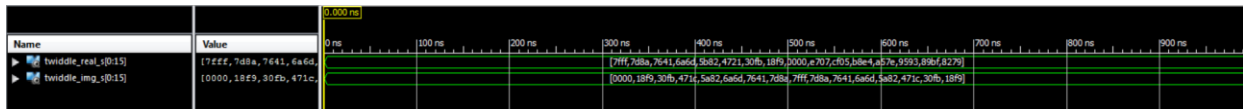
Stage 5



Swapper



Twiddle



Full FFT – With Working Output, but unverified accuracy

