16-bit MRAA Processor

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Overview

Multi-Register Accumulator Architecture

- Designed to minimize processor area and complexity of software
- Uses a primary accumulator register and several supplementary registers
- Multi-cycle design maximizes clock speed while allowing variable instruction timing

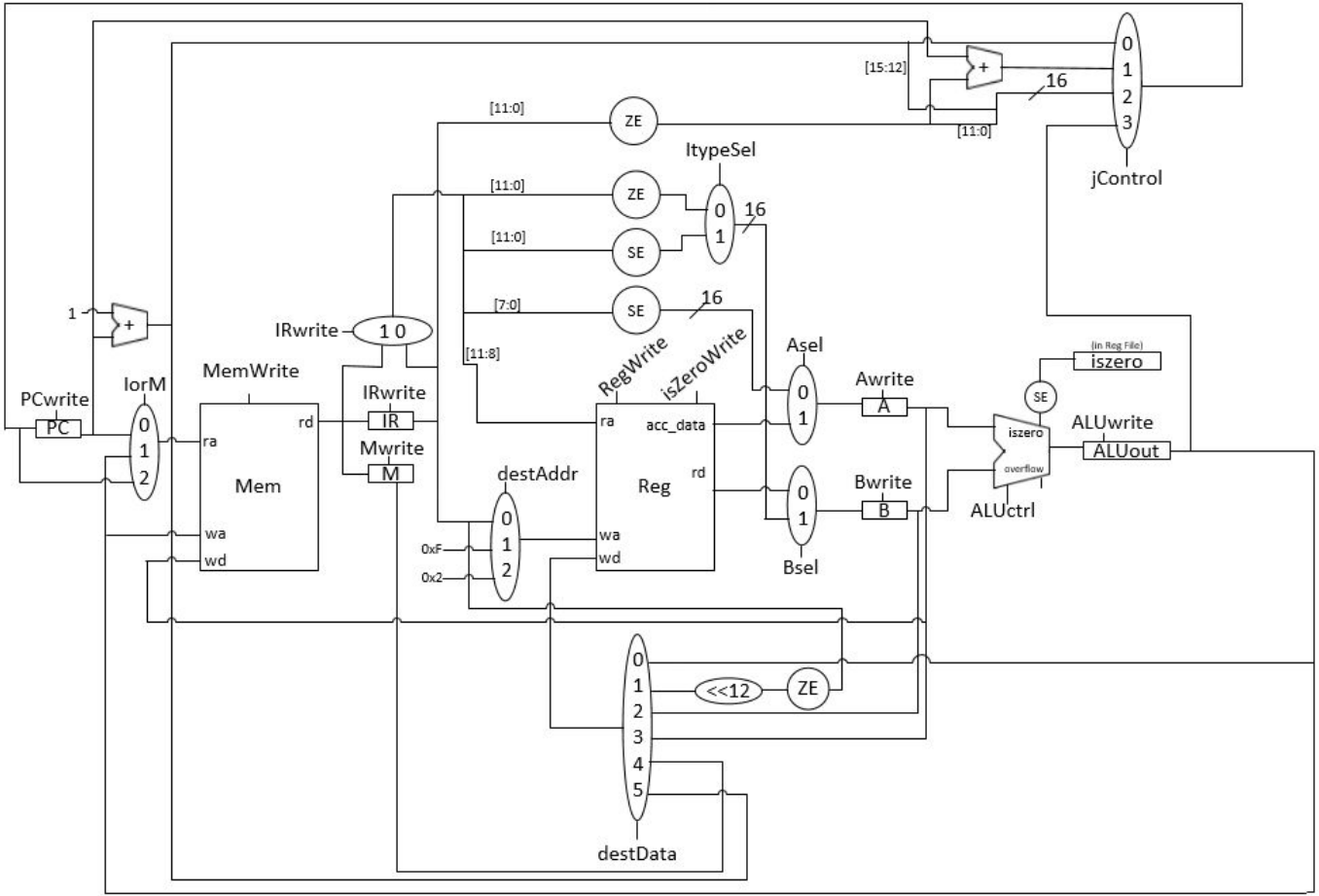
Unique Aspects

Destination Control

- Results of all instructions involving multiple registers can be stored in either the accumulator register or a target register using a single bit in the instruction
- Focused on moving data between registers as efficiently as possible

Branch Control

- Jump instructions used for branches are based on the most significant bit of the accumulator register
- Allows for very fast and flexible branches and loop control


[15:12]
+
16
[11:0]
0
1
2
3
jControl
[11:0]
ZE
ItypeSel
[11:0]
ZE
0
1
16
[11:0]
SE
[7:0]
SE
16
1
+
IRwrite
1 0
[11:8]
RegWrite
isZeroWrite
Asel
(in Reg File)
iszero
PCwrite
PC
IorM
0
1
2
MemWrite
ra
rd
Mem
wa
wd
IRwrite
IR
Mwrite
M
destAddr
0xF
0x2
0
1
2
ra
acc_data
Reg
rd
wa
wd
0
1
Bsel
Awrite
A
Bwrite
B
SE
iszero
overflow
ALUctrl
ALUwrite
ALUout
0
1
2
3
4
5
<<12
ZE
destData

Datapath

Preferred Changes

1. Improve efficiency of Control Unit
2. Only use one ALU for all operations
3. Implement Pipelining

Challenging & Interesting Aspects

Control Unit Timing

The most difficult aspect of debugging the processor was ensuring the control signals appeared on the right cycle alongside the right memory data

Memory Delay

In order to overcome the clock cycles required for data to appear from memory we began by double-clocking the memory but found the reduction in overall clock speed made it faster to add cycle delays instead which nearly doubled our clock speed

FPGA Implementation & Xilinx

Programming the FPGA added another learning curve and created complexity in interfacing our processor with the LCD and the input devices

Xilinx did not play well with SVN or long file names

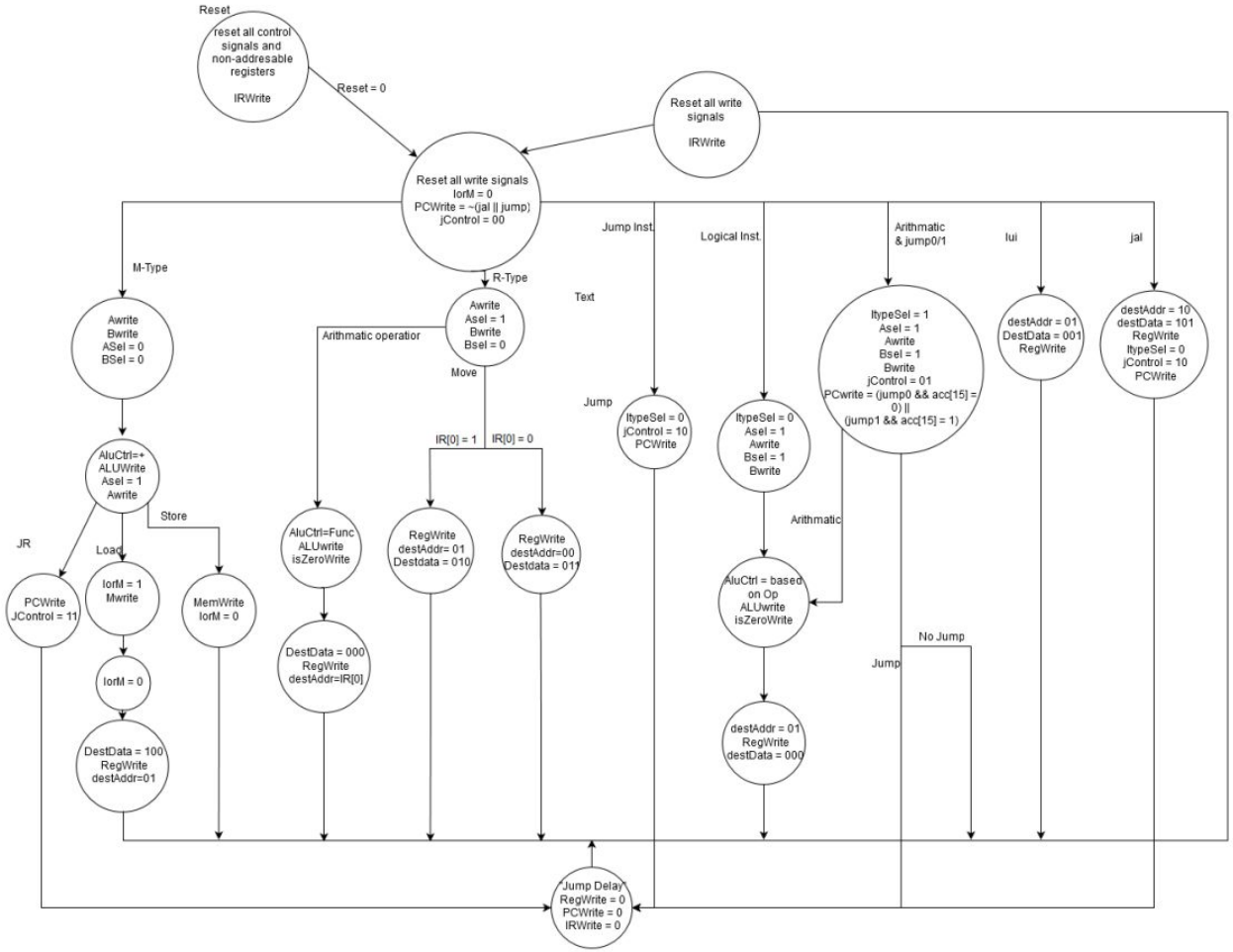
Performance Data

Number of Memory Bytes required: 128+ 6 = 134
(Program) (stack)

When n = 0x 13B0 :

- Total Number of Instructions: 102,111
- Total Number of cycles: 408,458
- Cycle time for Design:
  - 10.669ns
  - 93.733MHz
- Total Execution Time:
  - CPI x Cycle Time x # inst = 4.3 ms

Control Unit



FPGA Board Demo