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EELE 317

April 22, 2025

BJT Amplifier

Purpose

A single stage BJT amplifier was designed, simulated, and built. The goal was to verify compliance with the given specifications.

Specifications

- +/- 12 Volt Power Supply
- Voltage Gain: 20 +/- 10% V/V
- Maximum Output Voltage: >= 1 V_{PP}
- Frequency Range: 1 kHz - 500 kHz
- Load Resistance: 10 kΩ
- Input Resistance: 20 kΩ
- Maximum Power Dissipation: 20 mW
- Specifications Met Over: 0-70°C

Circuit Performance Specifications

	Output Gain (Typical)	Input Impedance (Typical)	Power Dissipation	Frequency Range
Required	18 - 22 V/V	20 kΩ	<= 20 mW	1 kHz - 500 kHz
Simulated	19.4 V/V	23.14 kΩ	9.6 mW	54.8 Hz - 2.9 MHz
Measured	21.6 V/V	26.7 kΩ	2.61 mW	100 Hz - 500 kHz

Table 1: Typical Specifications Comparison

	Typical	Min	Max
A_V	19.4 V/V	17.9 V/V	19.5 V/V
R_i	23.14 kΩ	18 kΩ	25.98 kΩ
P_O	9.6 mW		
f_L-f_H	54.8 Hz - 2.9 MHz		

Table 2:Simulated Specifications over Temperature

Circuit Design

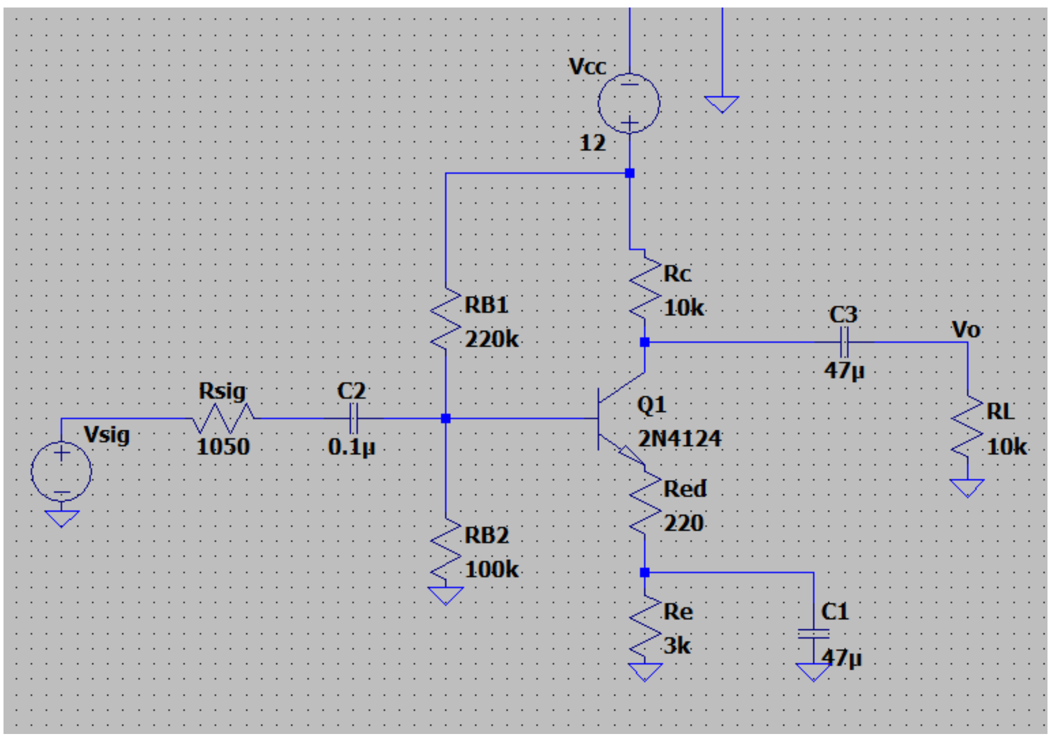


Figure 1: Circuit Schematic

Theory of Operation

The circuit uses a common emitter configuration with degeneration and a voltage divider at base. DC bias current was set at 1 mA, as power output was estimated to be 20 mW if I_C was

1.67 mA, while a current of at least 0.1 mA was needed in order to have a voltage output of 1 V_{pp}. The voltage supply was set to +12 V on the V_{CC} while V_{EE} was grounded, in order to provide flexibility in ensuring the BJT would stay active with a large collector voltage.

Using the chosen value I_C, transistor characteristics were found. With these values, the range A_V could fluctuate over and the resistance range that R_{in} could fluctuate over were determined. R_{ED} was arbitrarily set to 220 Ω, then the value's effectiveness was later verified. The following equations were used to set gain:

$A_{V\ Min} = -\alpha(R_{in}/(R_{in} + R_{sig}))(R_O/(r_e + R_{ED}))$, where $R_{in} = (h_{fe,\ min} + 1)(r_e + R_{ED}) \parallel R_{B1} \parallel R_{B2}$

$A_{V\ Max} = (R_O/(r_e + R_{ED}))$

It was found that the output resistance had to be at least 4.7 kΩ, but could not be more than 5.4 kΩ. Output resistance is described as:

$$R_o = R_C \parallel R_L \parallel r_o$$

Assuming a r_o of 111 kΩ, this would make R_C equal 10 kΩ, if a reasonable lower range R_C value is used.

Additionally, for the BJT to remain active, the base voltage had to be larger than the emitter voltage. As, $V_B = V_E + 0.7$, V_B was set to 3.92 V by arbitrarily setting R_E to 3 kΩ. As R_{in} needs to be at least 20 kΩ while V_B would be a voltage divider, so it was found that R_{B1} had to be at least 174.8 kΩ whilst R_{B2} was to be at least 94.8 kΩ. R_{B1} was chosen to be set to 220 kΩ while R_{B2} was chosen to be set at 100 kΩ.

For meeting the frequency range requirements, the capacitor values were adjusted. capacitors of larger values, 47 uF, were chosen for C_1 and C_3 in order to make C_2 the designable aspect, using dominant approximation. It was found that the frequency of 1 kHz or less could be achieved with a capacitor greater than or equal to 45.9 nF. A 0.1 uF capacitor was chosen for C_2, as it was larger than that minimum but two orders of magnitude smaller than C_1 and C_3. Lastly, the high frequency response was verified and found to meet specifications as long as the input resistance was high enough.

Spice Simulation Results

The amplifier was then simulated in LTSpice, using R_{sig} of 1050 Ω. Power output was calculated by determining the power dissipation over R_{ed}, R_E, and R_C resistors, and was found to be 9.556 mW. To determine the R_{in}, the peak current over R_{sig} was found using time domain analysis, and R_{in} was considered a voltage divider with peak V_{sig} and R_{in}. This resulted in a typical R_{in} of 23.14 kΩ. The gain vs. frequency was plotted from 1 Hz to 5 MHz, and over the temperatures 0°, 25°, and 70°. It was found that the gain was within specification over the desired frequency range. At 70°, the behavior was less than desired, though, it was close to the specified range.

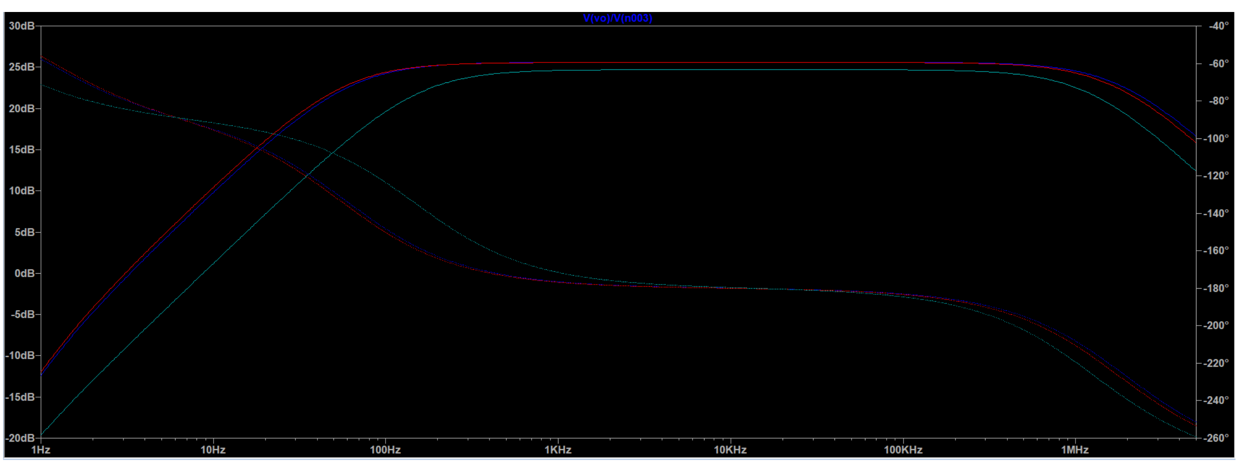


Figure 2: SPICE gain vs frequency plot

Then it was verified that the output could drive at least 1 V_{pp} by setting V_{in} to a sine wave of $0.06V_{pp}$, which resulted in roughly 1.1 V_{pp}.

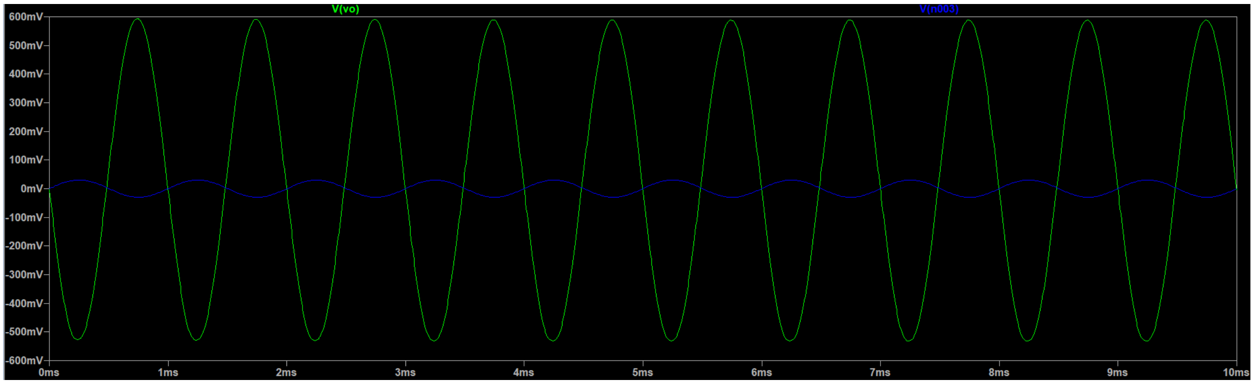


Figure 3: V_O in time domain

Measured Circuit Performance

The circuit was then built in the lab. R_C was slightly reduced to 4.4 kΩ in order to meet the gain specifications. A smaller than expected r_o could explain the need to reduce R_C, and adjusting the value of R_C would only significantly impact A_V, and additionally, r_o only impacts R_C for design purposes. After adjusting this resistor, an oscilloscope was used to measure the voltage gain over 100 Hz to 1 MHz while V_{sig} was set at 50 mV_{pp}.

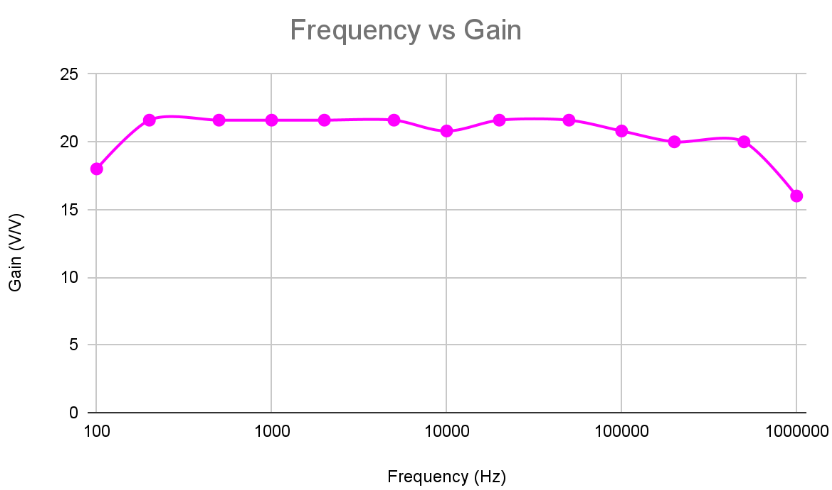


Figure 4: Frequency vs Gain

The input resistance was then measured by finding the voltage drop and current over R_{sig} and comparing it to V_{sig} in order to find R_{in}. R_{in} was found to be 26.7 kΩ. Then the power dissipation was calculated by using the known resistor values and the voltage drop over the resistors in the circuit. By adding up all the power dissipation of the resistors, a total power dissipation of 2.61 mW was found.

Conclusion

Through the process of analyzing and building the circuit, a circuit was developed that successfully met specifications. The voltage gain of the amplifier was found to be within the required range, with a measured value of 21.6 V/V, slightly exceeding the target of 20 V/V. The input resistance was above the minimum 20 kΩ, having measured 26.7 kΩ. Additionally, the amplifier demonstrated output voltages over 1 V_{pp} and maintained gain over the frequency rage 100 Hz - 500 kHz. Lastly, power dissipation was found to be only 2.61 mW. The circuit mostly showed stability across temperature range, though the performance was impacted at higher temperatures due to some variation in the h_{fe} at I_C.

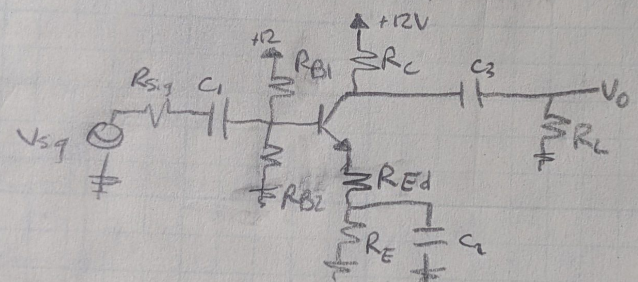
Appendix

The following pages are attached:

- Written Design Process
- 2N4124 DataSheet

- +12V & −12V power supplies.
- 2N4124 npn BJT: $120 \le \beta_{ac} \le 480$ & $120 \le \beta_{dc} \le 360$ at $T = 25°$ & $I_C = 2mA$
- Voltage Gain: $A_V = 20 \pm 10\% \; [\frac{V}{V}]$
- Max $V_{out} \ge 1V_{pp}$
- Frequency Range: 1kHz − 500kHz
- Load resistance $R_L = 10k\Omega$
- Input Resistance: $R_{in} \ge 20k\Omega$
- $P_o = 20mW$ max
- Must be met over 0 − 70°C.

The above specifications must be made for a BJT amplifier:



AC:

$R_o = R_C \| R_L \| r_o$

$R_i = (\beta+1)(r_e) \| (R_{B1} \| R_{B2}) \ge 20k\Omega$

$$A_V = -\alpha\left(\frac{R_i}{R_i + R_{sig}}\right)\left(\frac{R_o}{r_e + R_{E_o}}\right)$$

$-18 \le A_V \le -22$

DC:

$r_e = \frac{1}{g_m} = \frac{V_T}{I_C}$

$r_o = \frac{V_A}{I_C}$, $V_A \approx 207.5$ (From Lab 6)

$V_B = 12\left(\frac{R_{B2}}{R_{B2} + R_{B1}}\right)$

Min: $-18 = -\frac{120}{121}\left(\frac{20k\Omega}{21k\Omega}\right)\left(\frac{R_o}{r_e + R_{Ed}}\right)$, $\beta_{ac} = 120$

$R_o = R_C \| R_L \| R_o = -18\left(\frac{121}{120}\right)\left(\frac{21}{20}\right)(245)$

$R_C > 9.5k\Omega$

Max: $22 \le \frac{R_o}{r_e + R_{Ed}}$

$R_C \le 13.1k\Omega$

$\boxed{R_C = 10k\Omega}$ $\boxed{R_{Ed} = 220\,\Omega}$

Let $I_C = 1mA$

$r_e = 25$
$g_m = 0.04$
$r_o = 111k\Omega$

Power $\approx (12V)(I_C) \le 20mW$

$I_C \le 1.67\,mA$

$$1mA = \frac{V_B - 0.7}{R_{Ed} + R_E} = \frac{12 - V_C}{R_C}$$

$V_C = 2V$, for $\boxed{R_E = 3.0k}$

$\frac{R_{B2}}{R_{B2} + R_{B1}} \approx 0.32$: $V_B = 3.75$, $V_E = 3.05$

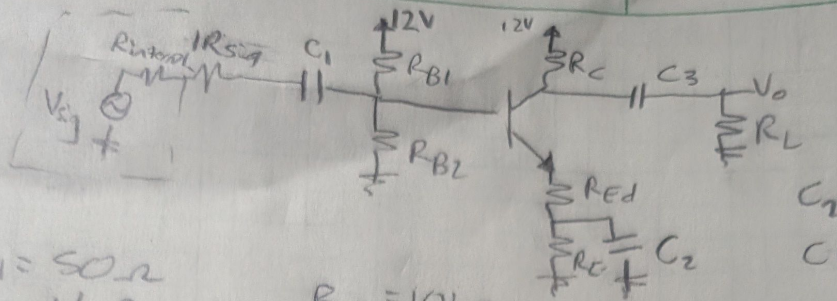
$20k = R_{B1} \| R_{B2} \| 20(245)$

$R_{B1} \ge 174.80k\Omega$ = 220k

$R_{B2} \ge 94.82k\Omega$ = 100k

$I_c = 2mA$ $\leq \beta_{ac} \leq 480$ & $120 \leq \beta_{ac}$

$\pm 10\%$ [V/V]



$C_2 \& C_3 = 330\mu F$

$C_1 = 0.047\mu F$

$R_{internal} = 50\Omega$

$R_{sig} = 1k\Omega$

$R_{B1} = 220k\Omega$

$R_{B2} = 100k\Omega$

$R_C = 10k\Omega$

$R_{Ed} = 220\Omega$

$R_E = 3k\Omega$

$R_L = 10k\Omega$

Low Frequency:

much larger

$$f_L \approx \frac{1}{R_{in}'C_1} + \frac{1}{(R_{E}\|R_{Z})C_2} + \frac{1}{R_{out}C_3}$$

$R_{out} =$

$$R_{in}' = R_{internal} + R_{sig} + (R_{B1} \| R_{B2} \| (\beta+1)(R_{Ed} + r_e))$$

For $\beta = 120$: $R_{in}' \geq 21763.387$

$$1kHz \geq \frac{1}{R_{in}'C_1}$$

$C_1 \geq 45.9\ nF$

~~$C_3 \& = 1\mu F$~~

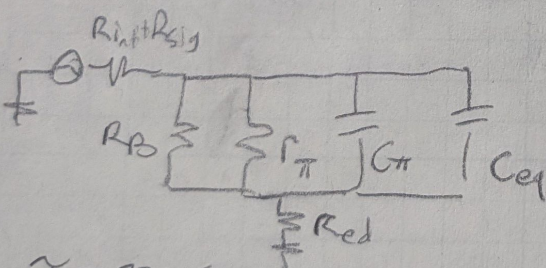
C_2 large, $= \boxed{330\mu F}$

$\boxed{C_1 = 0.147\mu F}$

High Frequency:

$$A_M = K = \frac{R_L'}{r_e + R_{Ed}} = \left(\frac{1}{245}\right)(R_C \| R_L \| R_o)$$

$K = 19.5$



$C_{eq} = C_\mu(1+K)$

$C_{eq} = 4pF(19.5)$

$C_{in} = 17.4pF + 82.116pF = 99.52\ pF$

$$f_H = \frac{1}{R_{sig}'C_{in}}$$

$\tau = 235ps$

For $I_C = 1mA$

$C_\pi = 17.4pF$, $C_\mu = 4pF$

$C_{je} = 8pF$

$R_{sig}' \geq 21763.387$

$f_H \approx 500kHz$

When simulated, adjustments were made.
All values good, but $R_c = 5.1k$

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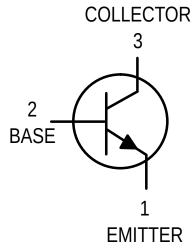
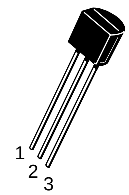
General Purpose Transistors

NPN Silicon

2N4123
2N4124





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	2N4123	2N4124	Unit
Collector–Emitter Voltage	V_{CEO}	30	25	Vdc
Collector–Base Voltage	V_{CBO}	40	30	Vdc
Emitter–Base Voltage	V_{EBO}	5.0		Vdc
Collector Current — Continuous	I_C	200		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_E = 0)	 2N4123 2N4124	$V_{(BR)CEO}$	 30 25	 — —	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	 2N4123 2N4124	$V_{(BR)CBO}$	 40 30	 — —	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 20 Vdc, I_E = 0)		I_{CBO}	—	50	nAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	—	50	nAdc

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			—
(I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc)	2N4123		50	150	
	2N4124		120	360	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N4123		25	—	
	2N4124		60	—	
Collector–Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	—	0.3	Vdc
Base–Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	—	0.95	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123		250	—	
	2N4124		300	—	
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	8.0	pF
Collector–Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 1.0 MHz)		C_{cb}	—	4.0	pF
Small–Signal Current Gain		h_{fe}			—
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 10 k ohm, f = 1.0 kHz)	2N4123		50	200	
	2N4124		120	480	
Current Gain — High Frequency		$\|h_{fe}\|$			—
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123		2.5	—	
	2N4124		3.0	—	
(I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	2N4123		50	200	
(I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	2N4124		120	480	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm,	2N4123		—	6.0	
f = 1.0 kHz)	2N4124		—	5.0	

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

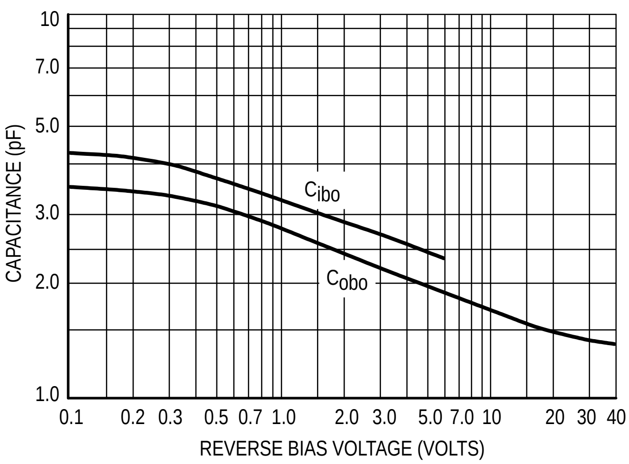


Figure 1. Capacitance

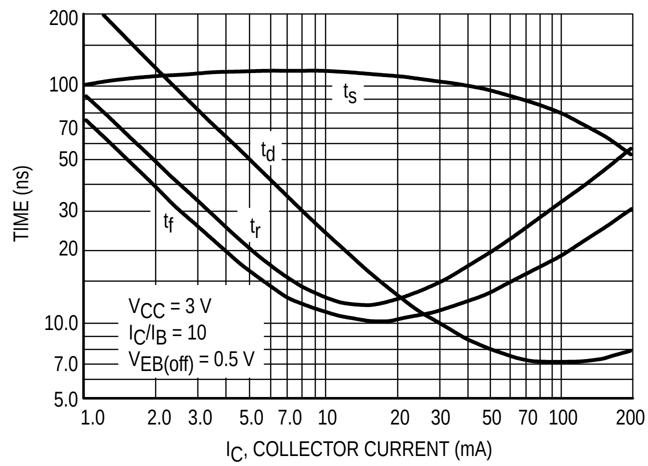


Figure 2. Switching Times

AUDIO SMALL–SIGNAL CHARACTERISTICS

NOISE FIGURE

(V_{CE} = 5 Vdc, T_A = 25°C)
Bandwidth = 1.0 Hz

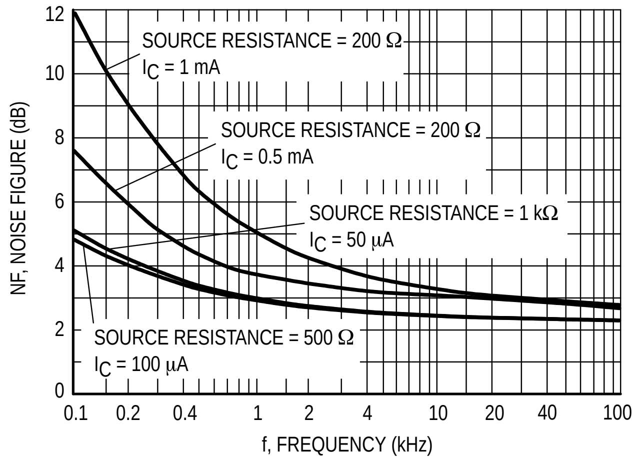


Figure 3. Frequency Variations

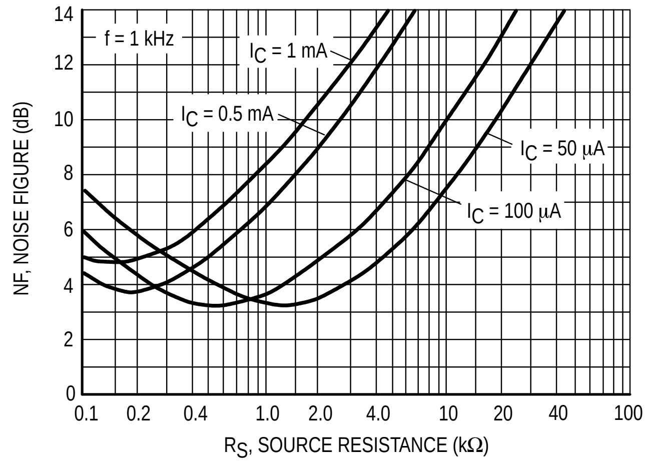


Figure 4. Source Resistance

h PARAMETERS

(V_{CE} = 10 V, f = 1 kHz, T_A = 25°C)

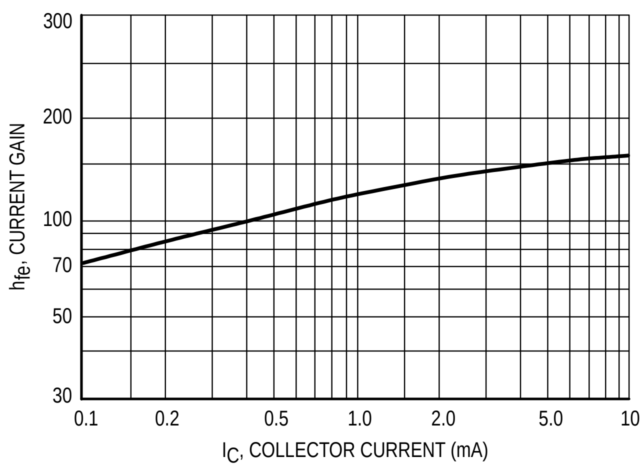


Figure 5. Current Gain

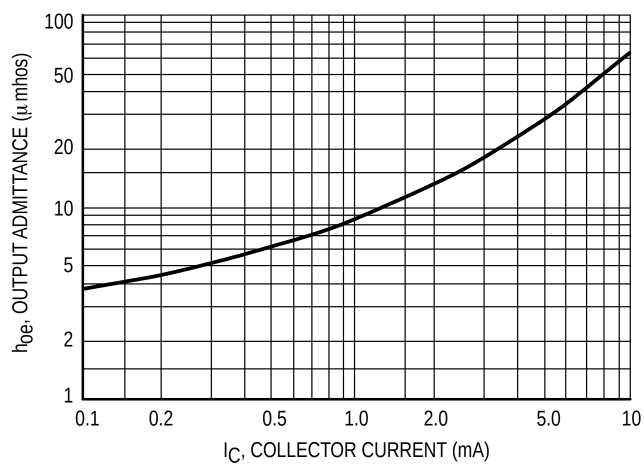


Figure 6. Output Admittance

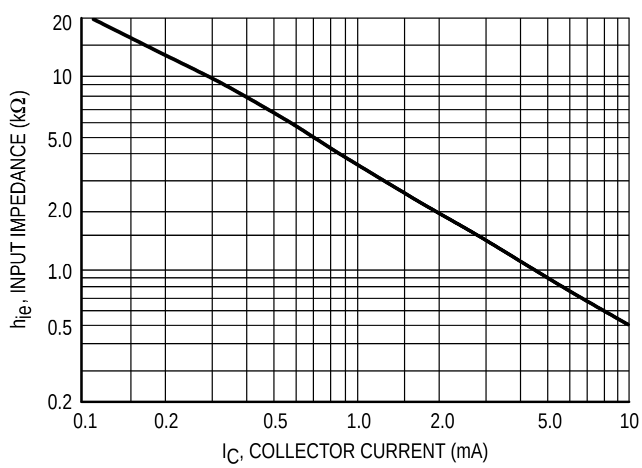


Figure 7. Input Impedance

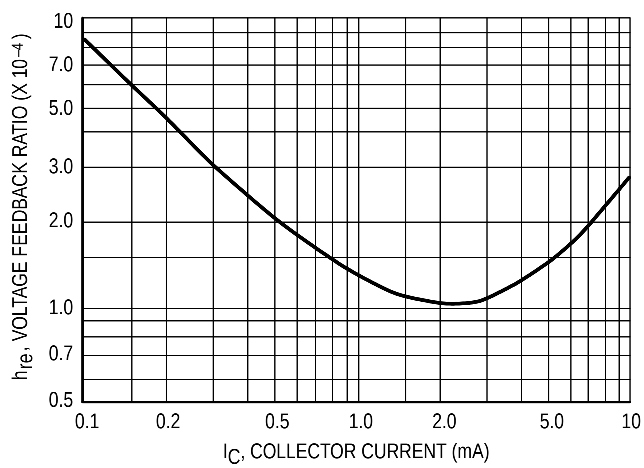


Figure 8. Voltage Feedback Ratio

STATIC CHARACTERISTICS

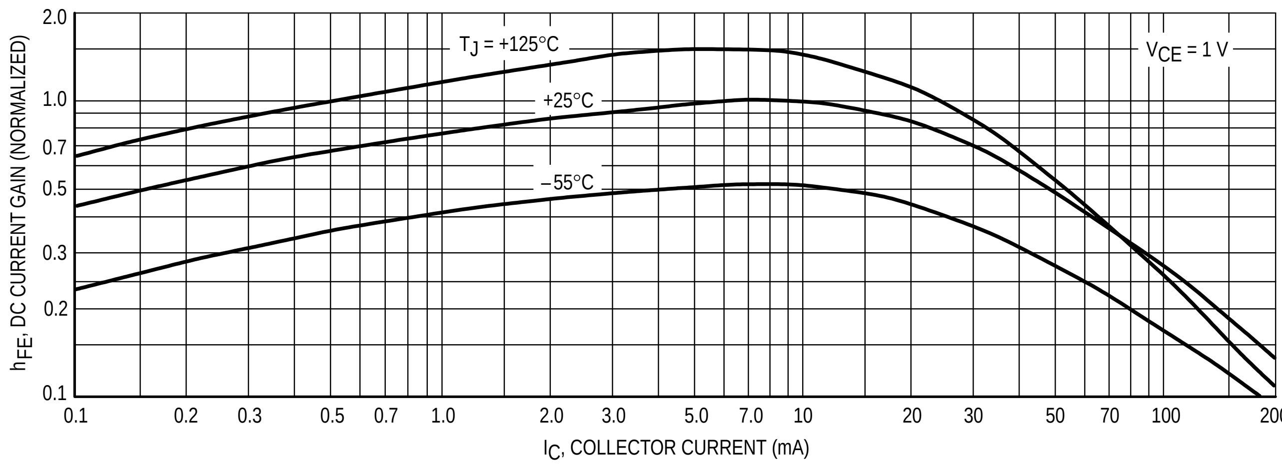


Figure 9. DC Current Gain

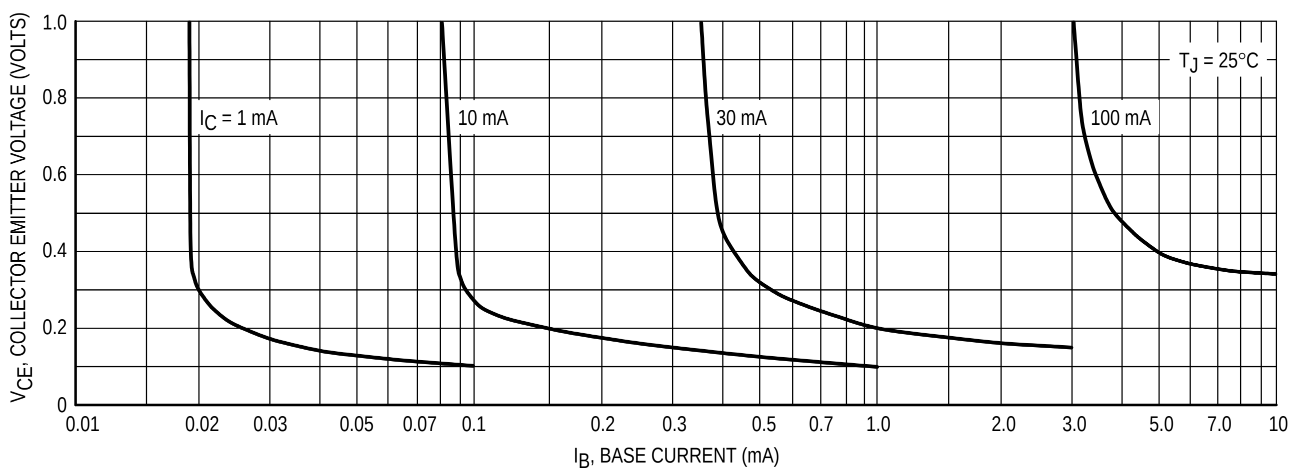


Figure 10. Collector Saturation Region

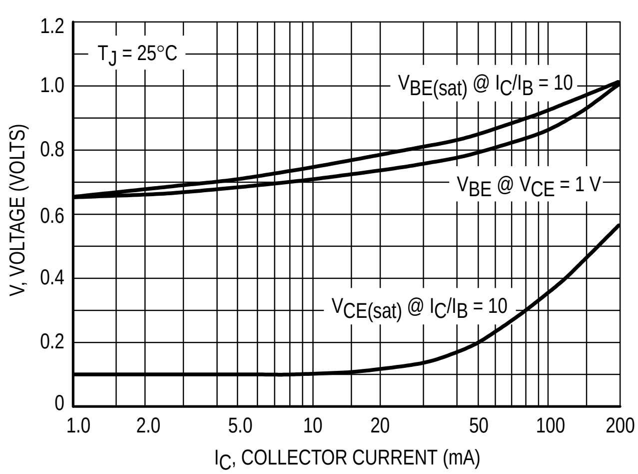


Figure 11. “On” Voltages

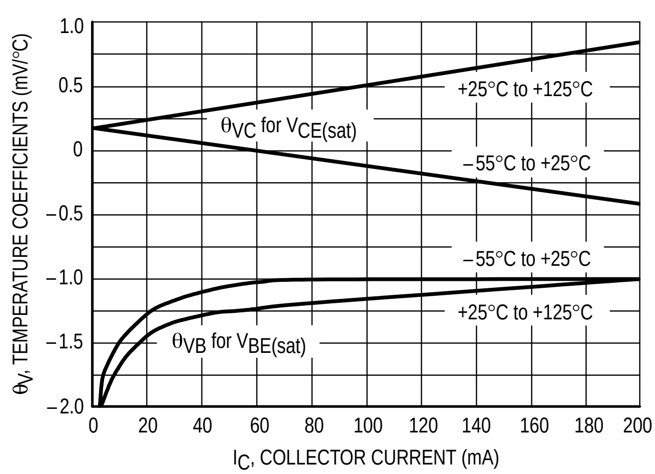
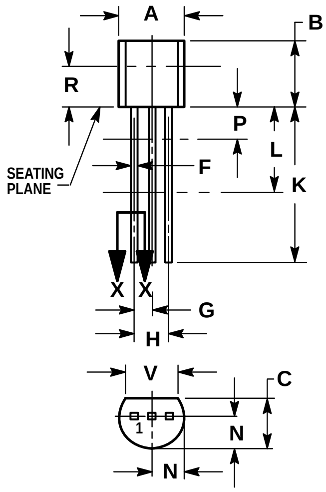
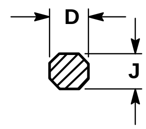


Figure 12. Temperature Coefficients

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

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