Chapter 2 Exercises

2.3 [5] $\langle 2.2 \rangle$ For the following C statement, write the corresponding RISC-V assembly code. Assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively.

```
B[8] = A[i-j];
```

RISC-V Translation:

```
sub x5 x28, x29  # f = i - j
slli x5, x5, 2  # f = f << 2  (f = f * 4)
add x6, x10, x5  # g = &A[i-j]
lw x6, 0(x6)  # g = A[i-j]
sw x6, 32(x11)  # B[8] = A[i-j]  (8 * 4 = 32)</pre>
```

2.7 [5] $\langle 2.2, 2.3 \rangle$ Translate the following C code to RISC-V. Assume that the variables f, g, h, i, and j are assigned to registers x5, x6, x7, x28, and x29, respectively. Assume that the base address of the arrays A and B are in registers x10 and x11, respectively. Assume that the elements of the arrays A and B are 8-byte words:

```
B[8] = A[i] + A[j];
```

RISC-V Translation:

```
\# i = i << 2
slli x28, x28, 2
add x5, x10, x28
                     # f = &A[i]
1 w x5, 0(x5)
                     # f = A[i]
slli x29, x29, 2
                     # j = j << 2
add x6, x10, x29
                     \# g = \&A[j]
1 w x6. 0(x6)
                     \# g = A[j]
add x7, x5, x6
                     # h = f + g
sw x7, 32(x11)
                     # B[8] = h
```

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2.13 [5] (2.5) Provide the instruction type and hexadecimal representation for the following instruction:

```
sw x5, 32(x30)
```

Instruction format S.

0000001 00101 11110 010 00000 0100011_{two} $\Rightarrow 25F2023_{\text{hex}}$