

## Lab 4: Design a Parking Meter

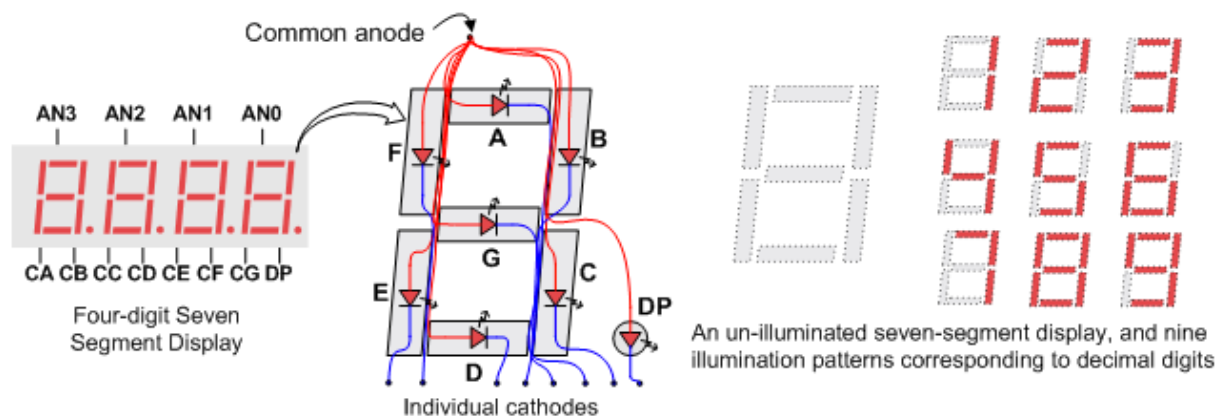
### I. Introduction

In this lab, we build a finite state machine (FSM) that models a parking meter that is fed coins and displays the correct timing left on the meter, represented by a four digits each modeled in a seven segment display. The segments are turned on in patterns that match the corresponding number of the time.

The inputs to the vending machine are listed as follows, with the corresponding change implemented immediately when the input is read.

Inputs	Function
add1	Add 60 seconds
add2	Add 120 seconds
add3	Add 180 seconds
add4	Add 300 seconds
rst1	Reset time to 16 seconds
rst2	Reset time to 150 seconds
clk	Frequency of 100 Hz
rst	Resets to the initial state

The output module displays the time in *hour hour : minute minute* in a four-digit display. Each digit written with seven segments as shown in the diagram below.



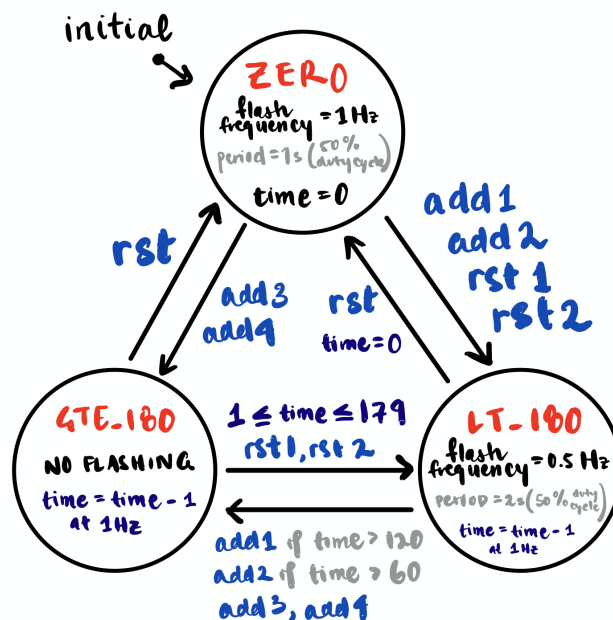
## II. Design Description

This system is written as a Verilog module called **parking\_meter.v**, which takes the seven inputs listed previously as input, mainly driven by the input clock **clk**. The module outputs **a1**, **a2**, **a3**, **a4**, which are the anode selectors for the seven segment display as shown above, with **a4** corresponding to the most significant bit **AN3** and **a1** corresponding to the least significant bit **AN0** in the above diagram. The module also outputs **led\_seg**, a 7-bit register that represents the seven segment display, the most to least significant bits represent **CA** to **CG** in the diagram. Finally, **val1**, **val2**, **val3**, **val4** are outputted, with **val1** being the LSB and **val4** the MSB.

### A. Finite State Machine

I modeled the system as the finite state machine shown below, with three distinct states:

- **ZERO**
  - Time is 0 seconds
  - Display flashes at 1Hz, i.e. period = 1s with 0.5s on and 0.5s off
  - Time stays at 0 seconds unless receives input that makes time nonzero
- **LT\_180**
  - Time is less than 180 seconds
  - Display flashes at 0.5Hz, i.e. period = 2s with 1s on and 1s off
  - Time decrements by 1 at 1Hz i.e. every second
- **GTE\_180**
  - Time is greater than or equal to 180 seconds
  - Display does not flash
  - Time decrements by 1 at 1Hz i.e. every second



The current state transitions between these three states in response to input signals and/or the time changing. All states go to **ZERO** in response to the **rst** signal and to **LT\_180** in response to **rst1** and **rst2** because these corresponding to **time = 16** seconds and **150** seconds respectively. The state transitions from the **add** signals are handled on a case by case basis depending on the current time and what the time would be after the addition. In the code, I

always handle the edge case of the time going above 9999, in which the time is set to 9999 instead of going above which is impossible to display. Lastly, changes to the time via countdown will make the current state go to the correct corresponding state.

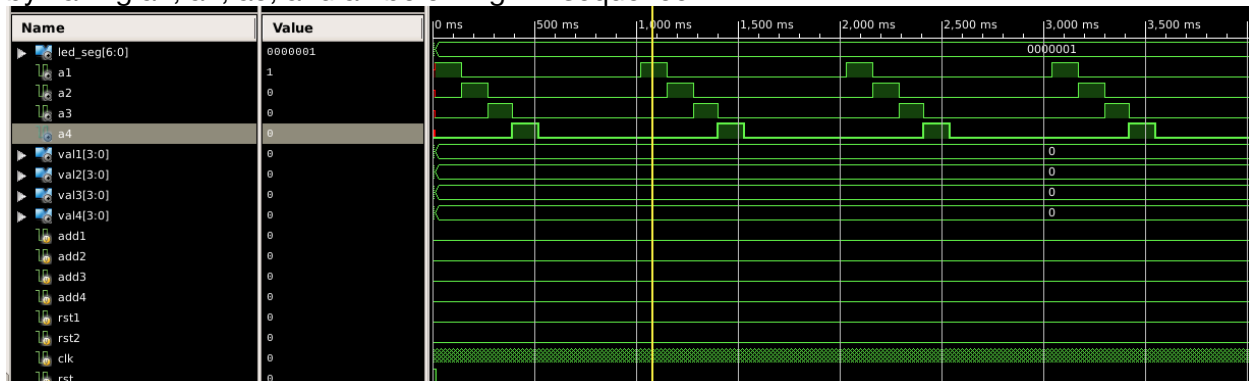
## B. Module Design

With the three states in mind, I write my model to coordinate several different aspects. I have a **current\_state** and a **next\_state** updated with changes to a data structure called **tm**, a 14 bit register keeping track of the seconds left on the meter, going up to 9999 seconds. I also have a **count\_to\_100** register that is incremented at every positive edge of input **clk**, and it is reset to 0 when it gets to 100, essentially counting 100 clk cycles since each clk cycle is 0.01 seconds, and 100 would be 1 second, which is the period between every update to the meter timer. I also use a **digit\_idx** register and a **display\_on** register, to control the outputs **a1**, **a2**, **a3**, **a4**, and **led\_seg** that compose the seven-segment display. The outputs **val1**, **val2**, **val3**, **val4** show the meter time in binary coded decimal from least to most significant digit, read from division and modulo operations on the value of **tm**.

## III. Simulation Tests

### Test 1: Flash Zero

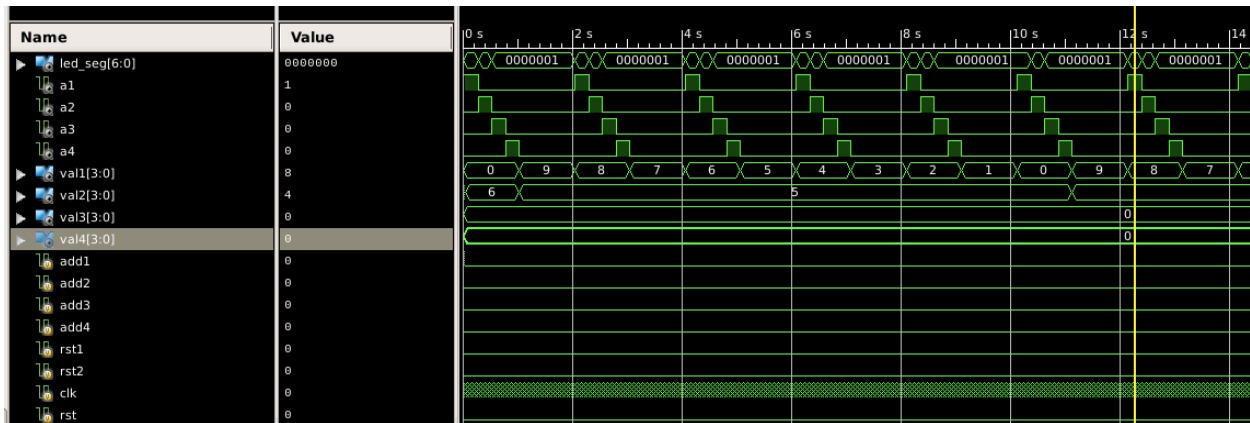
The first and simplest test case is to see if the parking meter correctly flashes when it is in its initial state ZERO. We see that val1, val2, val3, and val4 correctly hold the value 0 the entire time, and led\_seg has the illumination pattern corresponding to 0, with only the G segment holding 1. We also see each cycle is 1 second long, of which the first 0.5 second flashes 0000 by having a1, a2, a3, and a4 be on high in sequence.



### Test 2: Count Down from 60

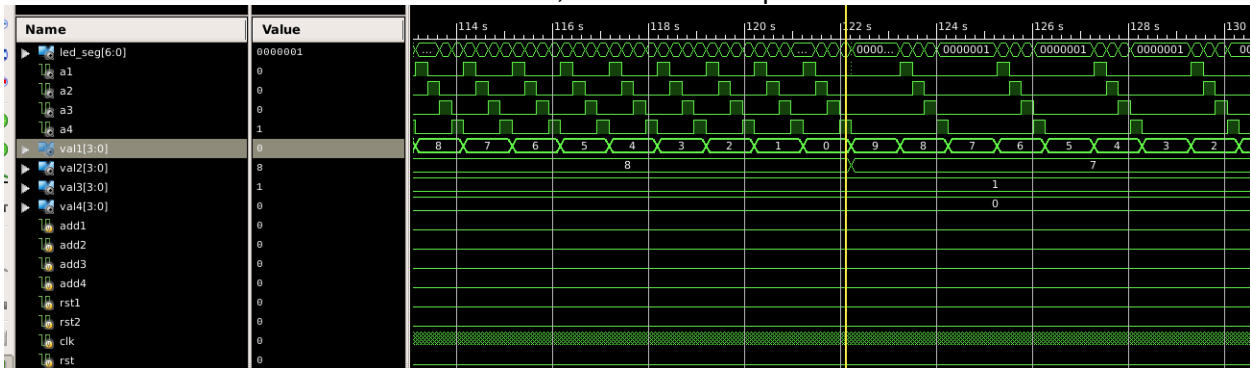
Here, add1 high for one clock cycle so that the time goes from 0 to 60 seconds. We observe the time shown by val1, val2, val3, val4 decrease by 1 per second. Within this second, the first 0.5 second has the display on (when the time value is even) with a1, a2, a3, a4 sequentially high and corresponding to correct hardcoded values for seven-segment display led\_seg. The second 0.5 second of each 1 second cycle has a1, a2, a3, a4 all low since the display is off.

For example, when the time is 48, val4=0, val3=0, val2=4, val1=8, and led\_seg holds the value for 8 for the first 0.25 seconds, 4 for the second 0.25 seconds, and 0 for the last half of the active second.



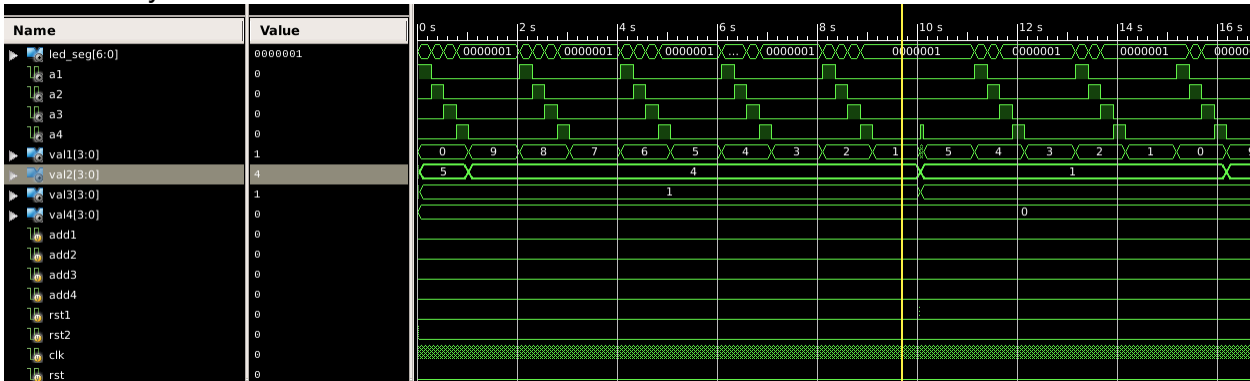
### Test 3: Count Down from 300

Here we test the switch from above 180 seconds to below, which is done by setting the time to 300 via add4 and seeing the time decrease by 1 per second, with a1, a2, a3, a4 being continually cycled through as there is no flashing and therefore no time where the display is not showing. When the time goes from 180 to 179 seconds, we see that the display is off for odd valued times and on for even valued times, as seen in the previous test case.



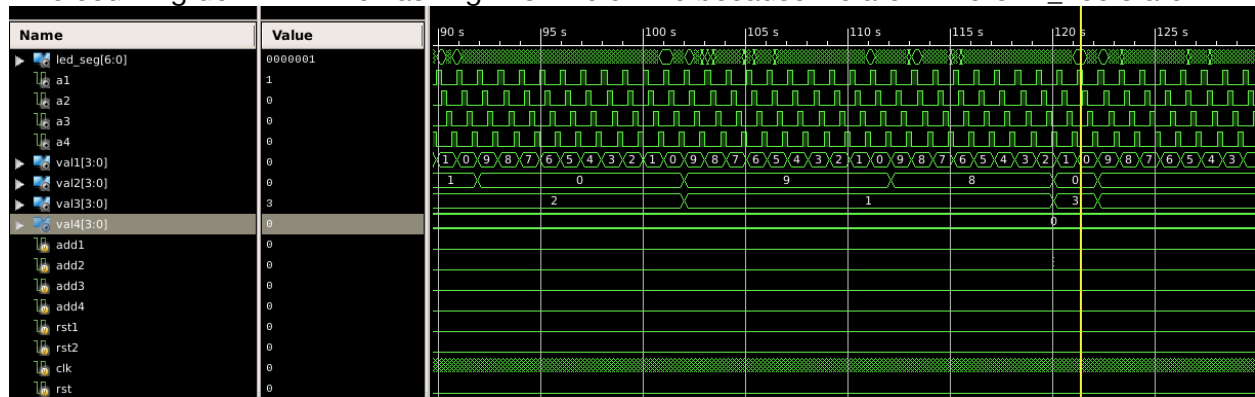
### Test 4: Reset to 16 and Reset to 150

Here we test the rst1 and rst2 inputs. First the rst2 input signal is set to high to make the time go to 150, which it does and begins to count down by 1 every second. After 10 seconds, the rst1 input signal is set to high to make the time go to 16 where begins to count down immediately.



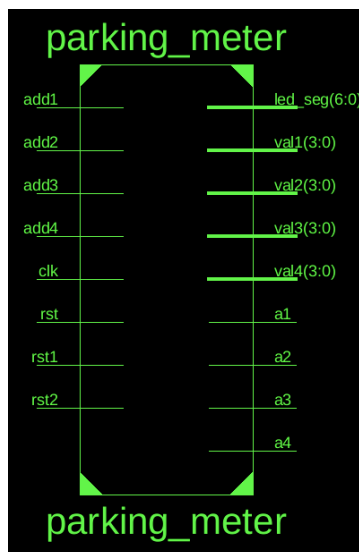
### Test 5: Press add4 and add2 (given in Spec)

Here we go through the test case provided in the spec, in which add4 is pressed making the time go to 300, before counting down to 180 when add2 is then pressed to make the time to back up to 300. Here we see the time go back up to 300 at this second button press and the time counting down with no flashing this whole time because we are in the GTE\_180 state.



## IV. Schematics

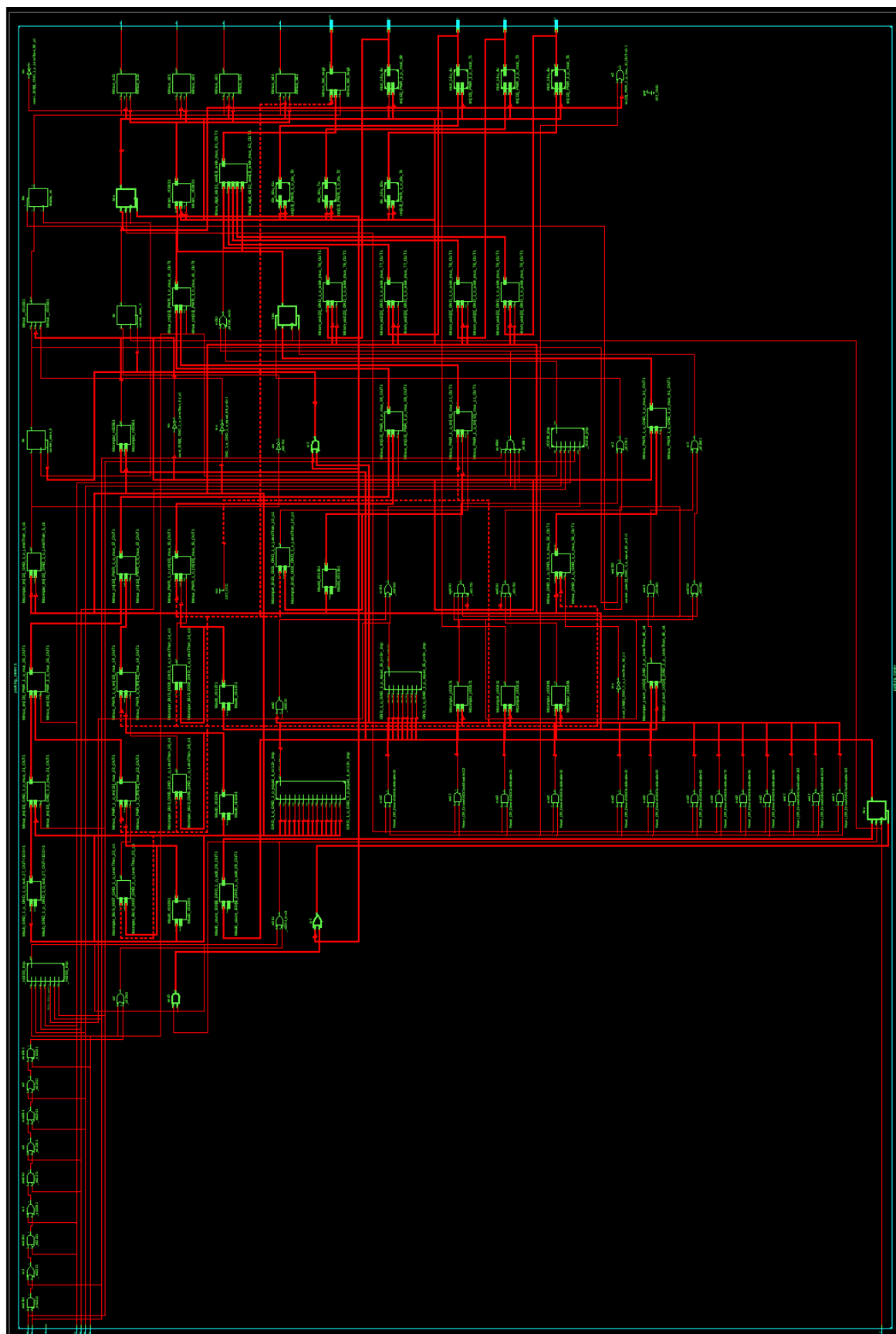
The top module parking\_meter is as shown:



The generated RTL schematic is as shown on the following page and rotated at a 90 degree angle to be able to be enlarged. Briefly, we see some of the vertically long rectangles with many inputs corresponding to blocks taking in all bits of important large registers like tm and count\_100 which control many different functions of the module. On the right, we see multiplexers outputting the final output values including a1, a2, a3, a4, and led\_seg.

## V. Design Summary

Attached at the end of the report are the design summary part of the synthesis report, the summary of the implementation (map) report, and the design summary. We see 6% of MUX's used and 8% of lookup tables used, all of which are used for logic and not memory.



## A. Design Summary of Synthesis Report

```
=====
*                               Design Summary                               *
=====
```

Top Level Output File Name : parking\_meter.ngc

Primitive and Black Box Usage:

```
-----
# BELS : 1293
# GND : 1
# INV : 33
# LUT1 : 28
# LUT2 : 22
# LUT3 : 128
# LUT4 : 86
# LUT5 : 194
# LUT6 : 301
# MUXCY : 232
# MUXF7 : 20
# VCC : 1
# XORCY : 247
# FlipFlops/Latches : 37
# FDR : 4
# FDRE : 32
# FDS : 1
# Clock Buffers : 1
# BUFGP : 1
# IO Buffers : 34
# IBUF : 7
# OBUF : 27
```

Device utilization summary:

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Selected Device : 6slx16csg324-3

Slice Logic Utilization:

Number of Slice Registers:	37	out of	18224	0%
Number of Slice LUTs:	792	out of	9112	8%
Number used as Logic:	792	out of	9112	8%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	799			
Number with an unused Flip Flop:	762	out of	799	95%
Number with an unused LUT:	7	out of	799	0%
Number of fully used LUT-FF pairs:	30	out of	799	3%
Number of unique control sets:	6			

IO Utilization:

Number of IOs:	35			
Number of bonded IOBs:	35	out of	232	15%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs:	1	out of	16	6%
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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.  
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT  
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal	Clock buffer(FF name)	Load
clk	BUFGP	37

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 6.002ns (Maximum Frequency: 166.613MHz)  
Minimum input arrival time before clock: 6.216ns  
Maximum output required time after clock: 34.801ns  
Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'  
Clock period: 6.002ns (frequency: 166.613MHz)  
Total number of paths / destination ports: 9859 / 74

-----

Delay: 6.002ns (Levels of Logic = 8)

Source: tm\_2 (FF)  
Destination: tm\_0 (FF)  
Source Clock: clk rising  
Destination Clock: clk rising

Data Path: tm\_2 to tm\_0

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDRE:C->Q	18	0.447	1.049	tm_2 (tm_2)
INV:I->O	1	0.206	0.000	Madd_n0139_lut<2>_INV_0
(Madd_n0139_lut<2>)				
MUXCY:S->O	1	0.172	0.000	Madd_n0139_cy<2> (Madd_n0139_cy<2>)
XORCY:CI->O	3	0.180	0.879	Madd_n0139_xor<3> (n0139<3>)
LUT6:I3->O	2	0.205	0.617	BUS_0007_GND_1_o_LessThan_22_o21
(BUS_0007_GND_1_o_LessThan_22_o2)				
LUT6:I5->O	4	0.205	0.684	BUS_0007_GND_1_o_LessThan_22_o22
(BUS_0007_GND_1_o_LessThan_22_o21)				
LUT6:I5->O	1	0.205	0.000	Mmux_tm[13]_PWR_1_o_mux_41_OUT42_SW0_F
(N171)				
MUXF7:I0->O	5	0.131	0.715	Mmux_tm[13]_PWR_1_o_mux_41_OUT42_SW0
(N14)				

LUT6:I5->0	2	0.205	0.000	Mmux_tm[13]_PWR_1_o_mux_41_OUT283
(tm[13]_PWR_1_o_mux_41_OUT<9>)				
FDRE:D		0.102		tm_9
-----				
Total		6.002ns (2.058ns logic, 3.944ns route) (34.3% logic, 65.7% route)		

=====  
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'  
Total number of paths / destination ports: 670 / 91  
=====

Offset: 6.216ns (Levels of Logic = 5)  
Source: add1 (PAD)  
Destination: tm\_4 (FF)  
Destination Clock: clk rising

Data Path: add1 to tm\_4

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->0	28	1.222	1.579	add1_IBUF (add1_IBUF)
LUT5:I0->0	1	0.203	0.808	BUS_0003_GND_1_o_LessThan_14_o23_SW0
(N127)				
LUT6:I3->0	6	0.205	1.109	Mmux_tm[13]_PWR_1_o_mux_41_OUT621
(Mmux_tm[13]_PWR_1_o_mux_41_OUT62)				
LUT6:I0->0	1	0.203	0.580	Mmux_tm[13]_PWR_1_o_mux_41_OUT241
(Mmux_tm[13]_PWR_1_o_mux_41_OUT24)				
LUT6:I5->0	2	0.205	0.000	Mmux_tm[13]_PWR_1_o_mux_41_OUT244
(tm[13]_PWR_1_o_mux_41_OUT<7>)				
FDRE:D		0.102		tm_7
-----				
Total		6.216ns (2.140ns logic, 4.076ns route) (34.4% logic, 65.6% route)		

=====  
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'  
Total number of paths / destination ports: 307330239440 / 27  
=====

Offset: 34.801ns (Levels of Logic = 33)  
Source: tm\_12 (FF)  
Destination: led\_seg<3> (PAD)  
Source Clock: clk rising

Data Path: tm\_12 to led\_seg<3>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
FDRE:C->Q	49	0.447	1.762	tm_12 (tm_12)
LUT4:I1->0	5	0.205	1.059	tm[13]_PWR_1_o_mod_69/
Mmux_a[10]_a[13]_MUX_200_o11 (tm[13]_PWR_1_o_mod_69/a[10]_a[13]_MUX_200_o)				
LUT5:I0->0	13	0.203	1.297	tm[13]_PWR_1_o_mod_69/
Mmux_a[10]_a[13]_MUX_214_o11 (tm[13]_PWR_1_o_mod_69/				
Madd_a[13]_GND_2_o_add_15_OUT_Madd_lut<10>)				
LUT6:I0->0	7	0.203	0.878	tm[13]_PWR_1_o_mod_69/
BUS_0008_INV_133_o11 (tm[13]_PWR_1_o_mod_69/BUS_0008_INV_133_o)				
LUT3:I1->0	1	0.203	0.924	tm[13]_PWR_1_o_mod_69/
Mmux_a[10]_a[13]_MUX_228_o11 (tm[13]_PWR_1_o_mod_69/a[10]_a[13]_MUX_228_o)				
LUT6:I1->0	28	0.203	1.463	tm[13]_PWR_1_o_mod_69/
BUS_0009_INV_148_o1 (tm[13]_PWR_1_o_mod_69/BUS_0009_INV_148_o)				
LUT3:I0->0	1	0.205	0.827	tm[13]_PWR_1_o_mod_69/
Mmux_a[6]_a[13]_MUX_246_o11 (tm[13]_PWR_1_o_mod_69/				
Madd_a[13]_GND_2_o_add_19_OUT_Madd_lut<6>)				
LUT6:I2->0	2	0.203	0.617	tm[13]_PWR_1_o_mod_69/
BUS_0010_INV_163_o1_SW0 (N63)				

```

LUT6:I5->0          1  0.205  0.000  tm[13]_PWR_1_o_mod_69/
BUS_0010_INV_163_o1_G (N220)
MUXF7:I1->0          23  0.140  1.498  tm[13]_PWR_1_o_mod_69/
BUS_0010_INV_163_o1 (tm[13]_PWR_1_o_mod_69/BUS_0010_INV_163_o)
LUT5:I0->0           5  0.203  1.079  tm[13]_PWR_1_o_mod_69/
Mmux_a[7]_a[13]_MUX_259_o11 (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_21_OUT_Madd_lut<7>)
LUT6:I0->0           1  0.203  0.580  tm[13]_PWR_1_o_mod_69/
BUS_0011_INV_178_o2_SW0 (N71)
LUT6:I5->0           38  0.205  1.721  tm[13]_PWR_1_o_mod_69/
BUS_0011_INV_178_o2 (tm[13]_PWR_1_o_mod_69/BUS_0011_INV_178_o)
LUT5:I0->0           5  0.203  0.962  tm[13]_PWR_1_o_mod_69/
Mmux_a[5]_a[13]_MUX_275_o11 (tm[13]_PWR_1_o_mod_69/a[5]_a[13]_MUX_275_o)
LUT5:I1->0           1  0.203  0.580  tm[13]_PWR_1_o_mod_69/
BUS_0012_INV_193_o2_SW0 (N69)
LUT6:I5->0           30  0.205  1.608  tm[13]_PWR_1_o_mod_69/
BUS_0012_INV_193_o2 (tm[13]_PWR_1_o_mod_69/BUS_0012_INV_193_o)
LUT5:I0->0           3  0.203  1.015  tm[13]_PWR_1_o_mod_69/
Mmux_a[11]_a[13]_MUX_283_o11 (tm[13]_PWR_1_o_mod_69/a[11]_a[13]_MUX_283_o)
LUT6:I0->0           1  0.203  0.684  tm[13]_PWR_1_o_mod_69/
BUS_0013_INV_208_o2_SW0 (N67)
LUT6:I4->0           25  0.203  1.537  tm[13]_PWR_1_o_mod_69/
BUS_0013_INV_208_o2 (tm[13]_PWR_1_o_mod_69/BUS_0013_INV_208_o)
LUT5:I0->0           2  0.203  0.616  tm[13]_PWR_1_o_mod_69/
Mmux_a[0]_a[13]_MUX_308_o131 (tm[13]_PWR_1_o_mod_69/a[3]_a[13]_MUX_305_o)
MUXCY:DI->0           1  0.145  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<3> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<3>)
MUXCY:CI->0           1  0.019  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<4> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<4>)
MUXCY:CI->0           1  0.019  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<5> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<5>)
MUXCY:CI->0           1  0.019  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<6> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<6>)
MUXCY:CI->0           1  0.019  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<7> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<7>)
MUXCY:CI->0           1  0.019  0.000  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<8> (tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_cy<8>)
XORCY:CI->0           1  0.180  0.944  tm[13]_PWR_1_o_mod_69/
Madd_a[13]_GND_2_o_add_27_OUT_Madd_xor<9> (tm[13]_PWR_1_o_mod_69/
a[13]_GND_2_o_add_27_OUT<9>)
LUT6:I0->0           1  0.203  0.924  tm[13]_PWR_1_o_mod_69/
BUS_0015_INV_238_o25 (tm[13]_PWR_1_o_mod_69/BUS_0015_INV_238_o24)
LUT5:I0->0           2  0.203  0.721  tm[13]_PWR_1_o_mod_69/
BUS_0015_INV_238_o26_SW0 (N187)
LUT6:I4->0           4  0.203  0.684  tm[13]_PWR_1_o_mod_69/Mmux_o41
(val1_3_0BUF)
LUT3:I2->0           5  0.205  1.059  Mmux_led_seg6141 (Mmux_led_seg614)
LUT6:I1->0           2  0.203  0.721  Mmux_led_seg75 (led_seg_6_0BUF)
LUT2:I0->0           1  0.203  0.579  Mmux_led_seg46 (led_seg_3_0BUF)
0BUF:I->0             2.571  led_seg_3_0BUF (led_seg<3>)
-----
Total                  34.801ns (8.462ns logic, 26.339ns route)
                        (24.3% logic, 75.7% route)
=====

```

Cross Clock Domains Report:

Clock to Setup on destination clock clk

Source Clock	Src:Rise	Src:Fall	Src:Rise	Src:Fall
	Dest:Rise	Dest:Rise	Dest:Fall	Dest:Fall
clk	6.002			

=====

Total REAL time to Xst completion: 14.00 secs

Total CPU time to Xst completion: 12.51 secs

-->

Total memory usage is 490852 kilobytes

Number of errors : 0 ( 0 filtered)  
Number of warnings : 8 ( 0 filtered)  
Number of infos : 5 ( 0 filtered)

## B. Summary of Implementation Report

Release 14.7 Map P.20131013 (lin64)  
Xilinx Mapping Report File for Design 'parking\_meter'

### Design Information

-----  
Command Line : map -intstyle ise -p xc6slx16-csg324-3 -w -logic\_opt off -ol high -t 1 -xt 0 -register\_duplication off -r 4 -global\_opt off -mt off -ir off -pr off -lc off -power off -o parking\_meter\_map.ncd parking\_meter.ngd parking\_meter.pcf  
Target Device : xc6slx16  
Target Package : csg324  
Target Speed : -3  
Mapper Version : spartan6 -- \$Revision: 1.55 \$  
Mapped Date : Sun Mar 14 02:07:59 2021

### Design Summary

-----  
Number of errors: 0  
Number of warnings: 0  
Slice Logic Utilization:  
Number of Slice Registers: 40 out of 18,224 1%  
Number used as Flip Flops: 37  
Number used as Latches: 0  
Number used as Latch-thrus: 0  
Number used as AND/OR logics: 3  
Number of Slice LUTs: 730 out of 9,112 8%  
Number used as logic: 729 out of 9,112 8%  
Number using 06 output only: 513  
Number using 05 output only: 27  
Number using 05 and 06: 189  
Number used as ROM: 0  
Number used as Memory: 0 out of 2,176 0%  
Number used exclusively as route-thrus: 1  
Number with same-slice register load: 0  
Number with same-slice carry load: 1  
Number with other load: 0

Slice Logic Distribution:  
Number of occupied Slices: 256 out of 2,278 11%  
Number of MUXCYs used: 284 out of 4,556 6%  
Number of LUT Flip Flop pairs used: 732  
Number with an unused Flip Flop: 692 out of 732 94%  
Number with an unused LUT: 2 out of 732 1%  
Number of fully used LUT-FF pairs: 38 out of 732 5%  
Number of unique control sets: 6  
Number of slice register sites lost to control set restrictions: 27 out of 18,224 1%

A LUT Flip Flop pair for this architecture represents one LUT paired with one Flip Flop within a slice. A control set is a unique combination of clock, reset, set, and enable signals for a registered element. The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

I/O Utilization:  
Number of bonded IOBs: 35 out of 232 15%

Specific Feature Utilization:  
Number of RAMB16BWERS: 0 out of 32 0%  
Number of RAMB8BWERS: 0 out of 64 0%  
Number of BUFIO2/BUFIO2\_2CLKs: 0 out of 32 0%

Number of BUFIO2FB/BUFIO2FB_2CLKs:	0 out of	32	0%
Number of BUFG/BUFGMUXs:	1 out of	16	6%
Number used as BUFGs:	1		
Number used as BUFGMUX:	0		
Number of DCM/DCM_CLKGENs:	0 out of	4	0%
Number of ILOGIC2/ISERDES2s:	0 out of	248	0%
Number of IODELAY2/IODRP2/IODRP2_MCBs:	0 out of	248	0%
Number of OLOGIC2/OSERDES2s:	0 out of	248	0%
Number of BSCANS:	0 out of	4	0%
Number of BUFHs:	0 out of	128	0%
Number of BUFPLLs:	0 out of	8	0%
Number of BUFPLL_MCBs:	0 out of	4	0%
Number of DSP48A1s:	0 out of	32	0%
Number of ICAPs:	0 out of	1	0%
Number of MCBs:	0 out of	2	0%
Number of PCILOGICSEs:	0 out of	2	0%
Number of PLL_ADVs:	0 out of	2	0%
Number of PMVs:	0 out of	1	0%
Number of STARTUPs:	0 out of	1	0%
Number of SUSPEND_SYNCs:	0 out of	1	0%

Average Fanout of Non-Clock Nets: 4.19

Peak Memory Usage: 769 MB

Total REAL time to MAP completion: 17 secs

Total CPU time to MAP completion: 15 secs

#### Table of Contents

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- Section 6 - IOB Properties
- Section 7 - RPMs
- Section 8 - Guide Report
- Section 9 - Area Group and Partition Summary
- Section 10 - Timing Report
- Section 11 - Configuration String Information
- Section 12 - Control Set Information
- Section 13 - Utilization by Hierarchy

#### Section 1 - Errors

#### Section 2 - Warnings

#### Section 3 - Informational

-----

INFO:MapLib:562 - No environment variables are currently set.

INFO:LIT:244 - All of the single ended outputs in this design are using slew rate limited output drivers. The delay on speed critical single ended outputs can be dramatically reduced by designating them as fast outputs.

INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)

INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report (.mrp).

INFO:Pack:1650 - Map created a placed design.

#### Section 4 - Removed Logic Summary

-----  
2 block(s) optimized away

## Section 5 - Removed Logic

-----

Optimized Block(s):

TYPE            BLOCK  
GND            XST\_GND  
VCC            XST\_VCC

To enable printing of redundant blocks removed and signals merged, set the detailed map report option and rerun map.

## Section 6 - IOB Properties

-----

+-----+-----+-----+-----+-----+-----+-----+-----+-----+								
IOB Name				Type	Resistor	IOB	Direction	IO Standard
Diff	Drive	Slew	Reg (s)					
Term	Strength	Rate				Delay		
+-----+-----+-----+-----+-----+-----+-----+-----+-----+								
a1	12	SLOW		IOB			OUTPUT	LVCMS25
a2	12	SLOW		IOB			OUTPUT	LVCMS25
a3	12	SLOW		IOB			OUTPUT	LVCMS25
a4	12	SLOW		IOB			OUTPUT	LVCMS25
add1				IOB			INPUT	LVCMS25
add2				IOB			INPUT	LVCMS25
add3				IOB			INPUT	LVCMS25
add4				IOB			INPUT	LVCMS25
clk				IOB			INPUT	LVCMS25
led_seg<0>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<1>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<2>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<3>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<4>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<5>	12	SLOW		IOB			OUTPUT	LVCMS25
led_seg<6>	12	SLOW		IOB			OUTPUT	LVCMS25
rst				IOB			INPUT	LVCMS25
rst1				IOB			INPUT	LVCMS25
rst2				IOB			INPUT	LVCMS25

val1<0>				I0B		OUTPUT	LVCMS25
val1<1>	12	SLOW		I0B		OUTPUT	LVCMS25
val1<2>	12	SLOW		I0B		OUTPUT	LVCMS25
val1<3>	12	SLOW		I0B		OUTPUT	LVCMS25
val2<0>	12	SLOW		I0B		OUTPUT	LVCMS25
val2<1>	12	SLOW		I0B		OUTPUT	LVCMS25
val2<2>	12	SLOW		I0B		OUTPUT	LVCMS25
val2<3>	12	SLOW		I0B		OUTPUT	LVCMS25
val3<0>	12	SLOW		I0B		OUTPUT	LVCMS25
val3<1>	12	SLOW		I0B		OUTPUT	LVCMS25
val3<2>	12	SLOW		I0B		OUTPUT	LVCMS25
val3<3>	12	SLOW		I0B		OUTPUT	LVCMS25
val4<0>	12	SLOW		I0B		OUTPUT	LVCMS25
val4<1>	12	SLOW		I0B		OUTPUT	LVCMS25
val4<2>	12	SLOW		I0B		OUTPUT	LVCMS25
val4<3>	12	SLOW		I0B		OUTPUT	LVCMS25
	12	SLOW					

---

## Section 7 – RPMs

---

## Section 8 – Guide Report

---

Guide not run on this design.

## Section 9 – Area Group and Partition Summary

---

### Partition Implementation Status

---

No Partitions were found in this design.

---

### Area Group Information

---

No area groups were found in this design.

---

## Section 10 – Timing Report

---

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated

using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

#### Section 11 – Configuration String Details

---

Use the "-detail" map option to print out Configuration Strings

#### Section 12 – Control Set Information

---

Use the "-detail" map option to print out Control Set Information.

#### Section 13 – Utilization by Hierarchy

---

Use the "-detail" map option to print out the Utilization by Hierarchy section.

parking_meter Project Status (03/14/2021 - 02:08:18)			
<b>Project File:</b>	lab4.xise	<b>Parser Errors:</b>	No Errors
<b>Module Name:</b>	parking_meter	<b>Implementation State:</b>	Mapped
<b>Target Device:</b>	xc6slx16-3csg324	• <b>Errors:</b>	No Errors
<b>Product Version:</b>	ISE 14.7	• <b>Warnings:</b>	<a href="#">8 Warnings (0 new)</a>
<b>Design Goal:</b>	Balanced	• <b>Routing Results:</b>	
<b>Design Strategy:</b>	<a href="#">Xilinx Default (unlocked)</a>	• <b>Timing Constraints:</b>	
<b>Environment:</b>	<a href="#">System Settings</a>	• <b>Final Timing Score:</b>	

Device Utilization Summary <span>[ - ]</span>				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	40	18,224	1%	
Number used as Flip Flops	37			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	3			
Number of Slice LUTs	730	9,112	8%	
Number used as logic	729	9,112	8%	
Number using O6 output only	513			
Number using O5 output only	27			
Number using O5 and O6	189			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	256	2,278	11%	
Number of MUXCYs used	284	4,556	6%	
Number of LUT Flip Flop pairs used	732			
Number with an unused Flip Flop	692	732	94%	
Number with an unused LUT	2	732	1%	
Number of fully used LUT-FF pairs	38	732	5%	
Number of unique control sets	6			
Number of slice register sites lost to control set restrictions	27	18,224	1%	
Number of bonded <a href="#">IOBs</a>	35	232	15%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	

Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	4.19			

Detailed Reports <span style="float: right;">[-]</span>					
Report Name	Status	Generated	Errors	Warnings	Infos
<a href="#">Synthesis Report</a>	Current	Sun Mar 14 10:39:48 2021	0	<a href="#">8 Warnings (0 new)</a>	<a href="#">5 Infos (0 new)</a>
<a href="#">Translation Report</a>	Current	Sun Mar 14 10:59:10 2021	0	0	0
<a href="#">Map Report</a>	Current	Sun Mar 14 10:59:33 2021	0	0	<a href="#">6 Infos (0 new)</a>
<a href="#">Place and Route Report</a>	Out of Date	Sun Mar 14 10:38:51 2021	0	0	<a href="#">3 Infos (3 new)</a>
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports <span style="float: right;">[-]</span>		
Report Name	Status	Generated
<a href="#">ISIM Simulator Log</a>	Out of Date	Sun Mar 14 10:33:14 2021

**Date Generated:** 03/14/2021 - 02:08:18