**2.2 Split gate approach**

In this approach, we have split the source reservoir gate for the sensing dot into two parts, as illustrated in figure 1(c). The gate labelled ‘accumulation gate’ serves to accumulate the 2DEG used as the source reservoir for the sensing dot, and the ‘lead gate’ accumulates a second 2DEG, connecting the reservoir 2DEG to the ohmic contact. Moreover, we connect the inductor for the RF readout to the ‘accumulation gate’. The RF signal from the inductor is coupled to the reservoir 2DEG through the capacitance between the ‘accumulation gate’ and the reservoir 2DEG [cite **volk2019**]. The advantage of the split gate approach is that the density of the lead 2DEG can be varied independently from the reservoir 2DEG, and can be made such that the resistance between the reservoir 2DEG and the Ohmic contact is large (>10MOhm). This effectively cuts off the leakage path of the RF signal through the Ohmic, significantly reducing the overall parasitic capacitance of the RF circuit, as well as preventing dissipation of the RF signal in the contact resistance of the Ohmic. In case of matching, the signal is dissipated in the sensing dot, otherwise it is reflected.

To explore the working limits of the lead gate approach, we simulated the resonance frequency and the matching sensing dot resistance of the circuit in figure 1(c), while varying the parasitic capacitance and the inductance (figure 3). To aid us in choosing the values for our circuit components, we define a desired range of the matching resistance to be between 100kOhm and 1MOhm, typical resistance values for sensing dots in Si/SiGe. Moreover, we limit the resonance frequency of the matching circuit to above 100MHz, within the range of widely available cryogenic components. From the simulation results (figure 3 (a) and (b)), we find that there is a rather large parameter space to achieve the desired matching condition.

We estimate the total parasitic capacitance of our circuit to be around Cp~250fF. We choose an inductor value of L=3.4uH, which leads to resonance frequency around 180MHz?, and matching at 300kOhm sensing dot resistance.

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An image of our inductor and chip is shown in figure 1(e). The parasitic capacitance (Cp) of the circuit can be broken down in 3 parts: the self-capacitance of the inductor, bondwire from the inductor to the chip and capacitance of the chip. The self-capacitance of the inductor is around 50fF, this is kept low using high kinetic inductance materials. We estimate the capacitance of the bondwire to be around 50fF from Comsol simulations. The chip capacitance is estimated to be 150fF using a microstrip model.

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Moreover, from additional simulations (not shown) we estimate that a minimal capacitance C2DEG=50fF (@200Mhz) is required between the accumulation gate and the reservoir 2DEG to not affect the matching condition of the circuit. And the resistance of the 2DEG below the lead gate RLead should be tuned at least 10 times larger than the matching resistance. When operating the device, we noticed that there is no difference between operating it around 10MOhm and open. This suggests it should possible to remove the ohmic and the lead gate altogether. Note that this could make the tune up of the device harder, as no transport measurements through the sensing dot would be possible.

We also simulated the effect of the bandwidth for this circuit (not shown 🡪 PUT |N sup?). We only see a weak dependence of the bandwidth in function of inductance and parasitic capacitance for practical values (bandwidth range from 0.5 to 1MHz). This means that the bandwidth cannot be tuned by choosing these parameters.

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Figure 1: Circuit models for several device layouts with one sensing dot incorporated in an RF tank circuit. In the top image of each panel, a circuit model of the device is shown, on the bottom, a sketch of the physical device layout is shown. L is the inductance of the inductor connected to the chip, Cp is the cumulative parasitic capacitance of the inductor, the bondwire and the accumulation gate. In panel (a) a classical device layout is shown. In such a design, the accumulation gate will have a large capacitance to the 2DEG below (C2DEG). Panel (b) shows the circuit model and a schematic for the ohmic approach. In addition to the schematic in panel (a), a blocking resistor is added on the PCB to artificially reduce the effective capacitance of the accumulation gate. This resistor has a resistance Rblock and a capacitance Cblock (this capacitance is significant due to the macroscopic size of the blocking resistor). In panel (c), the lead gate approach is shown, where the inductor is connected to the accumulation gate. This RF signal will couple to the 2DEG via the capacitive coupling of the accumulation gate. To make sure that the signal does not escape via the ohmic, a lead gate (see sketch) is added that allows to tune the resistance to the ohmic (RLead). In panel (d), a picture shows the assembly of the inductor, resistor and sample for the ohmic approach and a device image. Panel (e) shows a similar image for the lead gate approach.

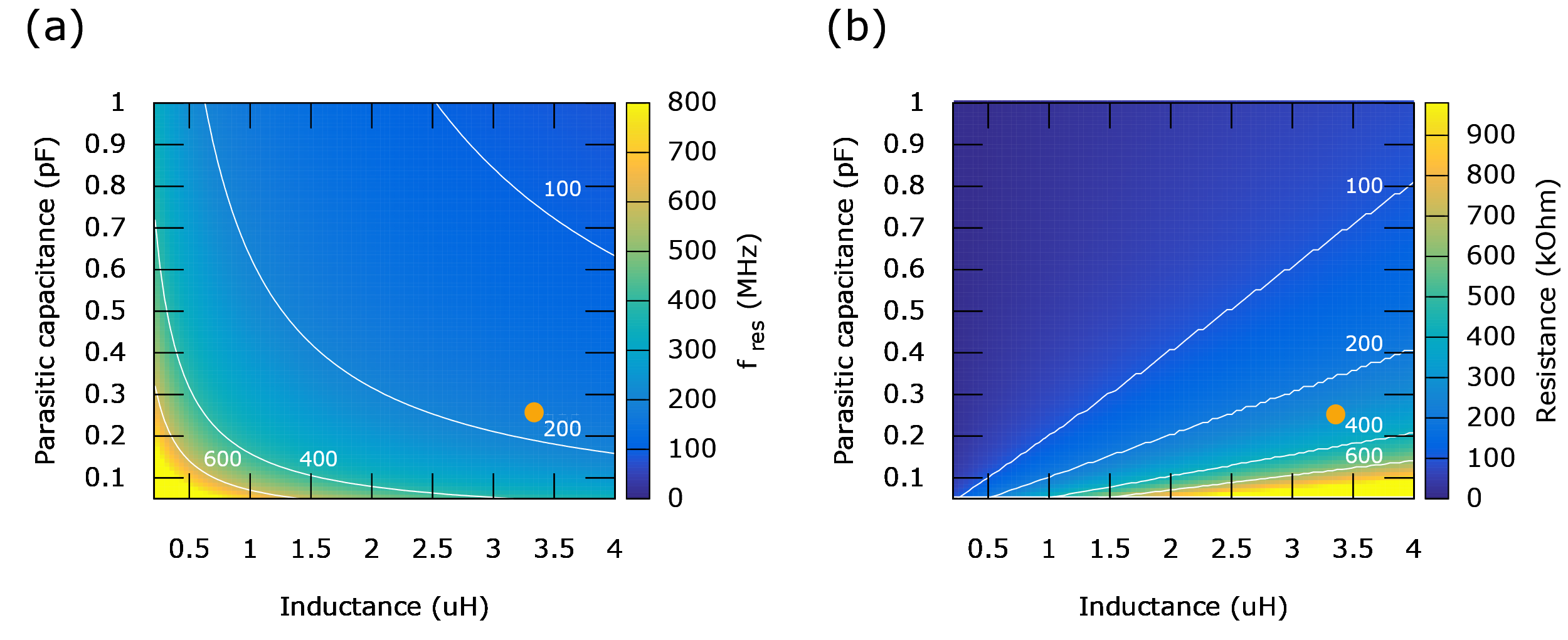


Figure 3: Circuit simulations for the circuit shown in figure1(c), where the inductance L and the parasitic capacitance Cp are varied. The resistance of the lead gate (Rlead) is set to 10MΩ (typical value used in the experiment), the capacitance of the accumulation gate to the 2DEG is set to 100fF. The orange dot indicates the parameters for the device and circuit used in this paper.

3.2 RF reflectometry with split gate approach

In figure 5(a), the response of the resonator versus frequency is shown for several resistances (below and above the matching point). From this figure one can derive the bandwidth of the matching circuit, which is equal to the linewidth of the resonance curve. At the matching sensing dot resistance, the expected bandwidth is 0.8MHz, and the minimal measurement time is 600ns (assuming perfect SNR).

In figure 5(b)we characterize the reflectance of the matching circuit versus the resistance of the sensing dot. The matching point is at 275kΩ. One can see that there are two highly sensitive regions around the matching point as indicated in figure 5(b). Note that these regions do not overlap in the IQ plane as the phase of the signal flips 180 degrees at Rmatch. The resistance of our sensing dot is in the range of 400kΩ to 1MΩ , we speculate that it would be possible to further increase the SNR of the matching circuit by decreasing the parasitic capacitance (Cp) from 250fF to 150fF (e.g. by making the footprint of the gates smaller),increasing the matching resistance to 600kΩ.

We analyse the performance of the readout in figure 5(c-d). As metric, we define the charge readout fidelity. This fidelity is defined as the probability to correctly determine if a quantum dot is occupied with zero (N=0) or one (N=1) electron for a given measurement time. To calculate the fidelity, we send a train of block pulses (10k) to the quantum dot which will enforce the charge state N=0 and N=1 (top/bottom of the block pulse). In the meanwhile, we sample for each half period of the block pulse the signal of the sensing dot. Later we calculate the distribution of the signals collected for the occupation N=0 and N=1 and calculate the overlap. The overlap between both signals is the reported fidelity. For these measurements, we used a digital bandpass filter (FIR type) to clean up the sampled signal. A passband was set between 100KHz and 2.5MHz. The lower frequency of the passband was determined by the slowest signal we wanted to see (e.g. 5us in this case). The upper frequency was taken close the bandwidth of the tank circuit.

In figure 5(c), the charge readout fidelity versus measurement time is plotted. In this graph, we see that we are limited to measure a signal with a size of 600-800ns. For shorter time ranges we are most likely limited by (1) the signal to noise ratio and/or (2) the effective bandwidth of the tank circuit. In figure 5(d) the readout fidelity versus power is plotted. For low powers we see that we need to sample longer to achieve the same fidelity, in other words, in this regime we are SNR limited. In case of high power, we see that the measurement time to reach 99% charge readout fidelity saturates. This saturation most likely occurs due to bandwidth limitations of the circuit (0.8MHz), but could also be a side effect of the broadening of the sensing dot.

When operating the tank circuit, one is free choose the applied power to the circuit. Figure 5(d) shows the dependence of the power applied to the tank circuit versus the electron temperature and the charge readout fidelity. As expected, the electron temperature increases as more power is applied on the sample. The charge readout fidelity increases with power. In other words, there is a tradeoff that needs to be made between both factors. From this data, we would recommend to only turn on the power for the tank circuit during the readout phase of a single shot experiment. In these experiments, the power was on all the time.

In conclusion, using this method we can obtain similar SNR as in other on-chip methods for RF readout [Nichol, Tarucha]. One scenario where the lead gate method would have a clear advantage over the ohmic method is if having a large contact resistance Rc and/or large 2DEG capacitance, C2DEG in the device are unavoidable.

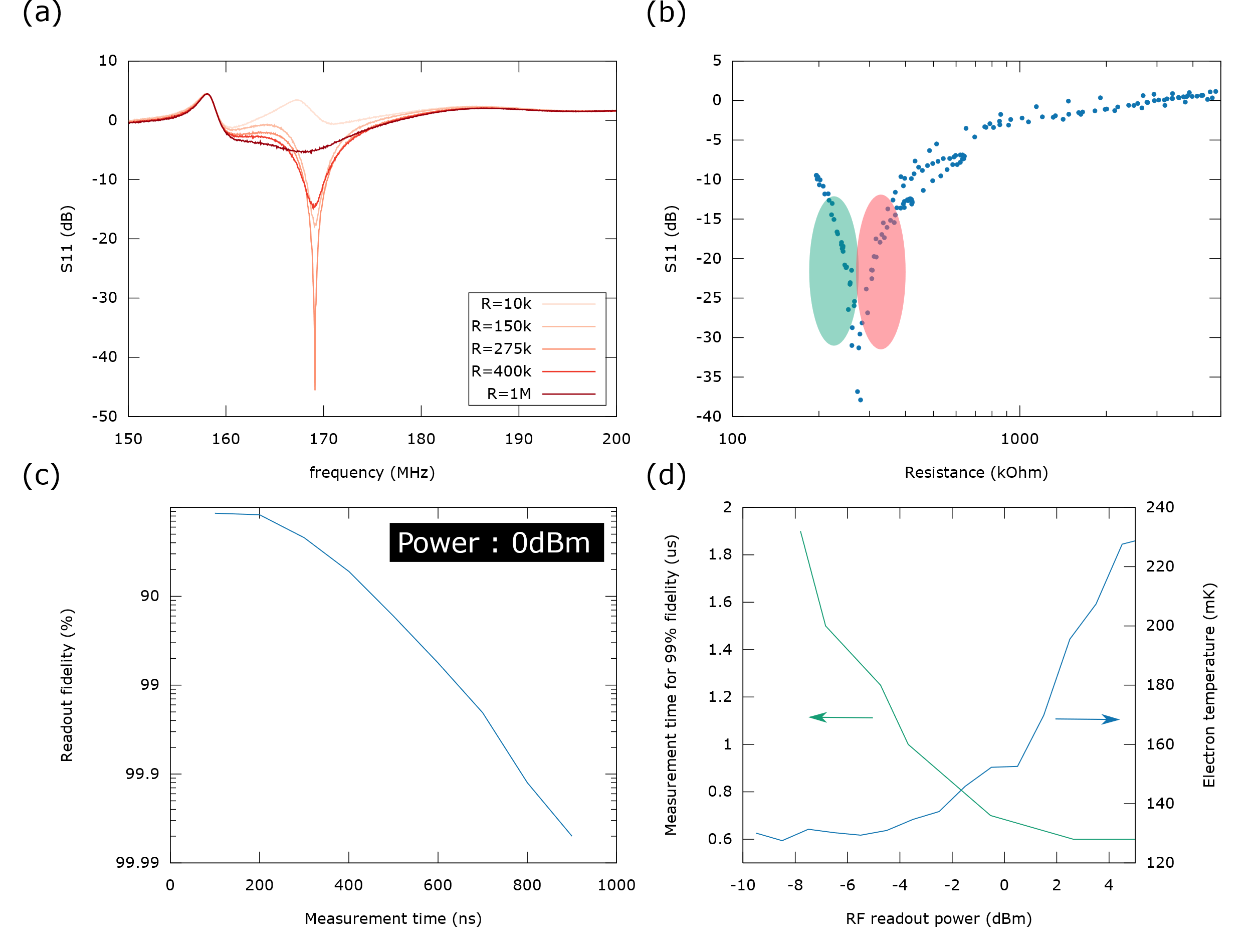


Figure 5: Characteristics and performance of the lead gate approach. (a) Reflection coefficient of the tank circuit as a function of frequency for several resistances of the sensing dot. (b) Reflection of the tank circuit at the resonance versus the resistance of the sensing dot. The matching condition of the circuit is met at 275kOhm. The sensitive regions are marked in red and green respectively. (c) Infidelity of charge detection versus measurement time for a intradot transition (d) Curves showing the relationship between the charge readout fidelity and the electron temperature versus the applied power to the tank circuit. The electron temperature was determined by measuring the polarization line (ADD REF).