**Abstract**

RF reflectometry for charge sensing is a fast and high fidelity method for spin qubit measurements. While it has been successfully implemented in gallium arsenide, silicon germanium has proved significantly more chal- lenging due to substantially larger capacitances of the devices to ground. We demonstrate that the effects of this extra capacitance can be miti- gated to enable RF reflectometry. Additionally, we demonstrate that this capacitance can actually serve as a pathway to introduce the RF tone to the sensor dot. We lay out the considerations for these two techniques.

Generally I guess the added values of our paper are:

* More detailed (compared to others) investigation of why the parasitic capacitance is bad for RF readout.
* Modification to chip and pcb to make the ohmic method work.
* Modification to chip to make it work via acc gate + performance charac.

Alternative version:

RF reflectometry for charge sensing is a fast and sensitive method for spin qubit measurements. We focus in this work on the implementation of RF readout in the Silicon Germanium heterostructures. The implementation proved challenging due to large parasitic capacitances of accumulation mode devices. We investigate the sources and effects of these parasitic capacitances. We describe two methods that are used to mitigate these parasitic capacitances, both by on and off chip methods. We show that using these methods it is possible to obtain a high-performance readout circuit in SiGe heterostructures.

**Intro**

As Moore’s law begins to break down, new computational schemes will be neces- sary for improved computation performance. Quantum computing is an exciting avenue that already boast algorithms that should provide speedups or perform tasks that are impossible on conventional computers (cite papers on quantum computation algorithm/proposals). Of the physical platforms available, spin based quantum bits (qubits) in semiconductors are particularly promising [3] cite papers on GaAs/SiGe/InAs/... spin qubit). These qubits can be initialized quickly and with high fidelity through spin dependent tunneling to a neighbor- ing Fermi sea. Single qubit gates with fidelities above 99% and two qubit gates above 90% have been demonstrated. The small size and localized nature of the control also lend themselves naturally to scaling to the number of qubits needed for a fully functioning quantum computer. One particularly interesting semi- conductor material is silicon germanium (SiGe) which hosts a two dimentional electron gas (2DEG) where spin qubits can be formed. The qubit overlaps with orders of magnitude less nuclear spins than in other materials, such as gallium aresenide (GaAs), which reduces decoherence due to the magnetic field noise from nuclear spin fluctuations cite papers.

Charge sensing is an important technique for measuring spin qubits because their long-lived spin states can be converted into detectable charge states. This is usually done by Elzerman readout or Pauli-Spin blockade readout (papers). To detect a charge state, one can make use of a sensing quantum dot (SD) in close proximity (d <∼ 300 nm) to the qubit. The current through the sensing dot is strongly dependent on the charge state of the qubit because the electric potential of the qubit shifts the Coloumb peaks of the sensor dot, drastically altering its resistance. The easiest way to measure this, is by using a DC current through the sensing dot with a amplifier at room temperature (e.g. with a JFET). However, this requires an integration time on the order of milliseconds, drastically slowing experiments because intializing and manipulating the qubit can be done on the nanosecond or microsecond scale. To reduce the noise temperature, people have also built low temperature DC amplifiers that are operated at base temperature. This is technically difficult Mark’s paper? due to issues like heating and converting the impedance to 50 Ohm. For this reason, high frequency techniques like RF readout are of great interst, as this allows for comparably low(er) noise temperatures and sub microsecond integration times.

Radio Frequency (RF) reflectometry was originally proven to be a very effective technique in GaAs spin qubits and has enabled single shot readout with only several microseconds of integration [5] more papers?. However, SiGe has proved to be a more challenging platform in which to implement RF reflectometry due to larger capacitances to ground. Typical GaAs substrates are depletion mode while SiGe wafers are most often accumulation mode and require metallic electrostatic gates to cover all current paths so that the 2DEG can be populated design papers?. This capacitive coupling between the 2DEG and gates is undesirable for RF reflectometry because it provides low impedance leakage pathways to ground that are independent of the SD. This reduces the sensitivity of the reflected signal to the qubit state. Previous work has addressed this problem by the use of resistors [1] and careful design of the accumulation gates [2]. In this work, we further develop the understanding of the leakage pathway introduced by this capacitance and introduce a alternative for achieving reflectometry.

Here we demonstrate that RF reflectometry can be achieved in SiGe using two general approaches that differ in how the measured RF signal is carried to the lead of the SD. In the ohmic style, the signal enters the 2DEG through an ohmic contact so that it carried in the 2DEG itself all the way to the SD, as in GaAs. For this approach, it is important to mitigate the effects of capacitance as much as possible. In the split gate style, the RF signal is carried by a gate which is capacitively coupled to the lead in the 2DEG near the sensor dot. For this approach, the capacitance is a resource and not a detractor because the capacitance is what enables the signal to reach the SD. For both schemes, we have achieved sensitivity of the RF reflection to the resistance through the SD and have performed charge readout of the target quantum dot.

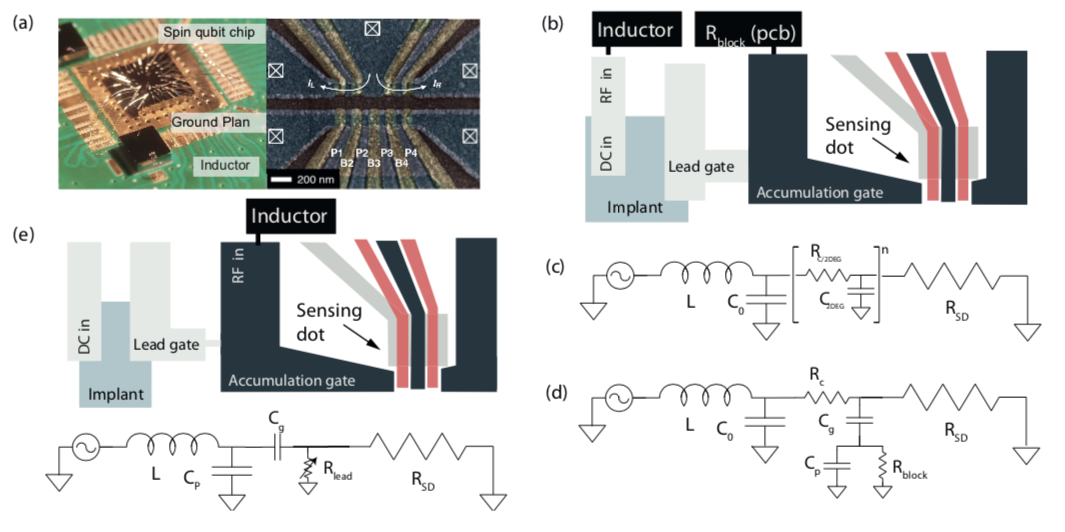


Figure 1: (a) Sample mounted and wired bonded to a circuit board. False color image of scanning electron micrograph of a typical SiGe overlap style device. (b) Sketch of the gate layout for the ohmic approach where the signal is applied to the SD through the ohmic. (c) Continuous model circuit diagram for the ohmic method. The bracketed section represents that the device has distributed capacitance and resistance. (d) Lumped element circuit diagram for the ohmic method. The distributed capacitance and resistance are replaced with lumped elements for computational simplicity. (e) Circuit diagram and sketch of the gate layout for the gate approach where the signal is applied to the SD through the accumulation gate.

2 RF Reflectometry

In RF reflectometry a fixed frequency signal is reflected off an impedance matching inductive capacitive (LC) tank circuit that is loaded with the SD with resis- tance RSD, as shown in Fig. 1(c). The reflection coefficient of this tank circuit is given by Γ = (Z − Z0)/(Z + Z0), where Z is the impedance of the loaded tank circuit and Z0 = 50Ω is the source impedance. When the device’s parasite capacitance C2DEG and contact resistance R2DEG can be ignored, the effective impedance of the loaded tank circuit is Z = i2πfL+1/(1/(RS +i2πfC0) at an input frequency f. In the experimental setup, L is a lumped element inductor and C0 represents the total capacitance to ground of the circuit board, a lumped element capacitor and the parasitic capacitance of the bond wires of the device.

Γ is strongly modulated near Γ = 0, which occurs at the matching condition that Z = Z0 when driven with f equal to the resonant frequency of fM = 1/(2π LC0) and with RSD equal to the matching resistance RM = L/C0Z0. RSD is very sensitive to the electric potential of the SD’s environment, and thus to the charge states in the nearby quantum dots used to form the qubits. Hence Γ is sensitive to the charge state of the qubit because of its dependence on RSD. The tank circuit is designed with L and C0 chosen so that the value of RM is where RSD is most sensitive to the qubit, typically in the range of 50 – 600 kΩ. For GaAs, this simple model is sufficient to capture the observed behavior.

In SiGe, the simple tank circuit model fails because R2DEG and C2DEG are no longer negligible. Figure 1(a) demonstrates a typical overlap style device. A quadruple quantum dot is formed with the lower set of gates and two sensors are formed with upper gates. Large accumulation gates control the electron density of the leads from the ohmic contacts to the quadruple dots used to form the qubits and the SDs. Compared to depletion mode devices, there is an additional C2DEG of 0.1–1 pF because of the accumulation gate, as seen in Figure 1(b). The RF signal used for reflectometry passes through the lossy 2DEG channel with resistance R2DEG and is shunted to ground through C2DEG, drastically reducing the sensitivity of Γ to RSD so that the qubit charge state cannot be detected.

To overcome this problem, we demonstrate two alternate approaches:  
􏰀 Ohmic Approach – Couple the tank circuit to the ohmic but mitigate the effects of C2DEG and R2DEG through engineering of the circuit board that carries the sample and elements used in the tank circuit, Figure 1(b).

􏰀 Split Gate Approach – Couple the tank circuit to the accumulation gate so that the signal capacitively enters the lead of the SD, Figure 1(e). This means that the signal passes through C2DEG intentionally and that it is not a leakage pathway.

A screenshot of a cell phone

Description automatically generated

Figure 2: (a) and (b) Simulations of fM and RM as a function of C0 and L with fixed parameters of Cg∗ = 0.2 pF and Rc = 3 kΩ. White regions are where no matching can be achieved. (c) Simulation of RM as a function of Rc and L with fixed Cg∗ = 0.2 pF, and C0 = 1.6 pF. (d) Simulation of RM as a function of C0 and Cg∗ with L = 1000 nH, and Rc = 3 kΩ. (e) Experimental demonstration of best matching with fM = 34 MHz. (f) Experimental demonstration of RM dependence on Rc. While Rc cannot be measured because it is so much smaller than RSD, it is dependent on VL. The left panel has VL=1 V and the right panel has VL=0.45 V and have RM=67 kΩ and RM=200 kΩ respectively.

3 Ohmic Approach

The ohmic approach is shown in Figure 1(b) and introduces the RF signal to the lead of the SD through the ohmic contact. The significant resistance of the 2DEG and capacitance to the accumulation gate prevent applying the simply RLC model to SiGe devices. Instead, the device has distributed capacitance and resistance, as modeled by the series of capacitors and resistors, shown in Figure 1(c). For simplicity, this can be treated as a single resistance, Rc and single capacitance, Cg, as shown in Figure 1(d). We will begin by explor- ing how the tank circuit parameters (C0 and L) and the device parameters (Rc and Cg ) affect the matching conditions (fM and RM ). This understanding will then be applied to demonstrate several key strategies that allow for ohmic style RF reflectometry in SiGe. We must design the tank circuit so that RM and fM are experimentally achievable and so that majority of the power is dissipated in RSD to achieve a usable signal to noise ratio (SNR).

3.1 Lumped Element Model

For the standard tank circuit model, there will always be some fM and RM where matching is achieved. However, simulations and experiments demonstrate that large values of Rc and Cg can prevent there being a RM and fM and therefore the ability to use the tank circuit for charge detection. In Figure 2 we explore the dependence of the matching conditions on C0, L, Cg and Rc. Simulations are performed by solving for RSD and f such that the Z of the loaded tank circuit is set equal to Z0 = 50 Ω to find the values of RM and fM respectively. The constraints that fM is real and that RM is real and positive result in there being conditions where no matching can be achieved, which are shown as white regions in Figure 2(a-d).

When a sample is fabricated, Cg and Rc are roughly fixed, meaning that the only way to change RM and fM is through the tank circuit parameters L and C0. We present numerical simulations of fM in Figure 2(a) and RM in Figure 2(b)asafunctionofLandC0 withCg∗ =0.2pFandRc =3kΩ. We note that far from the non-matching regions, the behavior is approximately that of the standard tank circuit model. Under these conditions, C0 ≫ Cg which means that C0 dominates the capacitance of the loaded tank circuit. When C0 is comparable to or smaller than Cg, there is very little dependence on RSD because the parallel pathway through Cg is low impedance.

Achieving best matching with both RM and fM in the desired range requires designing the sample with Rc and Cg in mind. The dependence of the matching conditions is strongly dependent on Rc, as shown in Figure 2(c). At Rc = 0, the model is reduced to the standard tank circuit model with an effective C0∗ = C0 + Cg. We note that the range of parameters that can achieve matching is drastically reduced as Rc increases. Reducing the resistance of the lead is therefore key to achieving RF reflectometry. To understand the impact of Cg, we present a simulation the dependence of RM in Figure 2(d). We again observe that matching is only achieved when C0 > Cg.

Together, these simulations suggest that the tank circuit itself should pro- vide the dominant contributions to the capacitance through C0 and that all contributions from the device other than RSD should be minimized. We apply this understanding experimentally in the next section

3.2 Implementing Ohmic Style RF Reflectometry

We have identified several experimental strategies for device and circuit design that enable RF reflectometry in SiGe by using the information provided in the previous section.

Block shunting to ground through Cg. Simulations have demonstrated that the RF signal in the lead has a low impedance path to RF ground through Cg. The gates themselves are connected to DC supplies and have RC filters to remove noise whose capacitors shunt the RF reflectometry signal to ground. In order to block this pathway, we have designed our printed circuit board (PCB) to have resistors, Rb between the sample bond pads and the RC filters to increase the impedance of the pathway to ground through Cg, figure 1(d). We use 10 kΩ 0201 resistors.

There is a parasitic capacitance, Cp, to ground from all the metal on the sample side of Rb (gate, bond wire, bond pad, PCB trace). This is in parallel to Rb and limits the ability to decrease the impact of Cg by just increasing Rb. Placing the Rb as close the bond pads as possible is ideal because it minimizes the amount of metal that contributes to Cp. This parasitic capacitance that cannot be entirely removed but it can be reduced by reducing the ground plane near the bond pads and by placing Rb as close to the bond pad as possible. Our PCB has Rb placed 3 mm away from the bond pads to minimize Cp while still allowing for sample bonding. Controlling both Rb and Cp serves to decrease the effective Cg that the device sees.

Ensure and control matching with C0 and L. The previous simulations demonstrated that the matching condition can be tuned when C0 ≫ Cg. Our PCB has been designed with solder pads for a surface mount inductor, L, and a surface mount capacitor to control C0. While the inductance of the PCB will be negligible without the surface mount component, the parasitic capacitance (which is not the same as Cp above) will be quite significant, usually on the order of 0.1 to 1 pF. As much ground plane near the tank circuit should be removed as possible in the design so that that the parasitic capacitance is re- duced. It is always possible to increase C0 through the surface mount element but it cannot be reduced below the parasitic capacitance of the board and for some devices we have found it optimal to have C0 < 1 pF.

We have two parameters that we would like to optimize, fM and RM , using the two design parameters, L and C0. As previously noted, C0 is has a lower limit set by the parasitic capacitance of the board. Practically, we need C0 is set as low as allowed by Cg because we want fM to be larger than 100 MHz. L has then been chosen so that RM =50-200 kΩ. We have found success using approximately L = 760 nH and C0 = 0.8 pF. While tuning C0 and L does enable the tank circuit to achieve matching with a usable RM , it may come at the cost of an unworkably low fM , as in Figure 2(e). For this reason, it is important to reduce the impacts of Cg and Rc.

Balancing the impacts of Cg and Rc in sample design. The sample design impacts both Cg and Rc, both of which we want to minimize, through the length l and width w of the accumulation gate. Knowing that Cg ∝ lw and Rc ∝ l/w reveals that decreasing l is ideal for both parameters while decreasing w to improve Cg comes at the cost of increasing Rc and vice versa. We have found that w =5 μm is sufficient to achieve consistent accumulation for usable Rc without increasing Cg drastically. The ohmic should be placed as close to the SD as possible to limit l and we have found that a distance of 10 μm does not decrease device performance.  
Tuning Rc. To experimentally confirm the dependence of RM on Rc, we

make use of the lead gate seen in Figure 1(b). This gate has a large width so that Rc on the order of 1–10 kΩ can be achieved. It is also designed to have a short length and only bridges between the ohmic and the accumulation gate so that it has a small area. The voltage on this gate can be tuned to vary Rc while minimally effecting Cg because of its small area.

In Figure 2(f) we demonstrate a tuneable best matching RM around 50∼ 200 kΩ at a resonant frequency of 220 MHz. The outside two panels plots the reflection power as a function of voltage applied to the sensor dot plunger gate VP at a higher (left panel) and lower (right panel) voltages applied to the lead gate. The middle panel plots corresponding the conductance of the sensor dot. With different gate voltage on the lead gate, the total conductance through the dot is unchanged with the same voltages of all other gates, indicating a small back-action to the sensor tuning. In the contrast, the best matching is achieved with 67 kΩ for the fully accumulated switch gate, and 200 kΩ for a partial accumulated switch gate. The only difference between them is Rc and this result agrees with the simulation in figure 2 (c). This tunability allows the use of fixed C0 and L for general devices as the matching condition of the device can be changed in situ. The tunable Rc, however, is not the final solution because the larger Rc, more energy is lost before the sensor dot, resulting in a smaller signal.