Lab 1: 4 to 1 Multiplexer

Course: COEN 122L
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Description

The multiplexer is a common hardware unit that is used to select certain data from a given set of inputs. It consists of n data inputs, a select input, and 1 data output (as pictured below). The n data inputs are passed into the multiplexer from external sources, and the multiplexer's job is to select one of these inputs by setting the output data to that value. The multiplexer knows which input to select based on the select input, which addresses the input lines. Therefore, the width of the select input (in bits) must be large enough to uniquely address the number of data lines. For example, if a multiplexer has 16 data inputs then the select input must be 4 bits wide to account for all 16 different values (the first value would be select 0000, the second value would be select 0001, etc.).

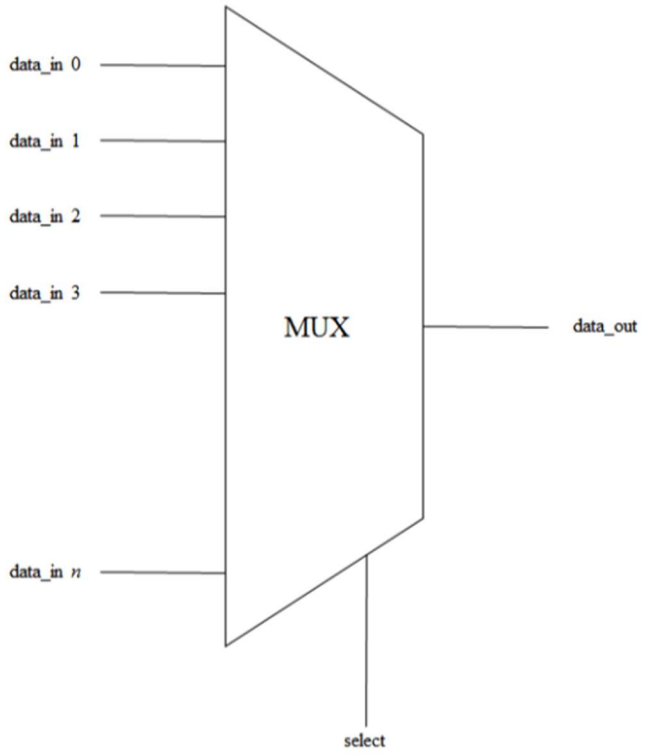

Figure 1: Block diagram of multiplexer

Assignment

In this lab you will write a description for a 4 to 1 multiplexer using the System Verilog language. Your multiplexer should have 4 one-bit inputs, a select line, and 1 one-bit output. You will write both the module description and a testbench to verify that your circuit functions correctly.
To receive full credit you will need to demo your working code and turn in copies of your source code and testbench.