Lab 4: Pipeline Buffers

Course: COEN 122L
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Description

A key component in a pipelined processor is the pipeline buffer. The buffer serves as a way to synchronize the pipeline across its multiple stages. Each buffer is responsible for taking the data from the preceding stage and, on each clock cycle, transferring it into the following stage. In your final design you may choose to use as many stages as you would like.

Assignment

In this lab you will design at least one pipeline buffer using the SystemVerilog language. As the actual inputs and outputs of the buffer(s) will reflect the layout of the whole pipeline you may select any inputs/outputs (at least 5 of each) to demonstrate the working buffer. I recommend that you think about the signals the pipeline will use and try to incorporate them into the buffer(s) for this lab as you may use them for your final project.

To receive full credit you will need to demo your working code and turn in copies of your source code and testbench.

Approach

In this lab we are again working with sequential circuits. Each of the pipeline buffers will be clocked just like the memory units from last week. The actual lab assignment for this week is intended to be lighter as we are transitioning into thinking about the final project. While this week's assignment is still individual, I strongly encourage you to begin drawing out a plan for the final processor. Next week in lab I will discuss a few modules you may find helpful to include in your pipeline, as well as several design features that may make your life easier.