Arithmetic Logic Unit

COEN 122 Lab 2

Grading

- Lab 1-4 (10% each) 40%
- Final Project 60%

Late Policy

- Late submissions submitted within 24 hours after the deadline receive 50% credit. After 24 hours, no credit is given.

Demo

- Labs submitted with no demo will receive no credit. Please demo to me before the lab is due.
- You can demo in either TAs Office Hours

Lab 2 Overview

- Objective: Implement a 32-bit ALU in Verilog using Vivado with a gate level implementation
- For the first 4 labs, you will be working individually, but will be working in teams for the project

Helpful website: http://www.asic-world.com/verilog/veritut.html

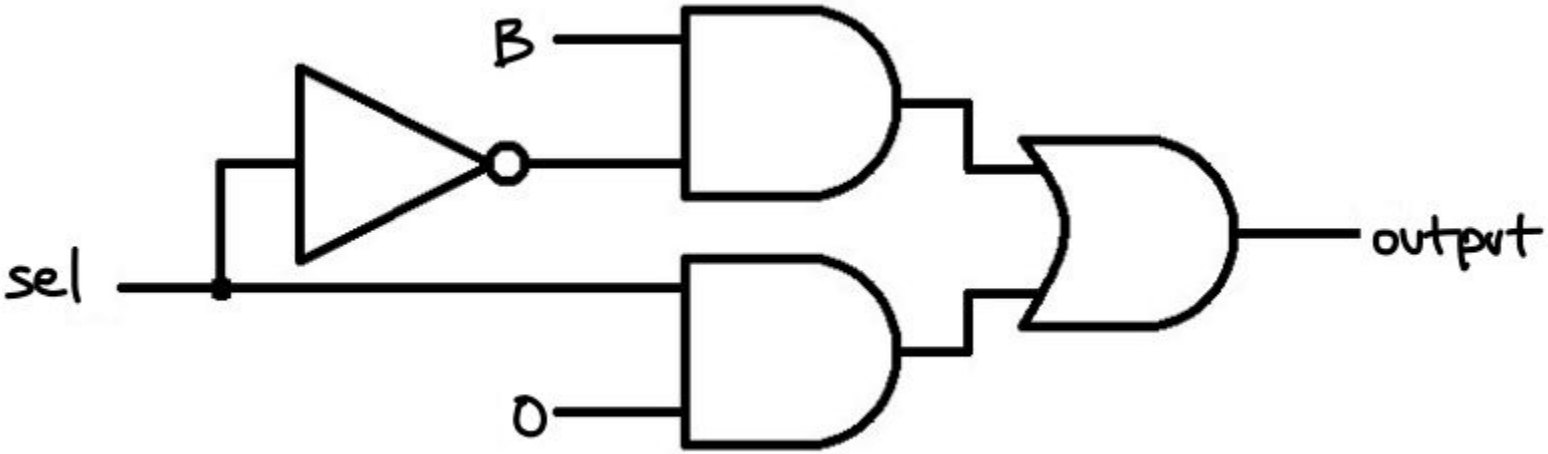
Design Flow

- Write code for logic block (e.g. 1-bit adder, full adder, 2-1 mux, 3-1 mux, 2s complement generator, selector)
- Write test bench to verify proper function of logic block
- Run Synthesis
- Run Simulation
- View waveform, verify results

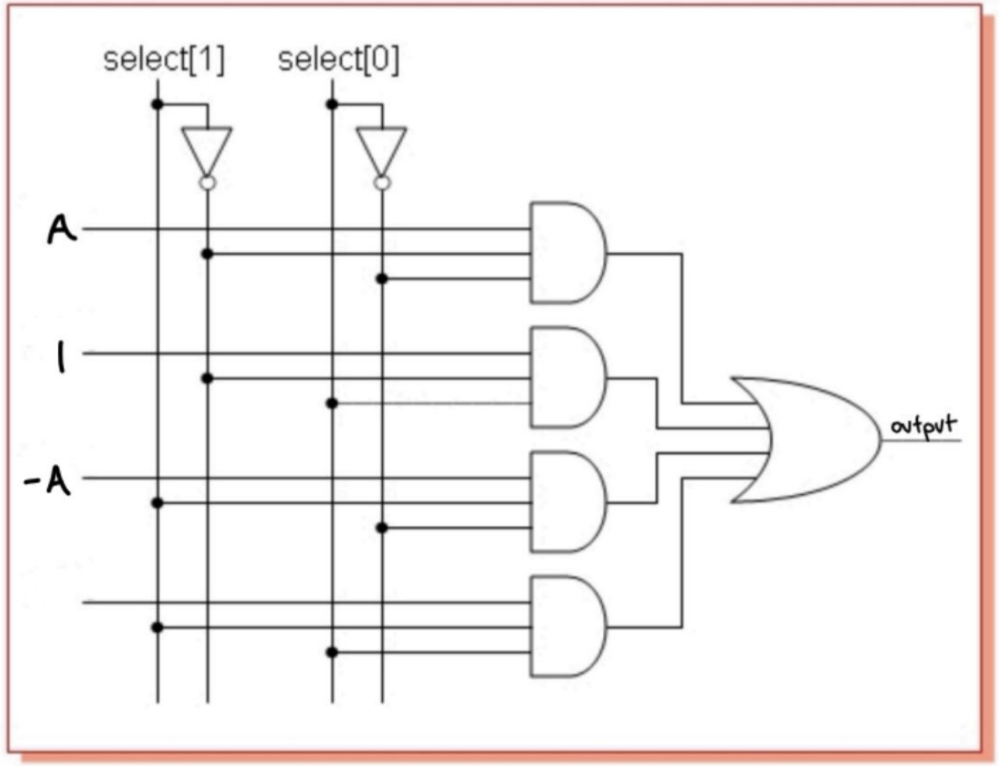
6 Modules to Build

- ALU
- 2:1 Mux
- 3:1 Mux
- 2’s Complement Generator
- 1 Bit Adder
- Full Adder

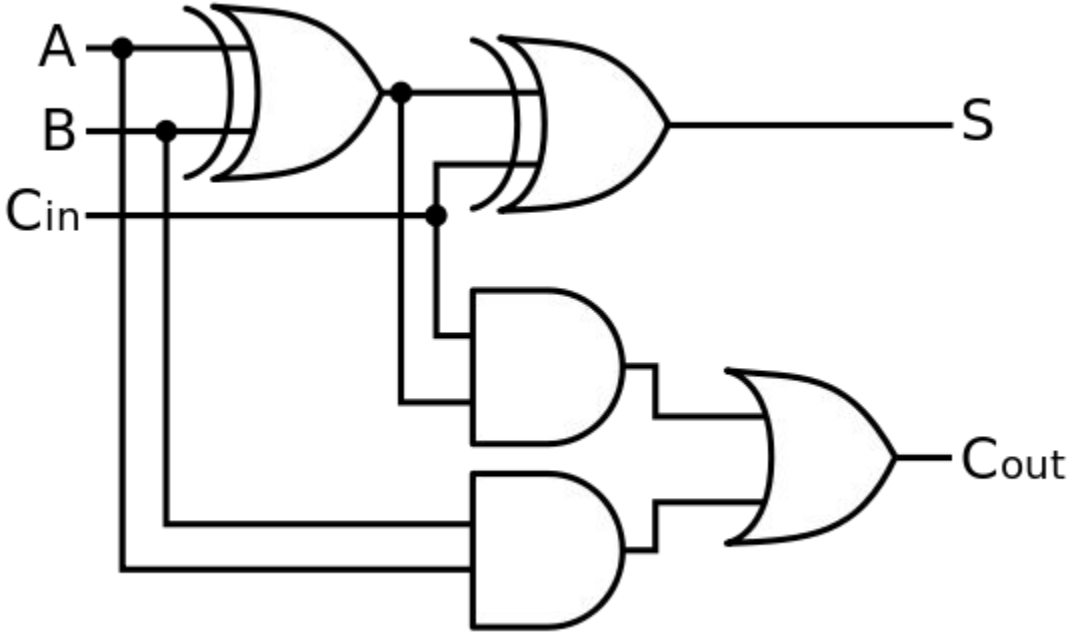
2:1 Mux Circuit Diagram



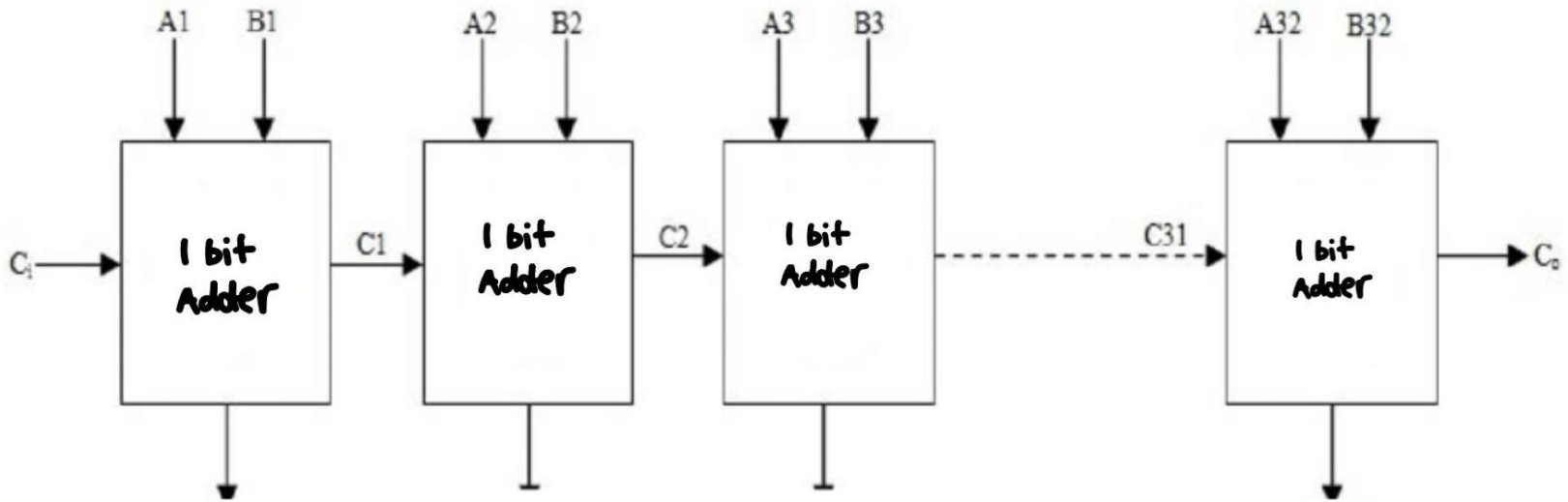
3:1 Mux Circuit Diagram



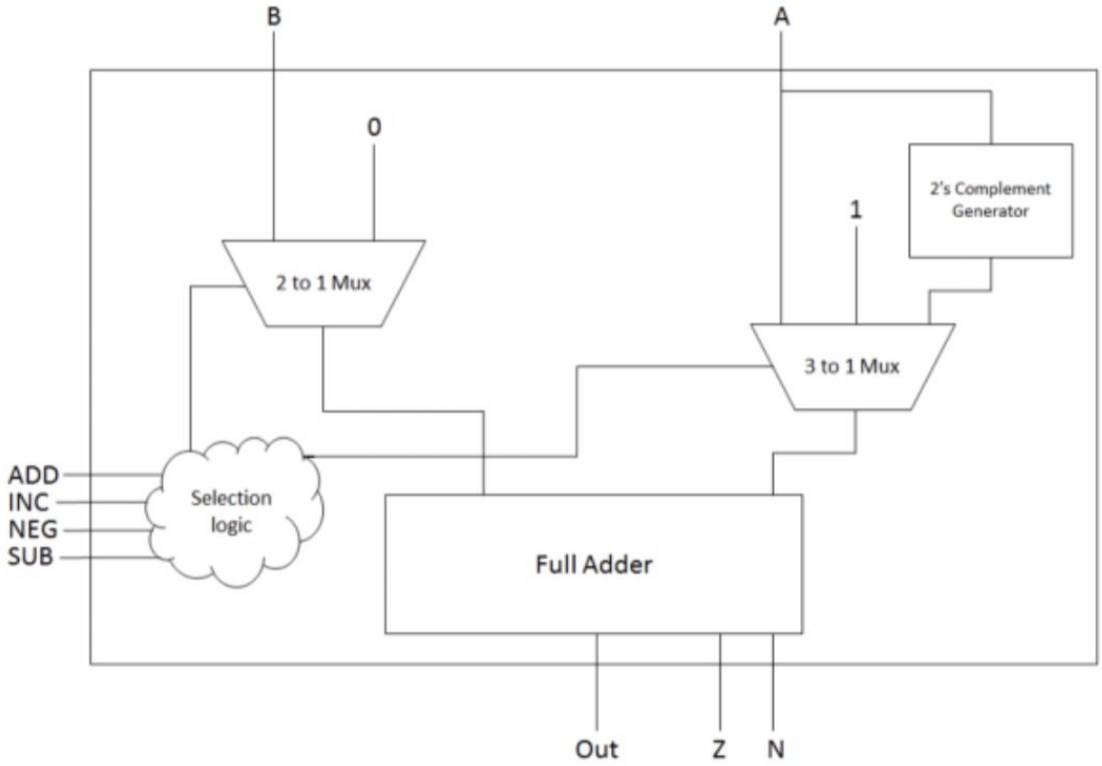
1 Bit Adder Circuit Diagram



Ripple Carry Full Adder Circuit Diagram



ALU Diagram


B
A
0
1
2's Complement Generator
2 to 1 Mux
3 to 1 Mux
ADD
INC
NEG
SUB
Selection logic
Full Adder
Out
Z
N

Generating Selects for Each Mux

- For 3:1 Mux:
  - not(not_sub, sub);
  - and(select[0], inc, not_sub);
  - nor(select[1], add, inc);
- For 2:1 Mux:
  - twoToOne mux_B(B, neg, outB), where select = neg

Module Definitions

- module ALU(A,B,add,inc,neg,sub,out,Z,N);
- module twoToOne(B,sel,out);
- module oneBitAdder(A, B, cin, cout, out);
- module fullAdder(A, B, cout, sum);
- module negate(A, out);
- module threeToOne(A, negA, sel, out);

ALU Truth Table

ADD	INC	NEG	SUB	OUT	Operation
1	0	0	0	B + A	Add
0	1	0	0	B + 1	Increment
0	0	1	0	-A	2’s complement
0	0	0	1	B - A	Subtract
1	1	1	1	A	Pass A

Notes

- NEGATE operator should return 2's complement, so just flipping the bits won't be sufficient (need to add 1 to the resulting value)
- For SUBTRACT, remember to add the 2's complement of A

- Test Cases:
  - Add
  - Increment
  - Negate
  - Subtract
  - Pass

Submission

- All ALU files as txt files
- ALU_testbench file as a txt file
- Screenshot of waveform