EXPLICIT WAVE DIGITAL FILTER IMPLEMENTATION OF THE FULLTONE OCD CIRCUIT

Lenoci Alice, Macrì Carlo, Polimeno Stefano

Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano
Piazza Leonardo Da Vinci 32, 20122 Milano, Italy
[alice.lenoci,carlo.macrì,stefano.polimeno]@mail.polimi.it

ABSTRACT

This work presents a Wave Digital Filter (WDF)-based white-box modeling of the Fulltone OCD overdrive pedal, a widely used analog circuit in electric guitar processing. The model aims to accurately reproduce the device's nonlinear behavior, with particular focus on the MOSFET-based clipping stage responsible for its dynamic and harmonically rich overdrive. Key challenges include capturing the asymmetrical distortion introduced by the MOSFETs and modeling their voltage-dependent resistance. To address these, we employ the Scattering Iterative Method alongside Canonical Piecewise-Linear approximations. The model is validated via comparison with Simscape simulations and implemented in both MATLAB and a JUCE-based real-time plugin, achieving a faithful digital emulation of the original circuit's sonic characteristics.

Index Terms— Virtual Analog, Wave Digital Filters, MOSFET Clipping, Overdrive Pedal, Nonlinear Modeling, Audio Plugin

1. INTRODUCTION

Over the years, significant advancements have been made in Virtual Analog (VA) modeling [1, 2], allowing for the digital emulation of the nonlinear characteristics of analog audio devices [3]. Among these, overdrive pedals have garnered particular attention due to their ability to shape the tonal character of electric guitars in a dynamic and expressive manner. This paper focuses on the analysis and modeling of the Fulltone OCD, a widely acclaimed overdrive pedal known for its transparent and amp-like saturation. Originally introduced in the early 2000s, the OCD has become a staple among guitarists for its ability to deliver a harmonically rich and responsive overdrive, closely resembling the breakup of a tube amplifier [4, 5]. Our approach leverages the Wave Digital Filter (WDF) method to construct an accurate physical model of the pedal, employing a white-box modeling approach, which ensures a precise replication of the circuit behavior using detailed internal information from schematics and component characteristics [6]. One of the biggest challenges in this process was the nonlinear MOSFET clipping stage, which plays a crucial role in defining the pedal's dynamic response and harmonic saturation. Unlike conventional diode clipping circuits used in many overdrive pedals, the MOSFET-based stage in the Fulltone OCD introduces asymmetrical waveform distortion, resulting in a highly dynamic touch-sensitive overdrive. To accurately model this behavior, it was necessary to capture the voltage-dependent resistance and complex charge dynamics of the MOSFETs, which significantly influence the shaping of the audio signal. Our approach utilized the Scattering Iterative Method (SIM) [7] in combination with the Canonical Piecewise Linear (CPWL) function [8] to efficiently solve the nonlinearities within the circuit. To validate the proposed model, we developed both a MATLAB implementation and a JUCE-based real-time audio plugin, comparing the results with a reference circuit simulated in Simscape.This report is structured as follows: Section 2 reviews the theoretical background; Section 3 outlines the modeling approach; Section 4 presents validation results; Section 5 describes the real-time implementation as a JUCE plugin; and Section 6 concludes the work.

2. THEORETICAL BACKGROUND

The Wave Digital Filter (WDF) approach, initially developed by Alfred Fettweis [9], is a mathematical framework for the discrete-time representation of analog systems using wave-based formalism. This technique extends classical circuit analysis by reformulating electrical quantities (such as voltages and currents) in terms of wave variables, facilitating efficient numerical computations while preserving energy-conserving properties. The transformation from conventional circuit representations to the Wave Digital domain is accomplished by introducing wave quantities a and b at each port of the system:

$$a = v + Zi, \tag{1}$$

$$b = v - Zi, \tag{2}$$

where a is the incident wave arriving at the port, b is the reflected wave leaving the port, v and i are the port voltage and port current, respectively, Z is the port resistance [9, 10].

2.1. Linear One-Port Elements

In the Wave Digital framework, linear one-port elements constitute the fundamental units of circuit modeling. Each component is reformulated in terms of discrete-time wave variables, where an incident wave $a[k]$ and a reflected wave $b[k]$ interact according to the element's constitutive law. This abstraction enables modular and numerically stable simulation architectures. The key behavior of each element is captured by a wave mapping and a corresponding adaptation condition, which defines the port resistance Z required to eliminate numerical reflections [9]. Table 1 summarizes the discrete-time relations for the most common linear one-port elements—including voltage sources with internal resistance, resistors, capacitors, and inductors—together with their associated port resistances under the adaptation condition.

Table 1: Wave mapping and adaptation condition for common WD one-port elements.

Element	Constitutive Eq.	Wave Mapping	Adaptation Z
Voltage source V_g	$v = E_g + R_g i$	$b[k] = E_g[k]$	$Z = R_g$
Resistor R	$v = Ri$	$b[k] = 0$	$Z = R$
Capacitor C	$i(t) = Cdv/dt$	$b[k] = a[k-1]$	$Z = T_s/2C$
Inductor L	$v(t) = Ldi/dt$	$b[k] = -a[k-1]$	$Z = 2L/T_s$

2.2. Topological and Scattering Foundations of Wave Digital Networks

A core principle of wave digital modeling is the decomposition of networks into elementary *junctions*, which enforce either voltage (series) or current (parallel) continuity. Each junction governs local wave scattering and is represented by a scattering matrix determined by its topology and port impedances. These localized behaviors are then composed to form the global model. In a linear reciprocal N-port network, the port voltages and currents are described by vectors $\boldsymbol{v} = [v_1, \ldots, v_N]^T$ and $\boldsymbol{i} = [i_1, \ldots, i_N]^T$. The variables can be partitioned into independent sets using a $\chi \times 1$ vector $\mathbf{v}_t$ of independent voltages and a $\psi \times 1$ vector $\mathbf{i}_l$ of independent currents, satisfying $\chi + \psi = N$ [11]. These independent variables relate to the overall voltage and current vectors via the fundamental cut-set and loop matrices, respectively, as

$$\boldsymbol{v} = \boldsymbol{Q}^T v_l, \quad \boldsymbol{i} = \boldsymbol{B}^T i_l, \tag{3}$$

where $\boldsymbol{Q} \in \mathbf{R}^{\chi \times N}$ and $\boldsymbol{B} \in \mathbf{R}^{\psi \times N}$ are derived from a directed graph representation of the network [12, 7]. Owing to the network's reciprocity, these matrices satisfy the orthogonality condition $\boldsymbol{B}\boldsymbol{Q}^T = 0$, which is intrinsically linked to partitioning the graph into χ twigs (tree edges) and ψ links (cotree edges) [13]. Within the wave digital framework, the relation between the incident wave vector $\boldsymbol{a}$ and the reflected wave vector $\boldsymbol{b}$ is globally described by the scattering matrix $\boldsymbol{S}$:

$$\boldsymbol{b} = \boldsymbol{S}\boldsymbol{a}, \tag{4}$$

with $\boldsymbol{S} \in \mathbf{R}^{N \times N}$. As demonstrated in [11], this matrix can be derived via two equivalent formulations, respectively based on cut-set and loop-set representations:

$$\boldsymbol{S} = 2\boldsymbol{Q}^{-1}(\boldsymbol{Q}^{-1})^T\boldsymbol{Q}\boldsymbol{Z}^{-1} - \boldsymbol{I}, \tag{5}$$

$$\boldsymbol{S} = \boldsymbol{I} - 2\boldsymbol{Z}(\boldsymbol{B}^T)^{-1}\boldsymbol{B}, \tag{6}$$

with $\boldsymbol{I}$ denoting the $N \times N$ identity matrix and $\boldsymbol{Z} = \mathrm{diag}(z_1, \ldots, z_N)$ the diagonal matrix of port resistances.

2.3. Nullors

The nullor, is a theoretical two-port element used in circuit theory to represent the ideal behavior of various multi-port systems [14, 15]. It consists of two distinct one-port elements: the nullator and the norator (fig.1), both of which lack physical realization. The nullator imposes the constraints of zero voltage and zero current at its port, whereas the norator permits arbitrary values for these variables [16]. Consequently, the nullor is defined by the constitutive equation

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{7}$$

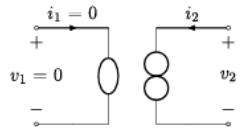


Figure 1: Nullor circuit symbol. the nullator is represented with an ellipse (port 1), while the norator with two circles (port 2).

Circuit analysis involving nullors relies on two complementary formulations: the voltage-based network $V - Net$ and the current-based network $I - Net$. In the $V - Net$ approach, the system is solved using voltage constraints, where the nullator imposes zero voltage and current, behaving as a short circuit, while the norator allows arbitrary values, acting as an open circuit. Conversely, in the $I - Net$ approach, the system is solved using current constraints, leading to an interpretation in which the nullator behaves as an open circuit while the norator functions as a short circuit [17].

2.4. Canonical Piecewise-Linear (CPWL) Modeling of Nonlinearities

An efficient strategy for modeling nonlinearities in the WDF framework is the Canonical Piecewise-Linear (CPWL) representation [8], which approximates nonlinear $i - v$ characteristics using a set of affine segments:

$$i(v) \approx m_k v + q_k \quad \text{for} \quad v \in [v_k, v_{k+1}]. \tag{8}$$

This formulation enables closed-form reflection coefficients per segment, bypassing costly iterative solvers.

2.5. Wave Digital Implementation of the MOSFET as a One-Port Element

The modeling of nonlinear three-terminal devices in the Wave Digital framework was first formalized by Bernardini et al. [18], who derived a general implicit wave-mapping approach for arbitrary constrained topologies. When such devices—e.g., MOSFETs in diode-connected mode—are subject to the condition $v_{GS} = v_{DS}$, they can be reduced to nonlinear one-port elements. This simplification enables direct integration of their i–v characteristics into the WD structure, reducing modeling complexity while preserving passivity and compatibility.

2.6. Scattering Iterative Method (SIM) description

The Scattering Iterative Method (SIM) provides a structured approach to iteratively resolve nonlinear wave interactions in complex networks, offering a robust solution strategy for handling non-analytic components within the WD framework [17]. At each iteration k, the SIM resolves the implicit nonlinearities by alternating two steps. First, in the *Local Scattering Stage*, each nonlinear one-port independently computes its reflected wave $b_n^{(k)}$ by solving its local constitutive relation (e.g. via a root-finding or CPWL segment lookup), using the previous incident-wave $a_n^{(k-1)}$ as input. These port-level updates are fully parallelizable. Second, in the *Global Scattering Stage*, the vector of reflected waves $\mathbf{b}^{(k)}$ is propagated through the network's scattering topology to produce the new incident-wave vector

$$\mathbf{a}^{(k)} = S\,\mathbf{b}^{(k)}, \tag{9}$$

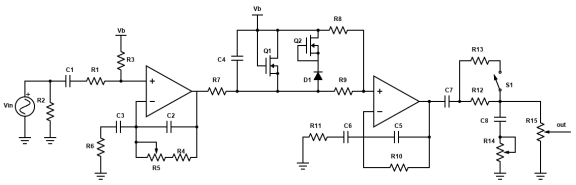


Figure 2: Fulltone OCD circuit.

where S is applied implicitly via local adaptor rules. The process iterates until the relative change $|\mathbf{a}^{(k)} - \mathbf{a}^{(k-1)}\|_2 < \xi$ for a small tolerance ξ (e.g. 10^{-8}), ensuring convergence to a self-consistent wave solution.

3. CIRCUIT OVERVIEW AND WD IMPLEMENTATION

The Fulltone OCD pedal's analog schematic (fig. 2) can be partitioned into three primary functional stages. First, the input stage consists of a high-pass RC filter followed by a non-inverting operational amplifier configured to provide gain and impedance buffering; this stage sets the overall gain and establishes the bias point for the subsequent nonlinear section. Second, the clipping stage employs a single diode in conjunction with two MOSFETs arranged in the feedback path of a second op-amp; the diode provides asymmetric soft clipping while the MOSFETs further shape the distortion response and bias conditions. Third, the output stage is composed of a simple passive low-pass/tone control network and a series output resistor, which together shape the high-frequency content and isolate the pedal from downstream loads. This same tripartite structure is preserved in the Wave Digital model implemented in MATLAB.

3.1. Stage 1: Modeling of the Input Amplifier

Referring to the schematic of the OCD pedal (Fig. 2), the first stage is implemented as a non-inverting amplifier. The free parameters of the linear elements are set to meet the relative adaptation conditions (Section 2.1). The operational amplifier is replaced by a nullor-norator pair, following the methodology introduced in Section 2.3. The topology resulting from this substitution is used to derive the associated voltage and current graphs. The decomposition into spanning tree and cotree follows standard WDF graph-based procedures (see [17] for nullor modeling and [12] for graph-based WDF construction). Based on this decomposition, the connectivity matrices Q_V and Q_I are constructed, allowing the scattering matrix to be computed using (5). The reflected wave vector is then calculated using (4).

3.2. Stage 2: Modeling of the Nonlinear Clipping Network

All linear elements are transformed into their discrete-time WD equivalents using the bilinear transform, ensuring passivity as outlined in Section 2.1. The operational amplifier is incorporated by replacing it with a nullor-based model, which is then absorbed into the connection network, as detailed in Section 2.3.The MOSFETs are arranged in a diode-connected configuration and biased to operate solely in saturation. Following the strategy of Section 2.5, we therefore employ a one-port formulation. Two different strategies are adopted to model the nonlinearities of the circuit. In the first one, the diode and the two MOSFETs are treated as independent one-port nonlinear elements. Their current-voltage $i - v$ characteristic curves are sampled and then approximated using a CPWL representation, as described in Section 2.4. These CPWL-modeled nonlinear one-ports, along with the linear and nullor-based op-amp elements, form a local nonlinear subnetwork. The global resolution of this entire stage is achieved at each sampling instant by employing the Scattering Iterative Method (Section 2.6). The SIM iteratively coordinates the local solutions from each CPWL-modeled nonlinear element with the global scattering behavior of the linear and op-amp network. At each iteration, the reflected waves from the nonlinear elements are updated based on their CPWL characteristics, and these are then propagated through the scattering matrix of the linear network to determine the new incident waves for the next iteration. This process continues until convergence is met within the predefined tolerance $\xi = 10^{-6}$.
In the second strategy, the entire nonlinear network is collapsed into a single adapted one-port by enforcing a zero-reflection condition on its distortion-stage scattering matrix. A symbolic solution yields a closed-form port impedance that exactly matches the combined nonlinear $i - v$ behavior. This computation is performed offline. At runtime,the nonlinear port uses this fixed impedance, forward propagation through the linear adaptors yields the incident wave at this composite node, a single CPWL lookup generates the reflected wave instantly, and a final scattering pass reintegrates it into the network. This algebraic adaptation replaces the iterative loop with one constant-time CPWL evaluation.

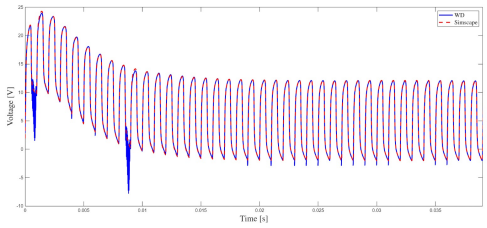
3.3. Stage 3: Modeling of the Output Network

The output stage is realized as a fixed seven-port network combining the tone potentiometer, output resistor, bypass capacitors, and load. All port impedances are collected in the diagonal matrix Z_{out}. A single 3×7 cut-set matrix B_{out} encodes the interconnection topology. The corresponding 7×7 scattering matrix S_{out} is computed following (6). At runtime, the known outgoing-wave vector $\mathbf{b}_{\text{out}}$ (driven by capacitor states and the preceding stage's output) is assigned, and the incident-wave vector is evaluated with (4) from which the output voltage is recovered exploiting (1) and (2).

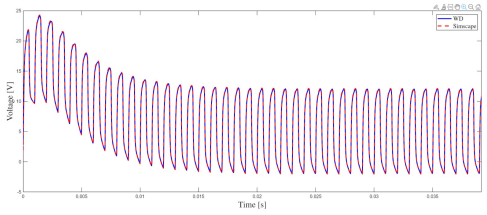
4. RESULTS AND DISCUSSION

To evaluate the accuracy of the proposed wave digital (WD) models[1], we compared their outputs to a high-fidelity reference simulation performed in Simscape, using custom MOSFET blocks (Table 2). Both WD implementations were driven by the same test signal: a 1kHz sine wave at 1V peak amplitude, over a total simulation time of 1s. Figure 3 compares the output voltages of the two WD implementations (solid blue) against the Simscape reference (dashed red) over the first 40ms of simulation. In both cases, an initial transient phase lasting approximately 10ms is observed, primarily due to charge accumulation and the nonlinear dynamic settling of the circuit. In the first implementation strategy, shown in Figure 3a, although some discrepancies appear during the transient, the WD output closely follows the reference waveform in both amplitude and shape once steady-state is reached. The RMS error of $152.3mV$, evaluated as $\text{RMS\_error} = \sqrt{\frac{1}{N}\sum_{n=1}^{N}\big(V_{\text{out}}[n] - V_{\text{sim}}[n]\big)^2}$, confirms the high accuracy of the model. However, the high computational load leads to a markedly low real-time performance ratio, measured at $0.07x$. In

[1] https://github.com/stepoliste/OCD/tree/main



(a) OCD output signal V_{out}



(b) OCD output signal V_{out}.

Figure 3: comparison between WD implementation and Simscape simulation. (a) First strategy, (b) second strategy.

contrast, Figure 3b illustrates the results from the second implementation strategy, in which the entire nonlinear feedback network is collapsed into a single adapted port. This version achieves a closer match to the Simscape reference even during the transient phase, with a lower RMS error of $100.6mV$ compared with the first modeling strategy and a better real-time performance, showing a dramatic improvement in efficiency with a real-time performance ratio of $3.59x$. Although both approaches faithfully reproduce the circuit's behavior, the second method trades off modularity for performance. By collapsing all nonlinear components into a unified structure, the model loses the internal separation between circuit elements. However, this allows the simulation to bypass iterative convergence and reduce per-sample computations to a single CPWL lookup and a global scattering step, resulting in significantly faster execution.

Table 2: Comparison of WD implementations against Simscape reference.

Implementation	RMS Error	real-time Ratio
1^{st} strategy	152.3 mV	0.07×
2^{nd} strategy	100.6 mV	3.59×

5. VST PLUGIN

To demonstrate the practical applicability of the proposed model, we opted for the second modeling strategy (Section 3.2), which collapses the nonlinear feedback stage into a single adapted port due to its superior computational efficiency. This implementation was integrated into a real-time VST plugin[2] developed using the JUCE framework, enabling interactive use in production environments. Several challenges were addressed to adapt the MATLAB-based model for real-time use. One primary issue involved the structure of the input signal. Unlike the original MATLAB implementation, which assumes a mono signal with a fixed sampling frequency, real-world audio workstations (DAWs) often handle stereo signals with variable sampling rates. Each processing stage of the pedal was modeled using the techniques previously described. Scattering matrices and capacitor values were directly transferred from the MATLAB experiments (Section 3) to the plugin implementation to avoid computationally expensive matrix inversions and to optimize performance. Additionally, potentiometer behavior was implemented and fine-tuned to further enhance the efficiency and responsiveness of the model in a real-time context. The GUI of the plugin exposes user-controllable parameters, reflecting the internal topology of the modeled circuit (Figure 4).

[2] https://github.com/stepoliste/OCD/tree/JUCE

Figure 4: GUI of the VST plugin.

5.1. Efficiency

We tested our VST plug-in in a real-time environment to measure its CPU usage at different buffer sizes, using a fixed sample rate of 48,000 Hz. The test was conducted using Ableton Live 12, a Scarlett 2i2 audio interface, and a 2.6 GHz Intel Core i7 six-core CPU. With a buffer size of 128 samples, the CPU usage was approximately 40%. Increasing the buffer size resulted in improved performance, with CPU usage dropping to 36% at 512 samples and 30% at 1024 samples.

6. CONCLUSIONS

In this work, we presented a wave digital (WD) model of a nonlinear analog audio circuit, demonstrating its ability to accurately reproduce the circuit's dynamic and nonlinear behavior. The model was validated against a high-fidelity Simscape simulation, used as a physical benchmark, showing a close match in both transient and steady-state responses. Two distinct implementation strategies were explored: the first maintained a modular structure by modeling each nonlinear component individually, while the second collapsed the entire nonlinear subnetwork into a single adapted port. Although both strategies provided faithful emulation, the second approach proved significantly more efficient in terms of real-time performance, achieving a lower computational cost by avoiding runtime iteration. However, this came at the expense of reduced modularity and interpretability. To demonstrate the model's practical applicability, the WD implementation was integrated into a real-time VST plugin using the JUCE framework, confirming the feasibility of using this approach in production environments. Overall, the results underscore the effectiveness of wave digital modeling as a robust and efficient framework for real-time emulation of complex nonlinear analog systems, offering a tunable balance between accuracy, modularity, and computational performance.

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