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Innovation from Engineers...

Section : AXI Protocol Overview

1. AXI Introduction
2. Types of AXI Bus
3. Channels on AXI
4. Main general AXI IP
5. AXI Interconnect
6. Example Design: VIVADO

AXI Protocols-Overview

Popular SoC Bus Protocol

- Core Connect
  - PLB/OPB/..
- Whishbone
  - Used by OpenCores IPs
- AXI
  - Advanced Extensible Interface, developed by ARM
  - Xilinx use ARM on its all of the FPGA Chip architecture
  - While many Xilinx SoC chip also consists of “ARM CPU Core”.
  - And Xilinx also have own Microblaze Architecture which also works on AXI interface protocol.

Reference: Mohammad Sadri

What is AXI?

- AXI is part of ARM AMBA, a family of micro controller buses first introduced in 1996. The first version of AXI was first included in AMBA 3.0, released in 2003. AMBA 4.0, released in 2010, includes the second version of AXI, AXI4.
- There are three types of AXI4 interfaces:
  - **AXI4**—for high-performance memory-mapped requirements.
  - **AXI4-Lite**—for simple, low-throughput memory-mapped communication (for example, to and from control and status registers).
  - **AXI4-Stream**—for high-speed streaming data.

Reference: UG1037, Xilinx

Summary of AXI4 Benefits

AXI4 is widely adopted in Xilinx product offerings, providing benefits to *Productivity*, *Flexibility*, and *Availability*:

- **Productivity**: By standardizing on the AXI interface, developers need to learn only a single protocol for IP.
- **Flexibility**: Providing the right protocol for the application:
  - AXI4 is for memory-mapped interfaces and allows high throughput bursts of up to 256 data transfer cycles with just a single address phase.
  - AXI4-Lite is a light-weight, single transaction memory-mapped interface. It has a small logic footprint and is a simple interface to work with both in design and usage.
  - AXI4-Stream removes the requirement for an address phase altogether and allows unlimited data burst size. AXI4-Stream interfaces and transfers do not have address phases and are therefore not considered to be memory-mapped.
- **Availability**: By moving to an industry-standard, you have access not only to the Vivado IP Catalog, but also to a worldwide community of ARM partners.
  - Many IP providers support the AXI protocol.
  - A robust collection of third-party AXI tool vendors is available that provide many verification, system development, and performance characterization tools. As you begin developing higher performance AXI-based systems, the availability of these tools is essential.

Reference: UG1037, Xilinx

AXI Channels

Both AXI4 and AXI4-Lite interfaces consist of five different channels:

- Read Address Channel
- Write Address Channel
- Read Data Channel
- Write Data Channel
- Write Response Channel

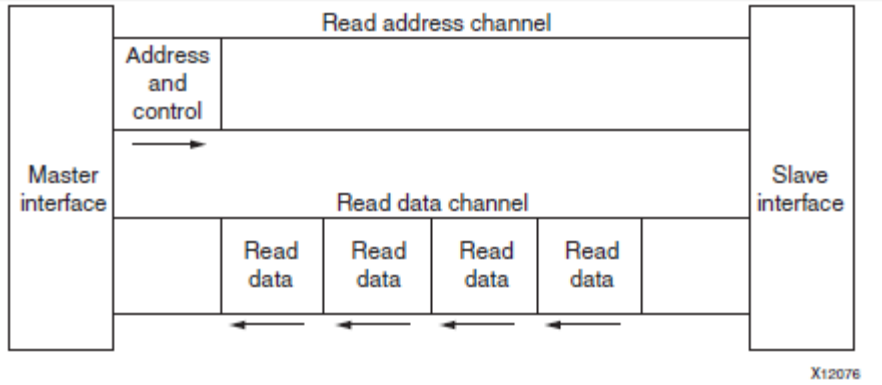


Figure 1-1: **Channel Architecture of Reads**

Figure 1-2 shows how a Write transaction uses the Write address, Write data, and Write response channels.

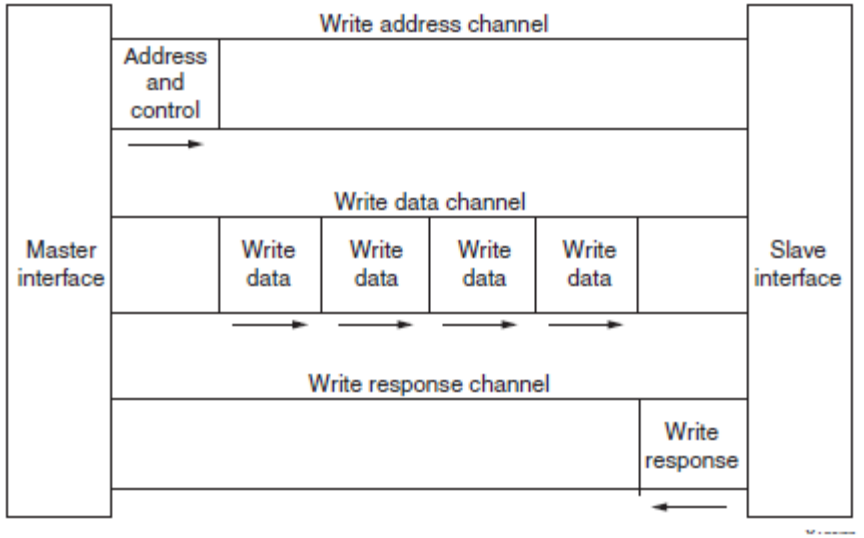
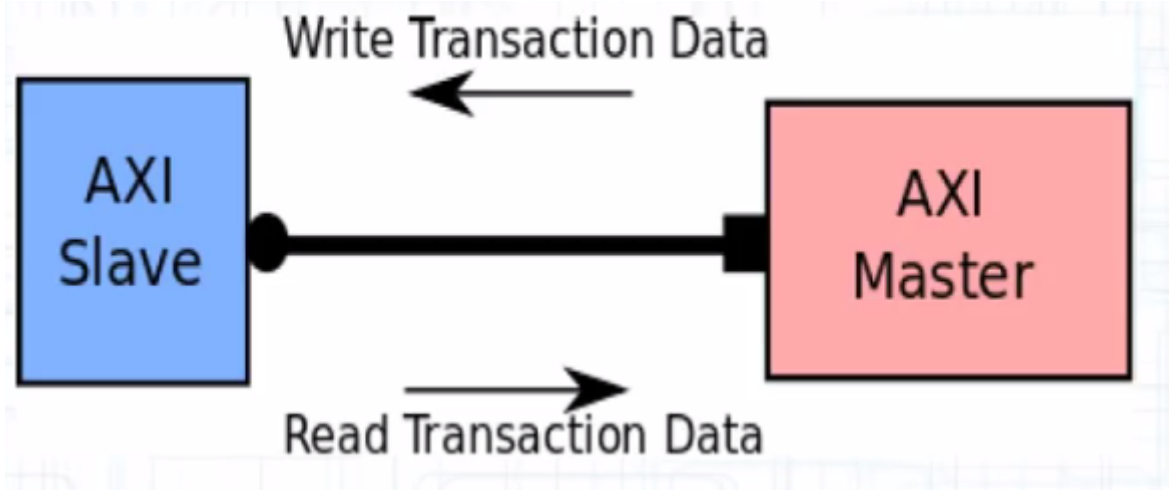


Figure 1-2: **Channel Architecture of Writes**

Reference: UG761, Xilinx

AXI Master vs. Slave

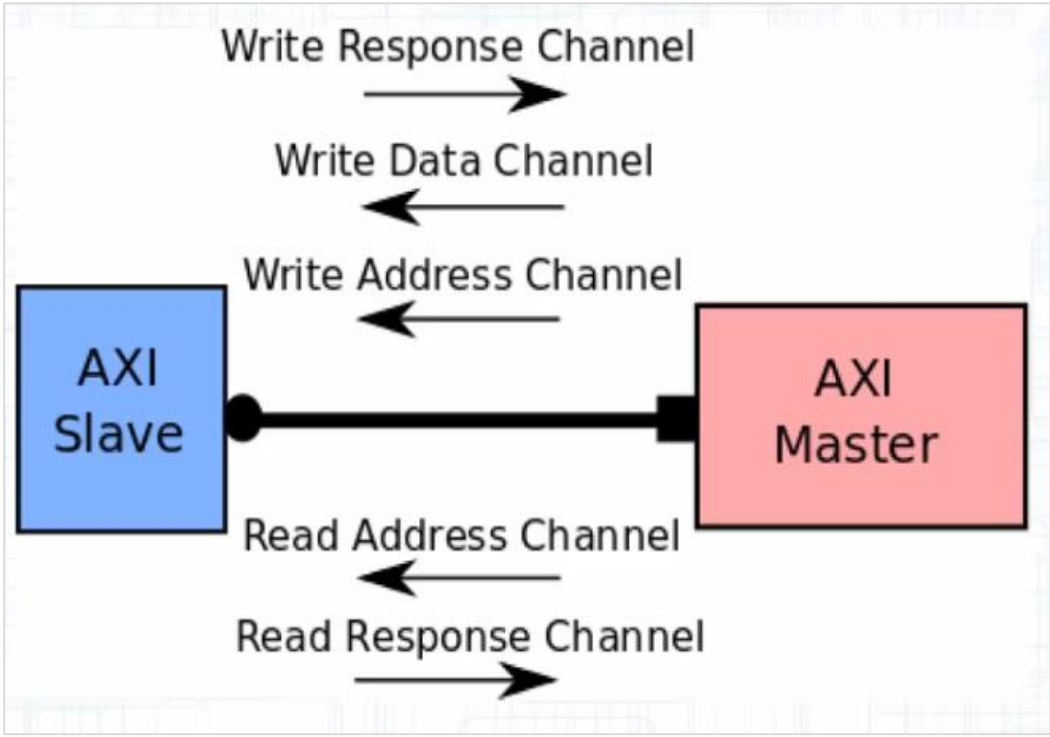
- AXI master and salve IP transact the data from one point in hardware to another point.
- Master IP can initiates the transaction
- Salve IP respond to the initiated transaction



Reference: Mohammad Sadri

Control Channels with AXI Master and Slave

1. Read Address Channel
2. Write Address Channel
3. Read Data Channel
4. Write Data Channel
5. Write Response Channel



Reference: Mohammad Sadri

AXI Infrastructure IP:

Some Examples:

- AXI Interconnect
- Processing System Reset
- AXI GPIO

- **Infrastructure IP**: An infrastructure IP is a building block used to help assemble systems. Infrastructure IP tends to be a generic IP that moves or transforms data around the system using general-purpose AXI4 interfaces and does not interpret data

  Examples of infrastructure IP are:

  1. AXI Register slices (for pipelining)
  2. AXI FIFOs (for buffering/clock conversion)
  3. AXI Interconnect IP and AXI SmartConnect IP (for connecting memory-mapped IP together)
  4. AXI Direct Memory Access (DMA) engines (for memory-mapped to stream conversion)
  5. AXI Performance Monitors and Protocol Checkers (for analysis and debug)
  6. AXI Verification IP (for simulation-based verification and performance analysis)

  These IP are useful for connecting IP together into a system, but are not generally endpoints for data.

Reference: UG1037, Xilinx

AXI Interconnect IP

1. AXI Interconnect help us to
   - ➢ Can connect different number of master and different number of slave IP or ports of IP.
   - ➢ Example1 : Connect one AXI Master with multiple Slaves
   - ➢ Example 2: Multiple AXI Master need to communicate to one AXI Slave.
2. It can also
   - ❖ Do Width conversion
   - ❖ AXI3 to AXI4 conversion
   - ❖ Clock Domain Transformation
   - ❖ Provide register slice, FIFOs

The AXI Interconnect core IP (axi_interconnect) connects one or more AXI memory-mapped master devices to one or more memory-mapped slave devices. The AXI interfaces conform to the AMBA® AXI version 4 specification from ARM®, including the AXI4-Lite control register interface subset.

Note: The AXI Interconnect core IP is intended for memory-mapped transfers only; AXI4-Stream transfers are not applicable. IP with AXI4-Stream interfaces are generally connected to one another, and to DMA IP.

The AXI Interconnect core IP is provided as an encrypted, non-licensed (free) pcore in the Xilinx Platform Studio software.

AXI Interconnect Core Features

The AXI Interconnect IP contains the following features:

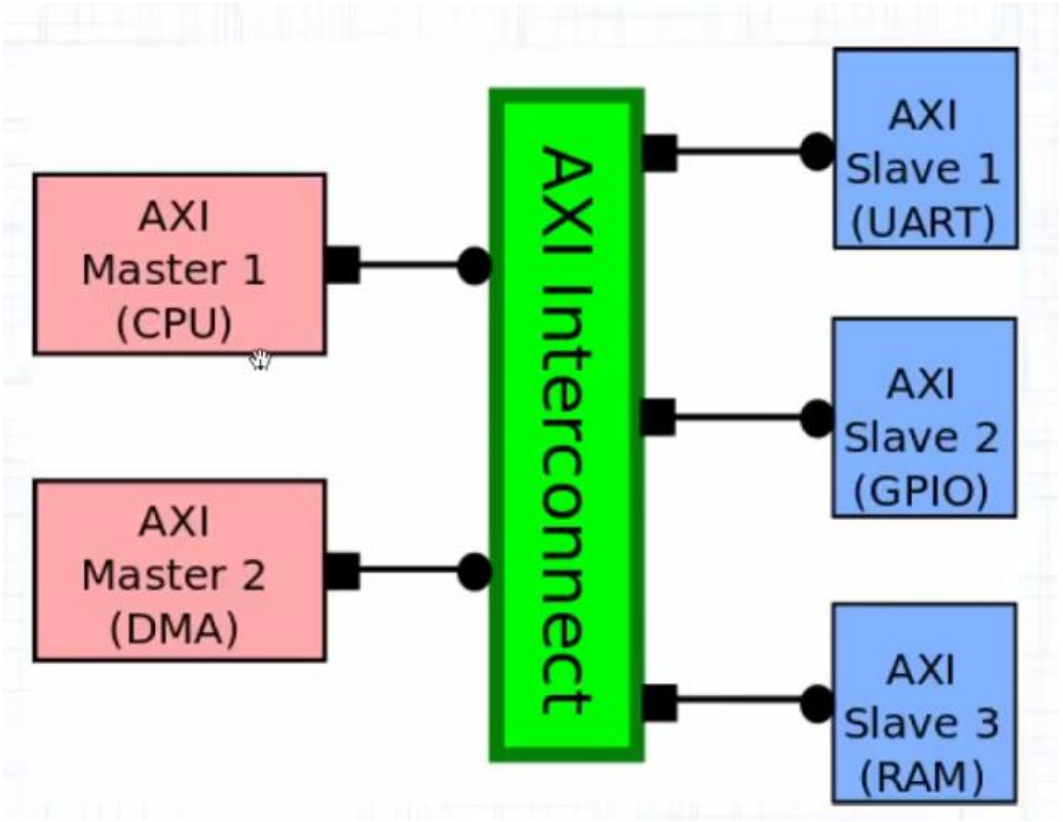
- AXI protocol compliant (AXI3, AXI4, and AXI4-Lite), which includes:
  - Burst lengths up to 256 for incremental (`INCR`) bursts
  - Converts AXI4 bursts >16 beats when targeting AXI3 slaves by splitting transactions.
  - Generates `REGION` outputs for slaves with multiple address decode ranges
  - Propagates `USER` signals on each channel, if any; independent `USER` signal width per channel (optional)
  - Propagates Quality of Service (QoS) signals, if any; not used by the AXI Interconnect core(optional)
- Interface data widths:
  - AXI4: 32, 64, 128, or 256 bits.
  - AXI4-Lite: 32 bits
  - 32-bit address width

Reference: UG761, Xilinx

AXI Interconnect Core Use Models

- The AXI Interconnect IP core connects one or more AXI memory-mapped master devices to one or more memory-mapped slave devices.
- The following subsections describe the possible use cases:
  1. Conversion Only
  2. N-to-1 Interconnect
  3. 1-to-N Interconnect
  4. N-to-M Interconnect (Sparse Crossbar Mode)

Example of AXI Interconnect in connection



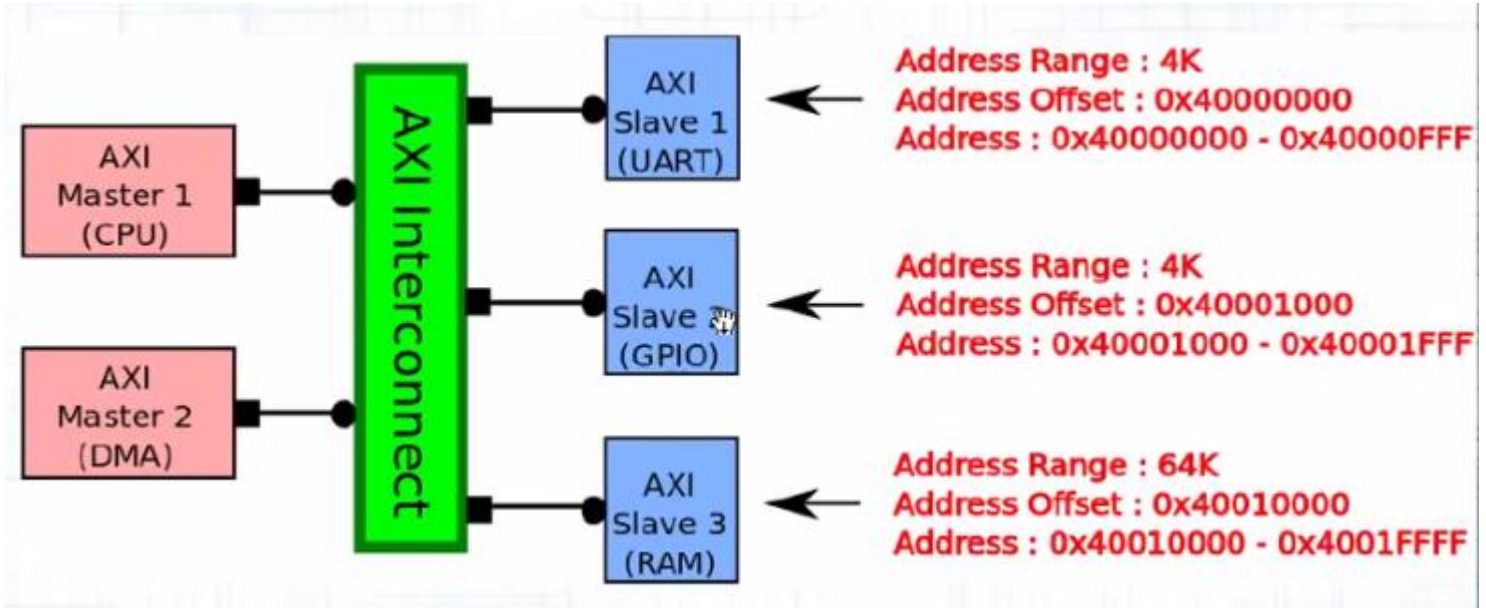
Reference: Mohammad Sadri

How the communication via interconnect work?

Addressing the Slave IP Port/Registers

General Rules:

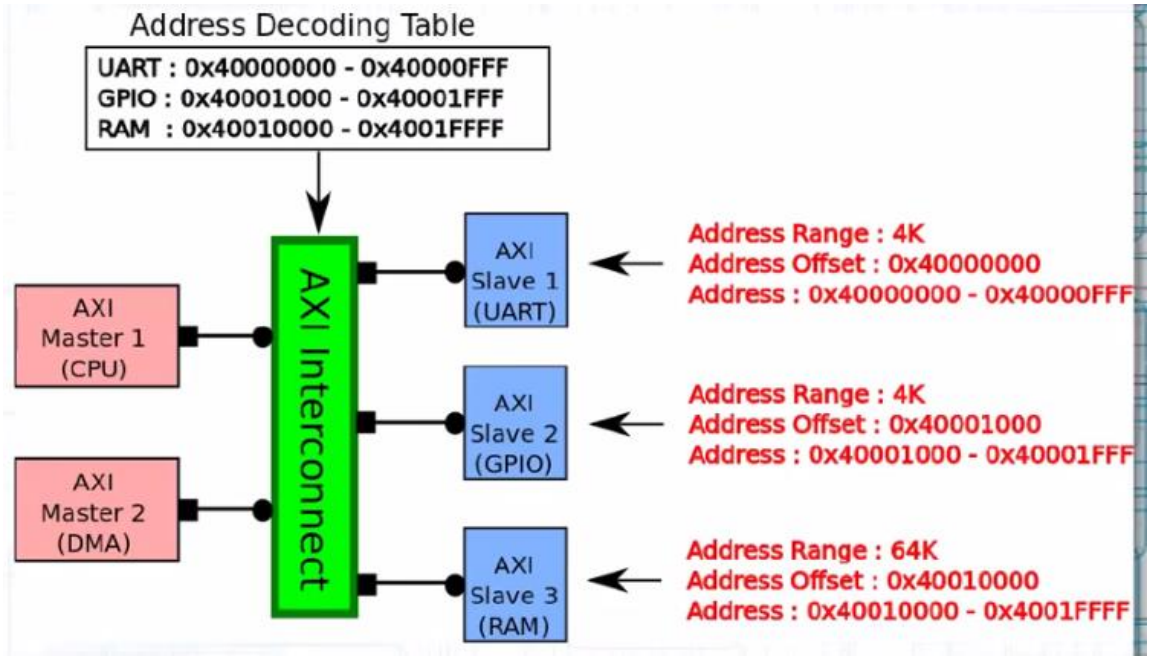
1. The address of one slave should not overlap to another one.
2. Address region must be separated completely.



Reference: Mohammad Sadri

Address Decoding by AXI Interconnect

- For sending and receiving data to/from master/slave

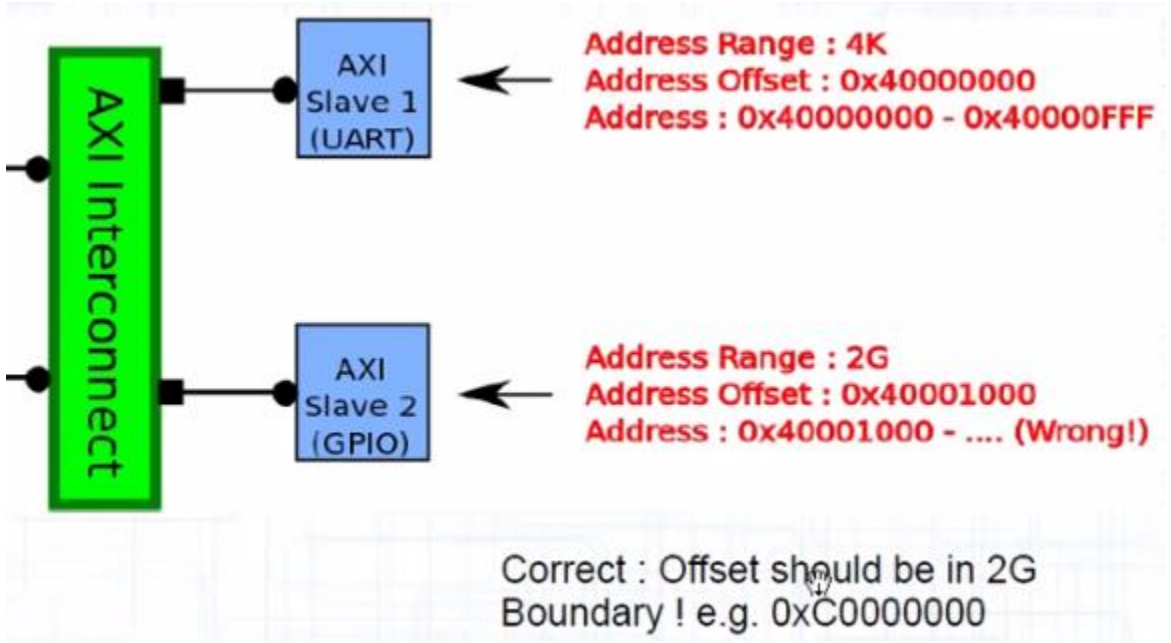


Reference: Mohammad Sadri

Address Alignment Rule

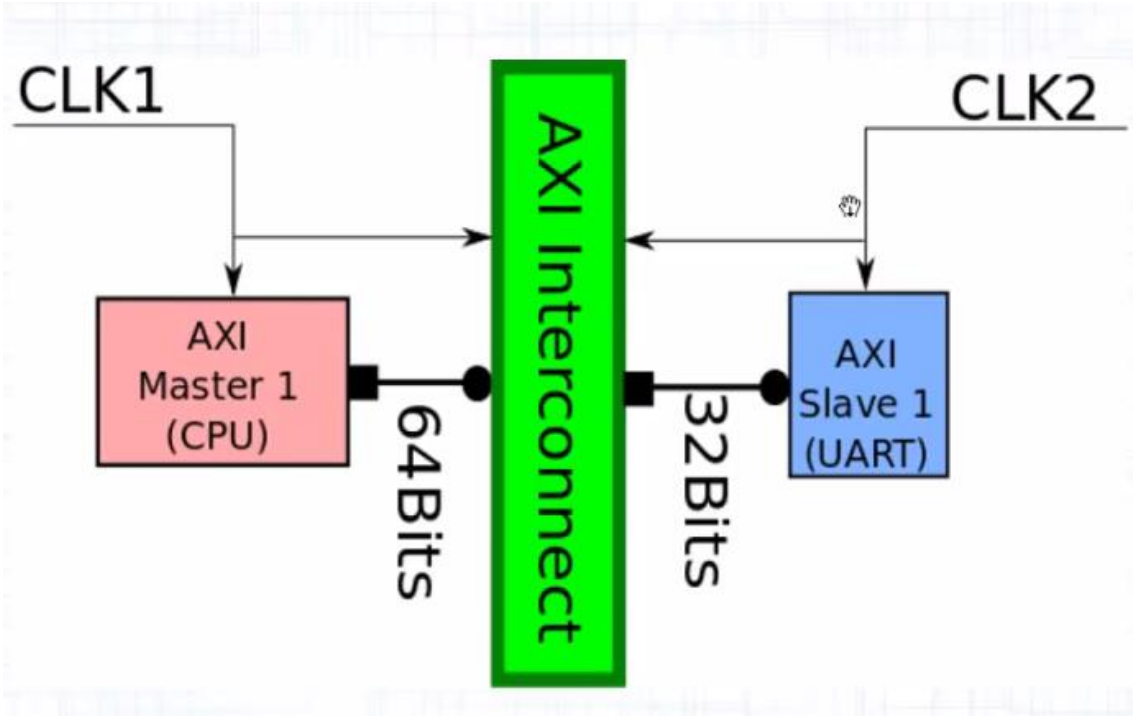
- This rule is for interconnecting high address range based address with the low address range based address.
- We cant give address to new IP from the last address of another one.

- Though VIVADO have “Auto Assign” option on Address Editor which works very well.



How AXI Interconnect allow to change clock domains?

- Example➔



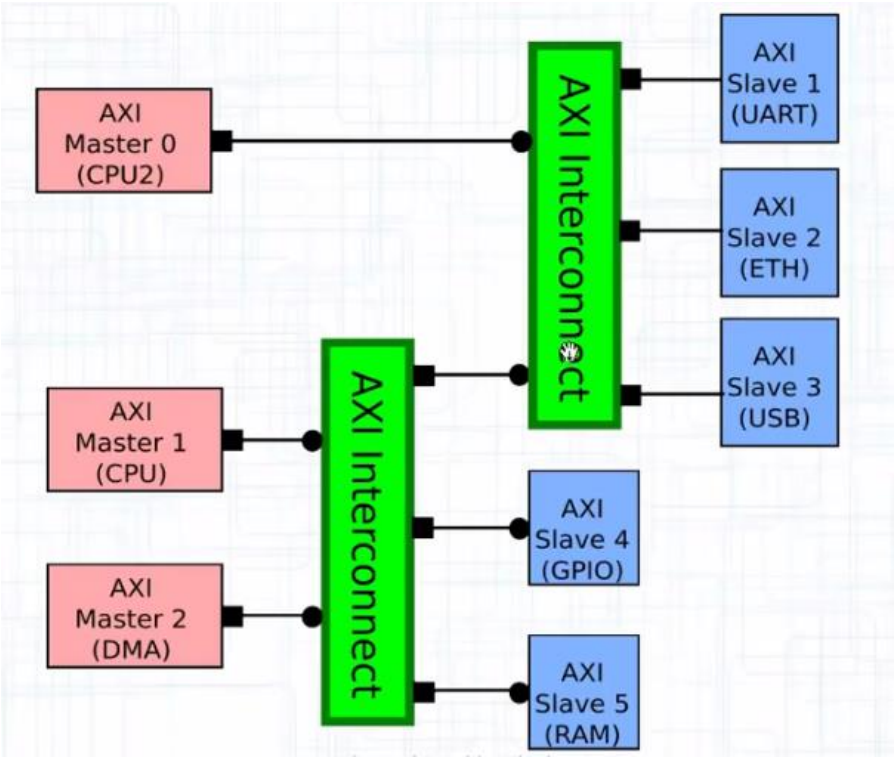
Reference: Mohammadsadegh Sadri

Hierarchical AXI Interconnects

❖This type of connection needed when:

1. There is limited number of AXI interconnect port limited. When number of slave is larger then the AXI interconnect ports.
2. Creating the design expandable when needed, so that the number of slaves can be added on the design later when needed.
3. With separate cluster, we can also create “Hierarchy of group of IP” which help to group and work on design.

❖In the design, the AXI Master 1 and DMA can access any of AXI slave IP while CPU2 can only access UART, ETH and USB.



Reference: Mohammadsadegh Sadri

AXI SmartConnect

- AXI SmartConnect is a drop-in replacement for the AXI Interconnect v2 core.
- AXI SmartConnect is more tightly integrated into the Vivado design environment to automatically configure and adapt to connected AXI master and slave IP with minimal user intervention.

Key Features and Benefits

- Up to 16 Slave Interfaces (SI) and up to 16 Master Interfaces (MI) per instance
- Instances of SmartConnect can be cascaded to interconnect a larger number of masters/slaves or for organizing the interconnect topology
- AXI Protocol compliant
- Burst transactions are automatically split, as needed, to remain AXI compliant
- Interface Data Widths (bits):
  - AXI4 and AXI3: 32,64,128,256,512 or 1024
  - AXI4-Lite: 32 or 64-bit
- Transactions between interfaces of different data widths are automatically converted by AXI SmartConnect

AXI Data Transfer Methods

Memory Mapped vs Stream Data Transfer

- Number of channel on Memory Mapped are 5 [3 channel for write transaction and 2 channel for read transaction].
- Number of channel needed for Streaming mode is just 1.

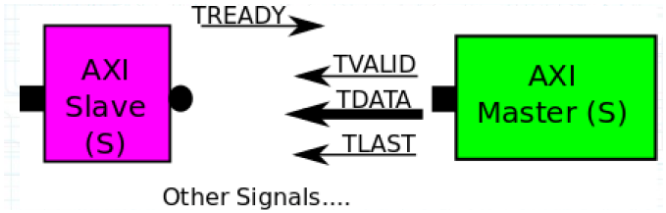


Figure: Streaming Channel details

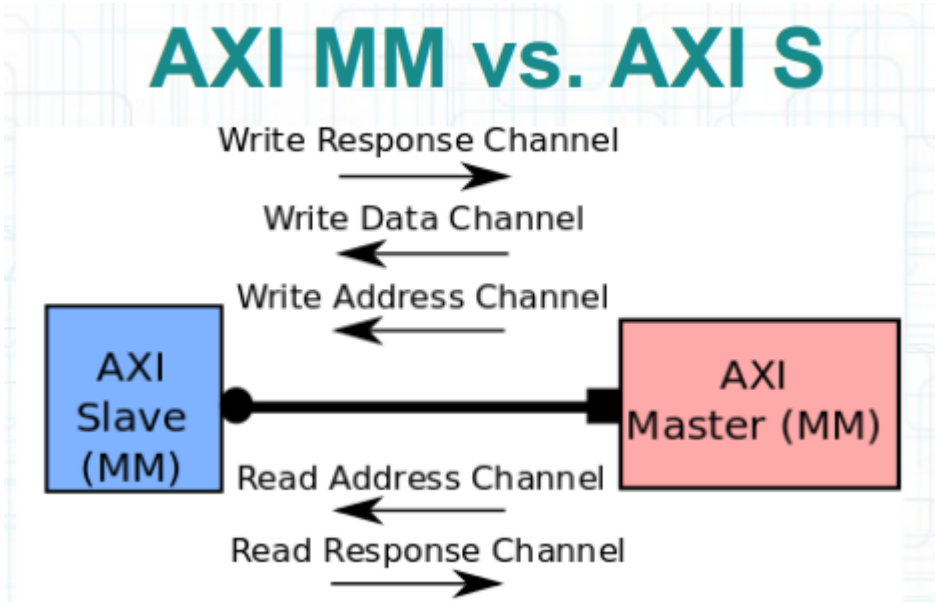


Figure: Memory Mapped Interface

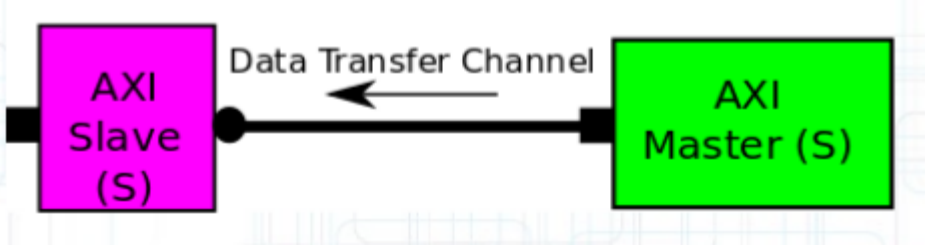


Figure: Streaming Interface

Reference: Mohammadsadegh Sadri

Thank You!