ECE 271 Design Arrject 12/6/2019 Alexander Eamons VGA Register clk Clock write write rout # X-next 6 r-out[3.0] x-next [5..0] g-out 4 g-out[3.0] y_next[5..0] y-next 16 b-out it x-write 16 X-write[5..0] 6-04[3.0] y-write,6 y-write[5.0] cwrite 13 r_write[2.0] g-Write[2..0] gwrite,3 bwrite,3 b-write[2.0]