S5K33DXX

1/3" VGA 7 μm Pixel Indirect ToF Sensor

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Data Sheet

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Chip Handling Guide

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2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

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Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

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Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

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Revision History

Revision No.	Date	Description	Author(s)
0.00	November 25, 2018	• Initial draft	Amit Eisenberg, Min-Sun Keel
0.01	December 11, 2018	• Table 20 has been corrected	Min-Sun Keel
0.02	June 28, 2019	• Table 1 modified with descriptions for LD driver IC I/F pads • Figure 3, 5 and 9 modified for actual 4-tap phase map • Section 4.1.3 added to describe MSPI for LD Driver Control • Figure 24 modified by adding the MSPI block for LD Drive Control • Section 5.12.1 added for MIPI slow frame • Chapter 7 modified with section 7.2 and 7.3 • Chapter 8: register map added	Amit Eisenberg, Min-Sun Keel

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Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
RW	Read/Write	The application has permission to read and writes in the Register field. Written value effects on the next frame.
RW/R	Read/Write	The application has permission to read and writes in the Register field. Written value effects only on exit from stand-by.
RW/C	Read/Write	The application has permission to read and writes in the Register field. Changing value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write	The application has permission to read and writes in the Register field. Changing value may cause entering stand-by / software reset.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

1.1 Introduction

S5K33DXX is a highly integrated indirect Time-of-Flight (ToF) sensor aimed for 3D depth sensing. S5K33DXX has VGA resolution and 7 μm pixel. The camera is integrated in a ToF system that also includes a modulated light source in Infrared (IR) band which is controlled by S5K33DXX. S5K33DXX chip includes demodulation ToF pixel array, analog/mixed-signal processing circuit including modulation signal generation and transmission, image correction functionality, low-power depth calculation chain, and serial transmission using up to 2-lane MIPI transmitter.

It is fabricated by the Samsung CMOS image sensor process to realize a high-efficiency and low-power photo sensor. The sensor consists of 640×480 effective pixels (644×484 active pixels) that meet with the 1/3.2-inch optical format.

The indirect ToF depth sensing concept requires four different samples of the pixel data in four different phases to calculate its depth value.

This sensor is designed as a 4-tap sensor, which means each pixel can sample four phases of data simultaneously. Each phase is considered internally as an independent pixel so conceptually, a 4-tap pixel array is expanded to 1280x960 effective pixels.

It is designed for fast but low-power operation, delivering full resolution (1280x960) capture at up to 60 frames per second (fps) for raw image data.

This sensor also includes simple H/W depth engine that provides low-accuracy depth image for simple depth applications such as proximity sensing. The depth engine can be enabled only in certain sensor output modes.

This sensor has on-chip 12-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce pixel reset noise and Fixed-Pattern Noise (FPN). It incorporates on-chip camera functions such as defect correction, exposure setting, image scaling, depth and proximity sensing, and auto exposure statistics.

S5K33DXX CIS is programmable through a CCI or SPI serial interface and includes an on-chip One-Time Programmable (OTP) Non-Volatile Memory (NVM).

S5K33DXX is suitable for a low-power camera module with a 2.8 V/1.05 V power supply.

The main application of the sensor is to output RAW phase data that are translated to depth image by post processing (either in S/W or in H/W) at the back-end chip which is an Application Processor (AP).

1.2 Indirect Time-of-Flight Depth Sensing Concept

The basic concept of indirect ToF method for depth calculation is to illuminate a scene with a modulated light source; the modulation function can be a sine wave or rectangular pulse. In this case, it is assumed to be a sinusoidal modulation.

Figure 1   **Indirect Time-of-Flight Concept**

The reflected light is captured on a sensor and the phase shift between illuminated and reflected sine waves is used to calculate the depth value of each pixel in the sensor.

The reflected light is sampled at four different phases (with respect to the illuminating signal) to measure the phase shift.

Figure 2   **Time-of-Flight Demodulation Concept: 4-Phase Sampling**

The phase shift (φ) and depth (d) are calculated according to the following equations (A0, A1, A2, and A3 are integrated pixel data for the phase-sampling point at 0°, 90°, 180°, and 270°, respectively).

$$\varphi = \operatorname{atan}\left(\frac{A_1 - A_3}{A_0 - A_2}\right)$$
$$d = \frac{c}{2f_m}\frac{\varphi}{2\pi}$$

The depth is assumed to be related to objects in the first harmony of the sine wave, therefore, the maximum range (or, unambiguous range) is a simple function of the modulation frequency (c: Speed of light and f_m: Modulation frequency) as described in the following equations.

$$\text{range} = \frac{c}{2f_m}$$

For example, for 100 MHz of modulation frequency, the maximal detectable range is 1.5 m.

Parameters such as amplitude and intensity are referred as depth confidence level. Use the following equations to calculate amplitude and intensity.

$$\text{Amplitude: } A \propto \sqrt{(A_0 - A_2)^2 + (A_1 - A_3)^2}$$
$$\text{Intensity: } I = \frac{1}{4}(A_0 + A_1 + A_2 + A_3)$$

Depth precision is inversely dependent on the modulation frequency.

1.3 Sensor Readout Modes

S5K33DXX supports phase sampling in the following two ways:

- 4-tap: All four phases are available for each pixel.

- 2-tap: Only two phases, whose phase difference is 180°, are available for each pixel.

1.3.1 4-Tap Mode

In the 4-tap mode, each pixel can sample four different phase points due to four storage nodes. This mode requires only one frame to calculate a depth map. The photo-gate control signals such as PGA, PGB, PGC, and PGD, are generated to sample reflected light signal at 0°, 90°, 180° and 270° points, respectively, as illustrated in *Figure 3*.

Figure 3   4-Tap Pixel Structure and Photo-Gate Control Signals

1.3.2 2-Tap Mode

In the 2-tap mode, each pixel holds two different taps of data per frame, so two frames are required to generate one depth frame. A 2-tap mode can be configured from 4-tap mode with simple averaging between adjacent vertical pixel outputs within a pixel. The 2-tap and 4-tap modes can be selected by a register setting. PGA and PGB are 0° and 180° sampling signals at the even frames, and 90° and 270° sampling signals at the odd frames, respectively.

Figure 4   2-Tap Pixel Structure (Conceptual) and Photo-Gate Control Signals

1.3.3 Tap-Shuffle Mode

The tap-shuffle mode is a supplementary mode to eliminate FPN due to pixel tap and ADC mismatch. In this mode, the two out-of-phase taps (with 180° difference) are shuffled, thus each phase is read twice through different pixel position and different column ADC. This mode has better FPN performance and better SNR, by sacrificing motion blur performance due to doubled raw frame requirement.

(a)　　　　　　　　　　　　　　　　　　　　　　　　　　　(b)

Figure 5　　Tap-Shuffle Mode: (a) 4-Tap and (b) 2-Tap

1.3.4 Dual-Frequency (Phase-Unfolding) Mode

Two different modulation frequencies are used to extend the unambiguous range with minimal effect on depth precision. In the dual-frequency mode, the scene is illuminated and read by two different modulation frequencies, and the distance is calculated by finding the number of phase folding cycles. The calculation example is illustrated in *Figure 6*. The range is extended by the Greatest Common Divisor (GCD) of the two frequencies, f_{m1} and f_{m2}.

$f_{m1} = 100\ MHz$, $f_{m2} = 75\ MHz$ (GCD(100,75) = 25)

➔ $d_{max1} = 1.5\ m$, $d_{max2} = 2\ m$

Actual depth, $d_{actual} = d_{max1} \times N_1 + d_1 = d_{max2} \times N_2 + d_2$

N_1 and N_2 should be determined

($N_1 = 3$ and $N_2 = 2$ in this example)

Figure 6　　Dual-Frequency (Phase Unfolding) Example

1.4 Features

S5K33DXX supports the following features:

- VGA 4:3 indirect Time-of-Flight sensor with 4-tap outputs per pixel and 1/3.2" optics

- Unit pixel size: 7.0 μm

- Effective resolution: 640 (H) $\times$ 480 (V) for pixel array, 1280 (H) $\times$ 960 (V) for output raw image

- Active resolution: 644 (H) $\times$ 484 (V) for pixel array, 1288 (H) $\times$ 968 (V) for output raw image

- Color filter: None

- Shutter type: Electronic global shutter

- Max. normal frame rate: 60 fps @ 1288 $\times$ 968

- Data rate: 1,600 Mbps/lane (up to two lanes)

- ADC accuracy: 12 bits

- Dual sensor synchronization

- Interfaces:
    - Fine interface frequency control using additional dedicated PLL for EMI avoidance and integration flexibility
    - MIPI CSI2: Two lanes (1.6 Gbps per lane)
    - Output formats: RAW12

- Control interface:
    - SPI interface: Four-wire serial communication circuit up to 20 MHz
    - Camera Control Interface (CCI) high-speed I2C-compatible - Two-wire serial communication circuit up to 1 MHz

- 32 Kb on-chip OTP memory mapped BPC and chip ID

- Vertical and horizontal flip mode

- Continuous frame capture mode

- Vertical average readout: x2, x4

- Horizontal digital binning: x2, x4

- On-sensor depth chain

- Low-power proximity sensing mode

- Pixel skip readout function

- Mapped bad pixel correction

- Built-in test pattern generation

- Supply voltage: 2.8 V for analog, 1.8 V or 2.8 V for I/O, and 1.05 V for digital core supply

- Operating temperature: -20 $^\circ$C to +70 $^\circ$C

2 Pad Configuration

Figure 7   Top View of Chip Dimension

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

2.1 Pad Description

Table 1   Pad Description

Pad No.	Pad Name	Type	A/D	Description
1	TST	I	D	Test configuration pin (tie low in normal operation)
2	VDDD	P	D	Digital power (1.05 V)
3	VDDD	P	D	Digital power (1.05 V)
4	VSSD	G	D	Digital ground (0 V)
5	VSSD	G	D	Digital ground (0 V)
6	MCLK	I	D	Main clock input
7	VSSIO	G	A	I/O ground (0 V)
8	VDDIO	P	A	I/O power (1.8 V)
9	VDDA_M	P	A	Analog power (2.8 V)
10	VDDD	P	D	Digital power (1.05 V)
11	VSSD	G	D	Digital ground (0 V)
12	M_DNDATA0	O	A	MIPI data lane 0 (negative)
13	M_DPDATA0	O	A	MIPI data lane 0 (positive)
14	M_DNDATA1	O	A	MIPI data lane 1 (negative)
15	M_DPDATA1	O	A	MIPI data lane 1 (positive)
16	VSSD	G	D	Digital ground (0 V)
17	M_DNCLK	O	A	MIPI clock lane (negative)
18	M_DPCLK	O	A	MIPI clock lane (positive)
19	VDDD	P	D	Digital power (1.05 V)
20	(NC)	-	-	No connection
21	(NC)	-	-	No connection
22	(NC)	-	-	No connection
23	(NC)	-	-	No connection
24	VSSD	G	D	Digital ground (0 V)
25	VDDD	P	D	Digital power (1.05 V)
26	VDDD	P	D	Digital power (1.05 V)
27	VDDD	P	D	Digital power (1.05 V)
28	VSSD	G	D	Digital ground (0 V)
29	VSSD	G	D	Digital ground (0 V)
30	SE	O	D	Modulation enable flag - used to drive LD driver IC
31	MSE	O	D	Master SPI M_CSN: Serial communication enable
32	VDDIO	P	A	I/O power (1.8 V)
33	VSSIO	G	A	I/O ground (0 V)
34	RSTN	I	D	Master reset, active low (XSHUTDOWN)
35	I2C_SPI_N_SEL	I	D	SPI/IIC select (1: IIC, 0: SPI)
36	VSYNC	O	D	Vertical sync. output

Pad No.	Pad Name	Type	A/D	Description
37	VSYNC_IN	I	D	Vertical sync. input to enable dual sensor function
38	HSYNC	O	D	Horizontal sync. output
39	(NC)	-	-	No connection
40	VSSA	G	A	Analog ground (0 V)
41	VDDA	P	A	Analog power (2.8 V)
42	VSSA	G	A	Analog ground (0 V)
43	VDDD	P	D	Digital power (1.05 V)
44	VSSD	G	D	Digital ground (0 V)
45	VDDPG	P	A	Photo-Gate Driver (PGD) power (1.05 V)
46	VSSA	G	A	Analog ground (0 V)
47	VDDPG	P	A	PGD power (1.05 V)
48	VSSA	G	A	Analog ground (0 V)
49	VDDPG	P	A	PGD power (1.05 V)
50	VSSA	G	A	Analog ground (0 V)
51	VDDPG	P	A	PGD power (1.05 V)
52	VSSA	G	A	Analog ground (0 V)
53	VSSA	G	A	Ground (0 V)
54	VDDMD	P	A	Power (2.8 V)
55	MD_CKP	O	A	Differential modulation clock output (positive)
56	MD_CKN	O	A	Differential modulation clock output (negative)
57	VSSD	G	D	Digital ground (0 V)
58	VDDD	P	D	Digital power (1.05 V)
59	VSSA	G	A	Analog ground (0 V)
60	VDDA	P	A	Analog power (2.8 V)
61	VSSA	G	A	Analog ground (0 V)
62	(NC)	-	-	No connection
63	(NC)	-	-	No connection
64	(NC)	-	-	No connection
65	(NC)	-	-	No connection
66	(NC)	-	-	No connection
67	(NC)	-	-	No connection
68	(NC)	-	-	No connection
69	(NC)	-	-	No connection
70	VNTG	G	A	NTG voltage
71	VNTGX	G	A	NTGX voltage
72	VNSG	G	A	NSG voltage
73	VNOG	G	A	NOG voltage
74	VTG	P	A	TG voltage
75	VRGSL	P	A	RGSL voltage

Pad No.	Pad Name	Type	A/D	Description
76	VSSA	G	A	Analog ground (0 V)
77	VDDA	P	A	Analog power (2.8 V)
78	VTGX	P	A	TGX voltage
79	VSG	P	A	SG voltage
80	VOG	P	A	OG voltage
81	VSSA	G	A	Analog ground (0 V)
82	VDDPG	P	A	PGD power (1.05 V)
83	VSSD	G	D	Digital ground (0 V)
84	VSSD	G	D	Digital ground (0 V)
85	VDDD	P	D	Digital power (1.05 V)
86	VDDD	P	D	Digital power (1.05 V)
87	VSSA	G	A	Analog ground (0 V)
88	VDDPG	P	A	PGD power (1.05 V)
89	VSSA	G	A	Analog ground (0 V)
90	VDDPG	P	A	PGD power (1.05 V)
91	VSSA	G	A	Analog ground (0 V)
92	VDDPG	P	A	PGD power (1.05 V)
93	SDI	B	D	SPI mode: Serial data input, IIC mode: IIC data
94	SCK	I	D	SPI mode: Serial clock input, IIC mode: IIC input clock
95	SDO	O	D	SPI mode: Serial data output, IIC mode: no connection
96	XCE	I	D	SPI mode: Serial communication enable, IIC mode: IIC slave address selection
97	VSSD	G	D	Digital ground (0 V)
98	VSSD	G	D	Digital ground (0 V)
99	VDDD	P	D	Digital power (1.05 V)
100	VDDD	P	D	Digital power (1.05 V)
101	VDDIO	P	A	I/O power (1.8 V)
102	VSSIO	G	A	I/O ground (0 V)
103	GPIO_3	B	D	Master SPI M_SDIO: Serial data input/output
104	GPIO_2	O	D	Master SPI M_SCK: Serial clock
105	GPIO_1	I	D	Emergency flag input from LD driver IC
106	VDDA_M	P	A	Analog power (2.8 V)
107	VSSD	G	D	Digital ground (0 V)
108	VDDD	P	D	Digital power (1.05 V)

2.2 Application Circuit

Figure 8 illustrates a module application circuit.

Figure 8   Module Application Circuit

2.3 Pixel Array Information

Figure 9 illustrates a diagram of pixel array.

Figure 9   Pixel Array Diagram

3 Power Sequence

3.1 Operating Modes

Sensor module has four operating modes such as power-off, hardware standby, software standby, and streaming (*Table 2*). Transition from one mode to another is achieved by issuing the appropriate mode command through the CCI serial control interface, the RSTN (XSHUTDOWN) signal changing state, and the power supplies. By default, S5K33DXX powers up with the CSI-2 serial data interface enabled. *Figure 10* illustrates the valid mode changes for the sensor module.

Figure 10   System State Diagram

Table 2   Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off
Hardware standby	No communication with the sensor is possible Internal core power shut-off only by external VDDD and VDDA power down.
Software standby	CCI communication with sensor is possible Core is powered on.
Streaming	The sensor module is fully powered and streams the image data on the CSI-2 bus

Table 3 describes the registers that control the operating mode of the camera module.

Table 3   Operating Mode Registers

Start	Reset	Name	Type	Width	Description
0x0100	0x00	api_rw_general_setup_mode_select	RW/SR	[0:0]	0 = Software standby 1 = Streaming (active video)

3.2 Power-Up Sequence

The digital and analog supply voltages can be powered up in any order, for example, VDDD then VDDA, or VDDA then VDDD.

After power up, RSTN (XSHUTDOWN) should be low when the power supplies are brought up, then the sensor module goes into hardware standby mode. As long as RSTN is low and VDDD is down, the sensor module stays in hardware standby mode.

The assertion of RSTN ensures that the CCI register values are initialized correctly to their default values.

When RSTN goes to high, all PADs exit from fail-safe mode, and switch to normal operating mode.

Either MCLK can be initially low and then enabled during software standby mode or MCLK can be a free running clock.

NOTE:
1. At hardware standby mode, external VDDD and VDDA should be off.
2. External clock (MCLK) is recommended to be off in software standby mode to reduce power consumption.

Figure 11   Power-Up Sequence

Table 4   Power-Up Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
VDDA//VDDD/VDDIO rising time	t0	VDDA/VDDD/VDDIO may rise in any order. The rising separation can vary from 0 ns to indefinite.		ns
VDDD rising to RSTN (XSHUTDOWN) rising	t1	0.0	–	ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t2	10	–	µs
Minimum no. of MCLK (EXTCLK) cycles prior to the first CCI transaction	t3	23,000	–	MCLK cycles
PLL startup/lock time	t4	–	1	ms
DPHY initialization period (TINIT)	t5	0.1	–	ms
Entering streaming mode - The first frame start sequence	t6	+ the delay according to the coarse integration time value		-

3.3 Power-Down Sequence

The digital and analog supply voltages are powered down in any order, for example, VDDD then VDDA, or VDDA then VDDD.

Similar to the power-up sequence, the MCLK (EXTCLK) input clock is either gated or continuous.

If the CCI command to exit streaming is received when a frame of valid active data is being output, then the sensor module must wait for the frame end code before entering the software standby mode. Frame end code can come either after all frame pixels are transmitted or during the frame when next line transmission is completed - based on a configuration register. For more information, refer to S5K33DXX Application Note.

If the CCI command to exit streaming mode is received during the inter frame time, then the sensor module must immediately enter the software standby mode.

Figure 12   Power-Down Sequence

Table 5   Power-Down Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
Enter software standby CCI command-Device in software standby mode	t0		When outputting a frame of MIPI, the data waits for the MIPI frame end code before entering software standby; otherwise it enters software standby mode immediately.	–
Minimum number of MCLK (EXTCLK) cycles after the last CCI transaction or MIPI frame end code	T1	512	–	MCLK cycles
Last CCI transaction or MIPI frame end code - RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD or VDDA falling	t3	0.0	–	ns
VDDA/VDDD/VDDIO falling time	t4		VDDA/VDDD/VDDIO may fall in any order. The rising separation can vary from 0 ns to indefinite.	

NOTE:

1.   For minimal power during hardware standby mode, external VDDD should be turned off.

3.4 Software Standby Mode Sequence

Entering software standby mode is the same as entering hardware standby mode but without RSTN (XSHUTDOWN) assertion to low and without applying external VDDD power down.

There are several options to define how the last frame before entering the software reset, according to the following parameter described in *Table 6*.

Table 6   Abort Frame Timing Transition Options upon Entering S/W Reset

Timing Transition Type	Setting
abort_timing_on_sw_stby	0 = Abort timing immediately, even during read out
	1 = Abort timing after read out ends
	2 = Abort timing on end of frame

4 Control Interface

S5K33DXX control is performed using register writes. S5K33DXX can be controlled using the Camera Control Interface (CCI).

Table 7   SPI/CCI PAD Sharing

SPI	CCI
SDI	SDA
SCK	SCL
XCE	I2C_ID
SDO	–
I2C_SPI_N_SEL	

4.1 SPI Control Interface

S5K33DXX can use the SPI interface for control registers communication. SPI interface is illustrated in *Figure 13*.

Figure 13   SPI Control Interface

The following legend table describes SPI signals in *Figure 13*.

Pin Name	Description
XCE	Serial communication enable
SCK	Serial communication clock input
SDI	Serial data input
SDO	Serial data output

If it is not necessary to read the control registers and chip ID, the SDO pad can be left unconnected.

4.1.1 SPI Timing Definitions

Figure 14   Timing Diagram of SPI Write Mode 11

Figure 15   Timing Diagram of SPI Read Mode 11

Table 8   SPI Write/Read Timing Specification

Description	Symbol	Min.	Typ.	Max.	Unit
MCLK (external clock) frequency	Fext	6	–	64	MHz
SPI clock frequency	F [1]	–	–	Fext/3	
	F [2]	–	–	20	
SPI clock period	T	1/F	–	–	nSec
SPI clock duty cycle	Tdc	45	–	55	%
XCE negedge to SCK edge	Txce2ck	T	–	–	nSec
SCK posedge to XCE edge	Tck2xce	2T	–	–	
SCK to SDI setup time	Tsck2di	7	–	–	
SCK to SDI hold time	Thck2di	5	–	–	
SCK to SDO setup time	Tsck2do	T/2-20	–	–	
SCK to SDO hold time	Thck2do	T/2	–	–	

NOTE:

1. External clock is used.
2. PLL stable. Internal system clock can be set to maximum of 60 MHz.

Figure 16   SPI Write/Read Mode 00

4.1.2 SPI Sequences

Figure 17   SPI Write Sequence (1 Cycle)

Figure 18   SPI Read

4.1.3 3-Wire Master SPI Control Interface

Figure 19 illustrates the SPI interface.

Figure 19   Master SPI Control Interface

S5K33DXX has 3-wire master SPI control. It is designated to control the driver IC of IR-illuminator.

Master SPI can also connect to other types of slaves.

The master SPI interface is configured to operate in 3-wire SPI protocol. GPIO_3 operates as M_SDIO and can be used as either M_SDI or M_SDO for data according to configuration.

4.2 Camera Control Interface

S5K33DXX supports the Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5K33DXX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically, only the receiver and transmitter are connected to the CCI bus. This ensures a pure S/W implementation.

The CCI is different from the system I2C bus, but I2C-compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of the I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in the I2C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize these I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification can have additional features implemented to support I2C.

Figure 20　　Timing Diagram of CCI

Table 9　　I2C Standard Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for start condition	T_1	4.0	–	µs
Setup time for stop condition	T_2	4.0	–	
Data setup time	T_3	250	–	ns
Data hold time	T_4	0	3.45	µs
High period of the SCL clock	T_5	4.0	–	
Low period of the SCL clock	T_6	4.7	–	
Bus free time between stop and start conditions	T_7	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Table 10   I2C Fast Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T_1	0.6	–	μs
Setup time for stop condition	T_2	0.6	–	
Data setup time, external clock (MCLK) above 12.8 MHz	T_3	0.1	–	μs
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T_4	0	0.9	μs
High period of the SCL clock	T_5	0.6	–	
Low period of the SCL clock	T_6	1.3	–	
Bus free time between stop and start conditions	T_7	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Table 11   I2C Fast Mode Plus (FM+) Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	1	MHz
Hold time for start condition	T_1	0.26	–	μs
Setup time for stop condition	T_2	0.26	–	
Data setup time, external clock (MCLK) above 24 MHz	T_3	0.05	–	μs
Data setup time, external clock (MCLK) between 12.8 and 24 MHz		0.1	–	
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T_4	0	–	μs
High period of the SCL clock	T_5	0.26	–	
Low period of the SCL clock	T_6	0.5	–	
Bus free time between stop and start conditions	T_7	0.5	–	
Rise time for both SDA and SCL signals	–	–	120	ns
Fall time for both SDA and SCL signals	–	–	120	
Capacitive load for each bus line	CB	–	550	pF

Figure 21   CCI Write Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

Figure 22   CCI Read Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

Figure 23   CCI Read Multiple Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

You can configure up to two I2C slave addresses using I2C_ID pins.

Table 12   I2C ID Address (XCE Pad)

XCE	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0	0010_0001b/21h	0010_0000b/20h	Address 1
1	0101_1011b/5Bh	0101_1010b/5Ah	Address 2

5 Functional Features

5.1 Block Diagram

S5K33DXX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip Phase-Locked Loop (PLL) to generate all internal clocks from a single master input clock running between 12 MHz and 60 MHz. Dedicated PLL generates the output interface clocks for maximum flexibility in interface frequency and for avoiding EMI.

The block diagram of the sensor is illustrated in *Figure 24*.

Figure 24   Functional Block Diagram

As an indirect ToF sensor, S5K33DXX has a dedicated modulation PLL and a modulation signal transmitter to control the IR illuminator. The modulation clock is also used in the photo-gate driver to perform demodulation at the pixel array.

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain.

The sensor is interfaced using a set of control and status registers that can be used to control many aspects of the sensor behavior, including frame size and exposure setting. These registers can be accessed through a CCI or SPI interface.

5.2 Data Processing Chain

Figure 25 illustrates the whole data processing chain of S5K33DXX. The data processing chain performs row noise reduction, frame black level recovery, and compensation for various analog circuit variations and non-uniform pixel levels. The flexible compensations are configured per readout modes and exposure level, which are performed in the Front-End Image Signal Processor (FEISP).

The data processing chain includes a bad pixels correction option (both static and dynamic) that can perform bad pixels detection and correction on flat surfaces.

S5K33DXX has on-sensor H/W depth calculation chain that can be used in certain readout modes and can be used for low-accuracy depth applications.

In addition, S5K33DXX activates deterministic pattern generator and a MIPI CSI-2 frame formatter with embedded line support.

Figure 25   Data Processing Chain

5.3 Sensor output modes

The sensor supports four different output modes such as RAW phase output, depth output, proximity mode, and RAW phase + proximity.

5.3.1 RAW Phase Output

The main application of the sensor is to output RAW phase-sampled data for the back-end depth post processing. In this mode, the output format is similar to the ADC output format; if the sensor is configured to 4-tap phase output, the output mode is the same.

Figure 26   RAW Phase Output Data Path Configuration

In this mode, Bad Pixel Compensation (BPC) can be enabled or disabled. There are no specific constraints on the BPC.

5.3.2 Depth Output

Low-accuracy depth can be calculated and output. In this mode, BPC and dual-frequency must be disabled. Depth output format can be either depth only or depth + confidence (which requires three components of data per pixel such as depth, intensity, and amplitude).

Figure 27   Depth Mode Data Path Configuration

Input Image Type	Output Image Type	Limitations	Notes
Raw phase: 4-tap	Depth or Depth + confidence	BPC is disabled. Phase re-order is required. 1 cycle gap between readout of each pixel in TG. Dual-frequency mode is disabled.	Proximity information can be calculated and read through I2C/SPI or flagged by GPIO.

5.3.3 Proximity Mode (No Output)

In proximity mode, output is not required, so MIPI and its preceding blocks can be disabled. Proximity information is either flagged on a GPIO or read externally through IIC/SPI.

Figure 28   Proximity Mode Data Path Configuration

5.3.4 RAW Phase + Proximity

Proximity calculation can be combined with RAW phase output. In this mode, the AP software calculates the high quality depth and low quality depth is used internally for proximity.

Figure 29   RAW Phase + Proximity Data Path Configuration

5.4 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The addressable pixel array is assigned anywhere on the pixel array. x_addr_start, y_addr_start, x_addr_end, y_addr_end, x_output_size, and y_output_size registers control the addressed region of the pixel array.

Figure 30   Window of Interest on Pixel Array

5.5 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

The sensor module supports the following four possible pixel readout orders:

a) **Standard Readout**
    The addressed region of the horizontal pixel data output is controlled by the x_addr_start and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_start and y_output_depth registers.

b) **Horizontally Mirrored Readout**
    The addressed region of the horizontal pixel data output is controlled by the x_addr_end, and x_output_width registers, and the vertical pixel data output is the same as that of the standard readout.

c) **Vertical Flipped Readout**
    The horizontal pixel data output is same as that of the standard readout, and the addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

d) **Horizontally Mirrored and Vertically Flipped Readout**
    The addressed region of the horizontal pixel data output is controlled by the x_addr_end and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

Figure 31   Horizontal Mirror and Vertical Flip at Normal/Binning Output Mode

5.6 Averaged Readout (Binned Readout)

By programming the averaged readout enable register, the sensor is configured to read out pixel data that has been averaged with adjacent pixel of same phase.

5.7 Frame Rate Control

Varying the size of the virtual frame changes the line rate and the frame rate. line_length_pck and frame_length_lines registers control the width and depth of virtual frame, respectively. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck-x_output_size, vertical blanking time: frame_length_lines-y_output_size) should meet the system requirements. Use the following formula to calculate the frame rate.

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

Figure 32   Example of Virtual Frame Format

5.7.1 Integration Time Control (Electronic Shutter Control)

The shutter operation controls the pixel integration time. During the shutter operation, the column step integration time control register (fine_integration_time) and the line step integration time control register (coarse_integration_time) determine the amount of time, integration time. Use the following formula to calculate the total integration time of the sensor module.

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time} × pclk period[sec]

5.7.2 Functional Operation Modes

S5K33DXX supports various operation modes, which are functions of the following mode parameters:

- Interface bandwidth
- H/W limitations: Minimal H/V-blank, delay of the blocks
- Requested sensor output size and sensor operation mode

- CIS output size and number of bits per pixel: RAW12 and RAW10 (through clamping)

- Required vertical blank time

- Pixel array configuration: 4-tap or 2-tap

- Output format: Phase, depth, or depth + confidence

Typical operation modes and related typical settings are described in *Table 13*.

Table 13   Typical Functional Operation Modes

Resolution	Mode	Array Mode	Output Mode	H	V	Frame Rate (fps)
VGA	Full	4-tap	RAW phase	1280	960	60
VGA	Full	2-tap	RAW phase	1280	480	120
QVGA	2x2 binning	4-tap	RAW phase	640	480	90
QVGA	2x2 binning	2-tap	RAW phase	640	240	180
QQVGA	4x4 binning	4-tap	RAW phase	320	120	120
QQVGA	4x4 binning	2-tap	RAW phase	320	240	240
16×16[*]	16x16 crop	4-tap	Proximity (no output)	32	32	10
VGA	Full	4-tap	Depth	640	480	60
VGA	Full	4-tap	Depth + Confidence	1920[**]	480	60

(*): Image size for the proximity mode can be configured to any value less than 32×32 resolution.
(**): Depth + Confidence image contains three different attributes per pixel (depth, intensity, and amplitude), thus, image width is $640 \times 3 = 1920$.

5.8 PLL and Clock Generator

S5K33DXX clock system uses system PLL, system clock dividers, output PLL, output clock dividers, and a modulation PLL to generate all internal clocks from a single master input clock running between 12 MHz and 60 MHz.

The maximum effective VCO frequency of output PLL for MIPI transmission is 1.6 GHz. The dedicated system PLL is used for maximal flexibility in interface frequency and for EMI avoidance. The maximum system PLL VCO frequency is 720 MHz. The modulation PLL allows flexible demodulation of the input modulation signal and for supplying sync signal for the IR illuminator. Modulation frequency can be changed for each frame to support dual-frequency mode. Clock dividers are used to generate all system clocks from a single PLL source.

The charge pump clock and the ADC clock are used for A/D conversion circuits, pixel clock is used for pixel processing and sensor control. Bit clock and output clock are set according to the required output rate.

Figure 33   Block Diagram of Clock System

5.8.1 Clock Relationships

The host provides the external input clock (with values varying between 12 and 60 MHz) in addition to setting dividers and multipliers to get the required video timing and output pixel clocks.

Figure 34   Clock Relationships

Figure 35   PLL Frequency Synthesis

Use the following formula to calculate PLL_CLK.

$$System\ PLL\_CLK = MCLK \times \frac{M}{P} \times \frac{1}{2^s}$$

$$Output\ PLL\_CLK = MCLK \times \frac{2M}{P} \times \frac{1}{2^s}$$

NOTE: Post scaler (PLL_S) in S5K33DXX is not controllable. Post dividers are used for lower frequency synthesis.

Table 14   PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	–	64	MHz	EXTCLK frequency range
System PLL reference frequency range	6	–	12	MHz	Output of the system PLL pre-divider (Fref)
System PLL VCO frequency range	500	–	1000	MHz	Output of the system PLL multiplier VCO oscillation range (Fvco)
System PLL output frequency range	31.25	–	1000	MHz	Output of the system PLL post scaler. Minimum value is only for testing ($4 > S \geq 1$).
Output PLL reference frequency range	6	–	12	MHz	Output of the output PLL pre-divider (Fref)
Output PLL VCO frequency range	1075	–	1600	MHz	Output of the output PLL multiplier VCO oscillation range (Fvco). Effective frequency for MIPI transmission is same as that of VCO.
Output PLL output frequency range	80	–	1600	MHz	Output of the output PLL post scaler. Minimum value is only for test ($4 > S \geq 1$). Effective frequency for MIPI transmission is the same as that of VCO.

NOTE: For more information about the PLL and clock system control, refer to S5K33DXX Application Note.

5.8.2 Master Clock Waveform

Figure 36   Master Clock Waveform Diagram

MCLK is the input clock to the S5K33DXX sensor, which is sometimes referred to as EXTCLK (external clock).

Table 15   EXTCLK Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
MCLK clock frequency	MCLK	6	–	64	MHz	–
MCLK period	tp	13.89	–	83.33	ns	–
MCLK rise/fall time	tr/tf	–	–	10		–
MCLK period jitter (peak-to-peak)	Tjitter	–	–	400	ps	–

NOTE: For higher I2C/SPI rate such as fast-mode or fast-mode plus, the minimum MCLK frequency of 12 MHz is required.

5.9 IR Illuminator Control

S5K33DXX can drive an IR illuminator through a differential modulation signal generated by an on-chip modulation-signal transmitter. An IR illuminator can be implemented by a Laser Diode (LD) or an LED. One possible candidate of the LDs is a Vertical-Cavity Surface-Emitting Laser (VCSEL).

The modulation-signal transmitter can transmit the IR modulation signal in Low-Voltage Differential Signaling (LVDS) level or full-swing CMOS level for low-frequency driving in low-power. This modulation clock signal is valid during the integration time.

The modulation enable flag signal (active high) can also be generated to wrap the modulation signal for an LD driver IC to inform the modulation period. The modulation flag signal can start earlier than the actual modulation signal to wake up the LD driver IC before the integration time.

Figure 37   Connection Between the ToF Sensor and IR Illuminator

5.10 Dual Camera Synchronization

Dual sync. is an attribute that enables the sensor to accept the VSync-in from an external source. The purpose of this function is to enable the sensor to synchronize its image data transmission with other sensors. Higher level applications can analyze multiple images from multiple sensors.

Dual sync. operates correctly only if both sensors are configured to work with the same frame rate, and the sensor can properly fix and adjust only minor drifts caused from physical differences between the sensors.

Figure 38   Dual camera system

The dual sync feature monitors two intervals on the slave sensor (that is, the sensor which is in synchronization with the external source such as the master sensor), which defines the line time between the master and slave sensors:

- VSync-in to VSync-in – The time between two consecutive VSync-in received from the master.

- VSync-in to VSync-out – The time between VSync-in received from the master and the internal VSync-out generated by the slave.

Time Interval	Label	Min.	Max.	Units
Dual sync. frames delay	Tframe_dly	1	2	Frames
Vsync (I) to Vsync (O) exposure time < Frame time - 60 H-times	T0	5	-	H-Times
Vsync (I) to Vsync (O) exposure time >= Frame time - 60 H-times		60	-	

Dual sync frames delay in S5K33DXX is one to two frames as illustrated in *Figure 39*.

Figure 39   Initialization Sequence of Dual Camera Synchronization

5.11 NVM OTP Memory

The OTP memory module is a non-volatile One-Time Programmable (OTP) memory module. This module enables the saving of unique data to each chip at the production stage.

OTP memory is used to store the following information:

- Chip ID data – Production history data to be stored during die sorting
- Parameter for lens shading
- 9 Kb for users

Following are two different ways to access each OTP memory:

- Externally, using I/O pads by configuring the chip to a dedicated test mode and performing full OTP memory IP write/read protocol.
- Internally, through the internal-bus using the controller.

5.11.1 OTP Read/Write Procedure

For more information, refer to S5K33DXX Application Note.

5.12 Output Data Interface

S5K33DXX MIPI CSI-2 interface is a two-lane high-speed serial interface that connects the camera sensor to a host processor. Maximum bitrate of MIPI of S5K33DXX is 1.6 Gbps per lane.

S5K33DXX supports all mandatory requirements in MIPI CSI-2 version 1.00 and DPHY 1.2 specifications. For more information, refer to MIPI DPHY 1.2 specification.

Following are some supported features and specifications of output data interface:

- Main output frame rates:
    - 4-tap VGA RAW phase: 60 fps
    - 4-tap QVGA RAW phase: 90 fps
    - 4-tap QQVGA RAW phase: 120 fps
    - VGA depth: 60 fps
    - VGA depth + confidence: 60 fps
- MIPI CSI-2: Two lanes with a maximum of 1.6 Gbps (bit clock rate)
- Data types: RAW8, RAW10, and RAW12
- Data output types:
    - Video stream
    - Embedded lines (embedded frame header output)
- Integrated MIPI DPHY
- MIPI transmission only
- Up to two data lanes and one clock lane
- Swap in MIPI data lanes
- Only +/- swap (not support between lanes)
- Ultra Low Power Mode (ULPM)

Figure 40   CSI-2 and CCI Transmitter and Receiver Interface

Figure 41   Two-Lane Transmitter and Two-Lane Receiver Example

Figure 42   Low-Level Protocol Packet Overview

Figure 43   Long Packet Structure

Preliminary product information describes products that are in development, for which full characterization data and associated errata are not yet available. Specifications and information herein are subject to change without notice.

LSB뭘   LSB뭘

| Line Start: | Packet Header | **P1[11:4]** | P2[11:4] | P2 [3:0] | **P1 [3:0]** | *P3[11:4]* | P4[11:4] | P4 [3:0] | **P3 [3:0]** | **P5[11:4]** | ···· |

| Line End: | ···· | P636 [3:0] | **P635 [3:0]** | **P637[11:4]** | P638[11:4] | P638 [3:0] | **P637 [3:0]** | *P639[11:4]* | P640[11:4] | P640 [3:0] | *P639 [3:0]* | Packet Footer |

LSB뭘   LSB뭘   LSB뭘

Figure 44   RAW12 Transmission

FS	Packer Header, PH	P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**	Packer Footer, PF	
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		
		P1	P2	**LSBs**	P3	P4	**LSBs**	....	P638	**LSBs**	P639	P640	**LSBs**		FE

Figure 45   RAW12 Frame Format

5.12.1 RAW Phase Frame Packing – Slow Frame

As described in Section *1.3* *Sensor Readout Modes*, a depth frame can be built from more than one RAW phase frame.

In a 2-tap mode, at least two consecutive frames are required to produce a depth frame.

When dual-frequency for extending depth range is applied, each frequency should have its own set of phase frames.

To allow simpler frame buffering and packing in the AP side, S5K33DX can pack all required phase frame for one depth frame with single Frame Start (FS) and Frame End (FE) MIPI packets.

When RAW phase frame packing is disabled, each RAW phase frame has its own FS and FE transmitted as illustrated in *Figure 46*.

Figure 46   Depth Frame from Two RAW Phase Frames – Frame Packing Disabled

When RAW phase frame packing is enabled, FS is transmitted at default virtual channel only for the first frame and FE is transmitted at default virtual channel only for the last frame in a depth frames pack. The remaining FS and FE packets of the depth frames pack can still be transmitted, but to a dummy virtual channel, as illustrated by the grey notation in *Figure 47*.

Figure 47   Depth Frame from Two RAW Phase Frames – Frame Packing Enabled

5.13 Embedded Line

S5K33DXX can be configured to generate an embedded MIPI header with frame information.

5.14 Test Pattern

S5K33DXX can be configured to generate deterministic test patterns. For more information, refer to S5K33DXX Application Note.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Table 16   Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit
Digital absolute maximum	VDDD (max.)	–0.5	–	1.5	V
Analog absolute maximum	VDDA (max.)	–0.3	–	3.6	V
I/O absolute maximum	VDDIO (max.)	–0.3	–	3.6	V
PGD absolute maximum	VDDPG (max.)	–0.5	–	1.5	V
Digital input voltages, absolute max. [1]	VIP (max.)	–0.3	–	VDDIO + 0.3	V
VCAP analog voltages, absolute max. [2]	VCAP	-0.3	–	4.2	V
Storage temperature	TSTR	–40	–	85	°C

NOTE:

1.   Digital inputs: MCLK, RSTN, I2C_SPI_N_SEL, XCE, SDI, SCK, VSYNC_IN and GPIO_1/2/3

2.   Voltage on external capacitors for analog nodes

6.2 Operating Conditions

Table 17   Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Digital power supply [1]	VDDD	0.95	1.05	1.15	V
Analog power supply [2]	VDDA	2.7	2.8	2.9	V
I/O supply	VDDIO	1.7 (or 2.7)	1.8 (or 2.8)	1.9 (or 2.9)	V
PGD supply [3]	VDDPG	0.95	1.05	1.15	V
Digital input voltages [4]	VIP	0	–	VDDIO	V
VCAP analog voltage	VCAP	0	–	4.2	V
Test temperature (Ta) [5]	TTEST	21	23	25	°C
Optimum operating temperature (Tj) [6]	TOPT	0	–	60	°C
Normal operating temperature (Tj) [7]	TOPR	–20	–	60	°C
Functional operating temperature (Tj) [8]	TFUNC	–20	–	70	°C

NOTE:

1. Digital supply tolerances: 1.05 V $\pm$ 100 mV
2. Analog supply tolerances: 2.8 V $\pm$ 100 mV
3. Photo-Gate Driver (PGD) supply tolerance: 1.05 V $\pm$ 100 mV
4. Digital inputs: MCLK, RSTN, I2C_SPI_N_SEL, XCE, SDI, SCK, VSYNC_IN and GPIO_1/2/3
5. Test temperature (T_a): Image quality test conditions
6. Optimum operating temperature (Tj): No visible degradation in image quality
7. Normal operating temperature (Tj): Camera produces acceptable images
8. Functional operating temperature (Tj): Camera fully functional

6.3 DC Characteristics

Table 18   DC Characteristics

(VDDA = 2.7 V to 2.9 V, VIP = 1.8 V $\pm$ 0.1 V or 2.8 V $\pm$ 0.1 V, T_j = $-$ 30 to + 70°C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	$0.7 \times$ VIP	–	VIP + 0.3	V
	VIL	–	–0.3	–	$0.3 \times$ VIP	
Input leakage current	IIL	VIN = VIP or VSS	–10	–	10	μA
High-level output voltage	VOH	IOH = –100 μA	VDDIO – 0.2	–	–	V
Low-level output voltage	VOL	IOL = 100 μA	–	–	0.2	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	–10	–	10	μA
Input capacitance	CIN	–	–	–	5	pF
Supply current	IHWSBA [1]	Hardware standby mode, analog	–	TBD	TBD	μA
	IHWSBD [1]	Hardware standby mode, digital	–	TBD	TBD	
	ISTRMA [2]	Streaming mode, analog, 4-tap @ 60 fps	–	TBD	TBD	mA
	ISTRMD [2]	Streaming mode, digital, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMIO [2]	Streaming mode, I/O, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMP [2]	Streaming mode, PGD, 4-tap @ 60 fps	–	TBD	TBD	

NOTE:

1. Digital IHWSBD - Digital and analog power off is required.

2. Conditions: VDDA = 2.8 V, VDDD = 1.05 V, VDDIO = 1.8 V, VDDPG = 1.05 V and T_j = 60°C

6.4 AC Characteristics

Table 19　　AC Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency [1]	fXCLK	–	6	–	64	MHz
External clock duty cycle [1]	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	--	–	500	µs

NOTE: Applied to the MCLK pin

1.　A fast-mode I2C-bus can be used with the external clock that exceeds 12 MHz.

7 Optical Specification

7.1 Target Chief Ray Angle (CRA)

Figure 48 illustrates the target CRA of the module lens.

Figure 48   Target CRA

Table 20   CRA with Image Height (Field)

Field	Image Height (mm)	CRA (Deg.)
0.0	0.000	0.0
0.1	0.282	6.2
0.2	0.564	12.4
0.3	0.846	18.2
0.4	1.128	23.2
0.5	1.410	26.7
0.6	1.692	28.7
0.7	1.974	29.6
0.8	2.256	30.0
0.9	2.538	29.4
1.0	2.820	25.8

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7.2 Spectral Response

Figure 49 illustrates the spectral response of S5K33DXX.

Figure 49   Spectral Response

Table 21   Spectral Response

Wavelength (nm)	Magnitude (%)	Wavelength (nm)	Magnitude (%)	Wavelength (nm)	Magnitude (%)
400	89.3	610	93.6	820	69.7
410	90.9	620	93.1	830	68
420	92	630	91.8	840	66.4
430	92.8	640	90.8	850	64.8
440	93.5	650	90.5	860	62.6
450	94.5	660	89.5	870	60
460	95	670	87.9	880	56.9
470	96.8	680	87.1	890	53.6
480	97.7	690	86.3	900	50.9
490	100	700	85.3	910	48.5
500	98.4	710	84	920	46
510	98.4	720	82.8	930	43.1
520	98.8	730	81.8	940	40.1
530	99.4	740	80.5	950	37.3
540	100	750	79.2	960	34.1
550	99.4	760	77.6	970	31
560	98.8	770	75.2	980	27.9

Wavelength (nm)	Magnitude (%)	Wavelength (nm)	Magnitude (%)	Wavelength (nm)	Magnitude (%)
570	97.4	780	74.5	990	25
580	96.4	790	73.5	1000	22.3
590	95.6	800	72.3	-	-
600	94.2	810	70.3	-	-

7.3 IR Band-Pass Filter

Figure 50 illustrates IR response of the Band-Pass Filter (BPF) on the module. The performance of IR BPF is critical for depth quality under the ambient light condition (outdoor use). *Table 22* describes the recommended characteristics of the IR BPF

Figure 50   IR Response of the Band-Pass Filter

Table 22   Recommended Characteristics of IR BPF

Items	Min.	Typ.	Max.	Unit
Center wavelength	945	–	–	nm
Bandwidth (@ 50% transmission, FWHM)	–	–	40	nm
Center wavelength shift (@ 30° incident angle)	–	–	11	nm

8 Register Description

This chapter describes the register map for S5K33DXX.

Table 23   Register Type

Type	Description
RO	Read only
RW	Read/Write Written value affects on the next frame.
RW/R	Read/Write Written value affects only when exit from standby.
RW/C	Read/Write Changing the value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write Changing the value (may) causes entering stand-by/software reset.

Table 24   Configuration Register

Register Name	Address	Access Type	Default Value	Description
api_rd_general_model_id	0x40000000	RO	0x303d	Camera module model identification number
api_rd_general_revision_number_major	0x40000002	RO	0xa0	Revision identifier of camera module for tuning/settings change
api_rd_general_manufacturer_id	0x40000003	RO	0x0	Module manufacturers code
api_rd_general_api_version	0x40000004	RO	0x50	API version
api_rd_general_frame_count	0x40000005	RO	0x0	0x00 = Wakeup (before first frame) 0xFF = S/W stand-by 1 - 254 = Frame counter value
api_rd_general_config_count	0x40000007	RO	0x0	Configuration change counter (frames aborted or corrupted frames)
api_rd_general_data_pedestal	0x40000008	RO	0x100	Data pedestal - typically code 64 for 10-bit systems
api_rd_general_temperature	0x4000000A	RO	0x0	Temperature in degrees (Celsius) Signed number with 8 fraction bits
api_rd_general_pixel_depth	0x4000000C	RO	0xC	8-bit, 10-bit, or 12-bit pixel data

Register Name	Address	Access Type	Default Value	Description
api_rd_general_cra	0x4000000E	RO	0x0	Chief Ray Angle (CRA)
api_rd_general_sample_type	0x4000000F	RO	0x1	0x01 = Typical sample 0x00 = Random and/or corner samples
api_rd_general_revision_number_minor	0x40000010	RO	0x0	Device revision identifier of the camera module for minor changes
api_rd_general_module_date_year	0x40000012	RO	0x0	Bits[3:0] = Last digit of manufacturing year
api_rd_general_module_date_month	0x40000013	RO	0x0	Bits[3:0] = Manufacturing month
api_rd_general_module_date_day	0x40000014	RO	0x0	Bits[3:0] = Manufacturing day
api_rd_general_module_date_phase	0x40000015	RO	0x1	Bits[2:0] = Manufacturing phase
api_rd_general_sensor_model_id	0x40000016	RO	0x0	Silicon identification number
api_rd_general_sensor_revision_number	0x40000018	RO	0x0	Device revision identifier of sensor silicon
api_rd_general_sensor_manufacturer_id	0x40000019	RO	0x0	Manufacturers code For more information, refer to GIIC Manufacturer Codes Document.
api_rd_general_sensor_firmware_version	0x4000001A	RO	0x0	Sensor firmware version
api_rd_general_serial_number	0x4000001C	RO	0x0	Running serial number
api_rd_general_sensor_setfile_version	0x4000001E	RO	0x0	Running setfile version number
api_rd_frame_format_model_type	0x40000040	RO	0x4	1 = 2 bytes data format
api_rd_frame_format_model_subtype	0x40000041	RO	0x11	Bits[7:4] = Number of horizontal descriptors Bits[3:0] = Number of vertical descriptors
api_rd_frame_format_descriptor_0	0x40000042	RO	0x5508	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_1	0x40000044	RO	0x53c8	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_2	0x40000046	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_3	0x40000048	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_4	0x4000004A	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_5	0x4000004C	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_6	0x4000004E	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_7	0x40000050	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size

Register Name	Address	Access Type	Default Value	Description
api_rd_frame_format_descriptor_8	0x40000052	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_9	0x40000054	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_10	0x40000056	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_11	0x40000058	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_12	0x4000005A	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_13	0x4000005C	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_frame_format_descriptor_14	0x4000005E	RO	0x0	[15:12] = Descriptor type [11:0] = Descriptor size
api_rd_data_format_model_type	0x400000C0	RO	0x1	Data format (0x01 = Two byte data format)
api_rd_data_format_model_subtype	0x400000C1	RO	0x4	Contains the used number of data format descriptors
api_rd_data_format_descriptor_0	0x400000C2	RO	0xa0a	Top 10-bit of internal pixel data Transmitted as RAW10.
api_rd_data_format_descriptor_1	0x400000C4	RO	0xa08	Top 10-bit of internal pixel data compressed to 8-bits Transmitted as RAW8.
api_rd_data_format_descriptor_2	0x400000C6	RO	0x808	Top 8-bit of internal pixel data Transmitted as RAW8.
api_rd_current_state_tg_clk_khz	0x400000D0	RW	0x0	Logical TGCLK (on ASIC, it is always same as system clock)
api_rd_current_state_pixel_clk_khz	0x400000D4	RW	0x0	The ISP clock x the number of pixels processed in each clock
api_rd_current_state_mipi_clk_khz	0x400000D8	RW	0x0	The MIPI clock
api_rd_current_state_vendor_error_type	0x400000DC	RW	0x0	System level error caused by wrong user configuration 0 = No error 1 = External clock is not defined 2 = External clock is defined, but out of range 10 = Main PLL pre_pll_clk_div is out of range 11 = Main PLL pll_ip_freq is out of range 12 = Main PLL pll_multiplier is out of range 13 = Main PLL l pll_s divider is out of

Register Name	Address	Access Type	Default Value	Description
				range 14 = Main PLL VCO frequency is out of range 15 = Main PLL FOUT frequency is out of range 20 = MIPI PLL pre_pll_clk_div is out of range 21 = MIPI PLL pll_ip_freq is out of range 22 = MIPI PLL pll_multiplier is out of range 23 = MIPI PLL pll_s divider is out of range 24 = MIPI PLL VCO frequency is out of range 25 = MIPI PLL FOUT frequency is out of range 30 = vt_sys_div is out of range 31 = vt_pix_div is out of range 32 = vt_sys_freq is out of range 33 = vt_pix_freq is out of range 34 = op_sys_div is out of range 35 = op_pix_div is out of range 36 = op_sys_freq is out of range 37 = op_pix_freq is out of range 38 = Ddr divider is out of range VENDOR_ERR_DHPY_FREQ_OUT_OF_RANGE - DPHY frequency divider is out of range 101 = Two or more functions are assigned to same GPIO 100 = Read from invalid OTP address VENDOR_ERR_NOT_SUPPORTED_COLUMNS_SUBSAMPLING - Configured columns sub-sampling is not supported
api_rd_current_state_time_of_flight_output_format	0x400000F0	RO	0x0	ToF only = Mode number
api_rd_current_state_time_of_flight_phase_map	0x400000F1	RO	0x0	ToF only = Phase map index of current frame
api_rd_current_state_time_of_flight_frequency_modulation_index	0x400000F2	RO	0x0	ToF only = Modulation frequency index of current frame
api_rd_current_state_time_of_flight_proximity_detected	0x400000F3	RO	0x0	ToF only = Depth proximity is detected in previous frame
api_rd_current_state_led_driver_ic_temperature	0x400000F4	RO	0x0	ToF only = LED driver IC temperature
api_rd_current_state_xemout_alarm_fr	0x400000F6	RO	0x0	ToF only = LED driver XEMOUT alarm

Register Name	Address	Access Type	Default Value	Description
om_led_driver				indication
api_rw_general_setup_mode_select	0x40000100	RW/S	0x0	0 = Software standby 1 = Streaming
api_rw_general_setup_image_orientation	0x40000101	RW/C	0x0	Image orientation: Horizontal mirror and vertical flip 0 = No horizontal mirror and no vertical flip 1 = Horizontal mirror and no vertical flip 2 = No horizontal mirror and vertical flip 3 = Horizontal mirror and vertical flip
api_rw_general_setup_software_reset	0x40000103	RW/R	0x0	1 = Software reset
api_rw_general_setup_grouped_parameter_hold	0x40000104	RW/C	0x0	The grouped parameter hold register disables the consumption of integration, gain, and video timing parameters 0 = Consume as normal 1 = Hold
api_rw_general_setup_mask_corrupted_frames	0x40000105	RW	0x1	On preserve timing mode 0 = Output the corrupted frame 1 = Do not output the corrupted frame
api_rw_general_setup_fast_standby_ctrl	0x40000106	RW	0x0	0 = Frame completes before mode entry 1 = Frame can be truncated before mode entry
api_rw_general_setup_cci_address_control	0x40000107	RW	0x20	Control CCI address Expressed as 8 bits (for example, 0x20 write and 0x21 read are entered as 0x20).
api_rw_general_setup_immediate_exposure_enable	0x4000010F	RW	0x0	Start exposure of next frame immediately (if exposure has not started yet) 0 = Disable immediate update for integration time 1 = Enable immediate update for integration time
api_rw_output_channel_identifier	0x40000110	RW	0x10	Virtual channel number [1:0] = VC of isp1 - Main video channel [5:4] = VC of isp2 - PDAF or Y data
api_rw_output_signalling_mode	0x40000111	RW	0x2	0 = PVI 2 = CSI-2 with DPHY (MIPI)
api_rw_output_data_format	0x40000112	RW/C	0xc0c	Data format [15:8] = Max. sensors ADC resolution [7:0] = Output data format 0x08 = Top 8 bits of pixel data (RAW8) 0x0A = Top 10 bits of pixel data (RAW10)

Register Name	Address	Access Type	Default Value	Description
api_rw_output_lane_mode	0x40000114	RW	0x0	Number of CSI-2 lanes to be used 0 = One lane 1 = Two lanes
api_rw_output_embedded_as_active_enable	0x40000117	RW	0x0	For debug footer Use this to allow the embedded to be output as (active) video lines.
api_rw_output_emb_use_header	0x40000118	RW	0x0	Enable/Disable the embedded line header 0 = Disable 1 = Enable
api_rw_output_emb_header_lines	0x40000119	RW	0x2	Defines the number of embedded lines (1 - 4)
api_rw_output_emb_footer_lines	0x4000011A	RW	0x0	Enable/Disable the embedded line footer 0 = Disable 1 = Enable
api_rw_output_emb_equal_to_data	0x4000011B	RW	0x1	Maintain embedded line same length as pixels line 0 = Embedded line length is shorter than data line length 1 = Embedded line length is equal to data line length Note: This is only the line length, not the actual byte that used for data (fixed to 256 pixels each line).
api_rw_output_emb_in_bytes	0x4000011C	RW	0x1	Maintain embedded line pixel bitage same as pixels data bitage 1 = Each embedded line pixel is byte 0 = Each embedded line pixel is equal to data pixel
api_rw_output_qual_mode_continues_enable	0x4000011E	RW	0x1	0 = Use legacy mode of continuous clock (PVI clock is always on)
api_rw_output_standby_power_mode	0x4000011F	RW	0x0	MIPI DPHY stand-by power mode 0 = ULPM 1 = LP11 (lane lines stay high) 2 = Disabled (lane lines are disconnected)
api_rw_flicker_detect_fd_mode	0x40000120	RW	0x0	Enable/Disable flicker detection 1 = Enable 0 = Disable
api_rw_op_cond_extclk_frequency_mhz	0x40000136	RW/S	0x0	Nominal external clock frequency (8.8 fixed point number)
api_rw_op_cond_extclk_scale_up	0x4000013D	RW	0x0	Allows using input clock higher than 255.99 MHz. For example, input clock 260 MHz is set as 0x8200 on

Register Name	Address	Access Type	Default Value	Description
				op_cond_extclk_frequency_mhz and as 0x01 on this vendor register (130 MHz << 1 = 260 MHz). For example, input clock 260 MHz is set as 0x8200 (130 MHz) on api register api_rw_op_cond_extclk_frequency_mhz and as 0x01 on this vendor register (130 MHz << 1 = 260 MHz).
api_rw_op_cond_extclk_frequency_additional_fraction_khz	0x4000013E	RW/S	0x0	Additional fraction of external frequency given in kHz External frequency is (extclk_frequency_mhz * 1000/256) << extclk_scale_up + extclk_frequency_additional_fraction_khz
api_rw_integration_time_fine_integration_time	0x40000200	RW	0x100	Fine integration time (of short exposure in WDR mode) in pixel clocks
api_rw_integration_time_coarse_integration_time	0x40000202	RW	0x100	Coarse integration time in h-times (of short exposure in WDR mode)
api_rw_clocks_modulation_pre_pll_clk_div	0x400002F0	RW/S	0x3	Pre-PLL clock divider value for the first frequency of the modulation PLL
api_rw_clocks_modulation_pll_multiplier	0x400002F2	RW/S	0x64	Multiplier value for the first frequency of the modulation PLL
api_rw_clocks_modulation_pll_post_scalar	0x400002F4	RW/C	0x0	2^S divider for the first frequency of the modulation PLL
api_rw_clocks_modulation_pix_clk_div	0x400002F6	RW/S	0x2	Modulation first pixel clock divider
api_rw_clocks_modulation_2nd_freq_pre_pll_clk_div	0x400002F8	RW/S	0x3	Pre-PLL clock divider value for the second frequency of the modulation PLL
api_rw_clocks_modulation_2nd_freq_pll_multiplier	0x400002FA	RW/S	0x50	Multiplier value for the second frequency of the modulation PLL
api_rw_clocks_modulation_2nd_freq_pll_post_scalar	0x400002FC	RW/C	0x0	2^S divider for the second frequency of the modulation PLL
api_rw_clocks_modulation_2nd_freq_pix_clk_div	0x400002FE	RW/S	0x2	Modulation second pixel clock divider
api_rw_clocks_vt_pix_clk_div	0x40000300	RW/S	0xa	Video timing pixel clock divider
api_rw_clocks_vt_pre_pll_clk_div	0x40000304	RW/S	0x4	Pre-PLL clock divider value
api_rw_clocks_vt_pll_multiplier	0x40000306	RW/S	0x78	PLL multiplier value
api_rw_clocks_vt_pll_post_scalar	0x4000030C	RW/C	0x0	2^S divider PLL frequency = Fvco/2^s
api_rw_clocks_op_pre_pll_clk_div	0x4000030E	RW/S	0x3	MIPI PLL pre PLL clock divider value
api_rw_clocks_op_pll_multiplier	0x40000310	RW/S	0x64	MIPI PLL multiplier value
api_rw_clocks_op_pll_post_scalar	0x40000312	RW/C	0x0	MIPI PLL 2^S divider

Register Name	Address	Access Type	Default Value	Description
api_rw_mipi_freq_hopping_enable	0x40000328	RW	0x0	Enable the support for MIPI PLL Frequency Hopping (FH)
api_rw_mipi_freq_hopping_pll_m_shift_on	0x40000329	RW	0x0	Request for MIPI PLL FH 0 = Use default MIPI PLL multiplier value 1 = Use shifted MIPI PLL multiplier value
api_rw_frame_timing_dynamic_frame_rate_enable	0x40000335	RW	0x0	Enable dynamic frame rate Frame rate changes according to integration time, but not smaller than frame_length_lines.
api_rw_frame_timing_frame_length_lines	0x40000340	RW	0x40c	Frame length in timing lines It can be increased by long_exposure registers.
api_rw_frame_timing_line_length_pck	0x40000342	RW/C	0x0	Line length (H-time) in pixel clocks (VT clock domain) It can be increased by long_exposure registers. 0 = FW select shortest time possible
api_rw_image_size_x_addr_start	0x40000344	RW/C	0x0	X-address of the top left corner of the visible pixel data (offset from full image size)
api_rw_image_size_y_addr_start	0x40000346	RW/C	0x0	Y-address of the top left corner of the visible pixel data (offset from full image size)
api_rw_image_size_x_addr_end	0x40000348	RW/C	0x507	X-address of the bottom right corner of the visible pixel data (offset from full image size)
api_rw_image_size_y_addr_end	0x4000034A	RW/C	0x3c7	Y-address of the bottom right corner of the visible pixel data (offset from full image size)
api_rw_image_size_x_output_size	0x4000034C	RW	0x508	Width of image data output from the sensor module
api_rw_image_size_y_output_size	0x4000034E	RW	0x3c8	Height of image data output from the sensor module
api_rw_image_size_digital_crop_x_offset	0x40000350	RW	0x0	Allow to cut off left side of output image (crop and pad)
api_rw_image_size_digital_crop_y_offset	0x40000352	RW	0x0	Allow to cut off top side of output image (crop and pad)
api_rw_sub_sample_x_even_inc	0x40000380	RW/C	0x1	Visible columns readout sub-sampling - even increment
api_rw_sub_sample_x_odd_inc	0x40000382	RW/C	0x1	Visible columns readout sub-sampling - odd increment
api_rw_sub_sample_y_even_inc	0x40000384	RW/C	0x1	Visible rows readout sub-sampling - even increment

Register Name	Address	Access Type	Default Value	Description
api_rw_sub_sample_y_odd_inc	0x40000386	RW/C	0x1	Visible rows readout sub-sampling - odd increment
api_rw_scaling_digital_scaling	0x40000402	RW/C	0x1010	Down scale factor: Range: 1 to 16 (should be determined upwards only) [7:0] - Row (vertical) scaling factor, four fraction bits [15:8] - Column (horizontal) scaling factor, four fraction bits. The factors of 1.5; 2; 3; 4 (for example, 24; 32; 48; and 64)
api_rw_scaling_hbin_digital_binning_factor	0x40000404	RW/C	0x10	Enable using digital horizontal binning NOTE: This digital binning is added onto the analog binning. 0x00 = Do not use HBIN in digital 0x10 = Do not use HBIN in digital 0x20 = Use FE-ISP horizontal binning 2 and so on up to 0x80.
api_rw_scaling_phase_reorder_enable	0x40000405	RW/C	0x0	Enable phase reorder
api_rw_scaling_bilinear_upscaling_enable	0x40000406	RW/C	0x0	Enable bilinear upscaling
api_rw_test_pattern_test_pattern_mode	0x40000600	RW	0x0	Controls the output of the test pattern module 0 = No pattern (default) 1 = Solid color 2 = 100% color bars 3 = Fade to grey color bars 4 = PN9
api_rw_test_pattern_fedtp_gradient_tof_pattern_en	0x4000061E	RW	0x0	Enable ToF raw phases gradient mode
api_rw_long_frame_timing_frame_length_lines_sh	0x40000702	RW/C	0x0	Left shifter for frame length in lines (Max. value is 11).
api_rw_long_frame_timing_line_length_pck_sh	0x40000703	RW/C	0x0	Shift-up value for line length pck
api_rw_long_frame_timing_coarse_integration_time_sh	0x40000704	RW/C	0x0	Left shifter for coarse integration time (Max. value is 11) Max. exposure should not be more than MAX_EXPOSURE_IN_SEC seconds.
api_rw_long_frame_timing_n_frames_as_one_slow	0x4000070D	RW	0x0	Number of frames to be considered as one slow 0 = Disable mode Non-zero = Number of frames
api_rw_long_frame_timing_total_slow_frame_timing_lines	0x4000070E	RW	0x0	Number of total frame timing lines for the one slow fps
api_rw_phy_dphy_requested_link_rate	0x40000800	RW	0x0	Target bitrate for CSI-2 transmission with

Register Name	Address	Access Type	Default Value	Description
				D-PHY This is bitrate (Mbps) in 16 fraction bits.
api_rw_phy_dphy_ctrl	0x40000804	RW	0x0	0 = Use automatic control 1 = Use UI control 2 = Use register control
api_rw_phy_dphy_skew_calibration_min_freq_mhz	0x40000806	RW	0x5dc	Minimal frequency for invocation of skew synchronization (added by Samsung)
api_rw_phy_dphy_skew_periodic_calibration_control	0x40000808	RW	0x0	0 = Do not send calibration sequence 2 = Send calibration sequence during frame blanking
api_rw_phy_dphy_skew_periodic_calibration_interval	0x40000809	RW	0x0	Output frame interval of period skew calibration 0 = No output 1 = Output with all frames. Otherwise, output once by X frames. (For example, number 2 means every second frame.)
api_rw_phy_dphy_skew_init_calibration_control	0x4000080A	RW	0x0	0 = Do not send calibration sequence 1 = Send calibration sequence during start of streaming
api_rw_phy_dphy_timing_tclk_post	0x4000080E	RW	0x0	Time that the transmitter should continue sending HS clock after the last associated data lane has transitioned to LP mode
api_rw_phy_dphy_timing_ths_prepare	0x4000080F	RW	0x0	THS-PREPARE is the time to drive LP-00 before starting the HS transmission on a data lane
api_rw_phy_dphy_timing_ths_zero_min	0x40000810	RW	0x0	HS-ZERO, MIN is the time to send HS-0, which turns on the line termination and drives the interconnect with the HS driver prior to sending the SoT sync sequence.
api_rw_phy_dphy_timing_ths_trail	0x40000811	RW	0x0	THS-TRAIL is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.
api_rw_phy_dphy_timing_tclk_trail_min	0x40000812	RW	0x0	Time to drive HS differential state after last payload clock bit of a HS transmission burst
api_rw_phy_dphy_timing_tclk_prepare	0x40000813	RW	0x0	Time to drive LP-00 to prepare for HS clock transmission
api_rw_phy_dphy_timing_tclk_zero	0x40000814	RW	0x0	Time for lead HS-0 drive period before starting clock
api_rw_phy_dphy_timing_tlpx	0x40000815	RW	0x0	Length of any low-power state period

Register Name	Address	Access Type	Default Value	Description
api_rw_phy_dphy_timing_ths_exit	0x40000816	RW	0x0	ths_exit timing
api_rw_binning_mode	0x40000900	RW/C	0x1	0 = Disabled analog binning 1 = Enabled analog binning 2 = Enabled analog summation, only in 2PD projects
api_rw_binning_type	0x40000901	RW/C	0x11	[3:0] = Row (vertical) binning factor [7:4] = Column (horizontal) binning factor
api_rw_binning_weighting	0x40000902	RW/C	0x0	0 = Averaged weighting 1 = Summed weighting 2 = Bayer weighting 3 = Module-specific weighting
api_rw_data_transfer_ctrl	0x40000A00	RW	0x0	[0]: 1 = Enable, 0 = Disable [1]: 1 = Write enable, 0 = Read enable [2]: 1 = Pending errors, read errors register. (For more information, refer to Protocol Documentation.)
api_rw_data_transfer_errors	0x40000A01	RW	0x0	Error flags [0] = Data corrupted error (failed to read from OTP) [1] = Error bit is not cleared before operation [2] = Trying to write to bit that is already set in OTP [3] = Request set (ctrl bit 0 set) during processing request [4] = Wrong page number
api_rw_data_transfer_page_select	0x40000A02	RW	0x0	Each page is 64 bytes. Do not exceed OTP size.
api_rw_data_transfer_data	0x40000A04	RW	0x0	64 x 8-bit register for read or write accesses
api_rw_isp_mapped_couplet_correct_enable	0x40000B06	RW	0x0	0 = Disabled static bad pixels correction 1 = Enabled static bad pixels correction
api_rw_dual_sensor_sync_ratio_mode	0x40000B31	RW	0x0	This field enables using a ratio between master and slave 0 - 1 = One clock ratio between master and slave 1 - 1 = N clock ratio between master and slave (faster master) 2 - N = One clock ratio between master and slave (faster slave)
api_rw_dual_sensor_sync_master_to_slave_ratio	0x40000B32	RW	0x2	The ratio between master and slave
api_rw_dual_sensor_sync_vsync_in_to_vsync_out_time	0x40000B34	RW	0x1	The time which should pass between the VSync-in and VSync-out signals. It is used for calculation of drift and

Register Name	Address	Access Type	Default Value	Description
				configured in timing lines.
api_rw_rta_motion_detected	0x40000B7E	RW	0x0	0 = Use normal settings. 1 = Use motion detected settings and calibration
api_rw_rta_face_detected	0x40000B7F	RW	0x0	1 = Use face detected settings and calibration 0 = Use normal settings
api_rw_sensor_out_pedestal	0x40000BC0	RW	0x100	Output pedestal
api_rw_sensor_offset_x	0x40000BC2	RW/C	0x0	Offset from X-address of the top left corner of the visible pixel data after analog crop, bin, and subsample (resizer)
api_rw_sensor_offset_y	0x40000BC4	RW/C	0x0	Offset from Y-address of the top left corner of the visible pixel data after analog crop, bin, and subsample (resizer)
api_rw_sensor_b_abort_timing_on_ch_cfg	0x40000BCA	RW	0x1	0 = Preserve timing (maintain frame rate) 1 = Abort timing if next frame is corrupted (on configuration change)
api_rw_sensor_abort_timing_method_on_rolling_sh	0x40000BCB	RW	0x1	This register describes when to abort when using rolling shutter 0 = Abort timing immediately even during read out 1 = Abort timing after read out ends 2 = Abort timing at the end of frame
api_rw_sensor_abort_timing_on_sw_stby	0x40000BCC	RW	0x1	This register describes when to abort when entering software standby 0 = Abort timing immediately even during read out 1 = Abort timing after read out ends 2 = Abort timing on end of frame
api_rw_sensor_time_of_flight_mode	0x40000BCD	RW/C	0x0	0 = Phases out 1 = Depth out 2 = Proximity only, no output 3 = Proximity and raw phases out 4 = Proximity and reformat phases out 5 = Proximity and depth out
api_rw_sensor_time_of_flight_depth_data_out_mode	0x40000BCF		0x7	[0:0] = Depth [1:1] = Intensity [2:2] = Amplitude
api_ro_pll_clock_limits_clock_tree_pll_capability	0x400010F0	RO	0x3	[0]: 0 = 2-PLL clock tree is not supported 1 = 2-PLL clock tree is supported [1]: 0 = 1-PLL clock tree is not supported 1 = 1-PLL clock tree is supported

Register Name	Address	Access Type	Default Value	Description
api_ro_pll_clock_limits_min_ext_clk_freq_mhz	0x400010F4	RO	0x40c0 0000	Minimum external clock frequency (IEEE754 format)
api_ro_pll_clock_limits_max_ext_clk_freq_mhz	0x400010F8	RO	0x4280 0000	Maximum external clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pre_pll_clk_div	0x400010FC	RO	0x1	Minimum pre PLL divider value
api_ro_pll_clock_limits_main_max_vt_pre_pll_clk_div	0x400010FE	RO	0x3f	Maximum pre PLL divider value
api_ro_pll_clock_limits_main_min_vt_pll_ip_freq_mhz	0x40001100	RO	0x40c0 0000	Minimum PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_ip_freq_mhz	0x40001104	RO	0x4140 0000	Maximum PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pll_multiplier	0x40001108	RO	0x10	Minimum PLL multiplier
api_ro_pll_clock_limits_main_max_vt_pll_multiplier	0x4000110A	RO	0x1ff	Maximum PLL multiplier
api_ro_pll_clock_limits_main_min_vt_pll_vco_freq_mhz	0x4000110C	RO	0x43fa 0000	Minimum VT PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_vco_freq_mhz	0x40001110	RO	0x447a 0000	Maximum VT PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pll_post_scalar	0x40001114	RO	0x5	Maximum post scaler S (2^S divider) value
api_ro_pll_clock_limits_main_min_op_pll_freq_mhz	0x40001118	RO	0x4200 0000	Minimum PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_op_pll_freq_mhz	0x4000111C	RO	0x447a 0000	Maximum PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_sys_clk_div	0x40001120	RO	0x1	Minimum video timing system clock divider value
api_ro_pll_clock_limits_main_max_vt_sys_clk_div	0x40001122	RO	0xc	Maximum video timing system clock divider value
api_ro_pll_clock_limits_main_min_vt_sys_clk_freq_mhz	0x40001124	RO	0x4200 0000	Minimum video timing system clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_sys_clk_freq_mhz	0x40001128	RO	0x447a 0000	Maximum video timing system clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_min_vt_pix_clk_div	0x4000112C	RO	0x1	Minimum video timing pixel clock divider value
api_ro_pll_clock_limits_main_max_vt_pix_clk_div	0x4000112E	RO	0xc	Maximum video timing pixel clock divider value
api_ro_pll_clock_limits_main_min_vt_pix_clk_freq_mhz	0x40001130	RO	0x4240 0000	Minimum video timing pixel clock frequency (IEEE754 format)
api_ro_pll_clock_limits_main_max_vt_pix_clk_freq_mhz	0x40001134	RO	0x4390 0000	Maximum video timing pixel clock frequency (IEEE754 format)

Register Name	Address	Access Type	Default Value	Description
api_ro_pll_clock_limits_output_min_op_pre_pll_clk_div	0x40001138	RO	0x1	Minimum pre OP PLL clock divider value
api_ro_pll_clock_limits_output_max_op_pre_pll_clk_div	0x4000113A	RO	0x3f	Maximum pre OP PLL clock divider value
api_ro_pll_clock_limits_output_min_op_pll_ip_freq_mhz	0x4000113C	RO	0x40c0 0000	Minimum OP PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_ip_freq_mhz	0x40001140	RO	0x4140 0000	Maximum OP PLL input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_min_op_pll_multiplier	0x40001144	RO	0x2c	Minimum OP PLL multiplier
api_ro_pll_clock_limits_output_max_op_pll_multiplier	0x40001146	RO	0xb4	Maximum OP PLL multiplier
api_ro_pll_clock_limits_output_min_op_pll_vco_freq_mhz	0x40001148	RO	0x4486 6000	Minimum OP PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_vco_freq_mhz	0x4000114C	RO	0x44c8 0000	Maximum OP PLL VCO frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_post_scalar	0x40001150	RO	0x5	Maximum post scaler S (2^S divider) value
api_ro_pll_clock_limits_output_min_op_pll_op_freq_mhz	0x40001154	RO	0x42a0 0000	Minimum OP PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_op_pll_op_freq_mhz	0x40001158	RO	0x44c8 0000	Maximum OP PLL output clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_min_op_sys_clk_div	0x4000115C	RO	0x1	Minimum output system clock divider value
api_ro_pll_clock_limits_output_max_op_sys_clk_div	0x4000115E	RO	0xc	Maximum output system clock divider value
api_ro_pll_clock_limits_output_min_op_sys_clk_freq_mhz	0x40001160	RO	0x42a0 0000	Minimum output system clock frequency
api_ro_pll_clock_limits_output_max_op_sys_clk_freq_mhz	0x40001164	RO	0x44c8 0000	Maximum output system clock frequency
api_ro_pll_clock_limits_output_min_op_pix_clk_div	0x40001168	RO	0x1	Minimum output pixel clock divider value
api_ro_pll_clock_limits_output_max_op_pix_clk_div	0x4000116A	RO	0xc	Maximum output pixel clock divider value
api_ro_pll_clock_limits_output_min_op_pix_clk_freq_mhz	0x4000116C	RO	0x4100 0000	Minimum output pixel clock frequency
api_ro_pll_clock_limits_output_max_op_pix_clk_freq_mhz	0x40001170	RO	0x4348 0000	Maximum output pixel clock frequency
api_ro_pll_clock_limits_output_min_dphy_freq_mhz	0x40001174	RO	0x42a0 0000	Minimum DPHY input clock frequency (IEEE754 format)
api_ro_pll_clock_limits_output_max_dphy_freq_mhz	0x40001178	RO	0x44c8 0000	Maximum DPHY input clock frequency (IEEE754 format)

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8 Register Description

Register Name	Address	Access Type	Default Value	Description
api_ro_frame_timing_min_frame_length_lines	0x400011A0	RO	0x64	Minimum number of lines per frame
api_ro_frame_timing_max_frame_length_lines	0x400011A2	RO	0xffff	Maximum possible number of lines per frame
api_ro_frame_timing_min_line_length_pck	0x400011A4	RO	0x0	Minimum line length allowed 0 = Auto select
api_ro_frame_timing_max_line_length_pck	0x400011A6	RO	0xffff	Maximum possible number of pixel clocks per line
api_ro_frame_timing_min_line_blanking_pck	0x400011A8	RO	0x50	Minimum line blanking time in pixel clocks
api_ro_frame_timing_min_frame_blanking_lines	0x400011AA	RO	0x36	Minimum frame blanking in video timing lines
api_ro_frame_timing_min_line_length_pck_step_size	0x400011AC	RO	0x8	Minimum step size of line length in pixel clocks
api_ro_size_limits_x_addr_min	0x400011B0	RO	0x0	Minimum X-address of the addressable pixel array
api_ro_size_limits_y_addr_min	0x400011B2	RO	0x0	Minimum Y-address of the addressable pixel array
api_ro_size_limits_x_addr_max	0x400011B4	RO	0x508	Maximum X-address of the addressable pixel array
api_ro_size_limits_y_addr_max	0x400011B6	RO	0x3c8	Maximum Y-address of the addressable pixel array
api_ro_size_limits_min_x_output_size	0x400011B8	RO	0x100	Minimum x output size in pixels
api_ro_size_limits_min_y_output_size	0x400011BA	RO	0x90	Minimum y output size in pixels
api_ro_size_limits_max_x_output_size	0x400011BC	RO	0x508	Maximum x output size in pixels
api_ro_size_limits_max_y_output_size	0x400011BE	RO	0x3c8	Maximum y output size in pixels
api_ro_sub_sample_min_even_inc	0x400011C0	RO	0x1	Minimum increment for even pixels
api_ro_sub_sample_max_even_inc	0x400011C2	RO	0xf	Maximum increment for even pixels
api_ro_sub_sample_min_odd_inc	0x400011C4	RO	0x1	Minimum increment for odd pixels
api_ro_sub_sample_max_odd_inc	0x400011C6	RO	0xf	Maximum increment for odd pixels