S5K33DXX

1/3" VGA 7 µm Pixel Indirect ToF Sensor

Revision 0.01

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Data Sheet

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
0.00	November 25, 2018	Initial draft	Amit Eisenberg, Min-Sun Keel
0.01	December 11, 2018	Table 20 has been corrected	Min-Sun Keel

Table of Contents

List of Figures

List of Tables

List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
RW	Read/Write	The application has permission to read and writes in the Register field. Written value effects on the next frame.
RW/R	Read/Write	The application has permission to read and writes in the Register field. Written value effects only on exit from stand-by.
RW/C	Read/Write	The application has permission to read and writes in the Register field. Changing value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write	The application has permission to read and writes in the Register field. Changing value may cause entering stand-by / software reset.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

1.1 Introduction

S5K33DXX is a highly integrated indirect Time-of-Flight (ToF) sensor aimed for 3D depth sensing. S5K33DXX has VGA resolution and 7 µm pixel. The camera is integrated in a ToF system that also includes a modulated light source in Infrared (IR) band which is controlled by S5K33DXX. S5K33DXX chip includes demodulation ToF pixel array, analog/mixed-signal processing circuit including modulation signal generation and transmission, image correction functionality, low-power depth calculation chain, and serial transmission using up to 2-lane MIPI transmitter.

It is designed for fast but low-power operation, delivering full resolution capture at up to 60 frames per second (fps) for raw image data.

It is fabricated by the Samsung CMOS image sensor process to realize a high-efficiency and low-power photo sensor. The sensor consists of 640×480 effective pixels (644×484 active pixels) that meet with the 1/3.2-inch optical format.

The indirect ToF depth sensing concept requires four different samples of the pixel data in four different phases to calculate its depth value.

This sensor is designed as a 4-tap sensor, which means each pixel can sample four phases of data simultaneously. Each phase is considered internally as an independent pixel so conceptually, a 4-tap pixel array is expanded to 1280x960 effective pixels.

The main application of the sensor is to output RAW phase data that are translated to depth image by post processing (either in S/W or in H/W) at the back-end chip which is an Application Processor (AP).

This sensor also includes simple H/W depth engine that provides low-accuracy depth image for simple depth applications such as proximity sensing. The depth engine can be enabled only in certain sensor output modes.

This sensor has on-chip 12-bit ADC arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce pixel reset noise and Fixed-Pattern Noise (FPN). It incorporates on-chip camera functions such as defect correction, exposure setting, image scaling, depth and proximity sensing, and auto exposure statistics.

S5K33DXX CIS is programmable through a CCI or SPI serial interface and includes an on-chip One-Time Programmable (OTP) Non-Volatile Memory (NVM).

S5K33DXX is suitable for a low-power camera module with a 2.8 V/1.05 V power supply.

1.2 Indirect Time-of-Flight Depth Sensing Concept

The basic concept of indirect ToF method for depth calculation is to illuminate a scene with a modulated light source; the modulation function can be a sine wave or rectangular pulse. In this case, it is assumed to be a sinusoidal modulation.

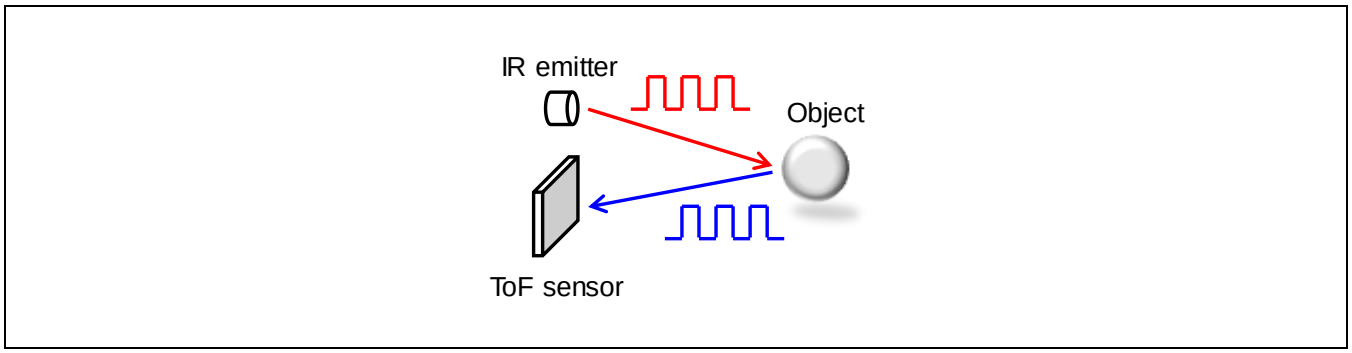


Figure 1 Indirect Time-of-Flight Concept

The reflected light is captured on a sensor and the phase shift between illuminated and reflected sine waves is used to calculate the depth value of each pixel in the sensor.

The reflected light is sampled at four different phases (with respect to the illuminating signal) to measure the phase shift.

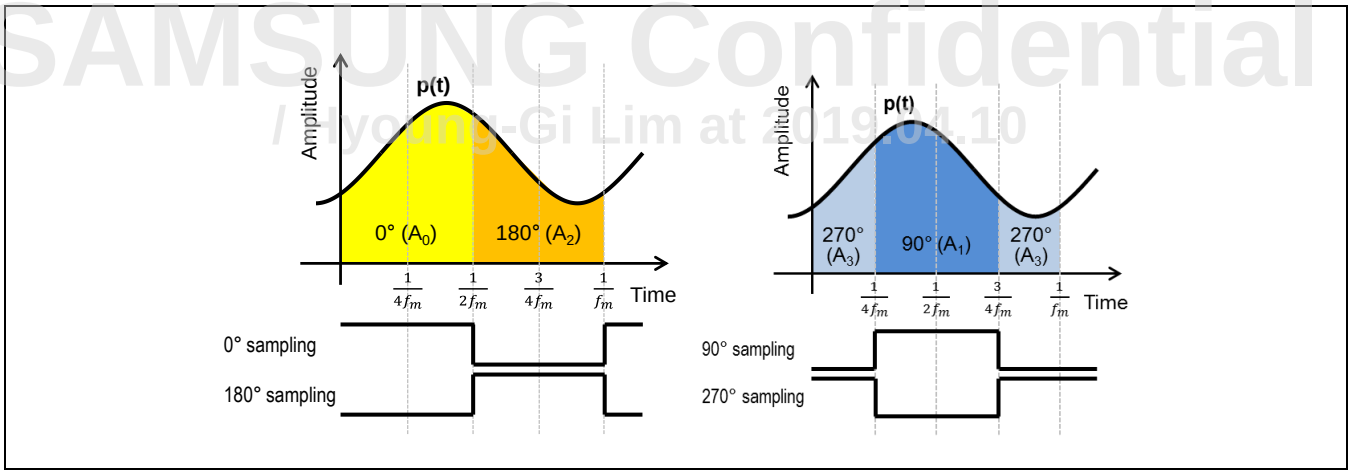


Figure 2 Time-of-Flight Demodulation Concept: 4-Phase Sampling

The phase shift (φ) and depth (d) are calculated according to the following equations (A0, A1, A2, and A3 are integrated pixel data for the phase-sampling point at 0°, 90°, 180°, and 270°, respectively).

$$\varphi = \mathrm{atan}\left(\frac{A_1 - A_3}{A_0 - A_2}\right)$$
$$\mathrm{d} = \frac{\mathrm{c}}{2f_m}\frac{\varphi}{2\pi}$$

The depth is assumed to be related to objects in the first harmony of the sine wave, therefore, the maximum range (or, unambiguous range) is a simple function of the modulation frequency (c: Speed of light and f_m: Modulation frequency) as described in the following equations.

$$\mathrm{range} = \frac{\mathrm{c}}{2f_m}$$

For example, for 10 MHz of modulation frequency, the maximal detectable range is 1.5 m.

Parameters such as amplitude and intensity are referred as depth confidence level. Use the following equations to calculate amplitude and intensity.

Amplitude: $A \propto \sqrt{(A_0 - A_2)^2 + (A_1 - A_3)^2}$

Intensity: $I = \frac{1}{4}(A_0 + A_1 + A_2 + A_3)$

Depth precision is inversely dependent on the modulation frequency.

1.3 Sensor Readout Modes

S5K33DXX supports phase sampling in the following two ways:

- 4-tap: All four phases are available for each pixel.
- 2-tap: Only two phases, whose phase difference is 180°, are available for each pixel.

1.3.1 4-Tap Mode

In the 4-tap mode, each pixel can sample four different phase points due to four storage nodes. This mode requires only one frame to calculate a depth map. The photo-gate control signals such as PGA, PGB, PGC, and PGD, are generated to sample reflected light signal at 0°, 90°, 180° and 270° points, respectively, as illustrated in *Figure 3*.

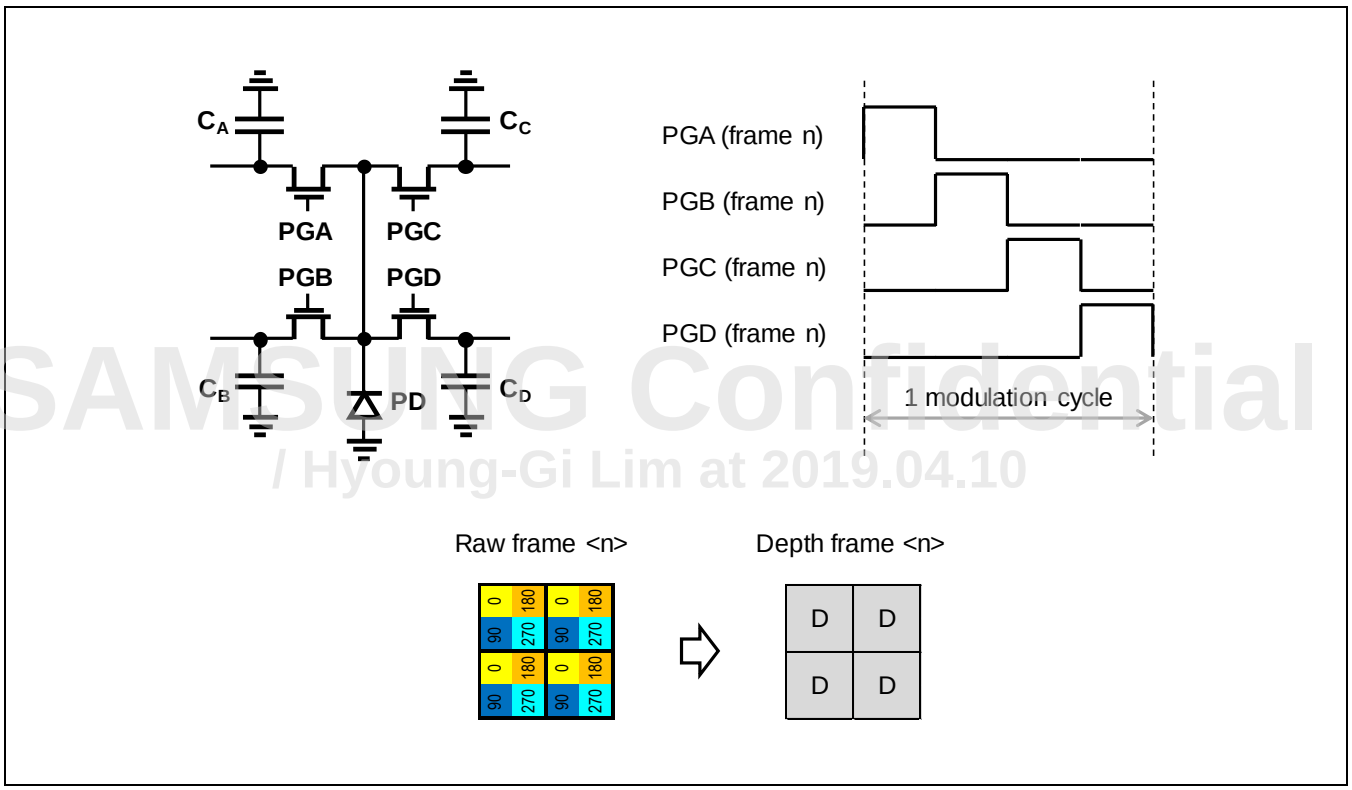


Figure 3 4-Tap Pixel Structure and Photo-Gate Control Signals

1.3.2 2-Tap Mode

In the 2-tap mode, each pixel holds two different taps of data per frame, so two frames are required to generate one depth frame. A 2-tap mode can be configured from 4-tap mode with simple averaging between adjacent vertical pixel outputs within a pixel. The 2-tap and 4-tap modes can be selected by a register setting. PGA and PGB are 0° and 180° sampling signals at the even frames, and 90° and 270° sampling signals at the odd frames, respectively.

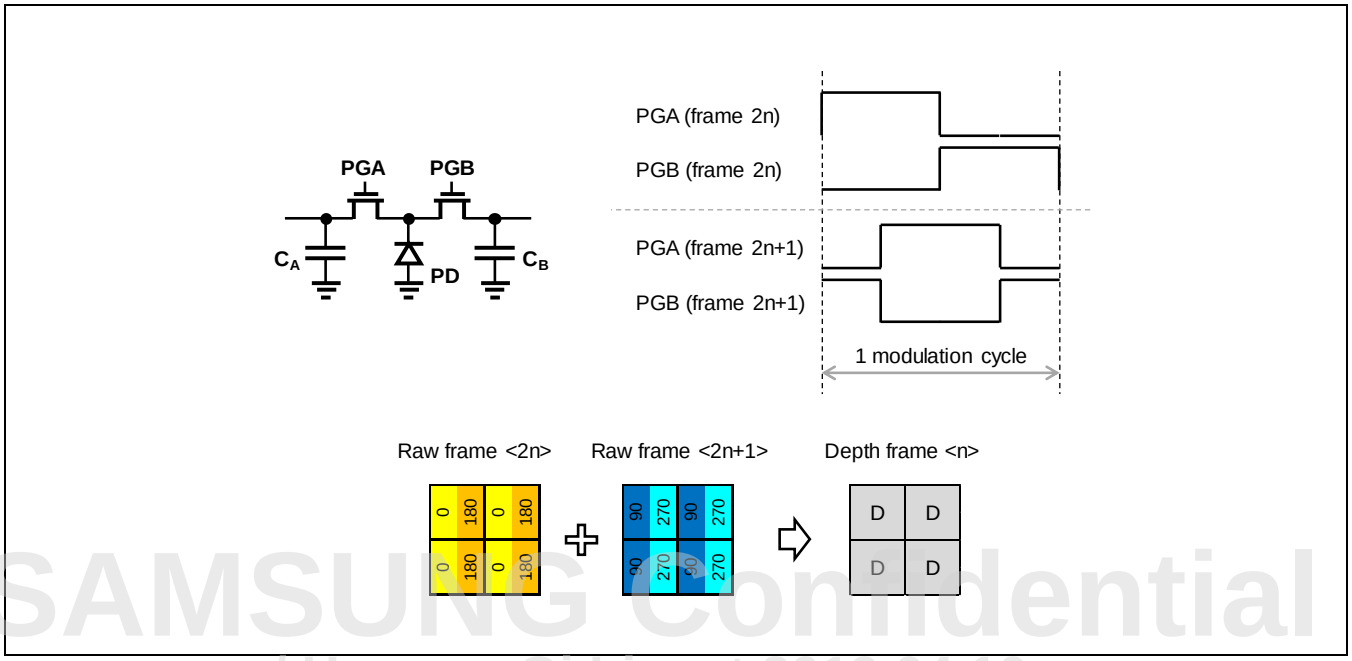


Figure 4 2-Tap Pixel Structure (Conceptual) and Photo-Gate Control Signals

1.3.3 Tap-Shuffle Mode

The tap-shuffle mode is a supplementary mode to eliminate FPN due to pixel tap and ADC mismatch. In this mode, the two out-of-phase taps (with 180° difference) are shuffled, thus each phase is read twice through different pixel position and different column ADC. This mode has better FPN performance and better SNR, by sacrificing motion blur performance due to doubled raw frame requirement.

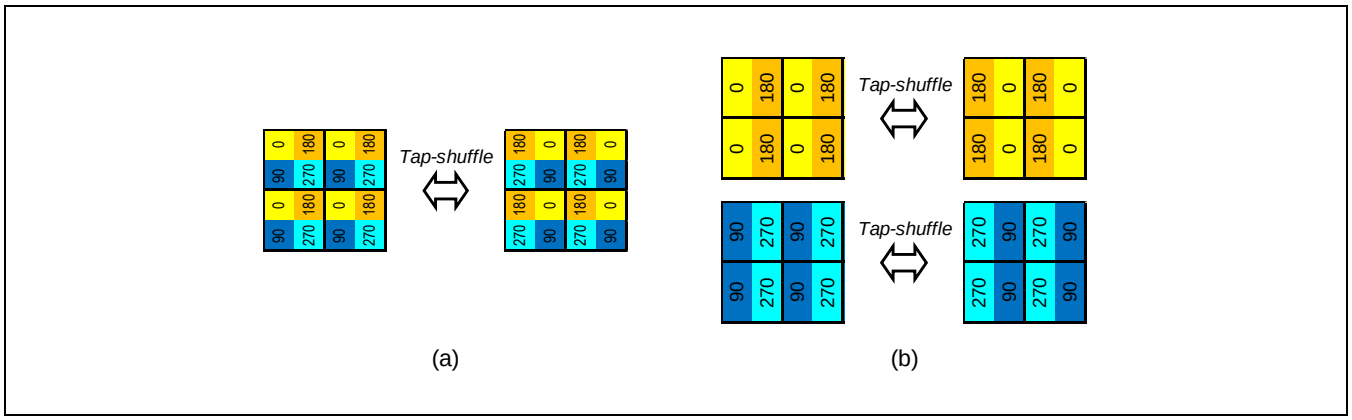
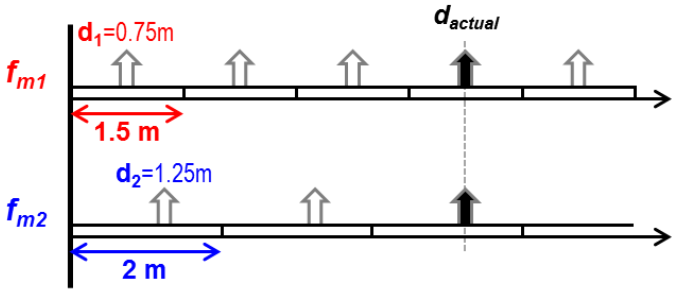


Figure 5 Tap-Shuffle Mode: (a) 4-Tap and (b) 2-Tap

1.3.4 Dual-Frequency (Phase-Unfolding) Mode

Two different modulation frequencies are used to extend the unambiguous range with minimal effect on depth precision. In the dual-frequency mode, the scene is illuminated and read by two different modulation frequencies, and the distance is calculated by finding the number of phase folding cycles. The calculation example is illustrated in *Figure 6*. The range is extended by the Greatest Common Divisor (GCD) of the two frequencies, f_{m1} and f_{m2}.



f_{m1} = 100 MHz, f_{m2} = 75 MHz (GCD(100,75) = 25)
➔ d_{max1} = 1.5 m, d_{max2} = 2 m
Actual depth, $d_{actual} = d_{max1} \times N_1 + d_1 = d_{max2} \times N_2 + d_2$
N_1 and N_2 should be determined
(N_1 = 3 and N_2 = 2 in this example)

Figure 6 Dual-Frequency (Phase Unfolding) Example

1.4 Features

S5K33DXX supports the following features:

- VGA 4:3 indirect Time-of-Flight sensor with 4-tap outputs per pixel and 1/3.2" optics
- Unit pixel size: 7.0 μm
- Effective resolution: 640 (H) × 480 (V) for pixel array, 1280 (H) × 960 (V) for output raw image
- Active resolution: 644 (H) × 484 (V) for pixel array, 1288 (H) × 968 (V) for output raw image
- Color filter: None
- Shutter type: Electronic global shutter
- Max. normal frame rate: 60 fps @ 1288 × 968
- Data rate: 1,600 Mbps/lane (up to two lanes)
- ADC accuracy: 12 bits
- Dual sensor synchronization
- Interfaces:
  - Fine interface frequency control using additional dedicated PLL for EMI avoidance and integration flexibility
  - MIPI CSI2: Two lanes (1.6 Gbps per lane)
  - Output formats: RAW12
- Control interface:
  - SPI interface: Four-wire serial communication circuit up to 20 MHz
  - Camera Control Interface (CCI) high-speed I2C-compatible - Two-wire serial communication circuit up to 1 MHz
- 32 Kb on-chip OTP memory mapped BPC and chip ID
- Vertical and horizontal flip mode
- Continuous frame capture mode
- Vertical average readout: x2, x4
- Horizontal digital binning: x2, x4
- On-sensor depth chain
- Low-power proximity sensing mode
- Pixel skip readout function
- Mapped bad pixel correction
- Built-in test pattern generation
- Supply voltage: 2.8 V for analog, 1.8 V or 2.8 V for I/O, and 1.05 V for digital core supply
- Operating temperature: -20 °C to +70 °C

2 Pad Configuration

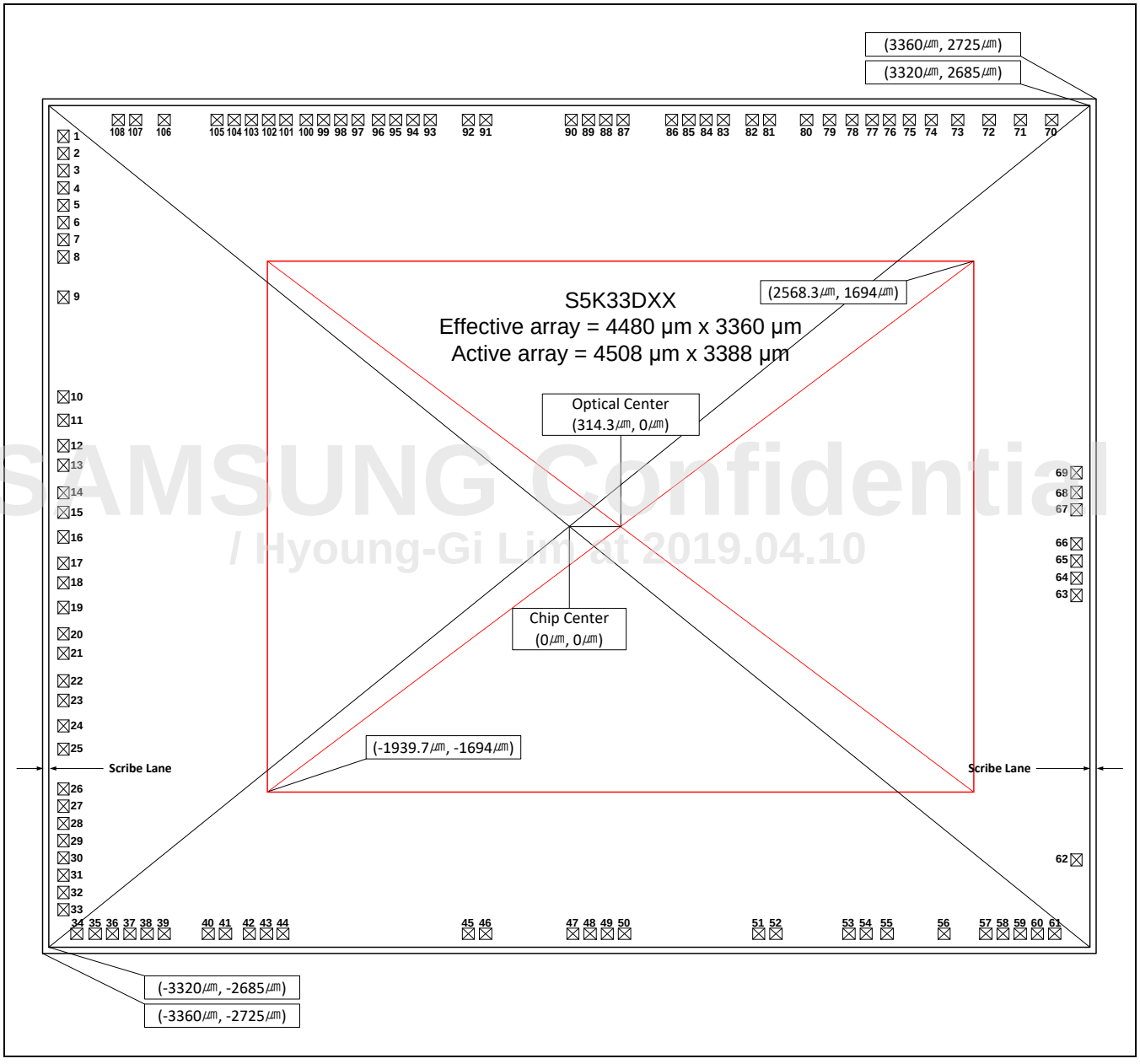


Figure 7 Top View of Chip Dimension

2.1 Pad Description

Table 1 Pad Description

Pad No.	Pad Name	Type	A/D	Description
1	TST	I	D	Test configuration pin (tie low in normal operation)
2	VDDD	P	D	Digital power (1.05 V)
3	VDDD	P	D	Digital power (1.05 V)
4	VSSD	G	D	Digital ground (0 V)
5	VSSD	G	D	Digital ground (0 V)
6	MCLK	I	D	Main clock input
7	VSSIO	G	A	I/O ground (0 V)
8	VDDIO	P	A	I/O power (1.8 V)
9	VDDA_M	P	A	Analog power (2.8 V)
10	VDDD	P	D	Digital power (1.05 V)
11	VSSD	G	D	Digital ground (0 V)
12	M_DNDATA0	O	A	MIPI data lane 0 (negative)
13	M_DPDATA0	O	A	MIPI data lane 0 (positive)
14	M_DNDATA1	O	A	MIPI data lane 1 (negative)
15	M_DPDATA1	O	A	MIPI data lane 1 (positive)
16	VSSD	G	D	Digital ground (0 V)
17	M_DNCLK	O	A	MIPI clock lane (negative)
18	M_DPCLK	O	A	MIPI clock lane (positive)
19	VDDD	P	D	Digital power (1.05 V)
20	(NC)	-	-	No connection
21	(NC)	-	-	No connection
22	(NC)	-	-	No connection
23	(NC)	-	-	No connection
24	VSSD	G	D	Digital ground (0 V)
25	VDDD	P	D	Digital power (1.05 V)
26	VDDD	P	D	Digital power (1.05 V)
27	VDDD	P	D	Digital power (1.05 V)
28	VSSD	G	D	Digital ground (0 V)
29	VSSD	G	D	Digital ground (0 V)
30	SE	O	D	Digital I/O
31	MSE	O	D	Digital I/O
32	VDDIO	P	A	I/O power (1.8 V)
33	VSSIO	G	A	I/O ground (0 V)
34	RSTN	I	D	Master reset, active low (XSHUTDOWN)
35	I2C_SPI_N_SEL	I	D	SPI/IIC select (1: IIC, 0: SPI)
36	VSYNC	O	D	Vertical sync. output
37	VSYNC_IN	I	D	Vertical sync. input to enable dual sensor function

Pad No.	Pad Name	Type	A/D	Description
38	HSYNC	O	D	Horizontal sync. output
39	(NC)	-	-	No connection
40	VSSA	G	A	Analog ground (0 V)
41	VDDA	P	A	Analog power (2.8 V)
42	VSSA	G	A	Analog ground (0 V)
43	VDDD	P	D	Digital power (1.05 V)
44	VSSD	G	D	Digital ground (0 V)
45	VDDPG	P	A	Photo-Gate Driver (PGD) power (1.05 V)
46	VSSA	G	A	Analog ground (0 V)
47	VDDPG	P	A	PGD power (1.05 V)
48	VSSA	G	A	Analog ground (0 V)
49	VDDPG	P	A	PGD power (1.05 V)
50	VSSA	G	A	Analog ground (0 V)
51	VDDPG	P	A	PGD power (1.05 V)
52	VSSA	G	A	Analog ground (0 V)
53	VSSA	G	A	Ground (0 V)
54	VDDMD	P	A	Power (2.8 V)
55	MD_CKP	O	A	Differential modulation clock output (positive)
56	MD_CKN	O	A	Differential modulation clock output (negative)
57	VSSD	G	D	Digital ground (0 V)
58	VDDD	P	D	Digital power (1.05 V)
59	VSSA	G	A	Analog ground (0 V)
60	VDDA	P	A	Analog power (2.8 V)
61	VSSA	G	A	Analog ground (0 V)
62	(NC)	-	-	No connection
63	(NC)	-	-	No connection
64	(NC)	-	-	No connection
65	(NC)	-	-	No connection
66	(NC)	-	-	No connection
67	(NC)	-	-	No connection
68	(NC)	-	-	No connection
69	(NC)	-	-	No connection
70	VNTG	G	A	NTG voltage
71	VNTGX	G	A	NTGX voltage
72	VNSG	G	A	NSG voltage
73	VNOG	G	A	NOG voltage
74	VTG	P	A	TG voltage
75	VRGSL	P	A	RGSL voltage
76	VSSA	G	A	Analog ground (0 V)

Pad No.	Pad Name	Type	A/D	Description
77	VDDA	P	A	Analog power (2.8 V)
78	VTGX	P	A	TGX voltage
79	VSG	P	A	SG voltage
80	VOG	P	A	OG voltage
81	VSSA	G	A	Analog ground (0 V)
82	VDDPG	P	A	PGD power (1.05 V)
83	VSSD	G	D	Digital ground (0 V)
84	VSSD	G	D	Digital ground (0 V)
85	VDDD	P	D	Digital power (1.05 V)
86	VDDD	P	D	Digital power (1.05 V)
87	VSSA	G	A	Analog ground (0 V)
88	VDDPG	P	A	PGD power (1.05 V)
89	VSSA	G	A	Analog ground (0 V)
90	VDDPG	P	A	PGD power (1.05 V)
91	VSSA	G	A	Analog ground (0 V)
92	VDDPG	P	A	PGD power (1.05 V)
93	SDI	B	D	SPI mode: Serial data input, IIC mode: IIC data
94	SCK	I	D	SPI mode: Serial clock input, IIC mode: IIC input clock
95	SDO	O	D	SPI mode: Serial data output, IIC mode: no connection
96	XCE	I	D	SPI mode: Serial communication enable, IIC mode: IIC slave address selection
97	VSSD	G	D	Digital ground (0 V)
98	VSSD	G	D	Digital ground (0 V)
99	VDDD	P	D	Digital power (1.05 V)
100	VDDD	P	D	Digital power (1.05 V)
101	VDDIO	P	A	I/O power (1.8 V)
102	VSSIO	G	A	I/O ground (0 V)
103	GPIO_3	B	D	General purpose I/O - 3
104	GPIO_2	B	D	General purpose I/O - 2
105	GPIO_1	B	D	General purpose I/O - 1
106	VDDA_M	P	A	Analog power (2.8 V)
107	VSSD	G	D	Digital ground (0 V)
108	VDDD	P	D	Digital power (1.05 V)

2.2 Application Circuit

Figure 8 illustrates a module application circuit.

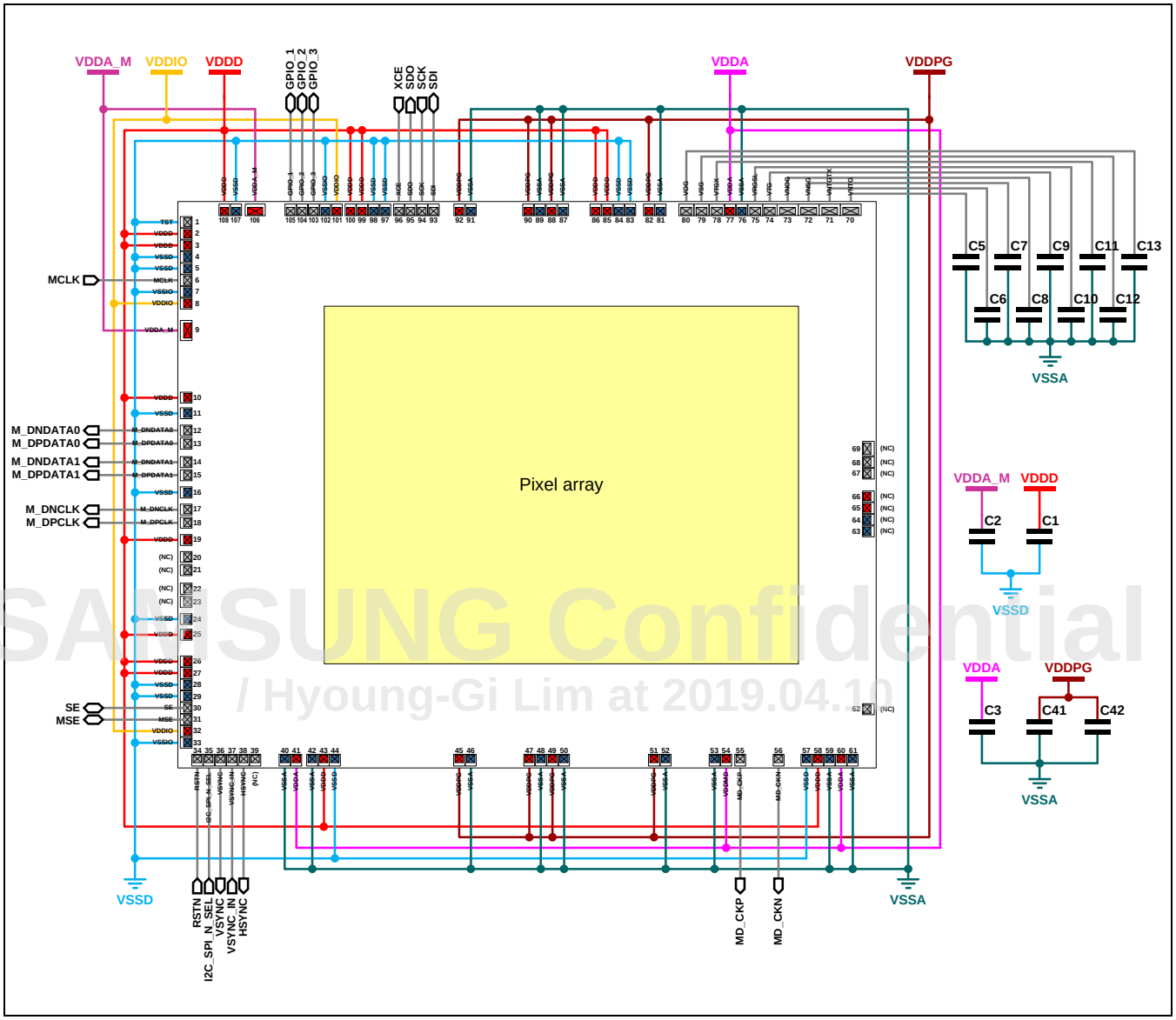


Figure 8 Module Application Circuit

2.3 Pixel Array Information

Figure 9 illustrates a diagram of pixel array.

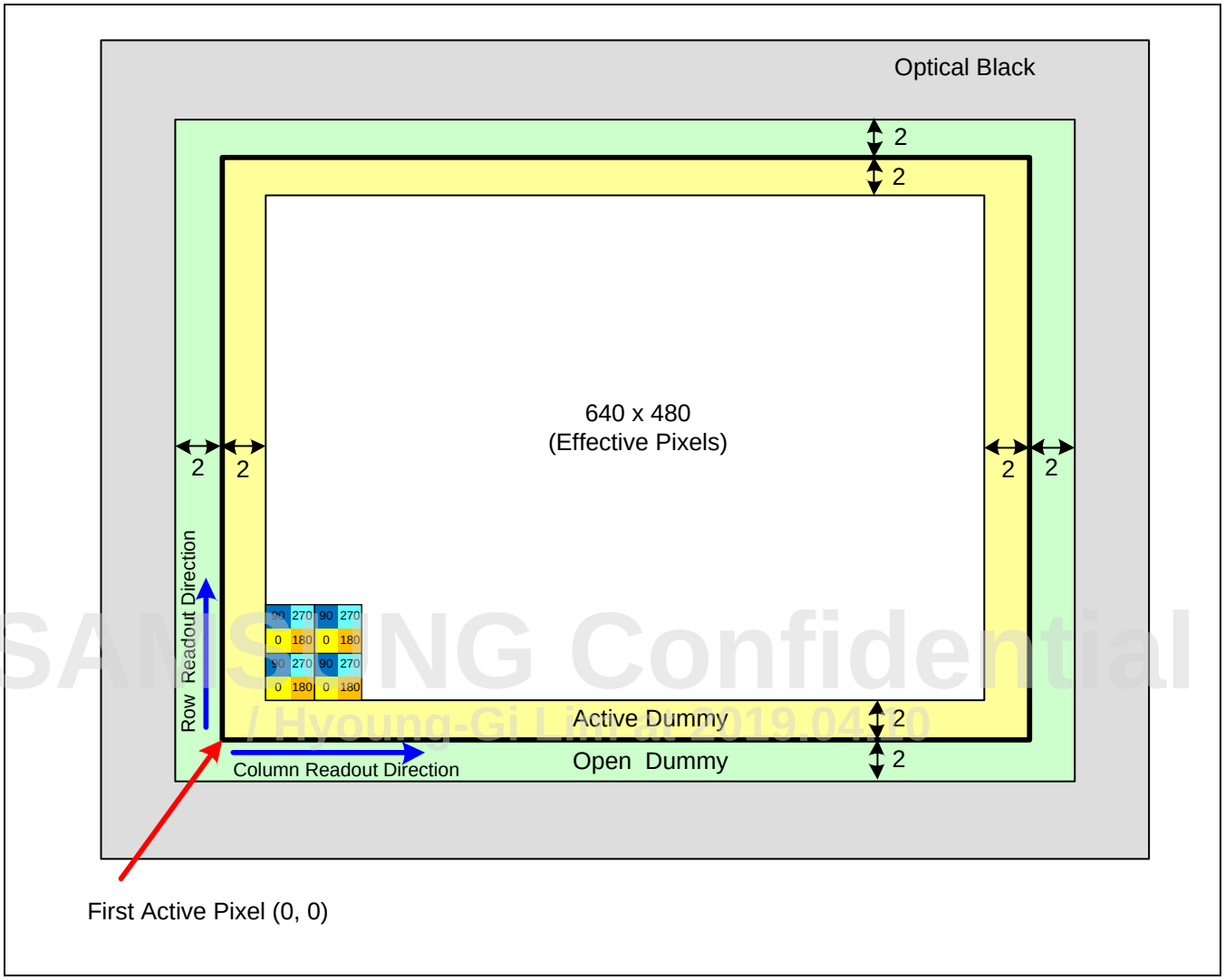


Figure 9 Pixel Array Diagram

3 Power Sequence

3.1 Operating Modes

Sensor module has four operating modes such as power-off, hardware standby, software standby, and streaming (*Table 2*). Transition from one mode to another is achieved by issuing the appropriate mode command through the CCI serial control interface, the RSTN (XSHUTDOWN) signal changing state, and the power supplies. By default, S5K33DXX powers up with the CSI-2 serial data interface enabled. *Figure 10* illustrates the valid mode changes for the sensor module.

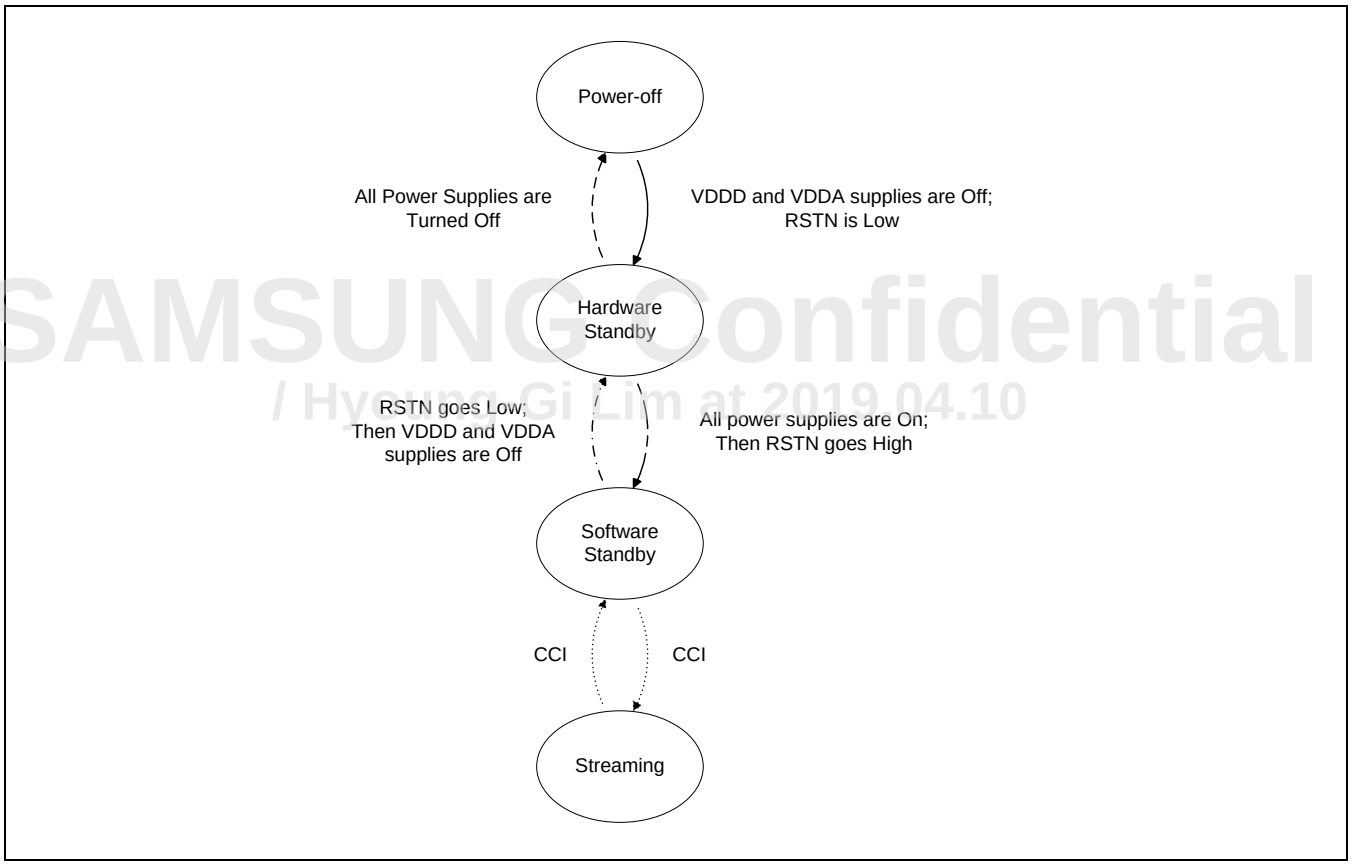


Figure 10 System State Diagram

Table 2 Operating Mode Summary

Power State	Description
Power-off	Power supplies are turned off
Hardware standby	No communication with the sensor is possible Internal core power shut-off only by external VDDD and VDDA power down.
Software standby	CCI communication with sensor is possible Core is powered on.
Streaming	The sensor module is fully powered and streams the image data on the CSI-2 bus

Table 3 describes the registers that control the operating mode of the camera module.

Table 3 Operating Mode Registers

Start	Reset	Name	Type	Width	Description
0x0100	0x00	api_rw_general_setup_mode_select	RW/SR	[0:0]	0 = Software standby 1 = Streaming (active video)

3.2 Power-Up Sequence

The digital and analog supply voltages can be powered up in any order, for example, VDDD then VDDA, or VDDA then VDDD.

After power up, RSTN (XSHUTDOWN) should be low when the power supplies are brought up, then the sensor module goes into hardware standby mode. As long as RSTN is low and VDDD is down, the sensor module stays in hardware standby mode.

The assertion of RSTN ensures that the CCI register values are initialized correctly to their default values.

When RSTN goes to high, all PADs exit from fail-safe mode, and switch to normal operating mode.

Either MCLK can be initially low and then enabled during software standby mode or MCLK can be a free running clock.

NOTE:

1. At hardware standby mode, external VDDD and VDDA should be off.
2. External clock (MCLK) is recommended to be off in software standby mode to reduce power consumption.

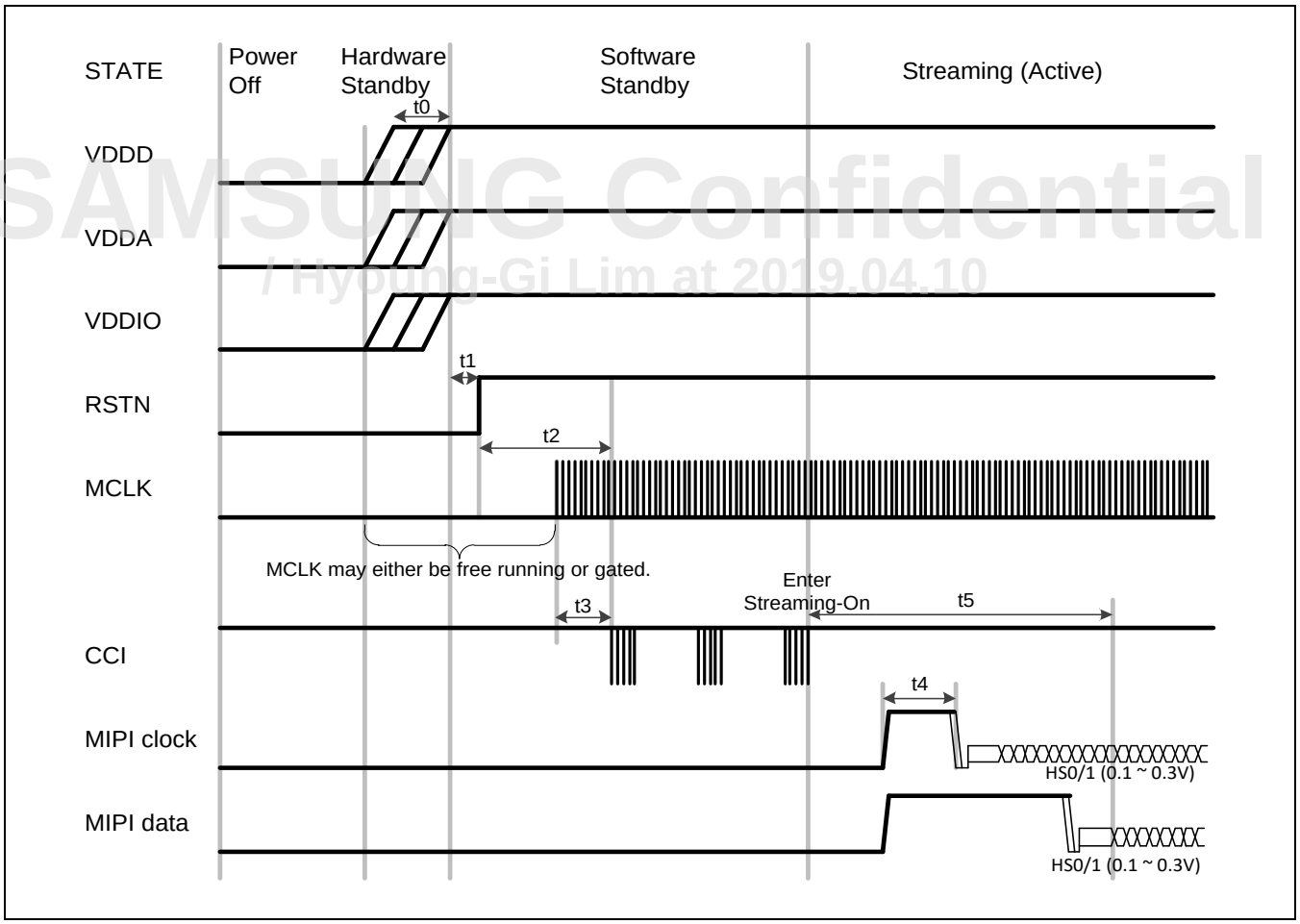


Figure 11 Power-Up Sequence

Table 4 Power-Up Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
VDDA//VDDD/VDDIO rising time	t0	VDDA/VDDD/VDDIO may rise in any order. The rising separation can vary from 0 ns to indefinite.		ns
VDDD rising to RSTN (XSHUTDOWN) rising	t1	0.0	–	ns
RSTN (XSHUTDOWN) rising to first CCI transaction	t2	10	–	µs
Minimum no. of MCLK (EXTCLK) cycles prior to the first CCI transaction	t3	23,000	–	MCLK cycles
PLL startup/lock time	t4	–	1	ms
DPHY initialization period (TINIT)	t5	0.1	–	ms
Entering streaming mode - The first frame start sequence	t6	+ the delay according to the coarse integration time value		-

3.3 Power-Down Sequence

The digital and analog supply voltages are powered down in any order, for example, VDDD then VDDA, or VDDA then VDDD.

Similar to the power-up sequence, the MCLK (EXTCLK) input clock is either gated or continuous.

If the CCI command to exit streaming is received when a frame of valid active data is being output, then the sensor module must wait for the frame end code before entering the software standby mode. Frame end code can come either after all frame pixels are transmitted or during the frame when next line transmission is completed - based on a configuration register. For more information, refer to S5K33DXX Application Note.

If the CCI command to exit streaming mode is received during the inter frame time, then the sensor module must immediately enter the software standby mode.

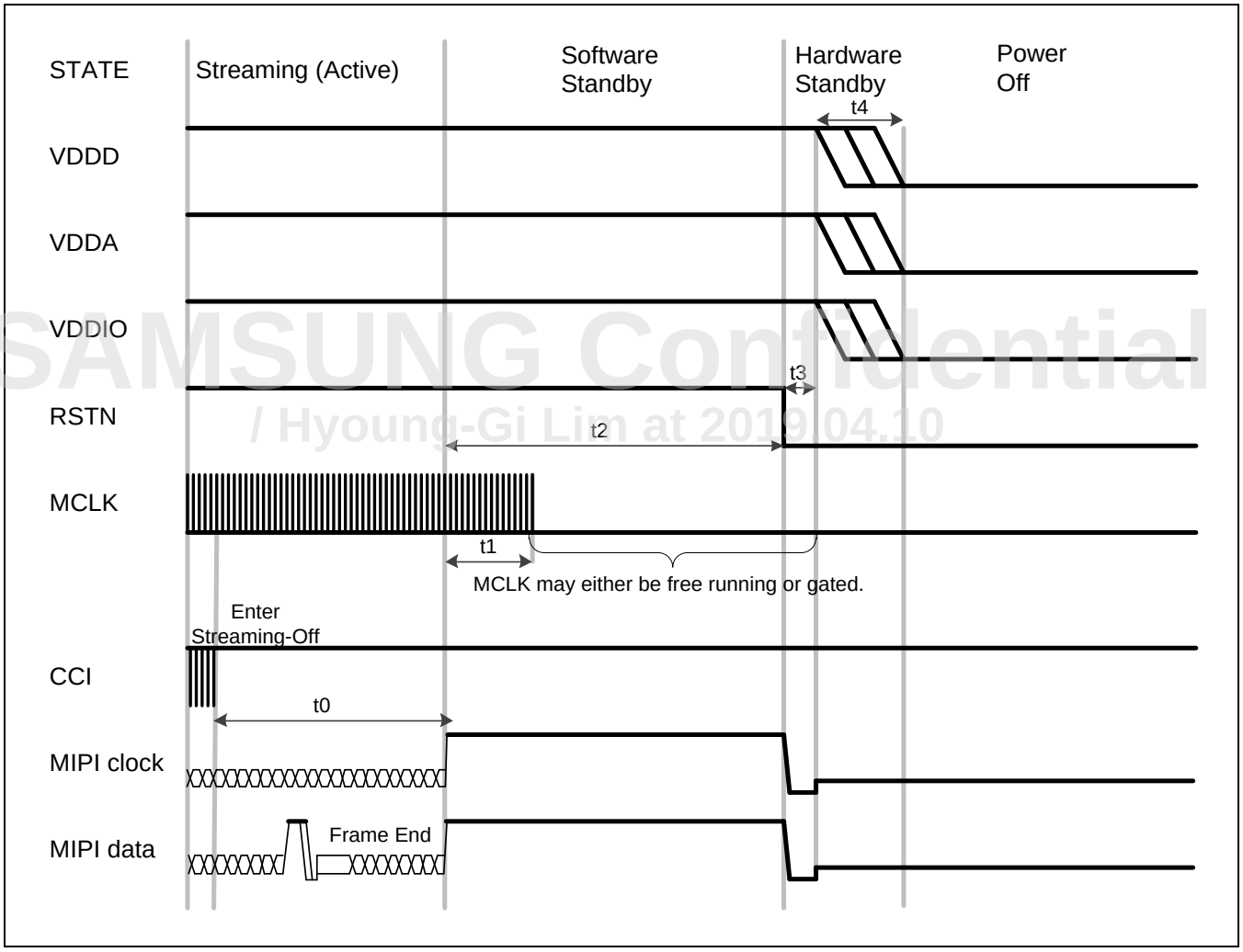


Figure 12 Power-Down Sequence

Table 5 Power-Down Sequence Timing Constraints

Constant	Label	Min.	Max.	Unit
Enter software standby CCI command-Device in software standby mode	t0	When outputting a frame of MIPI, the data waits for the MIPI frame end code before entering software standby; otherwise it enters software standby mode immediately.		–
Minimum number of MCLK (EXTCLK) cycles after the last CCI transaction or MIPI frame end code	T1	512	–	MCLK cycles
Last CCI transaction or MIPI frame end code - RSTN (XSHUTDOWN) falling	t2	512	–	
RSTN (XSHUTDOWN) falling to VDDD or VDDA falling	t3	0.0	–	ns
VDDA/VDDD/VDDIO falling time	t4	VDDA/VDDD/VDDIO may fall in any order. The rising separation can vary from 0 ns to indefinite.		

NOTE:

1. For minimal power during hardware standby mode, external VDDD should be turned off.

3.4 Software Standby Mode Sequence

Entering software standby mode is the same as entering hardware standby mode but without RSTN (XSHUTDOWN) assertion to low and without applying external VDDD power down.

There are several options to define how the last frame before entering the software reset, according to the following parameter described in *Table 6*.

Table 6 Abort Frame Timing Transition Options upon Entering S/W Reset

Timing Transition Type	Setting
abort_timing_on_sw_stby	0 = Abort timing immediately, even during read out
	1 = Abort timing after read out ends
	2 = Abort timing on end of frame

4 Control Interface

S5K33DXX control is performed using register writes. S5K33DXX can be controlled using the Camera Control Interface (CCI).

Table 7 SPI/CCI PAD Sharing

SPI	CCI
SDI	SDA
SCK	SCL
XCE	I2C_ID
SDO	–
I2C_SPI_N_SEL	

4.1 SPI Control Interface

S5K33DXX can use the SPI interface for control registers communication. SPI interface is illustrated in *Figure 13*.

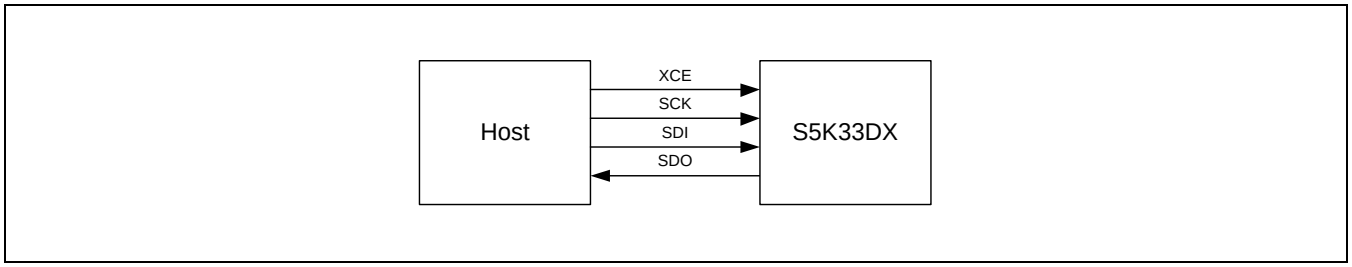


Figure 13 SPI Control Interface

The following legend table describes SPI signals in *Figure 13*.

Pin Name	Description
XCE	Serial communication enable
SCK	Serial communication clock input
SDI	Serial data input
SDO	Serial data output

If it is not necessary to read the control registers and chip ID, the SDO pad can be left unconnected.

4.1.1 SPI Timing Definitions

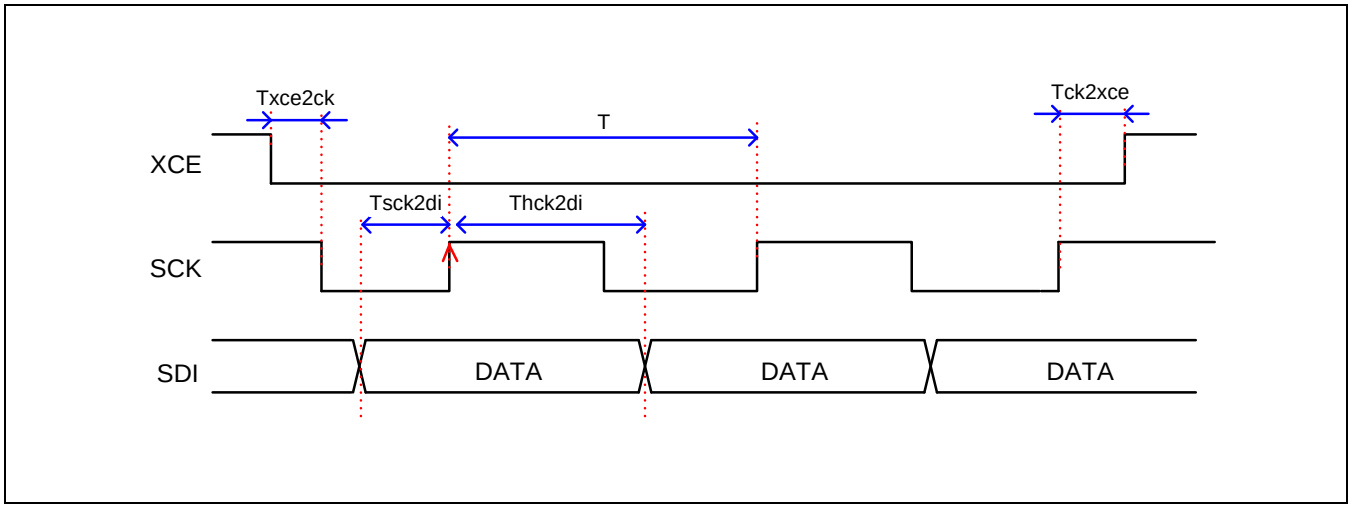


Figure 14 Timing Diagram of SPI Write Mode 11

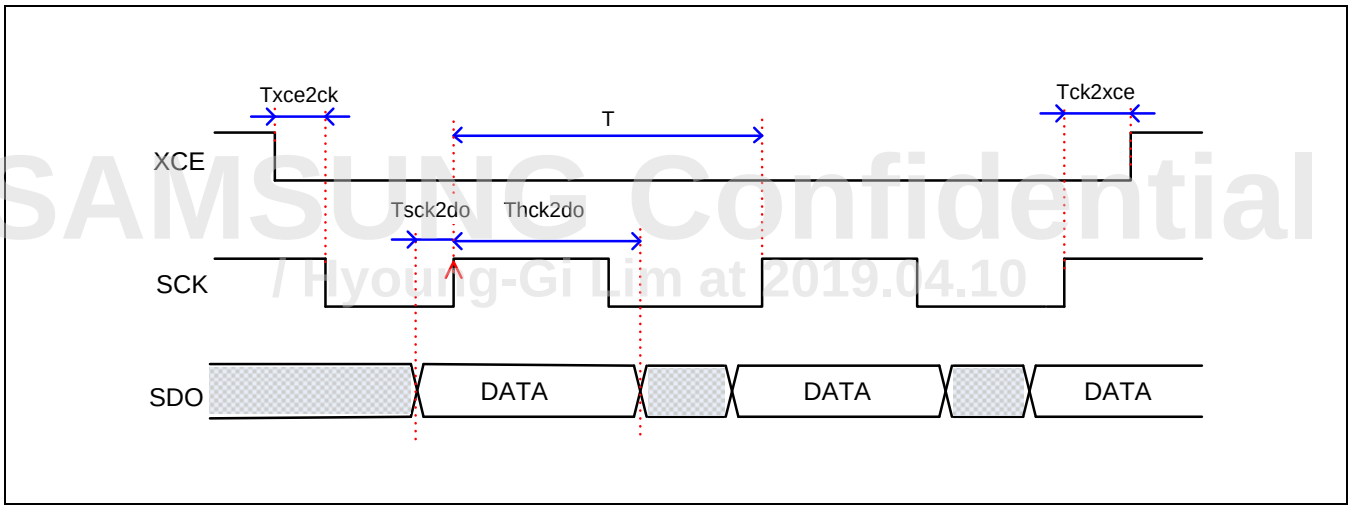


Figure 15 Timing Diagram of SPI Read Mode 11

Table 8 SPI Write/Read Timing Specification

Description	Symbol	Min.	Typ.	Max.	Unit
MCLK (external clock) frequency	Fext	6	–	64	MHz
SPI clock frequency	F (1)	–	–	Fext/3	
	F (2)	–	–	20	
SPI clock period	T	1/F	–	–	nSec
SPI clock duty cycle	Tdc	45	–	55	%
XCE negedge to SCK edge	Txce2ck	T	–	–	nSec
SCK posedge to XCE edge	Tck2xce	2T	–	–	
SCK to SDI setup time	Tsck2di	7	–	–	
SCK to SDI hold time	Thck2di	5	–	–	
SCK to SDO setup time	Tsck2do	T/2-20	–	–	
SCK to SDO hold time	Thck2do	T/2	–	–	

NOTE:

1. External clock is used.
2. PLL stable. Internal system clock can be set to maximum of 60 MHz.

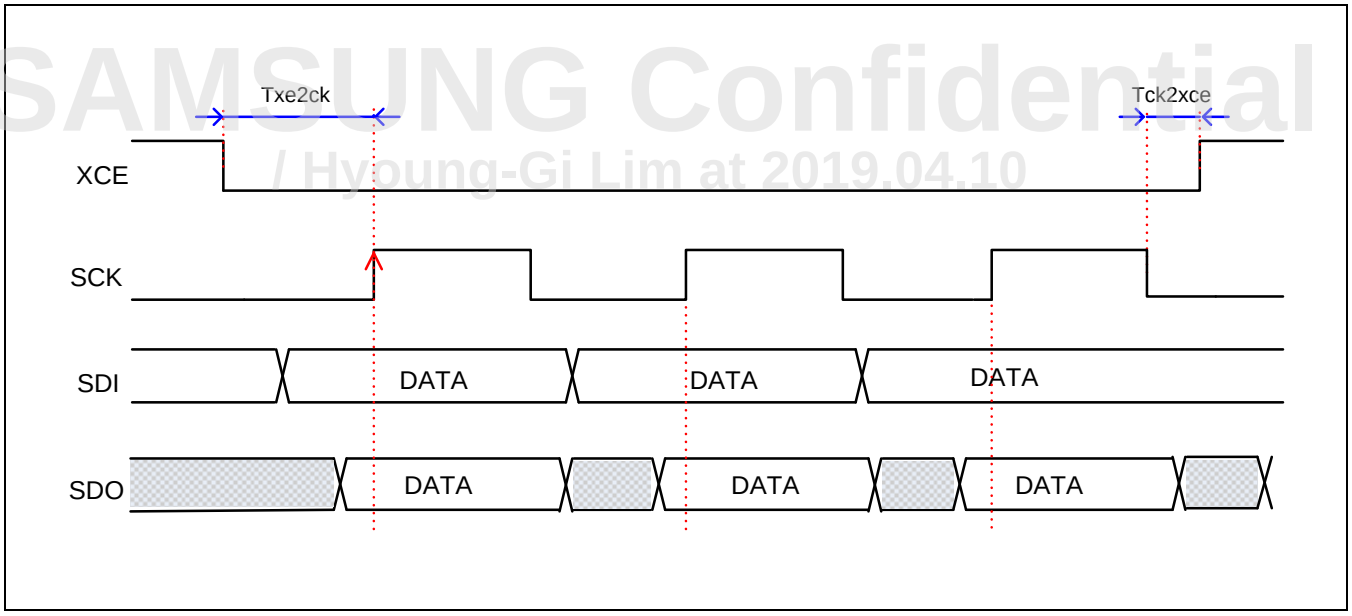


Figure 16 SPI Write/Read Mode 00

4.1.2 SPI Sequences

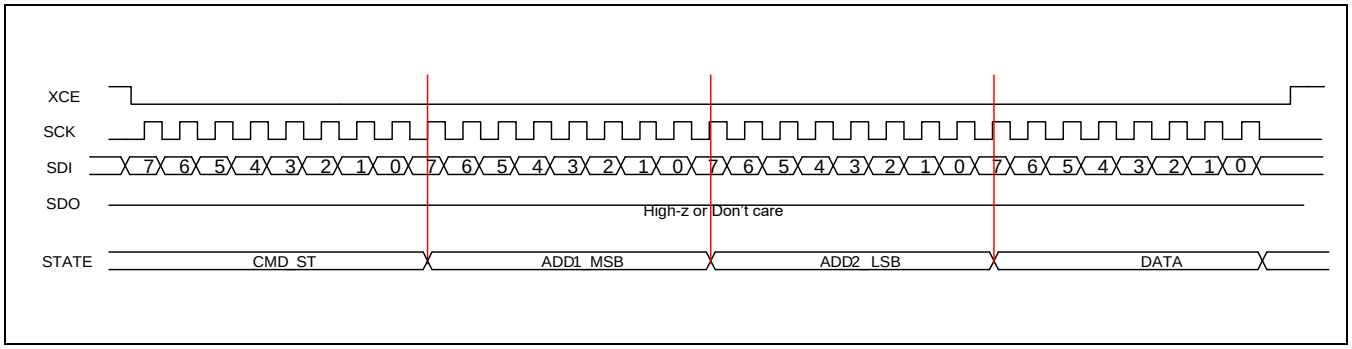


Figure 17 SPI Write Sequence (1 Cycle)

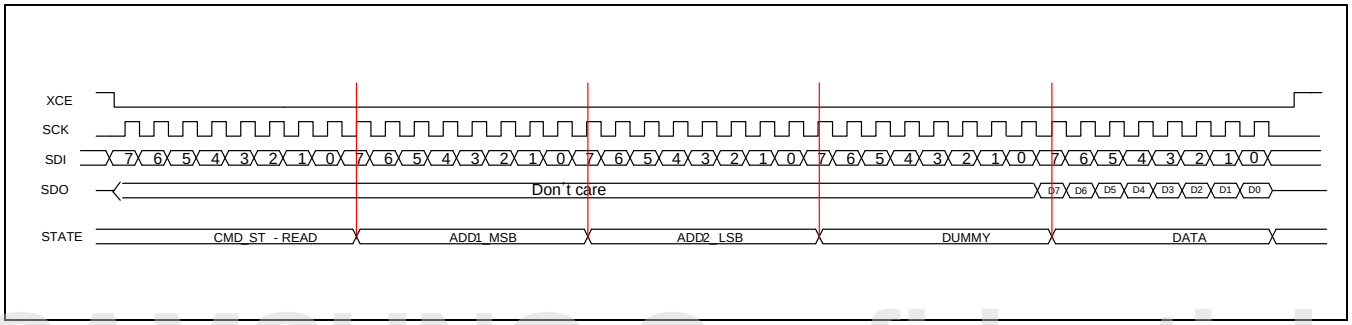


Figure 18 SPI Read

4.2 Camera Control Interface

S5K33DXX supports the Camera Control Interface (CCI), which is an I2C fast-mode compatible interface for controlling the transmitter. S5K33DXX always acts as a slave in the CCI bus. CCI is capable of handling several slaves in the bus, but multi-master mode is not supported. Typically, only the receiver and transmitter are connected to the CCI bus. This ensures a pure S/W implementation.

The CCI is different from the system I2C bus, but I2C-compatibility ensures that it is also possible to connect the transmitter to the system I2C bus. CCI is a subset of the I2C protocol, including the minimum combination of obligatory features for the I2C slave device specified in the I2C specification. Therefore, transmitters complying with the CCI specification can also be connected to the system I2C bus. However, it is important to ensure that the I2C masters do not try to utilize these I2C features, which are not supported in transmitters complying with the CCI specification. Each transmitter conformed to the CCI specification can have additional features implemented to support I2C.

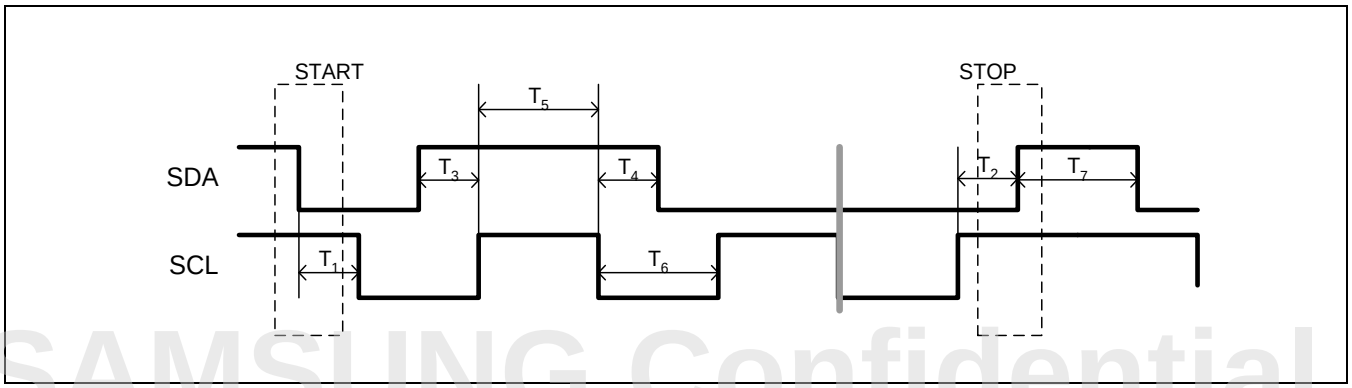


Figure 19 Timing Diagram of CCI

Table 9 I2C Standard Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	100	kHz
Hold time for start condition	T_1	4.0	–	µs
Setup time for stop condition	T_2	4.0	–	
Data setup time	T_3	250	–	ns
Data hold time	T_4	0	3.45	µs
High period of the SCL clock	T_5	4.0	–	
Low period of the SCL clock	T_6	4.7	–	
Bus free time between stop and start conditions	T_7	4.7	–	
Rise time for both SDA and SCL signals	–	–	1000	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Table 10 I2C Fast Mode Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	400	kHz
Hold time for start condition	T_1	0.6	–	µs
Setup time for stop condition	T_2	0.6	–	
Data setup time, external clock (MCLK) above 12.8 MHz	T_3	0.1	–	µs
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T_4	0	0.9	µs
High period of the SCL clock	T_5	0.6	–	
Low period of the SCL clock	T_6	1.3	–	
Bus free time between stop and start conditions	T_7	1.3	–	
Rise time for both SDA and SCL signals	–	–	300	ns
Fall time for both SDA and SCL signals	–	–	300	
Capacitive load for each bus line	CB	–	400	pF

Table 11 I2C Fast Mode Plus (FM+) Timing Specifications

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	–	0	1	MHz
Hold time for start condition	T_1	0.26	–	µs
Setup time for stop condition	T_2	0.26	–	
Data setup time, external clock (MCLK) above 24 MHz	T_3	0.05	–	µs
Data setup time, external clock (MCLK) between 12.8 and 24 MHz		0.1	–	
Data setup time, external clock (MCLK) below 12.8 MHz		0.6	–	
Data hold time	T_4	0	–	µs
High period of the SCL clock	T_5	0.26	–	
Low period of the SCL clock	T_6	0.5	–	
Bus free time between stop and start conditions	T_7	0.5	–	
Rise time for both SDA and SCL signals	–	–	120	ns
Fall time for both SDA and SCL signals	–	–	120	
Capacitive load for each bus line	CB	–	550	pF

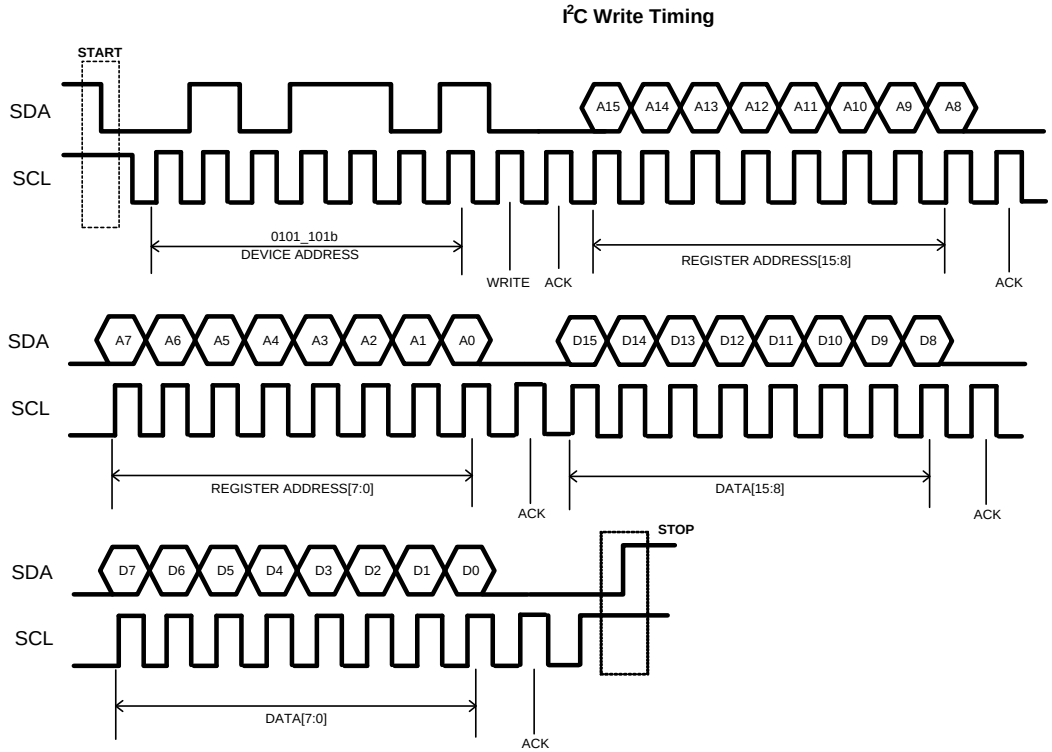


Figure 20 CCI Write Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

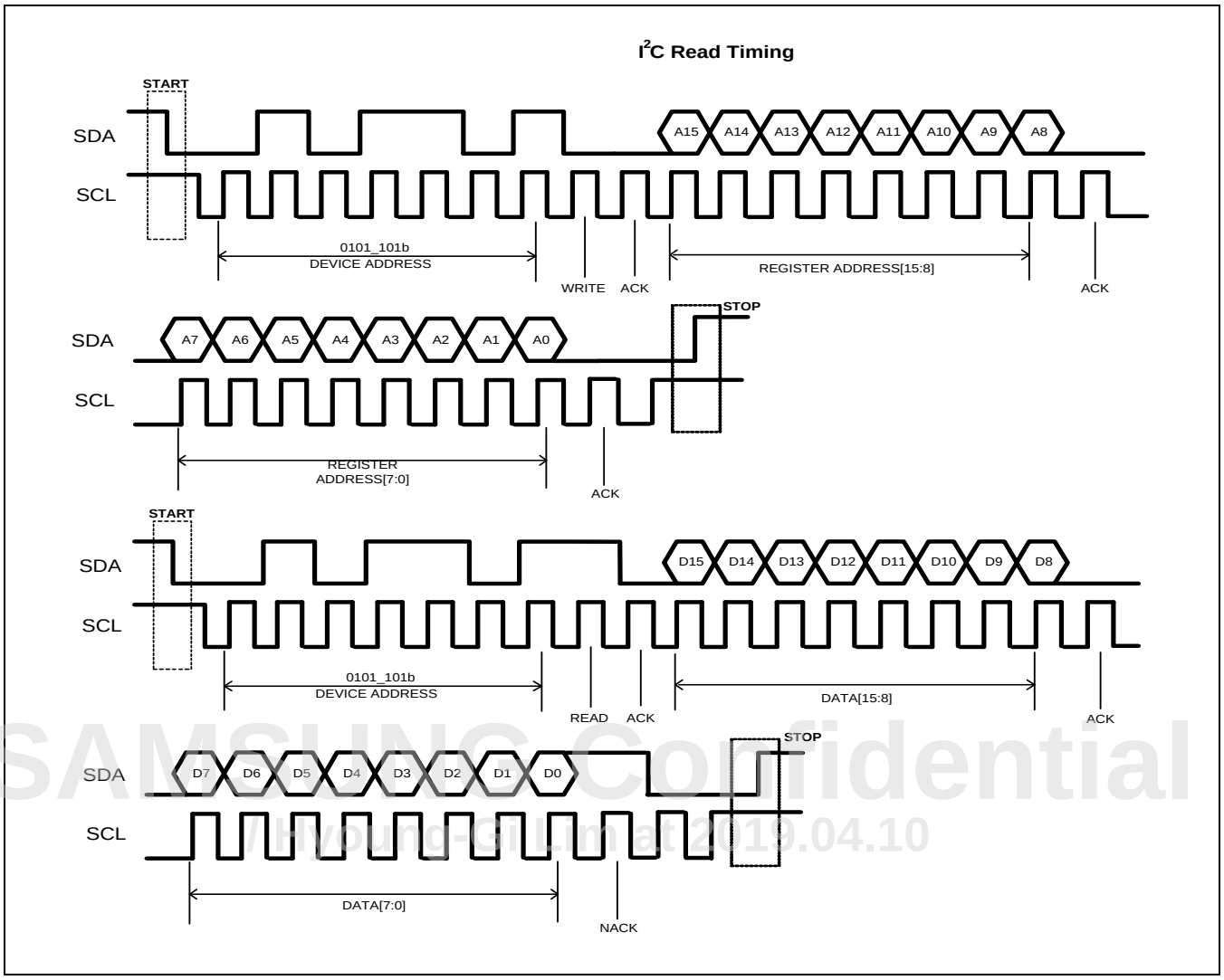


Figure 21 CCI Read Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

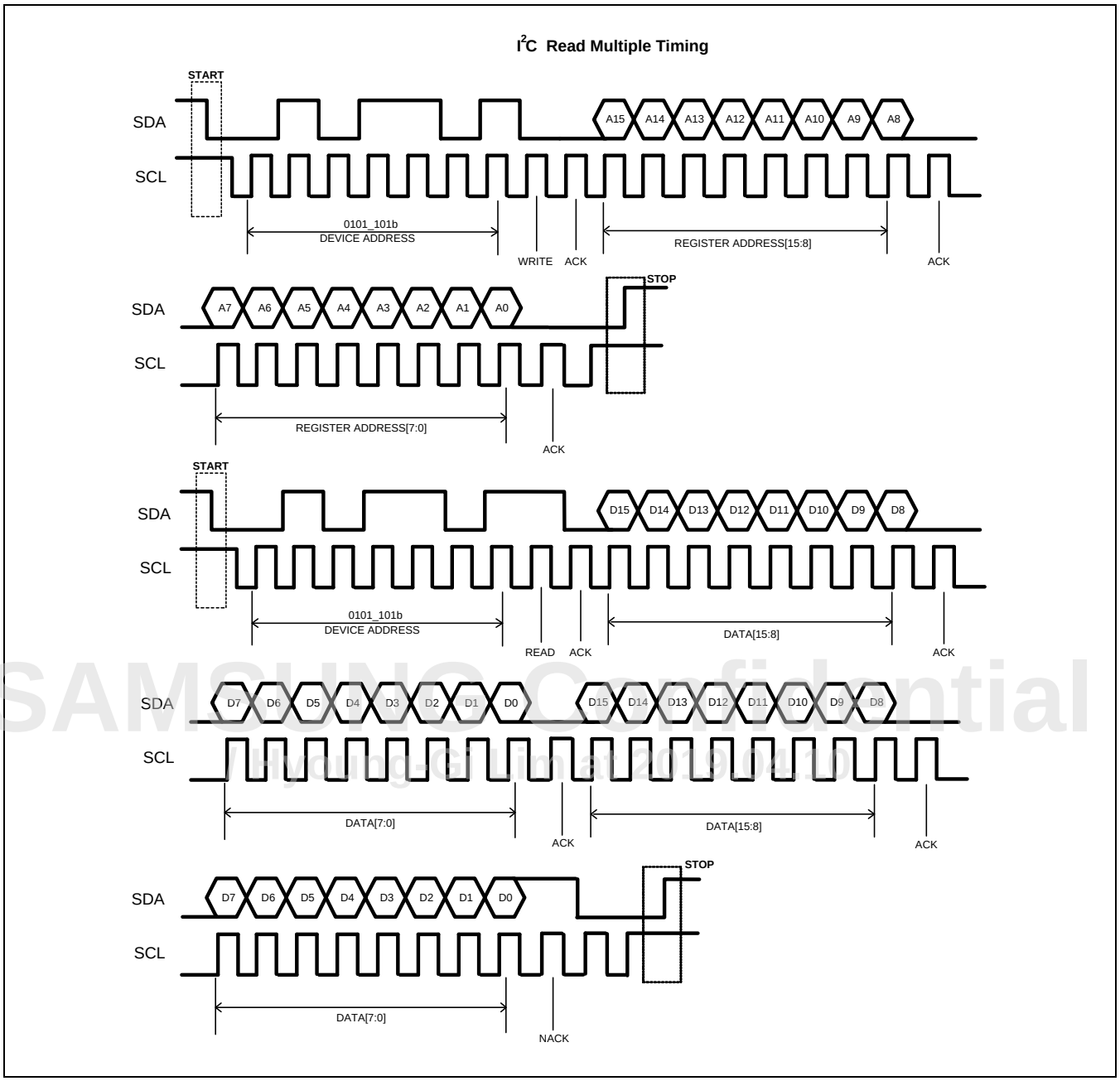


Figure 22 CCI Read Multiple Timing Example

NOTE: Pin configuration of I2C_ID changes the device address as described in the pad description.

You can configure up to two I2C slave addresses using I2C_ID pins.

Table 12 I2C ID Address (XCE Pad)

XCE	Slave Address (7-bit + Read Mode)	Slave Address (7-bit + Write Mode)	Comment
0	0010_0001b/21h	0010_0000b/20h	Address 1
1	0101_1011b/5Bh	0101_1010b/5Ah	Address 2

5 Functional Features

5.1 Block Diagram

S5K33DXX is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip Phase-Locked Loop (PLL) to generate all internal clocks from a single master input clock running between 12 MHz and 60 MHz. Dedicated PLL generates the output interface clocks for maximum flexibility in interface frequency and for avoiding EMI.

The block diagram of the sensor is illustrated in *Figure 23*.

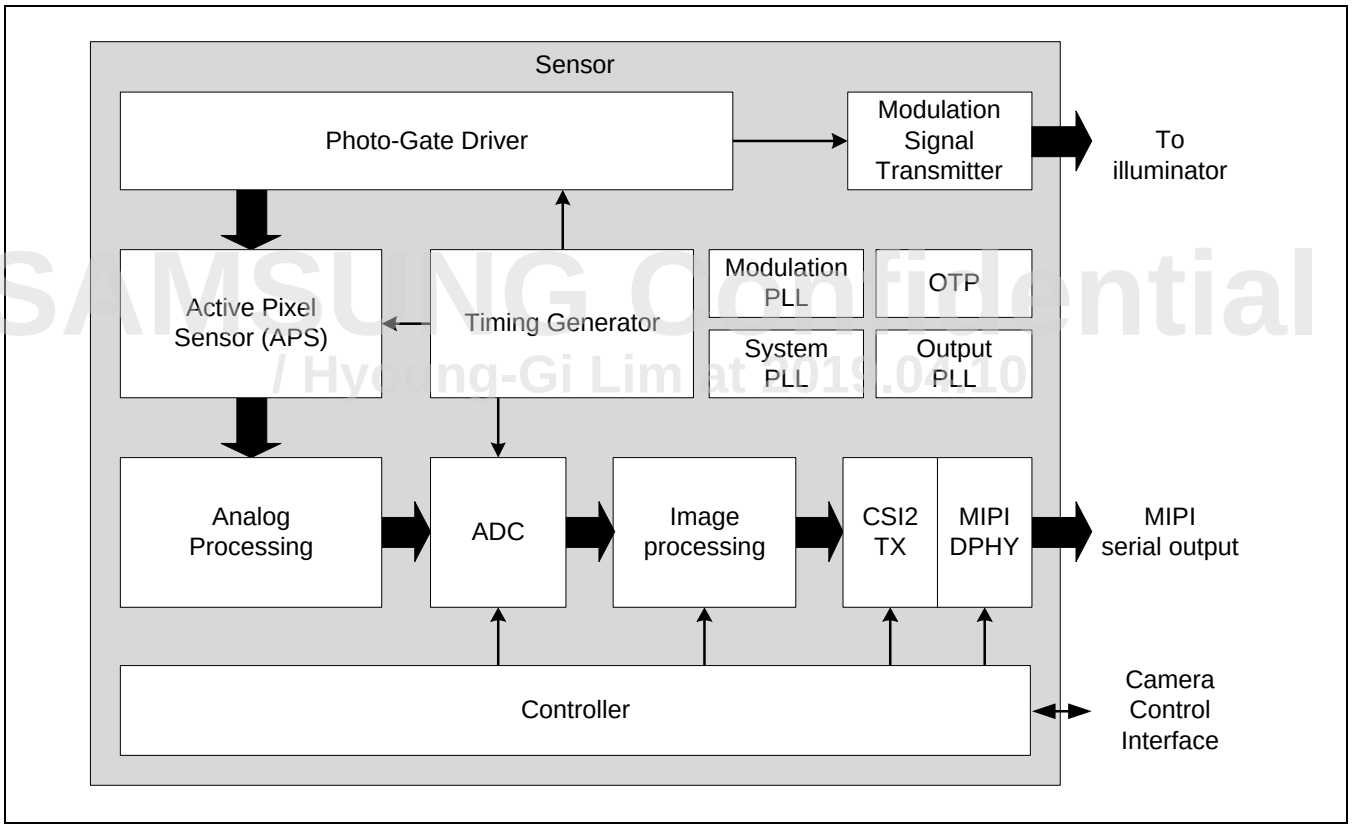


Figure 23 Functional Block Diagram

As an indirect ToF sensor, S5K33DXX has a dedicated modulation PLL and a modulation signal transmitter to control the IR illuminator. The modulation clock is also used in the photo-gate driver to perform demodulation at the pixel array.

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-power analog processing.

The analog output signal of each pixel includes some temporal random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, a Correlated Double Sampling (CDS) circuit is used before converting to digital.

The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain.

The sensor is interfaced using a set of control and status registers that can be used to control many aspects of the sensor behavior, including frame size and exposure setting. These registers can be accessed through a CCI or SPI interface.

5.2 Data Processing Chain

Figure 24 illustrates the whole data processing chain of S5K33DXX. The data processing chain performs row noise reduction, frame black level recovery, and compensation for various analog circuit variations and non-uniform pixel levels. The flexible compensations are configured per readout modes and exposure level, which are performed in the Front-End Image Signal Processor (FEISP).

The data processing chain includes a bad pixels correction option (both static and dynamic) that can perform bad pixels detection and correction on flat surfaces.

S5K33DXX has on-sensor H/W depth calculation chain that can be used in certain readout modes and can be used for low-accuracy depth applications.

In addition, S5K33DXX activates deterministic pattern generator and a MIPI CSI-2 frame formatter with embedded line support.

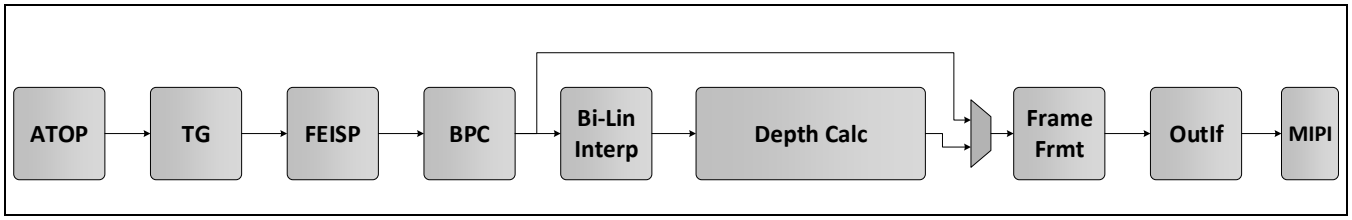


Figure 24 Data Processing Chain

5.3 Sensor output modes

The sensor supports four different output modes such as RAW phase output, depth output, proximity mode, and RAW phase + proximity.

5.3.1 RAW Phase Output

The main application of the sensor is to output RAW phase-sampled data for the back-end depth post processing. In this mode, the output format is similar to the ADC output format; if the sensor is configured to 4-tap phase output, the output mode is the same.

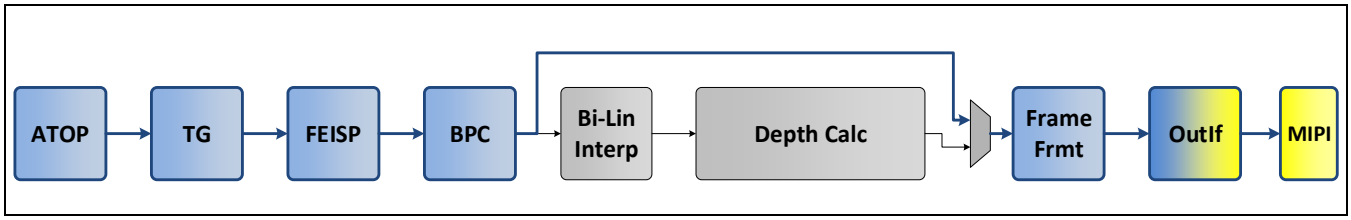


Figure 25 RAW Phase Output Data Path Configuration

In this mode, Bad Pixel Compensation (BPC) can be enabled or disabled. There are no specific constraints on the BPC.

5.3.2 Depth Output

Low-accuracy depth can be calculated and output. In this mode, BPC and dual-frequency must be disabled. Depth output format can be either depth only or depth + confidence (which requires three components of data per pixel such as depth, intensity, and amplitude).

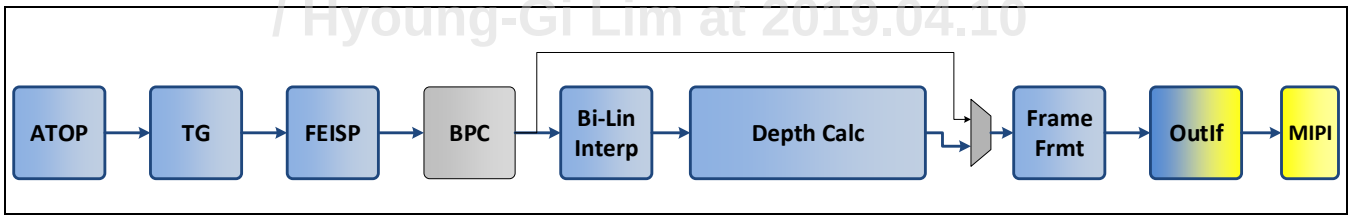
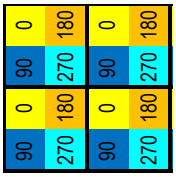
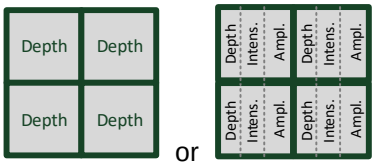


Figure 26 Depth Mode Data Path Configuration

Input Image Type	Output Image Type	Limitations	Notes
Raw phase: 4-tap	Depth or Depth + confidence	BPC is disabled. Phase re-order is required. 1 cycle gap between readout of each pixel in TG. Dual-frequency mode is disabled.	Proximity information can be calculated and read through I2C/SPI or flagged by GPIO.
			

5.3.3 Proximity Mode (No Output)

In proximity mode, output is not required, so MIPI and its preceding blocks can be disabled. Proximity information is either flagged on a GPIO or read externally through IIC/SPI.

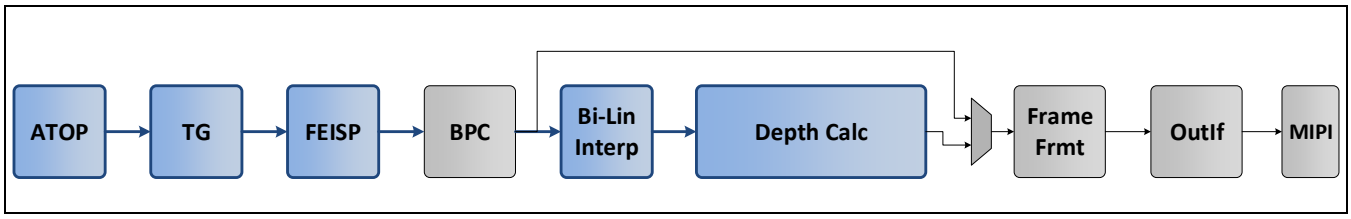


Figure 27 Proximity Mode Data Path Configuration

5.3.4 RAW Phase + Proximity

Proximity calculation can be combined with RAW phase output. In this mode, the AP software calculates the high quality depth and low quality depth is used internally for proximity.

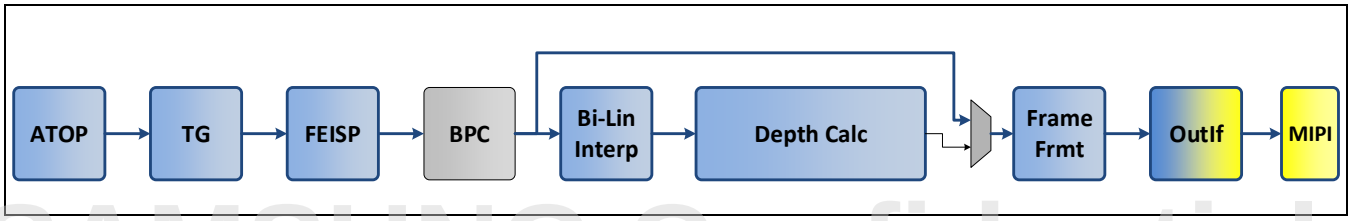


Figure 28 RAW Phase + Proximity Data Path Configuration

5.4 Pixel Array Addresses

Addressable pixel array is defined as the pixel address range to be read. The addressable pixel array is assigned anywhere on the pixel array. x_addr_start, y_addr_start, x_addr_end, y_addr_end, x_output_size, and y_output_size registers control the addressed region of the pixel array.

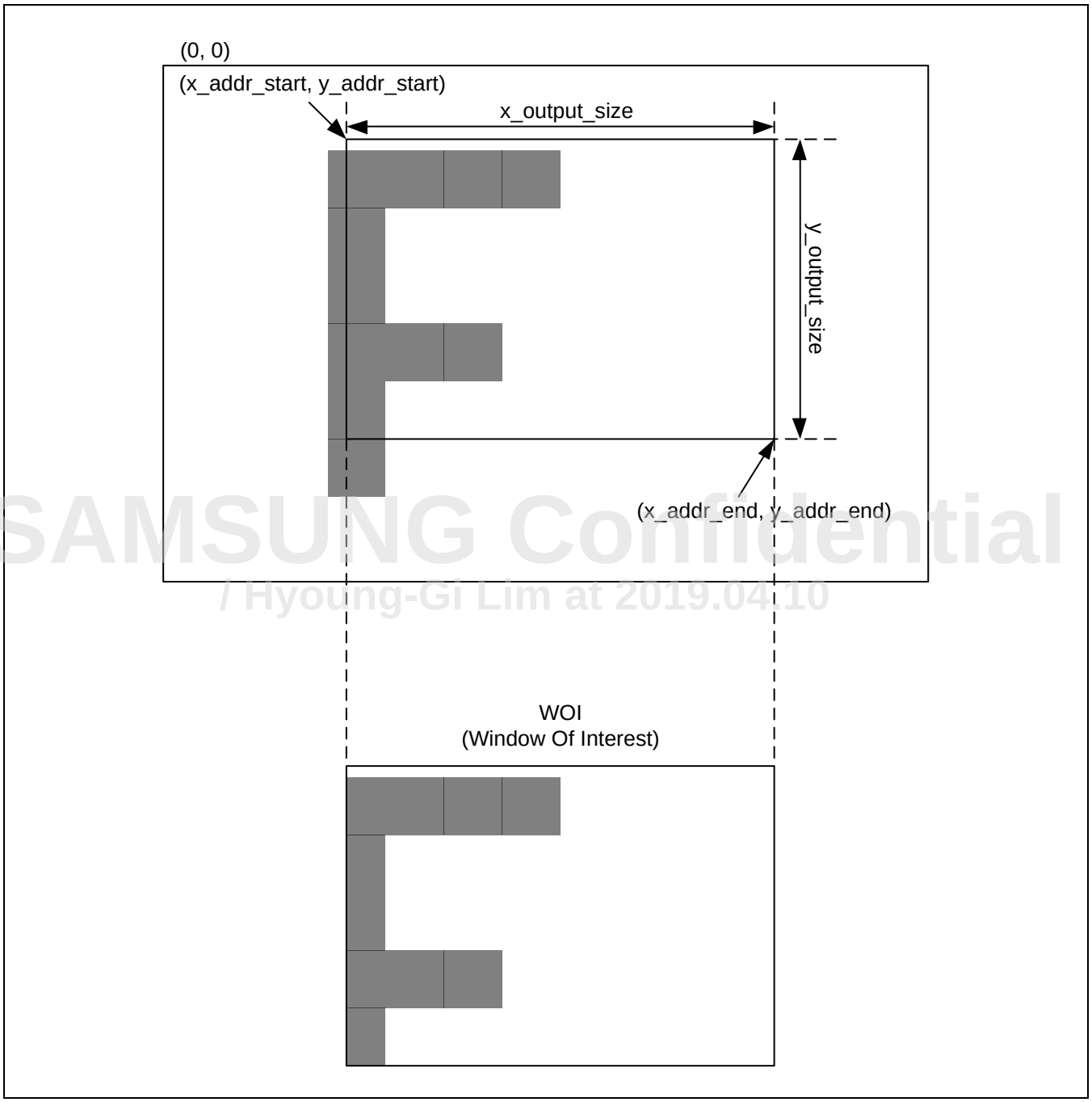


Figure 29 Window of Interest on Pixel Array

5.5 Horizontal Mirror and Vertical Flip

The pixel data is normally read out from left to right in the horizontal direction and from top to bottom in the vertical direction. By changing the mirror/flip mode, the read-out sequence can be reversed, and the resulting image can be flipped like a mirror image. Pixel data is then read out from right to left in horizontal mirror mode and from bottom to top in vertical flip mode. The horizontal mirror and the vertical flip mode can be programmed by the image orientation register.

The sensor module supports the following four possible pixel readout orders:

a) Standard Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_start and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_start and y_output_depth registers.

b) Horizontally Mirrored Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end, and x_output_width registers, and the vertical pixel data output is the same as that of the standard readout.

c) Vertical Flipped Readout
The horizontal pixel data output is same as that of the standard readout, and the addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

d) Horizontally Mirrored and Vertically Flipped Readout
The addressed region of the horizontal pixel data output is controlled by the x_addr_end and x_output_width registers. The addressed region of the vertical pixel data output is controlled by the y_addr_end and y_output_depth registers.

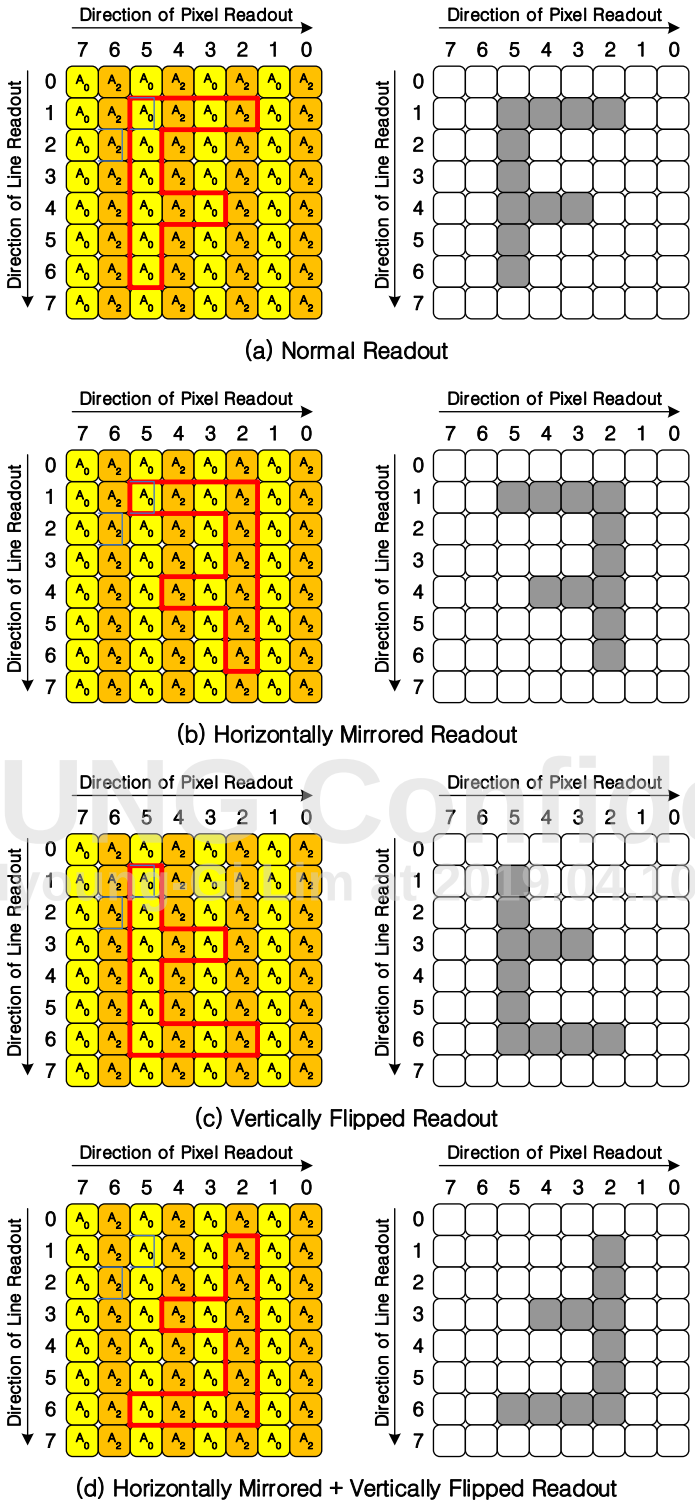


Figure 30 Horizontal Mirror and Vertical Flip at Normal/Binning Output Mode

5.6 Averaged Readout (Binned Readout)

By programming the averaged readout enable register, the sensor is configured to read out pixel data that has been averaged with adjacent pixel of same phase.

5.7 Frame Rate Control

Varying the size of the virtual frame changes the line rate and the frame rate. line_length_pck and frame_length_lines registers control the width and depth of virtual frame, respectively. The horizontal and vertical blanking times (horizontal blanking time: line_length_pck-x_output_size, vertical blanking time: frame_length_lines-y_output_size) should meet the system requirements. Use the following formula to calculate the frame rate.

Frame rate = vt_pix_clk/(frame_length_lines × line_length_pck)

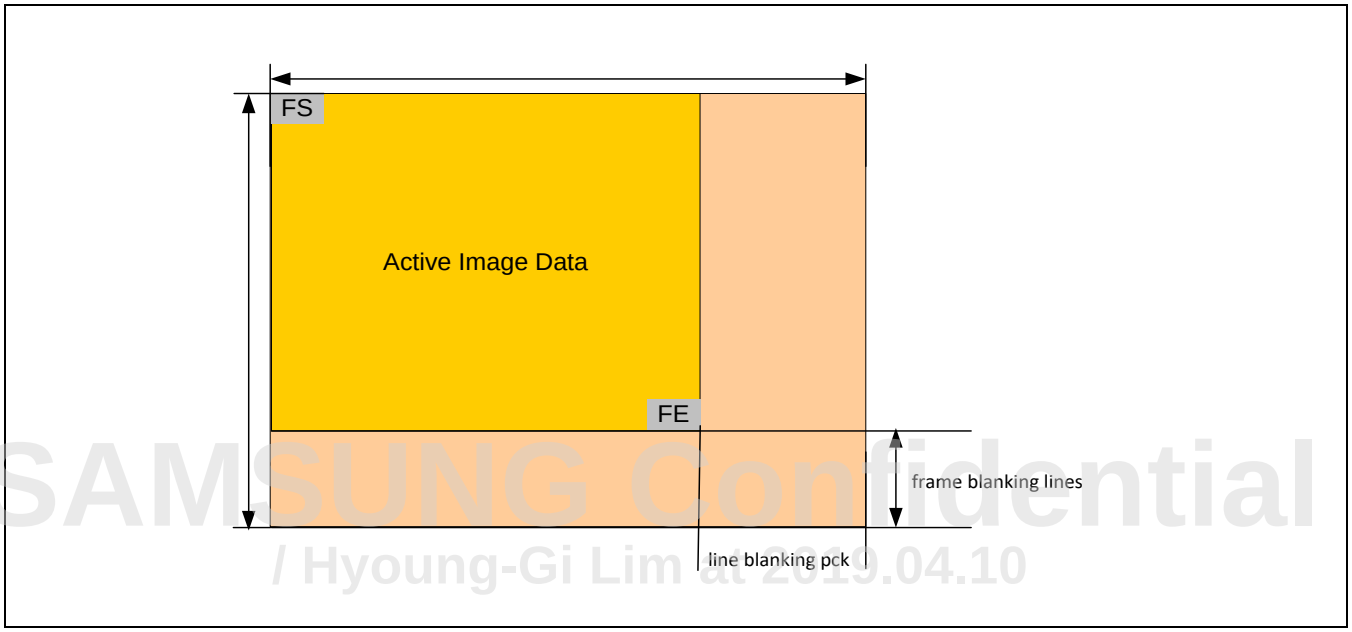


Figure 31 Example of Virtual Frame Format

5.7.1 Integration Time Control (Electronic Shutter Control)

The shutter operation controls the pixel integration time. During the shutter operation, the column step integration time control register (fine_integration_time) and the line step integration time control register (coarse_integration_time) determine the amount of time, integration time. Use the following formula to calculate the total integration time of the sensor module.

Total_integration_time = {coarse_integration_time × line_length_pck + fine_integration_time} × pclk period[sec]

5.7.2 Functional Operation Modes

S5K33DXX supports various operation modes, which are functions of the following mode parameters:

- Interface bandwidth
- H/W limitations: Minimal H/V-blank, delay of the blocks
- Requested sensor output size and sensor operation mode

- CIS output size and number of bits per pixel: RAW12 and RAW10 (through clamping)
- Required vertical blank time
- Pixel array configuration: 4-tap or 2-tap
- Output format: Phase, depth, or depth + confidence

Typical operation modes and related typical settings are described in *Table 13*.

Table 13 Typical Functional Operation Modes

Resolution	Mode	Array Mode	Output Mode	H	V	Frame Rate (fps)
VGA	Full	2-tap	RAW phase	1280	480	120
VGA	Full	4-tap	RAW phase	1280	960	60
QVGA	2x2 binning	2-tap	RAW phase	640	240	180
QVGA	2x2 binning	4-tap	RAW phase	640	480	90
QQVGA	4x4 binning	2-tap	RAW phase	320	240	240
QQVGA	4x4 binning	4-tap	RAW phase	320	120	120
16×16(*)	16x16 crop	4-tap	Proximity (no output)	32	32	10
VGA	Full	4-tap	Depth	640	480	60
VGA	Full	4-tap	Depth + Confidence	1920(**)	480	60

(*): Image size for the proximity mode can be configured to any value less than 32 × 32 resolution.
(**): Depth + Confidence image contains three different attributes per pixel (depth, intensity, and amplitude), thus, image width is 640 × 3 = 1920.

5.8 PLL and Clock Generator

S5K33DXX clock system uses system PLL, system clock dividers, output PLL, output clock dividers, and a modulation PLL to generate all internal clocks from a single master input clock running between 12 MHz and 60 MHz.

The maximum effective VCO frequency of output PLL for MIPI transmission is 1.6 GHz. The dedicated system PLL is used for maximal flexibility in interface frequency and for EMI avoidance. The maximum system PLL VCO frequency is 720 MHz. The modulation PLL allows flexible demodulation of the input modulation signal and for supplying sync signal for the IR illuminator. Modulation frequency can be changed for each frame to support dual-frequency mode. Clock dividers are used to generate all system clocks from a single PLL source.

The charge pump clock and the ADC clock are used for A/D conversion circuits, pixel clock is used for pixel processing and sensor control. Bit clock and output clock are set according to the required output rate.

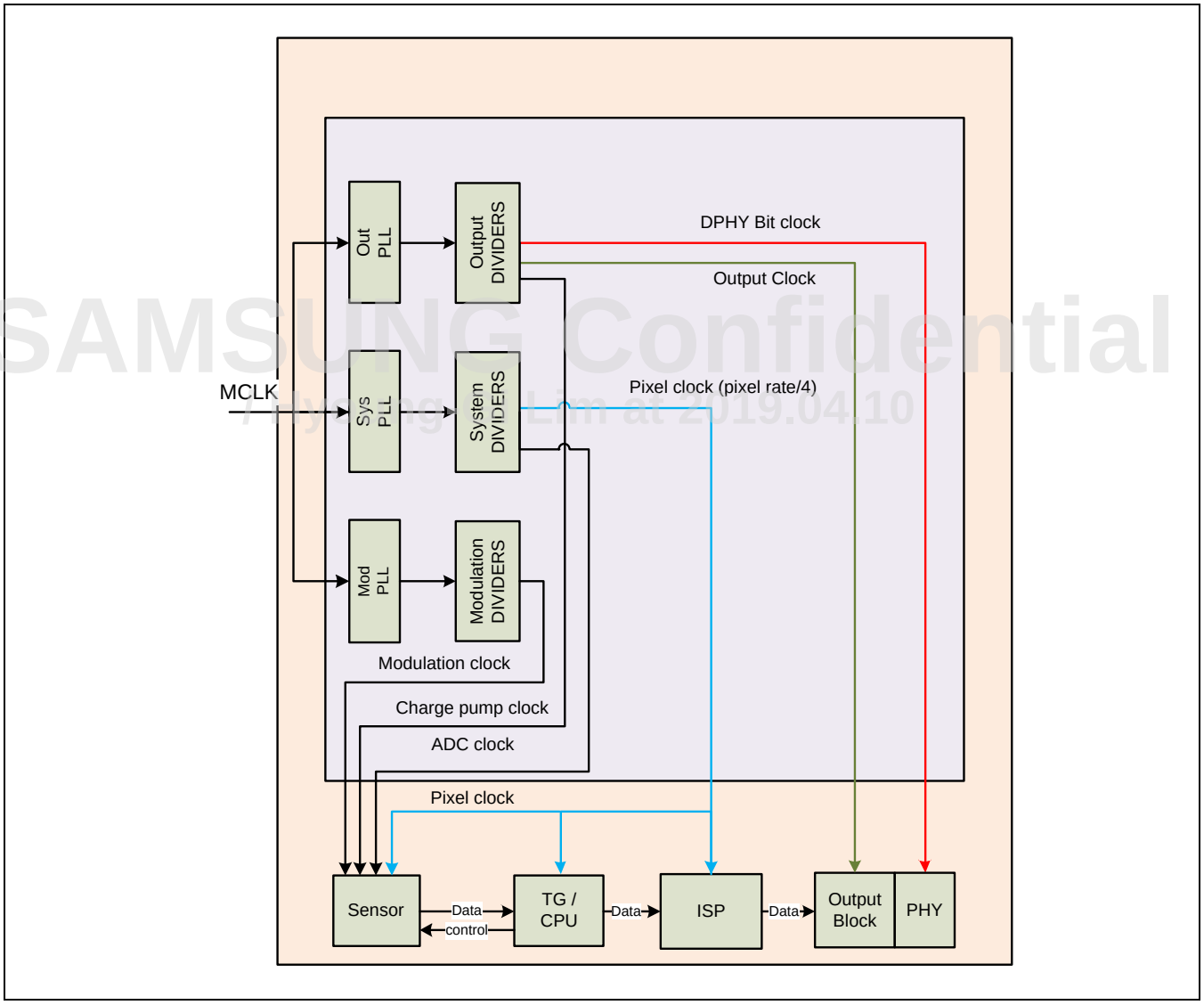


Figure 32 Block Diagram of Clock System

5.8.1 Clock Relationships

The host provides the external input clock (with values varying between 12 and 60 MHz) in addition to setting dividers and multipliers to get the required video timing and output pixel clocks.

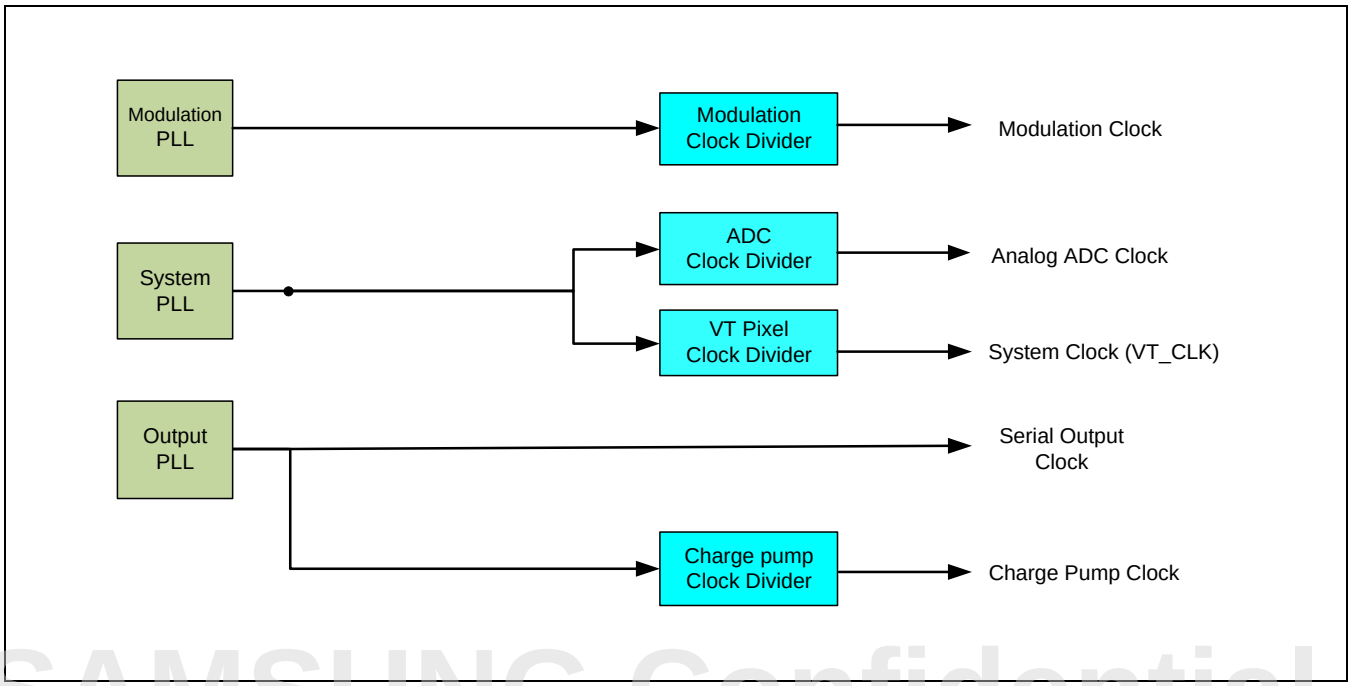


Figure 33 Clock Relationships

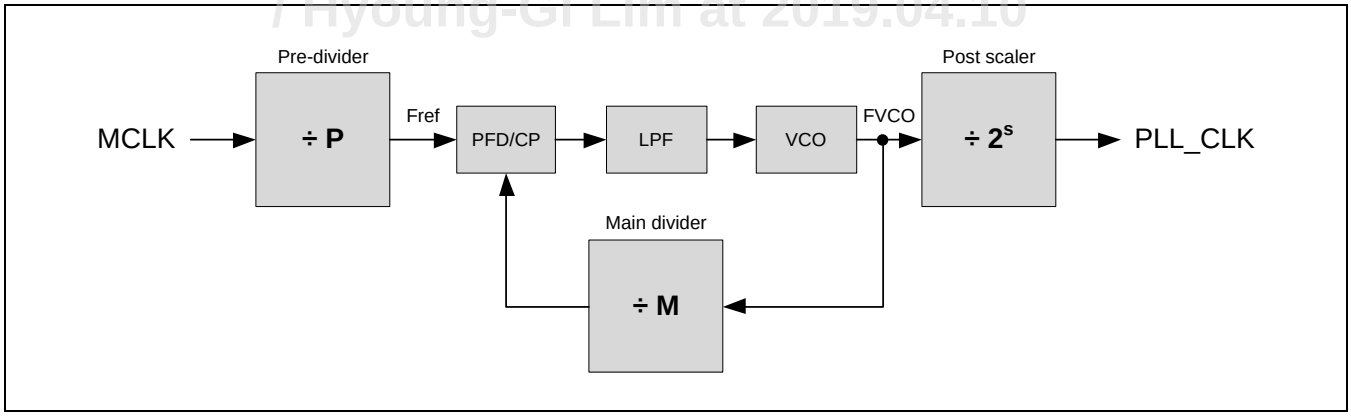


Figure 34 PLL Frequency Synthesis

Use the following formula to calculate PLL_CLK.

$$System\ PLL\_CLK = MCLK \times \frac{M}{P} \times \frac{1}{2^S}$$
$$Output\ PLL\_CLK = MCLK \times \frac{2M}{P} \times \frac{1}{2^S}$$

NOTE: Post scaler (PLL_S) in S5K33DXX is not controllable. Post dividers are used for lower frequency synthesis.

Table 14 PLL Component Output Frequency

Parameter	Min.	Typ.	Max.	Unit	Remarks
Input frequency range	6	–	64	MHz	EXTCLK frequency range
System PLL reference frequency range	6	–	12	MHz	Output of the system PLL pre-divider (Fref)
System PLL VCO frequency range	500	–	1000	MHz	Output of the system PLL multiplier VCO oscillation range (Fvco)
System PLL output frequency range	31.25	–	1000	MHz	Output of the system PLL post scaler. Minimum value is only for testing (4 > S ≥ 1).
Output PLL reference frequency range	6	–	12	MHz	Output of the output PLL pre-divider (Fref)
Output PLL VCO frequency range	1075	–	1600	MHz	Output of the output PLL multiplier VCO oscillation range (Fvco). Effective frequency for MIPI transmission is same as that of VCO.
Output PLL output frequency range	80	–	1600	MHz	Output of the output PLL post scaler. Minimum value is only for test (4 > S ≥ 1). Effective frequency for MIPI transmission is the same as that of VCO.

NOTE: For more information about the PLL and clock system control, refer to S5K33DXX Application Note.

5.8.2 Master Clock Waveform

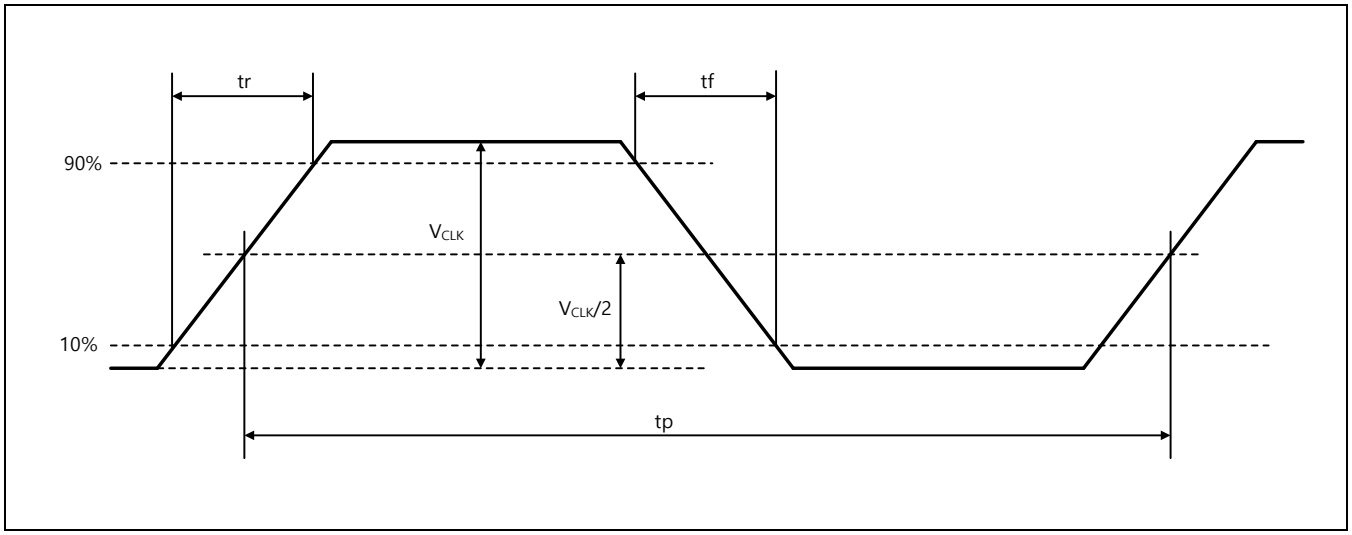


Figure 35 Master Clock Waveform Diagram

MCLK is the input clock to the S5K33DXX sensor, which is sometimes referred to as EXTCLK (external clock).

Table 15 EXTCLK Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
MCLK clock frequency	MCLK	6	–	64	MHz	–
MCLK period	tp	13.89	–	83.33	ns	–
MCLK rise/fall time	tr/tf	–	–	10		–
MCLK period jitter (peak-to-peak)	Tjitter	–	–	400	ps	–

NOTE: For higher I2C/SPI rate such as fast-mode or fast-mode plus, the minimum MCLK frequency of 12 MHz is required.

5.9 IR Illuminator Control

S5K33DXX can drive an IR illuminator through a differential modulation signal generated by an on-chip modulation-signal transmitter. An IR illuminator can be implemented by a Laser Diode (LD) or an LED. One possible candidate of the LDs is a Vertical-Cavity Surface-Emitting Laser (VCSEL).

The modulation-signal transmitter can transmit the IR modulation signal in Low-Voltage Differential Signaling (LVDS) level or full-swing CMOS level for low-frequency driving in low-power. This modulation clock signal is valid during the integration time.

The modulation enable flag signal (active high) can also be generated to wrap the modulation signal for an LD driver IC to inform the modulation period. The modulation flag signal can start earlier than the actual modulation signal to wake up the LD driver IC before the integration time.

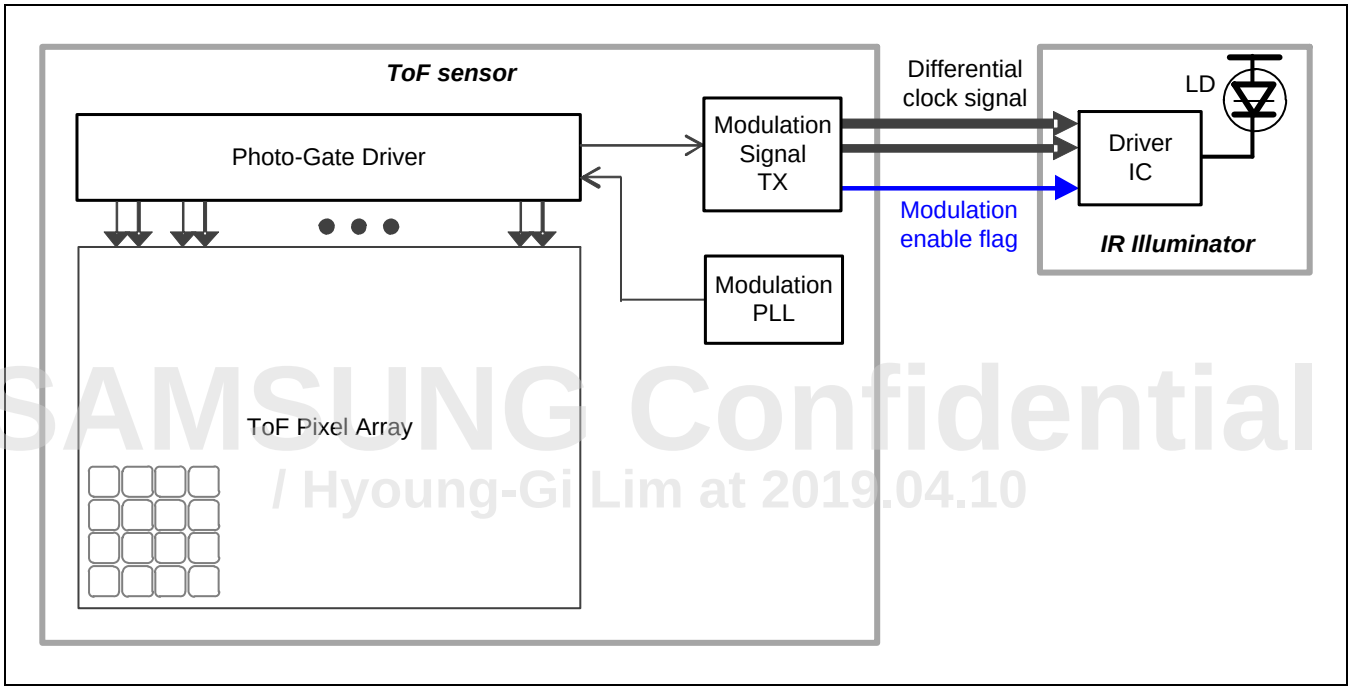


Figure 36 Connection Between the ToF Sensor and IR Illuminator

5.10 Dual Camera Synchronization

Dual sync. is an attribute that enables the sensor to accept the VSync-in from an external source. The purpose of this function is to enable the sensor to synchronize its image data transmission with other sensors. Higher level applications can analyze multiple images from multiple sensors.

Dual sync. operates correctly only if both sensors are configured to work with the same frame rate, and the sensor can properly fix and adjust only minor drifts caused from physical differences between the sensors.

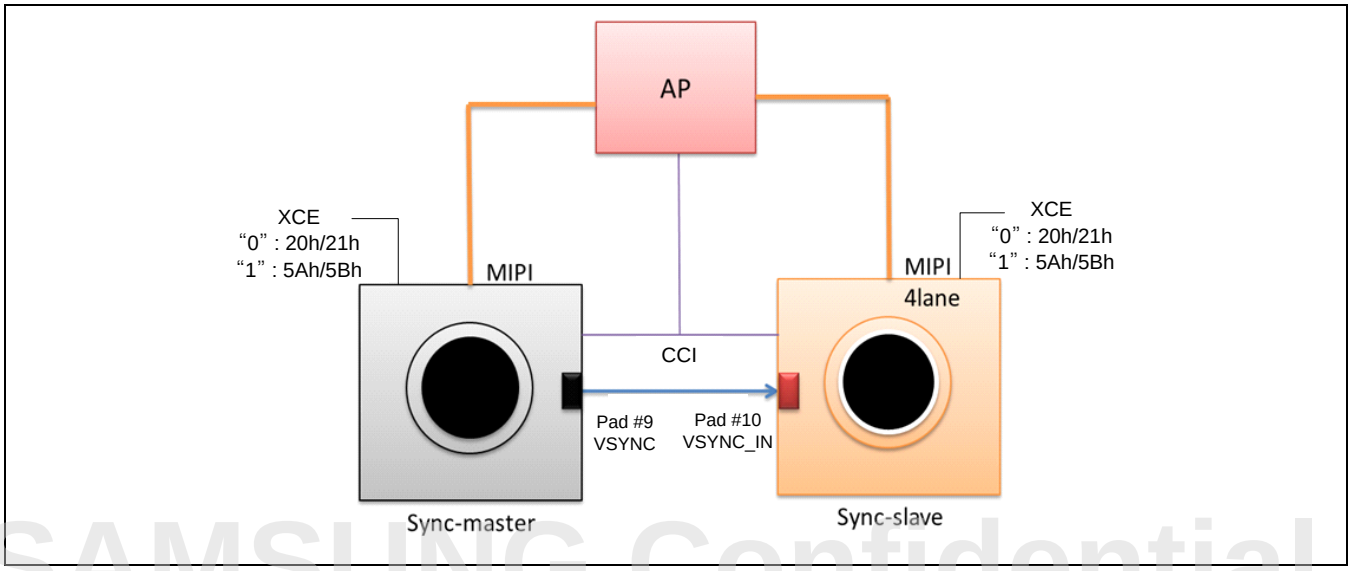


Figure 37 Dual camera system

The dual sync feature monitors two intervals on the slave sensor (that is, the sensor which is in synchronization with the external source such as the master sensor), which defines the line time between the master and slave sensors:

- VSync-in to VSync-in – The time between two consecutive VSync-in received from the master.
- VSync-in to VSync-out – The time between VSync-in received from the master and the internal VSync-out generated by the slave.

Time Interval	Label	Min.	Max.	Units
Dual sync. frames delay	Tframe_dly	1	2	Frames
Vsync (I) to Vsync (O) exposure time < Frame time - 60 H-times	T0	5	-	H-Times
Vsync (I) to Vsync (O) exposure time >= Frame time - 60 H-times		60	-	

Dual sync frames delay in S5K33DXX is one to two frames as illustrated in *Figure 38*.

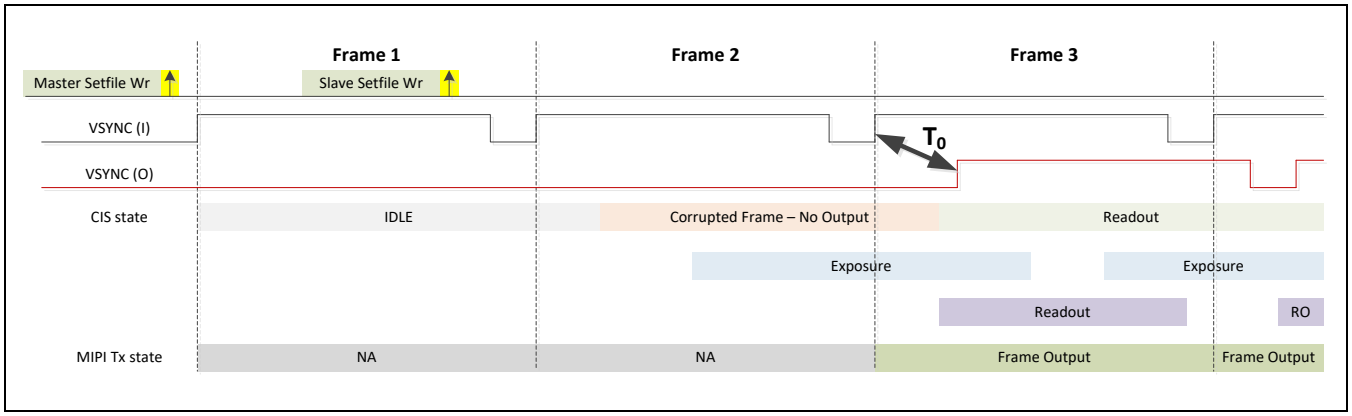


Figure 38 Initialization Sequence of Dual Camera Synchronization

5.11 NVM OTP Memory

The OTP memory module is a non-volatile One-Time Programmable (OTP) memory module. This module enables the saving of unique data to each chip at the production stage.

OTP memory is used to store the following information:

- Chip ID data – Production history data to be stored during die sorting
- Parameter for lens shading
- 9 Kb for users

Following are two different ways to access each OTP memory:

- Externally, using I/O pads by configuring the chip to a dedicated test mode and performing full OTP memory IP write/read protocol.
- Internally, through the internal-bus using the controller.

5.11.1 OTP Read/Write Procedure

For more information, refer to S5K33DXX Application Note.

5.12 Output Data Interface

S5K33DXX MIPI CSI-2 interface is a two-lane high-speed serial interface that connects the camera sensor to a host processor. Maximum bitrate of MIPI of S5K33DXX is 1.6 Gbps per lane.

S5K33DXX supports all mandatory requirements in MIPI CSI-2 version 1.00 and DPHY 1.2 specifications. For more information, refer to MIPI DPHY 1.2 specification.

Following are some supported features and specifications of output data interface:

- Main output frame rates:
  - 4-tap VGA RAW phase: 60 fps
  - 4-tap QVGA RAW phase: 90 fps
  - 4-tap QQVGA RAW phase: 120 fps
  - VGA depth: 60 fps
  - VGA depth + confidence: 60 fps
- MIPI CSI-2: Two lanes with a maximum of 1.6 Gbps (bit clock rate)
- Data types: RAW8, RAW10, and RAW12
- Data output types:
  - Video stream
  - Embedded lines (embedded frame header output)
- Integrated MIPI DPHY
- MIPI transmission only
- Up to two data lanes and one clock lane
- Swap in MIPI data lanes
- Only +/- swap (not support between lanes)
- Ultra Low Power Mode (ULPM)

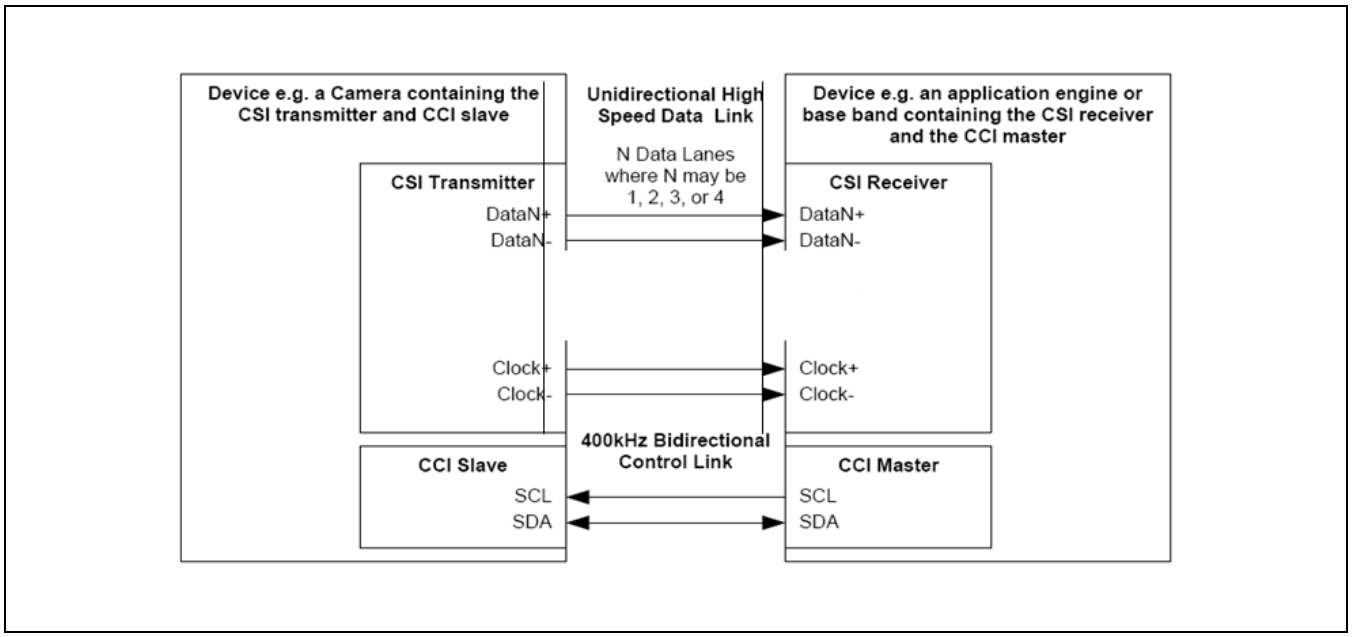


Figure 39 CSI-2 and CCI Transmitter and Receiver Interface

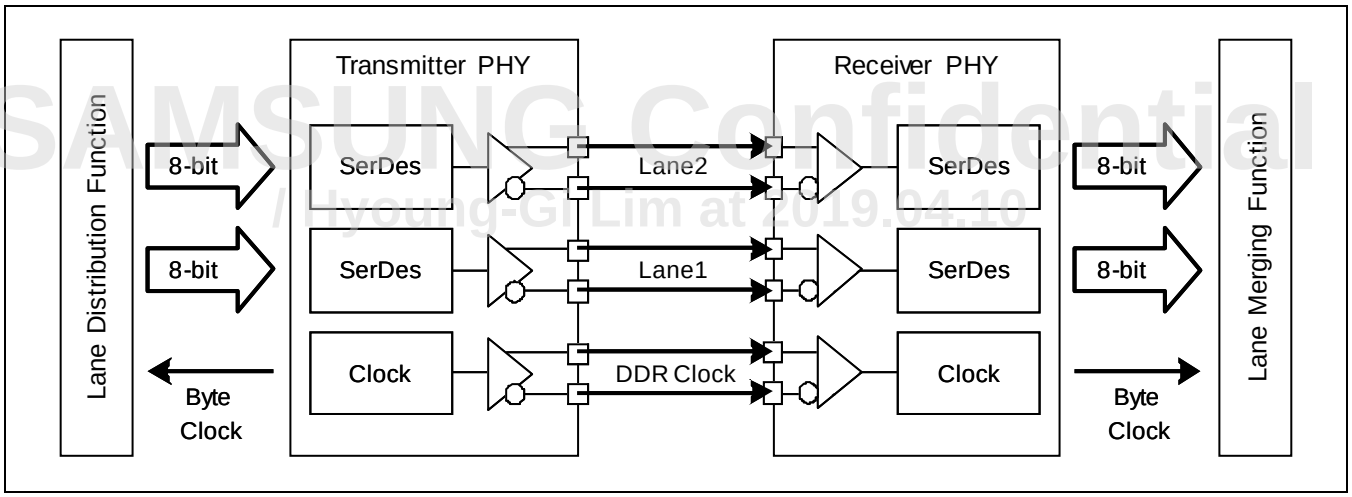


Figure 40 Two-Lane Transmitter and Two-Lane Receiver Example

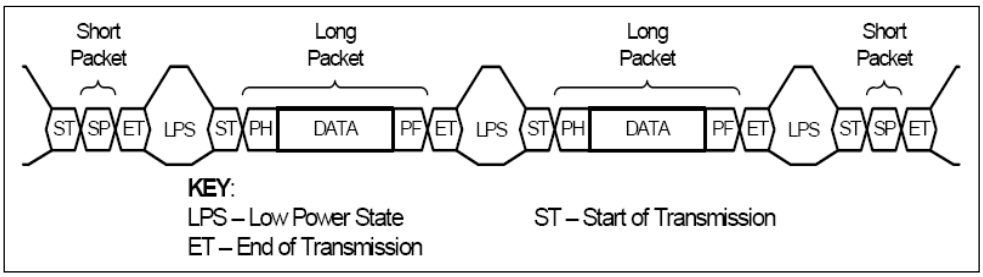


Figure 41 Low-Level Protocol Packet Overview

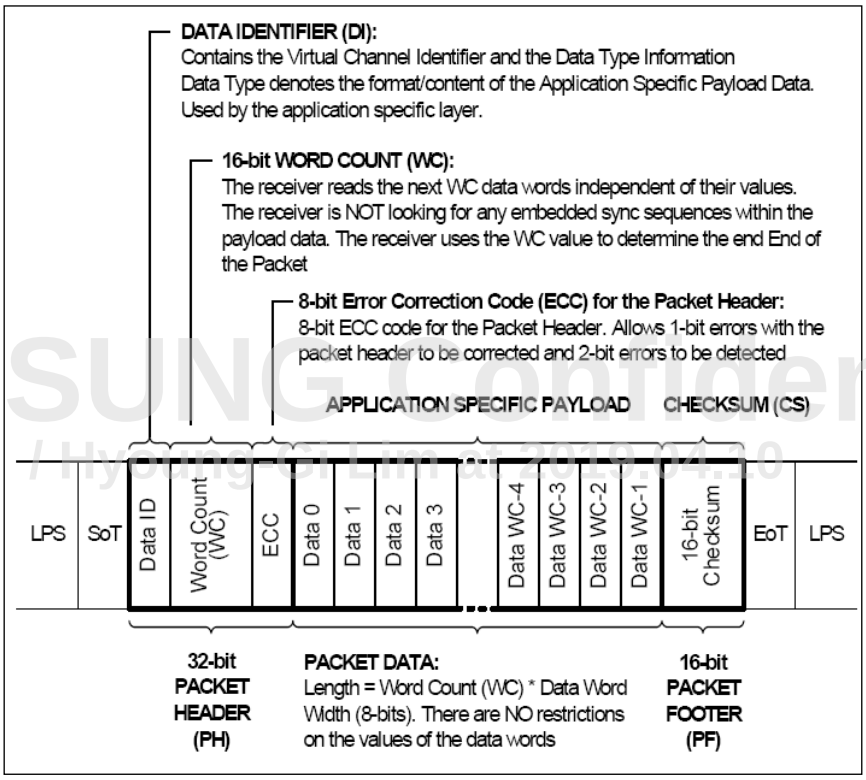


Figure 42 Long Packet Structure

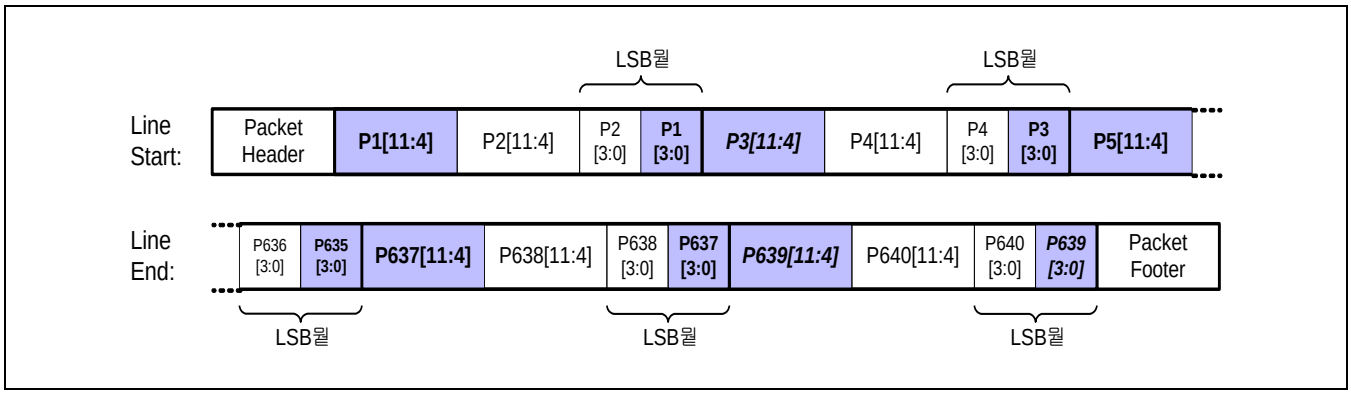


Figure 43 RAW12 Transmission

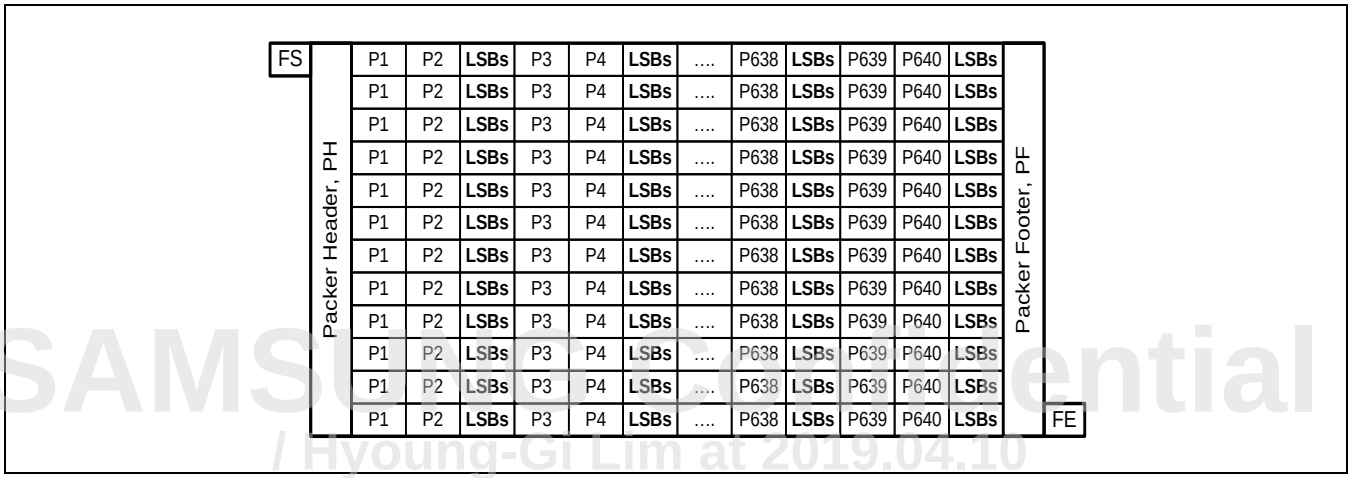


Figure 44 RAW12 Frame Format

5.13 Embedded Line

S5K33DXX can be configured to generate an embedded MIPI header with frame information.

5.14 Test Pattern

S5K33DXX can be configured to generate deterministic test patterns. For more information, refer to S5K33DXX Application Note.

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Table 16 Absolute Maximum Rating

Description	Symbol	Min.	Typ.	Max.	Unit
Digital absolute maximum	VDDD (max.)	–0.5	–	1.5	V
Analog absolute maximum	VDDA (max.)	–0.3	–	3.6	V
I/O absolute maximum	VDDIO (max.)	–0.3	–	3.6	V
PGD absolute maximum	VDDPG (max.)	–0.5	–	1.5	V
Digital input voltages, absolute max. (1)	VIP (max.)	–0.3	–	VDDIO + 0.3	V
VCAP analog voltages, absolute max. (2)	VCAP	-0.3	–	4.2	V
Storage temperature	TSTR	–40	–	85	°C

NOTE:

1. Digital inputs: MCLK, RSTN, I2C_SPI_N_SEL, XCE, SDI, SCK, VSYNC_IN and GPIO_1/2/3
2. Voltage on external capacitors for analog nodes

6.2 Operating Conditions

Table 17 Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit
Digital power supply (1)	VDDD	0.95	1.05	1.15	V
Analog power supply (2)	VDDA	2.7	2.8	2.9	V
I/O supply	VDDIO	1.7 (or 2.7)	1.8 (or 2.8)	1.9 (or 2.9)	V
PGD supply (3)	VDDPG	0.95	1.05	1.15	V
Digital input voltages (4)	VIP	0	–	VDDIO	V
VCAP analog voltage	VCAP	0	–	4.2	V
Test temperature (Ta) (5)	TTEST	21	23	25	°C
Optimum operating temperature (Tj) (6)	TOPT	0	–	60	°C
Normal operating temperature (Tj) (7)	TOPR	–20	–	60	°C
Functional operating temperature (Tj) (8)	TFUNC	–20	–	70	°C

NOTE:

1. Digital supply tolerances: 1.05 V ± 100 mV
2. Analog supply tolerances: 2.8 V ± 100 mV
3. Photo-Gate Driver (PGD) supply tolerance: 1.05 V ± 100 mV
4. Digital inputs: MCLK, RSTN, I2C_SPI_N_SEL, XCE, SDI, SCK, VSYNC_IN and GPIO_1/2/3
5. Test temperature (T_a): Image quality test conditions
6. Optimum operating temperature (Tj): No visible degradation in image quality
7. Normal operating temperature (Tj): Camera produces acceptable images
8. Functional operating temperature (Tj): Camera fully functional

6.3 DC Characteristics

Table 18 DC Characteristics

(VDDA = 2.7 V to 2.9 V, VIP = 1.8 V ± 0.1 V or 2.8 V ± 0.1 V, T_j = – 30 to + 70°C, CLOAD = 20 pF)

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	VIH	–	0.7 × VIP	–	VIP + 0.3	V
	VIL	–	–0.3	–	0.3 × VIP	
Input leakage current	IIL	VIN = VIP or VSS	–10	–	10	μA
High-level output voltage	VOH	IOH = –100 μA	VDDIO – 0.2	–	–	V
Low-level output voltage	VOL	IOL = 100 μA	–	–	0.2	
High-Z output leakage current	IOZ	VOUT = VSS or VDDD	–10	–	10	μA
Input capacitance	CIN	–	–	–	5	pF
Supply current	IHWSBA (1)	Hardware standby mode, analog	–	TBD	TBD	μA
	IHWSBD (1)	Hardware standby mode, digital	–	TBD	TBD	
	ISTRMA (2)	Streaming mode, analog, 4-tap @ 60 fps	–	TBD	TBD	mA
	ISTRMD (2)	Streaming mode, digital, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMIO (2)	Streaming mode, I/O, 4-tap @ 60 fps	–	TBD	TBD	
	ISTRMP (2)	Streaming mode, PGD, 4-tap @ 60 fps	–	TBD	TBD	

NOTE:

1. Digital IHWSBD - Digital and analog power off is required.
2. Conditions: VDDA = 2.8 V, VDDD = 1.05 V, VDDIO = 1.8 V, VDDPG = 1.05 V and T_j = 60°C

6.4 AC Characteristics

Table 19 AC Characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
External clock frequency (1)	fXCLK	–	6	–	64	MHz
External clock duty cycle (1)	fXDUTY	–	45	–	55	%
PLL locking time	tLOCK	–	--	–	500	µs

NOTE: Applied to the MCLK pin

1. A fast-mode I2C-bus can be used with the external clock that exceeds 12 MHz.

7 Lens Specification

7.1 Target Chief Ray Angle (CRA)

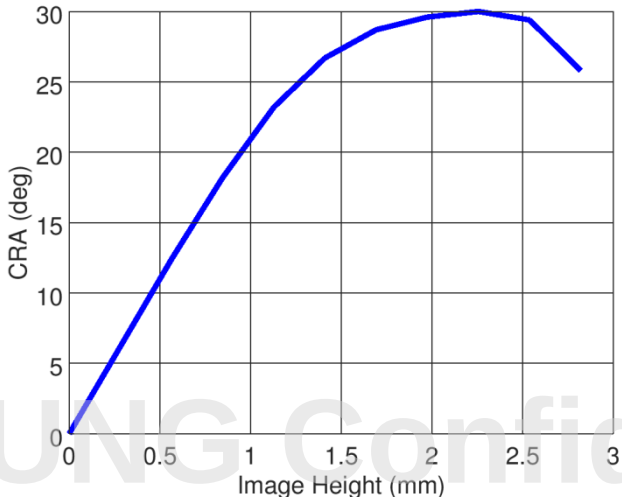


Figure 45 Target CRA

Table 20 CRA with Image Height (Field)

Field	Image Height (mm)	CRA (deg.)
0.0	0.000	0.0
0.1	0.282	6.2
0.2	0.564	12.4
0.3	0.846	18.2
0.4	1.128	23.2
0.5	1.410	26.7
0.6	1.692	28.7
0.7	1.974	29.6
0.8	2.256	30.0
0.9	2.538	29.4
1.0	2.820	25.8

7.2 Pixel-Shading Characteristics

Figure 46 illustrates shading characteristics over difference between target CRA and actual CRA of given lens.

TBD

Figure 46 Shading Characteristics

7.3 Spectral Response

TBD

Figure 47 Spectral Response

Table 21 Spectral Response

Wavelength (nm)	Magnitude
TBD	TBD

7.4 IR Band-Pass Filter Selection

Figure 48 illustrates IR response of the Band-Pass Filter (BPF). The performance of IR BPF is critical for depth quality under the ambient light condition (outdoor use).

TBD

Figure 48 IR Response of the Band-Pass Filter

8 Register Description

TBD