Steven Mills

**6449 S Liveoak Pl Boise, ID 83716**

[**steve1138@hotmail.com**](mailto:steve1138@hotmail.com)

**(503) 734-9978**

Experienced Semiconductor and Systems Test Engineer

**Strengths**

Versatile Skillset, Programming, Hardware Design, Test/Product Engineering, New Product Development, Verification, Validation, Debugging, Data Analysis and High Volume Manufacturing Test.

**Experience**

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| **2015-present** | **Micron Technology, Inc.** | **Boise, ID** |

***Senior Specialty DRAM Test Engineer***

* Verilog vector generation for HMC/MCDRAM products
* SH1/SM3 Python development
* Verilog logic cosim
* HMC3 DRAM APG pattern development/simulation

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| **2013-2015** | **NXP Semiconductors** | **Tempe, AZ** |

***Test Engineer Principal / Verification Engineer***

Mixed Signal Test on Advantest 93k

* Test development for USB PD/BC1.2 and USB TypeC interface devices
* Advantest PS1600 development
* Design of high voltage (30V) ATE module
* C++ Testmethod development
* I2C pattern scripting in Python

Design Verification

* Write directed ATE tests
* Develop UVM Components for I2C, SPI
* ATE vector playback

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| **2010-2013** | **Cypress Semiconductor** | **San Jose, CA** |

***Test Engineer Principal***

High Speed Memory Test, 500-2000 MHz, QDR-II+, QDR-IV

* Verigy 93k Pinscale 3600, Pinscale 9G, HSM6800
* Advantest T5581, T5592, T5593, T5501
* Verilog test bench development
* Bench Characterization
* C, Perl, Python, JMP, R

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| **2009-2010** | **Tabula** | **Santa Clara, CA** |

***Senior Staff Engineer***

Developed Infrastructure for testing and validation of a novel FPGA device using bench characterization boards, Verilog, and Verigy 93000

* RTL coding of DFT circuits
* wrote software tools for GPIO configuration, characterization, DC - 1.2 Gbps
* virtual testing with logic vectors
* parallel characterization of 1000 pin device on 93000 tester
* Bench Testing using JTAG, GPIB, Tcl

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| **2008 – 2009** | **Integrated Device Technology** | **San Jose, CA** |

***Senior Test Engineer***

Developed Verigy 93000 Tools for TCAM and Algorithmic Search Accelerators and Cisco T4 Semiconductor Devices

* Developed Virtual Test solution for 93000 logic vectors and APG Memory Test vectors using C++, perl, Verilog. Allowed for concurrent design and test development
* Developed Source Synchronous Data Acquisition and Analysis software. C++ based data acquisition, and post-processing to reconstruct digital/analog waveforms
* Developed Error Map Reconstruction Memory Raster solution. C++ solution for creating physical bitmaps of TCAMs for Failure Analysis

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| **2006-2007** | **Verigy** | **Portland, OR** |

***Senior Applications Engineer***

Professional in Residence at Intel, Jones Farm Microprocessor Development Group

* Developed Automated Design Validation solution for Intel QuickPath 6.4 GTS and 800 MHz DDR3 interfaces using Verigy 93000 HXA hardware in multi-clock domain
* Jitter Toolbox, Eye Diagrams, Tester Training, PLL keep alive
* C++ Test Method Library development
* Perl automation
* Instructed Intel PDE, Technical Management with all facets of Verigy 93000 Systems application
* GPIB programming. (Delta Design ETC)
* Verigy R&D/Customer liaison

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| **2005-2006** | **Intel** | **Aloha, OR** |

***Product Development Engineer***

AFO Sort Engineer.

* High Volume Microprocessor Wafer Sort
* Developed Sort programs for Merom Dual Core microprocessor
* Schlumberger DeFT/S9k development
* Inline fuse programming of microprocessors
* New Product Debug and Ramp to HVM

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| **1997-2005** | **Integrated Device Technology** | **Salinas, CA** |

***Test Engineering Manager***

Developed Characterization and Production Test programs for SRAM and TCAM semiconductor memories, Redundancy Analysis and Repair

* Managed IPC Test Engineering group
* Test Engineering lead of TCAM/NSE Products
* Developed novel application of Verigy 93000 Software APG to test, bitmap, and repair TCAM memories in production test
* Wafer Sort program development
* High Volume Manufacturing Test
* Characterization/Debug
* SRAM test development engineering using Teradyne J994 memory tester
* Custom Test Template development for Teradyne J994

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| **1994-1997** | **Bently Nevada** | **Minden, NV** |

***Test Engineer***

Designed Test hardware and software for Rotating Machine Instruments.

* Developed i386/DOS based automated test equipment
* Designed automated load current tester for Switching Power Supply
* 68HC11, CPU16/32 assembly programming for embedded systems test
* Circuit board design in PCAD
* Test fixture design in AutoCAD
* GPIB programming

**Education**

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| **1994** | **California State University** | **Chico, CA** |

***BSEE***

**References**

References are available on request.