Lecture 14 – Return-oriented programming

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Based on slides by Bailey, Brumley, and Miller

ROP Overview

- Idea: We forge shellcode out of existing application logic gadgets
- Requirements:
 vulnerability + gadgets + some unrandomized code
- History:
 - No code randomized: Code injection
 - DEP enabled by default: ROP attacks using libc gadgets published 2007
 - ROP assemblers, compilers, shellcode generators
 - ASLR library load points: ROP attacks use .text segment gadgets
 - Today: all major OSes/compilers support position-independent executables



ROP Programming

- 1. Disassemble code (library or program)
- 2. Identify *useful* code sequences (usually ending in ret)
- 3. Assemble the useful sequences into reusable gadgets*
- 4. Assemble gadgets into desired shellcode

^{*} Forming gadgets is mostly useful when constructing complicated return-oriented shellcode by hand

A note on terminology

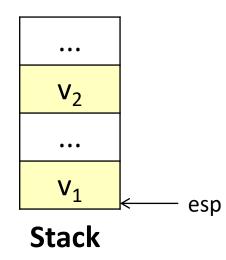
- When ROP was invented in 2007
 - Sequences of code ending in ret were the basic building blocks
 - Multiple sequences and data are assembled into reusable gadgets
- Subsequently
 - A gadget came to refer to any sequence of code ending in a ret
- In 2010
 - ROP without returns (e.g., code sequences ending in call or jmp)

There are many semantically equivalent ways to achieve the same net shellcode effect

Equivalence

Mem[v2] = v1

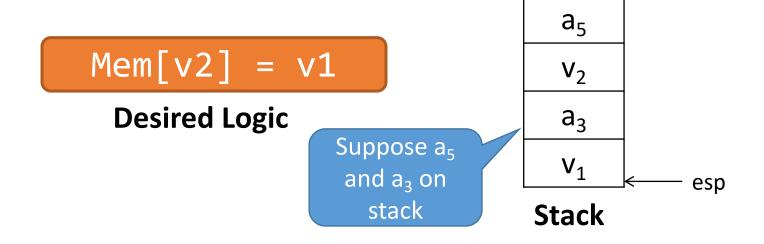
Desired Logic



```
a_1: mov eax, [esp]
```

 a_2 : mov ebx, [esp+8]

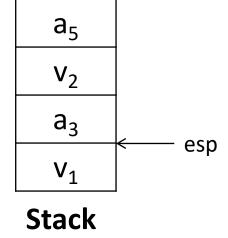
 a_3 : mov [ebx], eax



eax	V_1
ebx	
eip	a_1

Mem[v2] = v1

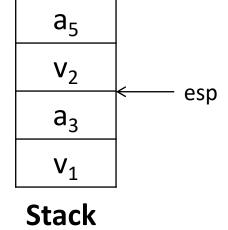
Desired Logic



eax	V ₁
ebx	
eip	a ₃

Mem[v2] = v1

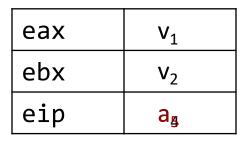
Desired Logic

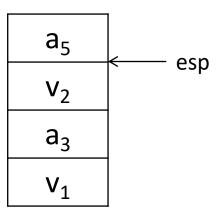


eax	V_1
ebx	V_2
eip	a ₃

Mem[v2] = v1

Desired Logic

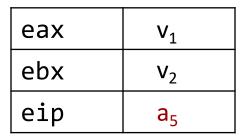


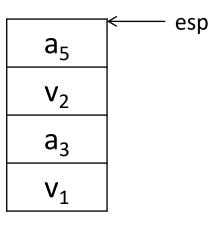


Stack

Mem[v2] = v1

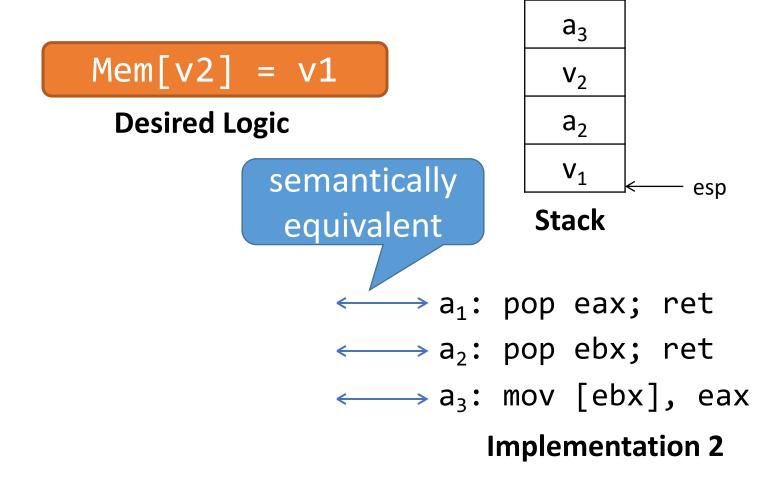
Desired Logic





Stack

Equivalence

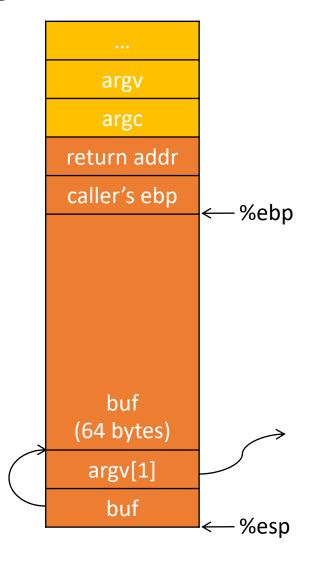


Return-Oriented Programming

Mem[v2] = v1

Desired Shellcode

- Find needed instruction gadgets at addresses a₁, a₂, and a₃ in existing code
- Overwrite stack to execute a₁,
 a₂, and then a₃



Return-Oriented Programming

Mem[v2] = v1

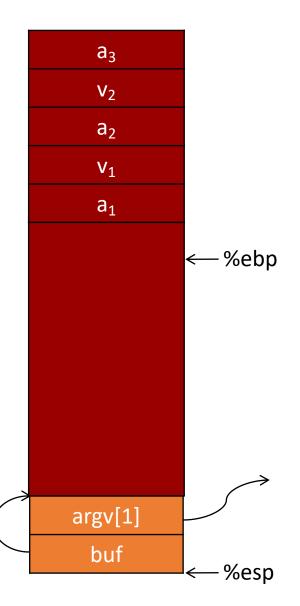
Desired Shellcode

a₁: pop eax; ret

a₂: pop ebx; ret

 a_3 : mov [ebx], eax

Desired store executed!



Arithmetic/logical operations: c = x op y

Basic strategy

- 1. Pop the address of one variable into a register
- 2. Load the value of the variable into a register
- 3. Pop the address of another variable into a register
- 4. Load the value of the variable into a register
- 5. Perform the operation
- 6. Pop the address of the destination variable into a register
- 7. Store the result of the operation at that address

Must be mindful of register interactions

• Addition: c = x + y

• popl %eax ret

• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

addl %eax, %ebx ret

movl %ebx, (%eax)
 ret

Stack contains

- Addresses of code snippets ending in ret
- Data (here, the addresses of our variables)

esp

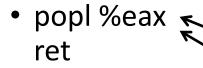
&c

&x

&у

Register	Value
eax	105
ebx	3852

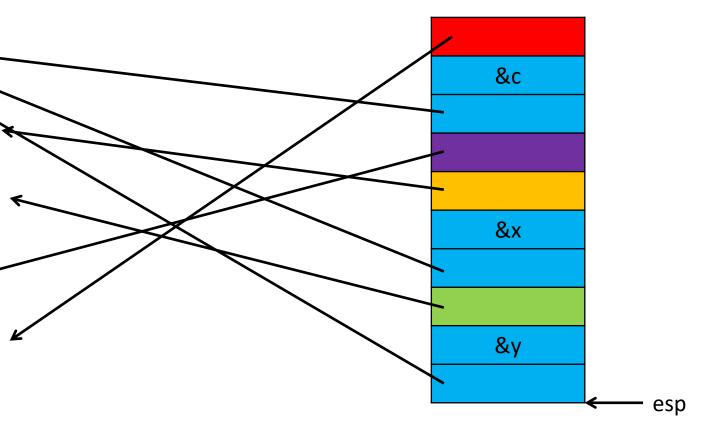




• movl (%eax), %eax ret

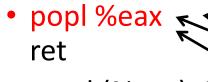
movl (%eax), %ebx ▼
 ret

addl %eax, %ebx ret



Register	Value
eax	105
ebx	3852

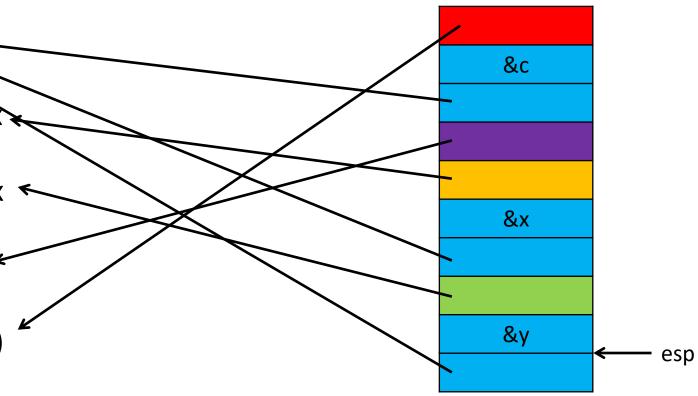
• Addition: c = x + y



• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	&y
ebx	3852

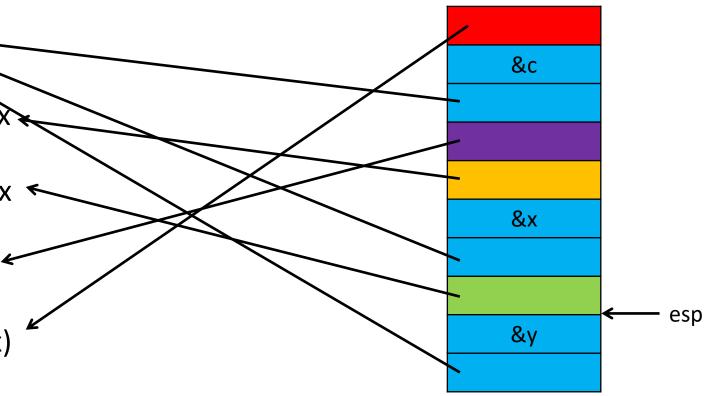
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	&y
ebx	3852

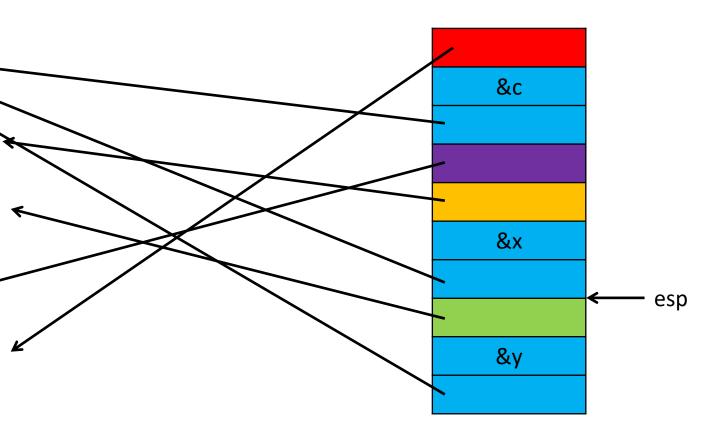
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	&y
ebx	У

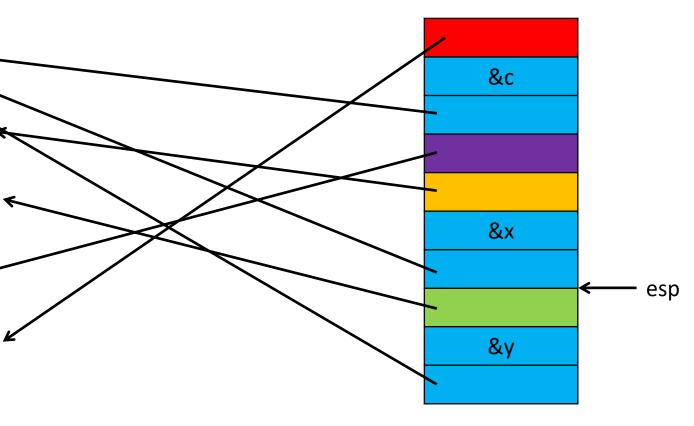
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

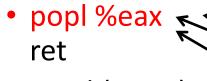
movl (%eax), %ebx ret

• addl %eax, %ebx ret



Register	Value
eax	&y
ebx	У

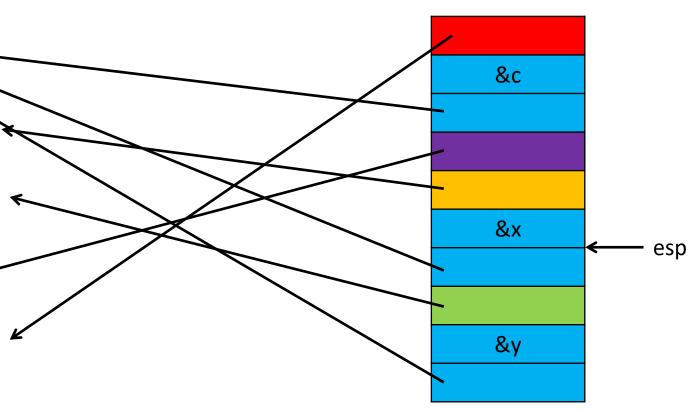
• Addition: c = x + y



• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	&x
ebx	У

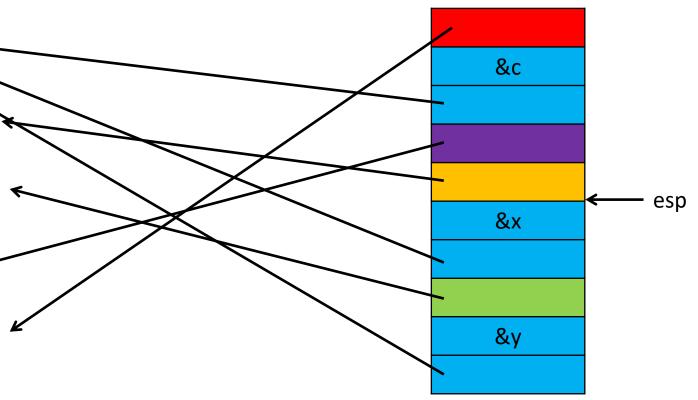
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

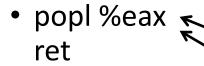
movl (%eax), %ebx ▼
 ret

addl %eax, %ebx ret



Register	Value
eax	&x
ebx	У

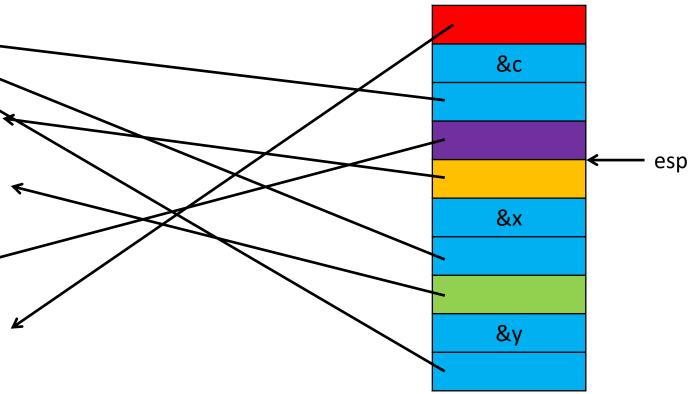




movl (%eax), %eax
 ret

movl (%eax), %ebx
 ret

addl %eax, %ebx ret



Register	Value
eax	X
ebx	У

• Addition: c = x + y

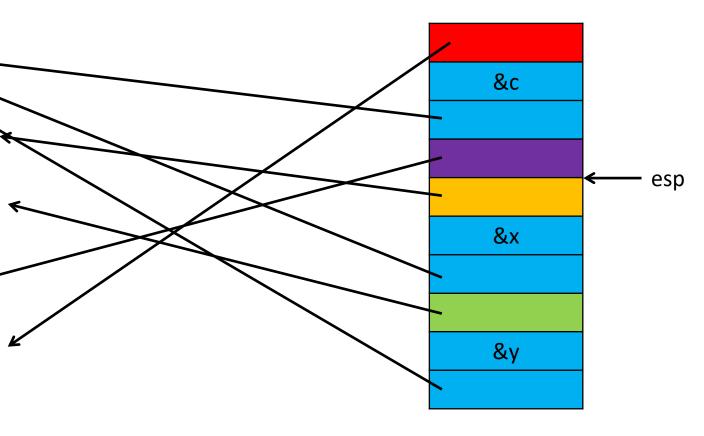
popl %eax ret

movl (%eax), %eax

ret

movl (%eax), %ebx ▼
 ret

• addl %eax, %ebx ret



Register	Value
eax	x
ebx	У

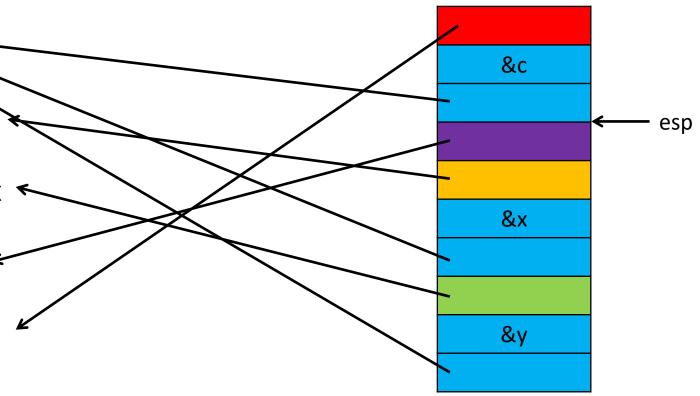
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	x
ebx	y + x

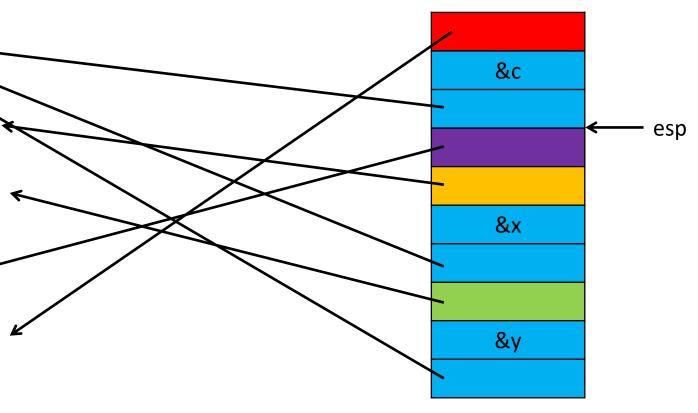
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

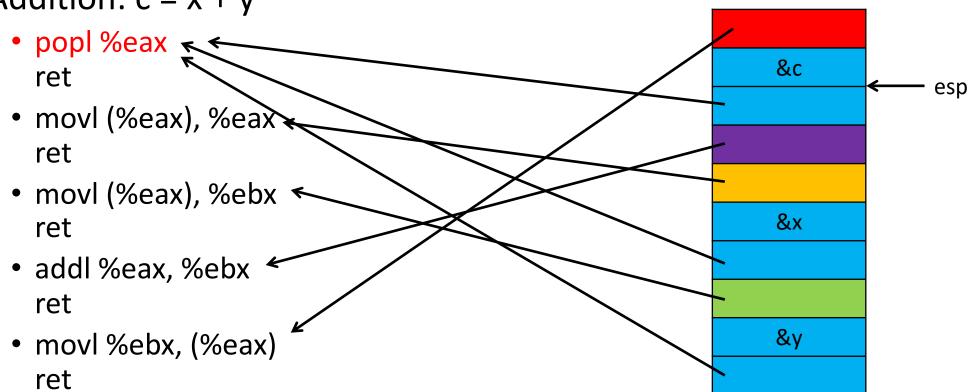
movl (%eax), %ebx
 ret

addl %eax, %ebx ret



Register	Value
eax	x
ebx	y + x

• Addition: c = x + y



Register	Value
eax	&c
ebx	y + x

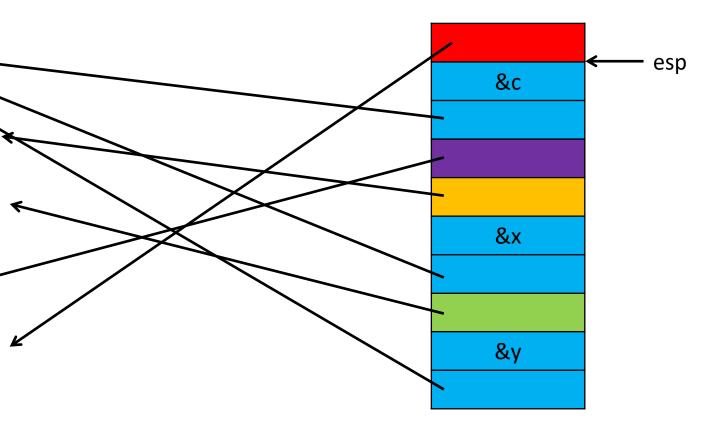


popl %eax ret

• movl (%eax), %eax ret

movl (%eax), %ebx ▼
 ret

• addl %eax, %ebx ret



Register	Value
eax	&c
ebx	y + x

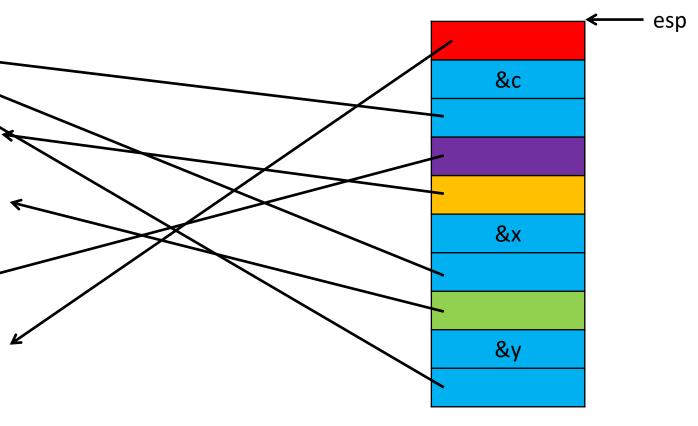
• Addition: c = x + y

popl %eax ret

• movl (%eax), %eax ret

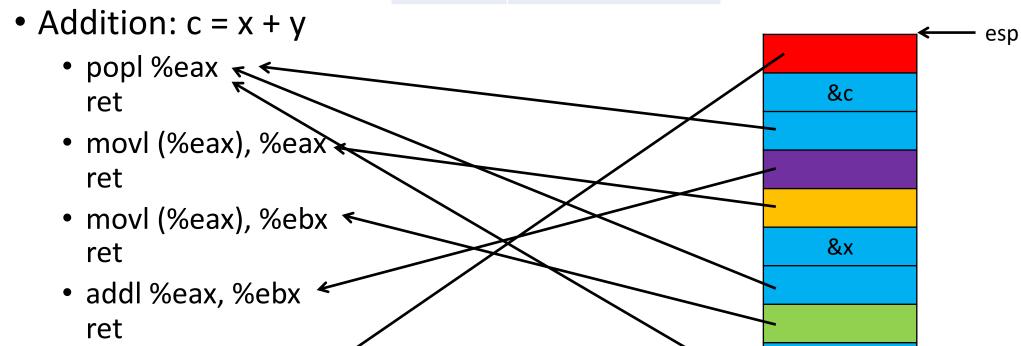
movl (%eax), %ebx
 ret

• addl %eax, %ebx ret



Register	Value
eax	&c
ebx	y + x

&у



What else can we do?

- Depends on the code we have access to
- Usually: Arbitrary Turing-complete behavior
 - Arithmetic
 - Logic
 - Conditionals and loops
 - Subroutines
 - Calling existing functions
 - System calls
- Sometimes: More limited behavior
 - Often enough for straight-line code and system calls

Comparing ROP to normal programming

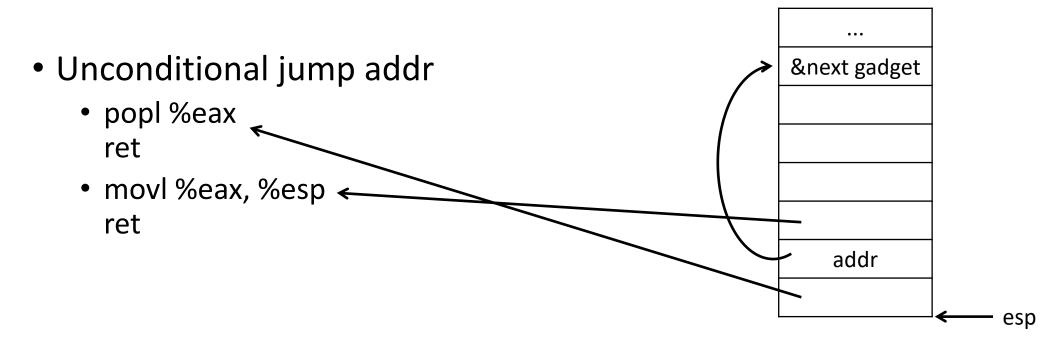
	Normal programming	ROP
Instruction pointer	eip	esp
No-op	nop	ret
Unconditional jump	jmp address	set esp to address of gadget
Conditional jump	jnz address	set esp to address of gadget if some condition is met
Variables	memory and registers	mostly memory
Inter-instruction (inter-gadget) register and memory interaction	minimal, mostly explicit; e.g., adding two registers only affects the destination register	can be complex; e.g., adding two registers may involve modifying many registers which impacts other gadgets

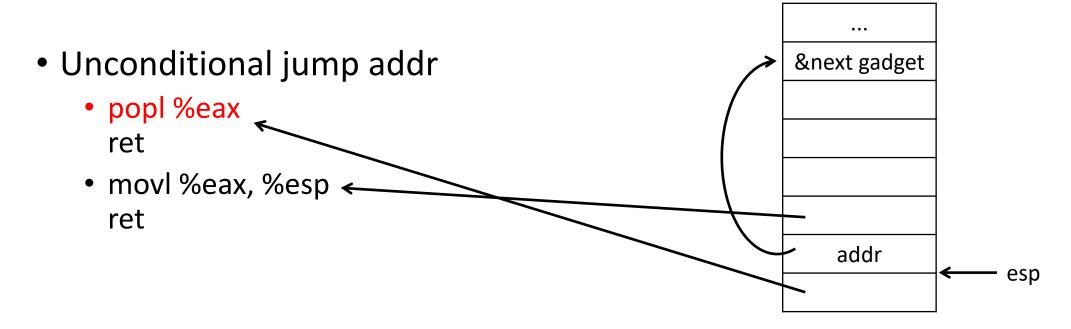
Return-oriented conditionals

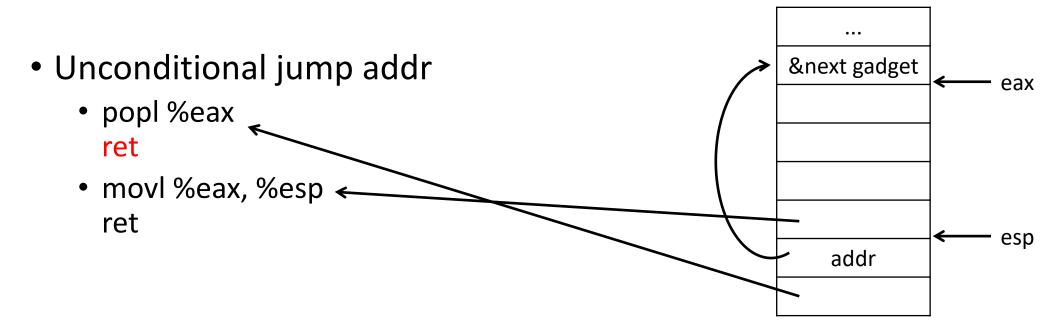
- Processors support instructions that conditionally change the PC
 - On x86
 - Jcc family: jz, jnz, jl, jle, etc. 33 in total
 - loop, loope, loopne
 - Based on condition codes mostly; and on ecx for some
 - On MIPS
 - beq, bne, blez, etc.
 - Based on comparison of registers
- Processors generally don't support for conditionally changing the stack pointer (with some exceptions)

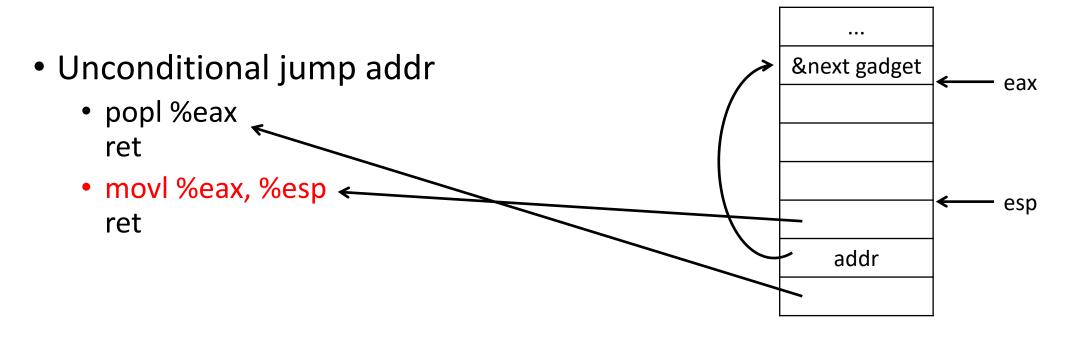
We want conditional jumps

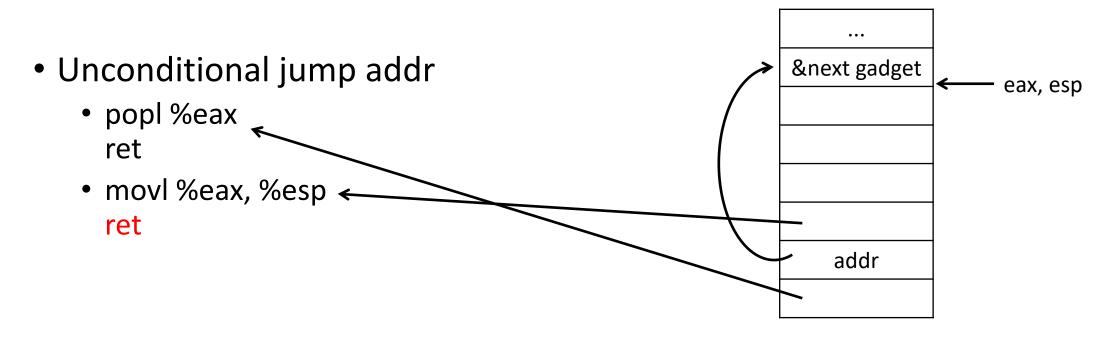
- Unconditional jump addr
 - popl %eax ret
 - movl %eax, %esp
 ret

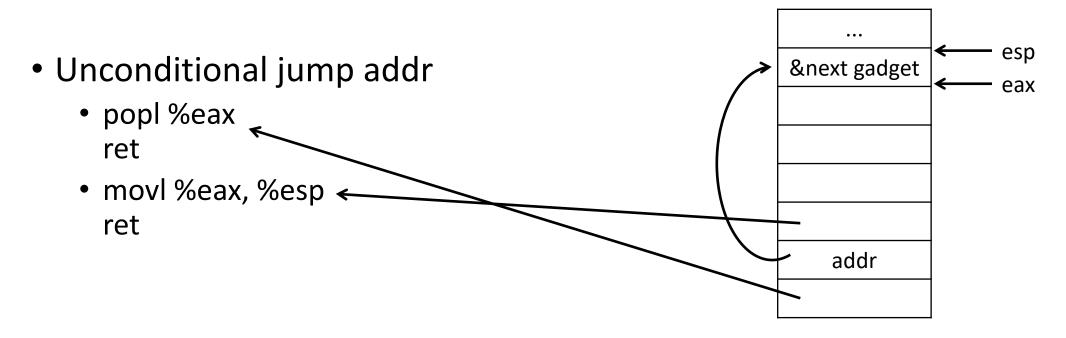












- Unconditional jump addr
 - popl %eax ret
 - movl %eax, %esp
 ret
- Conditional jump addr, one way
 - Conditionally set a register to 0 or 0xffffffff
 - Perform a logical AND with the register and an offset
 - Add the result to esp

Conditionally set a register to 0 or 0xffffffff

- Compare registers eax and ebx and set ecx to
 - Oxffffffff if eax < ebx
 - 0 if eax >= ebx
- Ideally we would find a sequence like cmpl %ebx, %eax set carry flag cf according to eax - ebx sbbl %ecx, %ecx ecx ← ecx - cf; or ecx ← -cf ret
- Unlikely to find this; instead look for cmp; ret and sbb; ret sequences

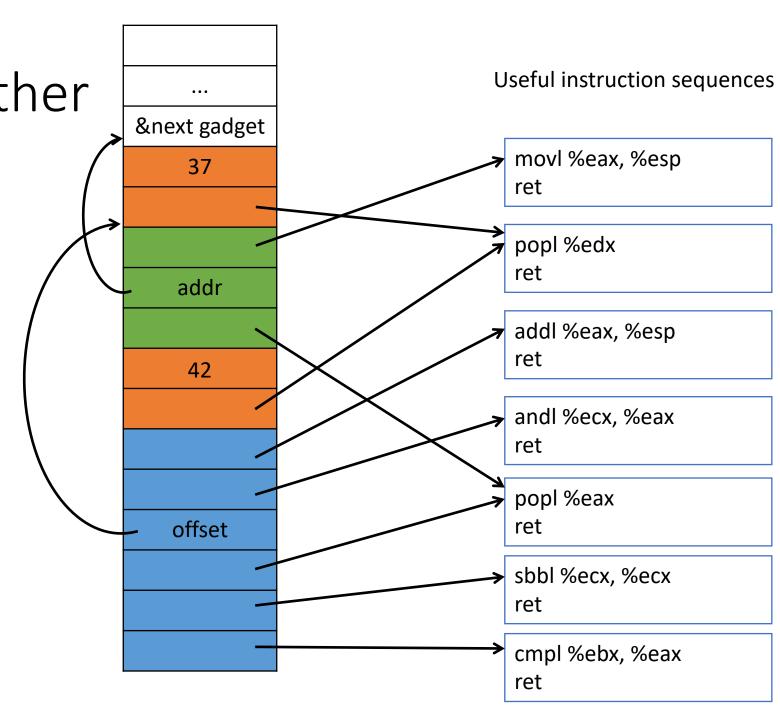
Performing a logical AND with a constant

- Pop the constant into a register using pop; ret
- Use an and; ret sequence

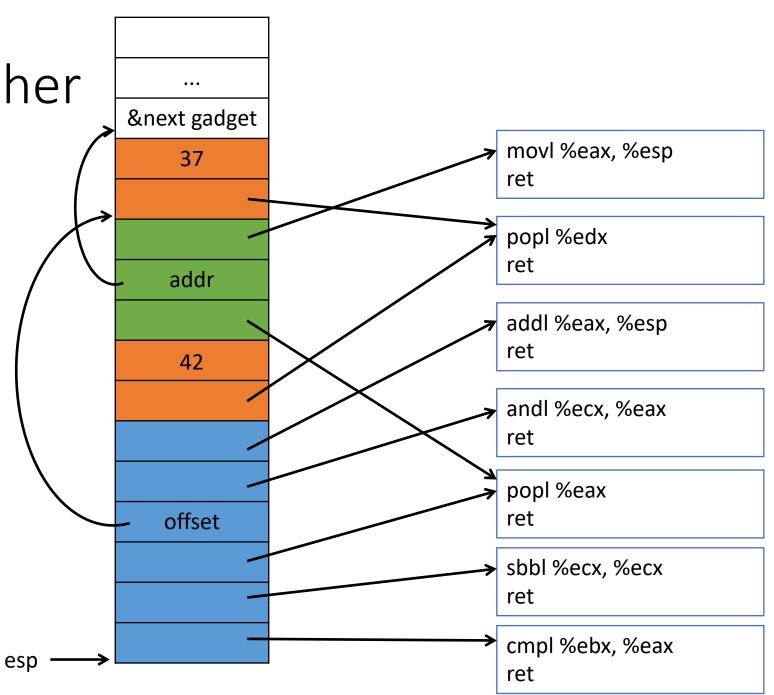
Updating the stack pointer

• Use an add esp; ret sequence

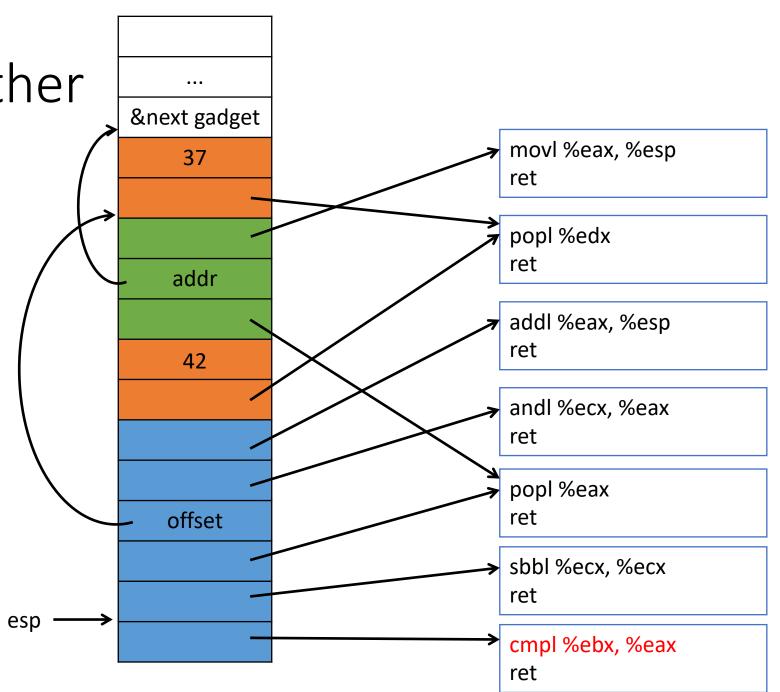
Conditional jump
Load constant in edx
Unconditional jump



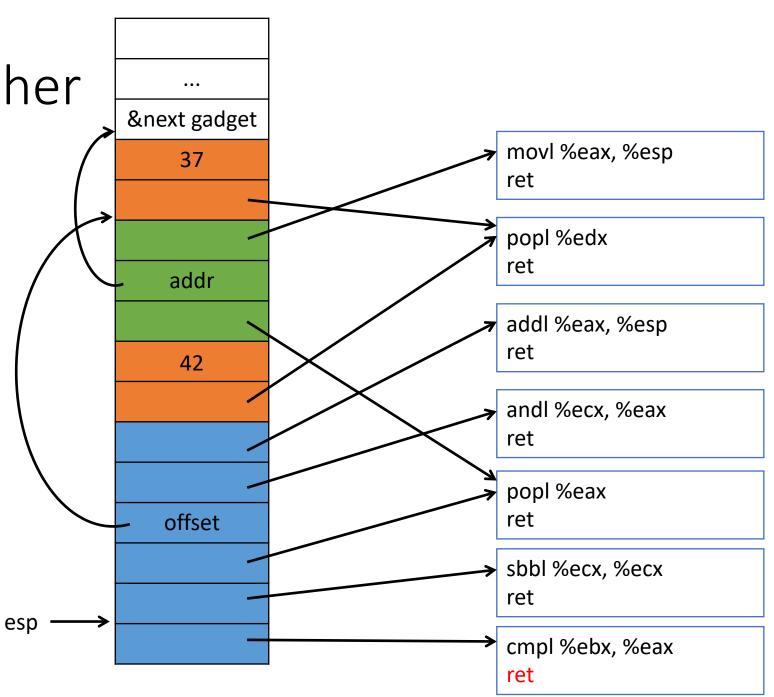
Register	Value
eax	10
ebx	20
есх	108
edx	17



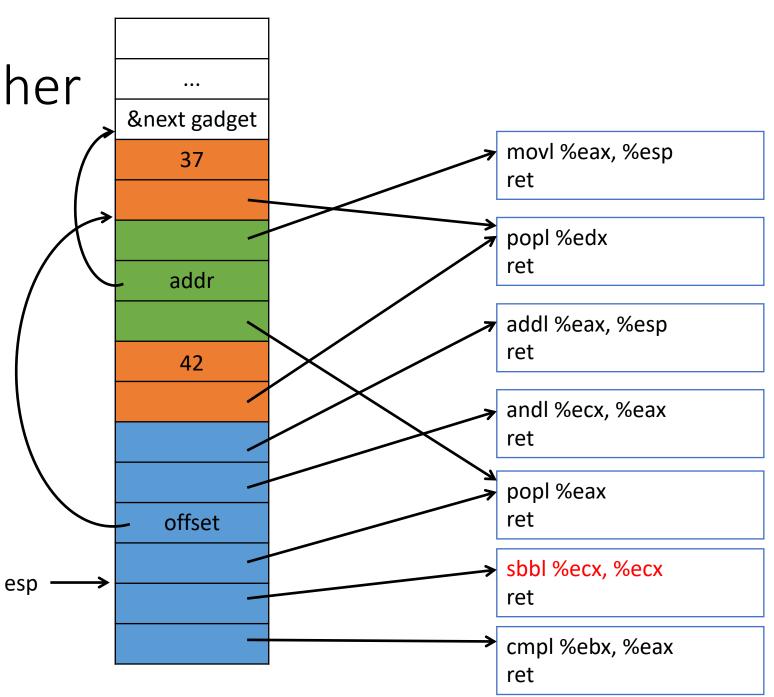
Register	Value
eax	10
ebx	20
есх	108
edx	17



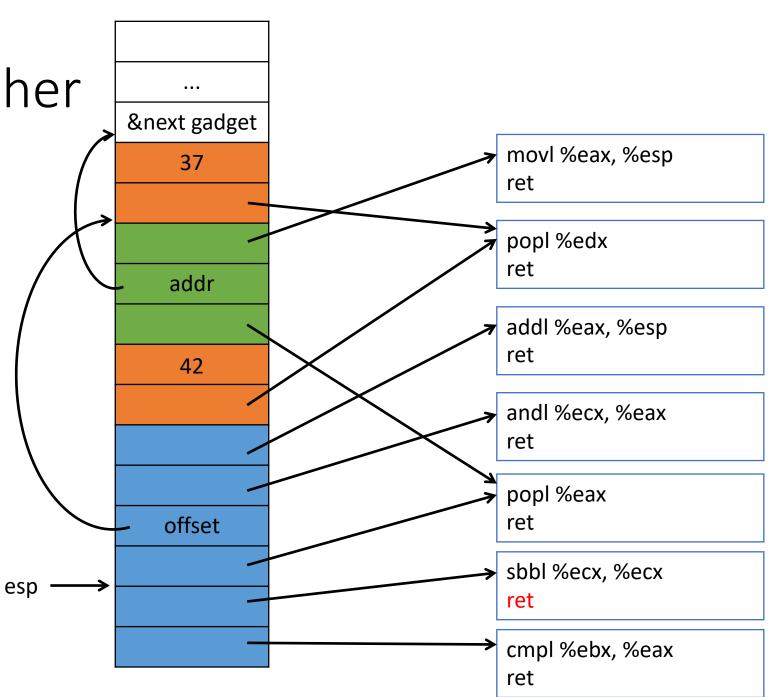
Register	Value
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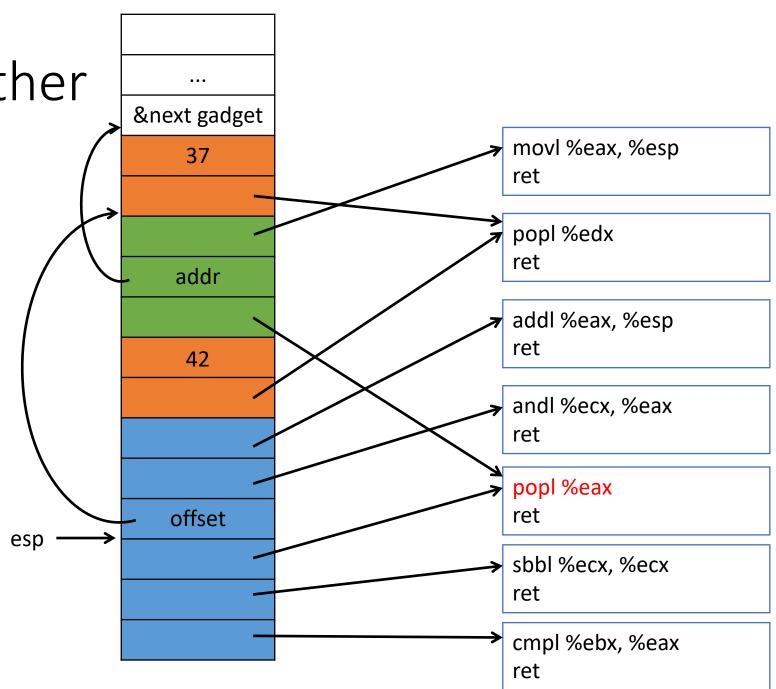
Register	Value
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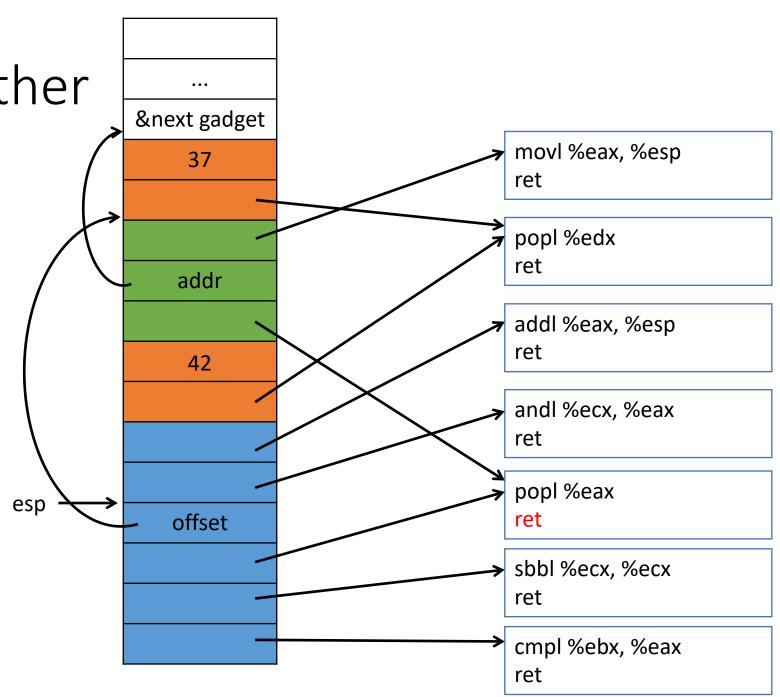
Register	Value
eax	10
ebx	20
есх	Oxfffffff
edx	17



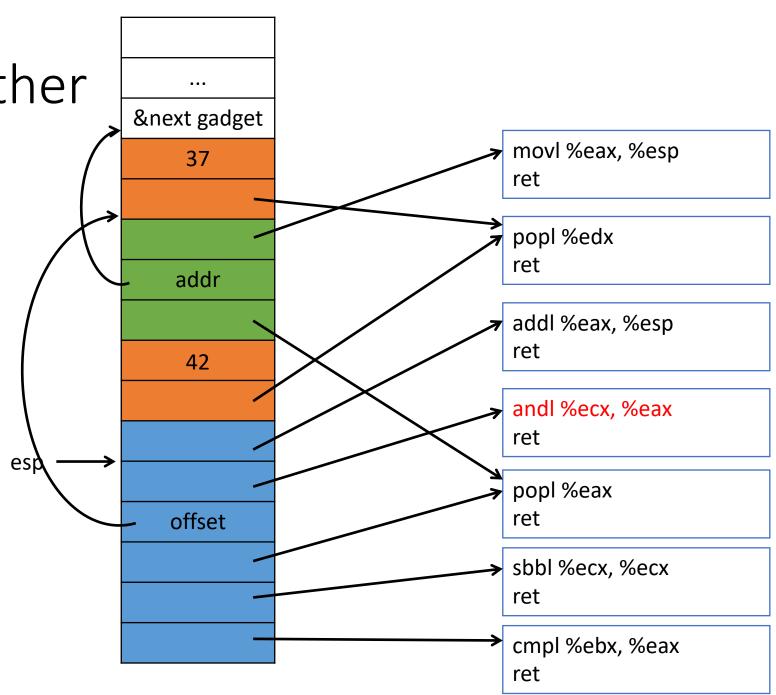
Register	Value
eax	10
ebx	20
есх	Oxfffffff
edx	17



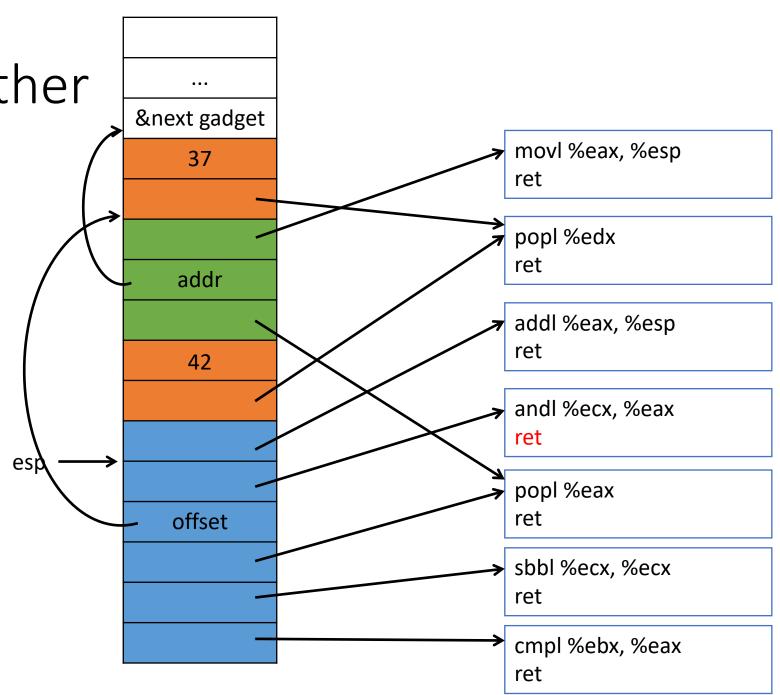
Register	Value
eax	20 = offset
ebx	20
есх	Oxfffffff
edx	17



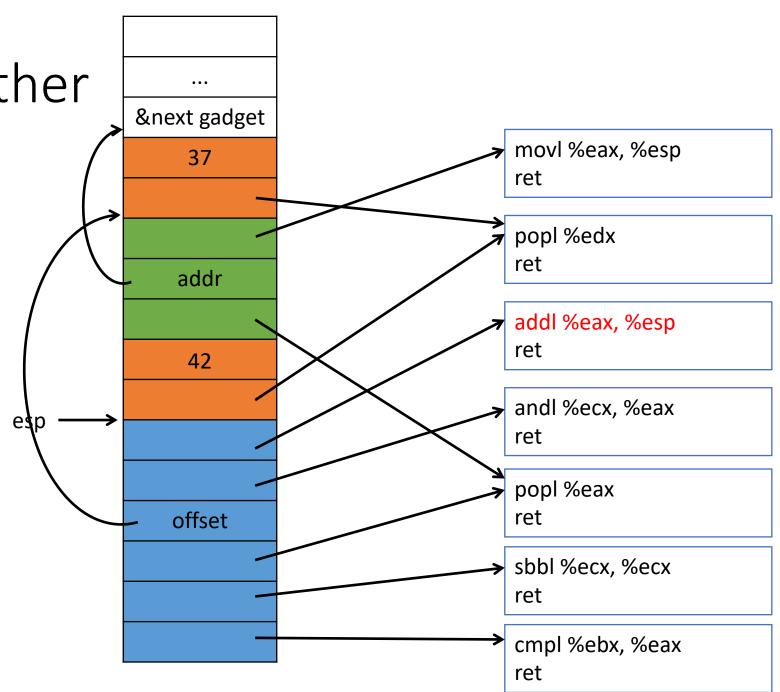
Register	Value
eax	20 = offset
ebx	20
есх	Oxffffffff
edx	17



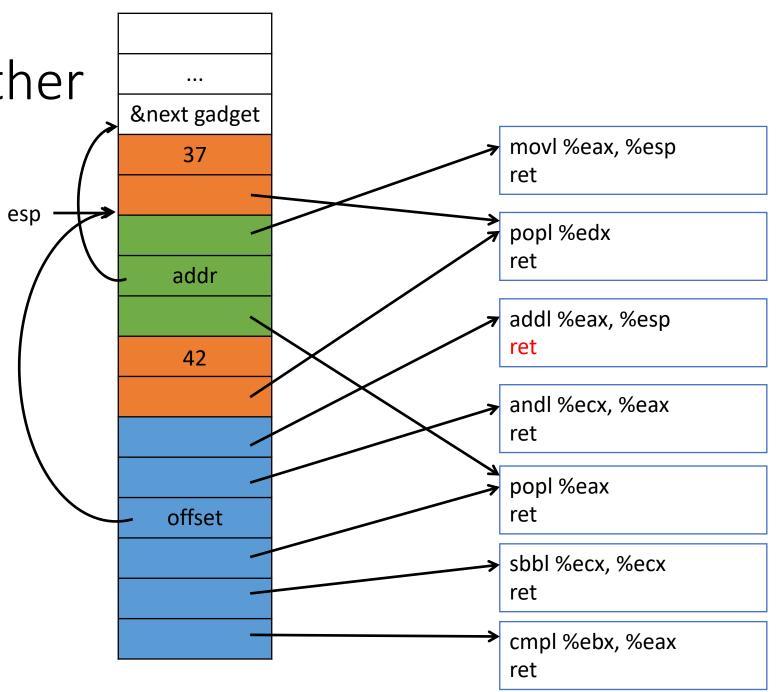
Register	Value
eax	20 = offset
ebx	20
есх	Oxffffffff
edx	17



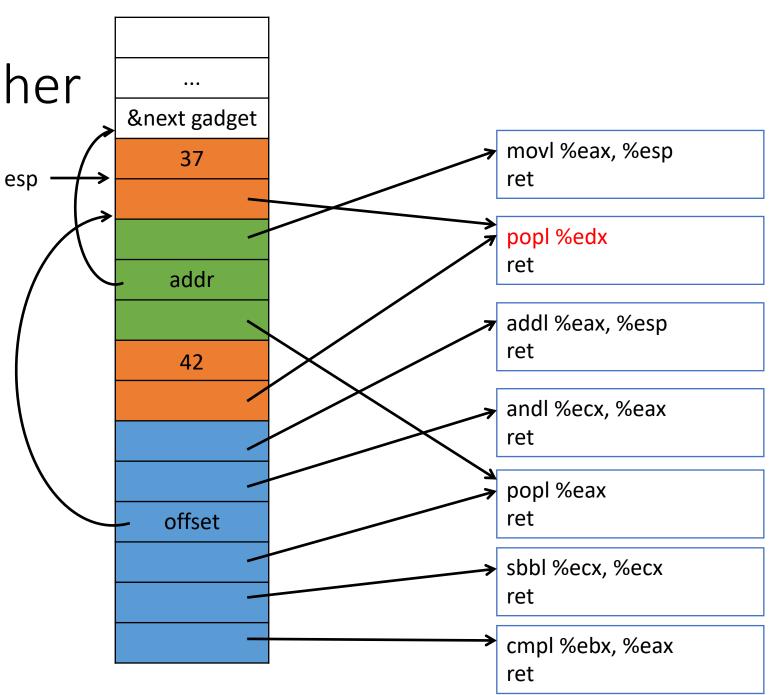
Register	Value
eax	20 = offset
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есх	Oxfffffff
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Register	Value
eax	20 = offset
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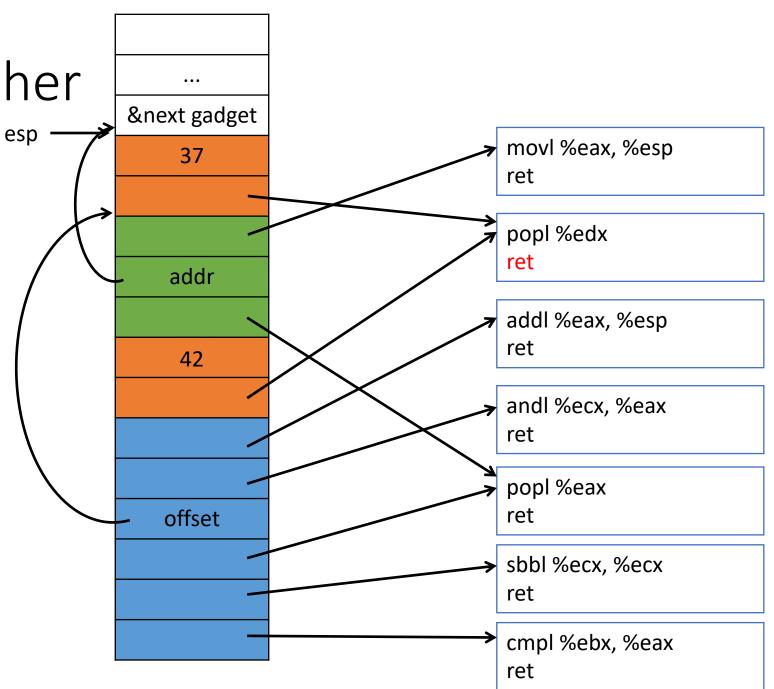


Register	Value
eax	20 = offset
ebx	20
есх	Oxffffffff
edx	17



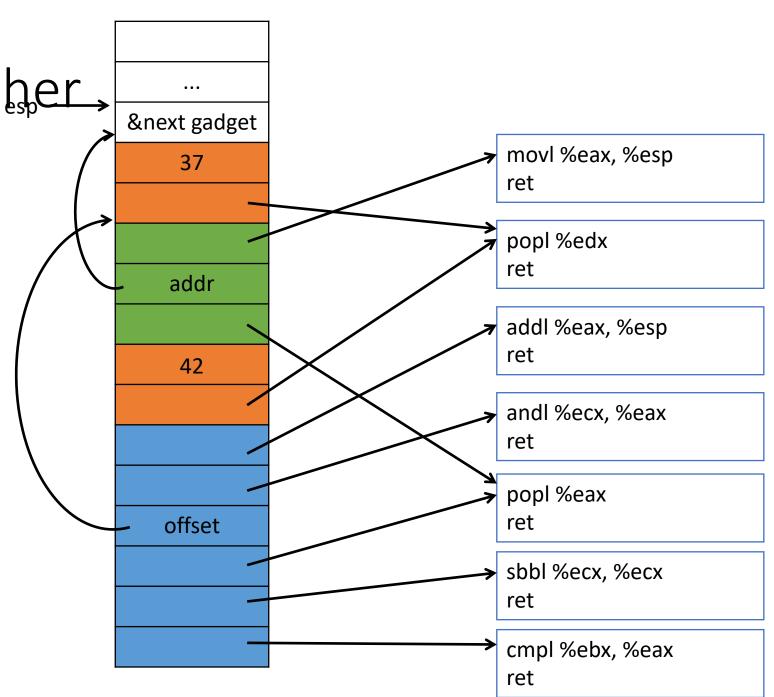


Register	Value
eax	20 = offset
ebx	20
есх	Oxfffffff
edx	37

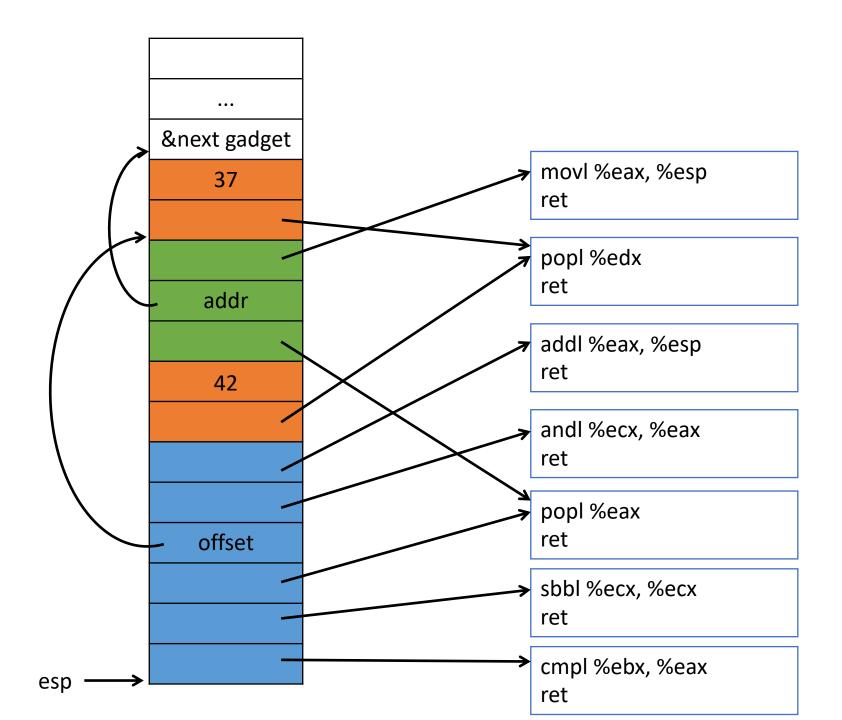




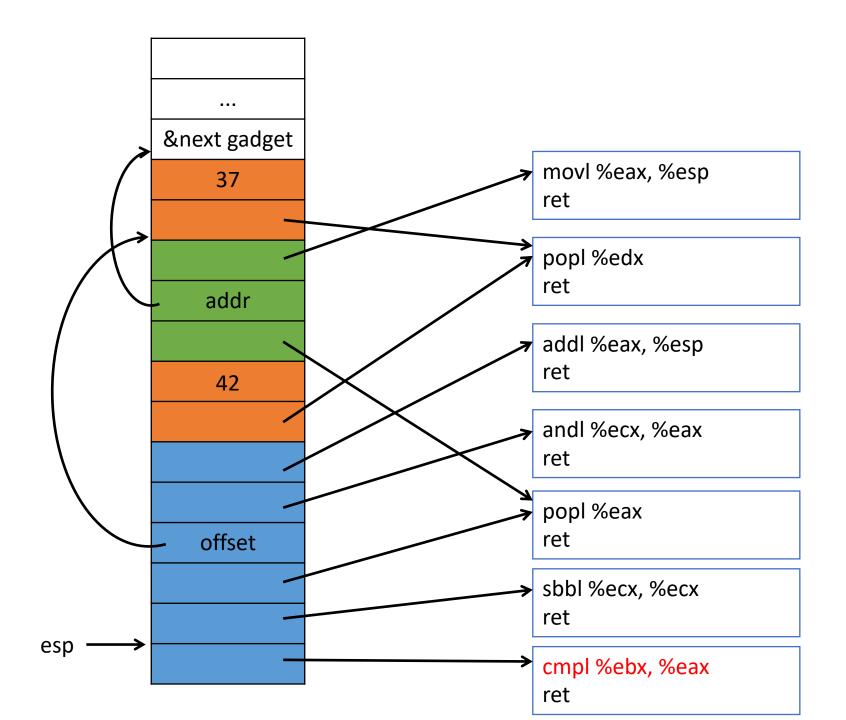
Register	Value
eax	20 = offset
ebx	20
есх	Oxfffffff
edx	37



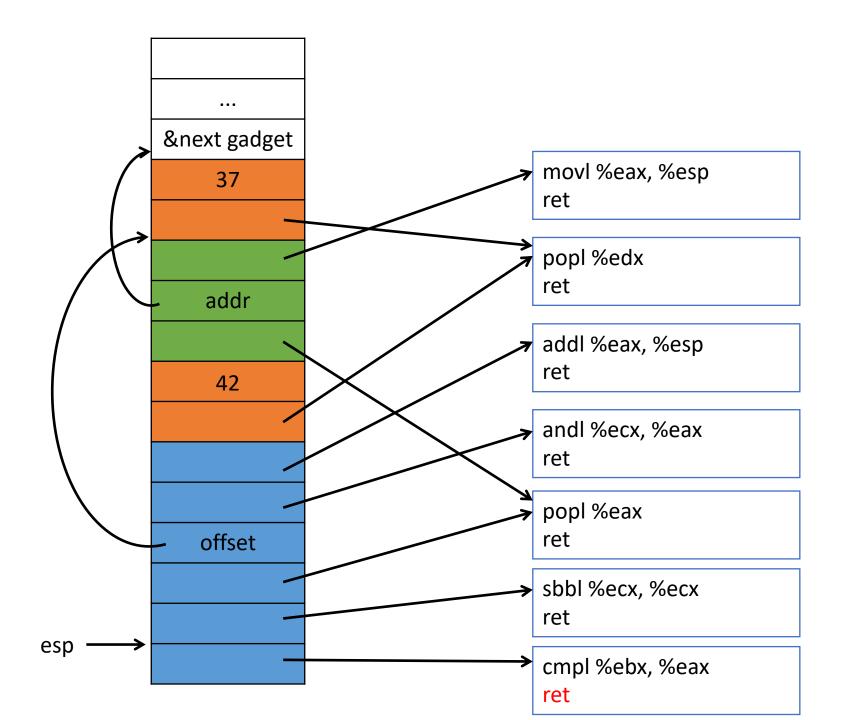
Register	Value
eax	500
ebx	20
есх	108
edx	17



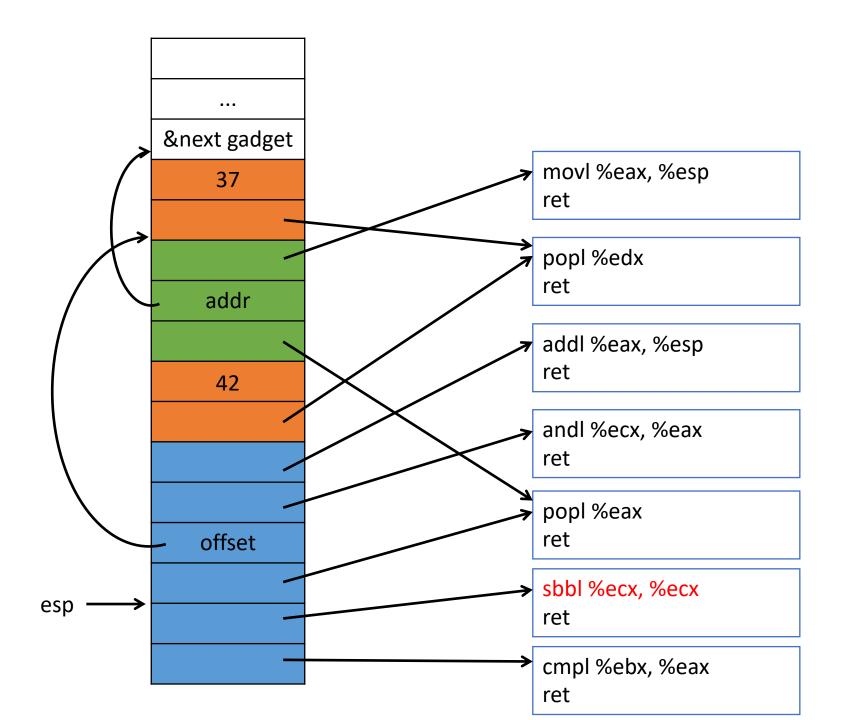
Register	Value
eax	500
ebx	20
есх	108
edx	17



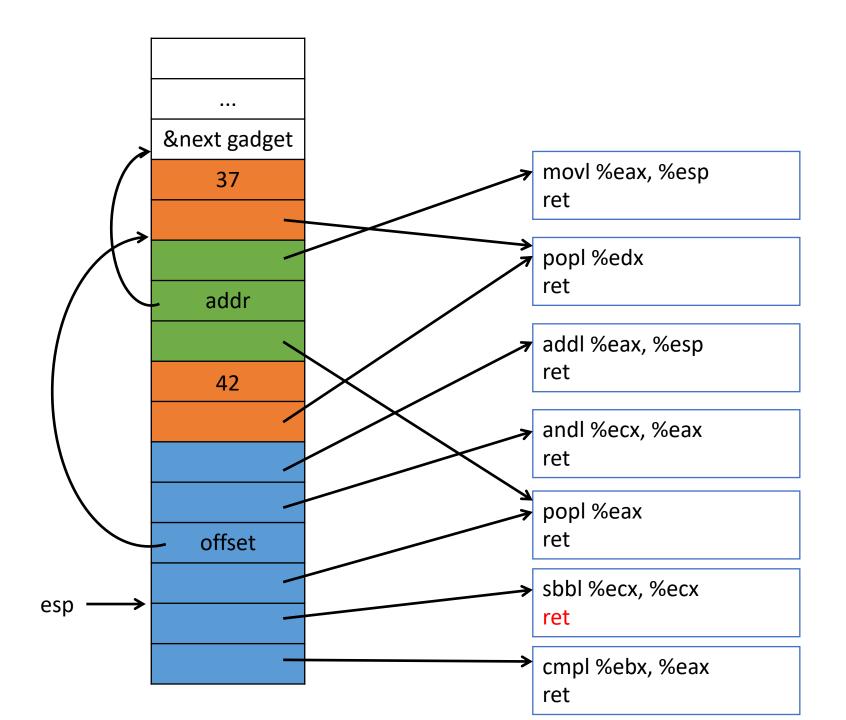
Register	Value
eax	500
ebx	20
есх	108
edx	17



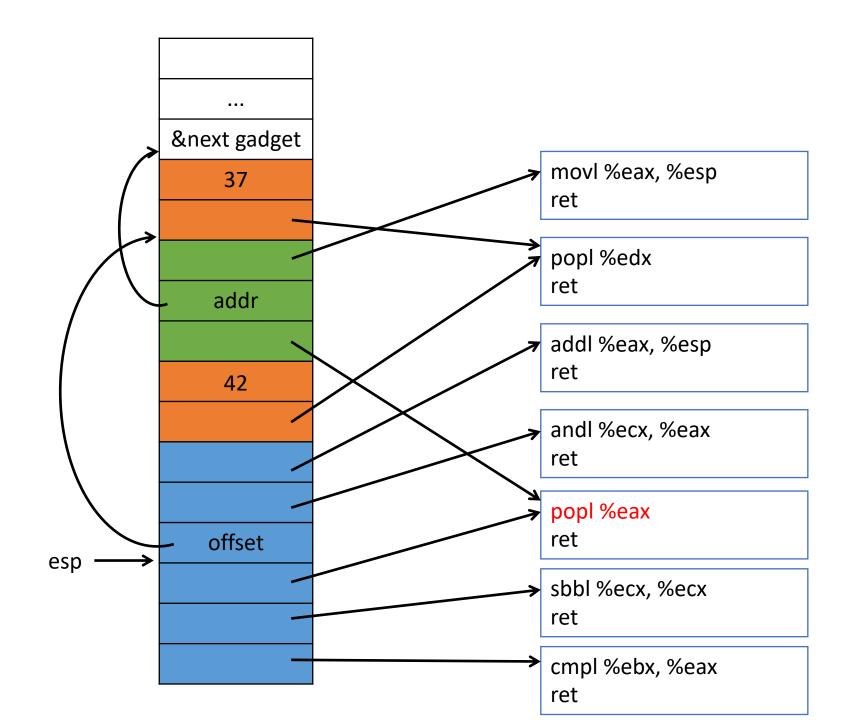
Register	Value
eax	500
ebx	20
есх	108
edx	17



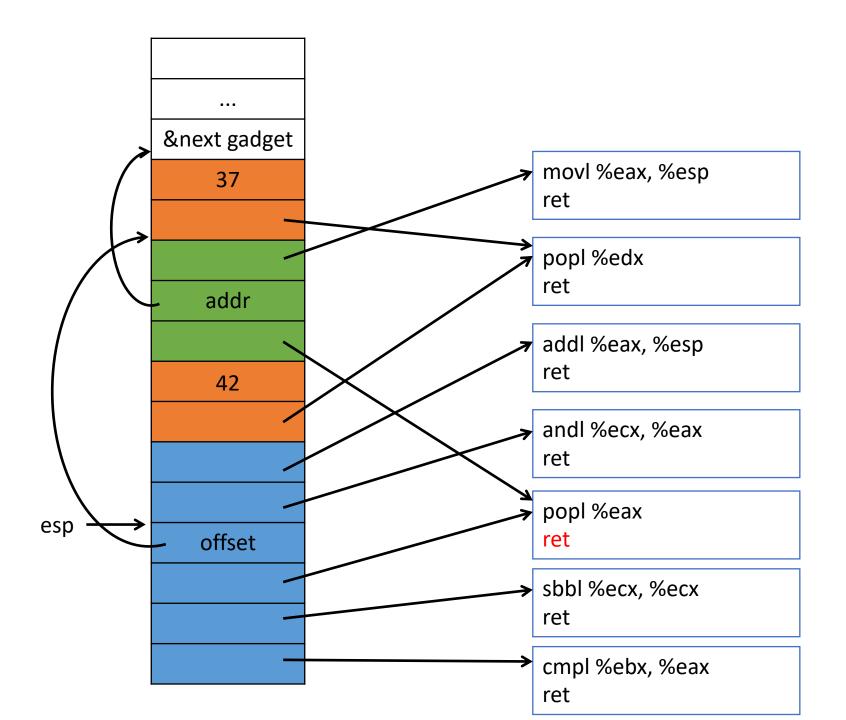
Register	Value
eax	500
ebx	20
есх	0
edx	17



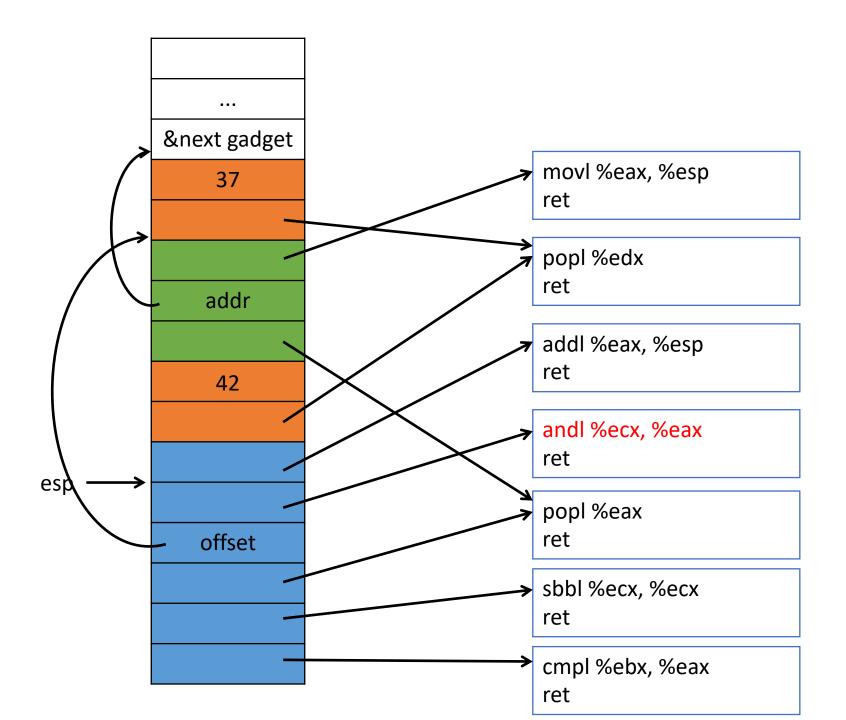
Register	Value
eax	500
ebx	20
ecx	0
edx	17



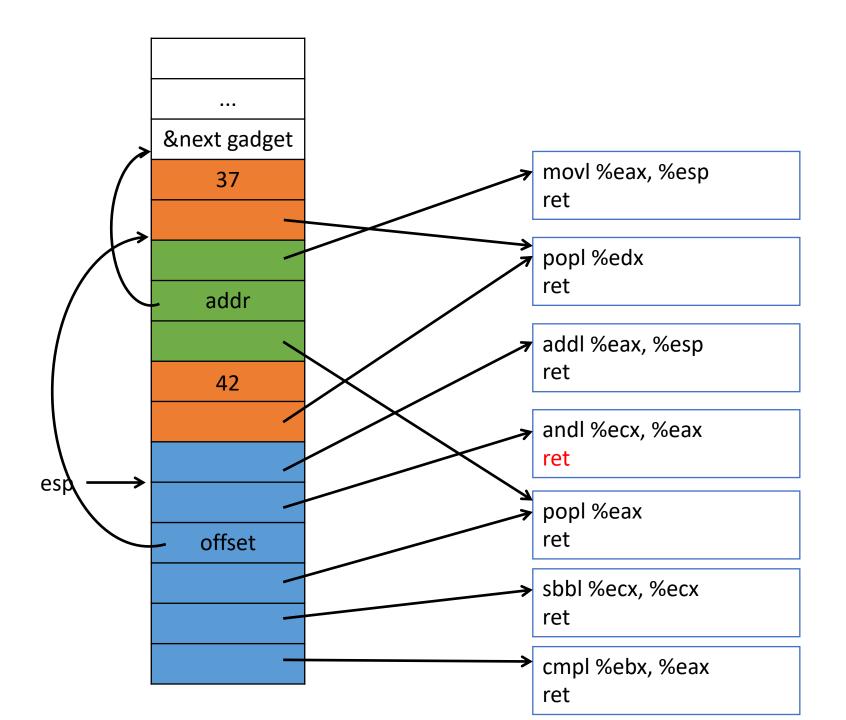
Register	Value
eax	20 = offset
ebx	20
ecx	0
edx	17



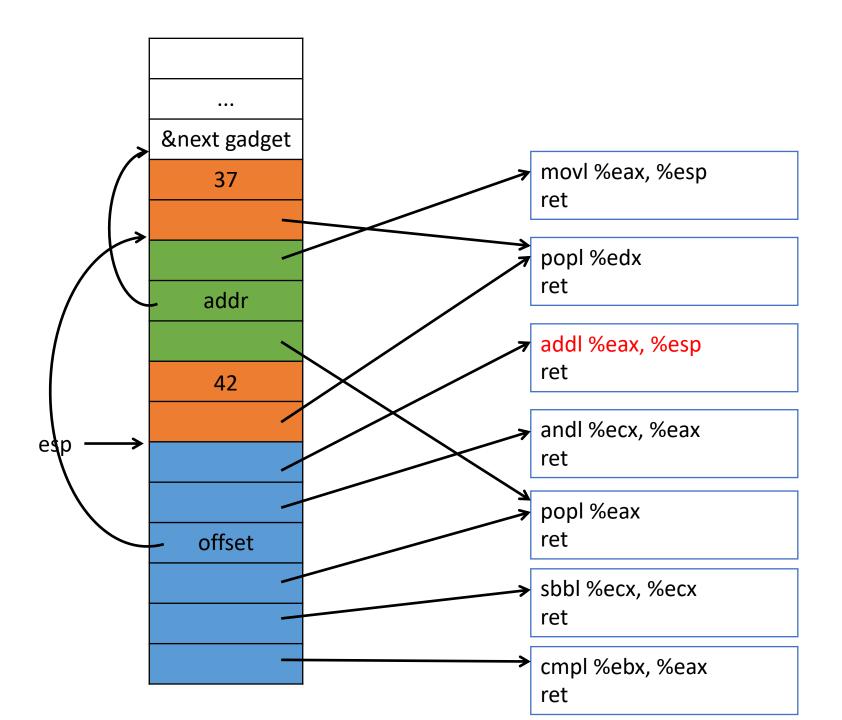
Register	Value
eax	20 = offset
ebx	20
есх	0
edx	17



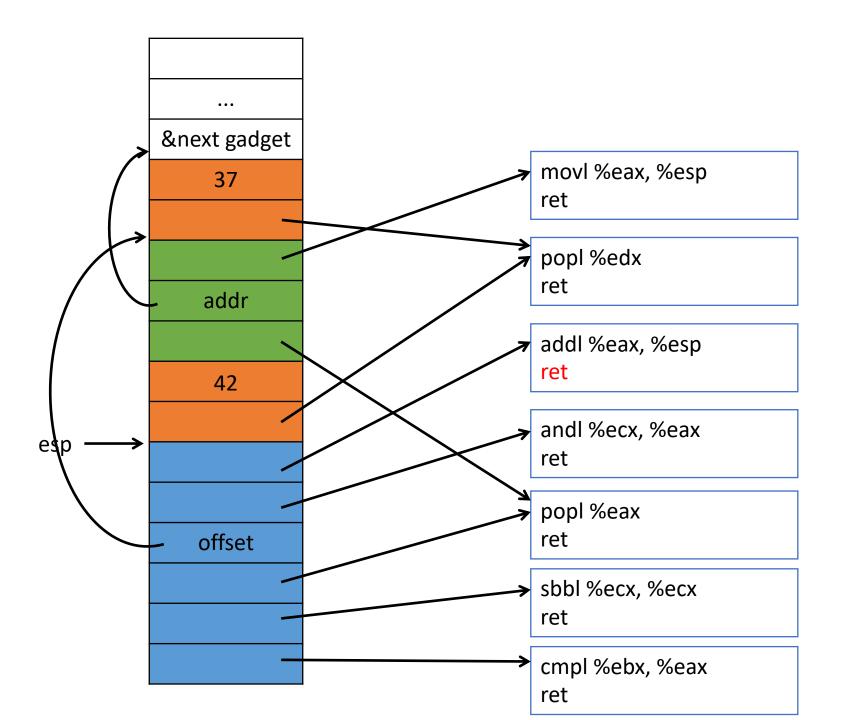
Register	Value
eax	0
ebx	20
есх	0
edx	17



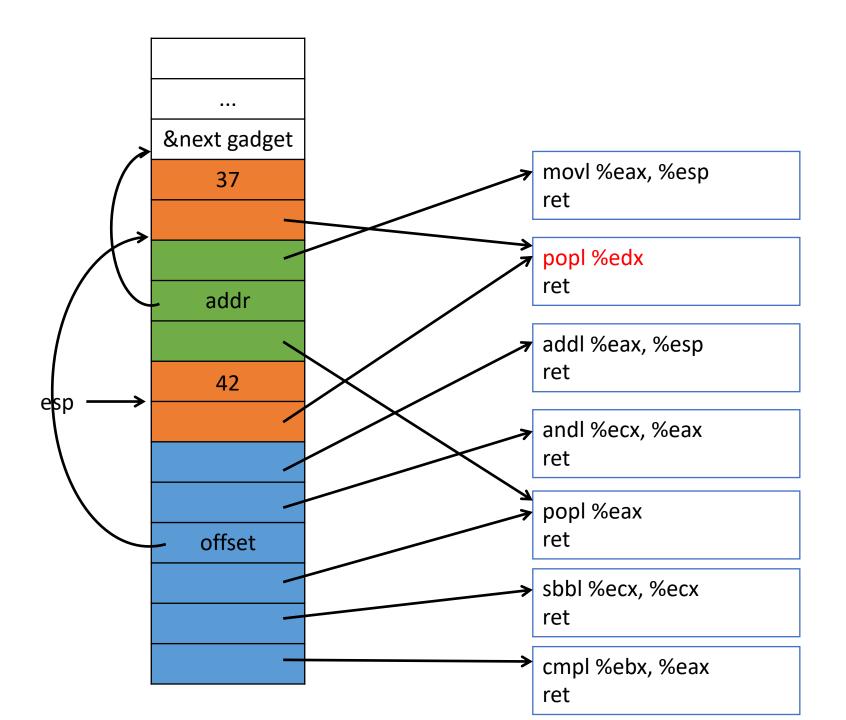
Register	Value
eax	0
ebx	20
есх	0
edx	17



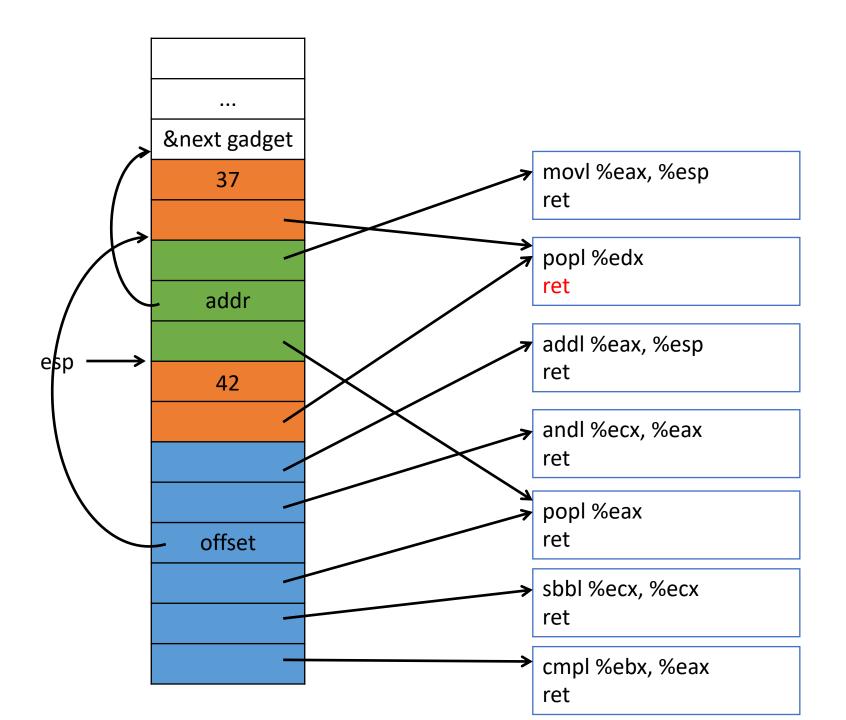
Register	Value
eax	0
ebx	20
есх	0
edx	17



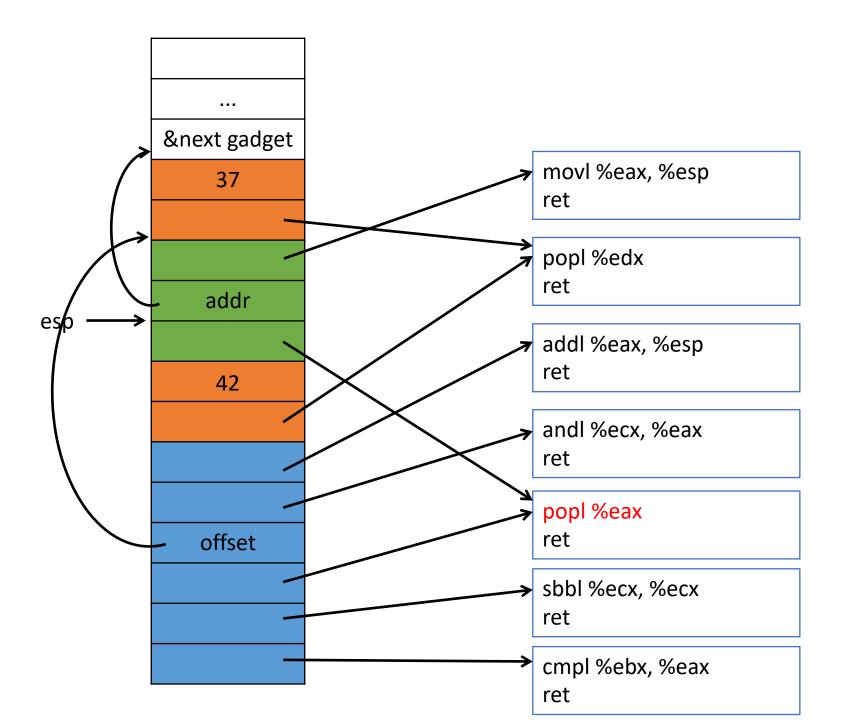
Register	Value
eax	0
ebx	20
есх	0
edx	17

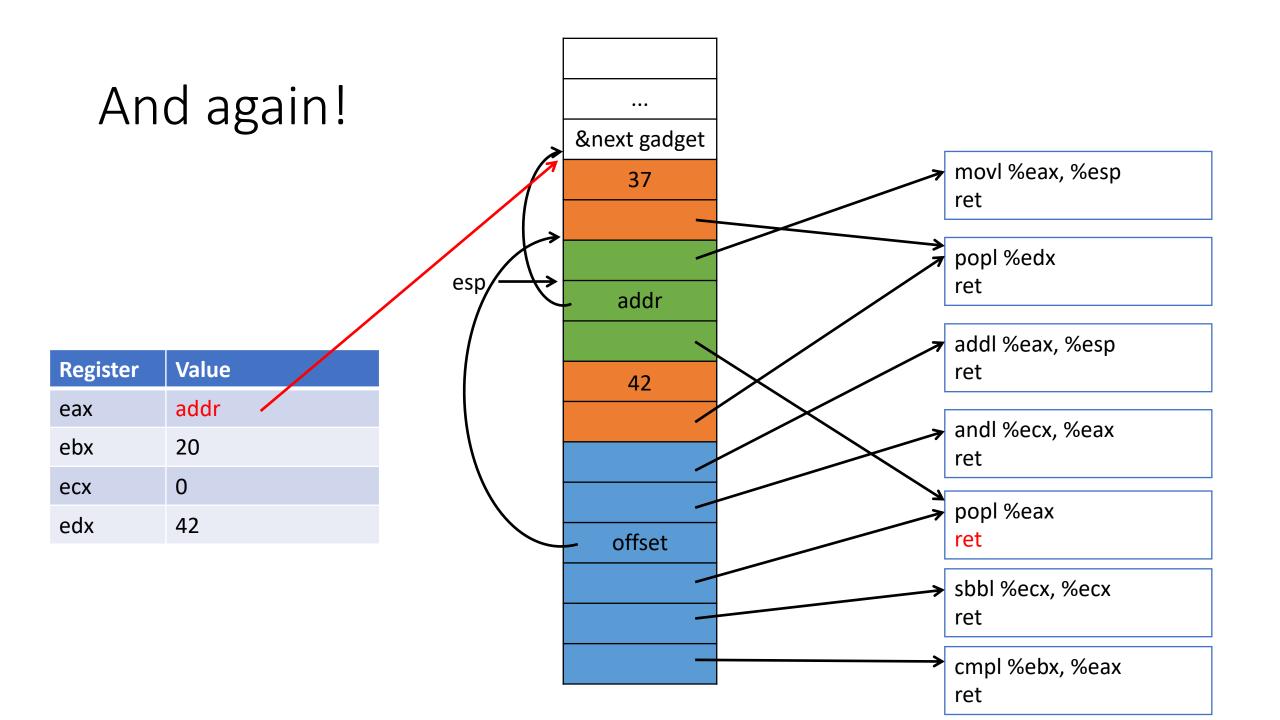


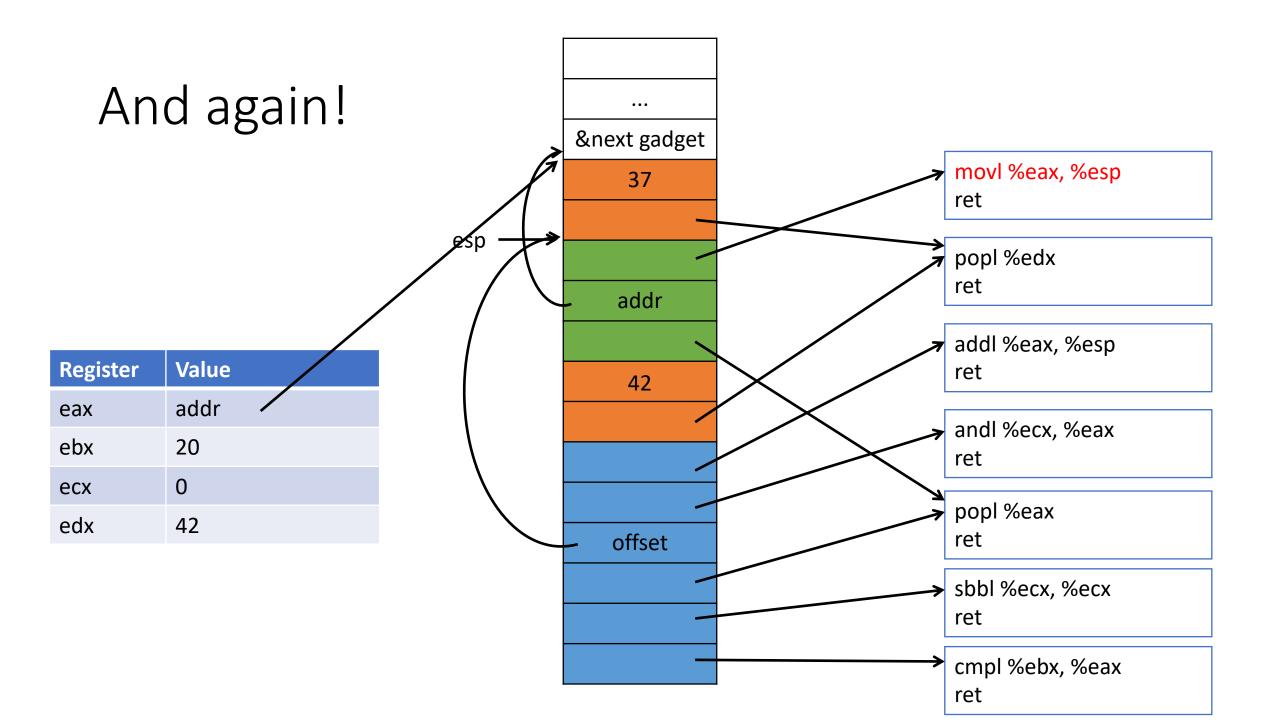
Register	Value
eax	0
ebx	20
есх	0
edx	42

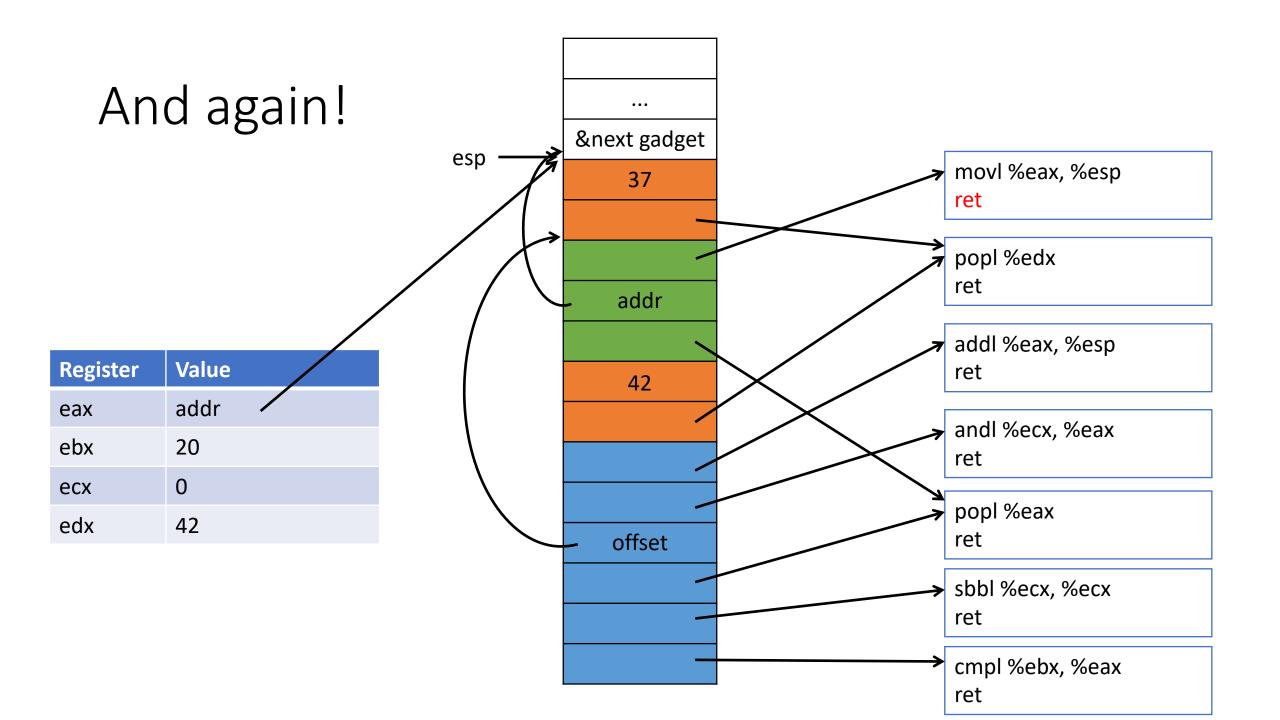


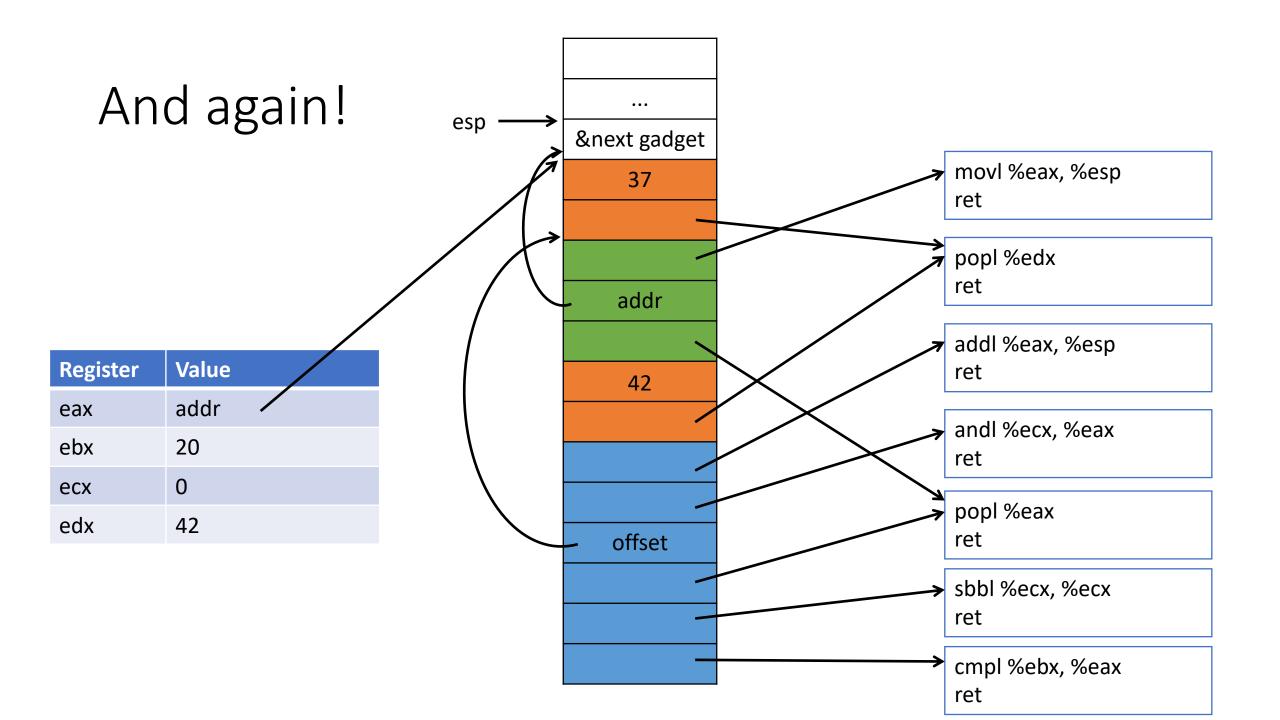
Register	Value
eax	0
ebx	20
ecx	0
edx	42





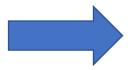






Compare

Register	Value
eax	10
ebx	20
есх	108
edx	17



Register	Value
eax	20
ebx	20
есх	Oxfffffff
edx	37

ebx)
edx = 37;
edx = 42;

Register	Value
eax	500
ebx	20
есх	108
edx	17



Register	Value
eax	addr
ebx	20
есх	0
edx	42