CSCI 210: Computer Architecture
Lecture 30: Pipelining the Datapath

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Oberlin College
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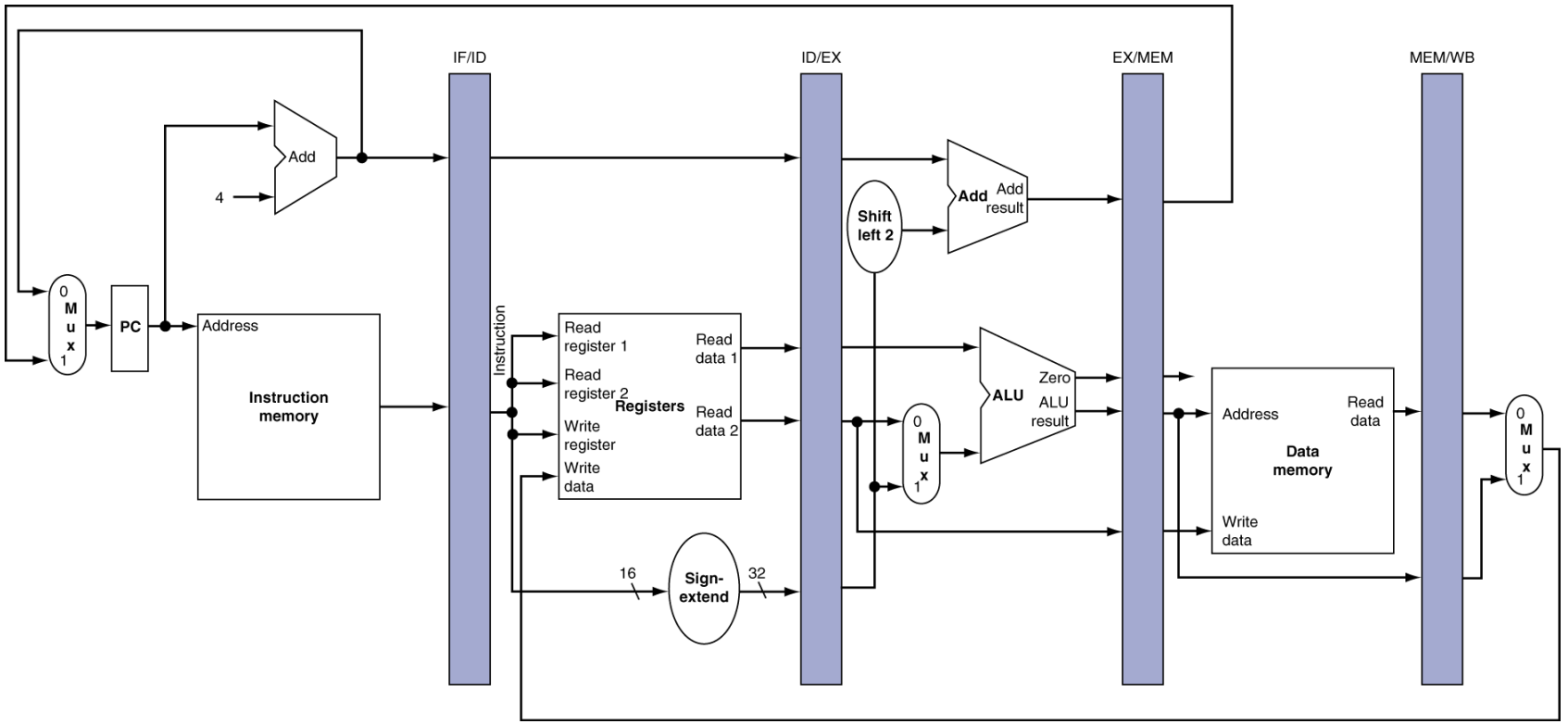
Slides from Cynthia Taylor

Announcements

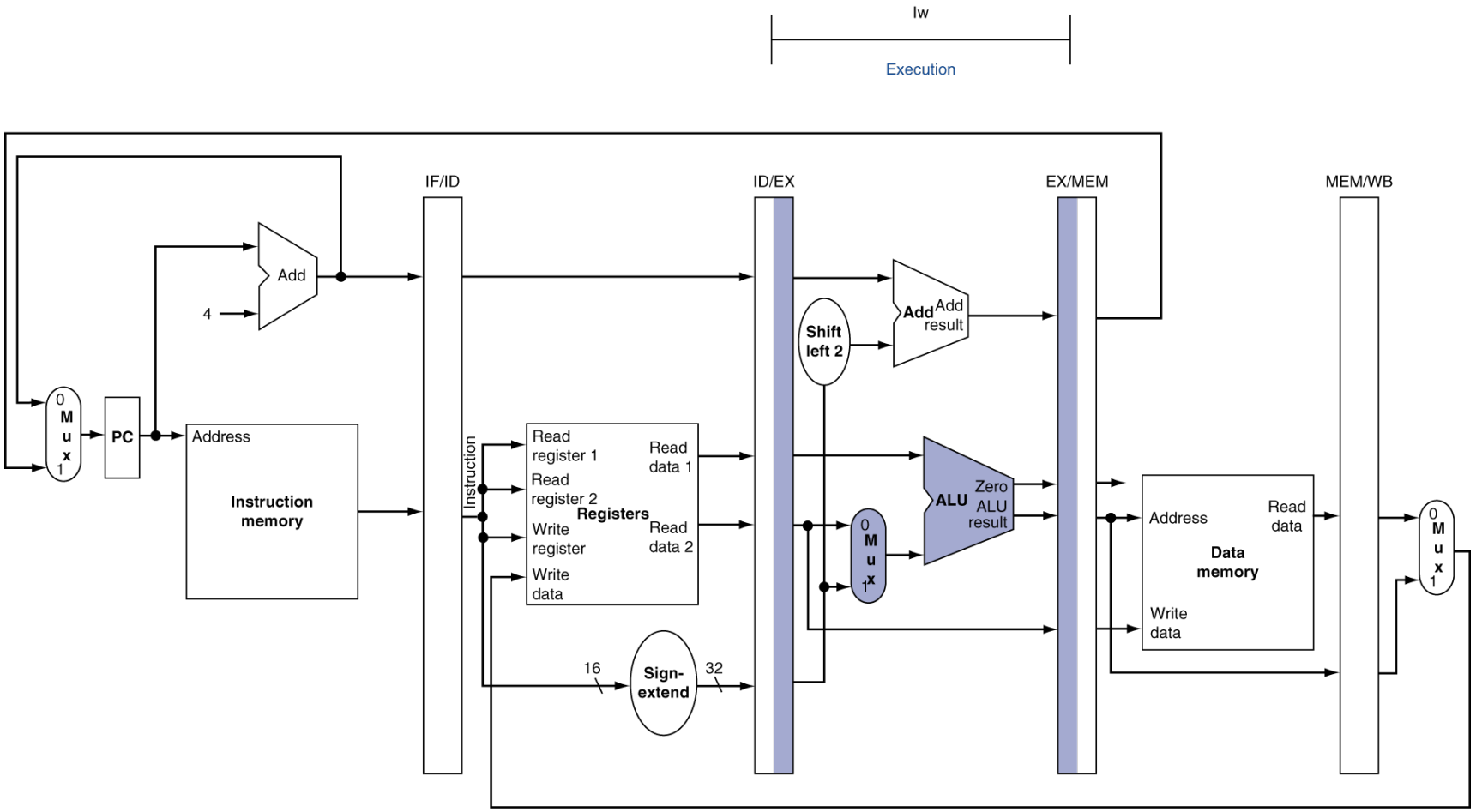
- Problem Set 10 due Jan. 2
- Lab 8 due Jan. 2
- Office Hours Friday 13:30 – 14:30

Pipeline registers

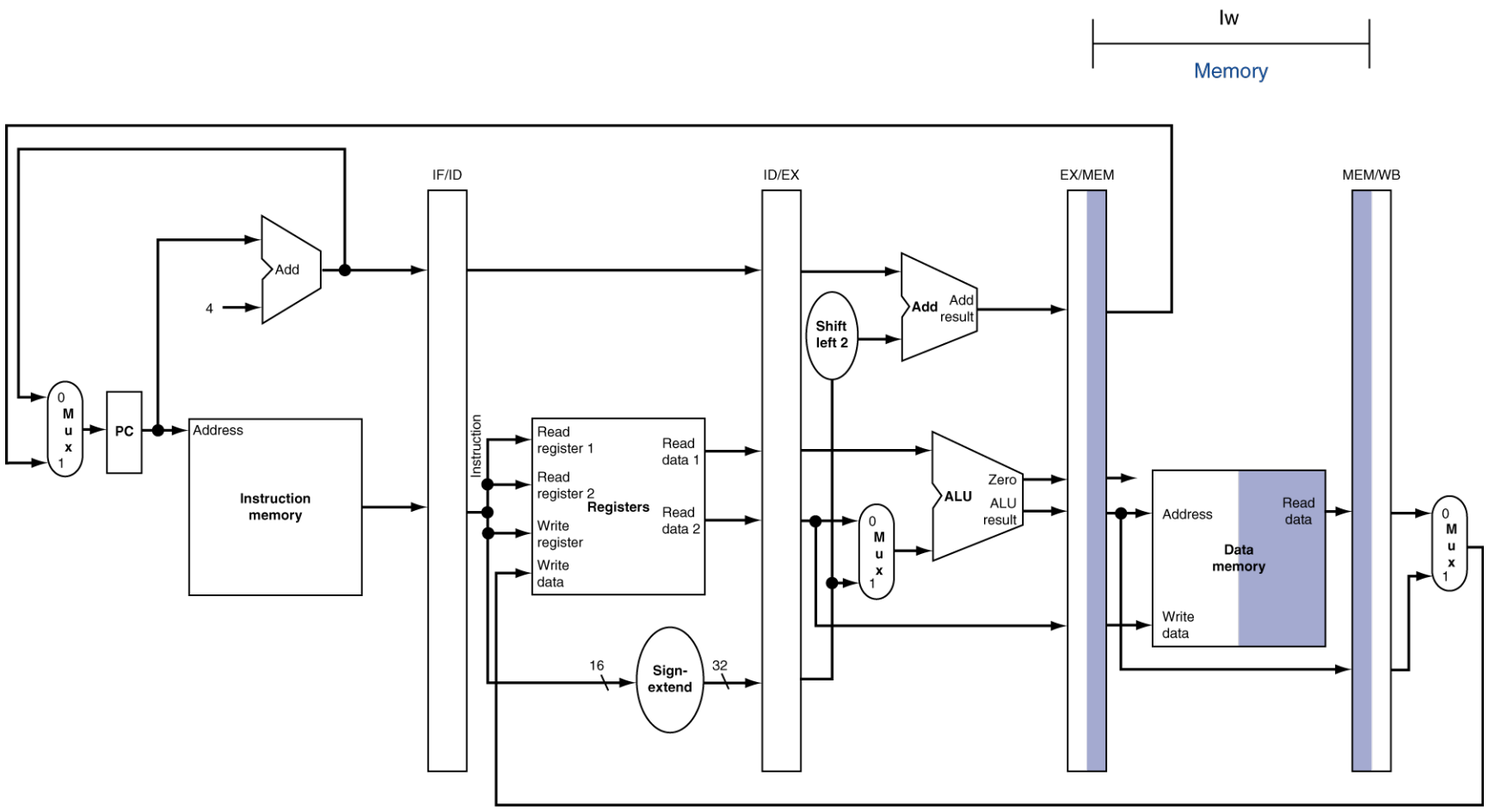
- Need registers between stages
  - To hold information produced in previous cycle



EX for Load


lw
Execution
IF/ID
ID/EX
EX/MEM
MEM/WB
Add
4
0
M
u
x
1
PC
Address
Instruction memory
Instruction
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
16
Sign-extend
32
Shift left 2
Add
Add result
ALU
Zero
ALU result
Address
Read data
Data memory
Write data

MEM for Load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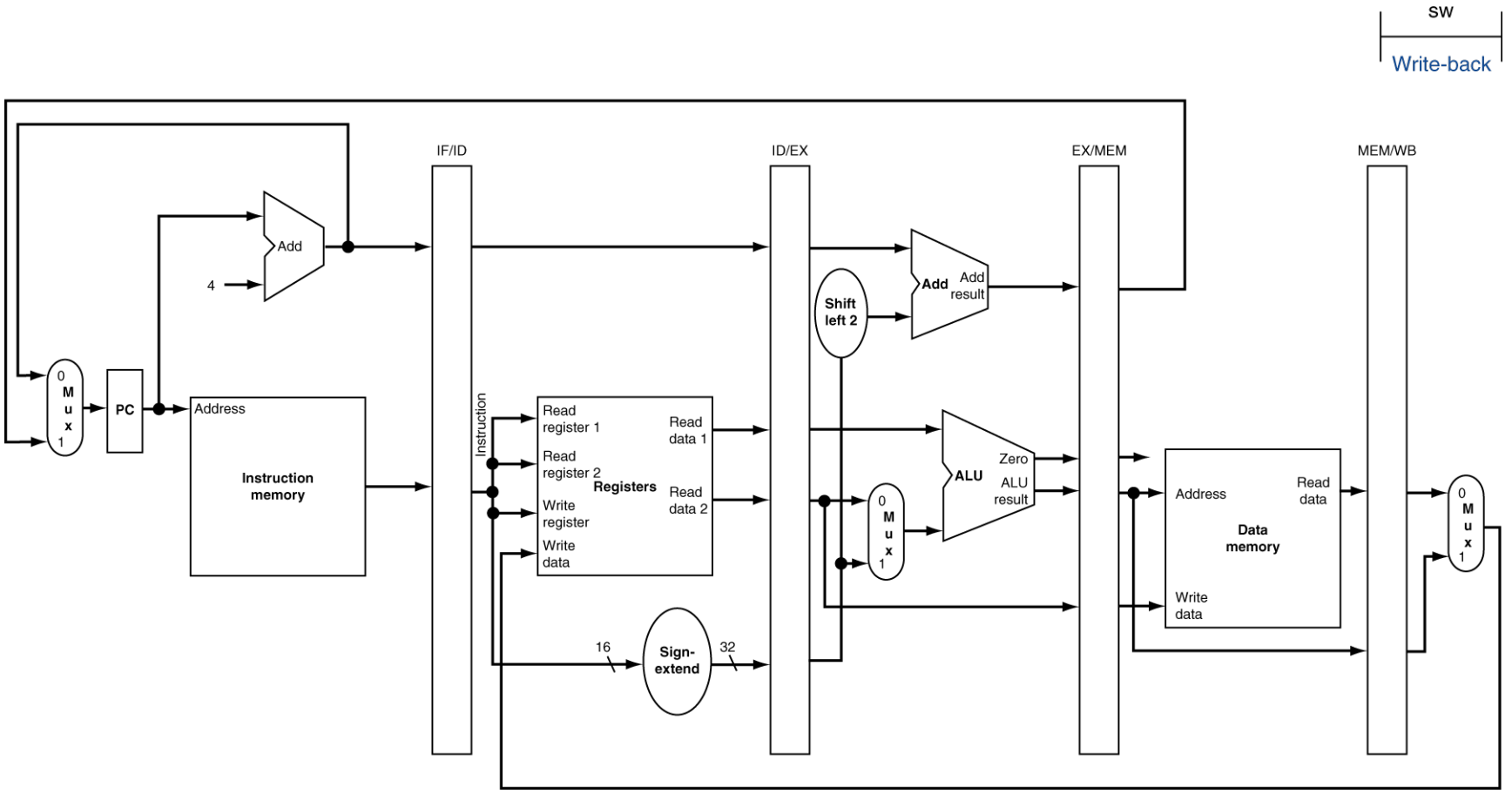
WB for Load


SW
Write-back
IF/ID
ID/EX
EX/MEM
MEM/WB
Add
4
M
u
x
0
1
PC
Address
Instruction memory
Instruction
Read register 1
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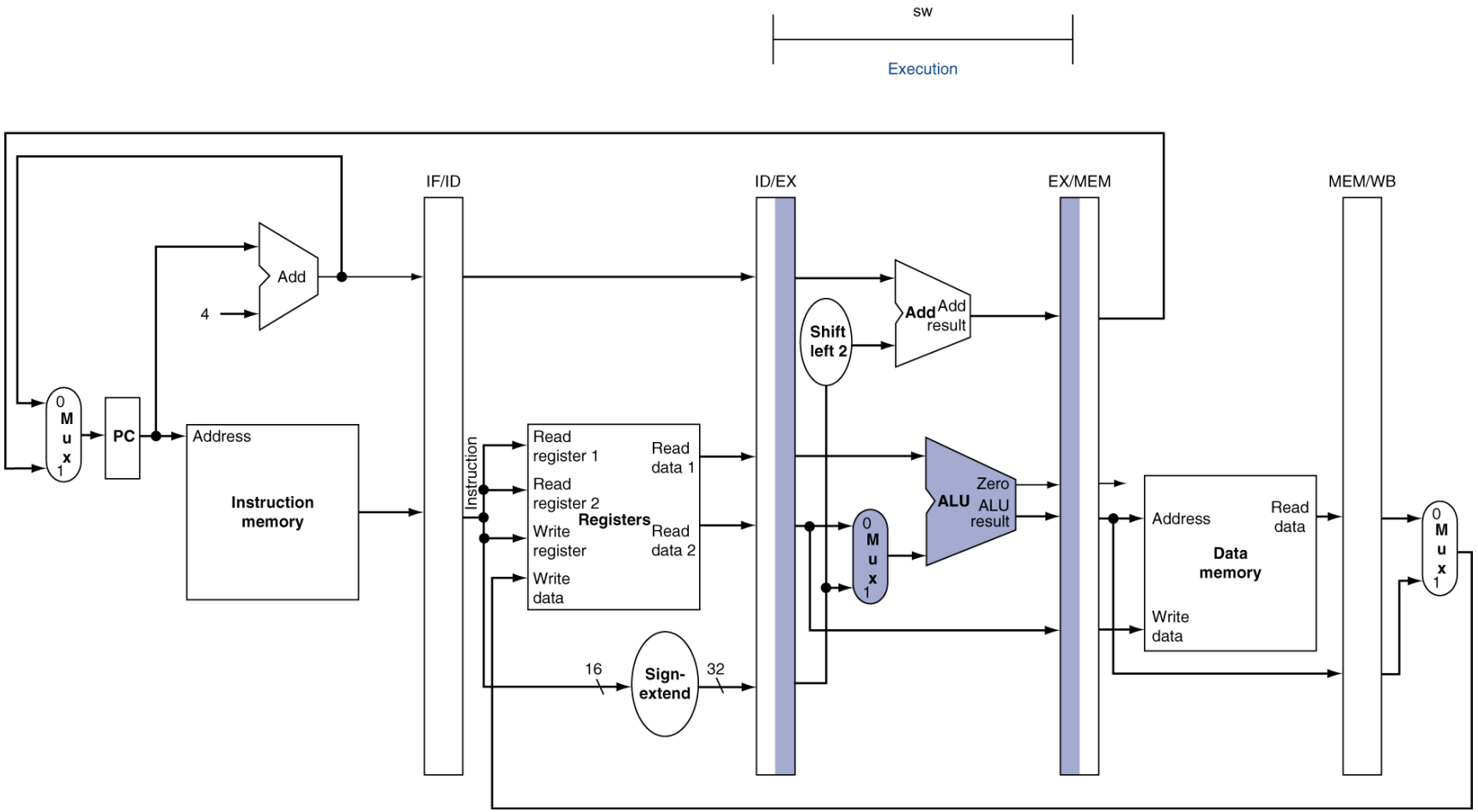
Read data
Data memory
Write data

EX for Store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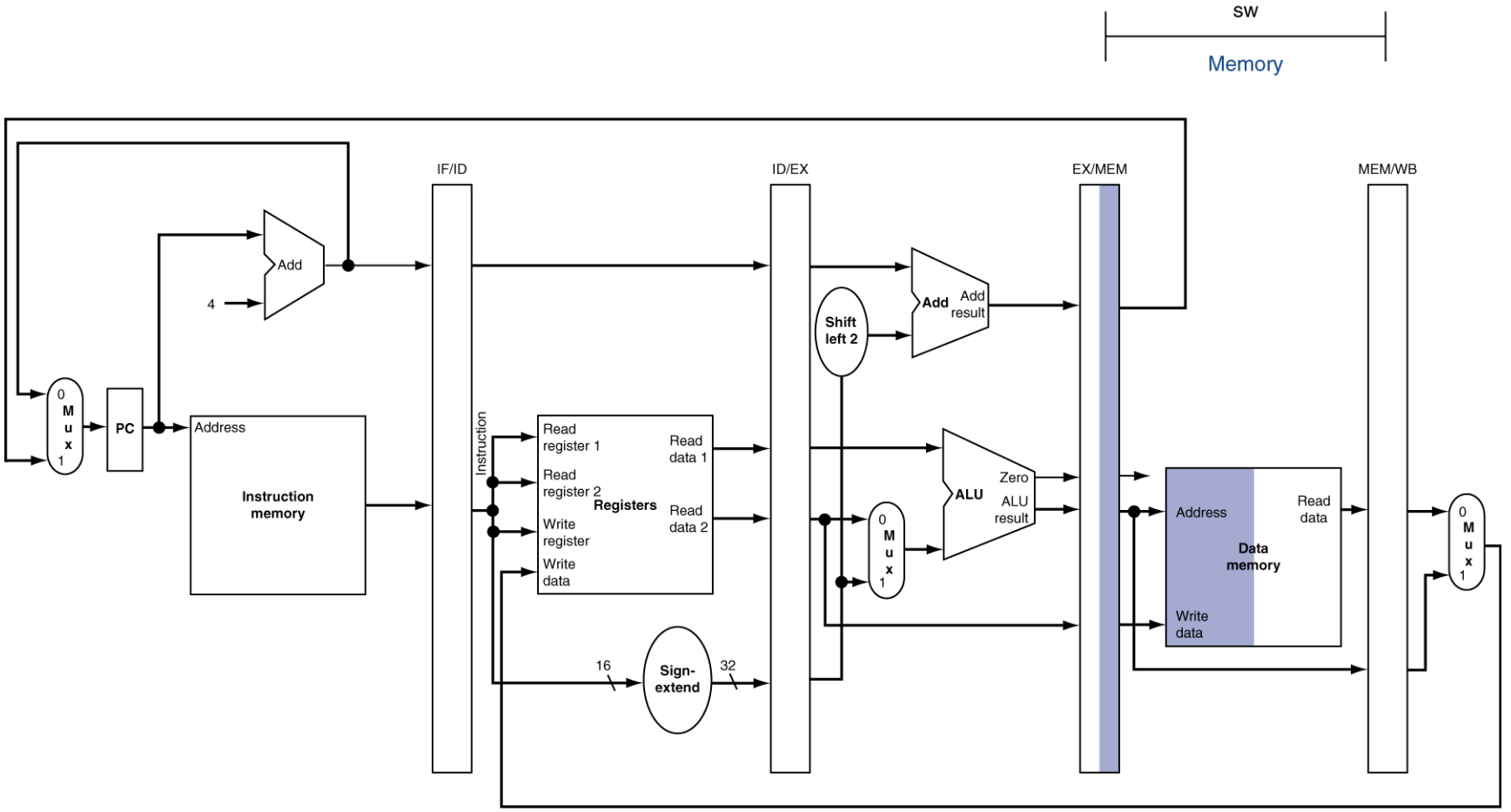
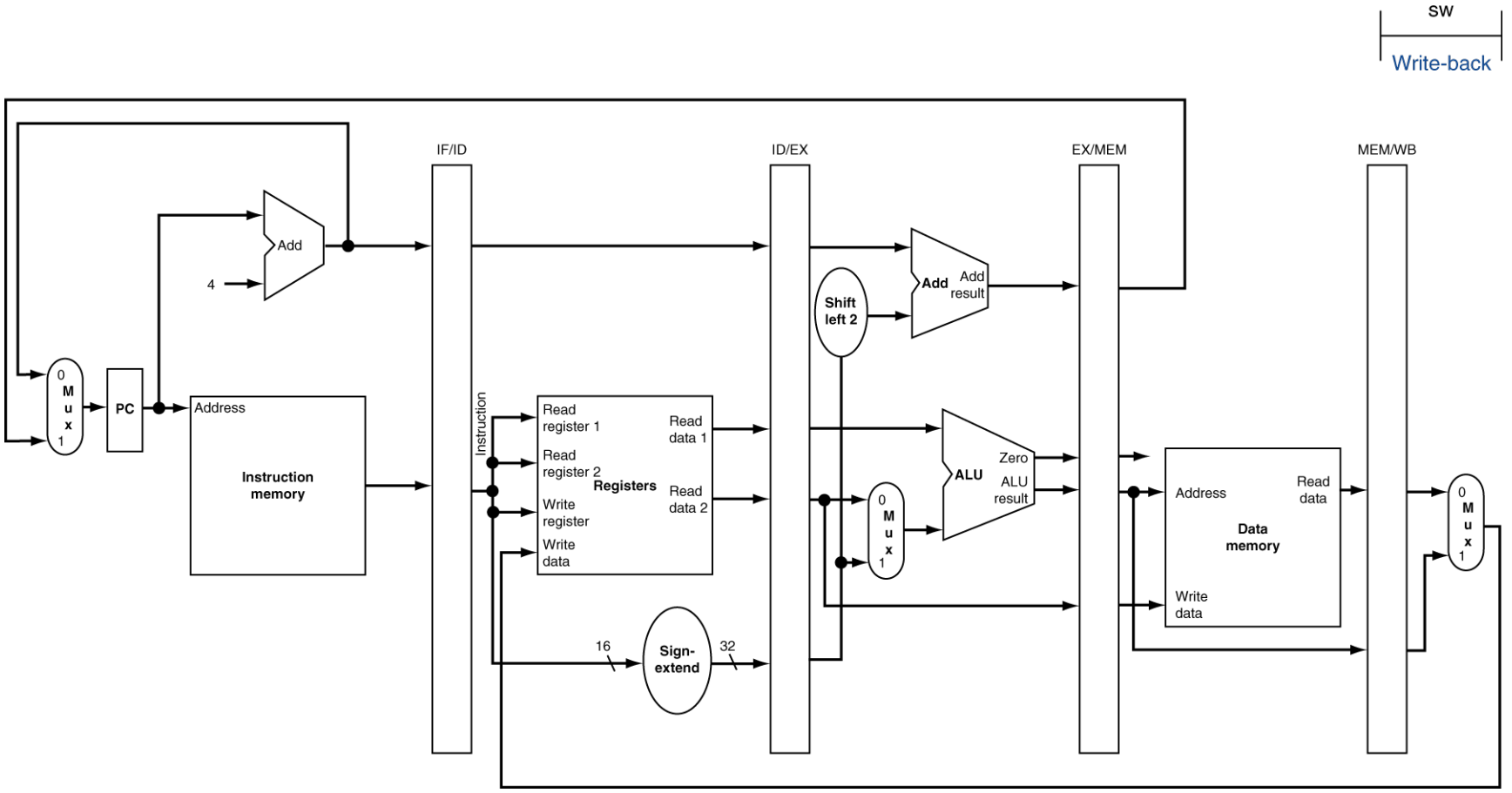
Write data

MEM for Store



WB for Store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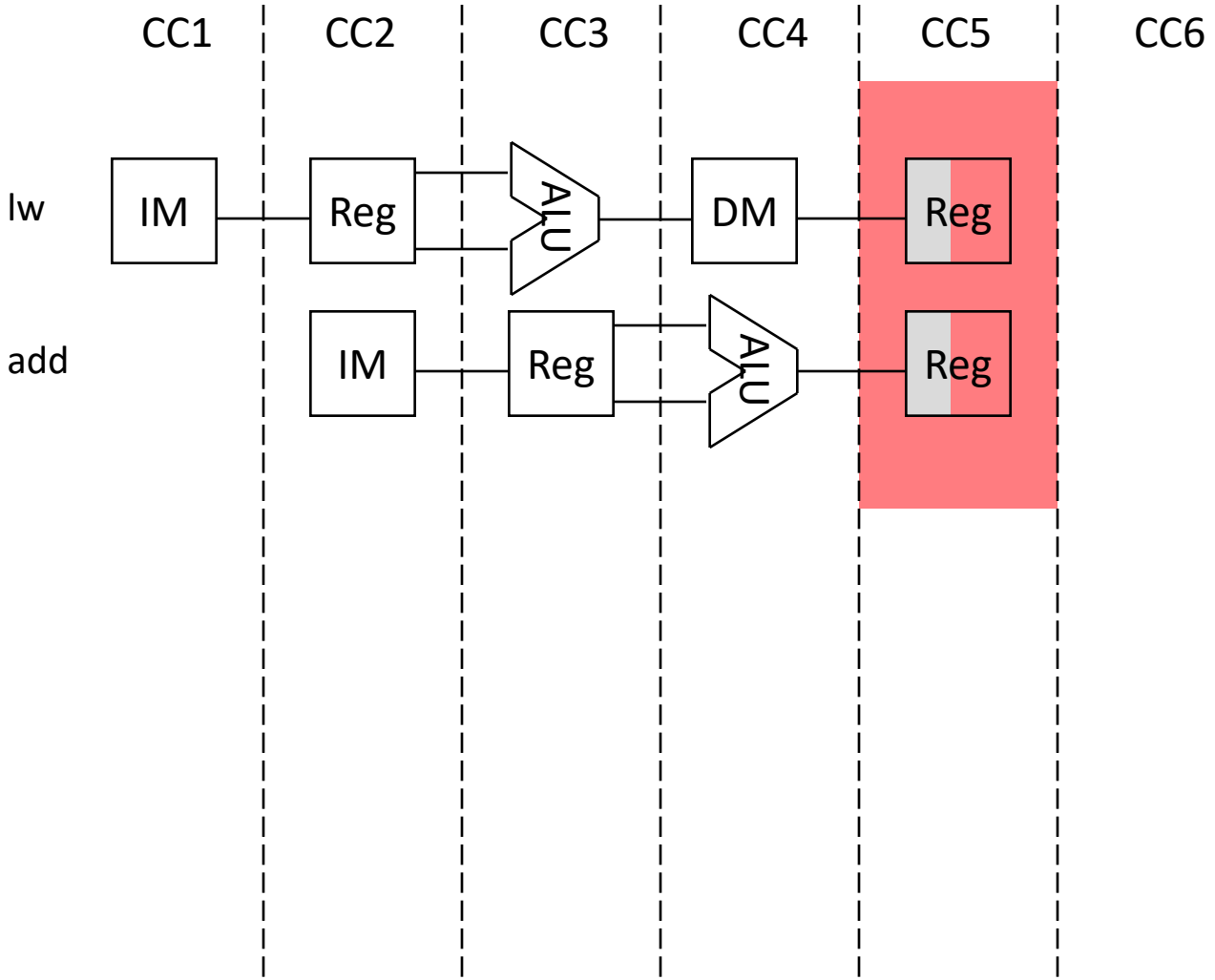
Pipeline Stages

Should we force every instruction to go through all 5 stages? Can we break it up, with R-type taking 4 cycles instead of 5?

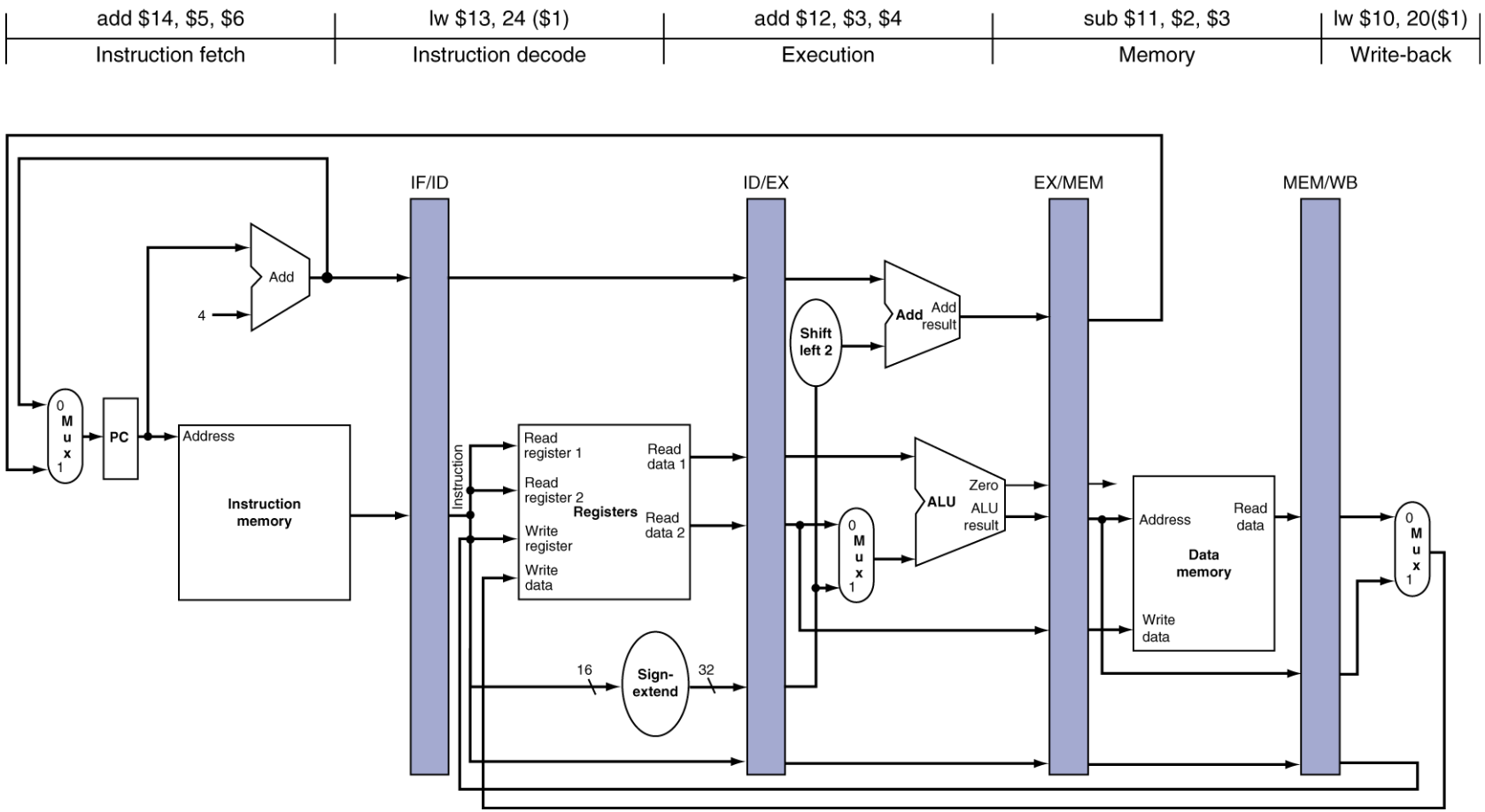
Selection	Yes/No	Reason (Choose BEST answer)
A	Yes	Decreasing R-type to 4 cycles improves instruction throughput
B	Yes	Decreasing R-type to 4 cycles improves instruction latency
C	No	Decreasing R-type to 4 cycles causes hazards
D	No	Decreasing R-type to 4 cycles causes hazards and doesn't impact throughput
E	No	Decreasing R-type to 4 cycles causes hazards and doesn't impact latency

Mixed Instructions in the Pipeline

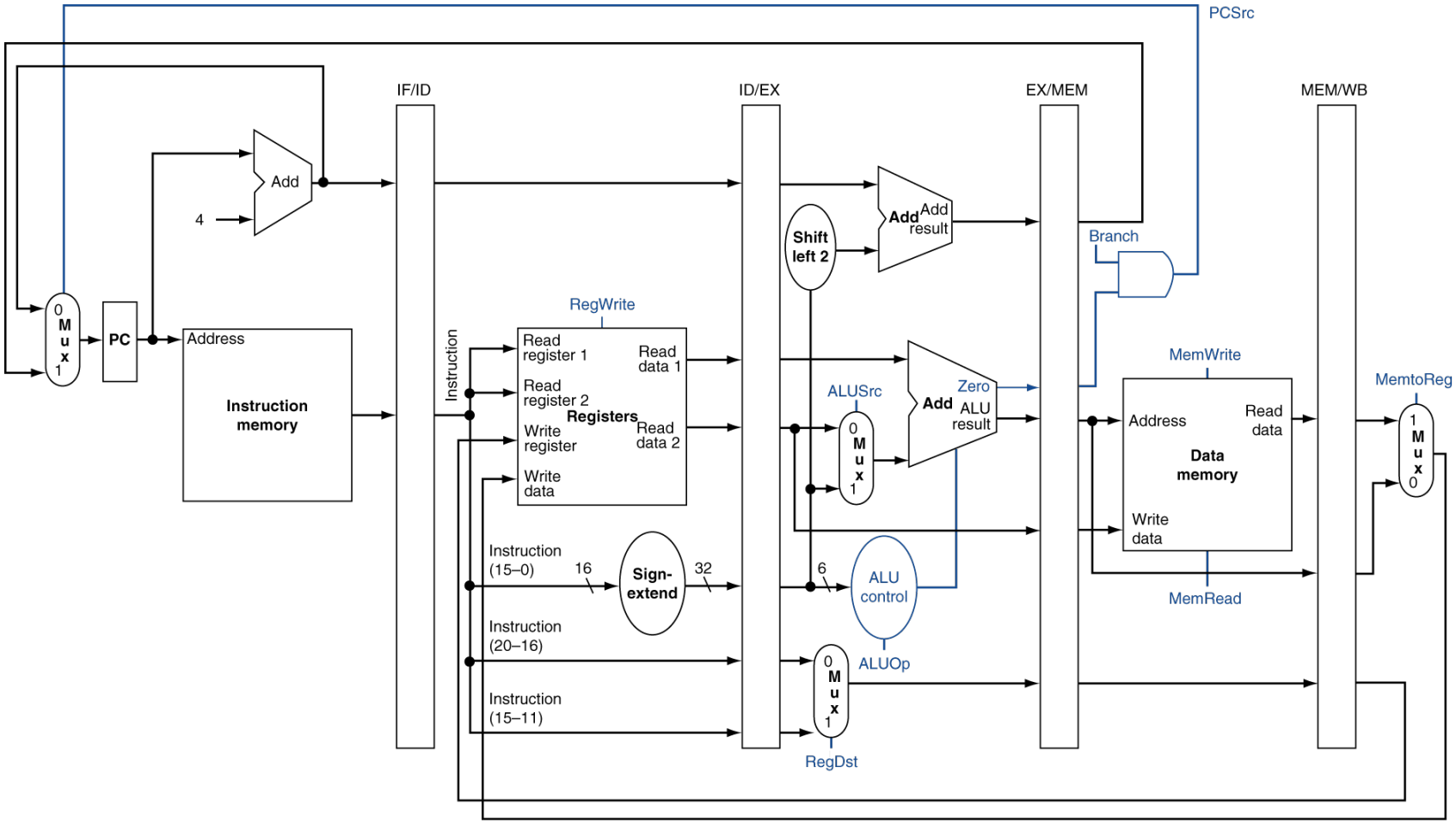


Single-Cycle Pipeline Diagram

- State of pipeline in a given cycle



Pipelined Control



How do we control our pipelined CPU?

A. We need to add new control signals.

B. We need to forward the control values to the correct stage.

C. We don’t need to do anything special; it will work the way it is.

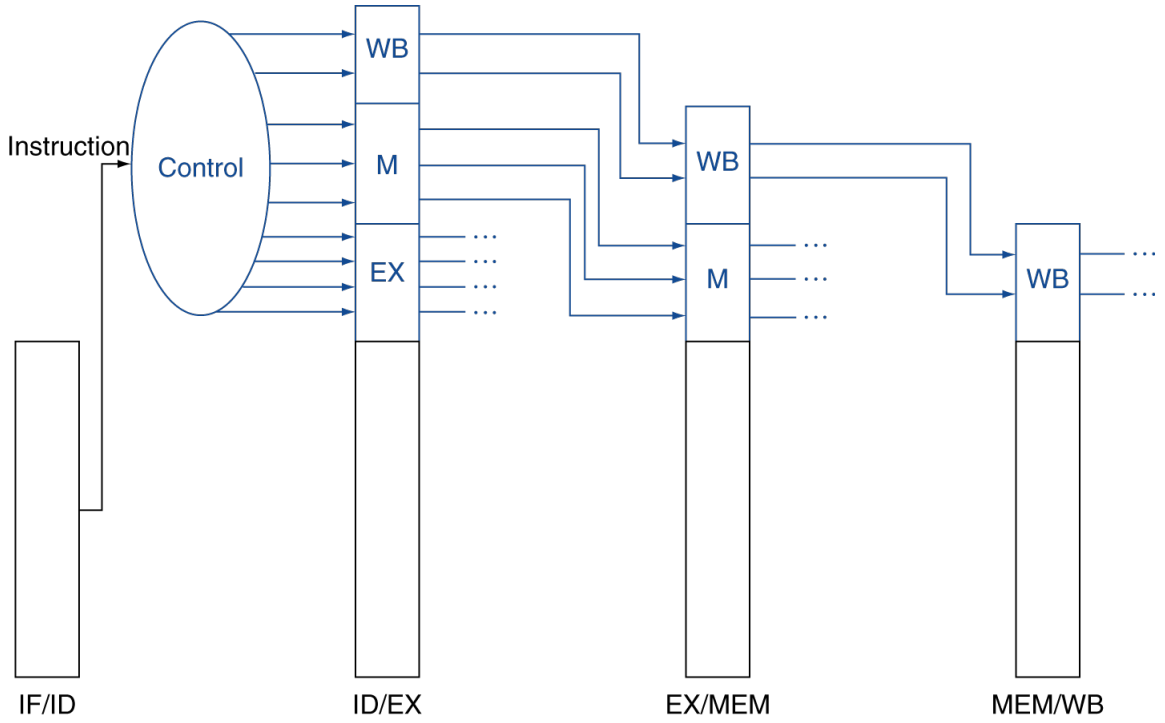
Pipeline Control

- IF Stage: read Instr Memory (always asserted) and write PC (on System Clock)
- ID Stage: no optional control signals to set

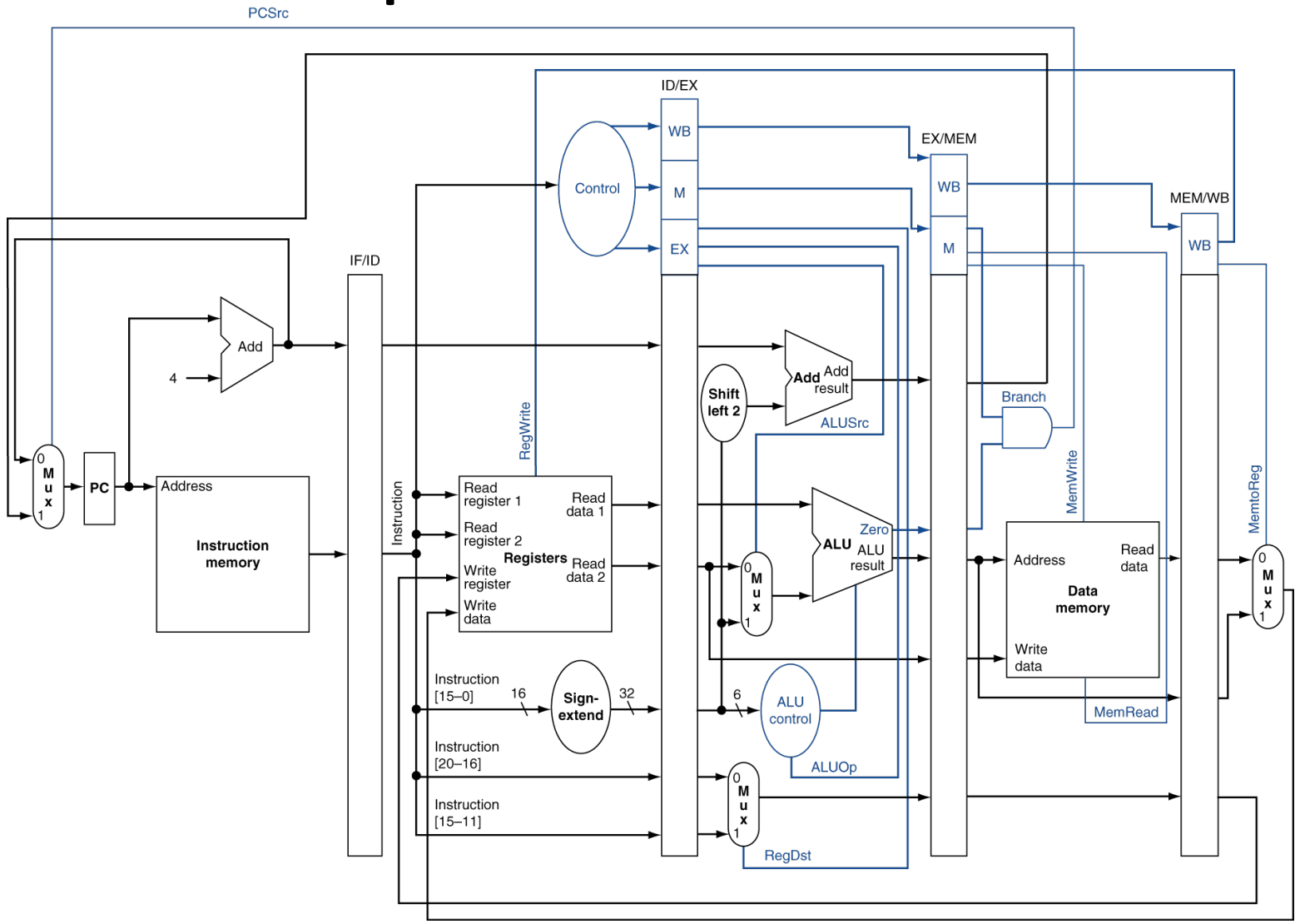
	EX Stage				MEM Stage			WB Stage	
	Reg Dst	ALU Op1	ALU Op0	ALU Src	Brch	Mem Read	Mem Write	Reg Write	Mem toReg
R	1	1	0	0	0	0	0	1	0
`lw`	0	0	0	1	0	1	0	1	1
`sw`	X	0	0	1	0	0	1	0	X
`beq`	X	0	1	0	1	0	0	0	X

Pipelined Control

Control signals derived from instruction



Pipelined Control



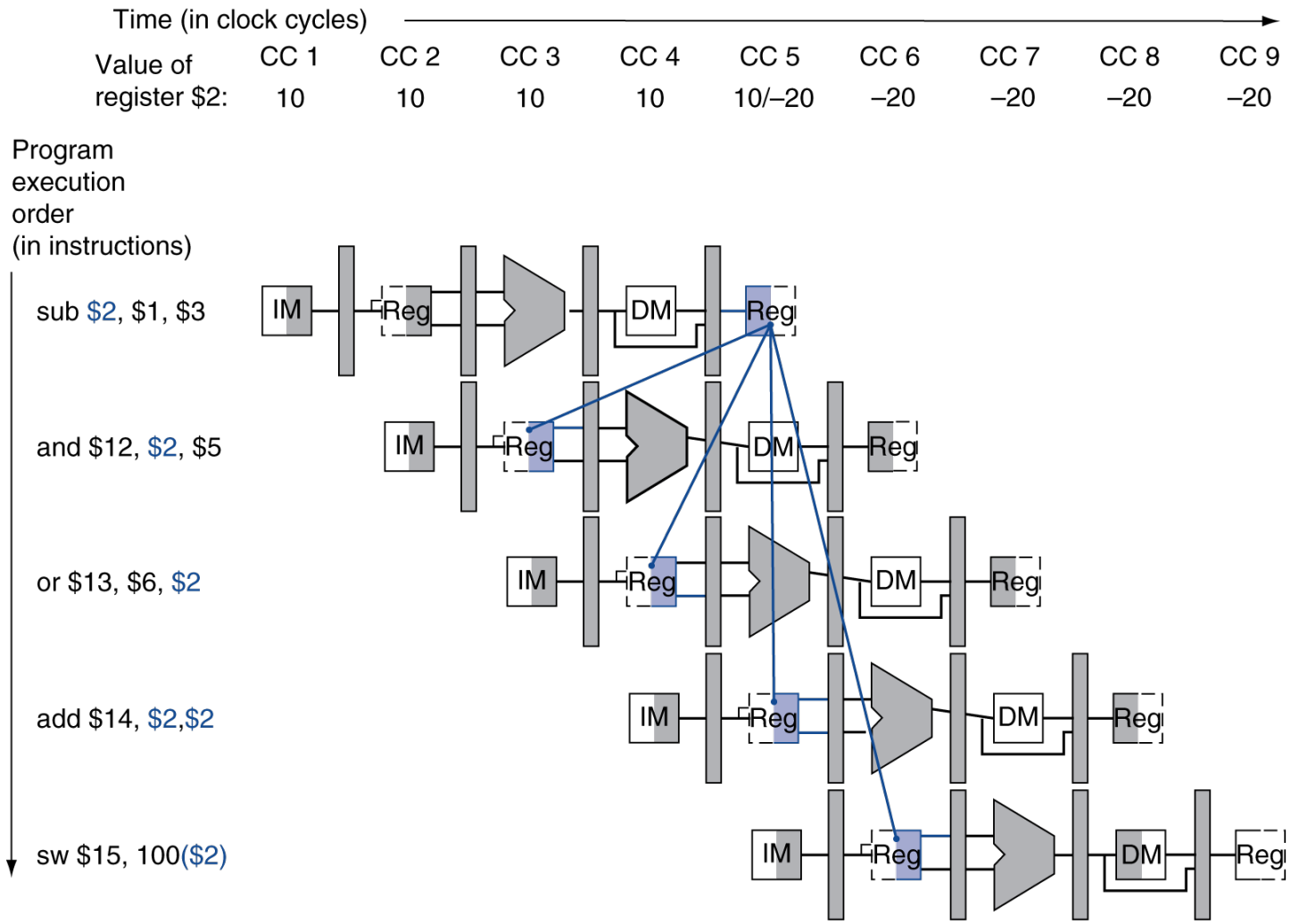
Will we need to add write control signals to our pipeline registers?

A. No, we can automatically write them on the clock cycle

B. Yes, we need to know if there's new information to write

C. Yes, we might not want to overwrite previous values

Dependencies & Forwarding



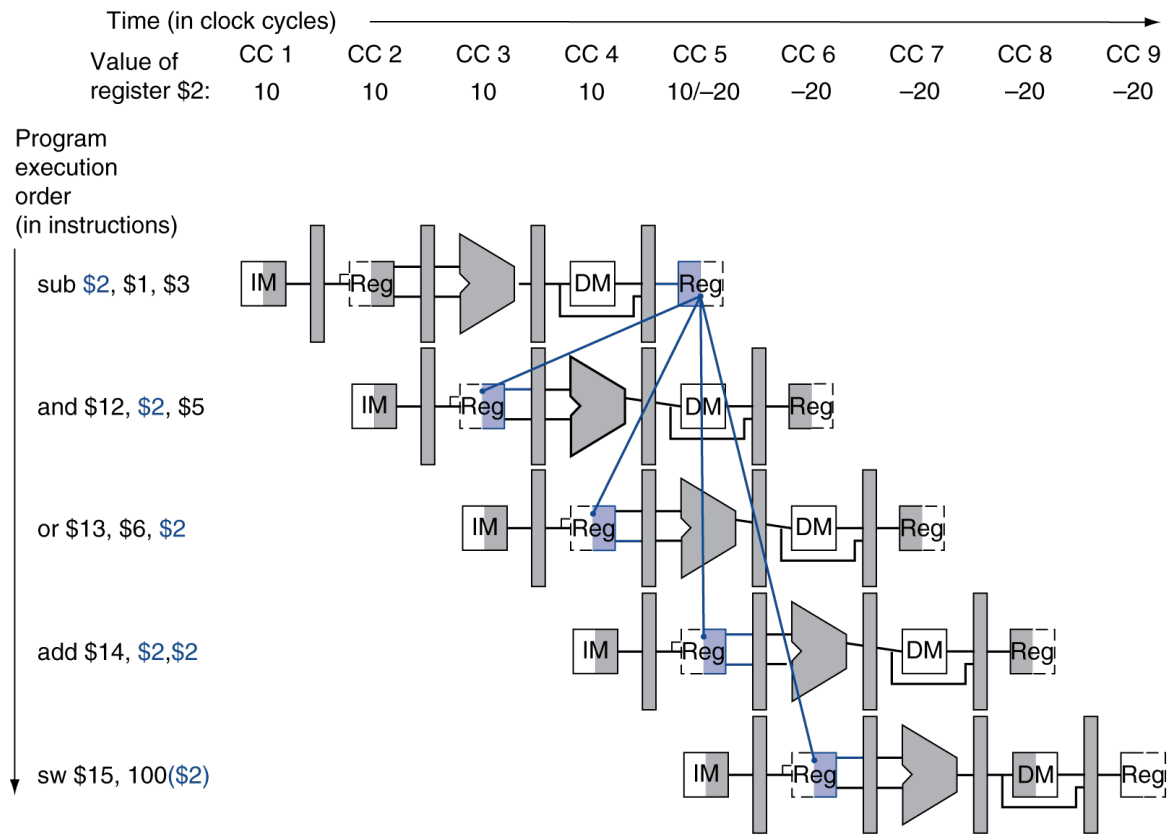
We can BEST solve these data hazards

A. By stalling.

B. By forwarding.

C. By combining forwards and stalls.

D. By doing something else.



Data Hazards in ALU Instructions

- Consider this sequence:

```
sub $2, $1,$3
and $12,$2,$5
or  $13,$6,$2
add $14,$2,$2
sw  $15,100($2)
```

- We can resolve hazards with forwarding
  - How do we detect when to forward?

Reading

- Next lecture: Data Hazards
  - Section 5.8