

# CSCI 210: Computer Architecture

## Lecture 29: More Pipelining

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Slides from Cynthia Taylor

# Announcements

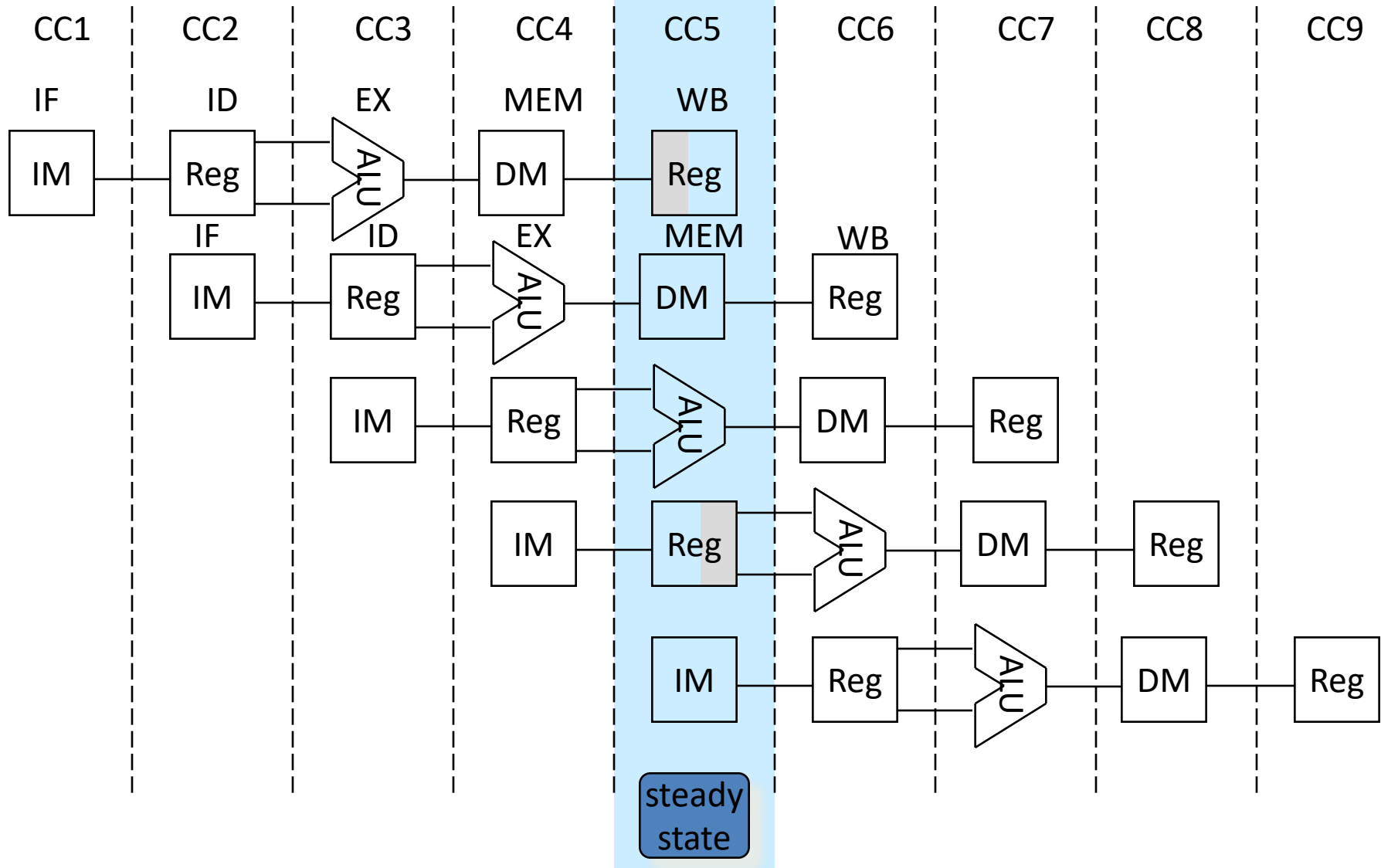
- Problem Set 9 due Friday
- Lab 8 due Sunday, January 2, 2022
- Office hours Friday 13:30–14:30

# MIPS Pipeline

Five stages, one step per stage, one clock cycle per stage

1. IF: Instruction fetch from memory
2. ID: Instruction decode & register read
3. EX: Execute operation or calculate address
4. MEM: Access memory operand
5. WB: Write result back to register

# Execution in a Pipelined Datapath



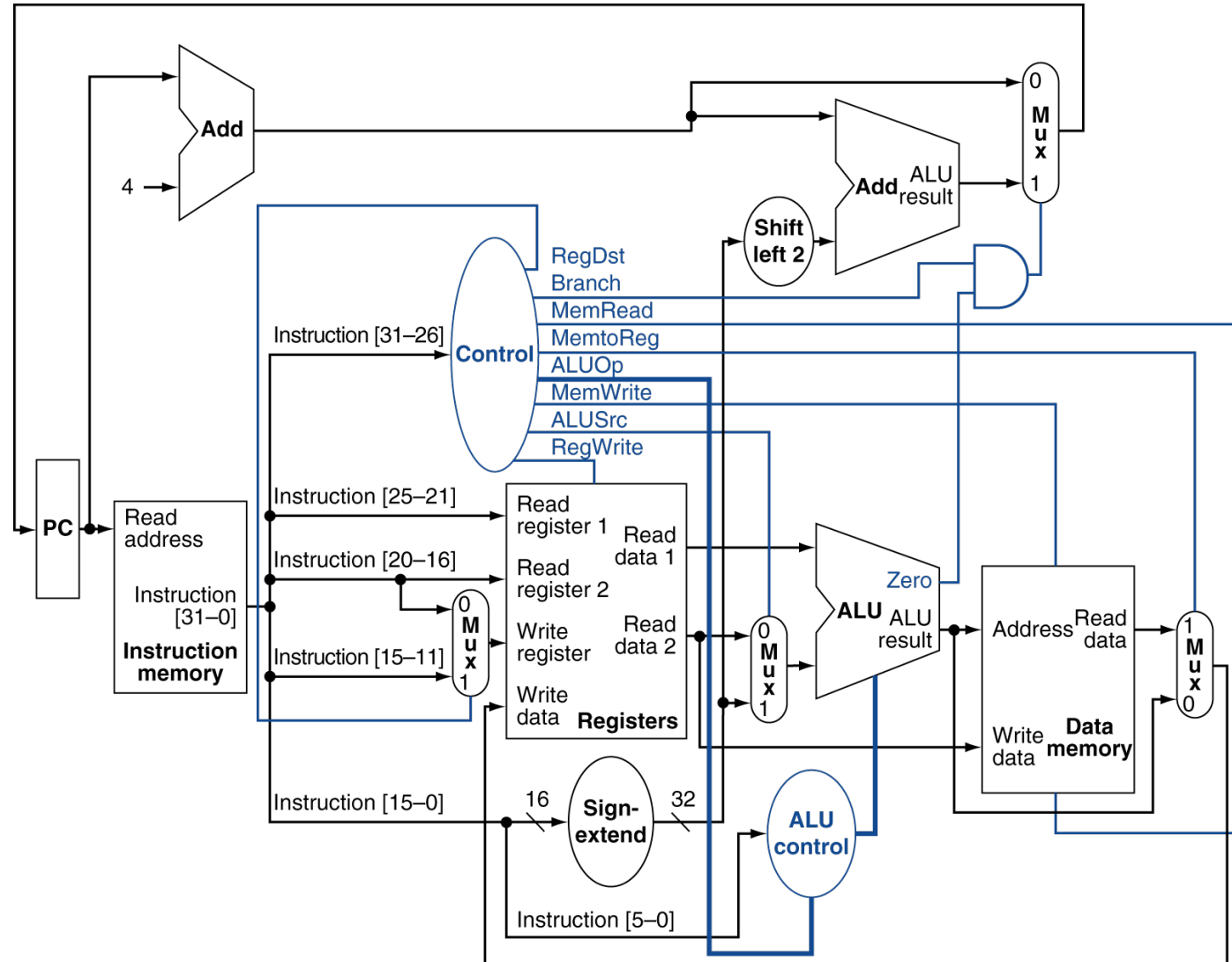
We can perform a register read and a register write in the same cycle. Which should we do first?

A. Read

B. Write

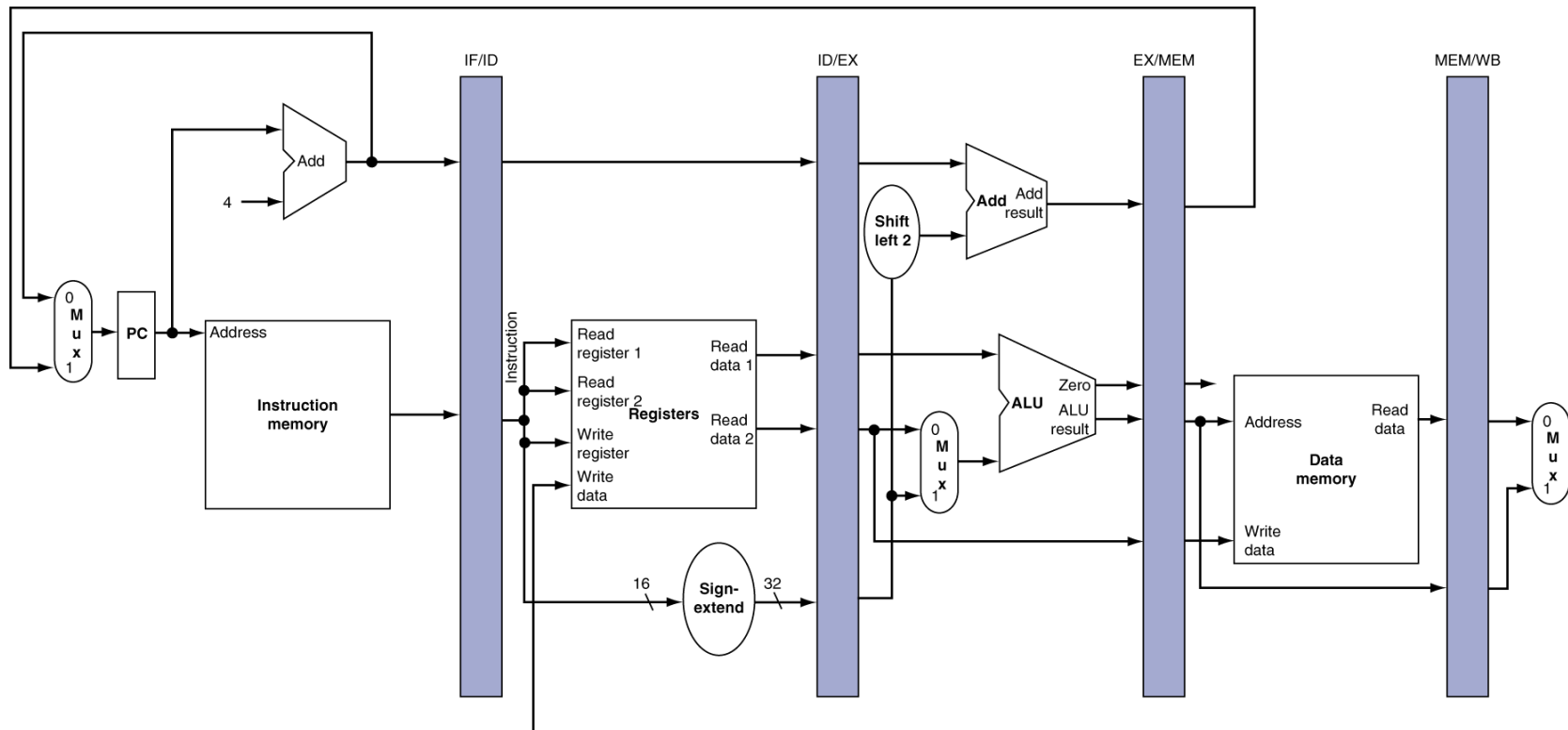
C. It doesn't matter

# Single Cycle Datapath

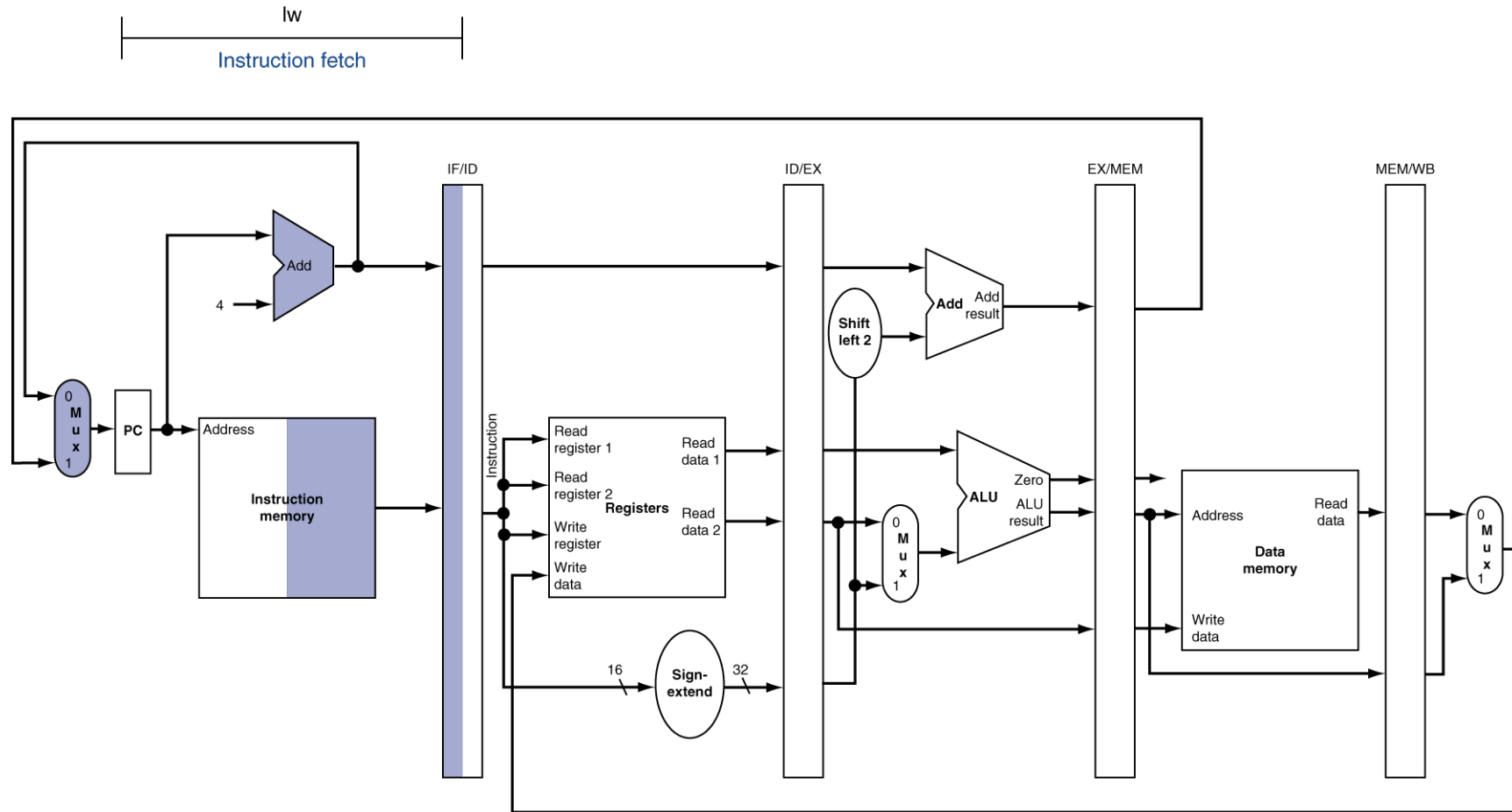


# Pipeline registers

- Need registers between stages
  - To hold information produced in previous cycle

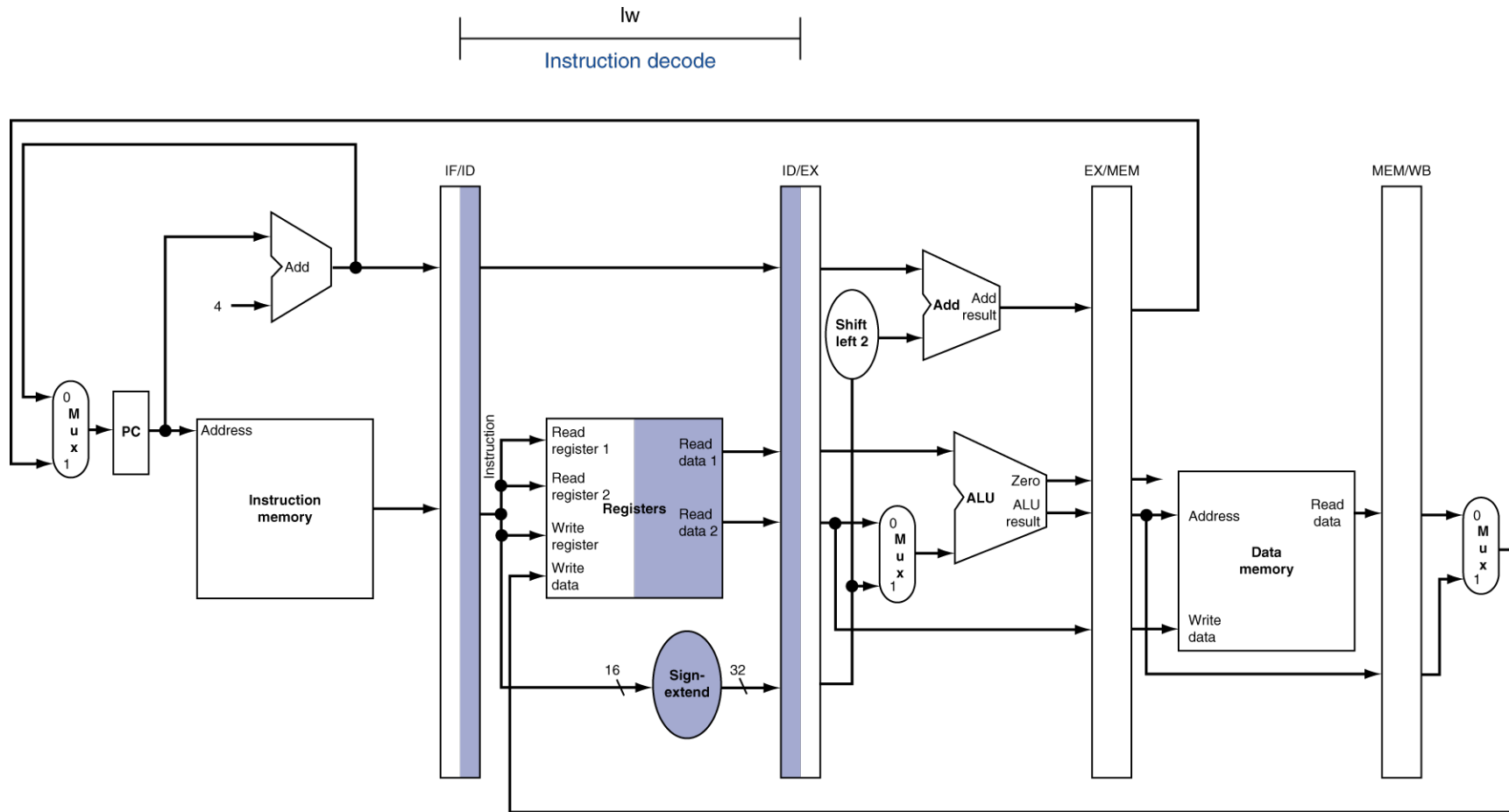


# IF for Load, Store, ...





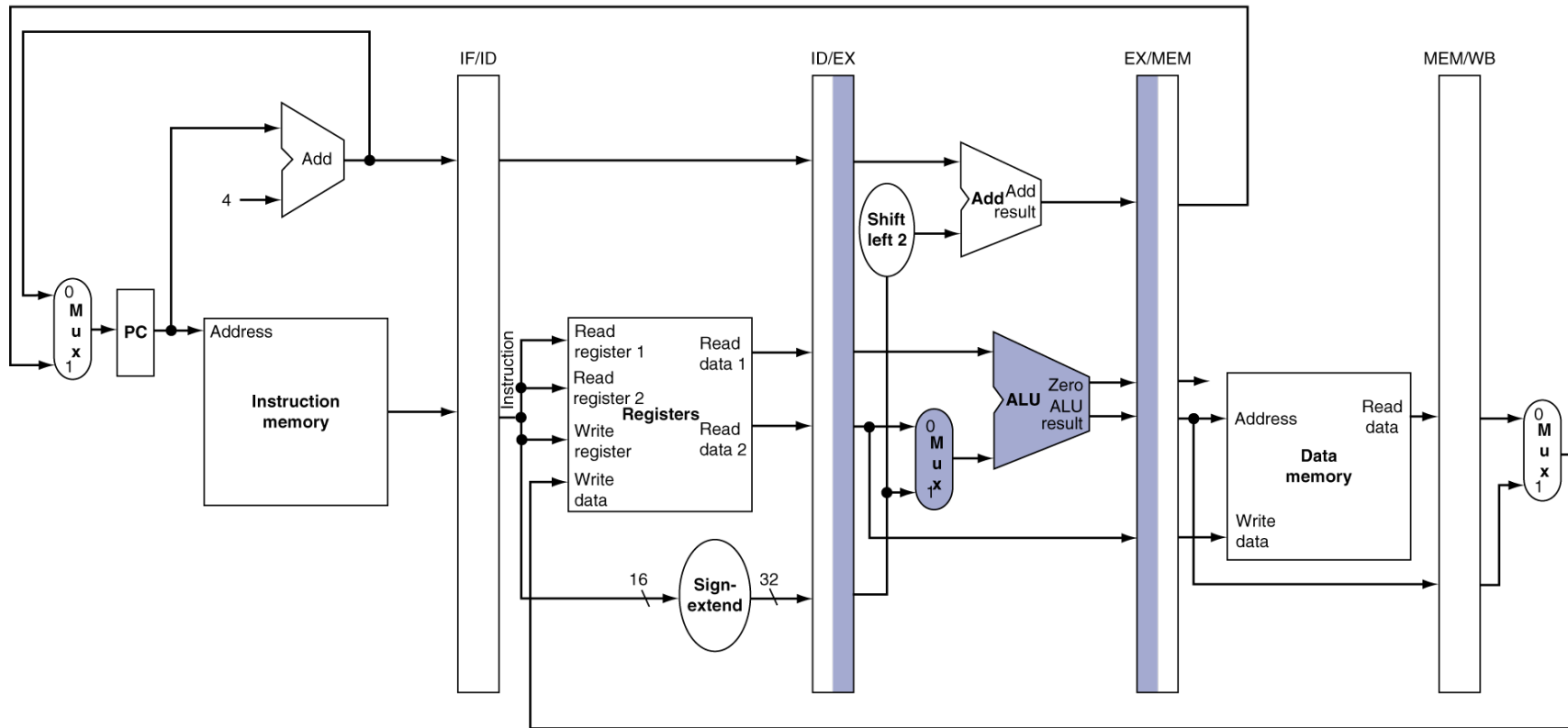
# ID for Load, Store, ...



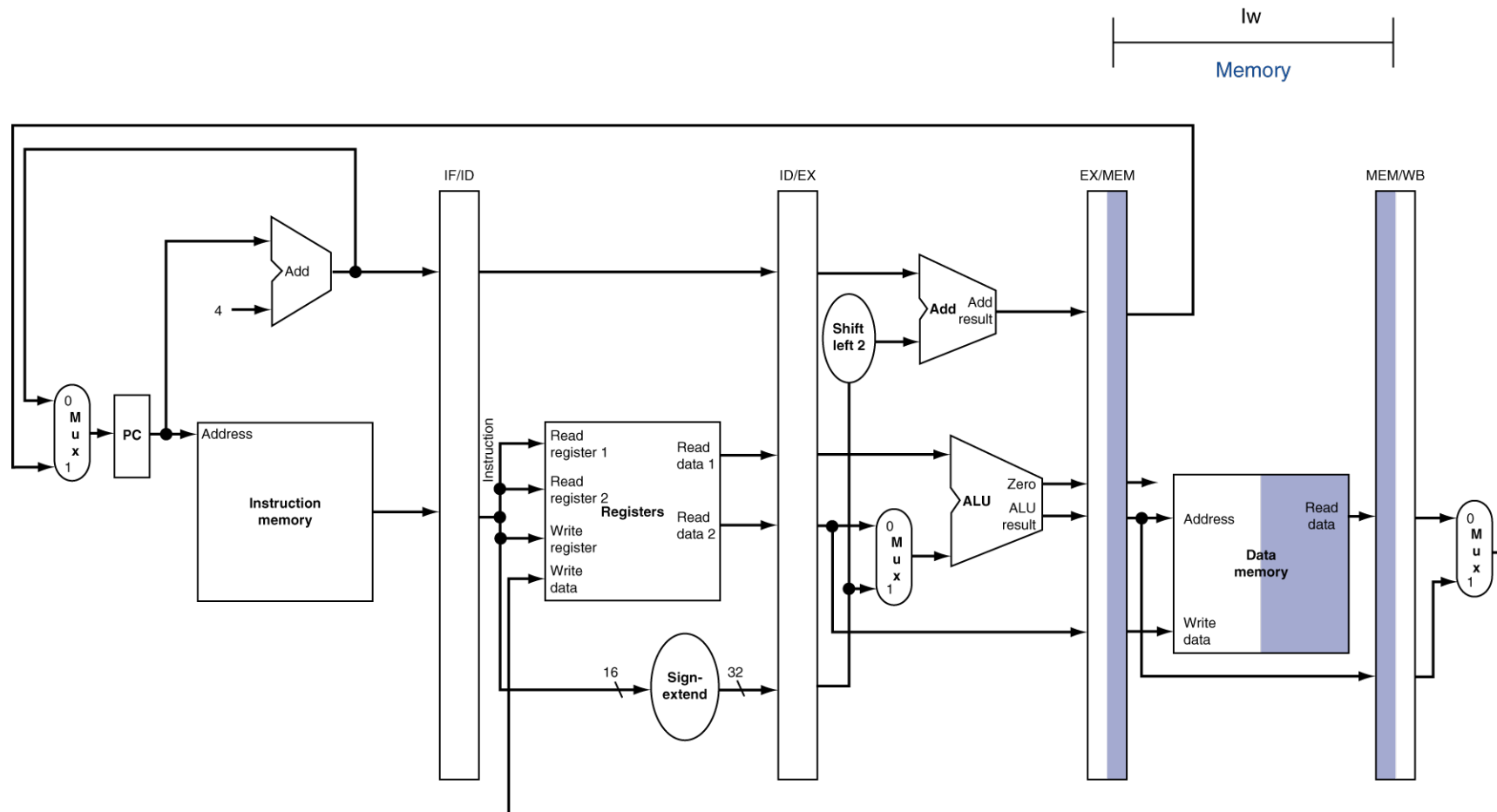
The register file will output data from both read registers, but load will only use one of them. We should

- A. Save both of them in ID/EX
- B. Only save the one we will use in ID/EX
- C. Do something else

# EX for Load

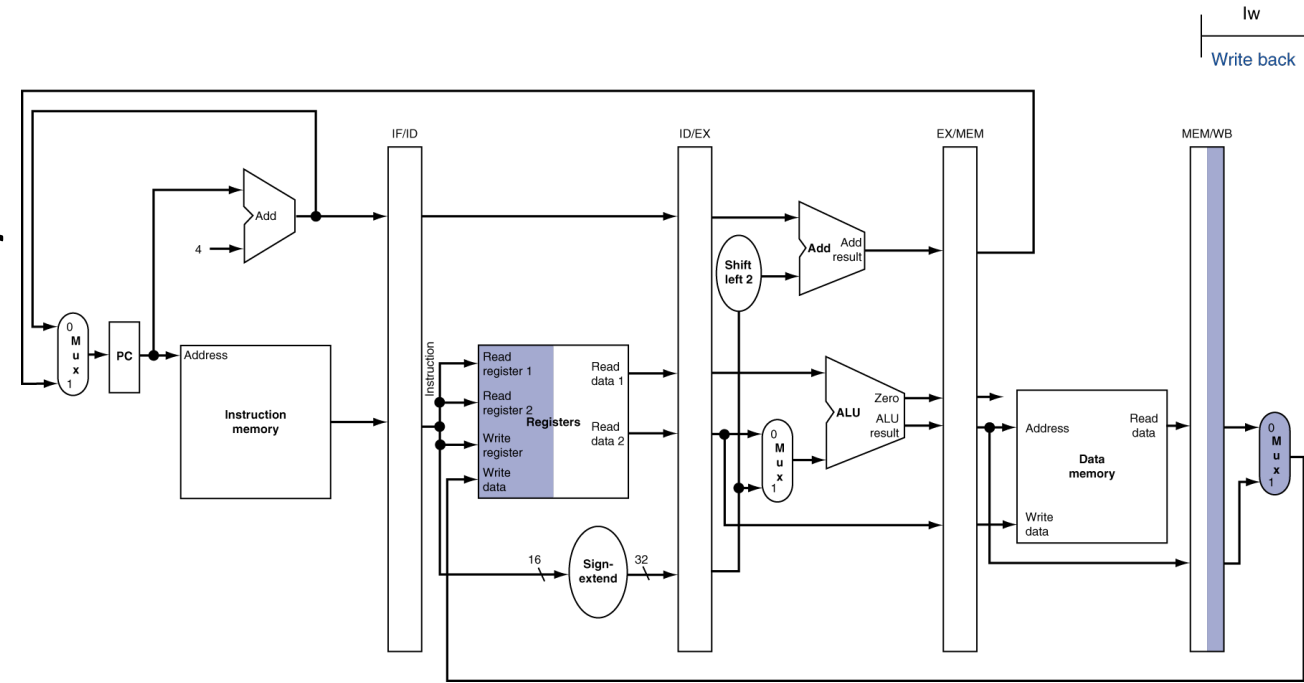


# MEM for Load

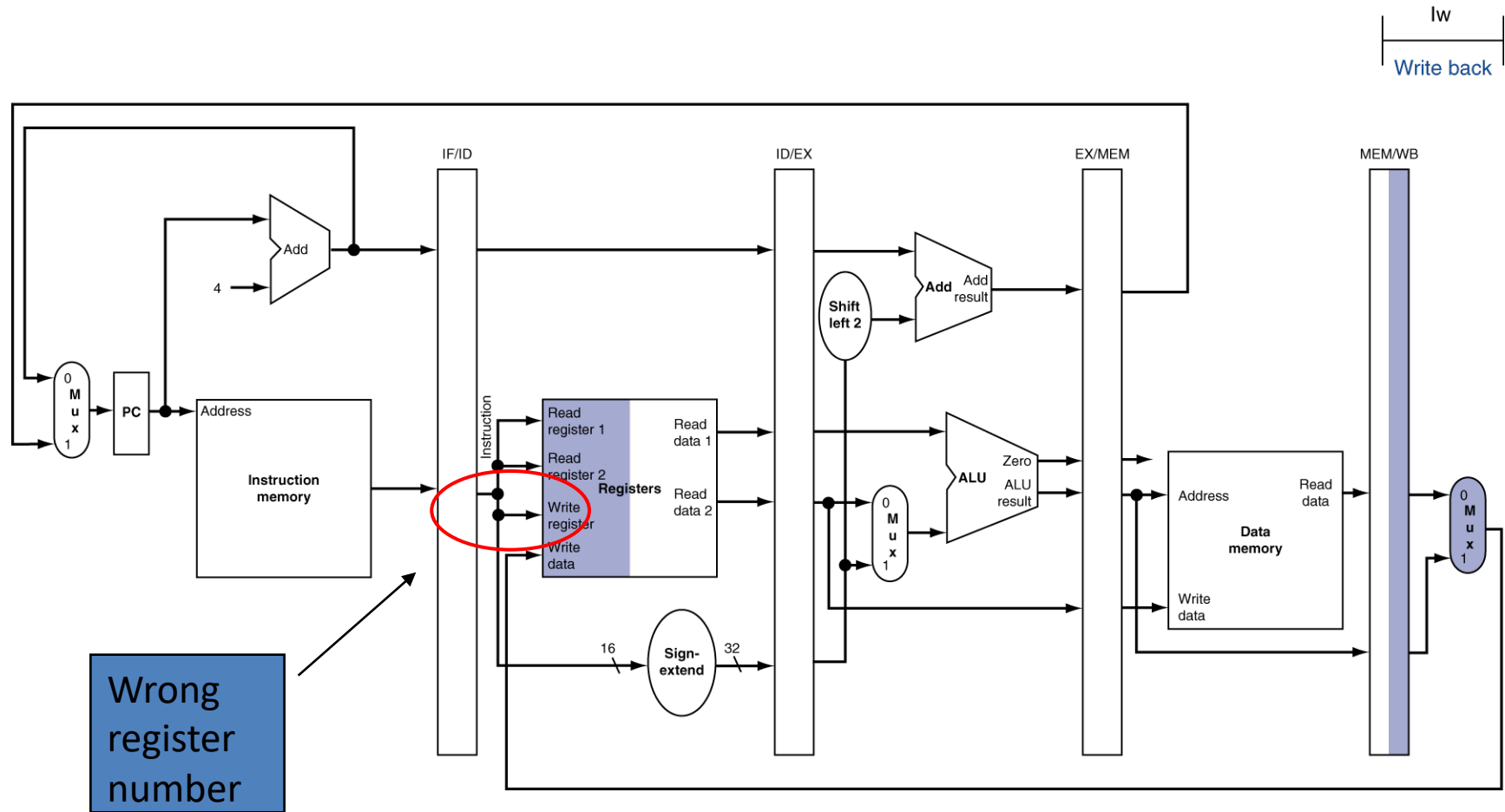


# When we do WB for load

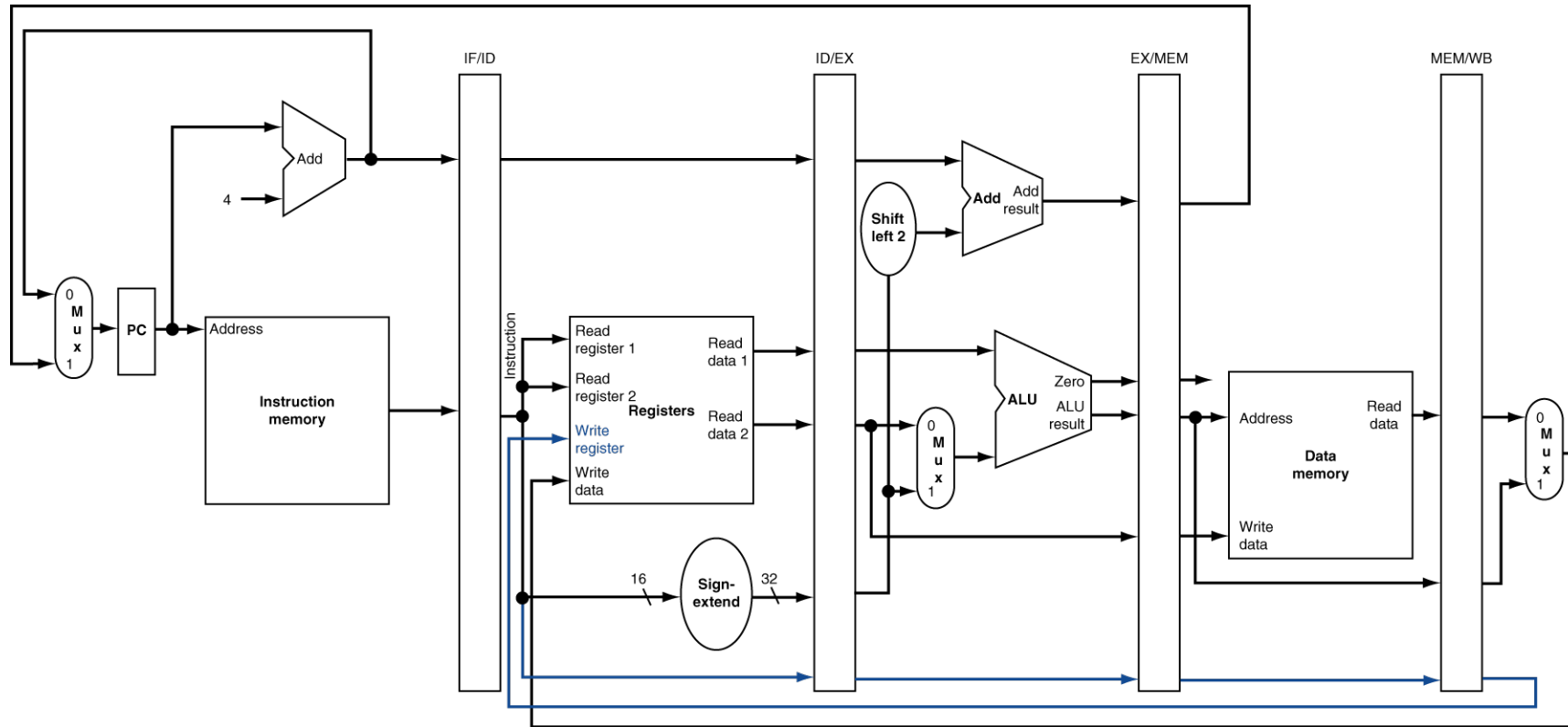
- A. Everything will be fine
- B. The data to write to the register will be wrong
- C. The register number to write to will be wrong



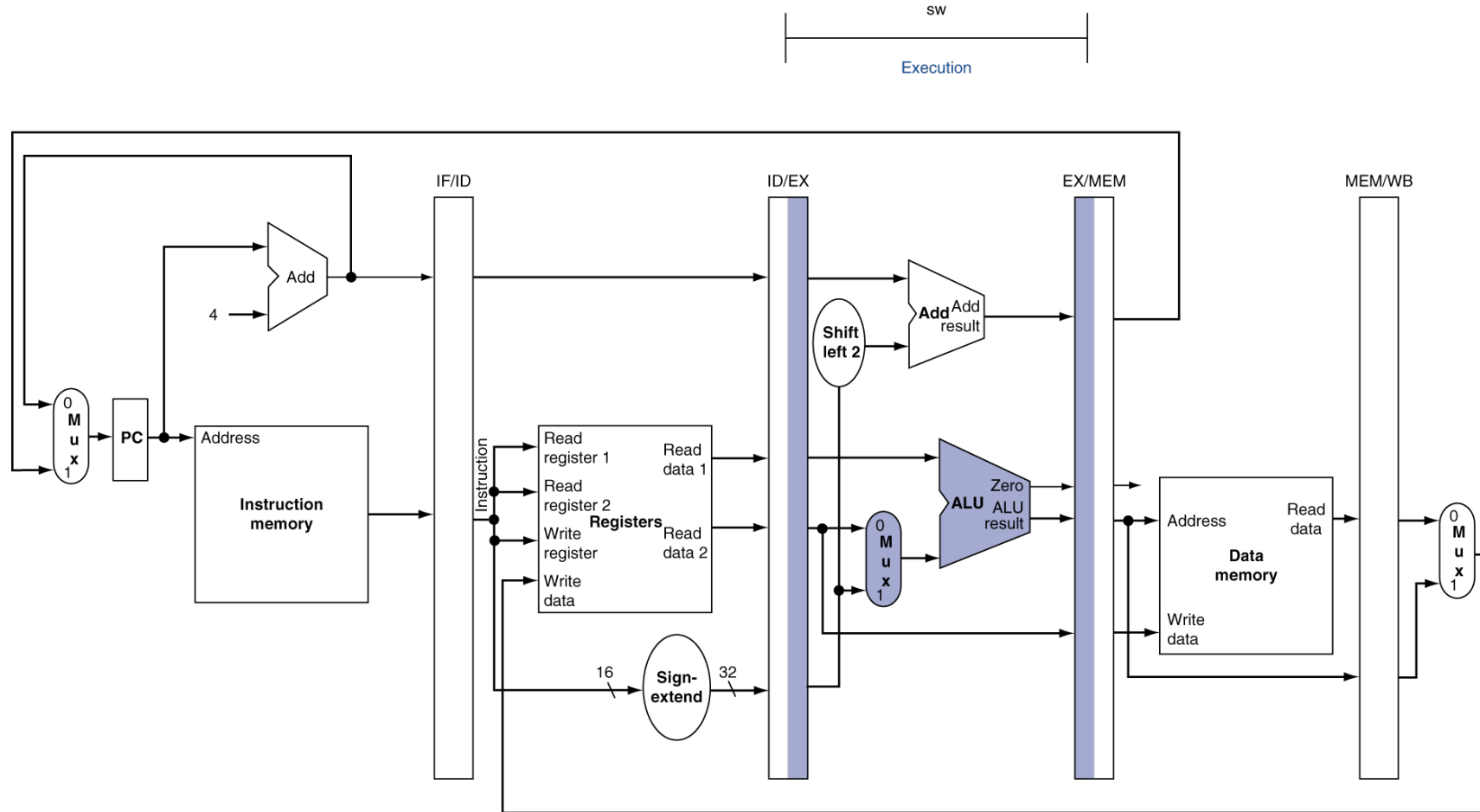
# WB for Load



# Corrected Datapath for Load

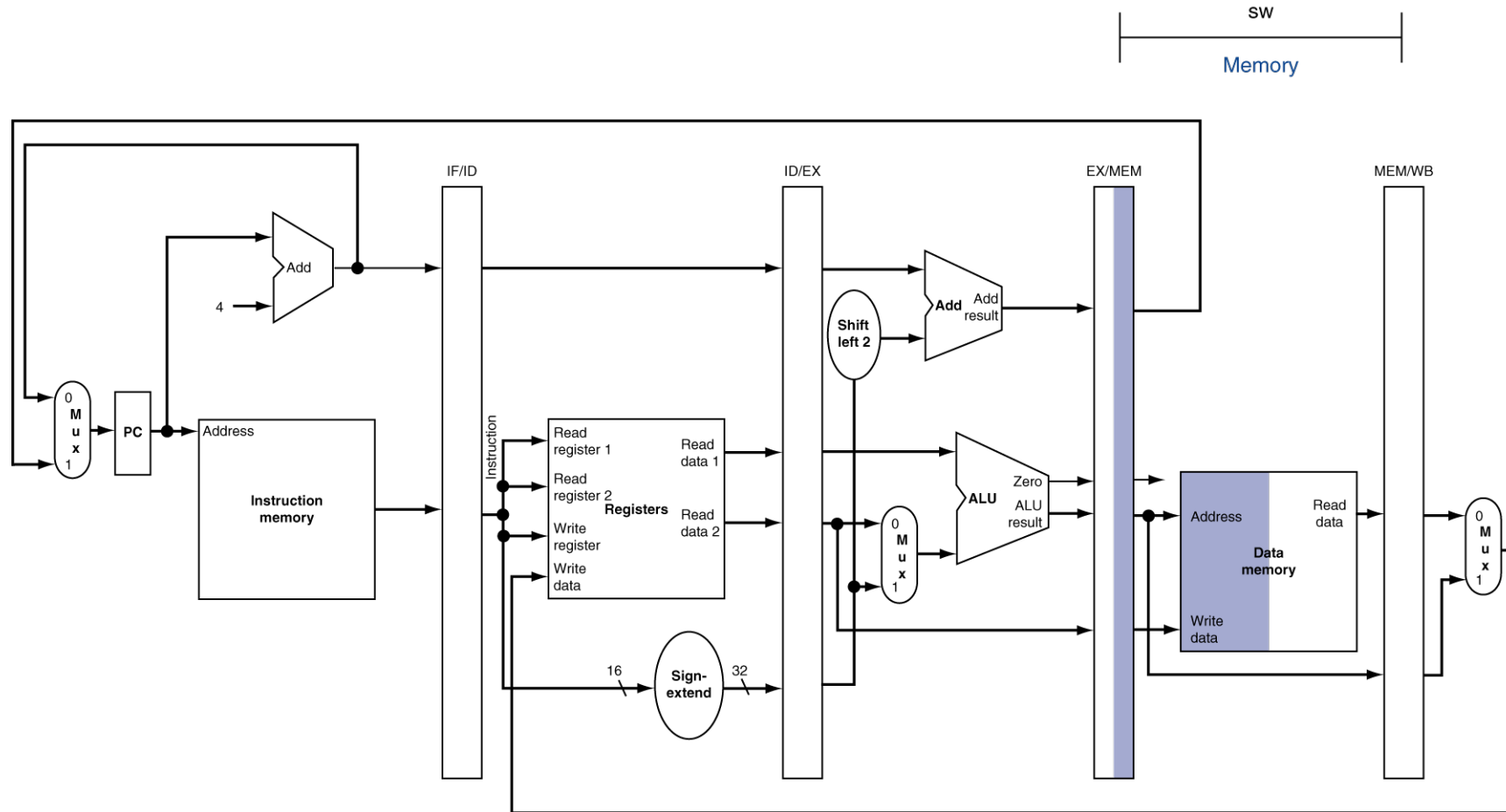


# EX for Store

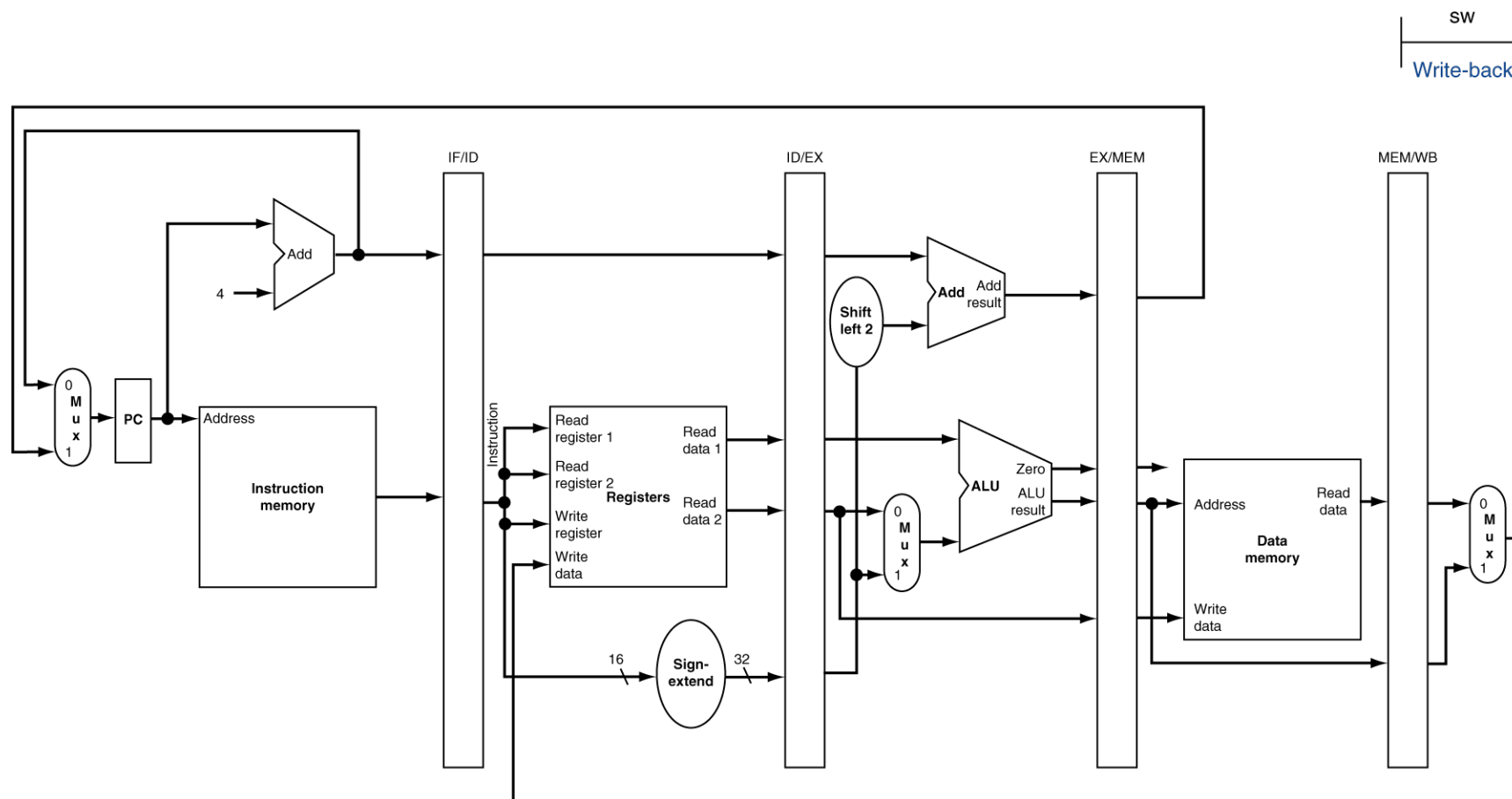




# MEM for Store



# WB for Store



# Reading

- Next lecture: Pipelined Datapath
  - Section 5.7
- Problem Set 10 due Friday
- Lab 8 due Monday