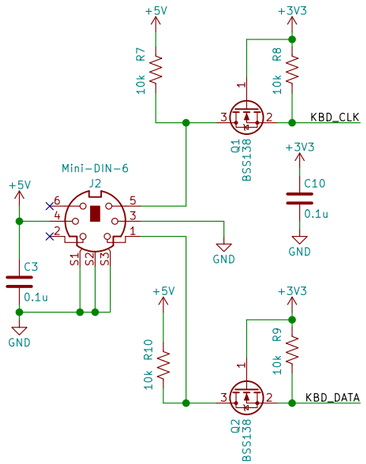
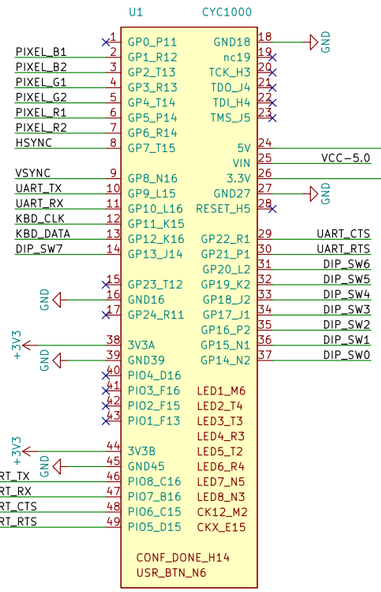
PS-2 Keyboards run on 5 volts, and the signals are open-collector.
We so far have no reason to drive them, but we do have to
level-shift them down to 3.3 volts for the FPGA. Our level-shifters
are bidirectional, so we can drive the keyboard, if we ever need to.

The keyboard provides the clock to the FPGA.

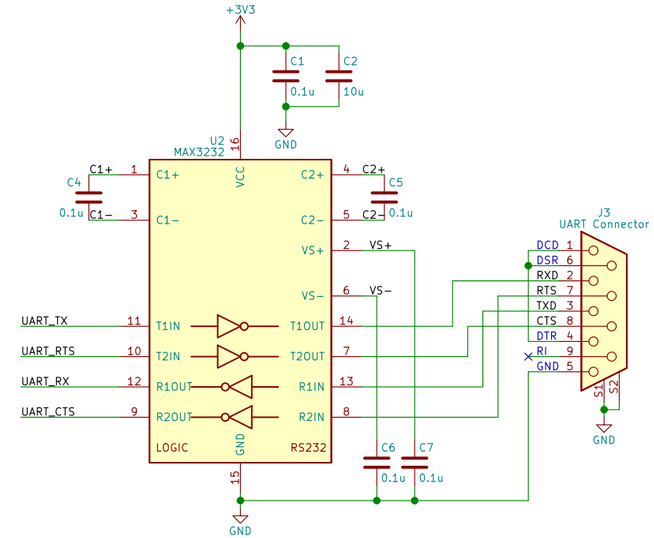


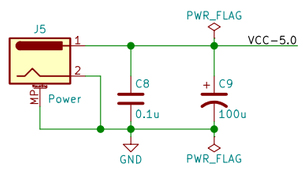


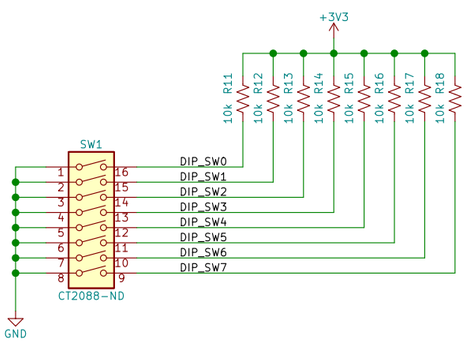
I've tried three VGA monitors and they all are able to sync with 3.3 volts
on H and V sync.

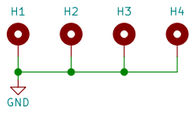
The pixel inputs should be 75 ohms, and need 0.7 volts to drive to full
brightness. 0.0 represents black.

We provide a cheesy D/A consisting of a few resistors per color.
Currently, I see no need for this, but if we ever support grayscale, it might be handy.









Signal names at the J3 UART Connector are named from the perspective
of the DTE to which we are connected, and are therefore backwards
with respect to our FPGA!

We are wired as a DCE (i.e., like a modem). We connect to a DTE (PC or
other computer) with a straight cable. However, the PiDP-11 is also
wired as a DCE, so we need a null-modem cable with it.

We receive data from the DTE on pin 3 (DTE TXD becomes our
UART_RX), and we transmit data to the DTE on pin 2 (our UART_TX
becomes DTE RXD).

Similarly, our UART_RTS signal becomes the DTE CTS signal on pin 8,
and the DTS RTS signal on pin 7 becomes our UART_CTS signal.

We deassert our UART_RTS when our receive buffer becomes too full.

Falco Engineering

Sheet: /		
File: terminal.sch		
Title: ASCII Terminal		
Size: B	Date: 2021-03-11	**Rev: 1**
KiCad E.D.A. kicad 5.1.9-1.fc33		Id: 1/1