STM32 Glossary

A

AHB/APB Bridges (APB)
Category: System Architecture
Definition: Bridges connecting Advanced High-performance Bus (AHB) and Advanced Peripheral Bus (APB).
Manual: Reference Manual, Page 37

AHB1 Peripheral Reset Register (RCC_AHB1RSTR)
Category: Reset and Clock Control (RCC)
Definition: Register controlling the reset of AHB1 peripherals.
Manual: Reference Manual, Page 111

C

Clock Security System (CSS)
Category: Clock System
Definition: A feature ensuring safe operation of the system clock by switching to a backup clock in case of a failure.
Manual: Reference Manual, Page 98

Core Registers
Category: Processor Model
Definition: Registers directly managed by the Cortex-M4 processor, including general-purpose and special-purpose registers.
Manual: Programming Manual, Page 17

D

DMA Peripheral Bus
Category: System Architecture
Definition: The bus used by the Direct Memory Access (DMA) controller to access peripherals.
Manual: Reference Manual, Page 37

F

Fault Status Registers (FSR)
Category: Fault Handling
Definition: Registers holding fault status information when an exception occurs.

Manual: Programming Manual, Page 46

M

Memory Protection Unit (MPU)
Category: Core Peripherals
Definition: A unit used to enforce memory access permissions to protect memory regions from unauthorized access.
Manual: Programming Manual, Page 192

Memory Management Fault Address Register (MMFAR)
Category: Fault Handling
Definition: Register storing the address of the memory access that caused a memory management fault.
Manual: Programming Manual, Page 241

S

SysTick Timer (STK)
Category: Core Peripherals
Definition: A timer used for generating a system tick or delay, useful for OS tick generation or event timing.
Manual: Programming Manual, Page 245