Programming Manual Part 2

Contents

Content

1.	${\it General}$	data processing instructions	80
2.	Core per	ripherals	192
	(a) Abo	out the STM32 Cortex-M4 core peripherals	192
	(b) Mei	mory protection unit (MPU)	192
	i.	MPU access permission attributes	194
	ii.		
	iii.	Updating an MPU region	195
		MPU design hints and tips	
	v.	MPU type register (MPU_TYPER)	199
	vi.	MPU control register (MPU_CTRL)	200
	vii.	MPU region number register (MPU_RNR)	201
	viii.	MPU region base address register (MPU_RBAR)	202
	ix.	MPU region attribute and size register (MPU_RASR) \dots	203
	x.	MPU register map	205
	(c) Nested vectored interrupt controller (NVIC)		
	i.	Accessing the Cortex-M4 NVIC registers using CMSIS \ldots	208
	ii.	Interrupt set-enable registers (NVIC_ISERx) \hdots	209
	iii.	Interrupt clear-enable registers (NVIC_ICERx) \hdots	210
	iv.	Interrupt set-pending registers (NVIC_ISPRx)	211
	v.	Interrupt clear-pending registers (NVIC_ICPRx)	212
	vi.	Interrupt active bit registers (NVIC_IABRx) \hdots	213
	vii.	Interrupt priority registers (NVIC_IPRx)	214
	viii.	Software trigger interrupt register (NVIC_STIR)	215
		Level-sensitive and pulse interrupts	
	х.	NVIC design hints and tips	217
	xi.	NVIC register map	218
	(d) System control block (SCB)		
	i.	Auxiliary control register (ACTLR)	221
	ii.	CPUID base register (CPUID)	223
	iii.	Interrupt control and state register (ICSR)	224
	iv.	Vector table offset register (VTOR)	226
	v.	Application interrupt and reset control register (AIRCR)	227

vi.	System control register (SCR)	229
vii.	Configuration and control register (CCR)	.230
viii.	System handler priority registers (SHPRx)	232
ix.	System handler control and state register (SHCSR)	234
X.	Configurable fault status register (CFSR; UFSR+BFSR+MN 236	MFSR)
xi.	Usage fault status register (UFSR)	237
xii.	Bus fault status register (BFSR)	238
xiii.	Memory management fault address register (MMFSR) \dots	239
xiv.	Hard fault status register (HFSR)	240
XV.	Memory management fault address register (MMFAR) $ \ldots $	241
xvi.	Bus fault address register (BFAR)	241
xvii.	Auxiliary fault status register (AFSR)	242
xviii.	System control block design hints and tips	242
xix.	SCB register map	243
(e) Sys	Tick timer (STK)	245
i.	SysTick control and status register (STK_CTRL) $\ldots \ldots$	246
ii.	SysTick reload value register (STK_LOAD)	247
iii.	SysTick current value register (STK_VAL)	. 248
iv.	SysTick calibration value register (STK_CALIB) \hdots	249
v.	SysTick design hints and tips	249
vi.	SysTick register map	250
(f) Flo	ating point unit (FPU)	251
i.	Coprocessor access control register (CPACR)	252
ii.	Floating-point context control register (FPCCR)	252
iii.	Floating-point context address register (FPCAR)	254
iv.	Floating-point status control register (FPSCR)	254
v.	Floating-point default status control register (FPDSCR)	256
vi.	Enabling the FPU	256
vii.	Enabling and clearing FPU exception interrupts	257