Programming Manual

Contents

Content

1. Typographical conventions 12
2. List of abbreviations for registers 12
3. About the STM32 Cortex-M4 processor and core peripherals 13
   (a) System level interface 14
   (b) Integrated configurable debug 14
   (c) Cortex-M4 processor features and benefits summary 14
   (d) Cortex-M4 core peripherals 15
4. The Cortex-M4 processor 16
   (a) Programmers model 16
      i. Processor mode and privilege levels for software execution .. 16
      ii. Stacks 16
      iii. Core registers 17
      iv. Exceptions and interrupts 25
      v. Data types 25
      vi. The Cortex microcontroller software interface standard (CMSIS) 25
   (b) Memory model 27
      i. Memory regions, types and attributes 28
      ii. Memory system ordering of memory accesses 28
      iii. Behavior of memory accesses 29
      iv. Software ordering of memory accesses 30
      v. Bit-banding 31
      vi. Memory endianness 33
      vii. Synchronization primitives 33
      viii. Programming hints for the synchronization primitives 35
   (c) Exception model 36
      i. Exception states 36
      ii. Exception types 36
      iii. Exception handlers 38
      iv. Vector table 39
      v. Exception priorities 40

vi. Interrupt priority grouping 40
vii. Exception entry and return 41
(d) Fault handling 43
i. Fault types 44
ii. Fault escalation and hard faults 45
iii. Fault status registers and fault address registers 46
iv. Lockup 46
(e) Power management 46
i. Entering sleep mode 47
ii. Wakeup from sleep mode 47
iii. External event input / extended interrupt and event input ..48
iv. Power management programming hints 48
5. The STM32 Cortex-M4 instruction set 49
(a) Instruction set summary 49
(b) CMSIS intrinsic functions 57
(c) About the instruction descriptions 59
i. Operands 59
ii. Restrictions when using PC or SP 59
iii. Flexible second operand 59
iv. Shift operations 61
v. Address alignment 64
vi. PC-relative expressions 64
vii. Conditional execution 64
viii. Instruction width selection 67
(d) Memory access instructions 68
i. ADR 69
ii. LDR and STR, immediate offset 70
iii. LDR and STR, register offset 72
iv. LDR and STR, unprivileged 73
v. LDR, PC-relative 74
vi. LDM and STM 75
vii. PUSH and POP 77
viii. LDREX and STREX 78
ix. CLREX 79
(e) General data processing instructions 80