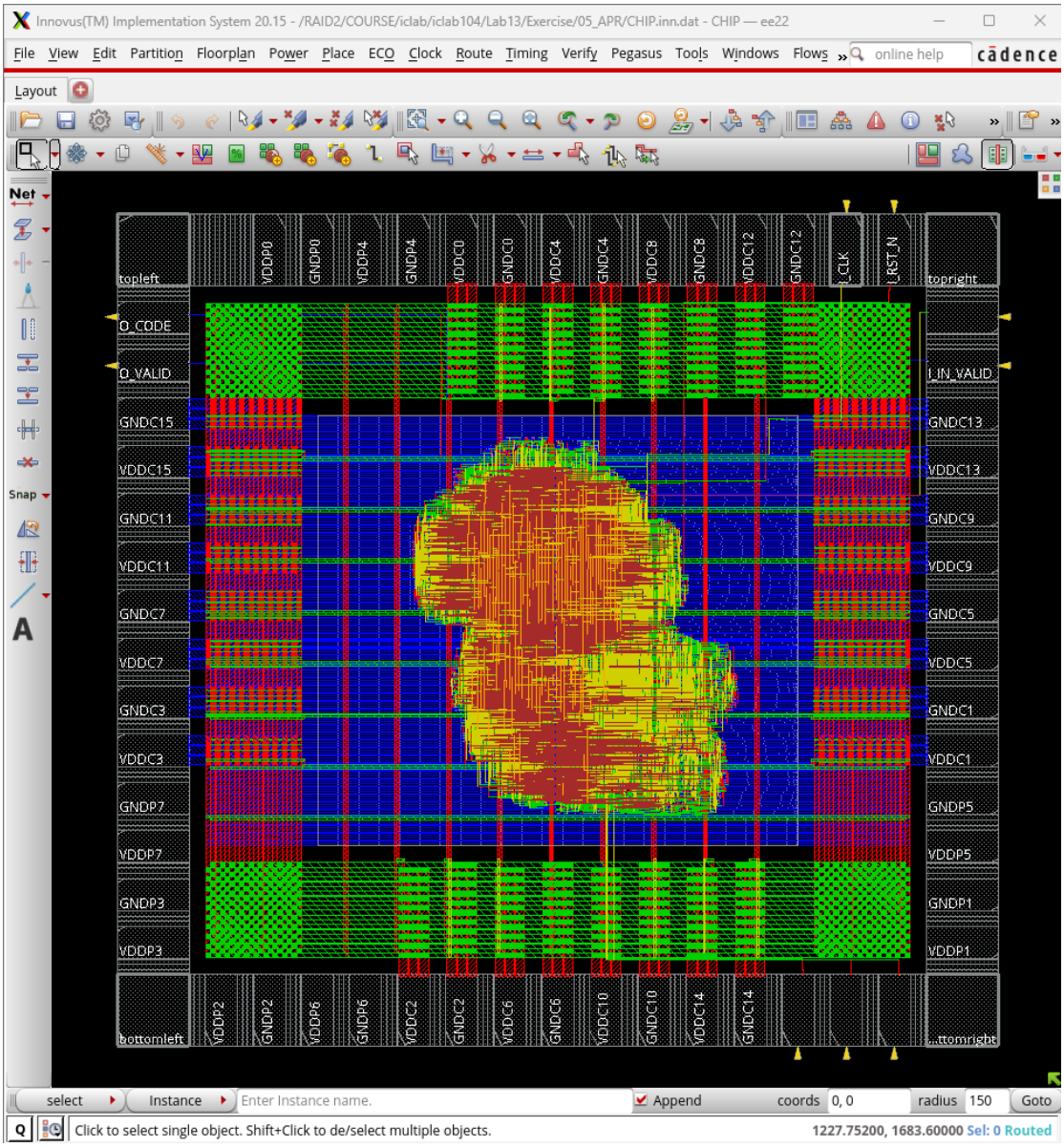
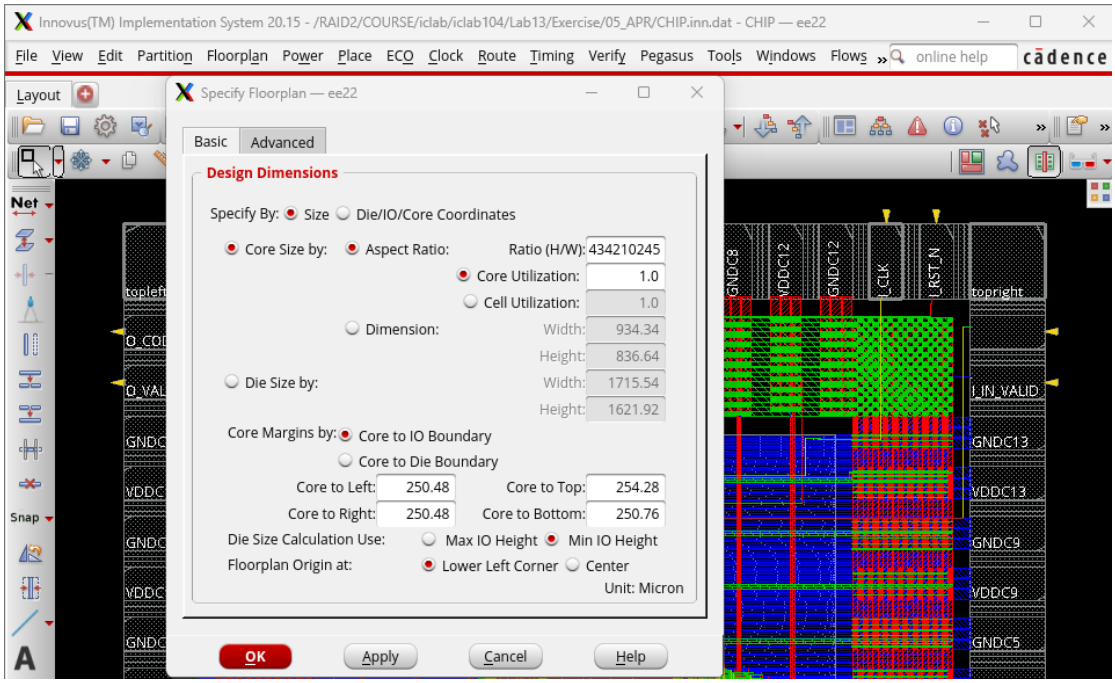
Report

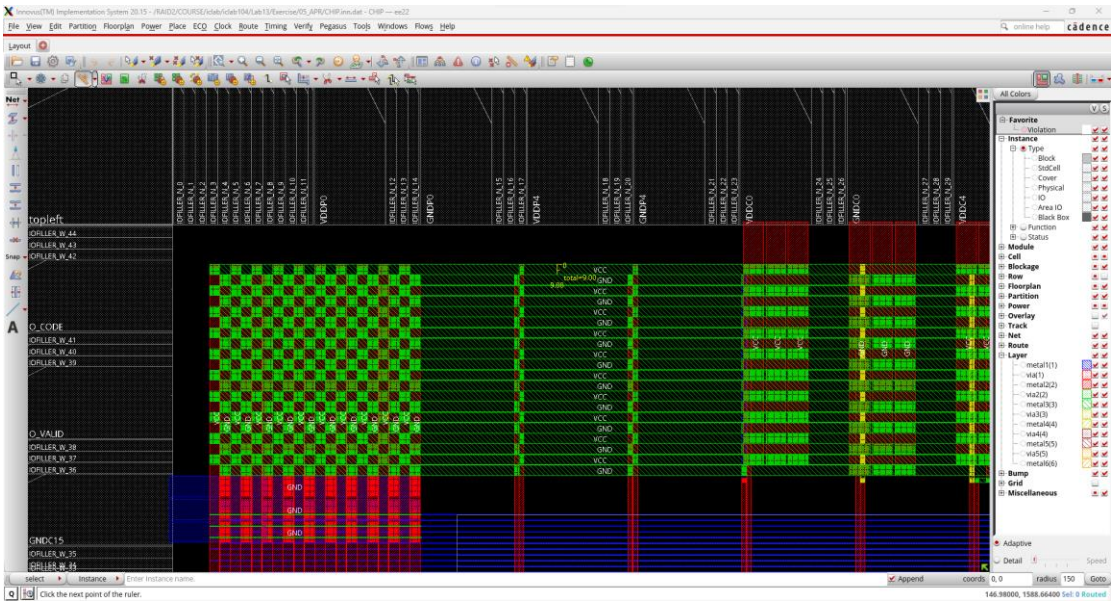
1. Chip Layout View :



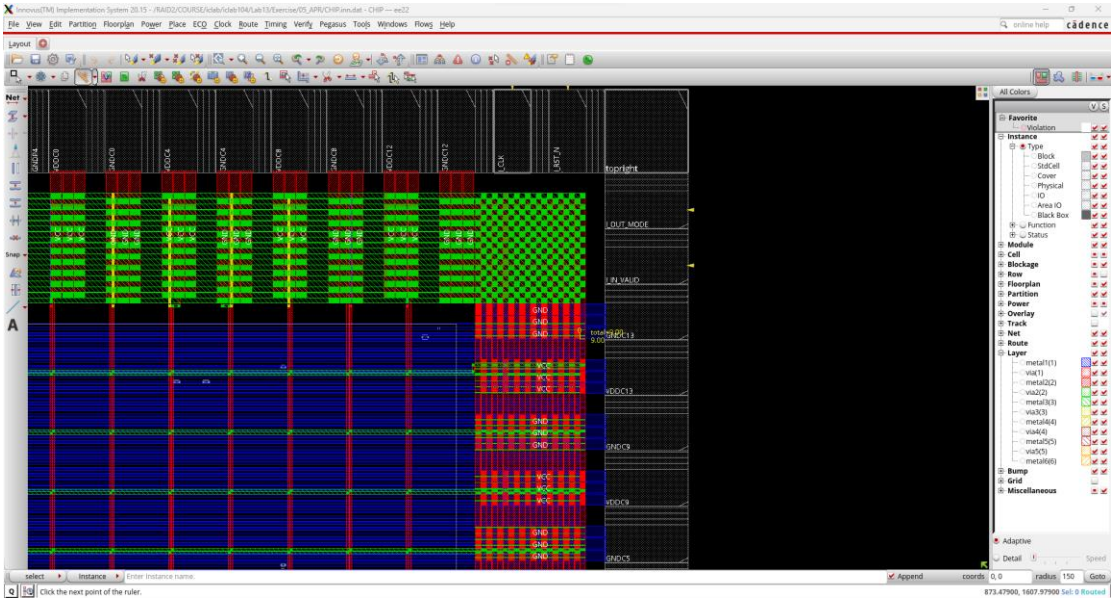
2. Core to IO boundary :



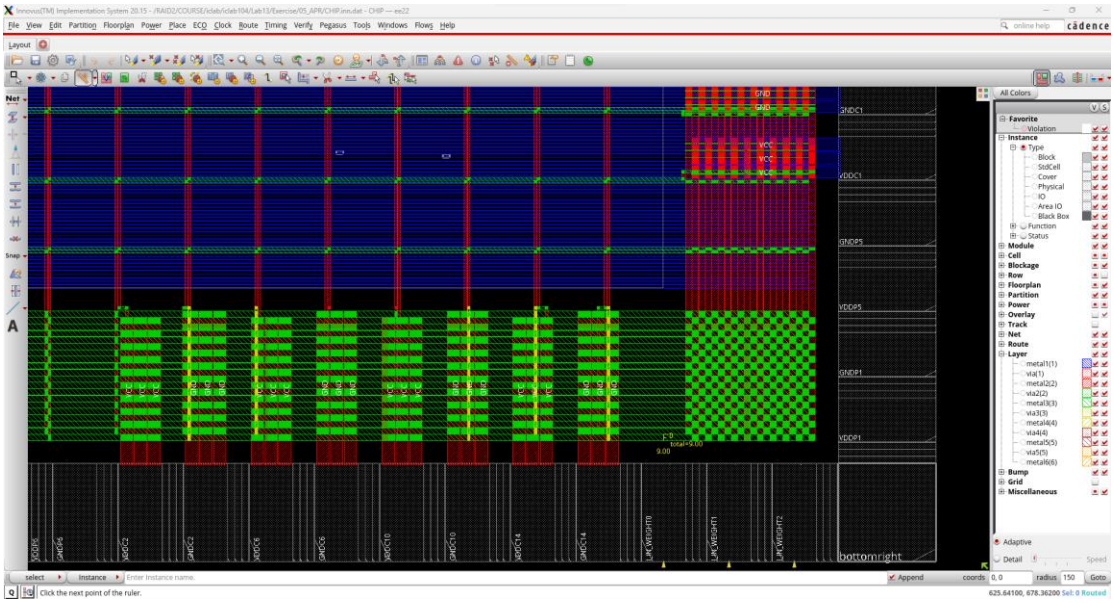
3. Core Ring :



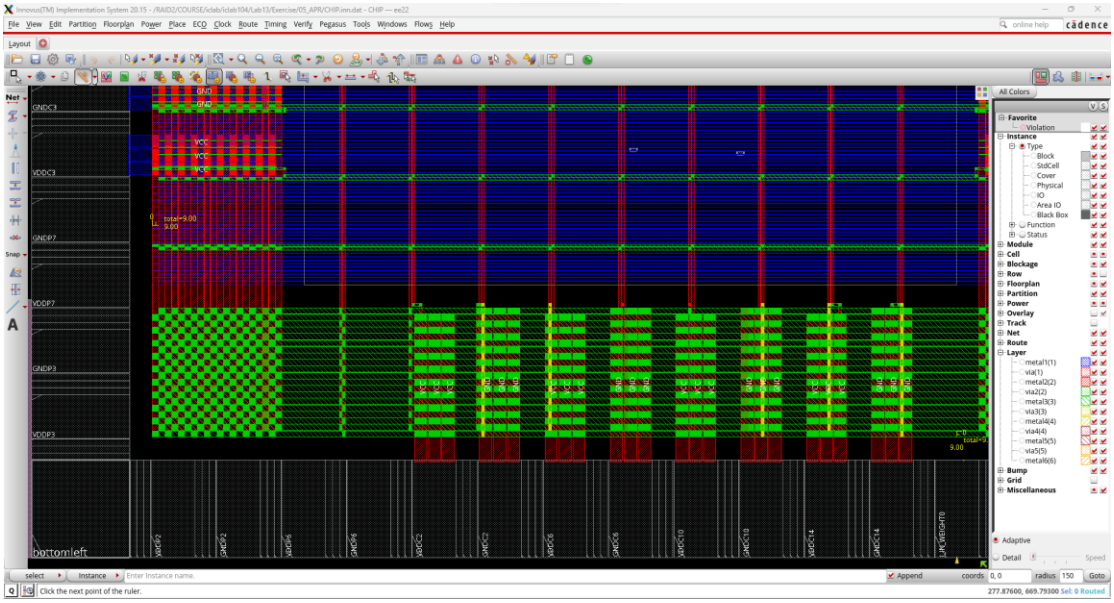
(top)



(right)

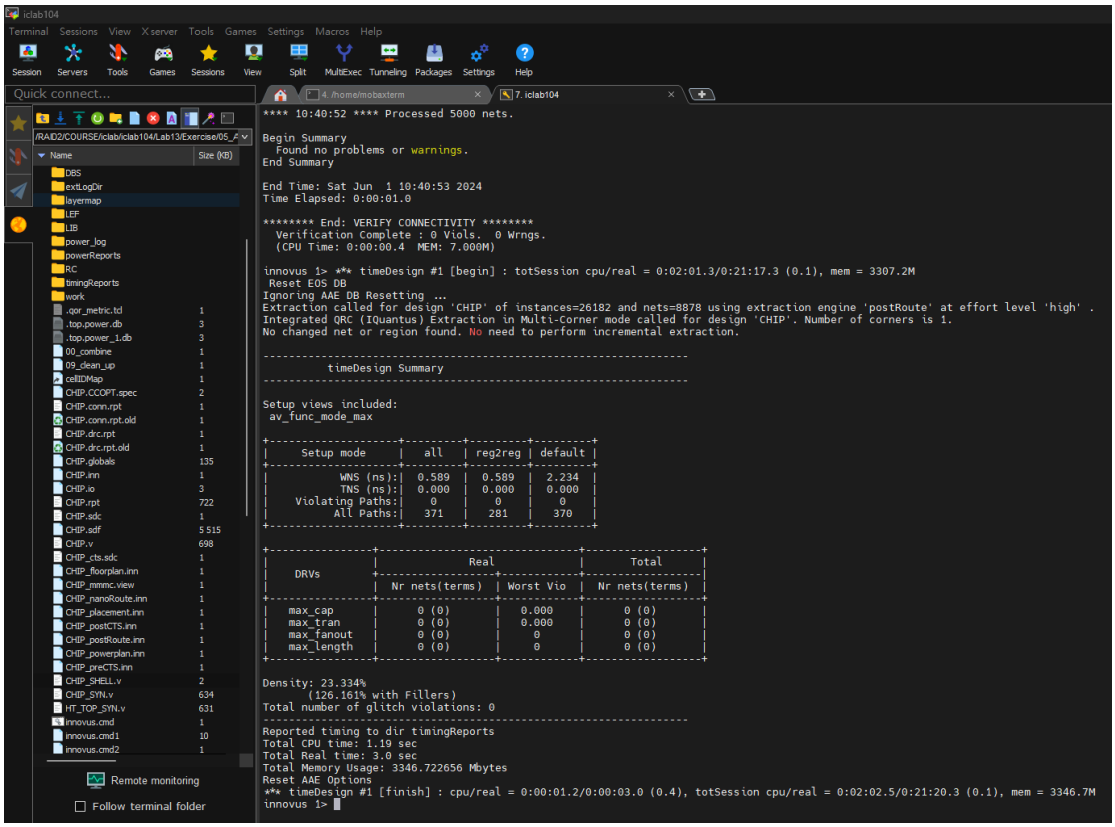


(bottom)

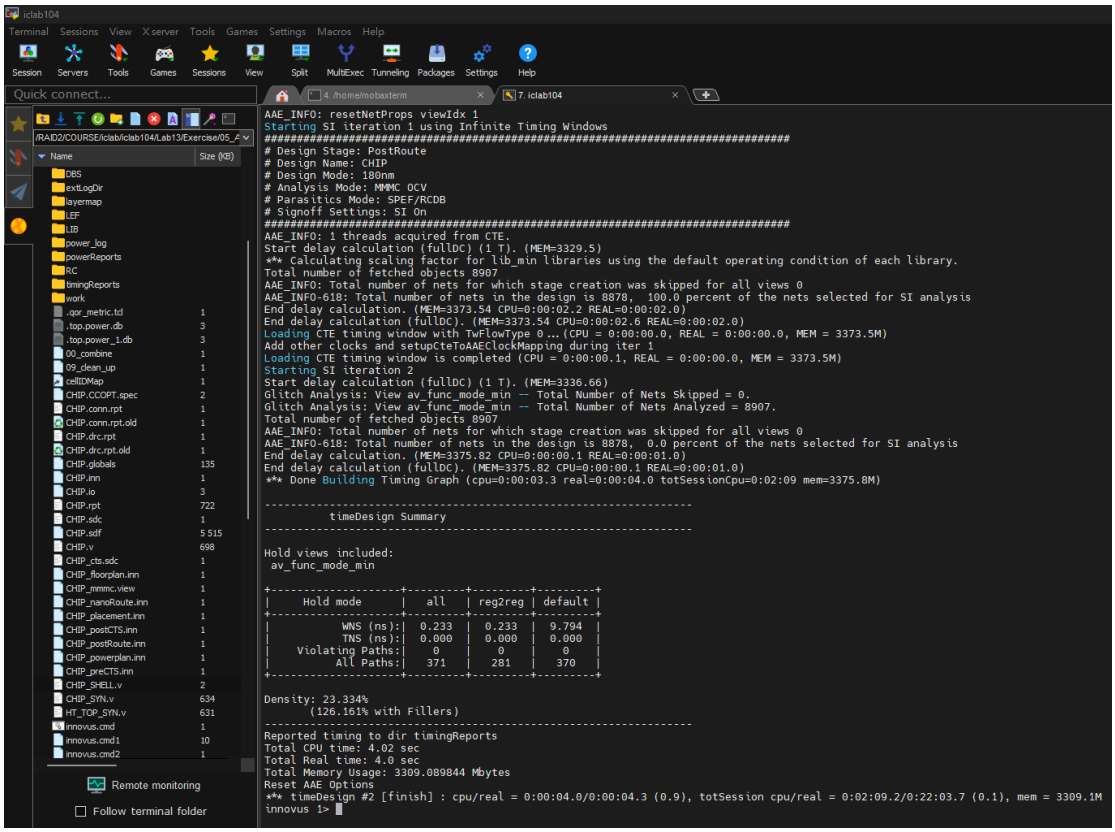


(left)

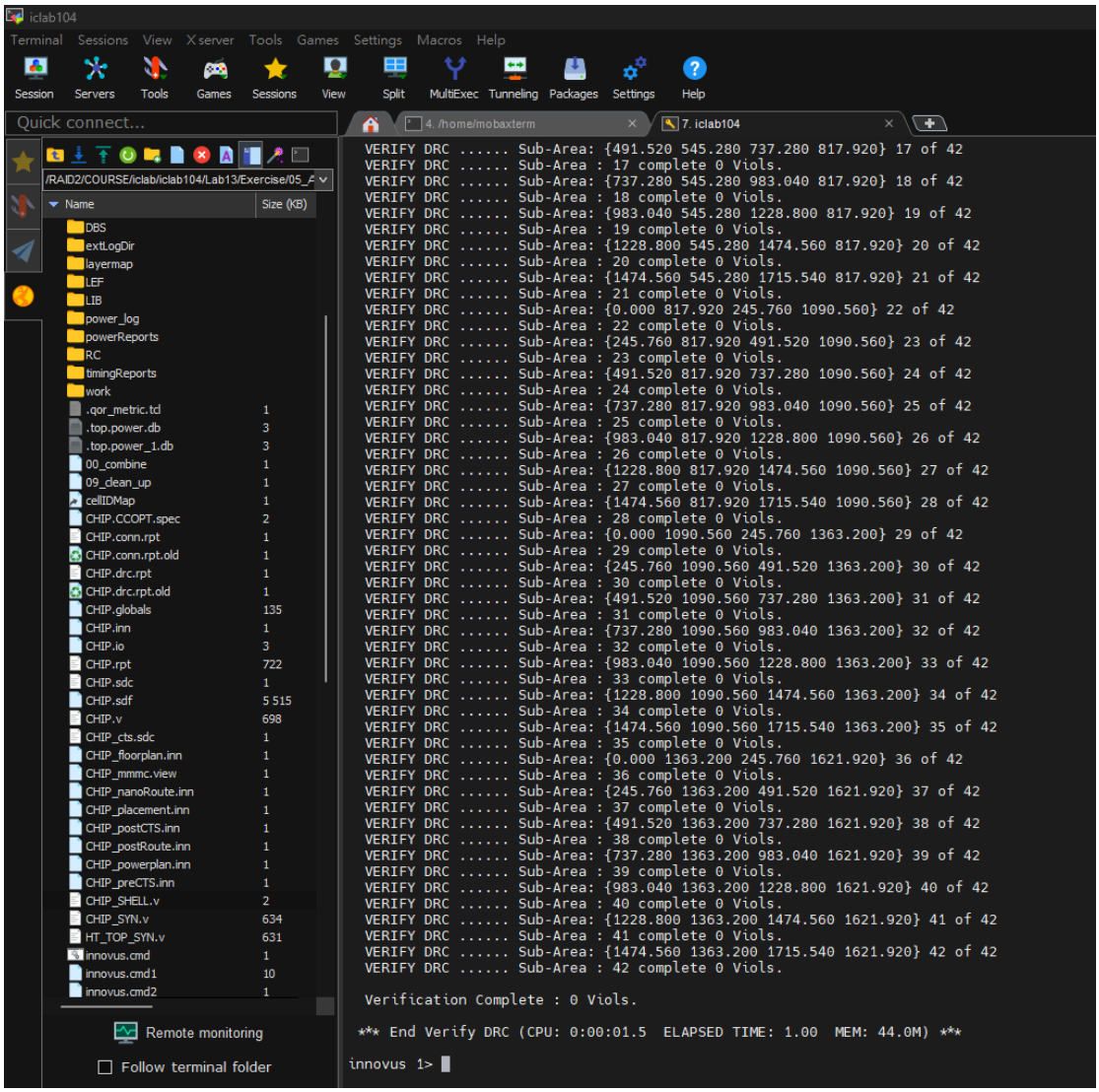
4. Post-Route setup time analysis :



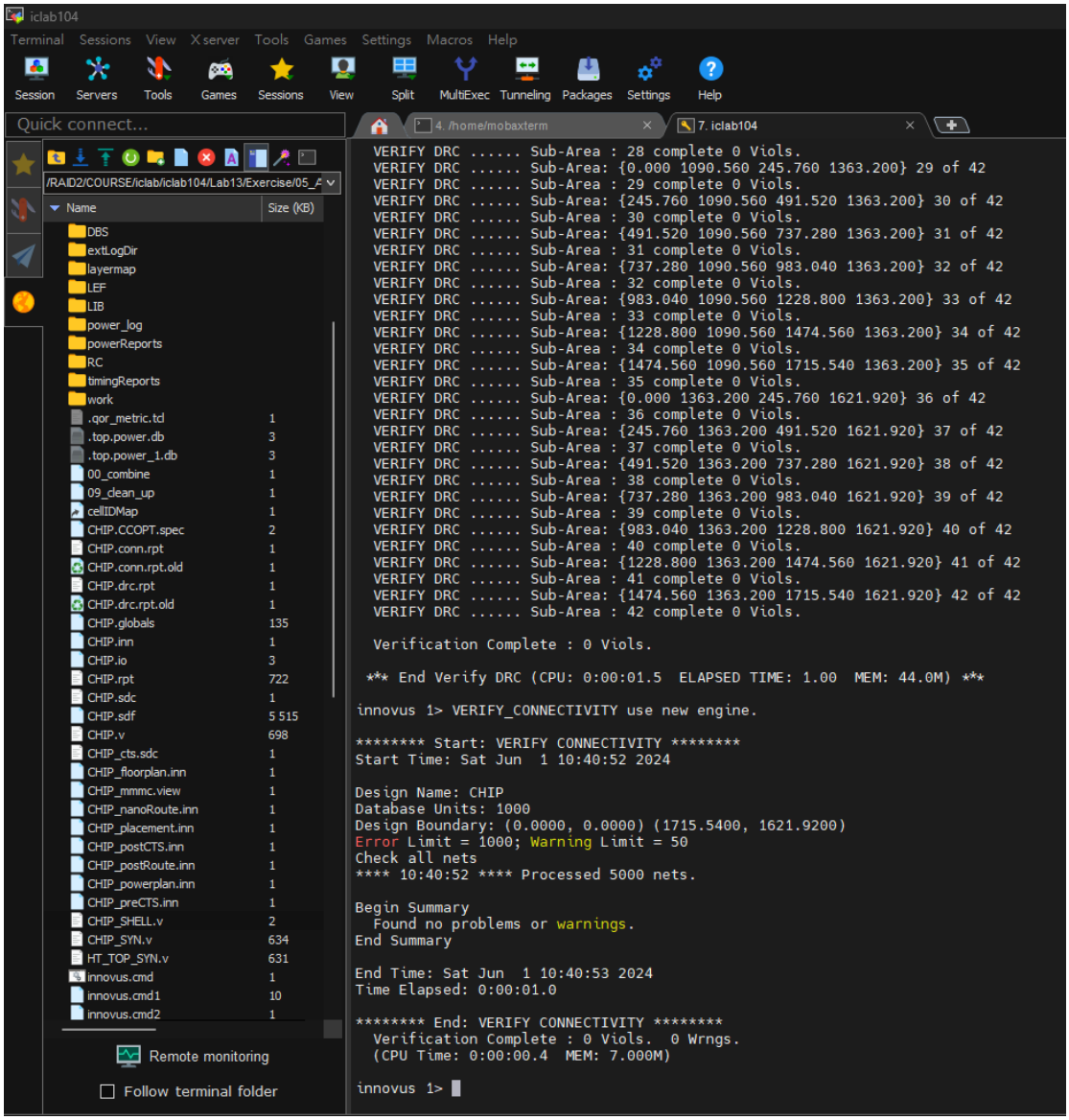
5. Post-Route hold time analysis :



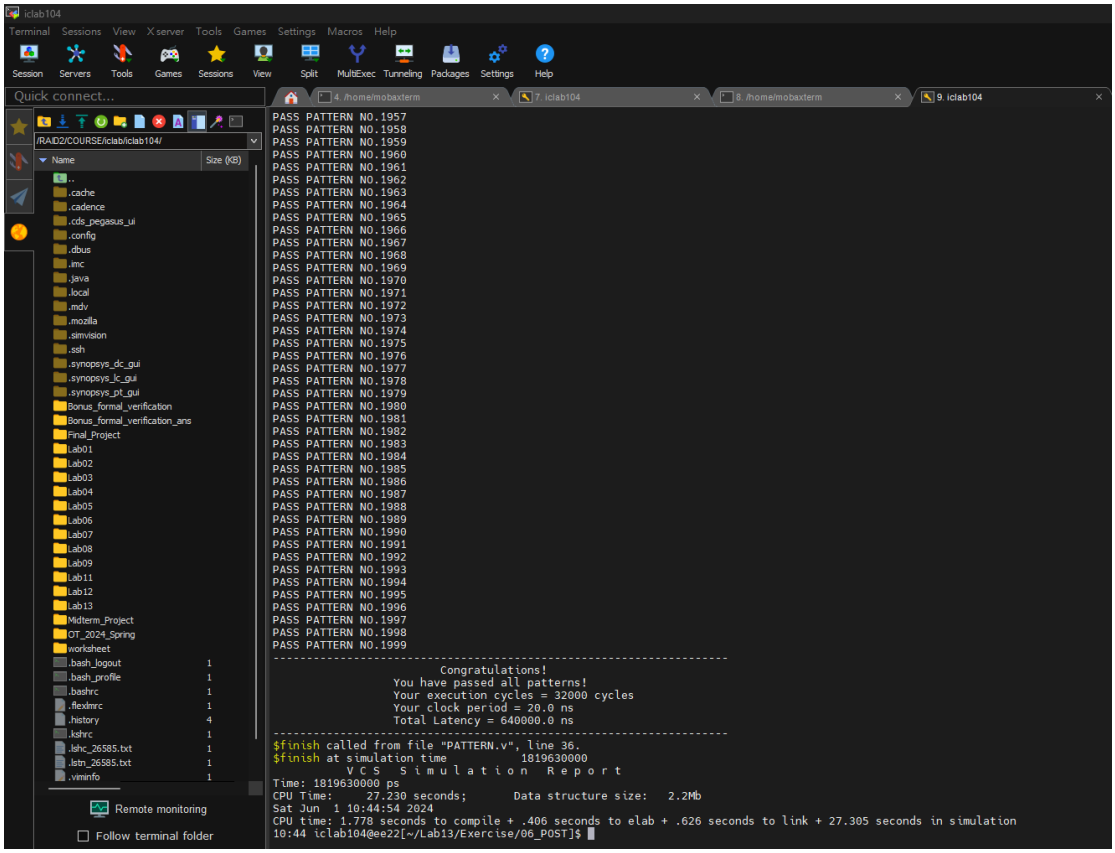
6. DRC result :


iclab104
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
4. /home/mobaxterm
7. iclab104
/RAID2/COURSE/iclab/iclab104/Lab13/Exercise/05_
Name Size (KB)
DBS
extLogDir
layermap
LEF
LIB
power_log
powerReports
RC
timingReports
work
.qor_metric.tcl 1
.top.power.db 3
.top.power_1.db 3
00_combine 1
09_clean_up 1
cellIDMap 1
CHIP.CCOPT.spec 2
CHIP.conn.rpt 1
CHIP.conn.rpt.old 1
CHIP.drc.rpt 1
CHIP.drc.rpt.old 1
CHIP.globals 135
CHIP.inn 1
CHIP.io 3
CHIP.rpt 722
CHIP.sdc 1
CHIP.sdf 5 515
CHIP.v 698
CHIP_cts.sdc 1
CHIP_floorplan.inn 1
CHIP_mmmc.view 1
CHIP_nanoRoute.inn 1
CHIP_placement.inn 1
CHIP_postCTS.inn 1
CHIP_postRoute.inn 1
CHIP_powerplan.inn 1
CHIP_preCTS.inn 1
CHIP_SHELL.v 2
CHIP_SYN.v 634
HT_TOP_SYN.v 631
innovus.cmd 1
innovus.cmd1 10
innovus.cmd2 1
Remote monitoring
Follow terminal folder
VERIFY DRC ..... Sub-Area: {491.520 545.280 737.280 817.920} 17 of 42
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 545.280 983.040 817.920} 18 of 42
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 545.280 1228.800 817.920} 19 of 42
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 545.280 1474.560 817.920} 20 of 42
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 545.280 1715.540 817.920} 21 of 42
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 817.920 245.760 1090.560} 22 of 42
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 817.920 491.520 1090.560} 23 of 42
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 817.920 737.280 1090.560} 24 of 42
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 817.920 983.040 1090.560} 25 of 42
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 817.920 1228.800 1090.560} 26 of 42
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 817.920 1474.560 1090.560} 27 of 42
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 817.920 1715.540 1090.560} 28 of 42
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1090.560 245.760 1363.200} 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1090.560 491.520 1363.200} 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1090.560 737.280 1363.200} 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1090.560 983.040 1363.200} 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1090.560 1228.800 1363.200} 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1090.560 1474.560 1363.200} 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1090.560 1715.540 1363.200} 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1363.200 245.760 1621.920} 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1363.200 491.520 1621.920} 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1363.200 737.280 1621.920} 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1363.200 983.040 1621.920} 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1363.200 1228.800 1621.920} 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1363.200 1474.560 1621.920} 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1363.200 1715.540 1621.920} 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.
Verification Complete : 0 Viols.
*** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 1.00 MEM: 44.0M) ***
innovus 1>

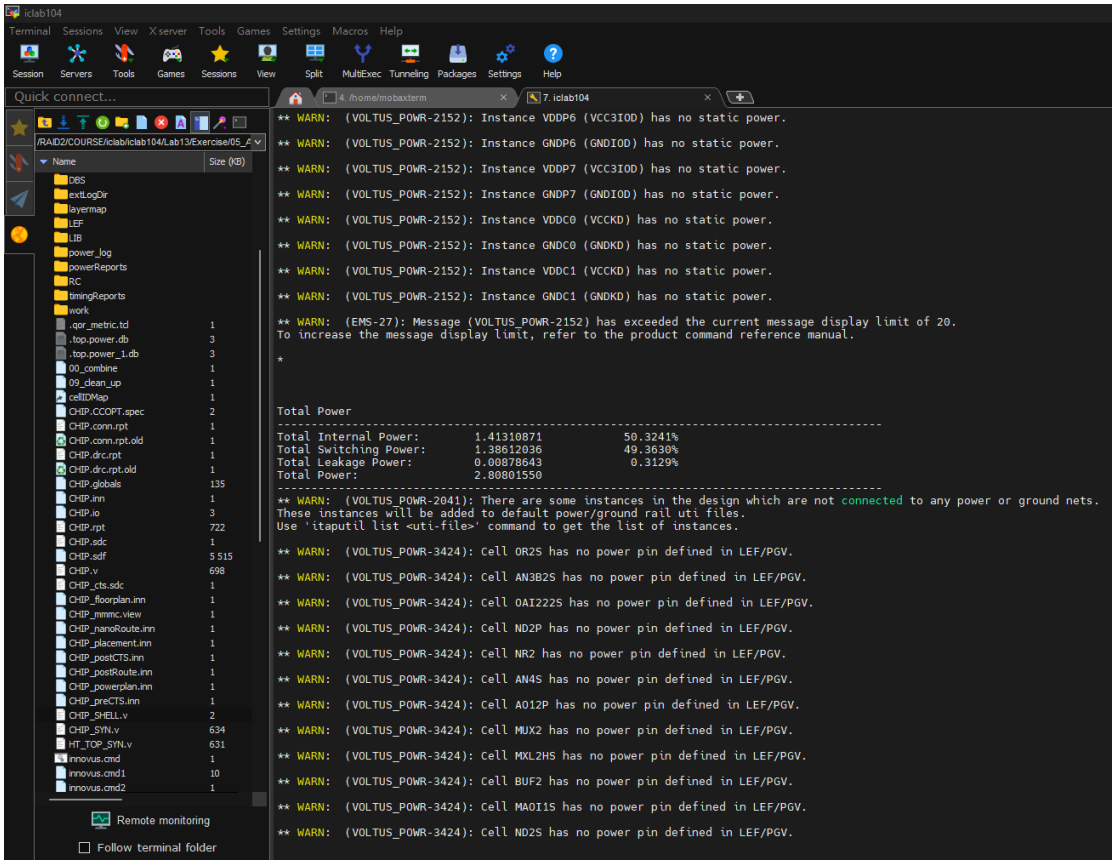
7. LVS result :


iclab104
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
4. /home/mobaxterm
7. iclab104
/RAID2/COURSE/iclab/iclab104/Lab13/Exercise/05_
Name Size (KB)
DBS
extLogDir
layermap
LEF
LIB
power_log
powerReports
RC
timingReports
work
.qor_metric.tcl 1
.top.power.db 3
.top.power_1.db 3
00_combine 1
09_clean_up 1
cellIDMap 1
CHIP.CCOPT.spec 2
CHIP.conn.rpt 1
CHIP.conn.rpt.old 1
CHIP.drc.rpt 1
CHIP.drc.rpt.old 1
CHIP.globals 135
CHIP.inn 1
CHIP.io 3
CHIP.rpt 722
CHIP.sdc 1
CHIP.sdf 5 515
CHIP.v 698
CHIP_cts.sdc 1
CHIP_floorplan.inn 1
CHIP_mmmc.view 1
CHIP_nanoRoute.inn 1
CHIP_placement.inn 1
CHIP_postCTS.inn 1
CHIP_postRoute.inn 1
CHIP_powerplan.inn 1
CHIP_preCTS.inn 1
CHIP_SHELL.v 2
CHIP_SYN.v 634
HT_TOP_SYN.v 631
innovus.cmd 1
innovus.cmd1 10
innovus.cmd2 1
Remote monitoring
Follow terminal folder
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1090.560 245.760 1363.200} 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1090.560 491.520 1363.200} 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1090.560 737.280 1363.200} 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1090.560 983.040 1363.200} 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1090.560 1228.800 1363.200} 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1090.560 1474.560 1363.200} 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1090.560 1715.540 1363.200} 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1363.200 245.760 1621.920} 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1363.200 491.520 1621.920} 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1363.200 737.280 1621.920} 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1363.200 983.040 1621.920} 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1363.200 1228.800 1621.920} 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1363.200 1474.560 1621.920} 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1363.200 1715.540 1621.920} 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.
Verification Complete : 0 Viols.
** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 1.00 MEM: 44.0M) **
innovus 1> VERIFY_CONNECTIVITY use new engine.
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Jun 1 10:40:52 2024
Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1715.5400, 1621.9200)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 10:40:52 **** Processed 5000 nets.
Begin Summary
Found no problems or warnings.
End Summary
End Time: Sat Jun 1 10:40:53 2024
Time Elapsed: 0:00:01.0
******** End: VERIFY CONNECTIVITY ********
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.4 MEM: 7.000M)
innovus 1>

8. Post Layout simulation result :



9. Power result :



10. IR Drop Results :

In Lab12, I set utilization at 75%. This time, I set 70%. Additionally, I add more core power pads. There are 4 pairs in each side, 16 pairs in total.