2024 SPRING ICLAB

Syllabus

Instructor:

- **Chen-Yi Lee**, National Yang Ming Chiao Tung University

Lecture:

- 3EF (13:20 ~ 15:10, Wednesday) @ ED415

TA List:

Name	Email
林文約	kenlin.ee09@nycu.edu.tw
廖展儀	jhan.yi.ee12@nycu.edu.tw
冉宜軒	game890921.ee12@nycu.edu.tw
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連紹華	eed0810766.ee108.ee08@nycu.edu.tw
吳彧嘉	jabywu@gmail.com
黃齊緯	i100486987@gmail.com
蔡睿煌	erictsai.ee12@nycu.edu.tw

TA Time:

- 1EF (13:20 ~ 15:10, Monday) @ ED415 for Lab1~Lab4

Prerequisites:

- Introduction to VLSI, Logic Design, Digital System Design, Computer Organization (opt)

Course Objectives:

This course aims to convey to the senior and graduated EE students techniques to design the VLSI chips using state-of-the-art CAD tools. In addition to learning CAD tools for performance-driven and cost-effective IC designs, a top-down design flow and related environment will also be addressed. Upon completion of the course, the student will be able to design the integrated circuits and systems based on standard cell library as well as full-custom layout approaches. As such, he/she will be able to work with a team of designers or stand-alone.

Online Course link:

The Webex link for the class is:
https://nycu.webex.com/nycu/j.php?MTID=ma3c5cfdd15ea6c15e846f457e7903b4c
Course Add/Drop Form: https://forms.gle/aeNm7EGQ2tMV46EL8

Course Schedule:

Week	Date	Course Content	TA
1	02/21	00、Introduction + Environment Setting	林文約
2	02/28	01、Cell Based Design Methodology + Verilog Combinational Circuit Programming	廖展儀
3	03/06	02、Finite State Machine + Verilog Sequential Circuit Programming	冉宜軒
4	03/13	03、Verification & Simulation + Verilog Test Bench Programming	曹宗叡
5	03/20	04、Sequential Circuit Design II (STA + Pipeline)	張成德
6	03/27	05、Memory & Coding Style (Memory Compiler + SuperLint)	廖展儀
7	04/03	06、Synthesis Methodology (Design Compiler + IP Design)	連紹華
8	04/10	No class: Study Days **Midterm Exam & Online Test (Sat. Afternoon, about 6 hours)**	吳彧嘉 黃齊緯
9	04/17	07、Timing: Cross Clock Domain + Synthesis Static Time Analysis	吳彧嘉
10	04/24	08、System Verilog (Design)	蔡睿煌
11	05/01	09、System Verilog II (Verification)	蔡睿煌
12	05/08	10、System Verilog (Formal Verification)	張成德
13	05/15	11、Power: Low Power Design	曹宗叡
14	05/22	12、APR I: From RTL to GDSII	冉宜軒
15	05/29	13、APR II: IR-Drop Analysis	連紹華
16	06/05	**Final Exam**	林文約
18	06/12	**Final Project Deadline (2nd demo @06/14, 3rd demo @06/19)**	吳彧嘉 黃齊緯

Grading Policy

Weekly Lab Exercise x 13	5*12+3=63%
Midterm Project	8%
Midterm Exam	8%
Online Test	5%
Final Project	8%
Final Exam	8%
Total	100%