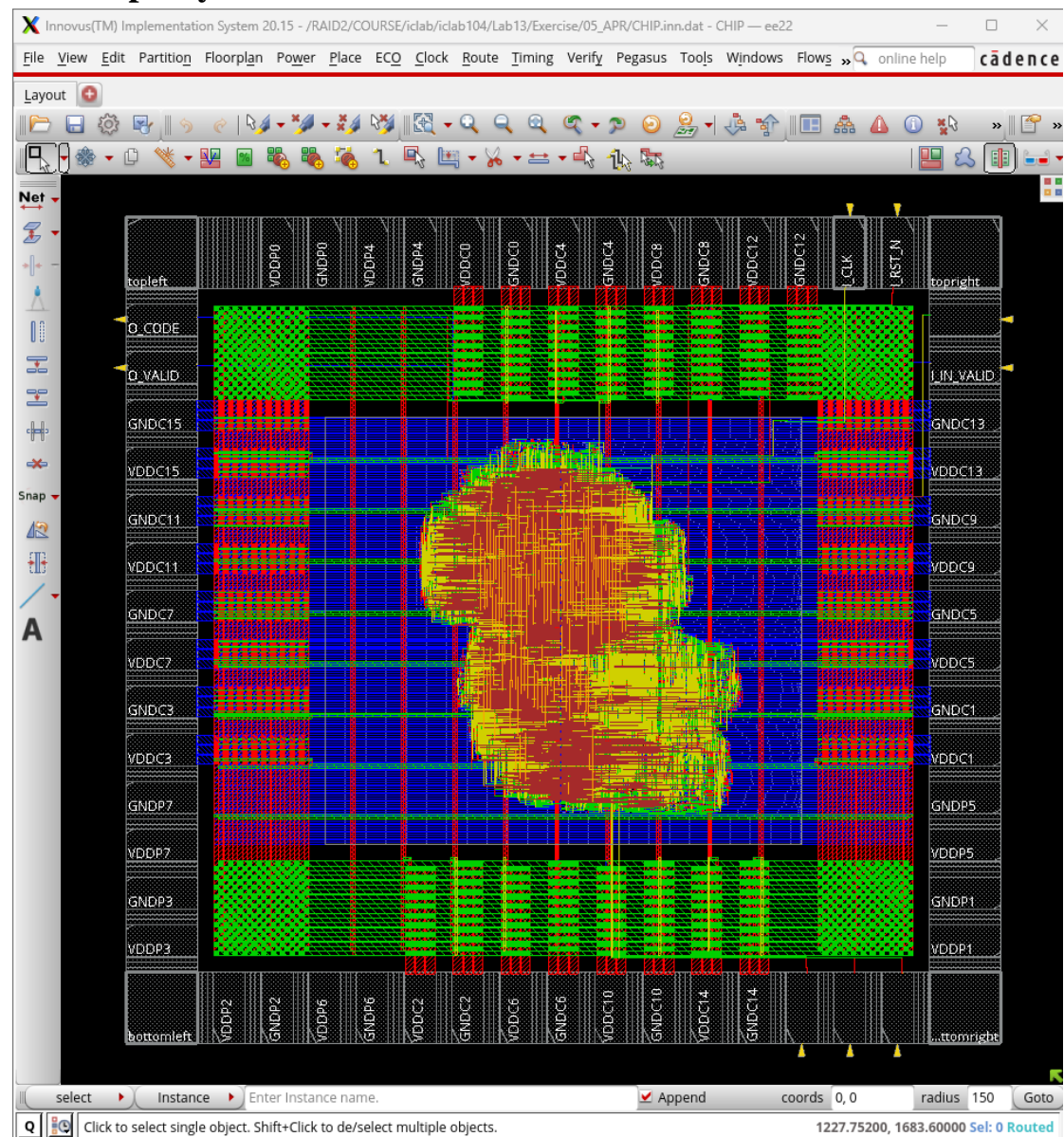
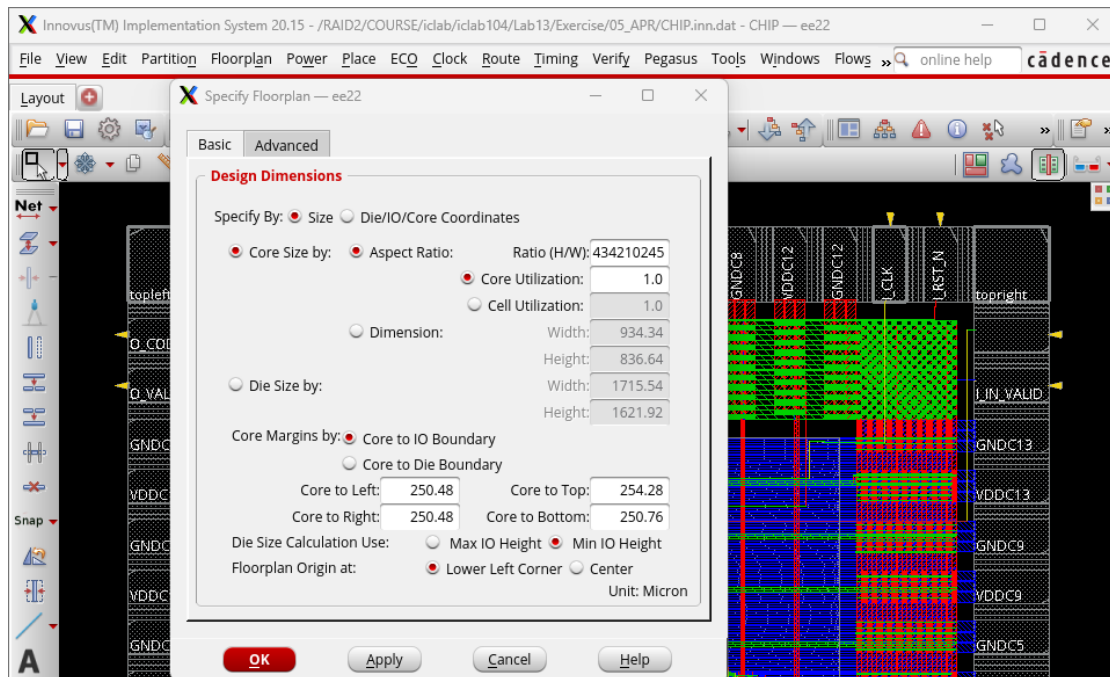


# Report

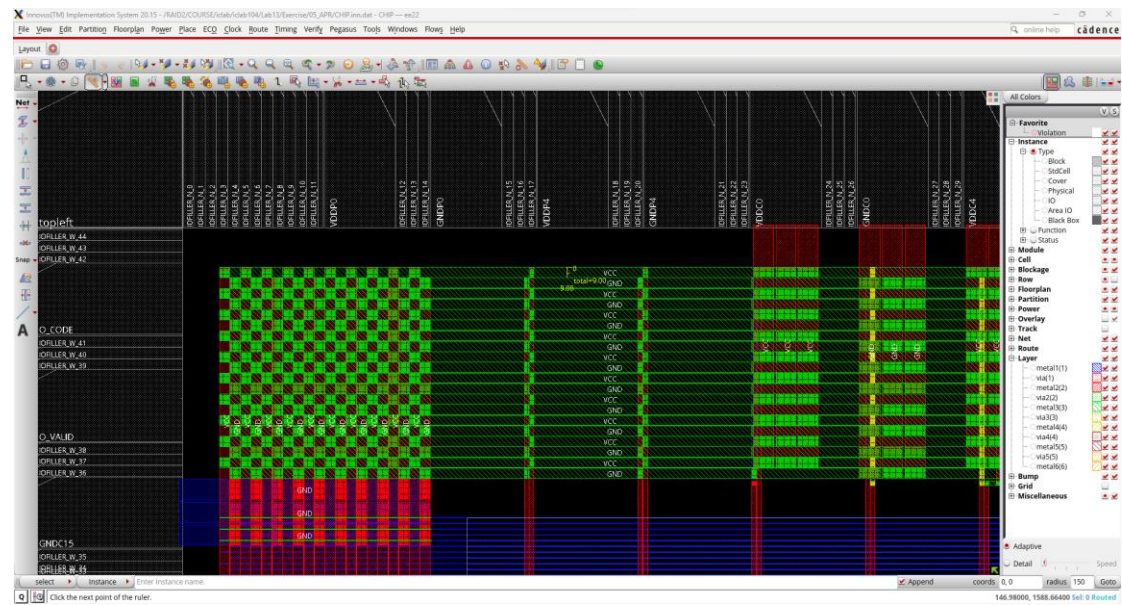
## 1. Chip Layout View :



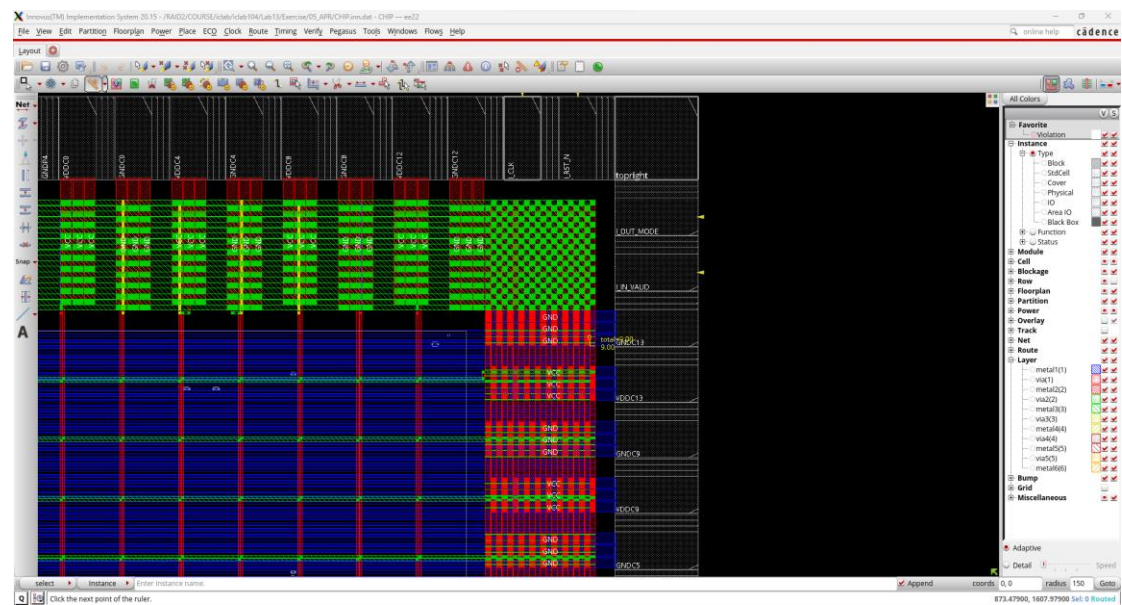
## 2. Core to IO boundary :



### 3. Core Ring :



**(top)**

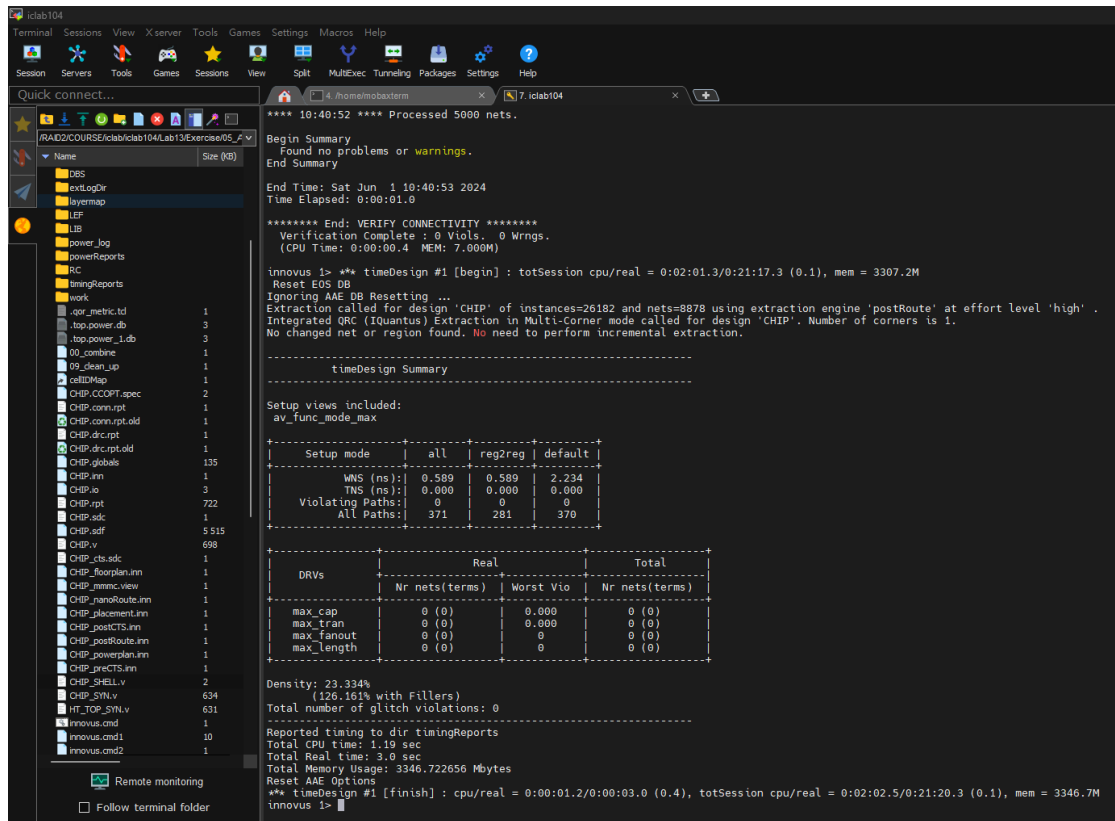


(right)





## 4. Post-Route setup time analysis :



```
**** 10:40:52 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

End Time: Sat Jun 1 10:40:53 2024
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.4 MEM: 7.000M)

innovus i> ** timeDesign #1 [begin] : totSession cpu/real = 0:02:01.3/0:21:17.3 (0.1), mem = 3307.2M
Reset EOS DB
Ignoring AAE DB Resetting ...
Extraction called for design 'CHIP' of instances=26182 and nets=8878 using extraction engine 'postRoute' at effort level 'high'.
Integrated QRC (IQuantus) Extraction in Multi-corner mode called for design 'CHIP'. Number of corners is 1.
No changed net or region found. No need to perform incremental extraction.

-----
timeDesign Summary
-----

Setup views included:
av_tunc_mode_max

+-----+-----+-----+-----+
| Setup mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns) | 0.589 | 0.589 | 2.234 |
| TNS (ns) | 0.000 | 0.000 | 0.000 |
| Violating Paths | 0 | 0 | 0 |
| All Paths | 371 | 281 | 370 |
+-----+-----+-----+-----+

+-----+-----+-----+-----+
| DRVs | Real | Total |
+-----+-----+-----+-----+
| Nr nets(terms) | Worst Vio | Nr nets(terms) |
+-----+-----+-----+-----+
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tfan | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+

Density: 23.334%
(126.161% with Fillers)
Total number of glitch violations: 0
Reported timing to dir timingReports
Total CPU time: 1.19 sec
Total Real time: 3.0 sec
Total Memory Usage: 3340.722656 Mbytes
Reset AAE Options
** timeDesign #1 [finish] : cpu/real = 0:00:01.2/0:00:03.0 (0.4), totSession cpu/real = 0:02:02.5/0:21:20.3 (0.1), mem = 3346.7M
innovus i>
```

## 5. Post-Route hold time analysis :

iclab104

Terminal Sessions View X\_server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

4 / home/mobsterm 7 / iclab104

RA02/COURSE/iclab/iclab104/Lab13/Exercise05\_1

Name Size (KB)

- DSS
- extLogDir
- layermap
- LEF
- LIB
- power\_log
- powerReports
- RC
- timingReports
- work
- qpr\_metric.td 1
- top.power.db 3
- top.power\_Ldb 3
- 00\_combine 1
- 09\_down\_up 1
- cellIDMap 1
- CHP.CC0PT.spec 2
- CHP.conn.rpt 1
- CHP.conn.rptold 1
- CHP.drcrpt 1
- CHP.drcrptold 1
- CHP\_globals 135
- CHP.inn 1
- CHP.js 3
- CHP.rpt 722
- CHP.sdc 1
- CHP.sdf 5515
- CHP.v 698
- CHP.cts.sdc 1
- CHP\_floorplan.inn 1
- CHP\_nmmc.view 1
- CHP\_nanoRoute.inn 1
- CHP\_placement.inn 1
- CHP\_postCTS.inn 1
- CHP\_postRoute.inn 1
- CHP\_powerplan.inn 1
- CHP\_preCTS.inn 1
- CHP\_SHELL.v 2
- CHP\_SYN.v 634
- HT\_TOP\_SYN.v 631
- innovus.cmd 1
- innovus.cmd1 10
- innovus.cmd2 1

Remote monitoring

Follow terminal folder

AAE\_INFO: resetNetDrops viewIdx 1

Starting SI iteration 1 using Infinite Timing Windows

#####

# Design Stage: PostRoute

# Design Name: CHIP

# Design Model: 180nm

# Analysis Mode: MMMC OCv

# Parasitics Mode: SPEF/RCDB

# Signoff Settings: SI On

#####

AAE\_INFO: 1 threads acquired from CTE.

Start delay calculation (fullDC) (1 T). (MEM=3329.5)

\*\*\* calculating scaling factor for lib\_mn libraries using the default operating condition of each library.

Total number of fetched objects 8907

AAE\_INFO: Total number of nets for which stage creation was skipped for all views 0

AAE\_INFO-618: Total number of nets in the design is 8878, 100.0 percent of the nets selected for SI analysis

End delay calculation. (MEM=3373.54 CPU=0:00:02.2 REAL=0:00:02.0)

End delay calculation (fullDC). (MEM=3373.54 CPU=0:00:02.0 REAL=0:00:02.0)

Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3373.5M)

Add other clocks and setupCteToAAEClockMapping during iter 1

Loading CTE timing window is completed (CPU = 0:00:00.1, REAL = 0:00:00.0, MEM = 3373.5M)

Starting SI iteration 2

Start delay calculation (fullDC) (1 T). (MEM=3336.66)

Glitch Analysis: View av\_func\_mode\_min -- Total Number of Nets Skipped = 0.

Glitch Analysis: View av\_func\_mode\_min -- Total Number of Nets Analyzed = 8907.

Total number of fetched objects 8907

AAE\_INFO: Total number of nets for which stage creation was skipped for all views 0

AAE\_INFO-618: Total number of nets in the design is 8878, 0.0 percent of the nets selected for SI analysis

End delay calculation. (MEM=3375.82 CPU=0:00:00.1 REAL=0:00:01.0)

End delay calculation (fullDC). (MEM=3375.82 CPU=0:00:00.1 REAL=0:00:01.0)

\*\*\* Done Building Timing Graph (cpu=0:00:03.3 real=0:00:04.0 totSessionCpu=0:02:09 mem=3375.8M)

-----

timeDesign Summary

-----

Hold views included:

av\_func\_mode\_min

Hold mode	all	reg2reg	default
WNS (ns):	0.233	0.233	0.794
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

Density: 23.334%

(126.161% with Fillers)

-----

Reported timing to dir timingReports

Total CPU time: 4.02 sec

Total Real time: 4.0 sec

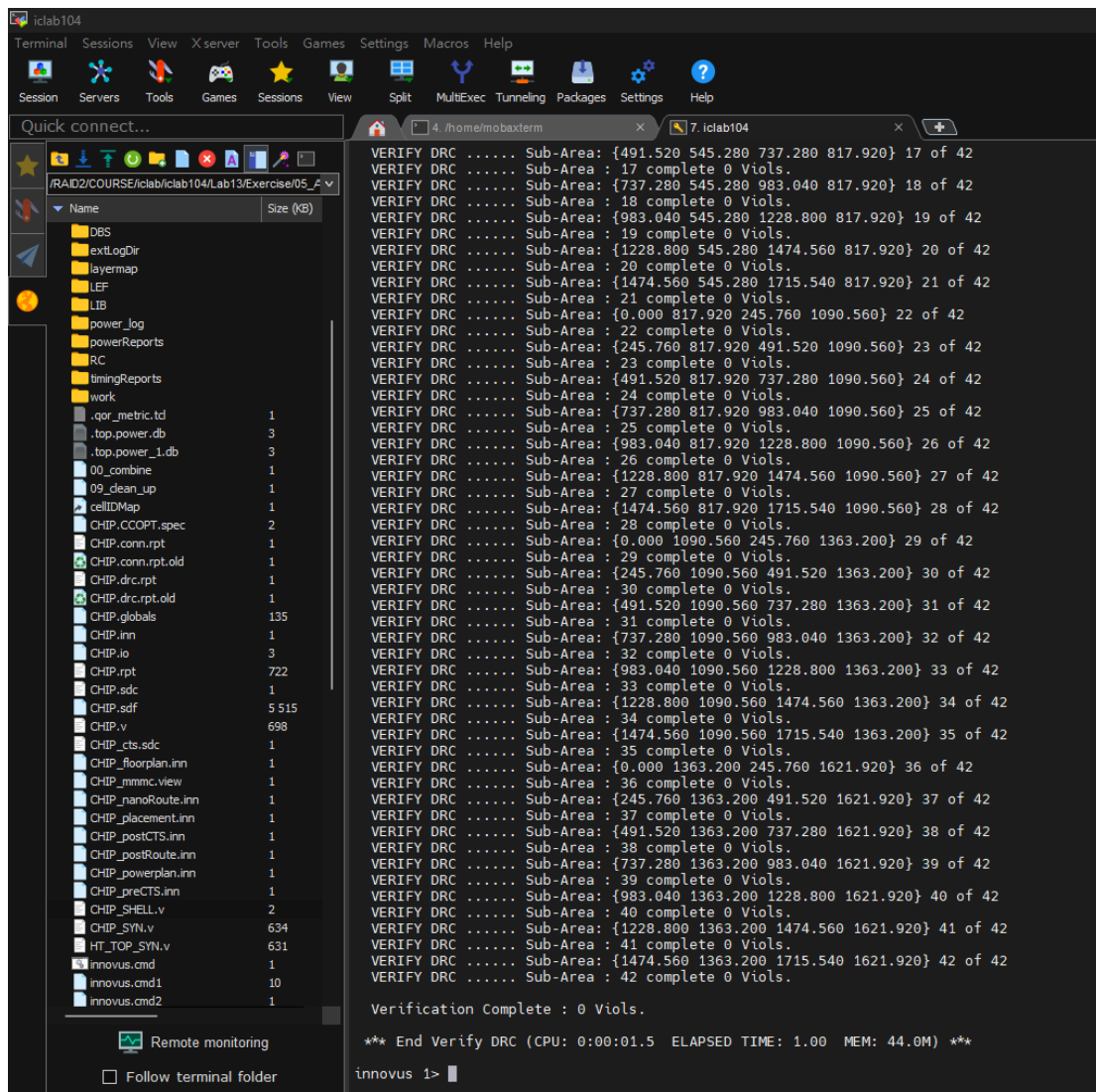
Total Memory Usage: 3309.889844 Mbytes

Reset AAE Options

\*\*\* timeDesign #2 [finish] : cpu/real = 0:00:04.0/0:00:04.3 (0.9), totSession cpu/real = 0:02:09.2/0:22:03.7 (0.1), mem = 3309.1M

innovus i>

## 6. DRC result :



The screenshot shows a terminal window with a multi-tabbed interface. The left sidebar displays a file tree for the project `/RAID2/COURSE/iclab/iclab104/Lab13/Exercise05_2`. The main terminal area shows the output of a Design Rule Check (DRC) process.

**File Tree (Left Sidebar):**

Name	Size (KB)
DBS	
extLogDir	
layermap	
LEF	
LIB	
power_log	
powerReports	
RC	
timingReports	
work	
.qor_metric.tcl	1
.top.power.db	3
.top.power_1.db	3
00_combine	1
09_clean_up	1
cellIDMap	1
CHIP_CCOPT.spec	2
CHIP_conn.rpt	1
CHIP_conn.rpt.old	1
CHIP_drc.rpt	1
CHIP_drc.rpt.old	1
CHIP_globals	135
CHIP.inn	1
CHIP.io	3
CHIP.rpt	722
CHIP.sdc	1
CHIP.sdf	5 515
CHIP.v	698
CHIP_cts.sdc	1
CHIP_floorplan.inn	1
CHIP_mmc.view	1
CHIP_nanoRoute.inn	1
CHIP_placement.inn	1
CHIP_postCTS.inn	1
CHIP_postRoute.inn	1
CHIP_powerplan.inn	1
CHIP_preCTS.inn	1
CHIP_SHELL.v	2
CHIP_SYN.v	634
HT_TOP_SYN.v	631
innovus.cmd	1
innovus.cmd1	10
innovus.cmd2	1

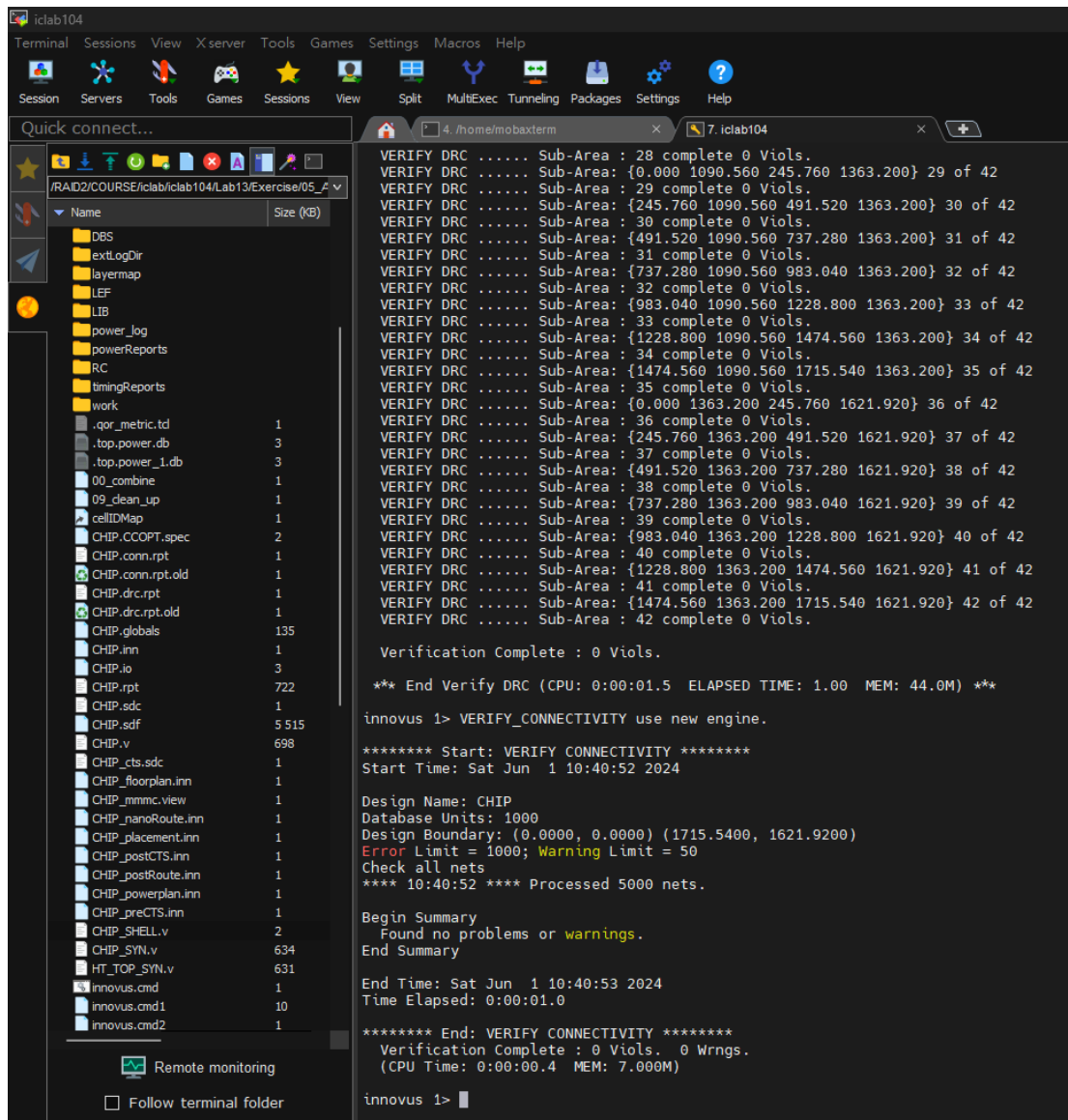
**Terminal Output (Main Area):**

```
VERIFY DRC ..... Sub-Area: {491.520 545.280 737.280 817.920} 17 of 42
VERIFY DRC ..... Sub-Area : 17 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 545.280 983.040 817.920} 18 of 42
VERIFY DRC ..... Sub-Area : 18 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 545.280 1228.800 817.920} 19 of 42
VERIFY DRC ..... Sub-Area : 19 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 545.280 1474.560 817.920} 20 of 42
VERIFY DRC ..... Sub-Area : 20 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 545.280 1715.540 817.920} 21 of 42
VERIFY DRC ..... Sub-Area : 21 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 817.920 245.760 1090.560} 22 of 42
VERIFY DRC ..... Sub-Area : 22 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 817.920 491.520 1090.560} 23 of 42
VERIFY DRC ..... Sub-Area : 23 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 817.920 737.280 1090.560} 24 of 42
VERIFY DRC ..... Sub-Area : 24 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 817.920 983.040 1090.560} 25 of 42
VERIFY DRC ..... Sub-Area : 25 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 817.920 1228.800 1090.560} 26 of 42
VERIFY DRC ..... Sub-Area : 26 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 817.920 1474.560 1090.560} 27 of 42
VERIFY DRC ..... Sub-Area : 27 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 817.920 1715.540 1090.560} 28 of 42
VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1090.560 245.760 1363.200} 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1090.560 491.520 1363.200} 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1090.560 737.280 1363.200} 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1090.560 983.040 1363.200} 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1090.560 1228.800 1363.200} 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1090.560 1474.560 1363.200} 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1090.560 1715.540 1363.200} 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1363.200 245.760 1621.920} 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1363.200 491.520 1621.920} 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1363.200 737.280 1621.920} 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1363.200 983.040 1621.920} 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1363.200 1228.800 1621.920} 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1363.200 1474.560 1621.920} 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1363.200 1715.540 1621.920} 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 1.00 MEM: 44.0M) ***
innovus 1>
```

## 7. LVS result :



```
iclab104
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
Name Size (KB)
DBS
extLogDir
layermap
LEF
LIB
power_log
powerReports
RC
timingReports
work
.qor_metric.td 1
.top.power.db 3
.top.power_1.db 3
00_combine 1
09_clean_up 1
cellIDMap 1
CHIP.CCOPT.spec 2
CHIP.conn.rpt 1
CHIP.conn.rpt.old 1
CHIP.drc.rpt 1
CHIP.drc.rpt.old 1
CHIP.globals 135
CHIP.inn 1
CHIP.io 3
CHIP.rpt 722
CHIP.sdc 1
CHIP.sdf 5515
CHIP.v 698
CHIP.cts.sdc 1
CHIP.floorplan.inn 1
CHIP.mmmc.view 1
CHIP.nanoRoute.inn 1
CHIP.placement.inn 1
CHIP.postCTS.inn 1
CHIP.postRoute.inn 1
CHIP.powerplan.inn 1
CHIP.preCTS.inn 1
CHIP.SHELL.v 2
CHIP_SYN.v 634
HT_TOP_SYN.v 631
innovus.cmd 1
innovus.cmd1 10
innovus.cmd2 1

Remote monitoring
Follow terminal folder

VERIFY DRC ..... Sub-Area : 28 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1090.560 245.760 1363.200} 29 of 42
VERIFY DRC ..... Sub-Area : 29 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1090.560 491.520 1363.200} 30 of 42
VERIFY DRC ..... Sub-Area : 30 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1090.560 737.280 1363.200} 31 of 42
VERIFY DRC ..... Sub-Area : 31 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1090.560 983.040 1363.200} 32 of 42
VERIFY DRC ..... Sub-Area : 32 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1090.560 1228.800 1363.200} 33 of 42
VERIFY DRC ..... Sub-Area : 33 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1090.560 1474.560 1363.200} 34 of 42
VERIFY DRC ..... Sub-Area : 34 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1090.560 1715.540 1363.200} 35 of 42
VERIFY DRC ..... Sub-Area : 35 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 1363.200 245.760 1621.920} 36 of 42
VERIFY DRC ..... Sub-Area : 36 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {245.760 1363.200 491.520 1621.920} 37 of 42
VERIFY DRC ..... Sub-Area : 37 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {491.520 1363.200 737.280 1621.920} 38 of 42
VERIFY DRC ..... Sub-Area : 38 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {737.280 1363.200 983.040 1621.920} 39 of 42
VERIFY DRC ..... Sub-Area : 39 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {983.040 1363.200 1228.800 1621.920} 40 of 42
VERIFY DRC ..... Sub-Area : 40 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1228.800 1363.200 1474.560 1621.920} 41 of 42
VERIFY DRC ..... Sub-Area : 41 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1474.560 1363.200 1715.540 1621.920} 42 of 42
VERIFY DRC ..... Sub-Area : 42 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:01.5 ELAPSED TIME: 1.00 MEM: 44.0M) ***

innovus 1> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sat Jun 1 10:40:52 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (1715.5400, 1621.9200)
Error Limit = 1000; Warning Limit = 50
Check all nets
**** 10:40:52 **** Processed 5000 nets.

Begin Summary
Found no problems or warnings.
End Summary

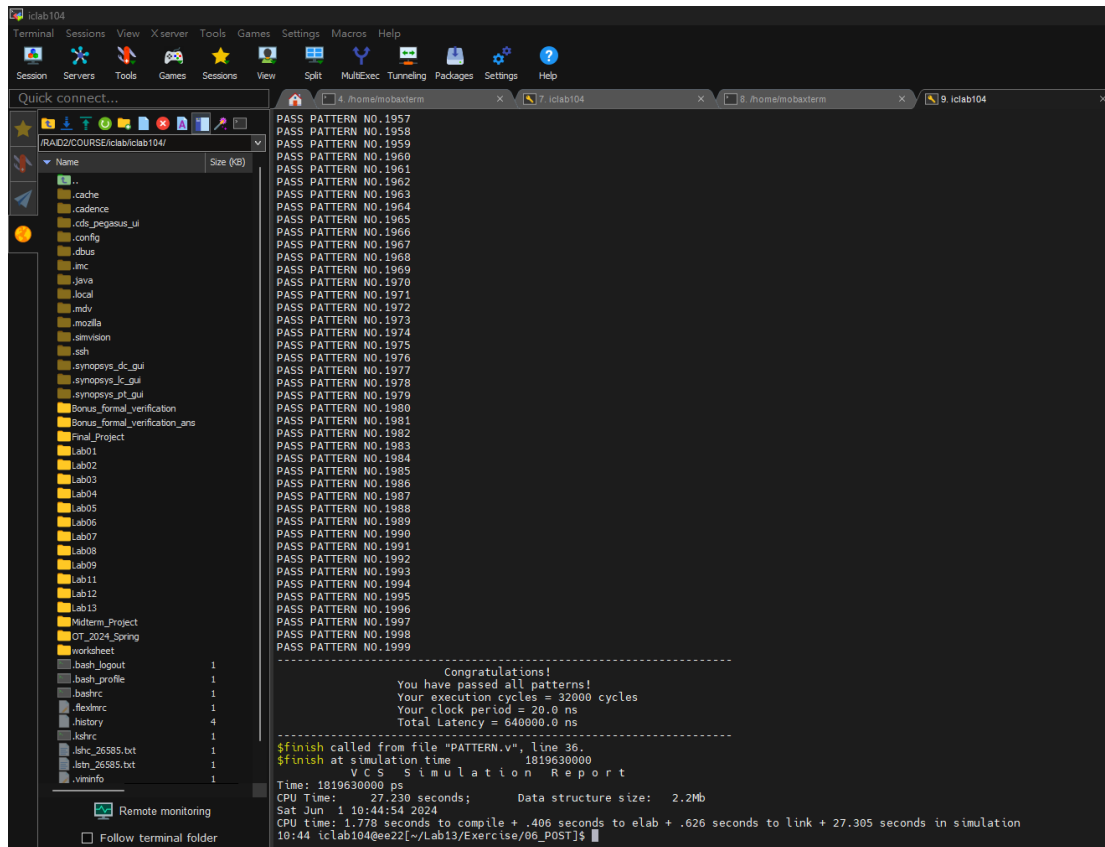
End Time: Sat Jun 1 10:40:53 2024
Time Elapsed: 0:00:01.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.4 MEM: 7.000M)

innovus 1>
```



## 8. Post Layout simulation result :



```
iclab104
Terminal Sessions View Xserver Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
[RAID2/COURSE/iclab/iclab104/]
Name Size (KB)
.
.cache
.cadence
.cds_pegasus_ui
.config
.cbus
.imc
.java
.local
.mdv
.mozilla
.smvision
.ssh
.synopsys_dc_gui
.synopsys_k_gui
.synopsys_pt_gui
Bonus_formal_verification
Bonus_formal_verification_ans
Final_Project
Lab01
Lab02
Lab03
Lab04
Lab05
Lab06
Lab07
Lab08
Lab09
Lab11
Lab12
Lab13
Midterm_Project
OT_2024_Spring
worksheet
.bash_logout 1
.bash_profile 1
.bashrc 1
.flexmrc 1
.history 4
.kshrc 1
.kshrc_26585.txt 1
.kshrc_26585.txt 1
.viminfo 1

Remote monitoring
Follow terminal folder

PASS PATTERN NO.1957
PASS PATTERN NO.1958
PASS PATTERN NO.1959
PASS PATTERN NO.1960
PASS PATTERN NO.1961
PASS PATTERN NO.1962
PASS PATTERN NO.1963
PASS PATTERN NO.1964
PASS PATTERN NO.1965
PASS PATTERN NO.1966
PASS PATTERN NO.1967
PASS PATTERN NO.1968
PASS PATTERN NO.1969
PASS PATTERN NO.1970
PASS PATTERN NO.1971
PASS PATTERN NO.1972
PASS PATTERN NO.1973
PASS PATTERN NO.1974
PASS PATTERN NO.1975
PASS PATTERN NO.1976
PASS PATTERN NO.1977
PASS PATTERN NO.1978
PASS PATTERN NO.1979
PASS PATTERN NO.1980
PASS PATTERN NO.1981
PASS PATTERN NO.1982
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999

-----
Congratulation!
You have passed all patterns!
Your execution cycles = 32000 cycles
Your clock period = 20.0 ns
Total Latency = 640000.0 ns
-----
$finish called from file "PATTERN.v", line 36.
$finish at simulation time 1819630000
VCS Simulation Report
Time: 1819630000 ps
CPU Time: 27.230 seconds; Data structure size: 2.2Mb
Sat Jun 1 10:44:54 2024
CPU time: 1.778 seconds to compile + .406 seconds to elab + .626 seconds to link + 27.305 seconds in simulation
10:44 iclab104@ee22[~/Lab13/Exercise/06_POST]$
```

## 9. Power result :

Terminal Sessions View Xserver Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

4. /home/mobaxterm 7. iclab104

File Explorer: /RAD2/COURSE/iclab/iclab104/Lab13/Exercise05\_2

- DBS
- extLogDir
- layermap
- LEF
- LIB
- power\_log
- powerReports
- RC
- timingReports
- work
- .qor\_metric.td
- .top.power.db
- .top.power\_1.db
- 00\_combine
- 09\_clean\_up
- cellIDMap
- CHP\_CCOPT.spec
- CHP\_conn.rpt
- CHP\_conn.rpt.old
- CHP\_drc.rpt
- CHP\_drc.rpt.old
- CHP\_globals
- CHP\_inn
- CHP\_io
- CHP\_rpt
- CHP\_sdc
- CHP\_sdf
- CHP.v
- CHP\_uts.sdc
- CHP\_floorplan.inn
- CHP\_mmm.view
- CHP\_nandroute.inn
- CHP\_placement.inn
- CHP\_postCTS.inn
- CHP\_postRoute.inn
- CHP\_powerplan.inn
- CHP\_preCTS.inn
- CHP\_SHELL.v
- CHP\_SYN.v
- HT\_TOP\_SYN.v
- innovus.cmd
- innovus.cmd1
- innovus.cmd2

Terminal Output:

```
** WARN: (VOLTUS_POWR-2152): Instance VDDP6 (VCC3I0D) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP6 (GNDI0D) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDP7 (VCC3I0D) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDP7 (GNDI0D) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC0 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDC0 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC1 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDC1 (GNDKD) has no static power.
** WARN: (EMS-27): Message (VOLTUS_POWR-2152) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
*

Total Power
-----
Total Internal Power:      1.41310871      30.3241%
Total Switching Power:    1.38812836      49.3630%
Total Leakage Power:      0.00878843      0.3129%
Total Power:              2.80801550

** WARN: (VOLTUS_POWR-2841): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'itaputil list <uti-file>' command to get the list of instances.

** WARN: (VOLTUS_POWR-3424): Cell OR2S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN3B2S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell OAT222S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND2P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell NR2 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN4S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell A012P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MUX2 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MXL2HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell BUF2 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MA01S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell ND2S has no power pin defined in LEF/PGV.
```

Remote monitoring

Follow terminal folder

## 10. IR Drop Results :

In Lab12, I set utilization at 75%. This time, I set 70%. Additionally, I add more core power pads. There are 4 pairs in each side, 16 pairs in total.

