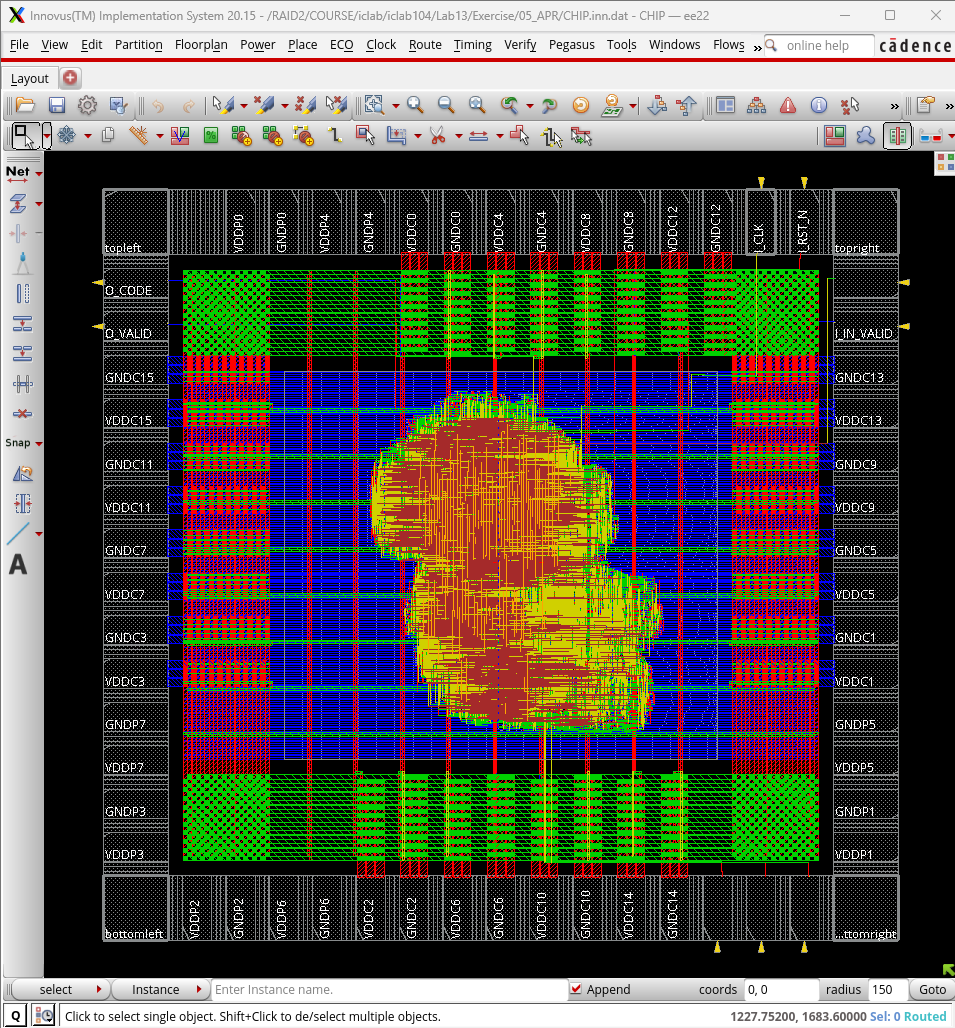
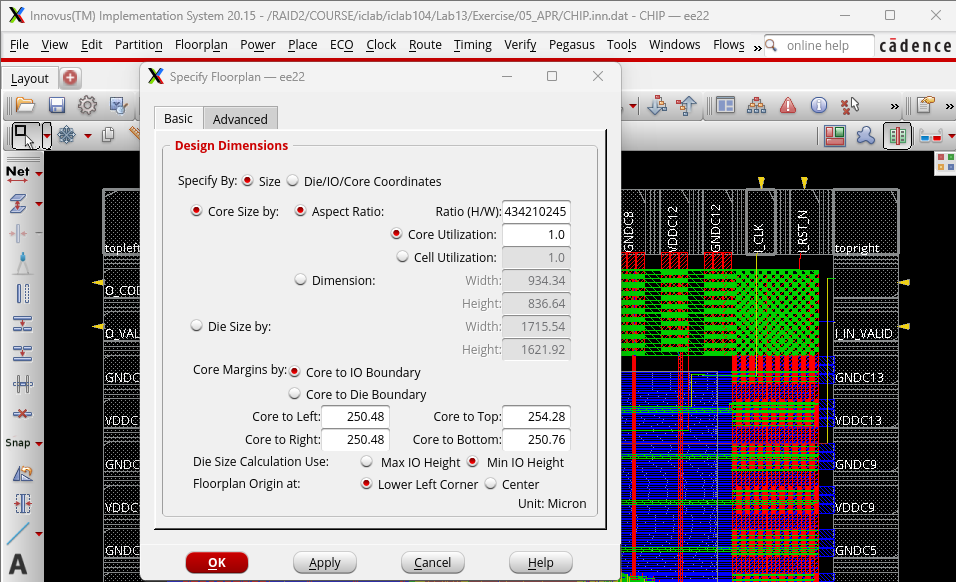
**Report**

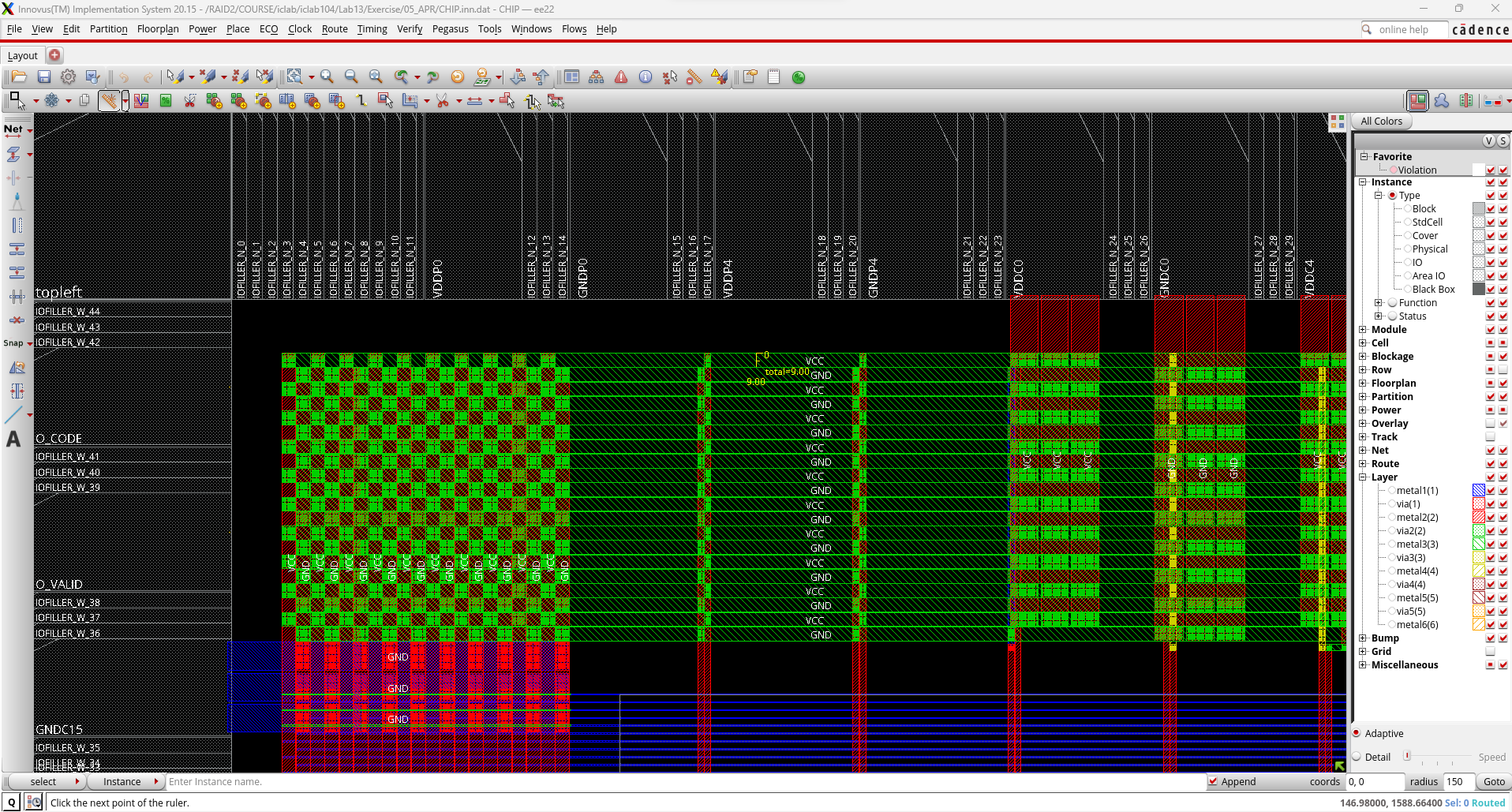
1. **Chip Layout View :**



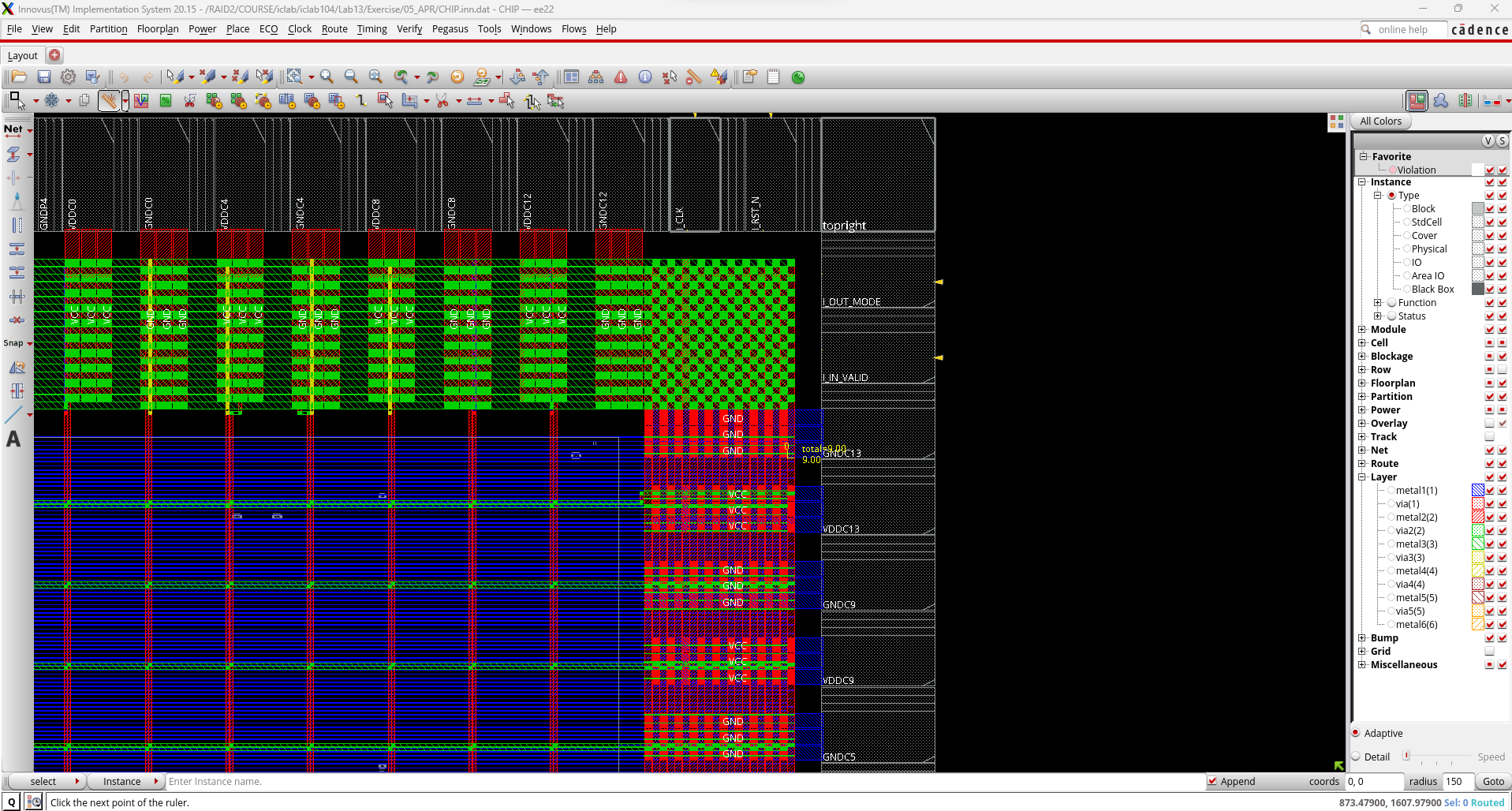
1. **Core to IO boundary :**



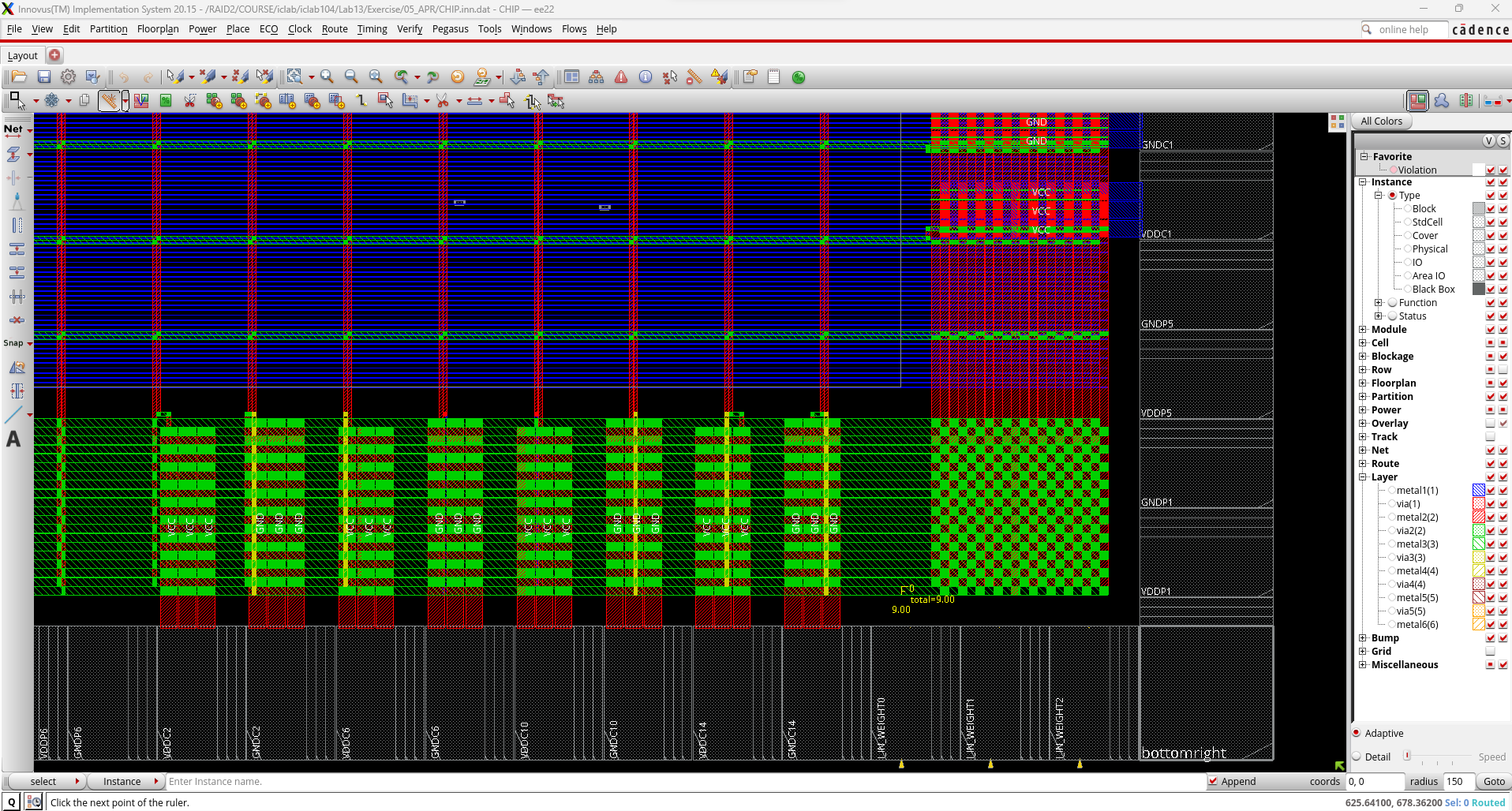
1. **Core Ring :**

****

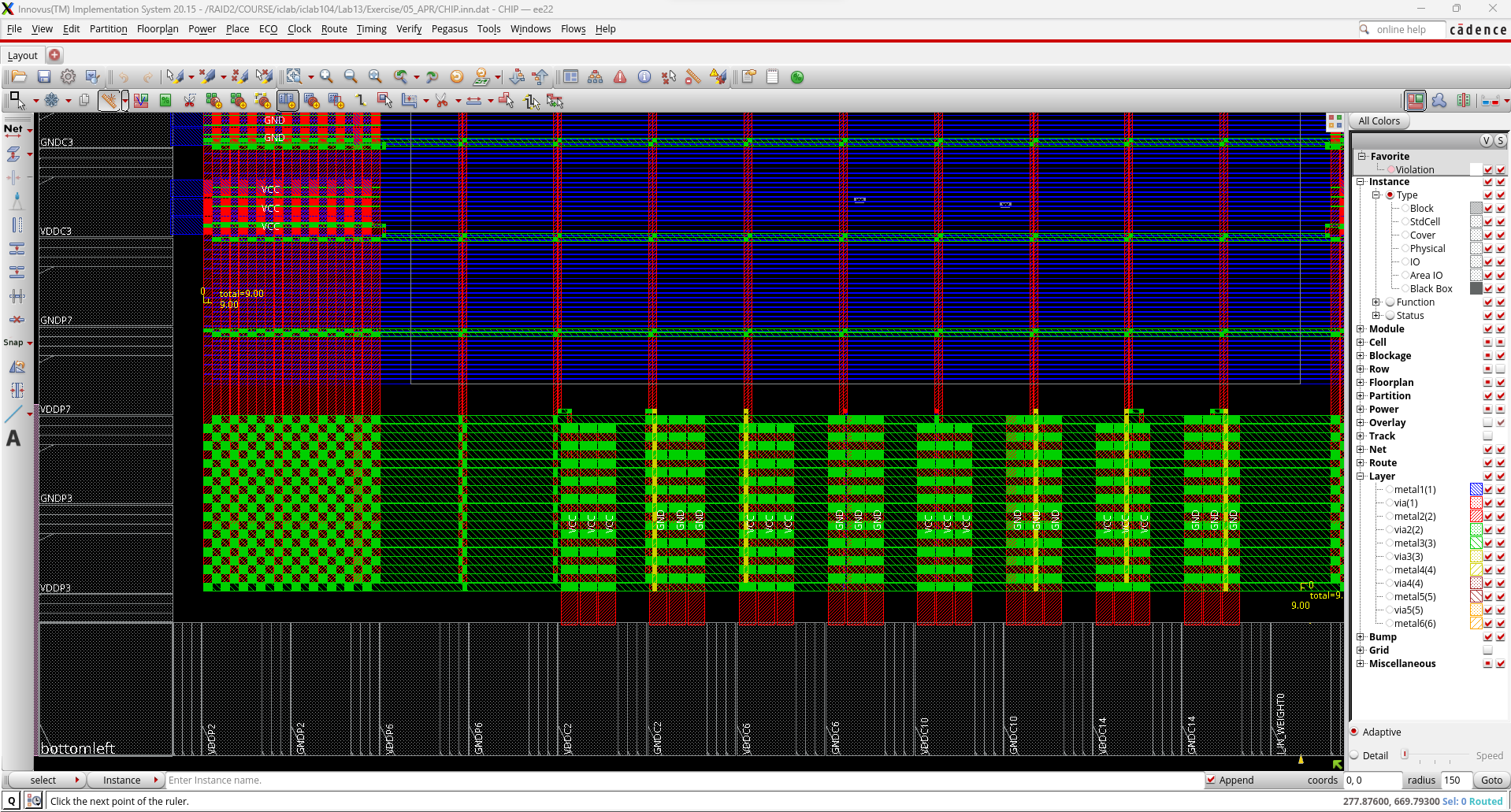
**(top)**

****

**(right)**

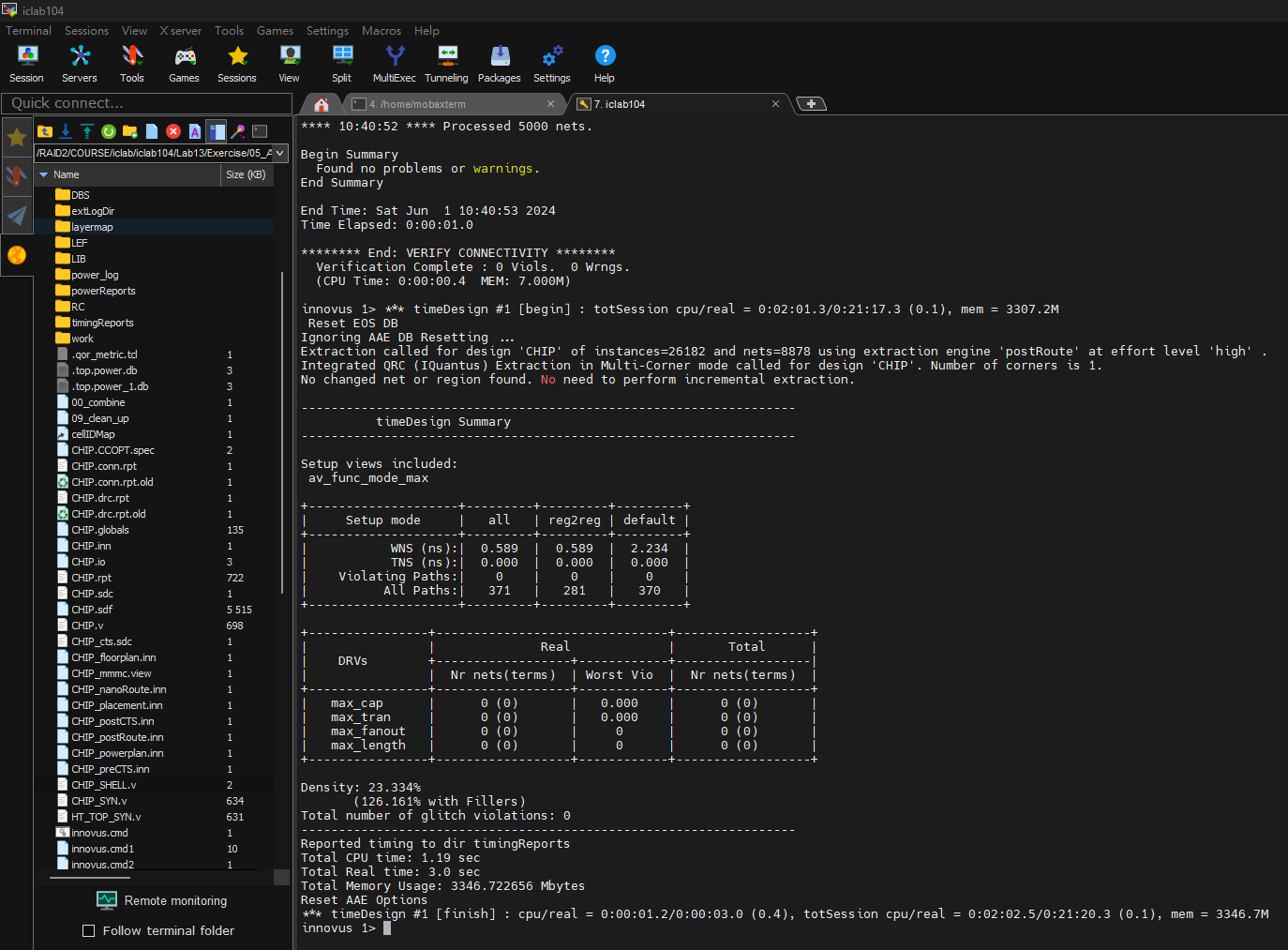
****

**(bottom)**

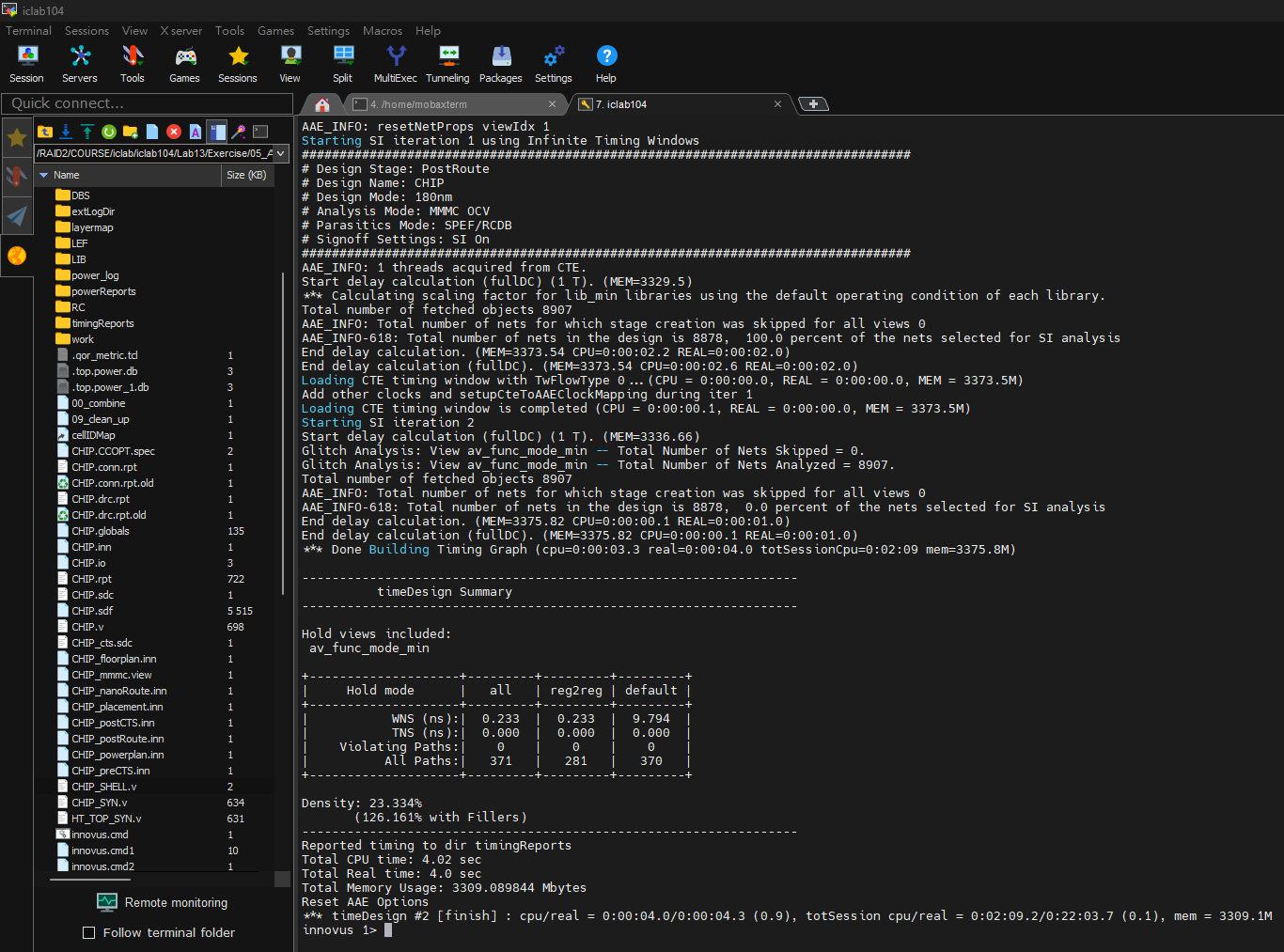
****

**(left)**

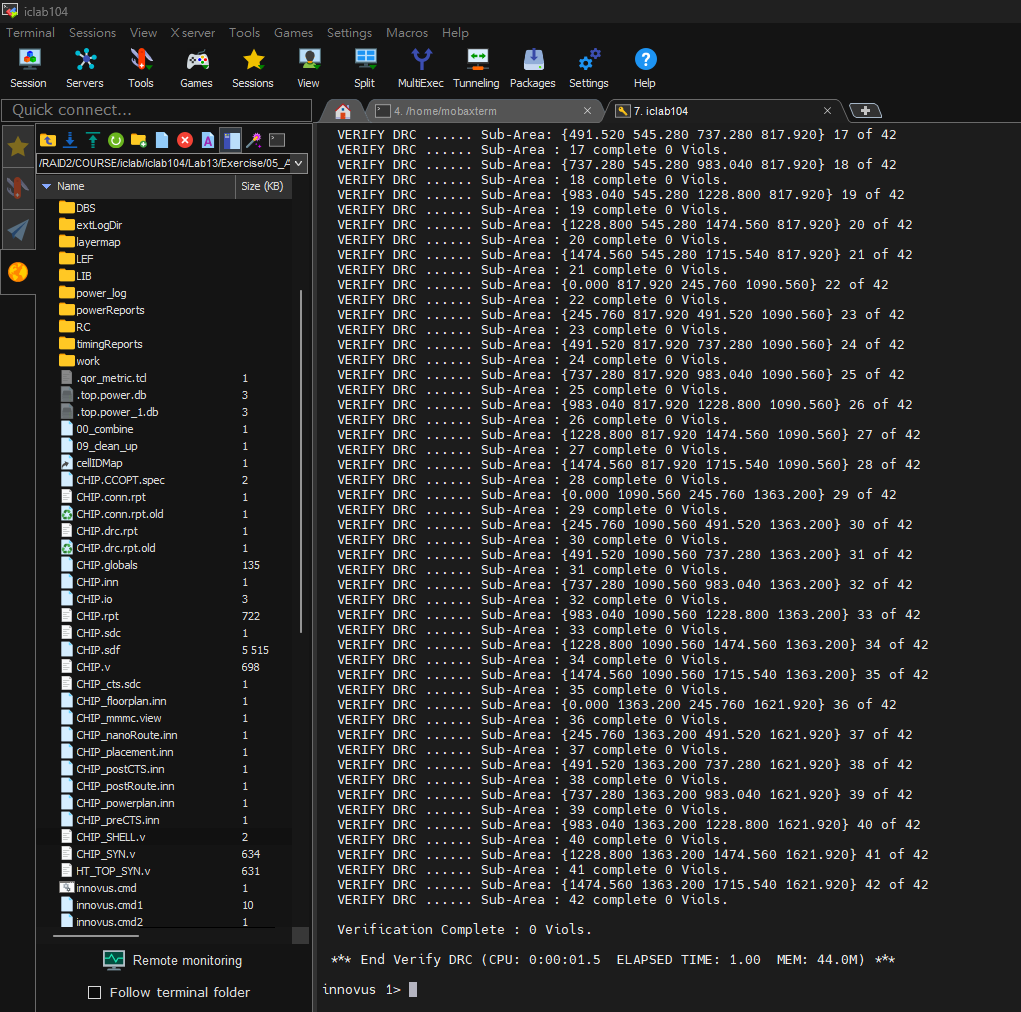
1. **Post-Route se**t**up time analysis :**

****

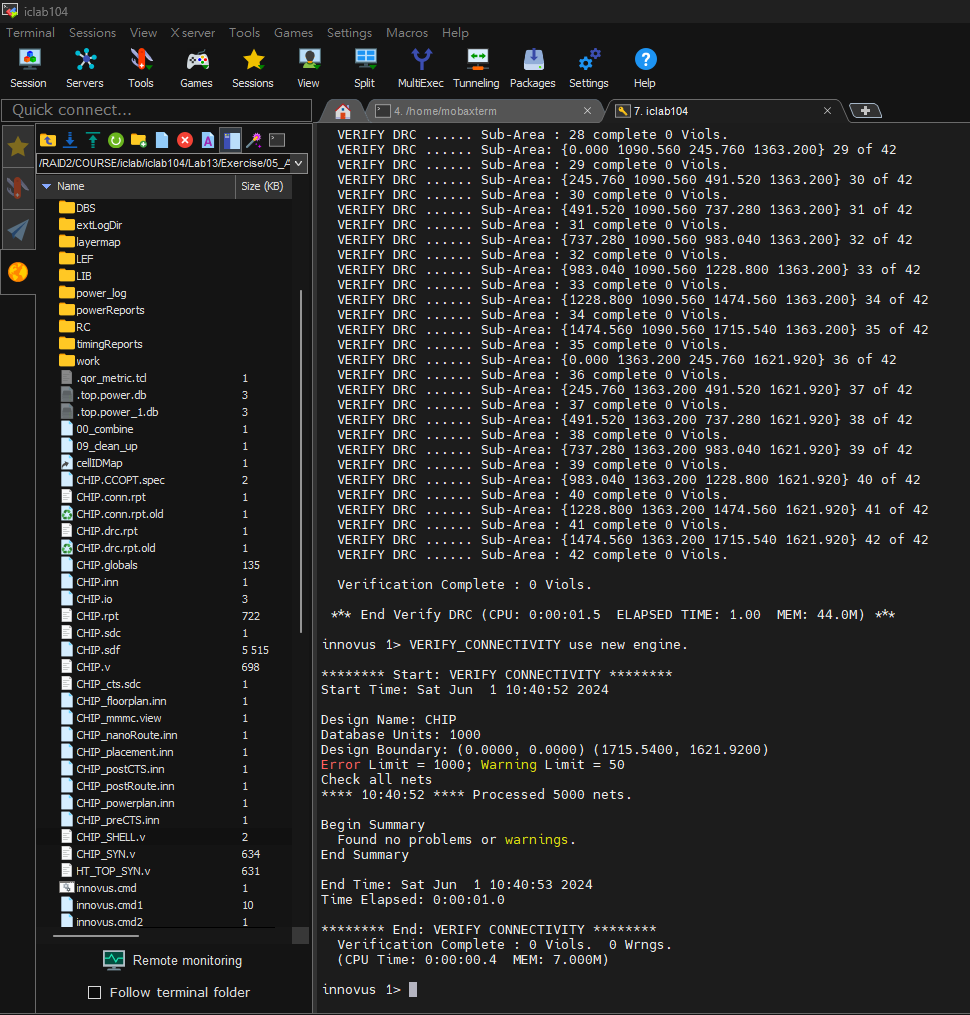
1. **Post-Route hold time analysis :**

****

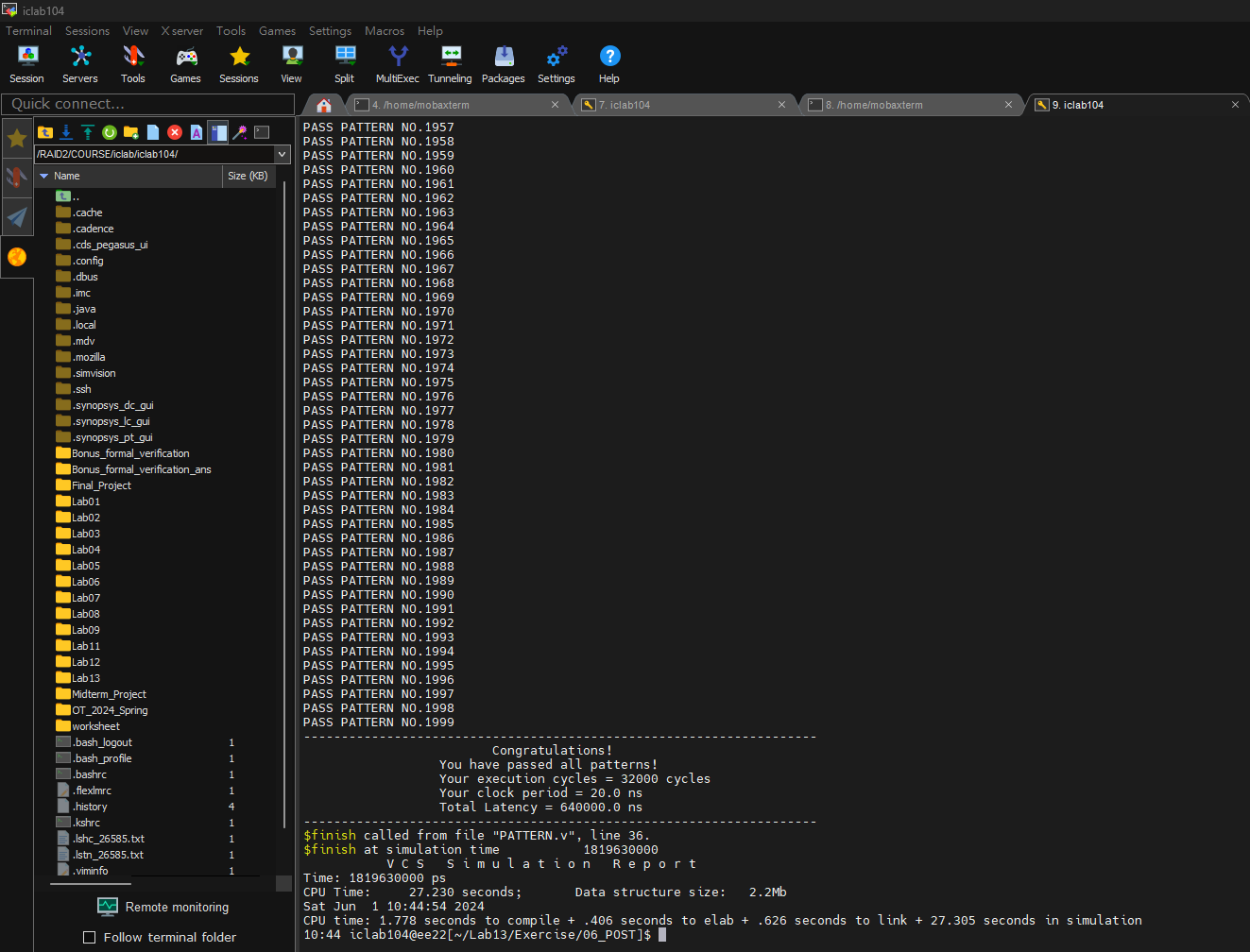
1. **DRC result :**

****

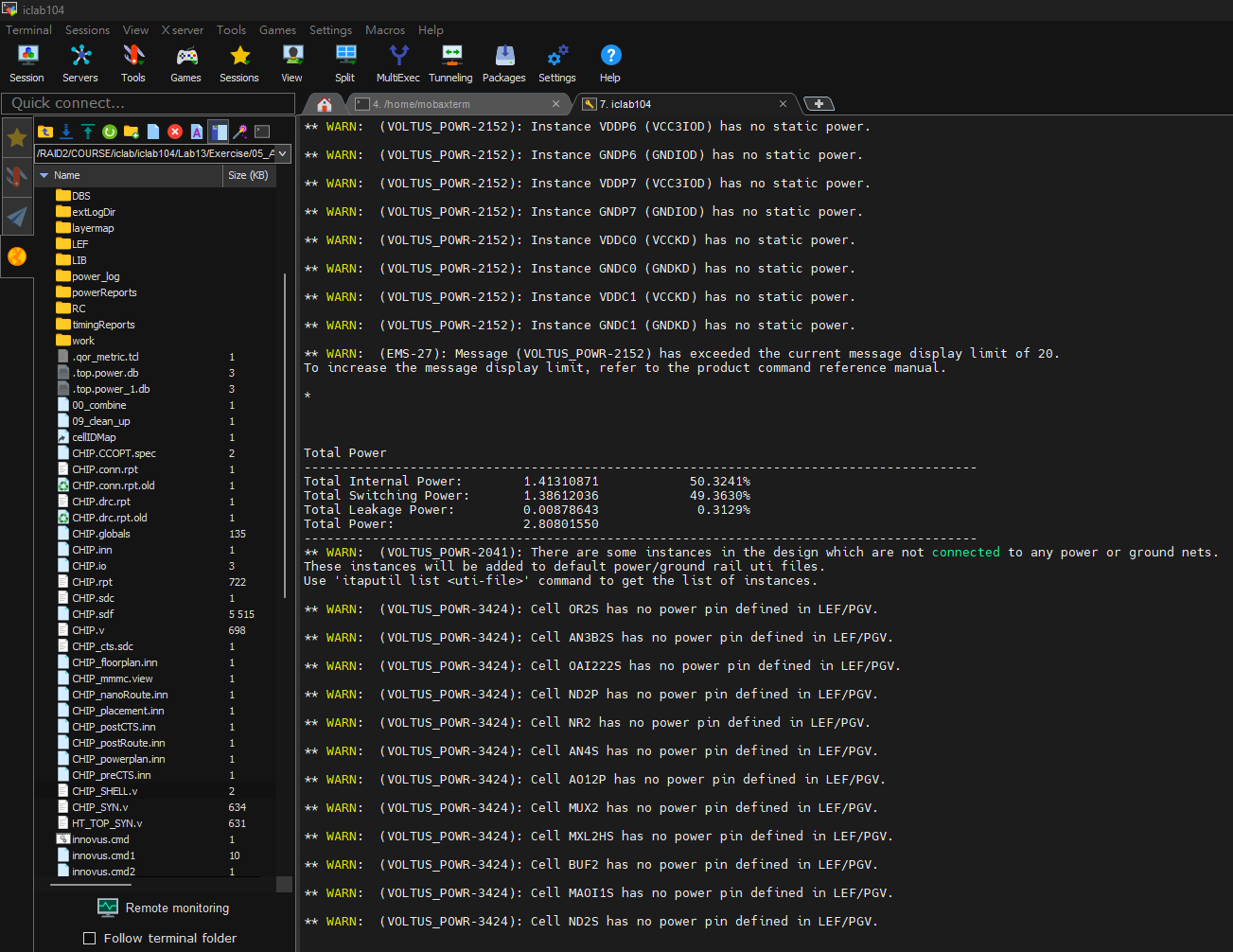
1. **LVS result :**

****

1. **Post Layout simulation result :**

****

1. **Power result :**



1. **IR Drop Results :**

In Lab12, I set utilization at 75%. This time, I set 70%. Additionally, I add more core power pads. There are 4 pairs in each side, 16 pairs in total.

