

Design and Optimization of 10-b SAR ADC: Achieving High Speed and SNDR

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Abstract—This paper presents the design of a 10-b Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) optimized for high sampling frequency, high Signal to Noise and Distortion Ratio (SNDR) and low static power consumption. The proposed architecture implements a binary-weighted capacitive Digital-to-Analog Converter (DAC) with top-plate sampling for high speed and a bootstrapped track and hold circuit for high linear sampling performance. A double-tail dynamic latch comparator is implemented to utilize the pre-amplifier gain to decrease the input-referred noise of the comparator. The ADC achieves a peak SNDR of 55.9 dB with a sampling frequency of 98.1 MHz and a power consumption of 617.6 μW .

Index Terms—SAR ADC, Double-Tail Dynamic Comparator, Bootstrap Track & Hold, Binary-Weighted DAC

I. INTRODUCTION

SUCCESSIVE Approximation Register (SAR) ADCs have become a cornerstone in mixed-signal systems due to their ability to balance power efficiency, high resolution, and reduced implementation complexity. Their compact size makes them ideal for applications in portable and wearable electronics [1]. This paper provides a comprehensive exploration of SAR ADC design, highlighting key building blocks such as the comparator, Digital-to-Analog Converter (DAC), and Track-and-Hold (T/H) circuitry. The comparator utilizes the double-tail latch architecture and is optimized for high sampling frequency, while the T/H circuit employs bootstrapped switches to enhance linearity and minimize charge injection. The DAC utilizes a binary-weighted capacitive array with control switches designed for fast switching via transmission gates. Through theoretical analysis and circuit simulations in Cadence Virtuoso, this work demonstrates a complete design workflow for a fully functional 10-b SAR ADC, addressing critical design challenges and performance trade-offs. Figure 1 shows the high level architecture of the proposed SAR ADC.

This design minimizes the Figure of Merit $\frac{P}{f_s^2}$ by prioritizing a high sampling frequency (f_s) and achieves a FOM of $6.41 * 10^{-20} \text{W}/\text{Hz}^2$.

II. SAR ADC ARCHITECTURES

A. Bootstrapped Track and Hold Design

The performance of a SAR ADC heavily depends on the linearity and the accuracy of the sampling process. A bootstrapped switch is commonly used to improve the performance of the sampling circuit, specifically in high-speed SAR ADCs. This added circuitry maintains a constant voltage across the gate and source terminals of the switching transistor during operation and prevents the change in its resistance due to

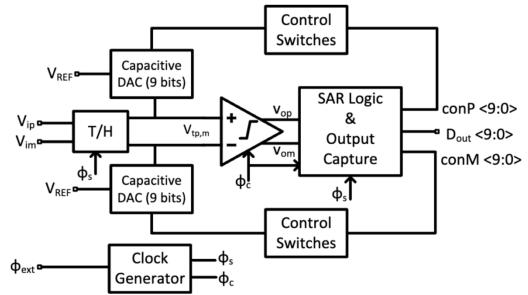


Fig. 1. High-level block diagram for SAR ADC

variations in the input signal. Reducing the nonlinearity from the switch's on-resistance, the bootstrapped track and hold minimized distortion and results in an improved SNDR.

A commonly accepted bootstrap circuitry is implemented in this SAR ADC architecture [2-3]. Figure 2 shows the bootstrap design for one of the differential inputs to the comparator.

The design choices for components C_3 and M11 are critical for the circuit's performance. Transistor M11 is made larger than auxiliary transistors as it lies directly in the signal path, minimizing R_{on} and ensuring better linearity. While other transistors are also scaled up to improve the SNDR, this leads to increased power consumption. However, this trade-off is justified given the importance of SNDR in this block's operation. For this SAR ADC, M11 is 10 μm in width, auxiliary transistors are 3 μm in width and C_3 is 1 pF. All transistors in this SAR ADC are 90 nm in length.

Capacitors C_1 and C_2 are designed to be very small to prevent spikes in the gate voltage. Larger capacitance would lead to these spikes propagating into the gate voltage, causing the track-and-hold circuit to continue tracking even after the sampling period and resulting in degraded accuracy. Therefore, those capacitors are chosen to be a value of 1 fF. Additionally, two inverters are used to generate $\bar{\phi}$ and ϕ_x , where ϕ_x is the output of the inverter connected to C_2 . These inverters are implemented with large transistors to ensure a clean and robust clock signal, further improving circuit reliability and performance. A transient simulation waveform is provided in Appendix A1, and a complete circuit schematic with transistor widths and lengths labeled is provided in A2.

B. Capacitive DAC and Control Switches

Binary-weighted capacitive DAC is implemented in many SAR ADC architectures as it provides a precise and low-power digital-to-analog conversion during operation with an easy implementation through direct binary scaling. Top-plate

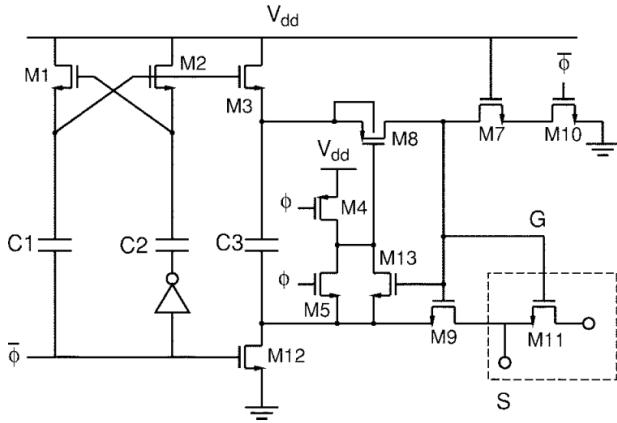


Fig. 2. Bootstrap circuit and switching device

sampling is also preferred over bottom-plate sampling for this architecture as it enables a simpler design for a lower-resolution ADC.

There are two key design challenges for the control switches in the SAR ADC. Firstly, it is crucial that all control signals from the SAR logic reach V_{DD} within half a cycle of the comparator clock period. This requirement ensures proper switching behavior and is addressed by using larger transistors for control signals associated with higher capacitance values, thereby reducing R_{ON} . To achieve this, transmission gates are used instead of NMOS-only switches, as they provide better on-resistance characteristics across the voltage range. In terms of transistor sizing, the RC time constant is kept uniform across all switches. Starting with a minimum width of 180 nm for the smallest capacitor, transistor sizes are scaled up in powers of two to match the increasing capacitance values. However, control switches 8 and 9 are kept at 32 times unit width instead of 64 and 128 to minimize rise time increased by capacitance. Figure 3 shows the circuit for one of the control switches with transmission gates and design parameters. The complete circuit diagram of all control switches can be found in A3.

Secondly, it is important to ensure that the inverters driving the control signals can sufficiently drive the larger transistors. In this design, the limiting signals were control signals 7 through 9, as the larger devices have a larger gate capacitance. To optimize for power while maintaining performance, only the inverters for these signals were modified, with the PMOS and NMOS transistor sizes set to 2 μm and 1 μm , respectively. The parameter sweep executed for this decision is provided in Appendix A4 and the transient simulation waveform for this block is provided in A5.

C. Comparator

When choosing a comparator architecture, various designs have trade offs between optimizing noise, speed, and power [4]. Given that the overall goal when designing the SAR ADC is to minimize the FOM, of all trade offs available, speed is the most critical. As long as the noise requirement is met, the

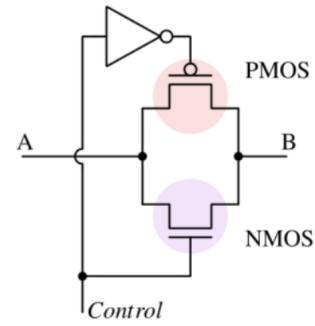


Fig. 3. Single DAC control signal switching block with transmission gate implementation.

design flow of the comparator will be to optimize for speed in every manner possible.

The double-tail dynamic latch comparator, shown in Figure 4, was chosen to be implemented over a traditional architecture such as the Class-A or Class-AB Comparator because this design is able to operate at much higher frequencies due to the large input current from the high-side tail MOSFET M12, allowing for a quicker regeneration period relative to the other architectures mentioned. There are also additional benefits in using this architecture, such as improved noise and power. First, the architecture inherently produces less input-referred noise compared to its counterparts because of the pre-amplifier stage which will reduce the output-referred noise by $|A_v|$, the gain of the pre-amplifier. This will allow for easier implementation of MOSFETS using minimal switch widths, which inherently have higher noise but are able to operate at higher frequencies. Second, the architecture operates dynamically, meaning there is no static power consumption from this design, providing significantly less overall power consumption compared to the other architectures previously mentioned (which both consume static power).

Typically in ADC design the comparator is the dominant factor in both noise and power consumption, and is also responsible for setting the maximum switching frequency of the ADC (i.e. the ADC speed is limited by the comparator). In this case, choosing transistor widths must be done carefully in order to maximize speed. Ultimately there are six design parameters in this design: the widths of M12, M9, M5/M6, M7/M8, M10/M11, and M1/M2/M3/M4. Of the six design parameters, the widths of M5/M6, M12, and M1/M2/M3/M4 are the most critical in optimizing for speed.

The width of M9 was chosen to be the minimum width of 180 nm, as this transistor width should be minimized to reduce comparator offset. M9 is mainly responsible for allowing a path for current to flow during regeneration, and a larger M9 equates to a higher offset. As for M12, this device should be as wide as possible to create a large current during the latching phase of operation, allowing quicker regeneration. Increasing the width of M12 also decreases the noise created by the comparator. After conducting a parametric sweep in

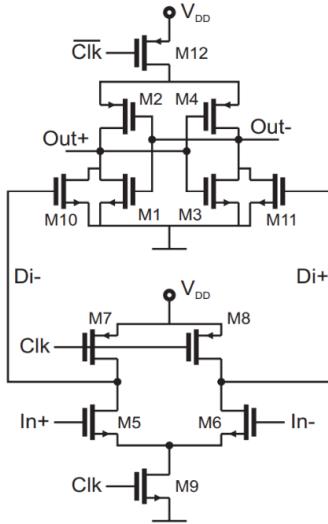


Fig. 4. Double-Tail Dynamic Latch Comparator Circuit

Cadence Virtuoso to analyze the noise, the width of M12 was chosen to be 5 μm , as increasing the width beyond 5 μm has minimal impact on the noise and only serves to dissipate more power; this width is sufficiently large to provide a large current relative to what the minimal sizing would provide. The results of the parametric sweep is shown in Appendix A6. To generate the $\overline{\text{CLK}}$ signal, an inverter with minimum sizing (NMOS width of 180 nm and PMOS width of 360nm) was chosen in order to minimize the delay from CLK to $\overline{\text{CLK}}$ to maintain synchronous operation.

Transistors M7 and M8 are utilized in pulling nodes Di+ and Di- to V_{DD} during reset, and are not active during regeneration. These transistors have minimal impact on noise and power as they are not on the signal path and are only active for reset. The widths of M7 and M8 were chosen to be 1.5 μm ; the sizing of these transistors are not critical to performance but do dictate the speed in which Di+ and Di- can be driven to V_{DD} . This width allows for slight reduction in noise with minimal impact on speed compared to the minimum width. M10 and M11 are also responsible for resetting the comparator, but M10 and M11 are on the signal path and contribute to the noise. In this case the noise is reduced linearly as the width increases, but causes a reduction in speed. M10 and M11 were chosen to have a width of 2 μm , slightly higher than M7 and M8 to utilize the reduction in noise.

The sizing of the cross-coupled inverters (M1-M4) was designed to minimize noise, as the inverters connect directly to the output. The unit width of these transistors was chosen to be 2 μm , with M1 and M3 at 2 μm and M2 and M4 at 4 μm ; a parametric sweep in Cadence Virtuoso showed that increasing the unit width beyond 2 μm had minimal impact on reducing the noise, and is shown in Appendix A7.

Finally, for the sizing of M5 and M6, the key factors in choosing a size are overall speed and amplifier gain. A transient simulation of the comparator output voltage was conducted with varying widths ranging from 1 μm to 5 μm . A width of 3 μm proved to be the fastest; this transient

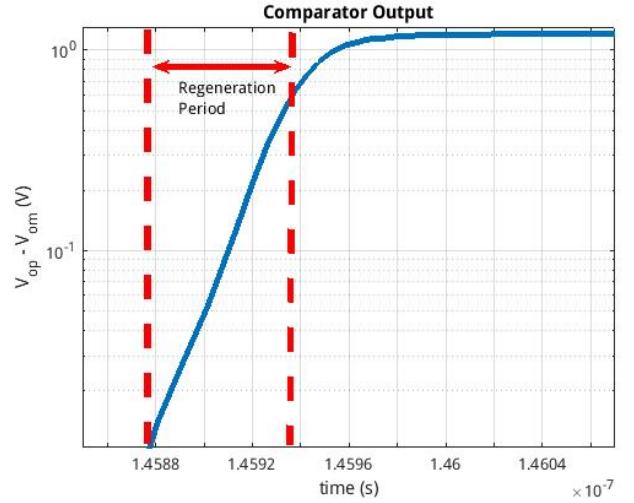


Fig. 5. Comparator output voltage waveform during regeneration.

plot is shown in Appendix A8. This sizing produced a gain of 16.27. Schematics of test benches used in comparator design are shown in Appendix A9 and A10, and a complete circuit schematic with transistor widths and lengths labeled is provided in A11.

With all transistor widths chosen for the comparator, a final transient analysis was conducted to calculate the maximum frequency of operation. Figure 5 shows $(\text{Out}+) - (\text{Out}-)$, the comparator output voltage during regeneration. Note the logarithmic y-axis as the regeneration occurs exponentially due to the positive feedback of the cross-coupled inverters. The slope of the line during the regeneration period provides τ_{reg} , the regeneration time constant. From the constraint of metastability (10^{-7}), along with τ_{reg} , and the gain of the preamplifier $|A_v|$, the maximum frequency is defined as:

$$f_{s,max} = \frac{1}{12(2\tau * \ln(\frac{V_{PP}}{P_{meta} * \frac{L_{SB}}{2} * |A_v|}))} \quad (1)$$

Note that $\tau = \tau_{reg} + t_{delay}$, where t_{delay} is the delay from the CLK signal switching to the time regeneration begins. The factor of 12 in the denominator is due to the conversion from external clock frequency to comparator sampling frequency.

III. SIMULATION RESULTS AND DISCUSSION

Full integration of the designed track & hold, comparator, control switches, and capacitative array with metal-insulator-metal (MIM) capacitors allowed all specifications to be met at the calculated $f_{s,max} = 89.1\text{MHz}$. The design has an SNDR above 55 dB with metastability upper bound of 10^{-7} , dissipates 617.64 μW of power, and has a FOM of $6.41 * 10^{-20}\text{W}/\text{Hz}^2$. Table 1 displays all these metrics, as well as some basic simulation parameters.

To verify the SNDR measurement, transient noise simulations were conducted at both low ($f_{in} = 3/64f_s$) and near Nyquist ($f_{in} = 31/64f_s$) input frequencies, and the fft was calculated in MATLAB; the script can be found in the Appendix. Figure 6 shows the resulting fft plot at low

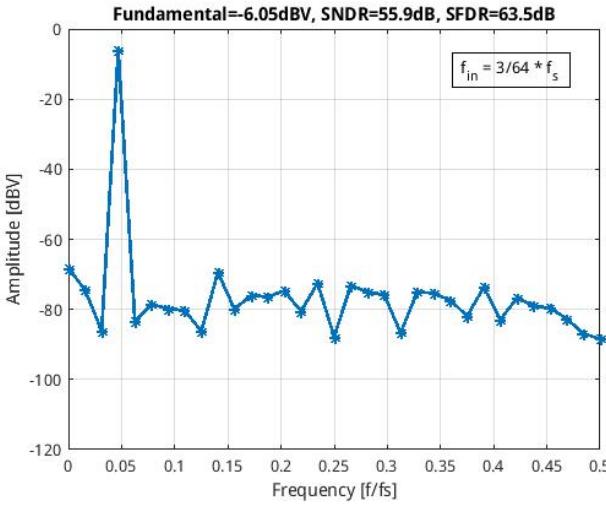


Fig. 6. FFT Plot at $f_{in} = 3/64 * f_s$. This verifies the SNDR specification is met at low frequencies.

frequencies, with an SNDR = 55.9 dB; Figure 7 shows the resulting fft plot at near Nyquist frequencies, with an SNDR = 55.1 dB. The total power consumption is on par with other 10-b ADCs in the literature [5]. The dynamic operation of the comparator helps to reduce overall power consumption.

TABLE I
DESIGN VARIABLES OF 10-B SAR ADC

Specification	Value	Units
V_{DD}	1.2	V
T	27	°C
W_{min}	180	nm
L_{min}	90	nm
SNDR	>55	dB
C_{min}	2.5	fF
V_{ic}	0.4 - 0.8	V
f_s	-	MHz
$V_{in,amp}$	-	V
V_{ref}	-	V
P_{DISS}	-	μW
FOM	$6.41 * 10^{-20}$	W/Hz ²

One very important factor to successful and smooth integration was robust testing of each individual component. When both the track & hold and comparator were isolated individually with all other components ideal, both circuits produced an SNDR of 61 dB. When the comparator and track & hold were integrated with the control switches and ideal capacitor bank, the system produced an SNDR of 57 dB. Once the final integration test was conducted, when converting the ideal capacitor bank to MIM capacitors, the resultant SNDR dropped to 47 dB. This lead to mass confusion and several days of simulation tests to try and debug the circuit. Originally the belief was that the control switches were the issue. After conducting numerous parametric sweeps, the noise

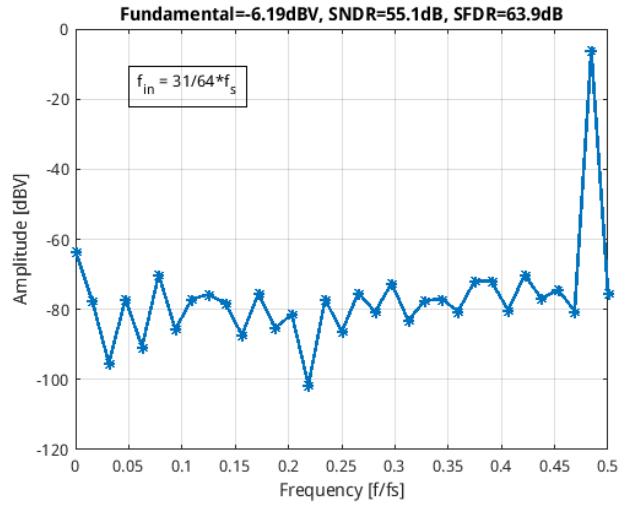


Fig. 7. FFT Plot at $f_{in} = 31/64 * f_s$. This verifies the SNDR specification is met at high (near $f_s/2$) frequencies.

would not change. Ultimately the issue was resolved, and was not a circuit issue but rather a simulation setup issue. When changing the ideal capacitors to MIM capacitors, the parasitic capacitance of 1% on the top plate changed the full scale voltage V_{FS} from 1.98 V to 1.96 V. This change was not correctly reflected in the simulation setup, as the input amplitude needed to be adjusted to correctly reflect the new V_{FS} . The incorrect amplitude resulted in the output signal clipping, limiting the SNDR regardless of what circuit parameters were changed. After this issue was fixed, the SAR ADC operated as designed. A transient plot showing the input signal and output signal are provided in A12.

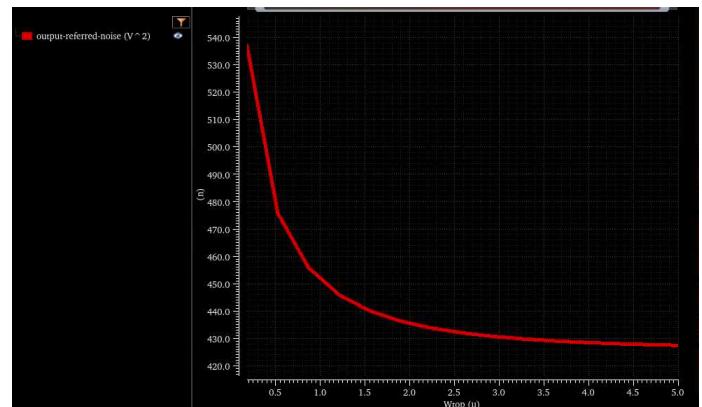
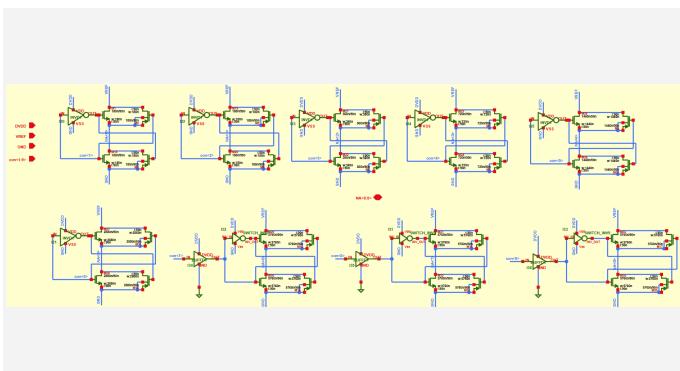
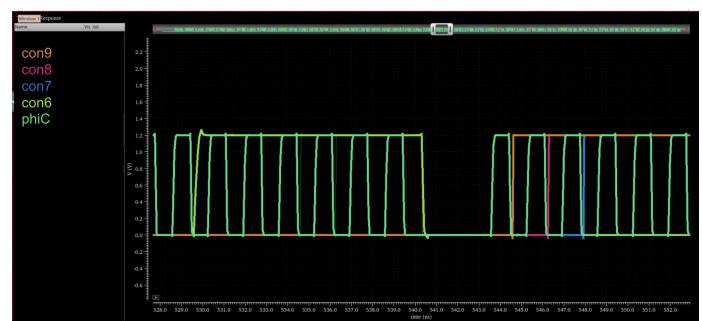
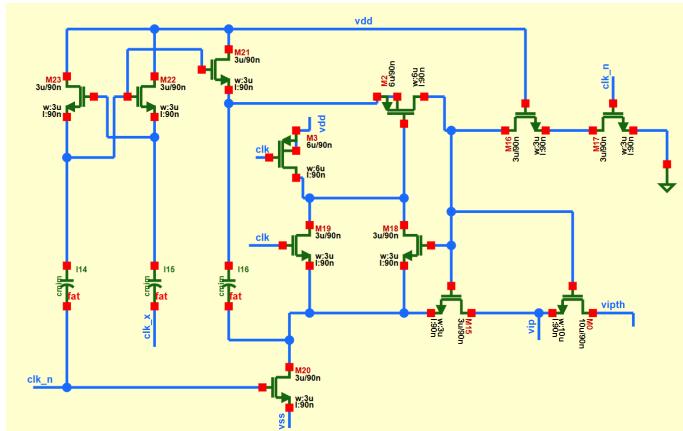
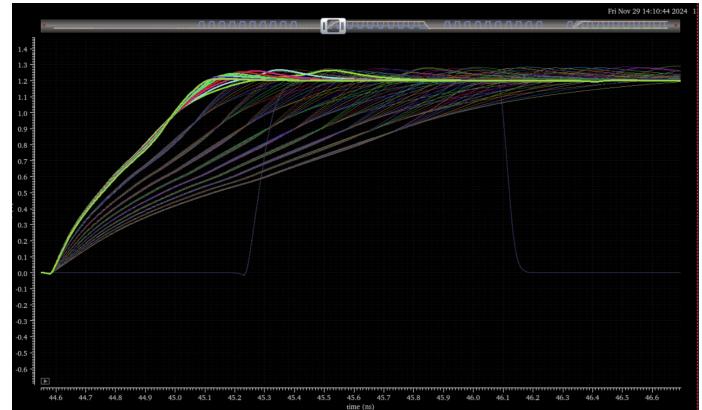
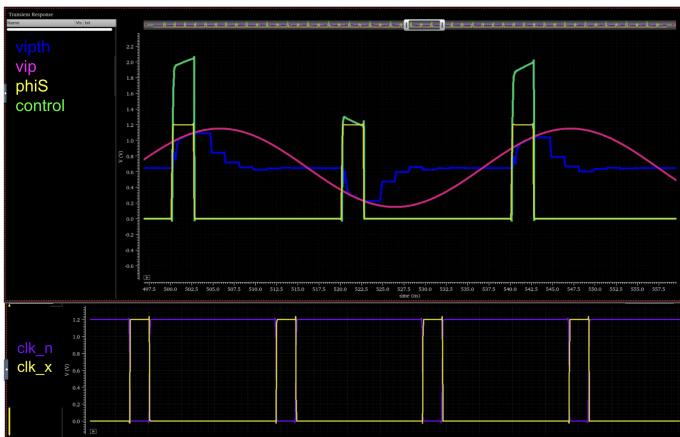
IV. CONCLUSION

Overall, the 10-b SAR ADC design was able to meet all required specifications and operate as a sampling frequency of 98.1 MHz. The bootstrapped track and hold design, double-tail latch dynamic comparator, and binary-weighted capacitive array with MIM capacitors switched with transmission gate control switches all function to make up the analog circuitry of the SAR ADC. Each individual circuit is discussed in great detail and design choices are discussed for the values of each component. This design is able to achieve high speeds and SNDR with low power consumption.

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APPENDIX



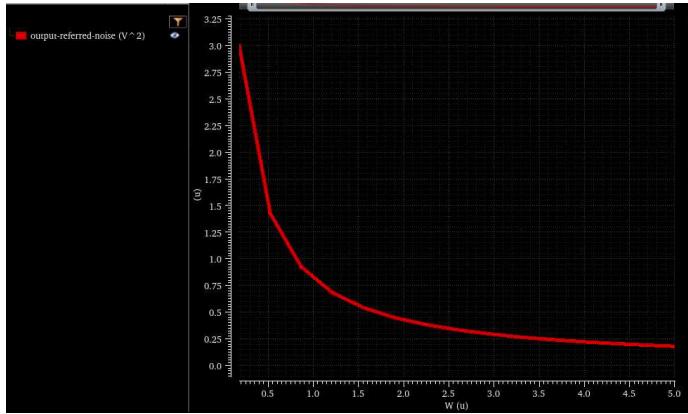


Fig. A7. Parameter sweep for M1-M4 in the comparator shows that increasing the width beyond 2 μm has minimal impact on the noise. Increasing the width from the minimum size of 180 nm greatly reduces noise.

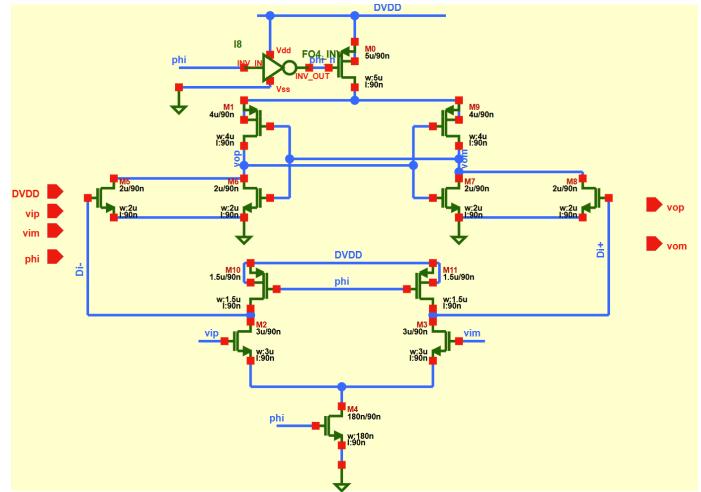


Fig. A11. Circuit diagram of designed double-tail latch comparator. All transistor widths and lengths are labeled.

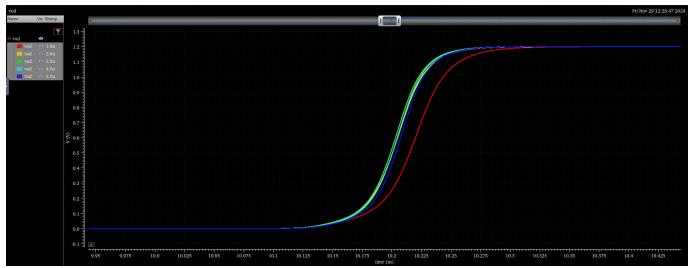


Fig. A8. Various transient plots of the comparator output voltage during regeneration as a function of M5, M6 width. From this transient plot it is apparent that choosing a width of 3 μm yields the fastest regeneration.

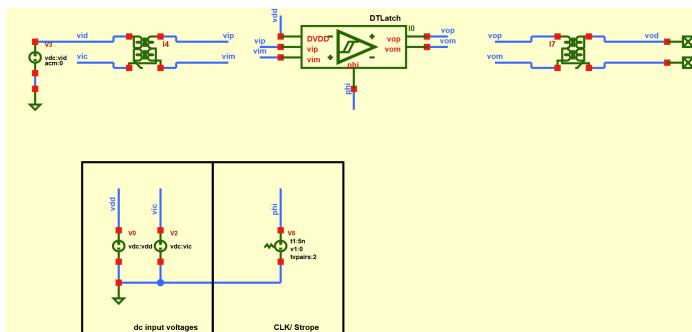


Fig. A9. Schematic of comparator test bench used for analyzing transients. The balun at the comparator output allowed for easy plotting of the output voltage.

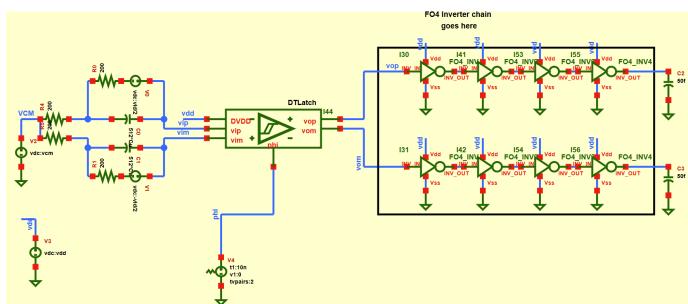


Fig. A10. Schematic of comparator test bench used for integrating capacitive loading of the inverter chain and how it affects transient waveforms and t_{regen} .

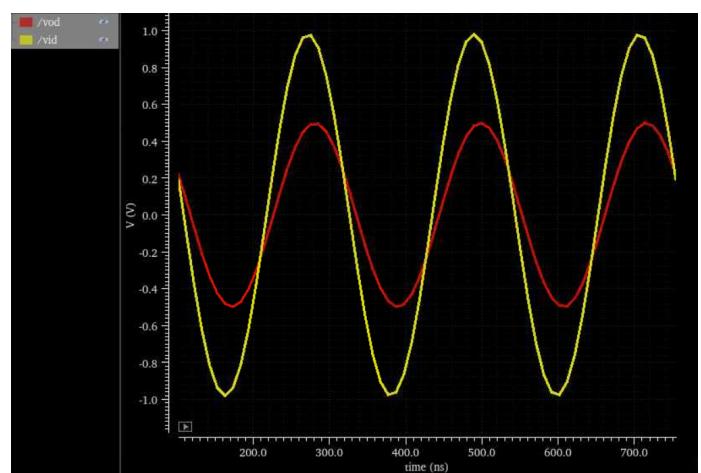


Fig. A12. Cadence Virtuoso transient analysis results with designed SAR ADC. The original input signal (yellow) and sampled output signal (red) are plotted.

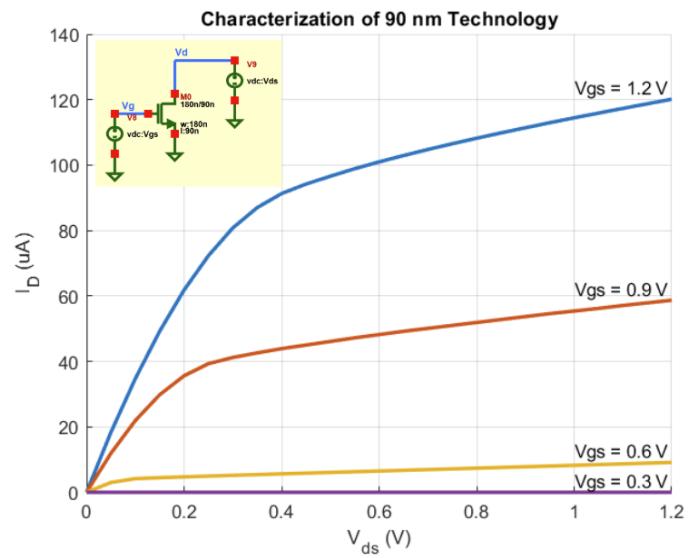


Fig. A13. I_D vs. V_{DS} curves of 90 nm technology at various gate voltages. These curves aided the design process when considering I_D and R_{ON} .

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EE 315 Final Project Calculations

Burcu Gulsah Alici & Steven Abrego

```
clear; close all; clc;

% Basic Device Parameters
Vdd = 1.2;
Vref = 1;
Vfs = 0.98*2;
B = 10;
LSB = Vfs / 2^B;
Pmeta = 10^-7;
```

90 nm Technology Characterization

```
mosfet_id = load('90nm_Id_Vds_Curves.csv');

x = mosfet_id(:, 1);
y1 = mosfet_id(:, 2)*10^6;
y2 = mosfet_id(:, 4)*10^6;
y3 = mosfet_id(:, 6)*10^6;
y4 = mosfet_id(:, 8)*10^6;
y5 = mosfet_id(:, 10)*10^6;

% Plot of 90 nm Technology Characterization (already included in Appendix)
% figure;
% hold on;
%
% plot(x, y1, 'LineWidth', 2);
% plot(x, y2, 'LineWidth', 2);
% plot(x, y3, 'LineWidth', 2);
% plot(x, y4, 'LineWidth', 2);
%
% xlabel('V_d_s (V)');
% ylabel('I_D (uA)');
% title('Characterization of 90 nm Technology');
% text(1, y1(end), ['Vgs = 1.2 V'], 'HorizontalAlignment', 'left', 'VerticalAlignment', 'bottom');
% text(1, y2(end), ['Vgs = 0.9 V'], 'HorizontalAlignment', 'left', 'VerticalAlignment', 'bottom');
% text(1, y3(end), ['Vgs = 0.6 V'], 'HorizontalAlignment', 'left', 'VerticalAlignment', 'bottom');
% text(1, y4(end), ['Vgs = 0.3 V'], 'HorizontalAlignment', 'left', 'VerticalAlignment', 'bottom');
%
% grid on;
% hold off;
%
%
```

Comparator

```
Av = 16.27;

% t1,t2, t_delay, and v1, v2 are results from transient analysis in Cadence Virtuoso
t2 = 202.602e-9; t1 = 202.5e-9;
v2 = 245e-3; v1 = 59.2e-6;
t_regen = (t2 - t1) / log(v2/v1)
t_delay = (202.446-202.4375)*10^-9
fsmax = 1 / (24*(t_regen+t_delay)*log(Vdd/(Pmeta*LSB/2*Av)))

Fmax = 10 / (2*pi*(t_regen+t_delay))

% Output Noise from noise analysis in Cadence Virtuoso
Output_Noise_rms = sqrt(8.1981e-7);
Input_Noise_rms = Output_Noise_rms / Av;

% Calculated quantization noise and sampling noise
P_quant = 3.18e-7;
P_samp = 6.47e-9;
P_comp = Input_Noise_rms^2;

Psig = (Vfs/2)^2/2;
Pnoise = P_comp + P_quant + P_samp;

Estimated_Comparator_SNR = 10*log10(Psig / Pnoise)

%
%
%
%
%
%
```

```
t_regen =
1.2248e-11

t_delay =
8.5000e-12

fsmax =
9.8142e+07

Fmax =
7.6710e+10

Estimated_Comparator_SNR =
61.6612
```

FOM Calculation

Currents extracted from Cadence Virtuoso (average value of 50 cycles in steady state)

```
Iavg_vdd = 394.2e-6;  
Iavg_vref = 144.6e-6;  
  
Total_ADC_Power = Iavg_vdd * Vdd + Iavg_vref * Vref  
  
FOM = Total_ADC_Power / (fsmax)^2
```

Total_ADC_Power =

6.1764e-04

FOM =

6.4125e-20

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FFT Analysis

```
clearvars;
close all;

% load sim output
vod_=cds_srr('simulation/ee315_finalProject/spectre/schematic/psf','tran-tran','vod');

% read into matlab variables
t    = vod_.time;
vod  = vod_.V;
N    = length(t)-1;

% if first and last point don't match within good precision, the fft data is garbage...
delta = vod(1)-vod(end)
if abs(delta)>10e-6
    disp('This looks like inaccurate fft data... ');
    beep
end

spectrum = abs(fft(vod(2:end)));
spectrum = 2/N*spectrum(1:N/2+1);
spectrumdb = 20*log10(spectrum+eps);
frequency = 1/N * (0:length(spectrumdb)-1);

[fund, fundidx] = max(spectrum);
funddb=20*log10(fund);
spec_nodc_nofund = [spectrum(2:fundidx-1); spectrum(fundidx+1:end)];
[spur, spuridx] = max(spec_nodc_nofund);

sfdrdb = funddb-20*log10(spur);
snr = norm(fund)/norm(spec_nodc_nofund);
snrdb=20*log10(snr);
funddb=20*log10(norm(fund))
nofunddb=20*log10(norm(spec_nodc_nofund))
norm(fund)
norm(spec_nodc_nofund)

figure(1);
plot(frequency, spectrumdb, '*-', 'linewidth', 2);
string = sprintf('Fundamental=%0.3gdBV, SNDR=%0.3gdB, SFDR=%0.3gdB', funddb, snrdb, sfdrdb)
title(string);
xlabel('Frequency [f/fs]');
ylabel('Amplitude [dBV]');
axis([0 0.5 -120 0]);
grid;
```