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SPECIFICATIONS

	Given	Achieved
Technology	1 μm CMOS	1 μm CMOS
Operating Temperature	25°C	25°C
V_{DD} /V_{SS}	+/- 2.5 V	+/- 2.5 V
Output load resistance (differential), R_L	20 kΩ	20 kΩ
Output load capacitance(differential), C_L	250 fF	250 fF
Input load capacitance, C_{in}	100 fF	100 fF
Common Mode Output Voltage	-0.5 V ≤ $V_{CM,OUT} \leq 0.5\,V$	-0.498 V
Power dissipation	$\leq 2mW$	$1.9710\,mW$
Gain	$\geq 40\,k\Omega$	$42.466\,k\Omega$
Gain response	Flat, then monotonically decreasing	Flat, then monotonically decreasing
-3dB Bandwidth	$\geq 50\,MHz$	$71.7246\,MHz$
Figure of Merit (FOM)	$\geq 1000\,k\Omega \cdot MHz/mW$	$1545.35\,k\Omega \cdot MHz/mW$
Current mirror channel length	≥ 2 μm	≥ 2 μm
Gate overdrive	≥ 150 mV	≥ 150 mV
Width/length size increments	$\Delta L_{MIN} = \Delta W_{MIN} = 0.2$ μm	$\Delta L_{MIN} = \Delta W_{MIN} = 1$ μm
Maximum current mirror ratio	20	20

Final Design Parameters

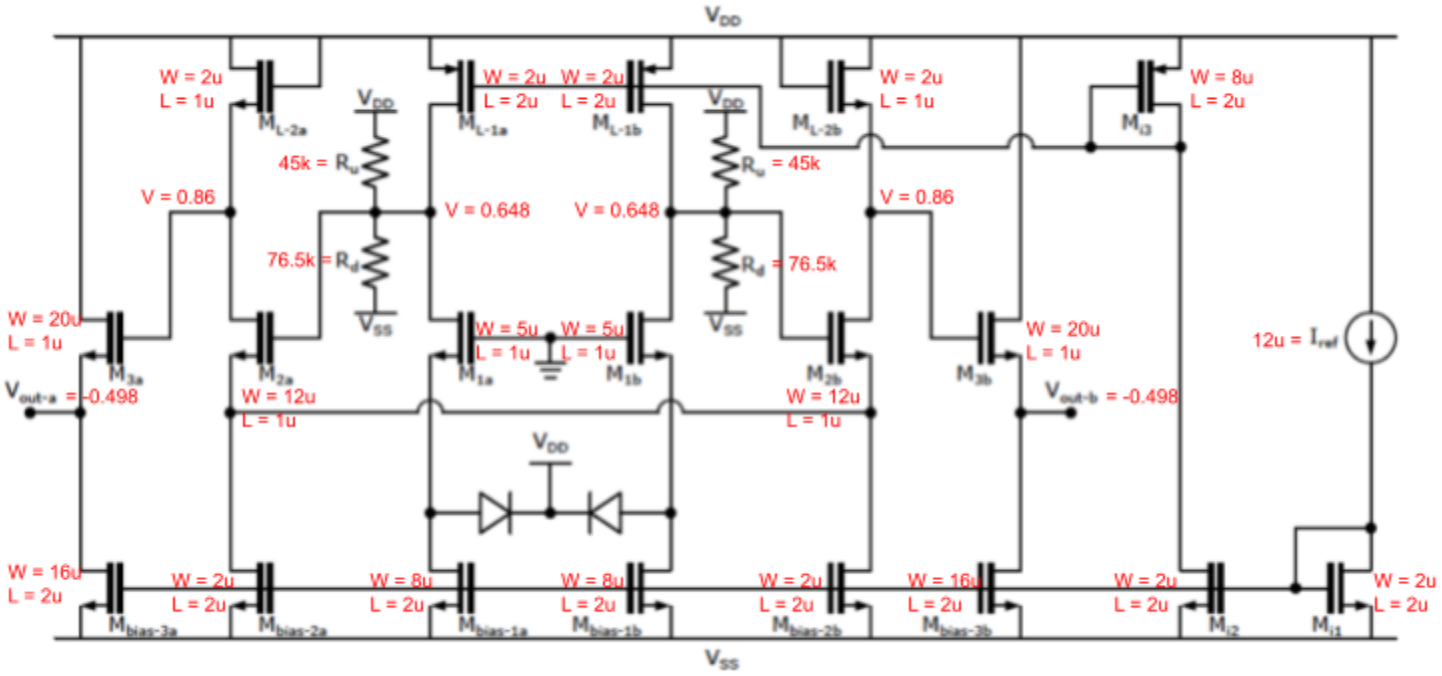

Figure 1: Full Schematic with design parameters labeled

Design Plots

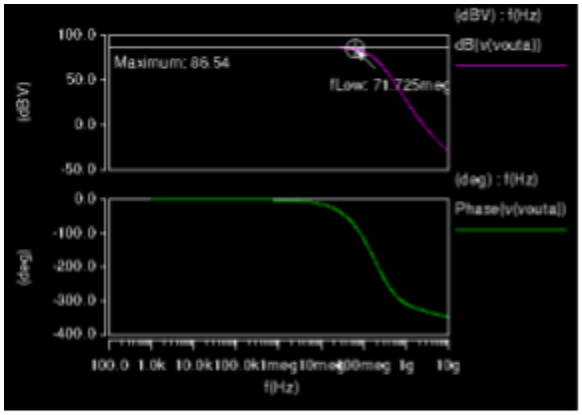

Figure 2 (Output A Magnitude and Phase)

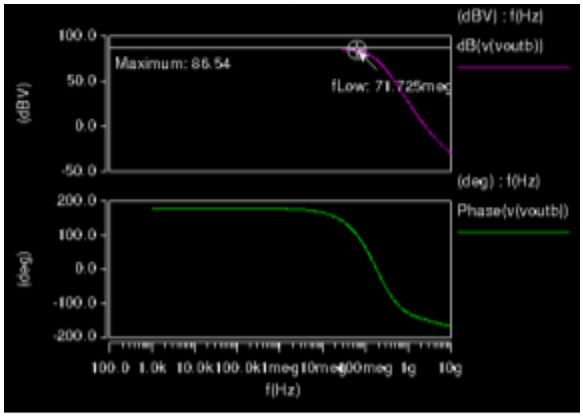

Figure 3 (Output B Magnitude and Phase)

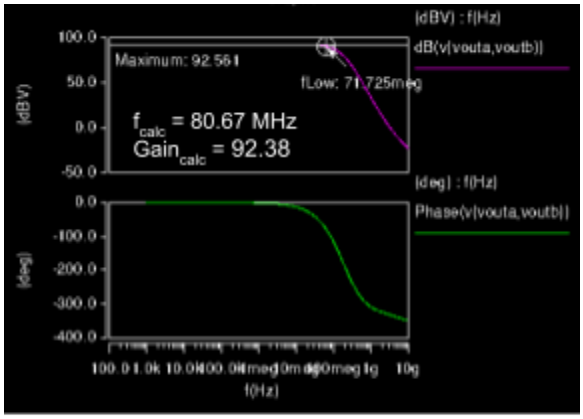

Figure 4 (Differential Output Magnitude and Phase)

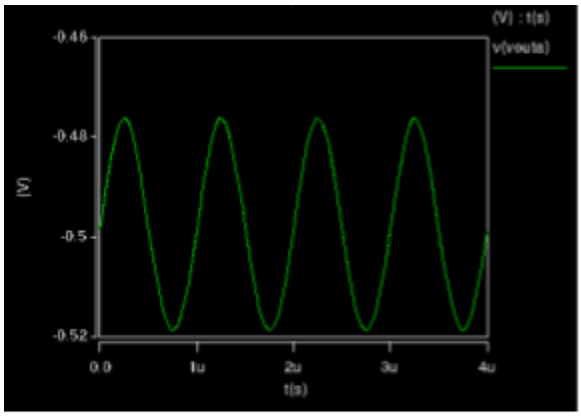

Figure 5 (Output A Transient Response)

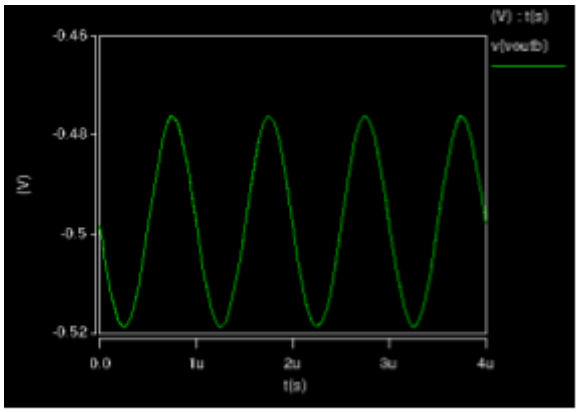

Figure 6 (Output B Transient Response)

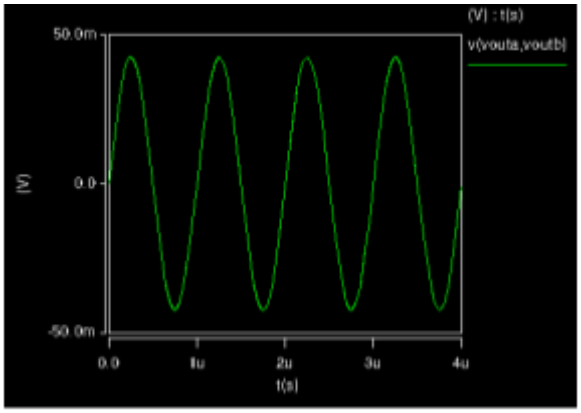

Figure 7 (Differential Output Transient Response)

Design Flow

High Level Approach

Our approach to designing the circuit began by identifying all the components in the schematic and understanding their particular function. For example, we began by identifying each transistor as a PMOS or NMOS. Then, acknowledging that the circuit was symmetrical, we utilized differential circuit analysis moving forward. We identified the different gain stages and understood how each stage would impact the differential gain. After that, we began to include the intrinsic capacitors from each device in order to understand the frequency response of the circuit. In order to simplify the analysis, we utilized dominant pole approximation to approximate the bandwidth of the circuit. From there, we analyzed the power consumption of the circuit. With a complete analysis of all three components (gain, frequency, and power), we were able to see the various design knobs for each component as well as where the tradeoffs would occur. In our design, the main design knobs were the widths of the transistors (we minimized the lengths for all transistors for the best frequency response), the overdrive voltages, and the resistors R_U and R_D. We ignored body effect in our analysis but instead decided to place a conservative gain on the common gate and common drain stage of 0.8 as opposed to 1. This will greatly simplify our analysis of those two stages moving forward.

Choosing Design Parameters

Our first design parameter was determining I_{Ref}. This parameter will set the stage for our total power consumption as the current mirrors will scale this current. From our power constraint of 2 mW, along with our equation for power:

$$P = 5 * (2 * I_{Mb1a} + 2 * I_{Mb2a} + 2 * I_{Mb3a} + 2 * \frac{5}{R_U+R_D} + I_{REF} + I_{Mi2})$$

We were able to determine bounds for our maximum I_{REF}. Assuming $R_U = R_D = 80k\Omega$, when all current mirror branches are at their maximum ratio of 20, I_{REF} cannot exceed 2.72 μA and when all current mirror branches are at their minimum ratio of 1, I_{REF} cannot exceed 48 μA.
We chose I_{REF} = 10 μA as it is a more conservative initial starting point and allows us great flexibility of our current mirror ratios. This value was slightly changed after initial simulation (see **iterations**).

Starting with M_{i1}, we chose Mi1 W/L = 1 as this is the base current that will be mirrored by all other branches. This allows us to scale the other branch currents based on I_{REF}. Also, there is no need to have a W/L larger than 1 as this branch does not contribute to gain or bandwidth.

We similarly chose Mi2 W/L = 1 as this branch does not contribute to gain or bandwidth directly, it only determines the current going through M_{i3}, which effectively biases M_{L1a}. Choosing a W/L of 1 will allow us to conserve power for other stages.

As for M_{i3}, scaling W/L correctly will have a slight impact on power consumption as well as frequency. The C_{gs} of M_{i3} can have a very small effect on the frequency response. While we recognize this does not contribute to the dominant pole, we still want to choose a correct value such that our design is optimized.

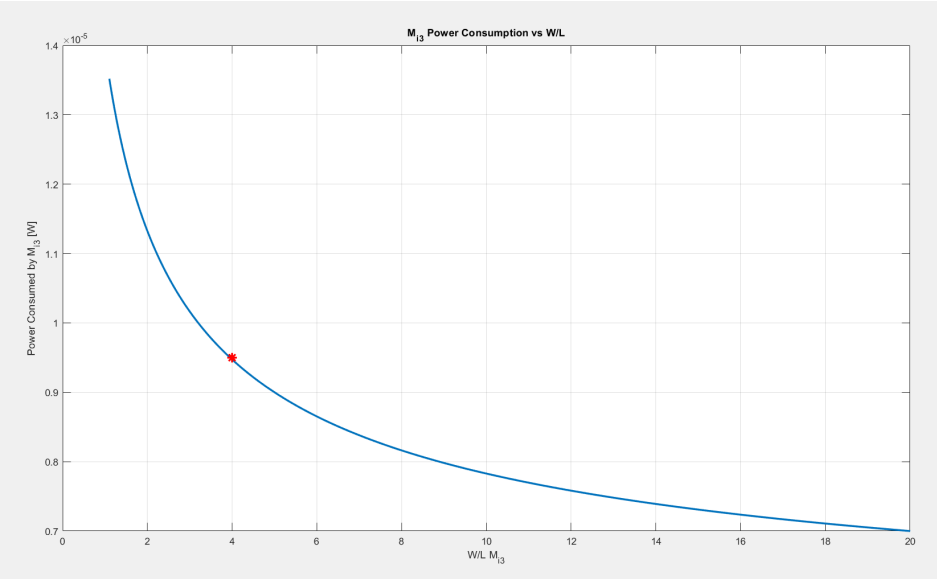

Figure 8: Power consumption of M_{i3} as a function of transistor scaling.

The plot in figure 8 shows the power consumption of M_{i3} as W/L is varied from 1 to 20. Ideally we want to minimize the power consumption, but we also recognize the tradeoff that increasing the width increases C_{gs}. As a result, we chose a value that provides a relatively low power consumption, with a relatively low scaling factor. Anywhere from W/L = 4 to 6 seems to be a reasonable choice, with W/L = 4 being the inflection point before W/L becomes so small that the power consumption increases rapidly. This low power consumption will allow us to use power in other branches where necessary.

From this we can calculate the gate voltage of ML1A, which is the same as the gate voltage of Mi3. To do so, we use the square law model for Mi3:

$$I_{D,Mi3} = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{ov}^{\ 2} \rightarrow V_{ov,Mi3} = \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} = 0.447V$$

We also know that for a PMOS:

$$V_{ov,Mi3} = V_s - V_G - |V_t|$$

So combining the two, we are able to find that

$V_{G,Mi3} = 1.55\,V$ which will be an important nodal voltage for further analysis.

Of the three stages (Common Gate, Common Source, Common Drain), we began analyzing the common drain first because this stage has a constraint that the common mode output voltage must be less than 0.5 V but greater than -0.5 V. We decided this was a good starting point for narrowing our number of open variables or “knobs” while meeting requirements.

CD Stage:

We knew that our CD stage would need to have a gain close to 1 in order for our approximation to be as realistic as possible. We know that:

$$A_{V,CD} = \frac{g_m R_s}{1+g_m R_s}, \text{ where } R_s = r_{o,b3a}$$

We also know g_m is proportional to I_D; therefore, in order to make the approximation $A_v \approx 1$, we want to maximize I_D. As a result, we choose M_{3A} W/L = 20, which would maximize g_m, I_D. As for capacitance, C_{gs} and C_{gd} on M_{3A} are not part of the dominant pole, so we determined it would be better to have g_m as large as possible despite having larger capacitances.

However, for M_{b3A} we noticed that the output pole has a 3dB frequency of 31.83 MHz, which is a bottleneck for the bandwidth. The capacitances are not an issue, they do not contribute in this case. The impedance looking into the output of the common drain is $r_{o,\,mb3a} \,||\, 1/g_{m,\,3a}$. Both values are dependent on I_D and therefore dependent on the W/L of M_{b3a}.

We can plot $f_{3dB} = \left(2 * \pi * C_L * (R_L \,||\, r_{o,mb3a} \,||\, 1/g_{m,3a})\right)^{-1}$, as a function of W/L as seen in Figure 9. This plot shows that W/L > 3 to exceed the dominant pole of 70 MHz. Therefore, we utilized W/L = 4 in order to maintain a bandwidth higher than 70 MHz, while minimizing the power consumption. However, we acknowledged that the power-frequency trade off would be a design knob to come back to in further iterations to increase bandwidth while still maintaining reasonable current through the branch. In our final design, the W/L was increased (see **iterations**).

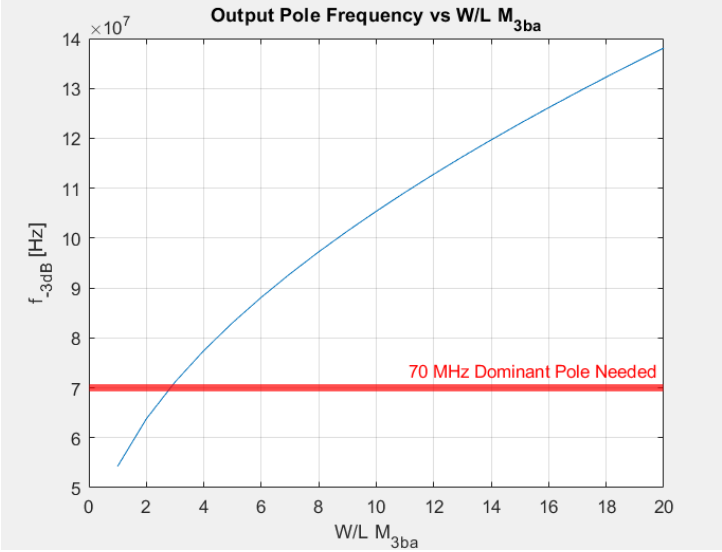

Figure 9: Output Pole frequency as M_{b3a} W/L Varies

CS Stage:

For this stage, we know that the gain is:

$$A_{V,\,CS} = \frac{-g_{m,M2A}}{g_{m,ML2A}} = \frac{-V_{OV,\,ML2A}}{V_{OV,\,M2A}},\ g_m = \frac{2I_D}{V_{OV}}$$

Therefore, to have a larger gain, we want to minimize $g_{m,ML2a}$ and maximize $g_{m,M2a}$.

In order to minimize $g_{m,ML2a}$, we want the smallest W/L ratio possible. Therefore, we will just set W/L= 1 since this transistor is diode-connected so we know it is always in saturation.

Furthermore, since we know the gain is a ratio of transconductance, and both transistors have the same current flowing through them, the gain is not a function of branch current. As a result, we can set M_{b2a} W/L = 1 to minimize the power consumption in this branch.

Lastly, for M_{2a} we want to minimize V_{OV} to achieve the highest gain possible. Figure 10 shows that in order to have a high g_m we must minimize $V_{OV,}$, as expected.

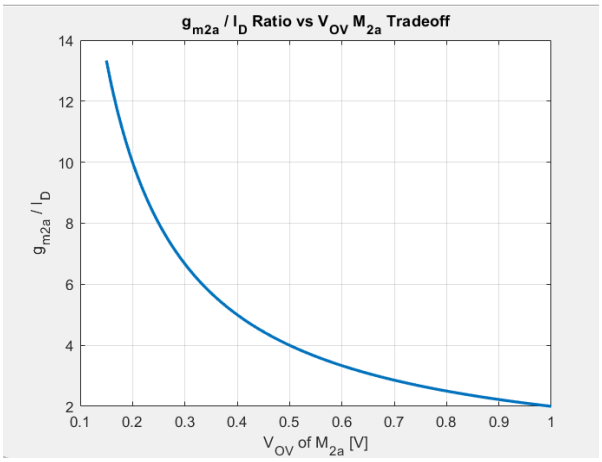

Figure 10: g_m/I_D as a function of V_{OV} for M_{2a}

While minimizing V_{OV} sounds simple, we noticed that the gate voltage of M_{2a} is a resistor divider. This creates an additional 2 degrees of freedom in R_U and R_D. To simplify this one step further, we decided to look at the ratio of R_U to R_D as opposed to straightforward values, as the ratio is ultimately what determines the biasing. Figure 11 shows the gain as a function of the resistor ratio for various W/L of M_{2a}, along with the 40 kΩ constraint. Any combination of resistor ratio and W/L are acceptable so long as the line is above the 40 kΩ red limit line. However, the optimal solution would be having the smallest W/L possible as M_{2a} is part of the dominant pole. Similarly, we want to operate as far to the right as possible to minimize power consumption (larger R values decrease current). From figure 11 we can see that the minimum W/L is 11, but this does not look very good for power. Instead, we chose W/L = 12 as it is fairly far to the right (low power) and still keeps W/L relatively low (lower capacitances, higher 3db frequency). At the 40 kΩ limit, this gives us an $R_U / R_D \approx 0.58$, which makes $V_{G,2a}$=0.648V. This ratio also ensures M_{L1a} is in saturation with the $V_{G,Mi3}$=$V_{G,L1a}$=1.55V from previously while minimizing $V_{OV,\,2a}$, as needed.

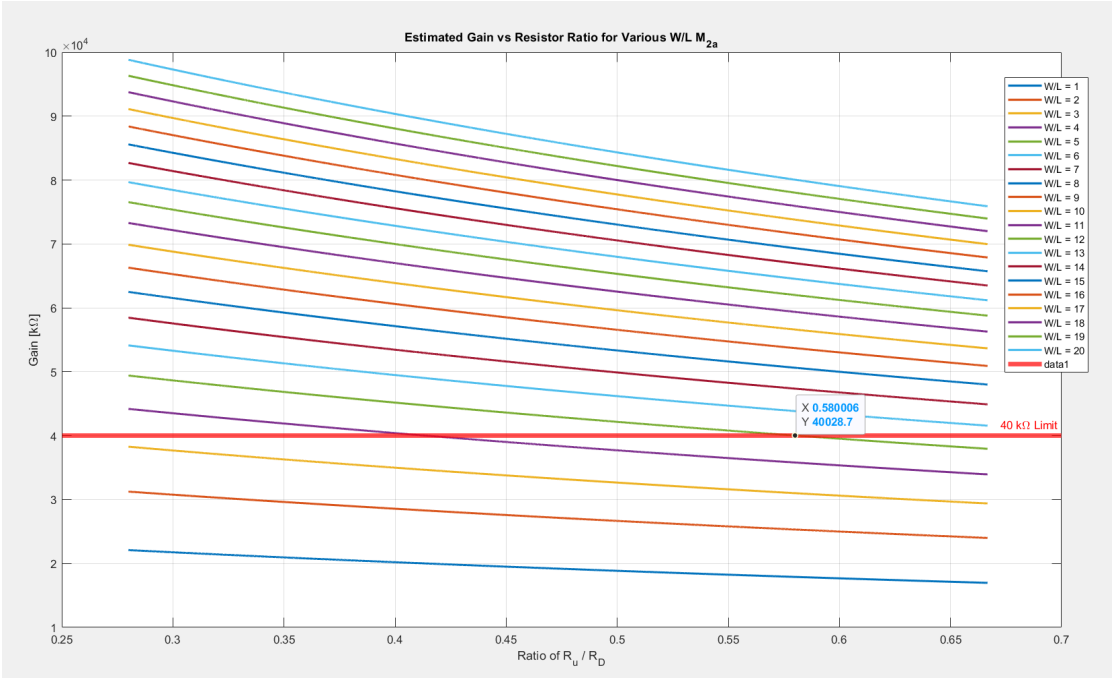

Figure 11: Estimated gain for various W/L ratios of M_{2a} as a function of R_U / R_D ratio.
*Note: R_U / R_D is already constrained such that M_{2a} stays in saturation.
**Note: A_V = (R_U || R_D || r_{oL1A}) * g_{m2a} / g_{mL2a} but here we assumed r_{oL1A} >> R_U, R_D to ignore it.

We initially chose R_U=40kΩ and R_D=68kΩ, but was slightly changed after simulating (see **iterations**).

For M_{L2A}, which is a diode connected NMOS, we can model the transistor as a resistor with resistance $1/g_{ML2A}$. Since we want to minimize g_{ML2A} for maximum gain, we want to maximize the allowable V_{OV}. For a given I_D, this means we want to make W/L as small as possible. This led to the design choice of making W/L=2, which was the smallest ratio able to be simulated.

CG Stage:

To determine the W/L for M_{b1a}, we recalculated our expected power since all other current mirror ratios have been determined, as well as R_U and R_D. We then found the maximum W/L that will allow us to stay within the 2 mW constraint, which happened to be 5. We chose W/L=4 to allow ourselves some flexibility in terms of power if simulation vastly differs from calculations.
As for M_{1a}, we realized that the W/L ratio has little to no effect on the bandwidth or gain of the circuit. This gave us freedom to choose a value so long as we did not begin to influence the 3db point with C_{gd}. We found W/L=5 to be a good value through simulation.

Iterations:

Once we had all our sizings determined, we simulated our circuit. We found that we were able to operate well below the 2mW power requirement (1.35 mW), but the bandwidth was slightly below the 70MHz mark (68MHz) and the gain was lower than our calculation ($35\ k\Omega$). From there, we decided to first attempt increasing the bandwidth, so we returned to the common drain stage, where we increased the W/L of M_{b3A}, such that W/L = 8, given that we could increase power. After another simulation, we found that we were able to meet the bandwidth requirement (exceeding 70 MHz), as well as operate under 2mW. However, our gain was still slightly under what we calculated. We believe this is because our assumption of $r_{oL1A} >> R_U, R_D$ was not entirely valid as r_{oL1A} may slightly lower the parallel resistance. Nonetheless, we had a good understanding of the circuit to understand gain-bandwidth tradeoffs. We increased R_U to 45kΩ , keeping our resistor ratio the same at 0.58 (to ensure equal biasing), which gave us a new R_D of 76.5kΩ. This increase in resistance makes the parallel combination larger, directly increasing the gain and decreasing the power. However, increasing the resistances does lower the 3db frequency. Our 3db frequency was originally 74 MHz, but with the new resistances dropped to 69.3 MHz. However, this gave us a power of 1.7 mW. We decided to increase I_{REF} from 10 μA to 12 μA to increase current in all branches and slightly boost the 3db point. This was successful and allowed us to meet gain, bandwidth, and power constraints.

Hand Calculations vs SPICE Results

	Hand Calculation	**SPICE**	**Error**
f_{3dB}	80.67 MHz	71.7246 MHz	11.09%
Power	2.09 mW	1.971 mW	5.76 %
Gain	$41.589\ k\Omega$	$42.466\ k\Omega$	2.11%

For the most part, all discrepancies are very small. The power was a bit of an overestimate but that is likely due to not including body effect/CLM in the square-law model. The gain was very accurate – our 0.8 assumption for the common gate and common drain stages was a very good approximation, it allowed our results to match very well with simulation. The small difference likely also comes from not accounting

for body effect, where the common gate and common drain stages may not be exactly 0.8. As for the 3db point, we accounted for 5 poles, and made some very feasible approximations because the equation was getting too long. This error is most likely a combination of rounding error having a large impact as well as ZVTC not being fully precise as a model, but our discrepancy is within reasoning.

Comments/Conclusion

Overall, this project was surprisingly fun to work on. We feel as though we do not get very many opportunities to truly design something and take ownership of our design, most classes are just analysis/closed form problems. We feel as though we learned a great deal regarding gain-bandwidth-power tradeoffs as well as seeing the effects in real time. Getting hands on experience helped us learn a tremendous amount. Once we had a good understanding of the circuit, we were able to tune knobs fairly quickly and know why we are changing/sweeping parameters. We ran into minimal issues during the project, it was mostly just working through the math and considering tradeoffs. All in all, we enjoyed the project.