Design and Fabrication of a 25 W DC-DC Wireless Power Transfer Converter Using a Tuned Class Φ_2 Inverter

Steven Abrego*, Malachi Hornbuckle*
*Department of Electrical Engineering, Stanford University, Stanford, CA, 94305

***Abstract*—This paper presents the design, simulation, and fabrication of a Class Φ_2 Inverter capable of delivering 25 W with inductive coupling. The inductive coupling consists of coils driven resonantly at 6.78 MHz with a spacing of 1 inch. The configuration has a maximum power density of 13.85 $\mathbf{mW/cm^3}$ and achieves a maximum drain efficiency of 92.66%.**

I. Introduction

The need for high power density circuits has driven people to investigate high frequency converters because of their ability to drastically reduce passive component sizing. Resonant converters are capable of operating at MHz frequencies with relatively high efficiencies. Specifically, the Class Φ_2 inverter utilizes a passive LC input network for harmonic control as well as a series LC tank at the output and only a single switch to deliver large amounts of power with high efficiency.

For this final project of EE 356A: Resonant Converters, given our design constraints of $V_{in} > 20\ V$ and a device rating of $< 60\ V$, we were essentially left with two circuit configurations that can easily meet these requirements: a Class D inverter or a Class Φ_2 inverter. The Class E inverter was quickly ruled out due to its peak drain voltage $\geq 3.6 * V_{in}$, which requires a device rating greater than $60\ V$ with a $20\ V$ input.

We considered both converters as viable options for this final project, but ultimately decided to implement the Class Φ_2 inverter as we have previously constructed a Class D inverter in lab and wanted to learn and gain experience about a Class Φ_2 inverter. For wireless power transfer (WPT) we decided to deliver power inductively due to the fact that it would be easier to implement and we both had a better understanding of inductive coupling as opposed to capacitive coupling.

Ultimately, we were able to meet all requirements utilizing the Class Φ_2 topoplogy with inductive coupling, operating at 6.78 MHz. In order to do so, we designed the converter, simulated the converter in LTspice, and built the converter, followed by tuning components to achieve our desired output power.

II. Specifications

For our converter, we were supposed to design to output $25\ W$ at $6.78\ MHz$. We must use a resonant DC/DC converter. The input voltage V_i must be greater than $20\ V$, while the maximum v_{ds} across any switching device must not exceed the rating of $60\ V$. Furthermore, our output DC voltage must not exceed $40\ V$ as that is the rating of the rectifying diodes we have been so generously gifted ownership over. As for the wireless power transfer (WPT) coils, the spacing of the coils must be at least 1 inch apart.

TABLE I
Input-output specifications of built Class Φ_2 Converter.

	Minimum	Nominal	Maximum	Units
V_{in}	18	22	23	V
f_{sw}	6.64	6.78	7.1	MHz
D	0.36	0.38	0.4	-
$V_{DS,MAX}$	51.8	57.3	60.5	V
Coil Spacing	1	1	1	in
Power Density	-	8.7	13.85	mW/cm^3
R_{load}	25	36	45	Ω
V_{out}	22	24.08	32.1	V
P_{out}	11.87	25.15	40	W
η_{Drain}	86.53	89.31	92.66	%

Table I shows all input-output specifications achieved by our converter. It is important to note the minimum and maximum values for the table are not absolute; they are just the most extreme values we recorded during testing. The minimum output power and input voltage fall below the requirements, but we decided to include them for completeness. Our nominal operation state of the converter meets all specifications.

III. Simulation Design

To start building a simulation that would accurately represent our converter, we first built and characterized a wireless power transfer transformer. As you can see in Figure 8, we 3D printed a cute little spacer to hold our transformer coils one inch apart, which made it easier to keep the parameters associating with the transformer more consistent as we played with it over the next few days.

Next, we needed to choose a strategy for making the coil and load look like a resistor from the perspective of the resonant converter (since we know how to design a resonant converter to drive a known load). By choosing to design for an output voltage of $30\ V$ (giving us headroom for both input voltage and diode rating requirements), we can constrain $R_o = 36\ \Omega \Rightarrow R_{eq} \approx 29\ \Omega$, the equivalent resistance seen by the secondary coil using $R_{eq} = \frac{8}{\pi^2} * R_o$ for a constant output voltage with a full-bridge rectifier. We considered a few ways to match this:

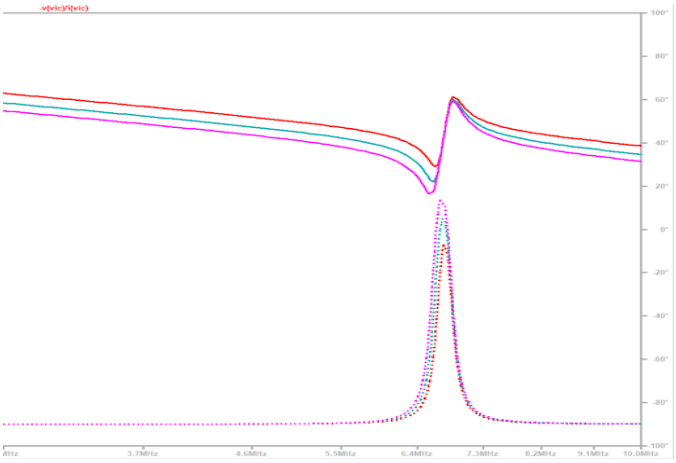

Fig. 1. Impedance plots of the transformer impedance using the cantilever method with varying capacitance. This shows that the cantilever model matching is very sensitive to capacitance values.

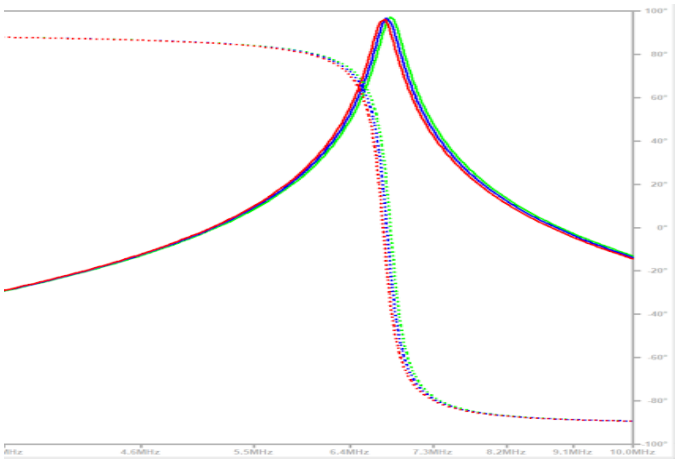

Fig. 2. Coupled inductor model matching with parallel capacitors is less sensitive to capacitance variation, but gives a large load which will be annoying to provide lots of power to.

1) We could use the cantilever transformer characterization with capacitors to resonate out leakage and magnetizing inductances. This was the first approach we considered (we even built a Class D utilizing this method that could output a whopping $0.5\ W$), but it was ultimately pretty futile. As you can see in Figure 1, the match varies pretty substantially as one of the capacitors used varies by $\pm\ 5\ pF$ (the capacitor is extremely small in the first place to cancel out the large leakage inductance), making this design very difficult to tune. Furthermore, the impedance seen by the converter itself is on the order of $1\ k\Omega$, meaning we would need to do further matching to deliver any substantial power (that's a very light load).
2) We could use a coupled inductor model for the transformer, with parallel capacitors by the primary and secondary to make the impedance seen looking from the primary resistive at our switching frequency. This does help reduce the variance of the match as capacitance varies by $\pm\ 5\ pF$ (see Figure 2, but the resulting load is greater than $1\ k\Omega$ (very light load) which would again require an external matching network in order to deliver any substantial power with the input voltage we have access to.
3) We could again use the coupled inductor model, but this time with series capacitors at the primary and secondary to provide a resistive overall impedance at our switching frequency. This is the option that we went with, since it provided a low impedance on the order of $3\ \Omega$ with little sensitivity to capacitor value variation (see Figure 3). Interestingly, the real impedance seen at the input of this network is $\frac{\omega^2 M^2}{R_e}$, where M is the mutual inductance. The inverse relationship with R_e means that as we increase our output load, the load seen by the converter will actually go down, allowing us to theoretically deliver more power. We verified that this was the case when testing our converter.

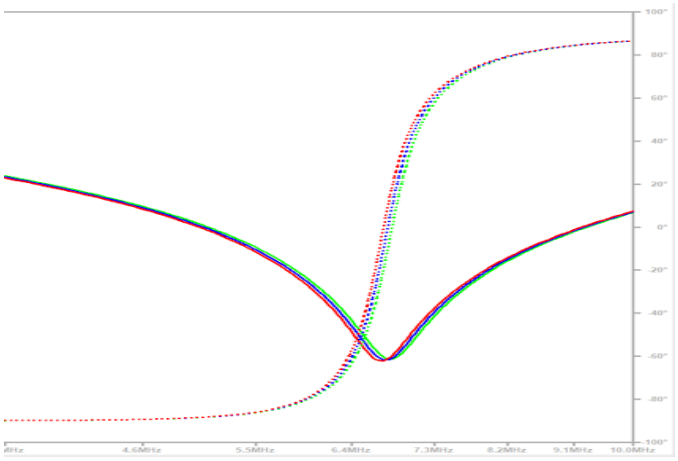

Fig. 3. Coupled inductor model matching with series capacitors is less sensitive to capacitance variation, plus gives a small load we can deliver lots of power to.

With our transformer characterized and matching strategy determined, we could design a Class Φ_2 converter (see Figure 4) to drive the load seen at the input of our transformer/matching network. Using the design methodology discussed in class, we chose C_{extra} to be as small as possible before the inductances in the wave-shaping network became impractically large to wind by hand ($\sim\ 500\ nH$). Then we chose L_S such that we could deliver $25\ W$ with our minimum input voltage of $V_{in}\ =\ 20\ V$ to our matched load. C_S was not necessary in this case because the series capacitor in our matching acts as a DC block already; you could imagine an infinite capacitance in series with that capacitor acting as C_S for the sake of having the constructed circuit match the schematic if you wish. Finally, we tuned the value of C_P until our $v_{ds}(t)$ waveforms looked correct. Increasing C_P makes the impedance seen at the third harmonic more capacitive and smaller, allowing us to use it to tune the shape of the drain waveform. Figure 5 shows our final simulated converter

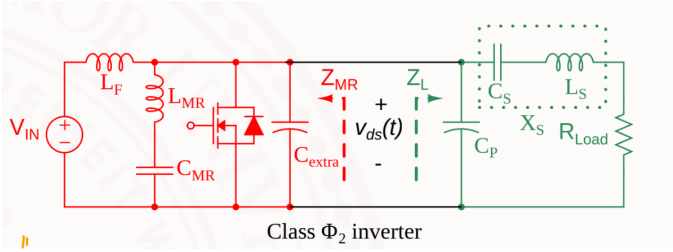

Fig. 4. Schematic of Class Φ_2 Converter from class

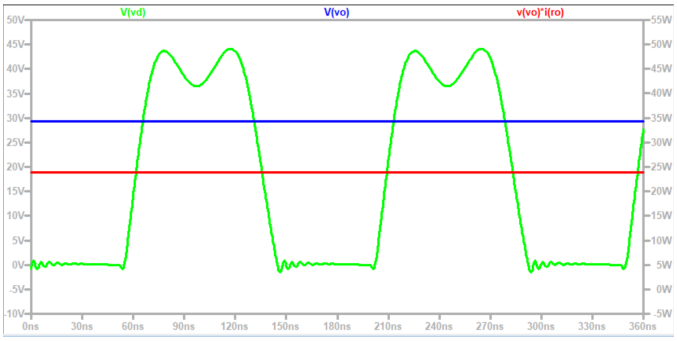

Fig. 5. Simulated waveforms associated with the converter. Green is $v_{ds}(t)$, blue is output voltage, and red is output power. The output voltage and power are slightly below the spec in this figure, but can be easily increased by decreasing L_S.

waveforms, including forward voltage drops in diodes and the manufacturer's MOSFET model.

IV. Board Construction

Once we verified our simulation was working as intended, we moved on to construct our converter. We utilized the Class E converter PCB provided to us from Lab 3; all we needed to add was a series $L_{MR}C_{MR}$ branch for our second harmonic short after the input inductor L_F to complete the input network. We used the same gate driver IC (LM5114) as well as the same MOSFET (BSC065N06LS5) from Lab 3, as we know they are fully capable of operating at 6.78 MHz from the Class E converter we built earlier in the quarter. We assumed C_{OSS} of the MOSFET was 750 pF from the datasheet. We added capacitors for our new values of C_{extra}, C_P, and C_S, taking into account the C_{OSS} as part of our C_P value. Lastly, we wound our inductors (L_F, L_S, L_{MR}) to meet our required inductances. All inductances were small enough to allow for coreless inductors.

For our WPT coils, once we wound the coils we were able to measure the self-inductances of each coil using a NanoVNA. Figure 6 shows a circuit model of the coupled coils represented by their self inductances L_{11} and L_{22}. We then were able to calculate the expected capacitances for C_1 and C_2 such that they resonante at 6.78 MHz with L_{11} and L_{22}, respectively. This allows the output impedance seen by the resonant tank to be only the equivalent load R_{eq}. When we attempted to build the Class D converter mentioned previously, we realized a majority of the power loss was occurring at the coils, likely

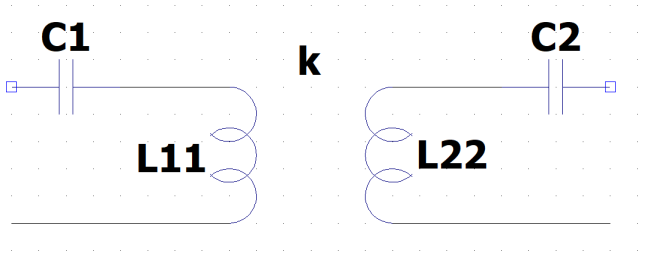

Fig. 6. Modeling of transformer with self-inductances L_{11} and L_{22} with series capacitors C_1 and C_2 to resonate out the inductances. The coils are coupled with coupling coefficient k.

because the impedance of the coils was dominating over the output resistance. Adding the series capacitors on each side of the coils allowed us to effectively reduce the impedance of the coils, and thus deliver more power.

As for the rectifer, we used the full-bridge rectifier from Lab 2. We verified that the diodes are functional at 6.78 MHz with a small sinusoidal test voltage. It is important to note that the maximum voltage rating of the diodes we used (PMEG040V050EPD) is 40 V, so the output voltage must not exceed 40 V – we monitored the output voltage during testing to ensure the diodes do not exceed their maximum rating.

When we initially soldered on the calculated values of C_1 and C_2, the impedance waveforms did not have a resonant peak at exactly 6.78 MHz as we were expecting. This is likely due to addional parasitics such as inter-winding capacitance from the coils. To choose the exact values of C_1 and C_2 to compensate our transformer, we started by attaching our secondary to the rectifier board (to account for the board parasitics) with the diodes removed. We tuned the value of C_2 until we had resonance with the secondary self-inductance L_{22} at the switching frequency with the primary open. Then we attached a dummy load (SMD resistor) close to our expected R_e value at the output of the compensated secondary, and tuned C_1 with the primary (connected to the board to account for parasitics of course) until the whole system looked like a small resistor at the switching frequency.

We wound inductors for L_F, L_{MR}, and L_S as close to our simulated values as we could get without too much pain, then tried different values for C_{MR} until we had a short at the second harmonic (for drain waveform shaping). At this point the drain impedance looked very similar to the simulation (see Figure 7), so we called it quits on the VNA-based tuning. One interesting thing to note is that our measured impedance at the third harmonic (should be dominated by C_P) is smaller than the sim, implying a larger C_P. This is probably because the nonlinear C_{OSS} of the MOSFET is much larger at low bias voltage (0 bias in fact for our VNA measurements), so in large signal it will be closer to the simulation. In fact, we actually added more capacitance to C_P while running our converter to make the waveform shape closer to simulation.

Figure 8 shows the completed assembly, including the Class Φ_2 converter, WPT coils, and output rectifier. Each of the

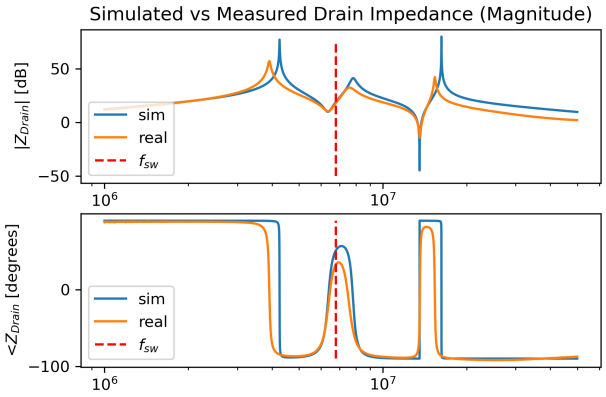

Fig. 7. Our simulated and measured drain impedances match pretty well

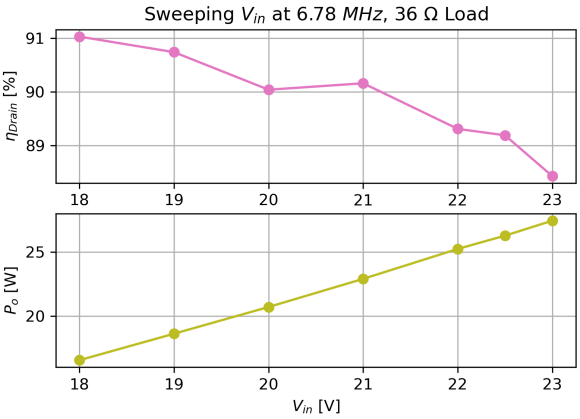

Fig. 9. Input voltage sweep

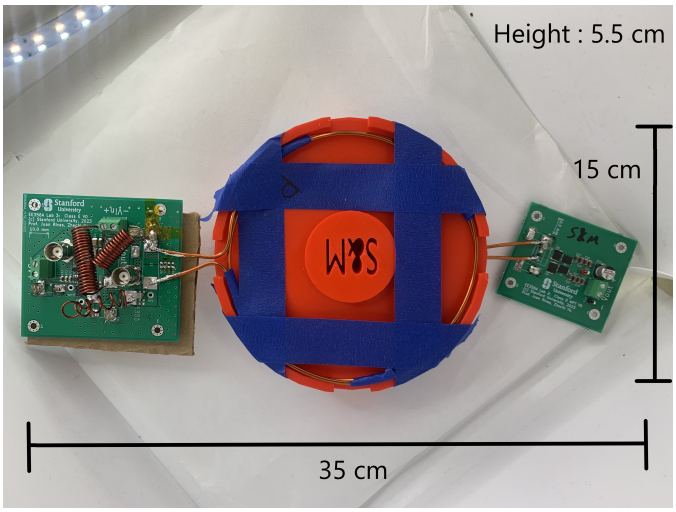

Fig. 8. Assembled Class Φ_2 converter (left) with wireless power transfer coils (middle) and rectifier (right). We 3D printed our own coil spacer to ensure 1 inch separation as well as keep our coil structures rigid.

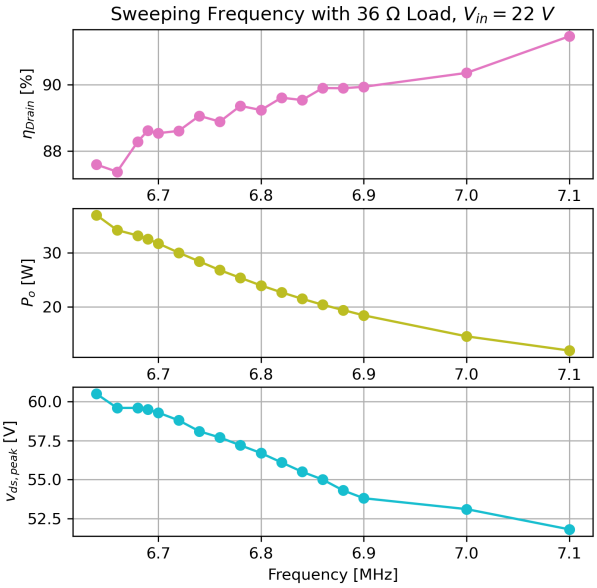

Fig. 10. Sweeping frequency

coils have 2 turns, allowing for a 1:1 turns ratio, each with a diameter of 15 cm (5.9 in). Our coils have a coupling coefficient k of 0.189. With our board constructed, we were ready to begin extracing measurments.

V. Results

During testing, we made two changes to our converter. First we noticed that our v_{ds} waveform had pretty sharp peaks and was also a bit unstable cycle to cycle (we think this was due to subharmonic oscillations). To fix this we added more capacitance to C_P and didn't have either of those problems again. We also noticed that our converter could not deliver 25 W at 6.78 MHz, but could at lower frequencies where the matched coil impedance was more capacitive (cancelling out some of L_S). To fix this we physically stretched out the L_S inductor to reduce its reactance, and also raise the resonant frequency such that we operate closer to resonance, but still above as to maintain zero-voltage switching (ZVS). We anticipated having to play with L_s since it's the main parameter that can be used to control output power. With these two changes we found our nominal operating point in Table I.

After finding our nominal operating point, we explored the behavior of the converter by sweeping parameters such as input voltage (Figure 9), frequency (Figure 10), and load (Figure 11). In most cases, we swept these parameters until we reached the maximum voltage across the MOSFET of 60 V. Figure 9 shows that our output power scales well with our input voltage, allowing us to achieve output powers greater than 25 W above 22 V input. At higher output power our drain efficiency slightly fell, but was above 89% for our nominal operating point. Figure 10 shows that our output

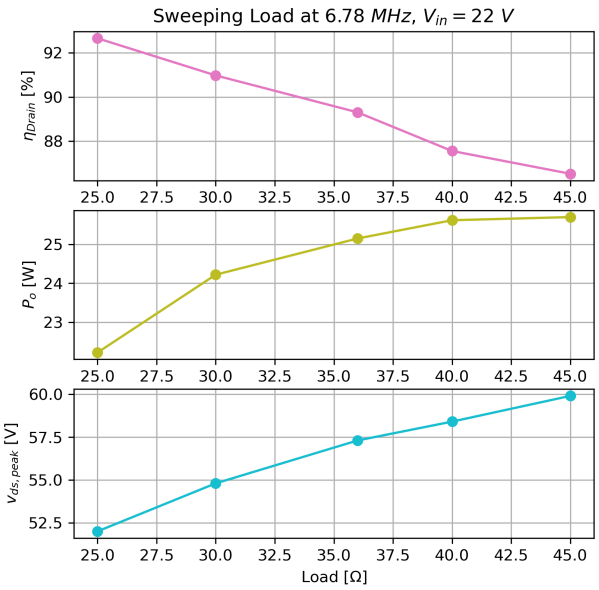

Fig. 11. Sweeping load

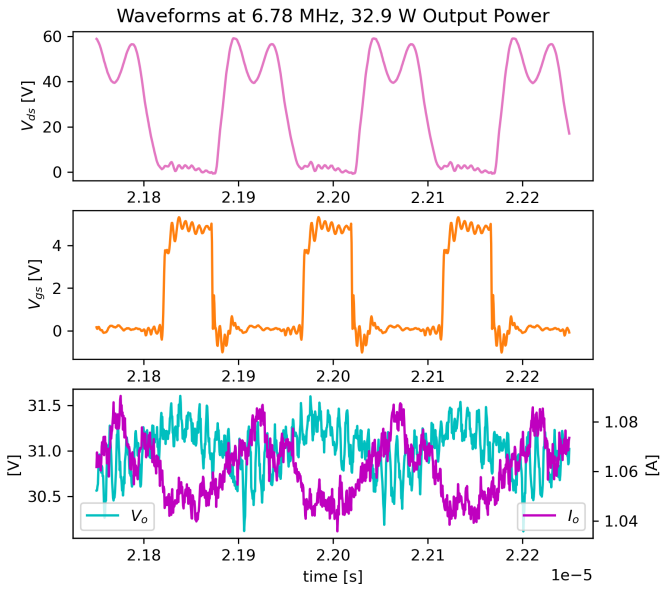

Fig. 12. Example of waveforms we captured during converter operation

power inversely scales with increasing MOSFET switching frequency. This is because at higher frequencies, the reactance of the inductor increases, allowing less power to be seen at the load. Drain efficiency increases with switching frequency, allowing us to achieve at most 89% drain efficiency while meeting the output power specifications. Figure 11 shows our final measurements, as we varied our output resistance from 25 Ω to 45 Ω. Out output power scaled with our load resistance, which is rather unintuitive, but matches our calculations. Drain efficiency decreases at lighter loads, which is likely due to higher circulating currents.

Finally, we pushed the converter to maximize output power to see the extent of our design. At the designed operating frequency of 6.78 MHz, we achieved a maximum output power of 32.9 W (waveforms shown in Figure 12). At a lower frequency (6.66 MHz) we reached just above 40 W on a 30 Ω load, with our MOSFET reaching $87°C$ despite using a fan to cool it off. Even at high output powers, we were still able to achieve ZVS and fairly good zero $\frac{dV}{dt}$ turn off.

VI. Conclusion

Overall, working with a Class Φ_2 converter was a challenge in and of itself, but was very rewarding in the end. We were capable of achieving the required output power of 25 W with a V_{in} of 22 V while keeping our drain-source voltage below 60 V. We both learned quite a bit along the way and had fun in the process. All in all, we are glad to have a functioning converter capable achieving a drain efficiency in the 90% range. This project definitely allowed us to get hands-on learning experience working with resonant converters.

VII. Acknowledgements

We would like to thank Zhechi Ye for all of his help through the design process and for being a great TA this quarter.

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