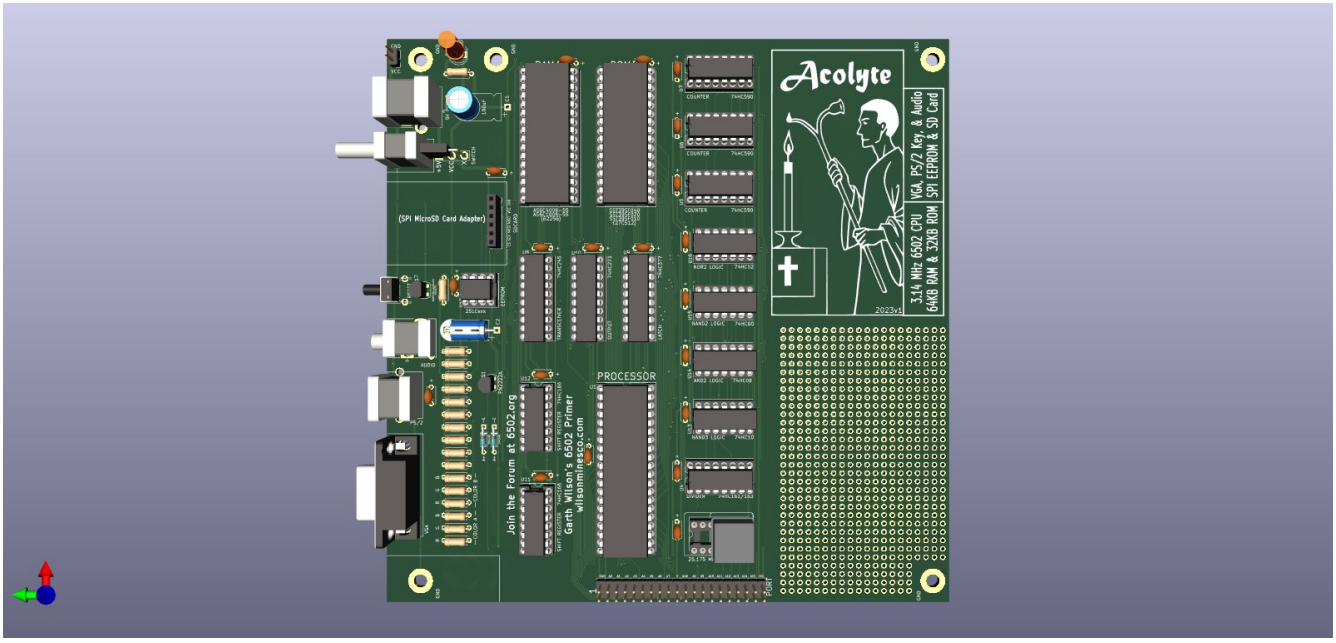
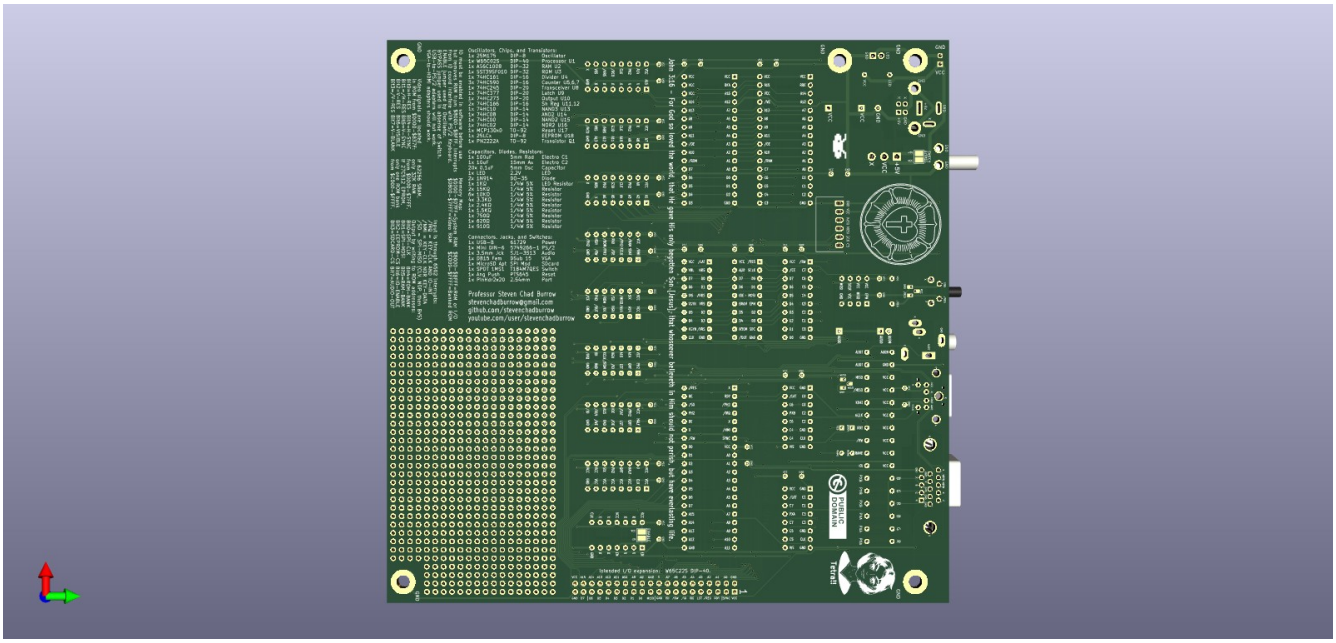
ACOLYTE COMPUTER





The Acolyte Computer is a “Homebrew” computer. It runs a 6502 at 3.14 MHz and has up to 64KB of RAM and 32KB of ROM available. Uses a PS/2 Keyboard, VGA, Audio, SPI EEPROM, and supports an SD Card.

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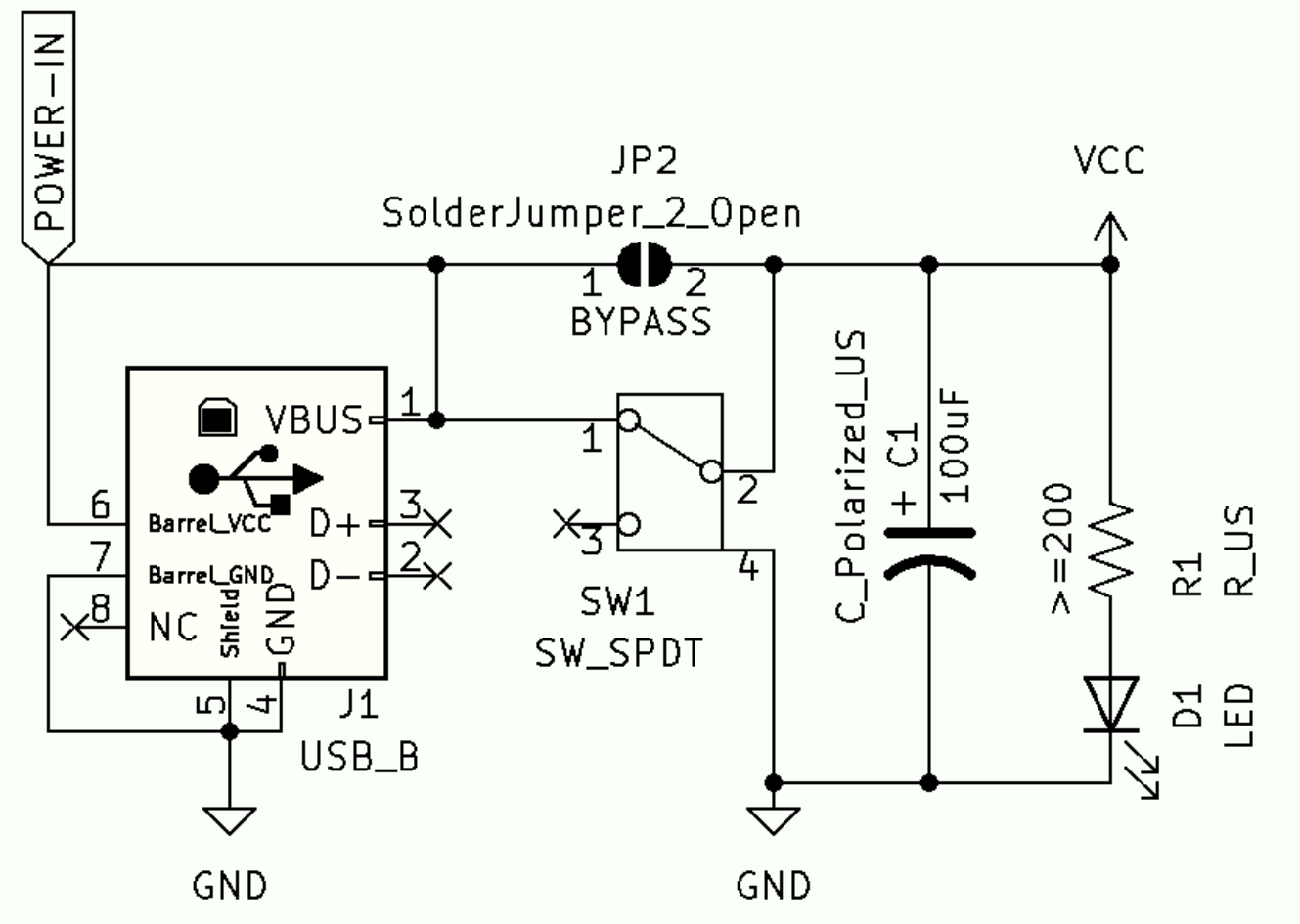
POWER



The Acolyte Computer is powered by a 5V source, typically a USB wall charger. The J1 connector on the board is a USB-B type, often used with printers, scanners, and other peripherials. The footprint on the board allows for use of a generic barrel jack as an alternative.

5V power then goes to the SW1 switch making it convenient to turn the the Acolyte Computer on and off without needing to constantly unplug it's power source. If the switch is not wanted, connect the JP2 "bypass" jumper ends with a blob of solder.

On the board, any label of "+5V" is from the power source, while any label "VCC" is power after the switch.

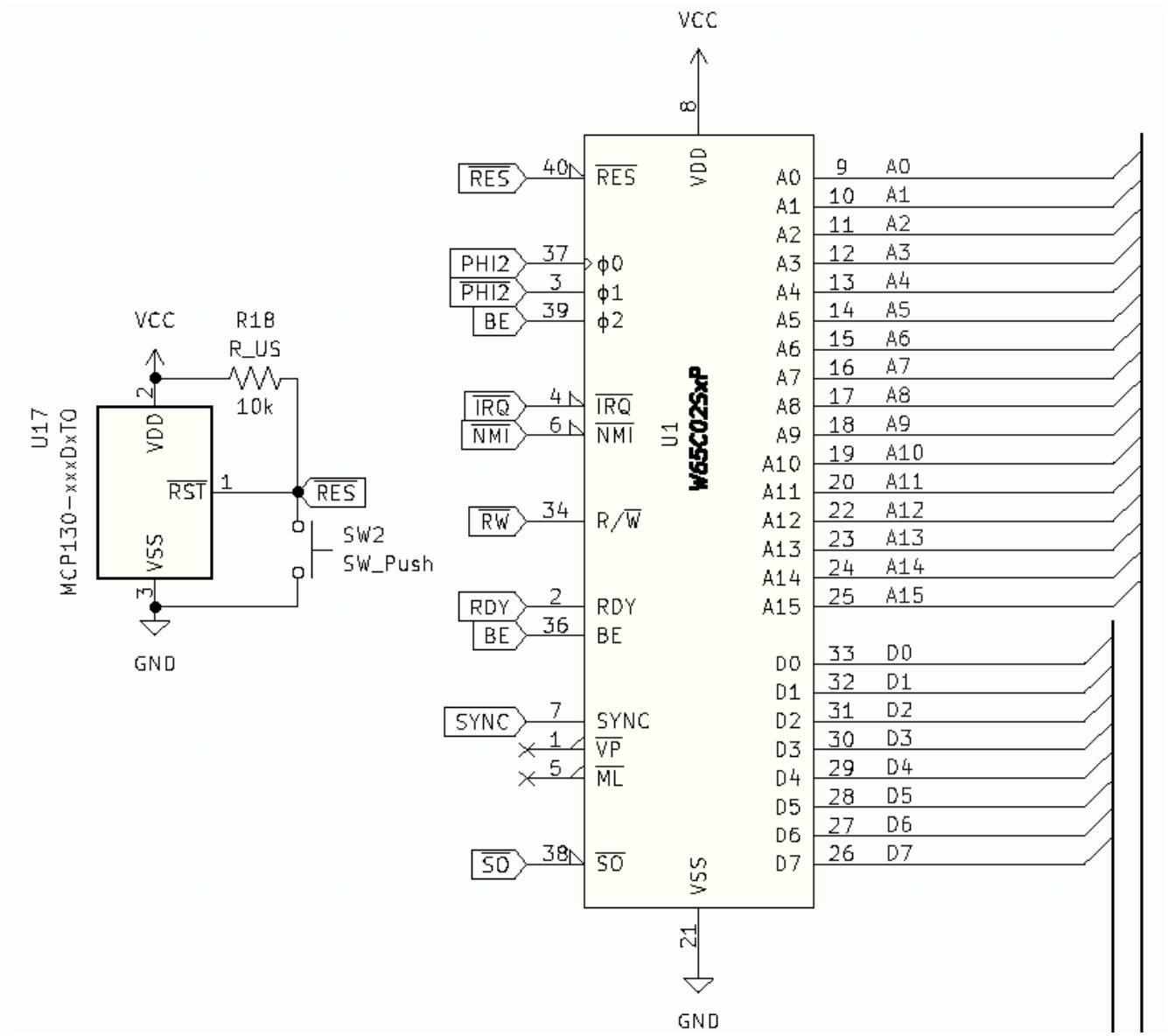
The C1 100uF decoupling capacitor helps regulate power fluctuations on the board. It is polarized, so installing it in the correct direction is absolutely critical. If flipped it could literally catch fire! The footprint on the board allows for either radial or axial versions of this capacitor.

The D1 LED light shines when the board is powered on. If it were directly connected to the 5V power source it would burn up, so the R1 resistor prevents that from happening. The smaller the resistance, the brighter the LED shines. It has a value of >=200 ohms, but typically a 1K ohm resistor works fine.

Components:

J1 - USB	USB-B Connector	
SW1 - SWITCH	SPDT Switch	
C1 - 100uF	100uF Polarized Capacitor	
D1 - LED	LED Light	
R1 - >=200Ω	1K ohm Resistor	

PROCESSOR



The Acolyte Computer uses the U1 W65C02S 8-bit microprocessor, in current production by WDC. This processor was used in the many famous computers in the early 1980's including the Apple II, Commodore 64, and the Nintendo Entertainment System.

Signal Descriptions:

A0 – A15	Address bus, capable of accessing 64KB of memory at a time (output).
D0 – D7	Data bus, capable of 256 numeric values (bi-directional).
/RES	Reset signal, resets the processor (input).
PHI2	Clock (input).

/PHI2	Inverted clock (output).
BE	Bus Enable, takes processor buses offline.
/IRQ	Maskable Interrupt, level triggered (input).
/NMI	Non-maskable Interrupt, edge triggered (input).
/RW	Read-Write (output).
RDY	Ready signal, halts the processor (input).
SYNC	Sync signal, tells when opcode is used (output).
/SO	Set Overflow, allows for fast polling (input).

The job of the processor is to access memory locations from RAM or ROM using A0-A15 . The data sent back and forth is on D0-D7. The processor requires the PHI2 clock signal to operate, which is 3.14 MHz on the Acolyte Computer.

In order to have a video display, the processor's address and data buses are taken offline half of the time. This is done with the BE signal. While PHI2 is low the video signals populate the address and data buses, and while PHI2 is high the processor is allowed to access RAM and ROM for normal operation.

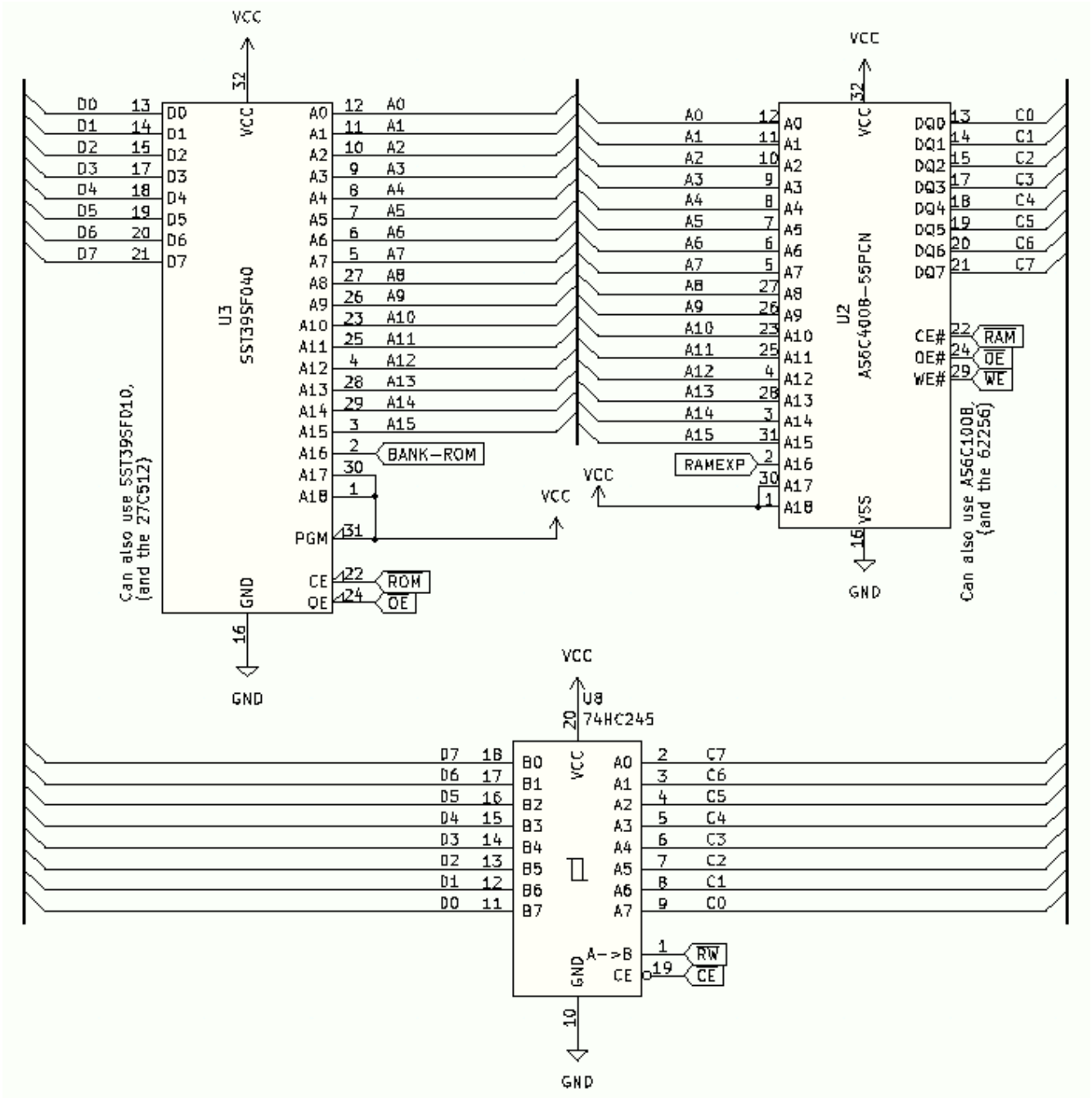
The Acolyte Computer uses many 'unconventional' methods with the 6502 processor. Using the processor's built-in /PHI2 inverter saves some glue logic. The BE signal is generated by the processor's PHI2-OUT to delay the signal. The /IRQ and /NMI signals are almost directly connected to the PS/2 Keyboard, and the /SO line is the inverted SPI-MISO signal. Though not directly used on-board, the SYNC signal can be used to detect $_3 illegal opcodes for extra output bits.

The U17 Supervisory Reset Circuit will reset the processor after power-up. This is critical, and without this tiny IC the processor will glitch every time the power is turned on. The SW2 push button is for reseting the processor without having to turn the power off. The R18 Resistor is not required if the Supervisory Reset Circuit is used but should still be installed.

Components:

U1 – PROCESSOR	W65C02S Microprocessor	
U17 – RESET	MCP130xxD Reset Circuit	
SW2 – RESET	SPST Reset Pushbutton	
R18 - 10KΩ	10K ohm Resistor (optional)	

MEMORY



The Acolyte Computer uses the U2 128KB+ SRAM chip for volatile memory, and the U3 128KB+ FlashROM chip for read-only memory. They share the address bus but the U8 Transceiver chip is capable of disconnecting their data buses.

Signal Descriptions:

A0 – A15	Shared address bus (input).
D0 – D7	ROM data bus, connected directly to processor (bi-directional).

C0 – C7	RAM data bus, connected through transceiver (bi-directional).
/RAM	RAM enable signal (input).
/ROM	ROM enable signal (input).
/OE	Output-Enable (input).
/WE	Write-Enable (input).
/RW	Read-Write (input).
/CE	Chip-Enable (input).
RAMEXP	RAM address expansion signal (input).
BANK-ROM	ROM address bank (input).

For the sake of versatility, many different versions of the RAM and ROM chips can be used interchangably. For example, the RAM could be an AS6C1008 or AS6C4008 without any changes in functionality. Similarly, the ROM could be an SST39SF040 or SST39SF010 without any changes to functionality.

Still further though, the RAM could be any version of the 32KB 62256 chip (given it is sufficiently fast enough), but it would then lose 16KB of available memory. This would disable BASIC on the Acolyte Computer, but all other functions will still work as expected. Similarly, the ROM could be any version of the 64KB 27C512 (given it is sufficiently fast enough), but would lose a bank of memory.

The reason for the Transceiver is to separate video sync and reset signals from color data. All video sync and reset signals are on the ROM at locations $0000-$837F, and all video color data are on the RAM at locations $0800-$7FFF.

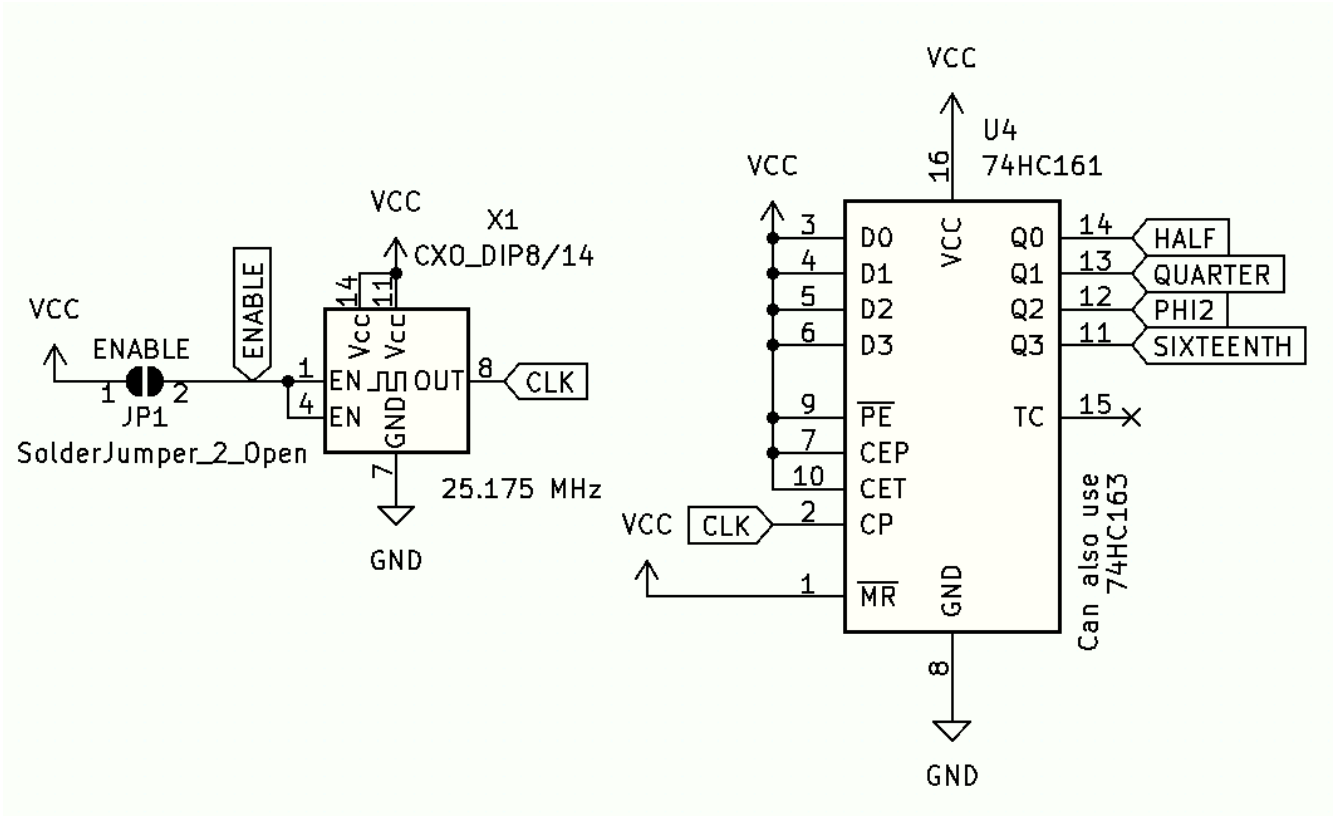
Volatile memory is on the RAM is accessable at locations $0000-$BFFF, with locations $8000-$BFFF being bankable. System read-only memory is on the ROM at locations $C000-$FFFF, but is banked to allow for more code.

All additional signals come from the “glue logic” portion of the Acolyte Computer.

Components:

U2 – RAM	AS6C1008 128KB SRAM	
U3 – ROM	SST39SF010 128KB FlashROM	
U8 – Transceiver	74HC245 Bi-Directional Bus Transceiver	

CLOCK



The Acolyte Computer has a master clock of 25.175 MHz from the X1 Oscillator. This is used for the VGA video display signal. The processor only runs at 3.14 MHz, which is 1/8th of the original clock speed, so the clock is divided down using the U4 Divider.

Signal Descriptions:

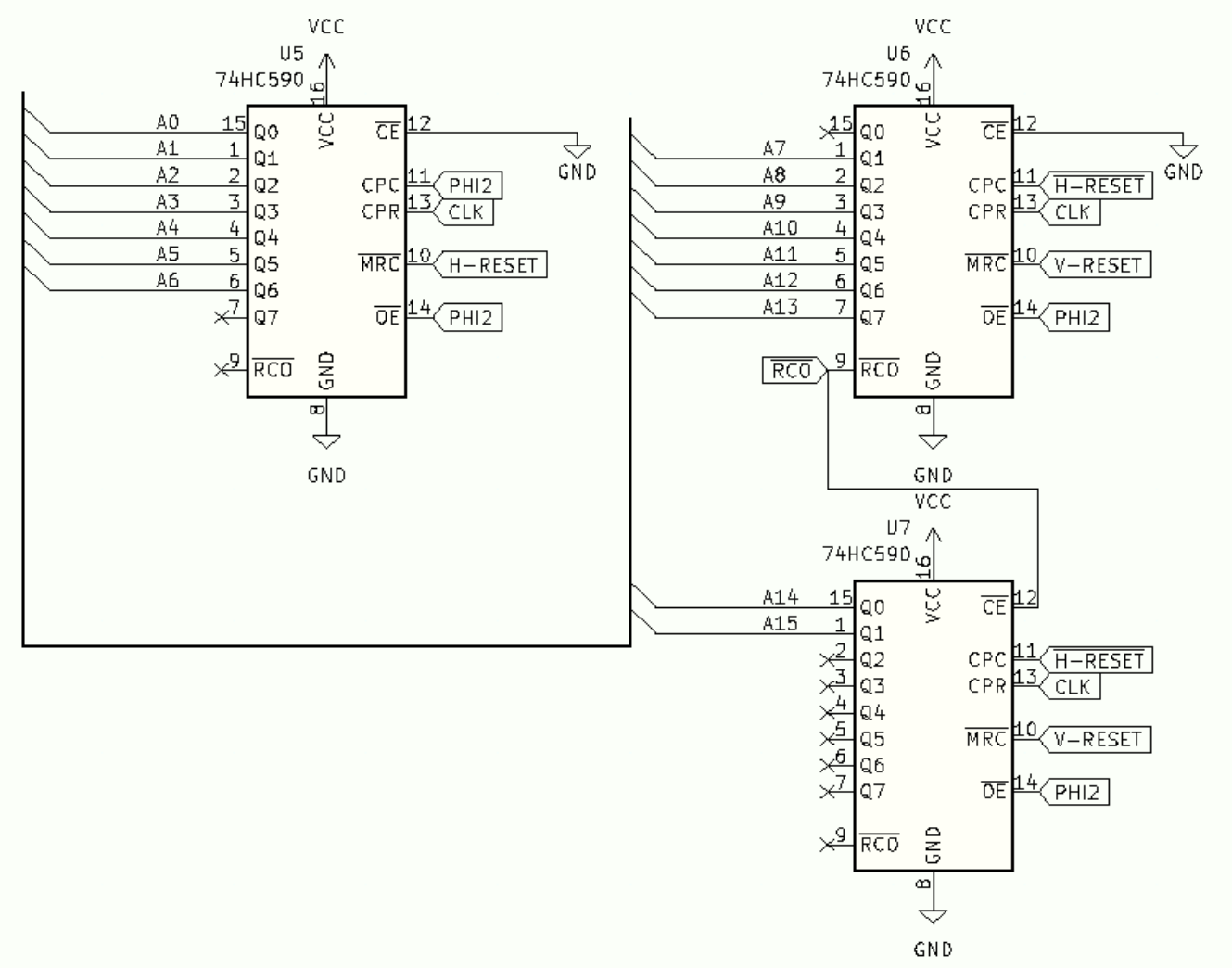
CLK	Master Clock at 25.175 MHz
HALF	Half of Master Clock at 12.59 MHz
QUARTER	Quarter of Master Clock at 6.29 MHz
PHI2	Eighth of Master Clock at 3.14 MHz, used by Processor
SIXTEENTH	Sixteenth of Master Clock at 1.57 MHz

The footprint for the Oscillator allows for either DIP-8 half-can or DIP-14 full-can oscillators. The JP1 “enable” jumper can be used if needed by the oscillator but is typically not required. The Divider could either be a 74HC161 or a 74HC163 4-bit counter chip.

Components:

U4 – DIVIDER	74HC161 or 74HC163 4-Bit Counter	
X1 - OSCILLATOR	25.175 MHz Can Oscillator (DIP-8 or DIP-14)	

COUNTERS



The Acolyte Computer uses the U5, U6, and U7 8-bit Counters for accessing video sync and reset signals and color data for the video display.

Signal Descriptions:

A0 – A15	Address Bus (output).
CLK	Master Clock at 25.175 MHz (input).
PHI2	Eighth of Master Clock at 3.14 MHz (input).
H-RESET and /H-RESET	Horizontal Reset signals from ROM (input).
V-RESET	Vertical Reset signal from ROM (input).
/RCO	Carry signal used with cascading counters.

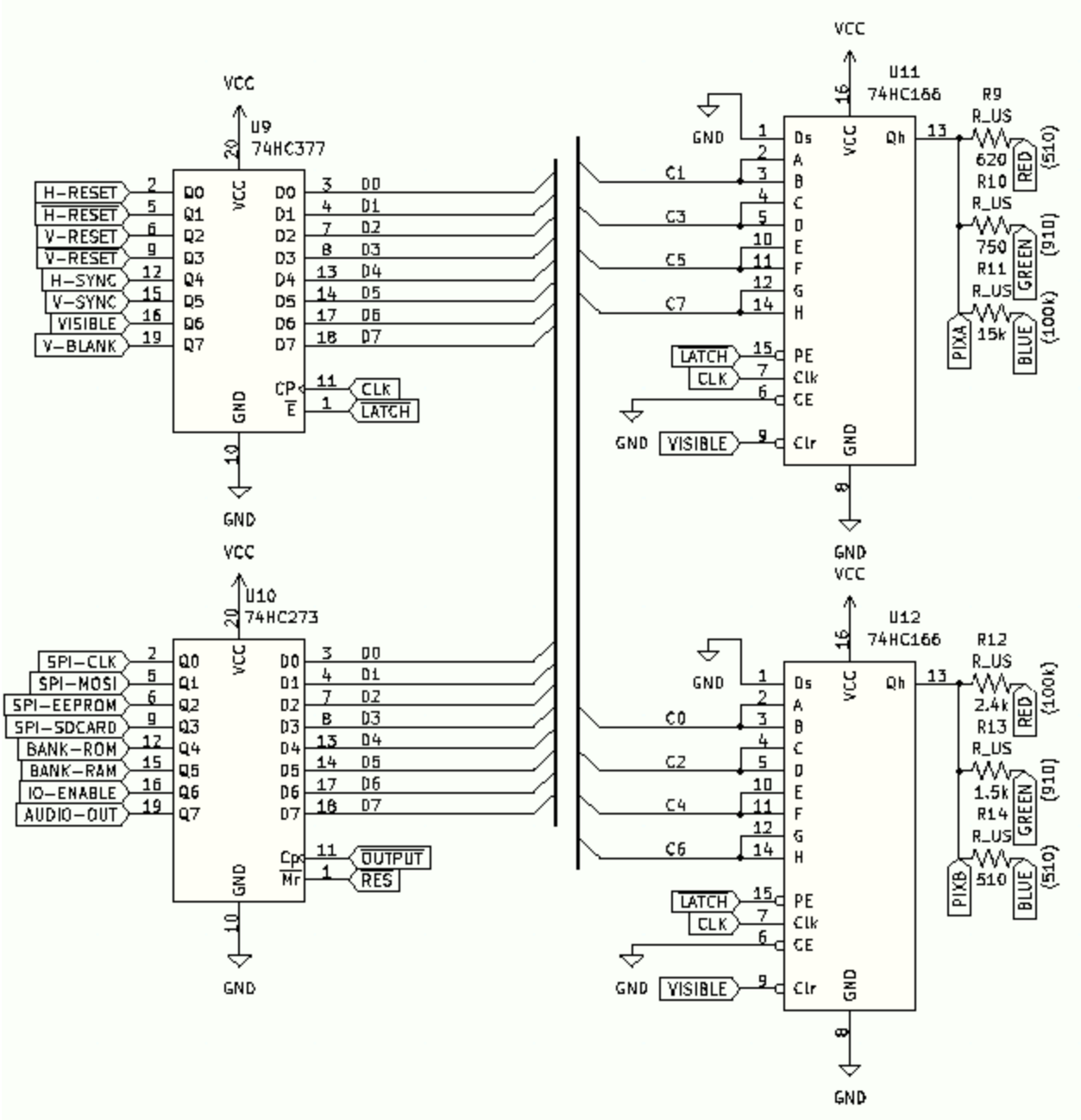
While PHI2 is low, these counters are online and access both the RAM and ROM. While PHI2 is high, these counters are offline, allowing the processor to access the address bus without conflict.

Once every PHI2 cycle the horizontal counter (U5) is incremented. When the location containing the H-RESET signal is accessed, the horizontal counter (U5) is reset, but the vertical counters (U6 and U7) are incremented. Finally when the location containing the V-RESET signal is accessed, the vertical counters (U6 and U7) are reset.

Components:

U4, U5, and U6 – COUNTER	74HC590 8-Bit Counters	

OUTPUT



The Acolyte Computer outputs various signals. The U9 Latch holds all of the video display's sync and reset signals. The U10 Latch holds various output bits for SPI interfacing, banking, and audio. The U11 and U12 Shift Registers hold the video display's color data, which goes through R9 to R14 Resistors.

Signal Descriptions:

D0 – D7	Data bus from ROM (input).
C0 – C7	Data bus from RAM (input).

CLK	Master Clock at 25.175 MHz (input).
/LATCH	Parallel Load Enable signal near end of PHI2 low (input).
/OUTPUT	Edge Triggered Load signal at end of PHI2 high (input).
/RES	Reset signal (input).
PIXA and PIXB	Color pixel data (output).
RED and GREEN and BLUE	Separated color data going to VGA connector (output).
H-RESET and /H-RESET	Horizontal Reset Signal (output).
V-RESET and /V-RESET	Vertical Reset Signal (output).
H-SYNC and V-SYNC	Horizontal and Vertical Sync Signals going to VGA connector (output).
VISIBLE	Visible color signal (output).
V-BLANK	Vertical blank signal (output).
SPI-CLK	SPI Clock signal (output).
SPI-MOSI	SPI Master-Out-Slave-In signal (output).
SPI-EEPROM	SPI Chip Enable for EEPROM (output).
SPI-SDCARD	SPI Chip Enable for SDCARD (output).
BANK-ROM	ROM Bank signal (output).
BANK-RAM	RAM Bank signal (output).
IO-ENABLE	I/O Enable for use with Expansion VIA (output).
AUDIO-OUT	Audio Output signal (output).

The U9 Latch and U11 and U12 Shift Registers all are directly used for the video display. The video sync and reset signals are programmed into the ROM, accessed by the 8-bit Counters (U5, U6, and U7), and then held by the U9 Latch. Video color data comes from the RAM, accessed by the same 8-bit Counters, and then held by the U11 and U12 Shift Registers.

Each pulse of the 25.175 MHz Master Clock shifts the color data into view by the video display. Each color bit is duplicated on load, displaying each color for two pixels, making an effective resolution of 320 pixels across. Likewise the first output of the vertical counter is unconnected, duplicating each scanline, making an effective resolution of 240 pixels down.

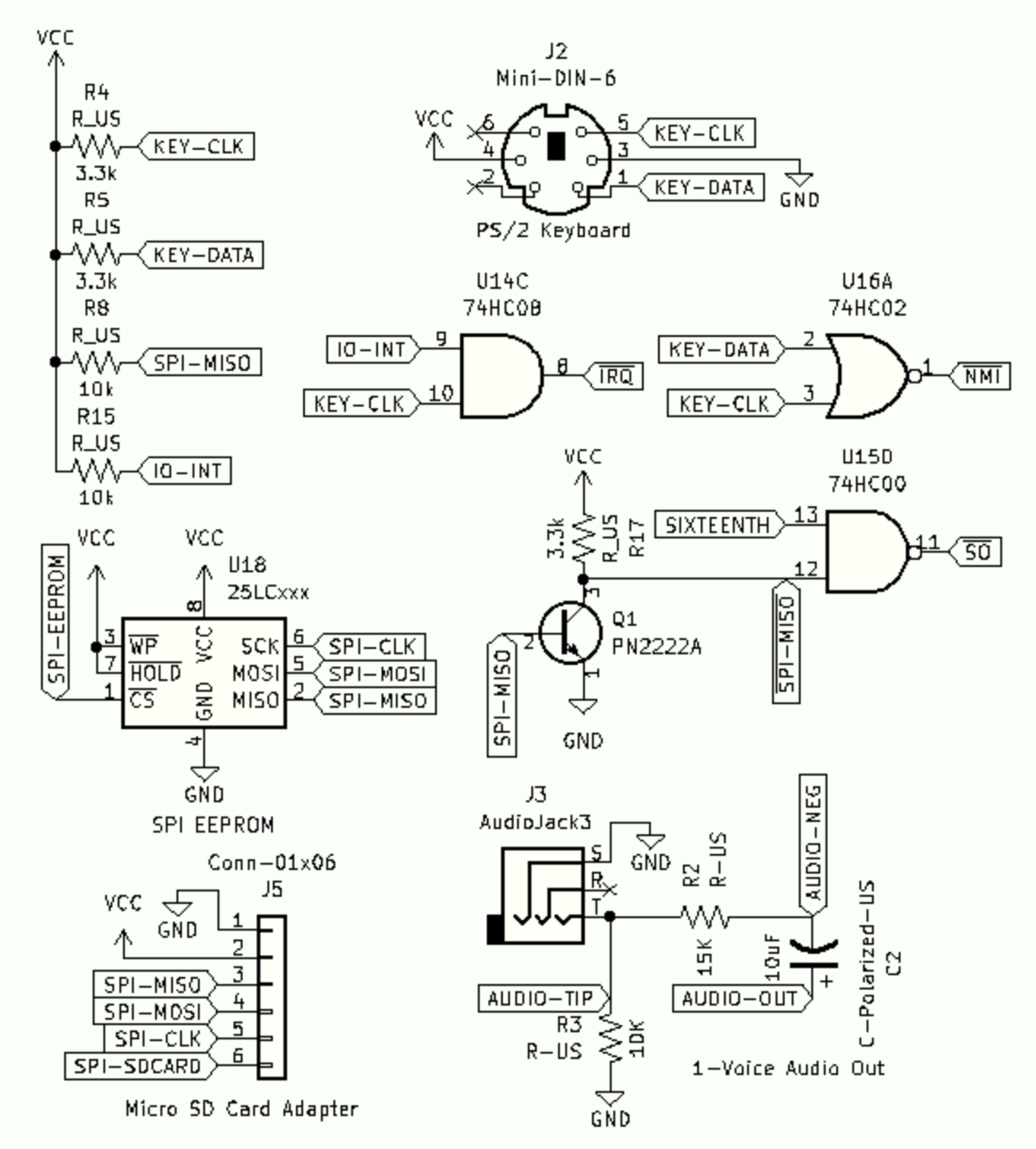
All SPI output bits come from the U10 Latch, while SPI-MISO is inverted into the processor's /SO line. Banking the ROM allows for two separate sections of 16KB. Banking the RAM allows for two separate sections of 16KB, on top of the always visible 32KB (mostly dedicated to video color data).

The IO-ENABLE signal will disable the banked RAM from $8000-$BFFF, thus allowing that space to be used with a 6522 VIA or other I/O devices. Square wave audio is created by fluctuating the AUDIO-OUT signal at certain frequencies between 200 Hz and 2,000 Hz.

Components:

U9 – LATCH	74HC377 8-Bit Latch	
U10 – OUTPUT	74HC273 8-Bit Latch	
U11 – SHIFT REGISTER	74HC166 8-Bit Shift Register	
U12 – SHIFT REGISTER	74HC166 8-Bit Shift Register	
R9 – 620Ω	620 ohm Resistor	
R10 – 750Ω	750 ohm Resistor	
R11 – 15KΩ	15K ohm Resistor	
R12 – 2.4KΩ	2.4K ohm Resistor	
R13 – 1.5KΩ	1.5K ohm Resistor	
R14 – 510Ω	510 ohm Resistor	

PERIPHERALS



The Acolyte Computer maximizes useful peripherals with minimum hardward. The U18 SPI EEPROM can store 8KB of memory even after power-down. The J5 connector leads to a SPI Micro SD Card Adapater, which can hold at least 2GB of data. The J2 PS/2 Keyboard gives access to over 100 buttons. The J3 Audio Jack can send square wave audio to external speakers or headphones.

Signal Descriptions:

KEY-CLK and KEY-DATA	PS/2 Keyboard Clock and Data signals (input).
IO-INT	I/O Interrupt from Expansion VIA (input).
/IRQ	Level-triggered Interrupt (output).

/NMI	Edge-triggered Interrupt (output).
SPI-MISO	SPI Master-In-Slave-Out signal (input).
/SPI-MISO	Inverted SPI-MISO signal.
SIXTEENTH	Sixteenth of Master Clock at 1.57 MHz (input).
/SO	Set-Overflow signal (output).
SPI-xxx	SPI output pins from U10 Latch (input).
AUDIO-OUT	Audio Output signal from U10 Latch (input).
AUDIO-NEG	Audio signal through C2 Capacitor.
AUDIO-TIP	Audio signal at Audio Jack tip (output).

The on-board SPI functionality is dedicated specifically to the EEPROM and SDCARD. Both use similar base functionality, both deal with memory access.

The PS/2 Keyboard is connected to the 6502 interrupt lines through minimal logic. If IO-INT is left unconnected, /IRQ = KEY-CLK. In addition, /NMI = KEY-CLK nor KEY-DATA. This combination of logic allows for extraction of data from keyboards of various speeds though it also delays program execution significantly.

The SPI-MISO line goes through the Q1 Transistor to be inverted and then tied to a sixteenth of the Master Clock. This combination will toggle /SO when SPI-MISO is low thus triggering the overflow flag. Using a simple code sequence of CLV, NOP, BVS would allow polling for the MISO signal.

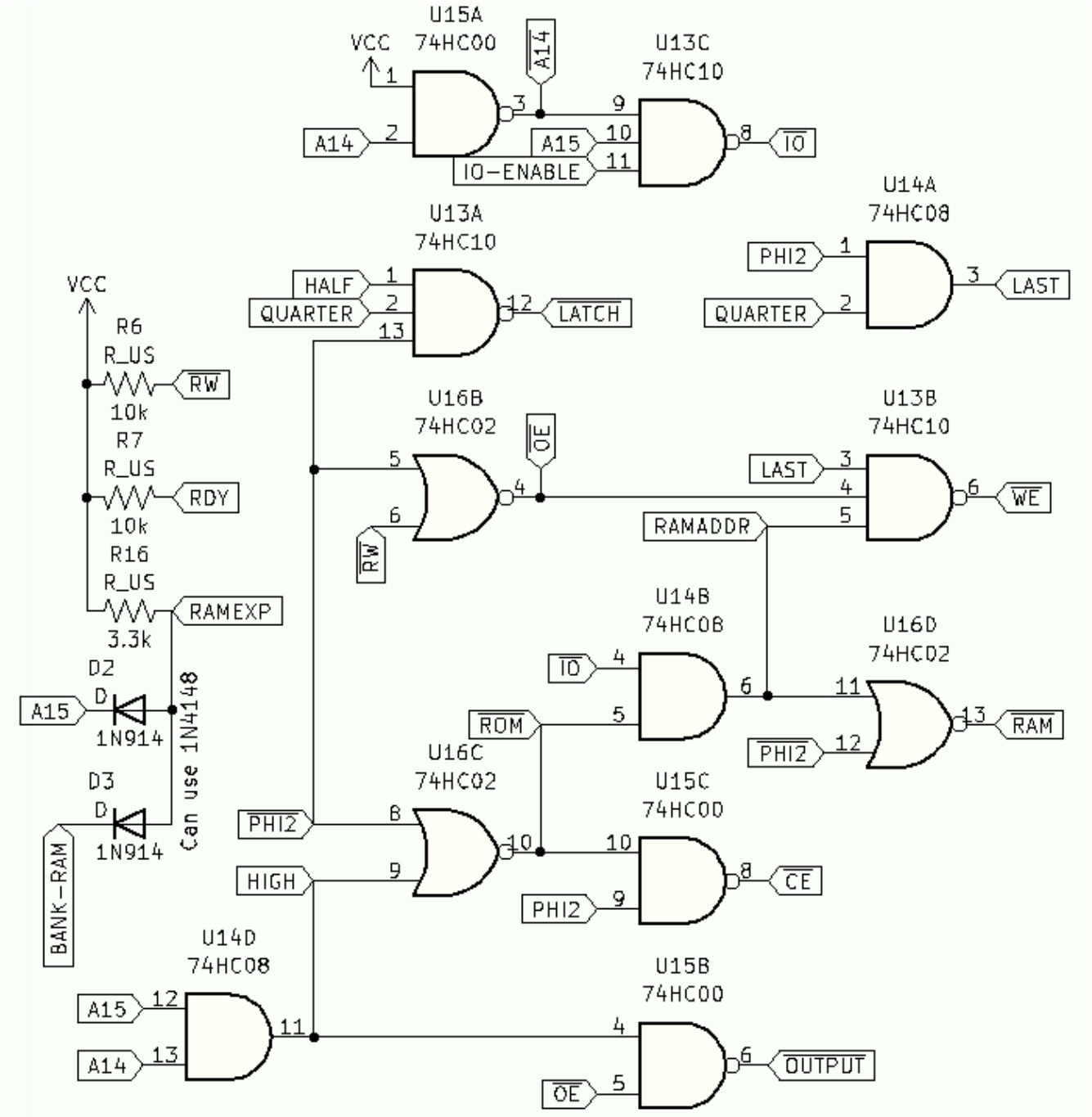
Square wave audio is created by fluctuating the AUDIO-OUT signal. This causes the C2 Capacitor to create positive and negative voltages. The R2 and R2 Resistors set the signal between -1V and +1V as needed for external audio devices.

Components:

J2 – PS/2	PS/2 Keyboard Connector	
J3 – AUDIO	Audio Jack Connector	
J5 – SDCARD	SPI Micro SD Card Adapter	
U18 – EEPROM	SPI EEPROM in DIP-8 package	
C2 – 10uF	10uF Polarized Capacitor	
Q1 – MISO	PN2222A Transistor	
U14, U15, and U15 – LOGIC	(See “Glue Logic”)	
R2 – 15KΩ	15K ohm Resistor	
R3 – 10KΩ	10K ohm Resistor	
R4 and R5 – 3.3KΩ	3.3K ohm Resistors	

R8 – 10KΩ	10K ohm Resistor	
R15 – 10KΩ	10K ohm Resistor	
R17 – 3.3KΩ	3.3K ohm Resistor	

GLUE LOGIC



The Acolyte Computer uses glue logic to tie together various signals so that they happen when needed. The U13 3xNAND, U14 2xAND, U15 2xNAND, and U16 2xNOR chips contain many logic gates to accomplish this goal.

Signal Descriptions:

PHI2 and /PHI2	Eighth of Master Clock at 3.14 MHz.
HALF and QUARTER	Half and Quarter of Master Clock.
A14 and /A14 and A15	Address lines.
IO-ENABLE	Output from U10.
/IO	Low when I/O is accessed.
/LATCH	Latch signal for U9, U11, and U12.
LAST	Clock pulse on last quarter of PHI2 cycle.
/RW	Read-Write from processor.
/OE	Output Enable, inverse of /RW.
/WE	Write Enable, inverse of /OE.
RAMADDR	Not ROM and not I/O.
/ROM and /RAM	Chip Enable for ROM and RAM.
/CE	Chip Enable for U8.
HIGH	Both A14 and A15 high.
/OUTPUT	Latch signal for U10.
RDY	Ready signal to processor.
RAMEXP	RAM bank.
BANK-RAM	Output from U10.

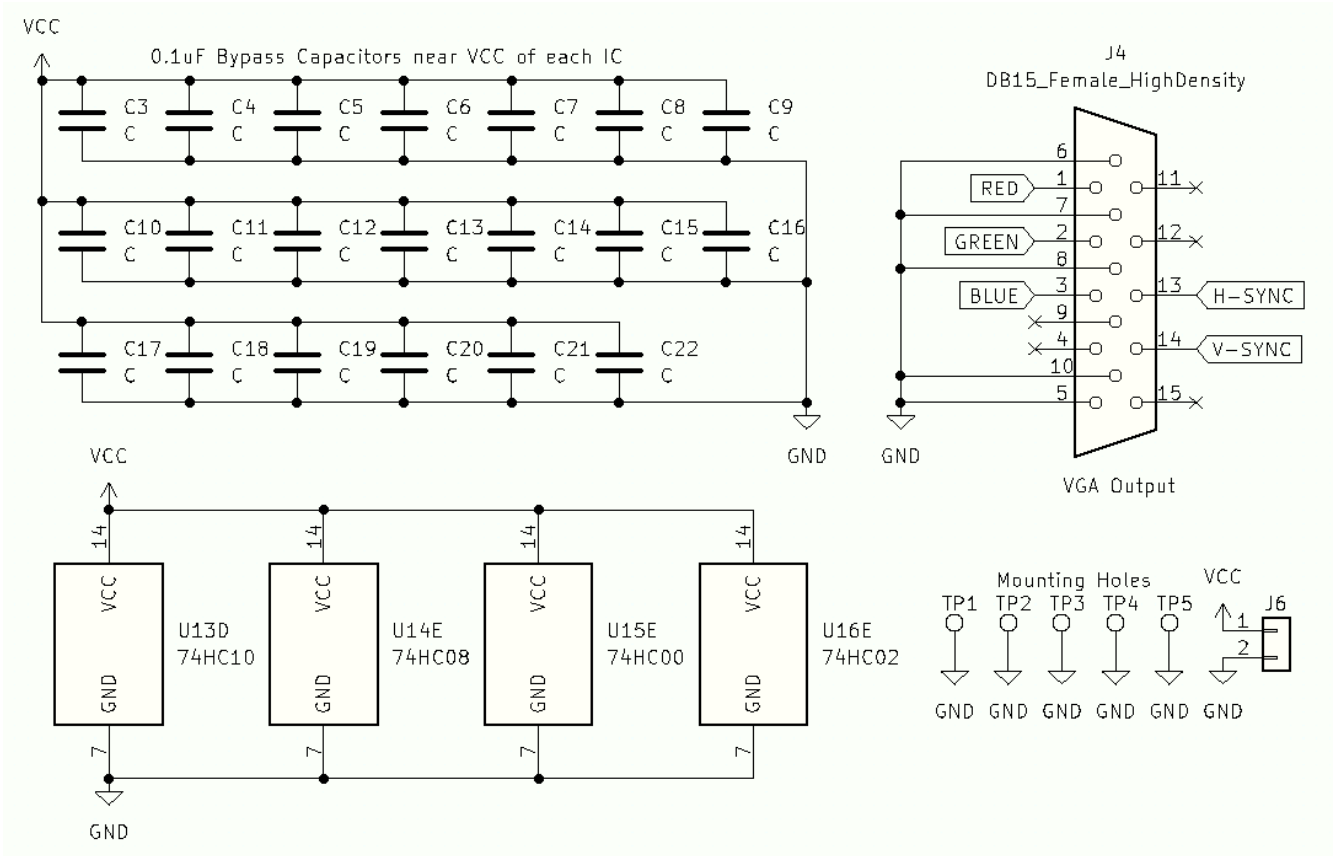
There is a lot going on here. The main thing to understand is that when PHI2 is low, data from RAM and ROM are for the video display. When PHI2 is high, the processor reads and writes to RAM and ROM normally.

The D2 and D3 diodes form “and” logic with A15 and BANK-RAM to create the RAMEXP signal. This both saves a logic gate and is an excuse to use some diodes on the board!

Components:

U13 – 3xNAND LOGIC	74HC10 Tri-NAND Logic	
U14 – 2xAND LOGIC	74HC08 Quad-AND Logic	
U15 – 2xNAND LOGIC	74HC00 Quad-NAND Logic	
U16 – 2xNOR LOGIC	74HC02 Quad-NOR Logic	
R6 and R7 – 10KΩ	10K ohm Resistors	
R16 – 3.3KΩ	3.3K ohm Resistor	
D2 and D3 – 1N914	1N914 or 1N4148 Signal Diodes	

MISC

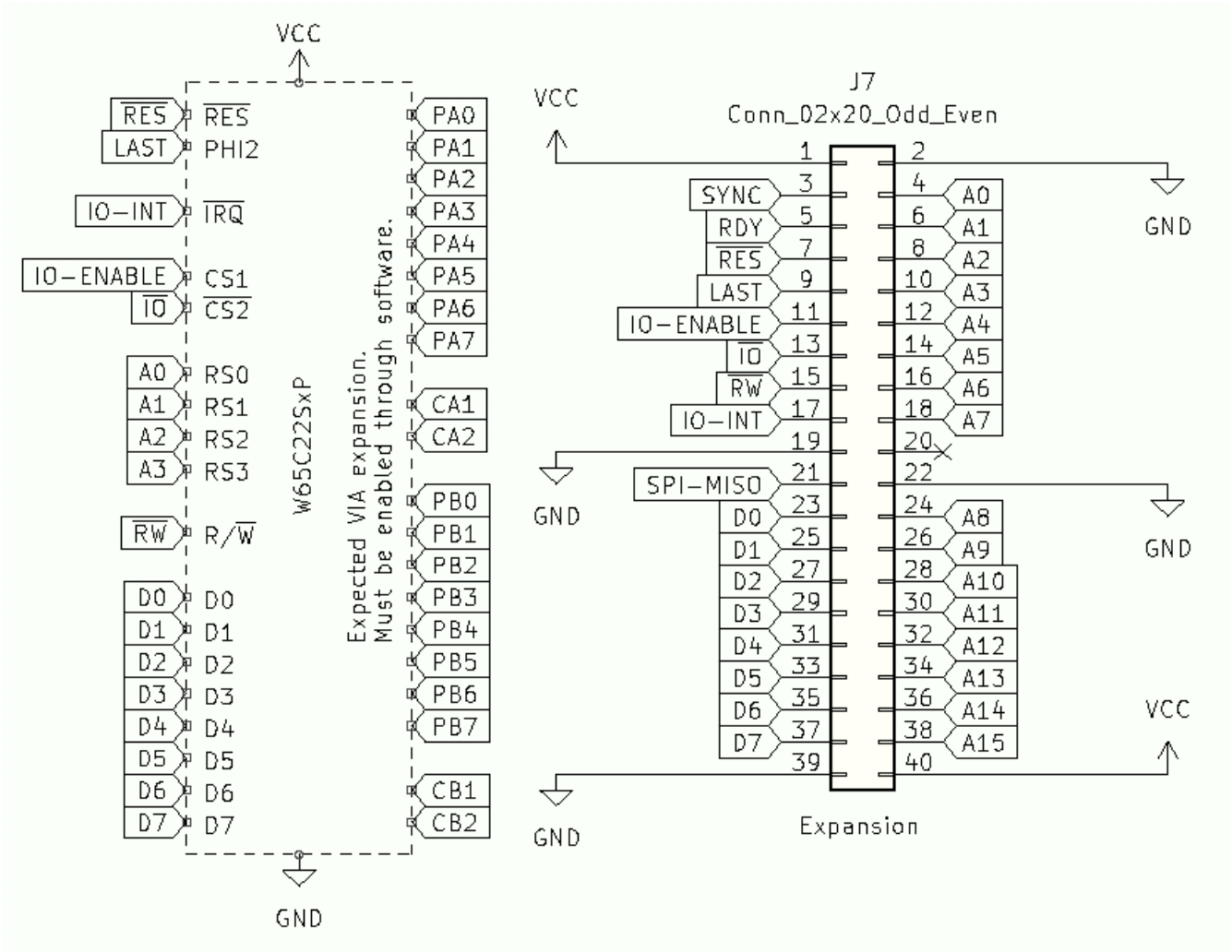


The Acolyte Computer has a lot of components. The J4 VGA connector has the RED, BLUE, GREEN, H-SYNC, and V-SYNC signals as an output to the video disiplay. The J6 pin header is a way to use VCC and GND from the board, or bypass the power circuit entirely. The TP1-TP5 test points are the mounting holes for the board. The U13-U16 chips were discussed in “glue logic”. And finally there are 20 Bypass Capacitors, all at 0.1uF. These need to be placed as close to each chip’s VCC and GND pins as possible.

Components:

J4 – VGA	DSUB15 VGA Connector	
C3 to C22 – 0.1uF	0.1uF Bypass Capacitors	

EXPANSION



The Acolyte Computer has the J7 Expansion Port which has many uses, one of which is to connect to a W65C22S VIA I/O Device. Another possible expansion is to use the SYNC and data bus to determine if a $_3 illegal opcode is being used, allowing for more output bits. SPI-MISO can be used as an additional input, but must be left floating when not in use.

Components:

J7 – PORT	2x20 Pin Header	