2025 Digital IC Design Homework 5

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Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

```
====================== RESULT ======================

All 10 patterns passed!

Cycle: 2096

** Note: $finish    : C:/Users/P76131474/Desktop/DIC_
   Time: 49896700 ps  Iteration: 0  Instance: /testfi
```

```
====================== RESULT ======================

All 10 patterns passed!

Cycle: 2097

** Note: $finish    : C:/Users/P76131474/Desktop/DIC_
   Time: 49904973 ps  Iteration: 0  Instance: /testfi
```

Synthesis Result

Total logic elements	2744
Total memory bits	0
Total registers	474
Embedded multiplier 9-bit elements	4
Clock period (ns)	23.8
Total Cycle used	2097

Flow Status	Successful - Sun Jun 15 22:47:43 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MCH
Top-level Entity Name	MCH
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	2,744 / 55,856 (5 %)
Total registers	474
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	4 / 308 (1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

一開始先把所有 20 筆資料讀進來，然後用 Andrew’s monotone algorithm 去找出所有的點，最後再計算面積。