

2025 Digital IC Design Homework 4

NAME	簡紹軒		
Student ID	P76131474		
ATCONV Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre>----- SUMMARY ----- Congratulations! Layer 0 data have been generated successfully! The result is PASS!! Congratulations! Layer 1 data have been generated successfully! The result is PASS!! terminate at 51204 cycle ----- ** Note: \$finish : C:/Users/P76131474/Desktop/DIC_HW/HW4_Atrous_Convolution_with_I Time: 2560200 ns Iteration: 0 Instance: /testfixture</pre>		<pre>----- SUMMARY ----- Congratulations! Layer 0 data have been generated successfully! The result is PASS!! Congratulations! Layer 1 data have been generated successfully! The result is PASS!! terminate at 51204 cycle ----- ** Note: \$finish : C:/Users/P76131474/Desktop/DIC_HW/HW4_Atrous_Convolution_with_I Time: 2560207952 ps Iteration: 0 Instance: /testfixture</pre>	
System Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre>----- SUMMARY ----- Congratulations! Layer 0 data have been generated successfully! The result is PASS!! Congratulations! Layer 1 data have been generated successfully! The result is PASS!! terminate at 51204 cycle ----- ** Note: \$finish : C:/Users/P76131474/Desktop/DIC_HW/HW4_Atrous_Convolution_with_I Time: 2560200 ns Iteration: 0 Instance: /testfixture</pre>		<pre>----- SUMMARY ----- Congratulations! Layer 0 data have been generated successfully! The result is PASS!! Congratulations! Layer 1 data have been generated successfully! The result is PASS!! terminate at 51204 cycle ----- ** Note: \$finish : C:/Users/P76131474/Desktop/DIC_HW/HW4_Atrous_Convolution_with_I Time: 2560207632 ps Iteration: 0 Instance: /testfixture</pre>	
ATCONV Synthesis Result			
Total logic elements	238		
Total memory bits	0		
Total registers	68		
Embedded multiplier 9-bit elements	2		
Total Cycle used	51204		

Flow Status	Successful - Sun May 18 22:49:12 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	238 / 55,856 (< 1 %)
Total registers	68
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)
System Synthesis Result	
Total logic elements	347
Total memory bits	0
Total registers	68
Embedded multiplier 9-bit elements	2
Total Cycle used	51204
Flow Status	Successful - Sun May 18 23:04:19 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	347 / 55,856 (< 1 %)
Total registers	68
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)
Description of your design	

做 convolution 運算時，每個 clock 把相對應的值拿出來乘上 kernel，最後把結果存進 SRAM，再往下一個 pixel 繼續做。

做 max pooling 運算時，每個 clock 把各個值拿出來依序比大小，最後把結果存進 SRAM，再往下一個 pixel 繼續做。