2025 Digital IC Design Homework 4

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| NAME |  | | | | |
| Student ID |  | | | | |
| **ATCONV Simulation Result** | | | | | |
| Functional simulation | | Pass/Fail | | Pre-Layout simulation | Pass/Fail |
| (your functional sim result) | | | | (your pre-sim result) | |
| **System Simulation Result** | | | | | |
| Functional simulation | | Pass/Fail | | Pre-Layout simulation | Pass/Fail |
| (your functional sim result) | | | | (your pre-sim result) | |
| **ATCONV Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Total registers | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| Total Cycle used | | |  | | |
| (your flow summary of ATCONV) | | | | | |
| **System Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Total registers | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| Total Cycle used | | |  | | |
| (your flow summary of System) | | | | | |
| **Description of your design** | | | | | |
|  | | | | | |