2025 Digital IC Design Homework 5

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| NAME |  | | | | |
| Student ID |  | | | | |
| **Simulation Result** | | | | | |
| Functional simulation | | Pass/Fail | | Pre-Layout simulation | Pass/Fail |
| (your functional sim result) | | | | (your pre-sim result) | |
| **Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Total registers | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| Clock period (ns) | | |  | | |
| Total Cycle used | | |  | | |
| (your flow summary of MCH) | | | | | |
| **Description of your design** | | | | | |
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