

$$D_{out}[0] = \overline{D_{in}[2]}' \overline{D_{in}[1]}' \overline{D_{in}[0]}' (000)$$

$$D_{out}[1] = \overline{D_{in}[2]}' \overline{D_{in}[1]}' D_{in}[0] (001)$$

$$D_{out}[2] = \overline{D_{in}[2]}' \overline{D_{in}[1]} D_{in}[0]' (010)$$

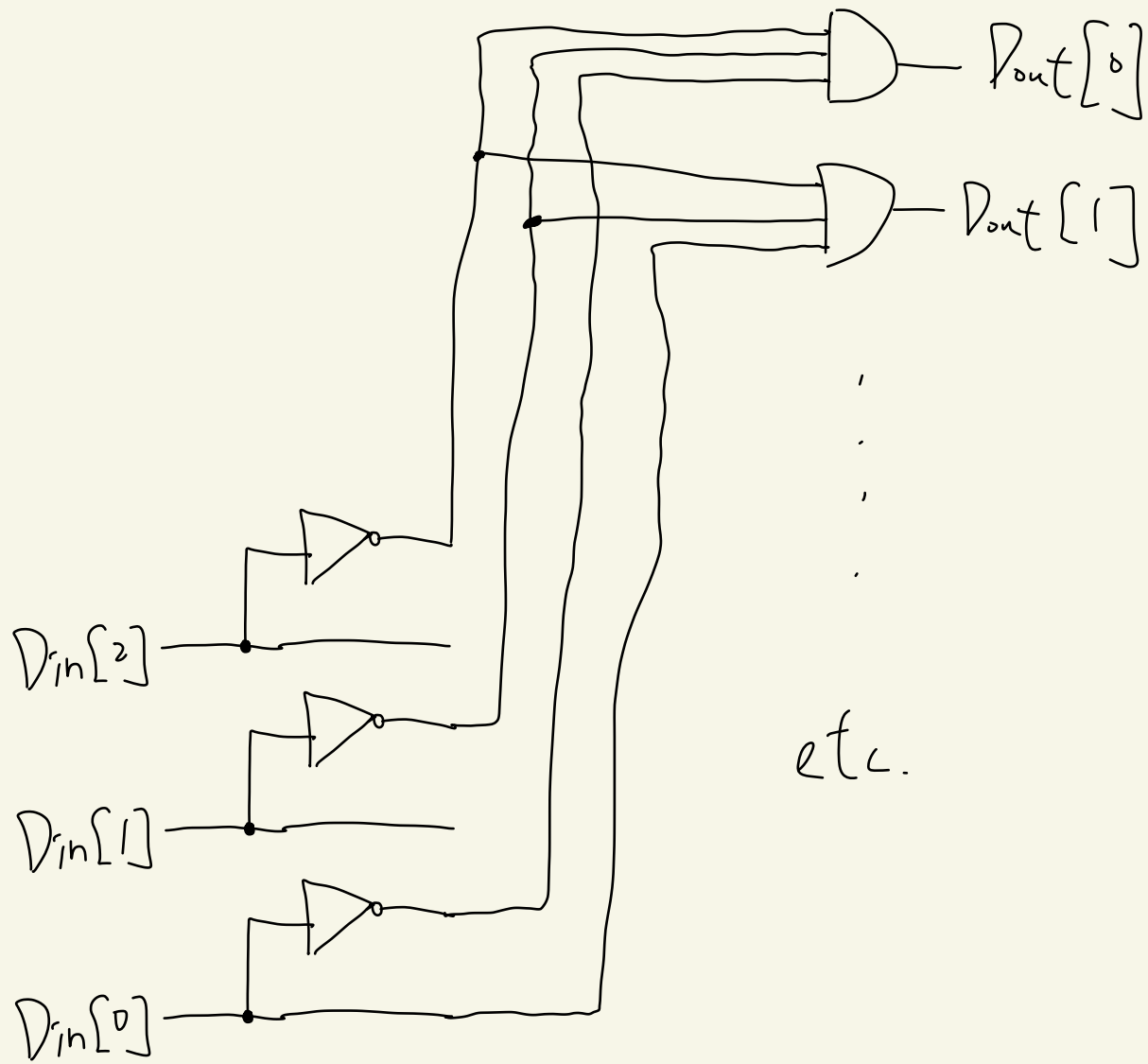
$$D_{out}[3] = \overline{D_{in}[2]}' \overline{D_{in}[1]} D_{in}[0] (011)$$

$$D_{out}[4] = \overline{D_{in}[2]} D_{in}[1]' \overline{D_{in}[0]}' (100)$$

$$D_{out}[5] = \overline{D_{in}[2]} D_{in}[1]' D_{in}[0] (101)$$

$$D_{out}[6] = \overline{D_{in}[2]} D_{in}[1] \overline{D_{in}[0]}' (110)$$

$$D_{out}[7] = \overline{D_{in}[2]} D_{in}[1] D_{in}[0] (111)$$



the design above is dataflow/gate level  
also can use behavior level, ex: case

