

Steven
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Homework 5

① The four possible output values for a 1 bit binary variable is I, 0, X, Z

2. The statements that are true are:

- ~~B) In Verilog, one module can instantiate other modules, and can have multiple instances of another module.~~
- C) always @ can be used in describing combinational circuits
- E) always @ can be used preceding a case statement

3. module mux_4to1 (input wire[3:0] I,
input wire[1:0] S,
input wire E;
output wire Y);

wire w1, w2;

mux_2to1 m1(w1, I[0], I[1], S[0]),
m2(w2, I[2], I[3], S[1]),
m3(F, w1, w2, S[1]);

end module,

4. module mux4_1_bh(I, select, y);

```
input I;  
input select;  
output y;  
reg v;  
always @ (select or I)  
case (select)  
 2'b00: y = I[0];  
 2'b01: y = I[1];  
 2'b10: y = I[2];  
endcase
```

```
endmodule  
module test_mux;  
reg [3:0] D;  
reg [1:0] S;  
wire Y;
```

mux4_1_bh test(I, select, y);

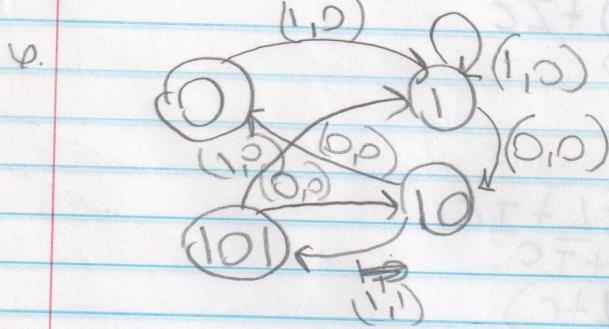
```
initial begin  
  d = 4'b0101;  
  s = 2'b00;  
  repeat (3)  
    s = 2'b01;
```

```
end  
initial
```

\$monitor ("`b`b`b", D, S, Y);

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	Present			Next			JK FlipFlop		
	A	B	C	A	B	C	J	K	J
0	0	0	0	0	X	X	X	X	b
0	0	0	0	0	X	X	X	X	c
0	0	0	1	0	0	1	X	X	a
0	0	1	0	0	0	1	X	X	b
0	1	0	0	1	0	0	X	X	c
0	1	0	1	1	0	0	X	X	a
1	0	0	0	0	1	0	X	X	b
1	0	0	1	0	1	1	X	X	c
1	0	1	0	0	1	0	X	X	a
1	1	0	0	1	0	0	X	X	b
1	1	0	1	1	0	1	X	X	c
1	1	1	0	0	X	X	X	X	a
1	1	1	1	X	X	X	X	X	b



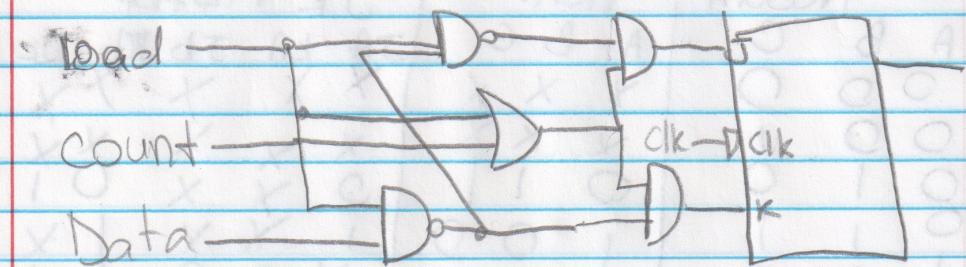
$$D_A = (A \oplus B)$$

$$D_B = B \oplus C$$

$$D_C = \bar{C}$$

	Present			Next			D	
	A	B	C	A	B	C	A	B
0	0	0	0	0	0	1	0	0
0	0	0	1	0	1	0	0	1
0	0	1	0	0	1	1	0	1
0	0	1	1	1	0	0	1	0
0	1	0	0	1	0	1	0	1
0	1	0	1	1	0	0	1	0
0	1	1	0	1	1	1	1	1
1	1	1	1	0	0	0	0	0

7.



A) $J = L\bar{I}_0 + \bar{L}C$
 $K = \underline{L\bar{I}_0 + \bar{L}C}$

B) $J = [L(\bar{L}I)](L+C)$

$$\begin{aligned} &= (\bar{L} + L\bar{I})L + C \\ &= \bar{L}L + L\bar{I}L + \bar{L}C + L\bar{I}C \\ &= \bar{L}I(\bar{L} + C) + \bar{L}C \\ &= \bar{L}I + \bar{L}C \end{aligned}$$

$$\begin{aligned} K &= (\bar{L}I)(L+C) \\ &= \bar{L}L + \bar{L}C + \bar{I}L + \bar{I}C \\ &= \bar{L}C + \bar{I}L + \bar{I}C \\ &= \bar{L}C + \bar{I}(L+C) \\ K &= C + \bar{L}I \end{aligned}$$

It does verify