ECEN4730 Noise Board Report

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## 1. **The project overview**

- My POR AND Expectations for what it means to "work.*"*
  In my POR, the first thing I have planned to do is the continuous ground plane in the bottom layer. But a portion of the bottom layer cannot be poured with ith ground plane since this lab aims to prove the best design practices to reduce the switching and crosstalk noise. Another good design practice is placing the decoupling capacitor near the power supply of each IC component and power rail. The close the decoupling capacitor, the better the noise reduction we can get. For what it means to "work",
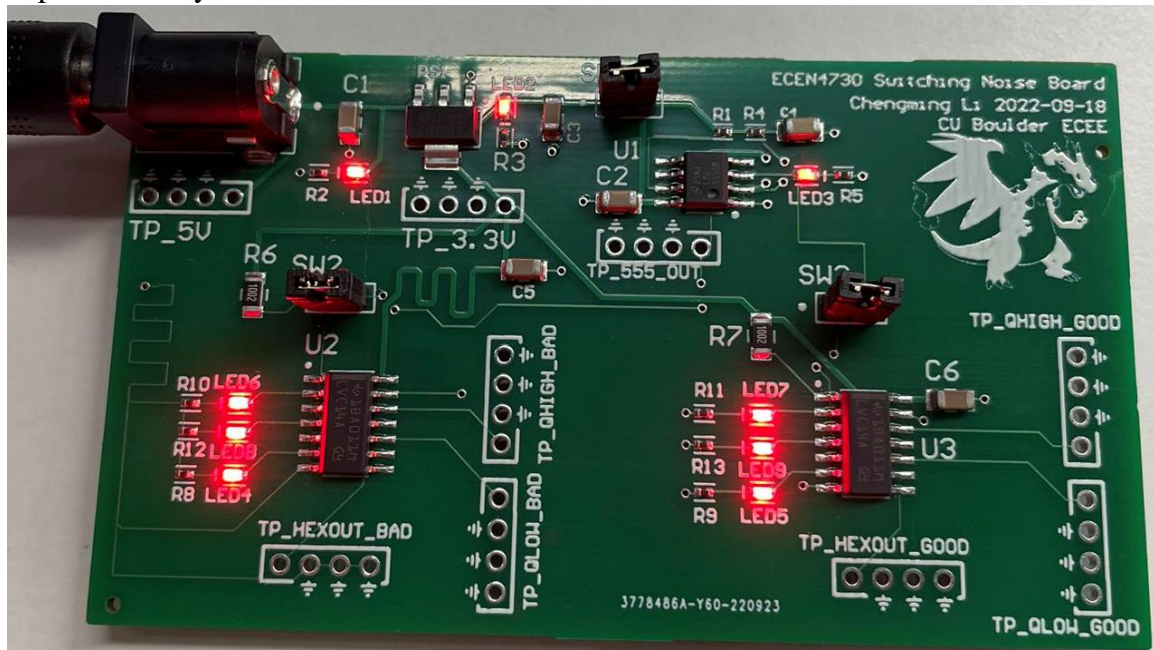
  1) The LDO can convert 5V to 3.3V
  2) The 555 timer output can generate about 500 Hz and about 50% duty cycle signal
  3) I can observe the noise reduction difference between the good layout and bad layout
  4) Pull-up resistor can successfully isolate the circuit. When the switch is not closed, the corresponding inverter circuit will not work as expected.
  5) Red LEDs light up as the load to three of the switching outputs of each hex inverter.
  6) I can measure the Quite High and Quite Low signals from one of the outputs of each hex inverter.
  7) Prove the noise effects of long trace to the decoupling capacitors and shared return path.

- The actual schematic capture used in Altium Designer
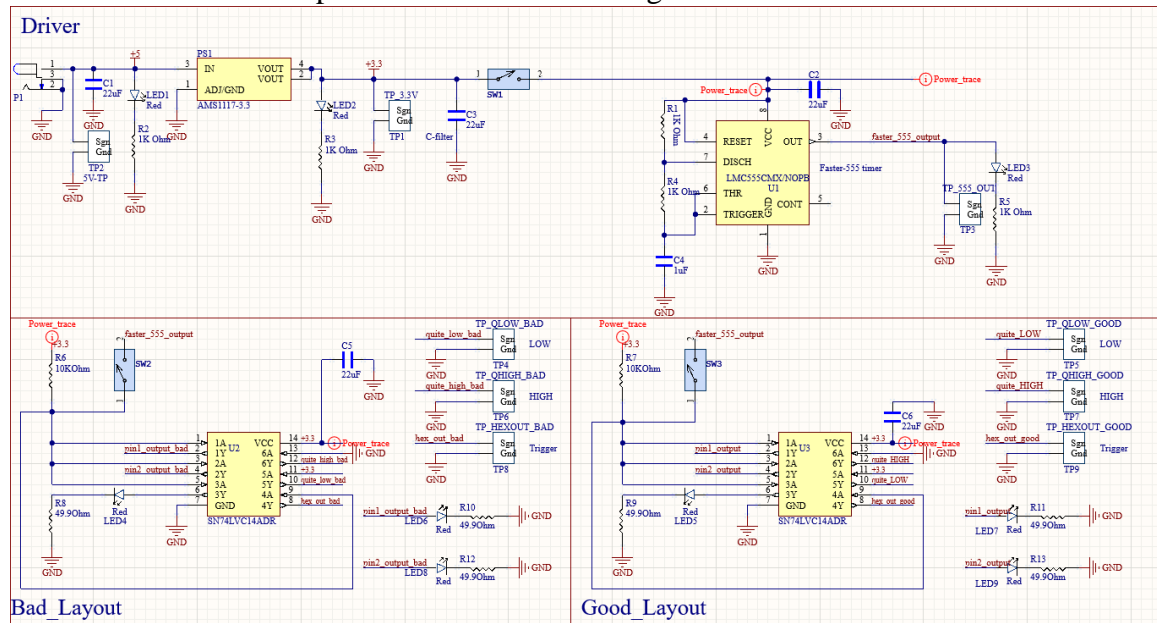
- The board layout I ended up with
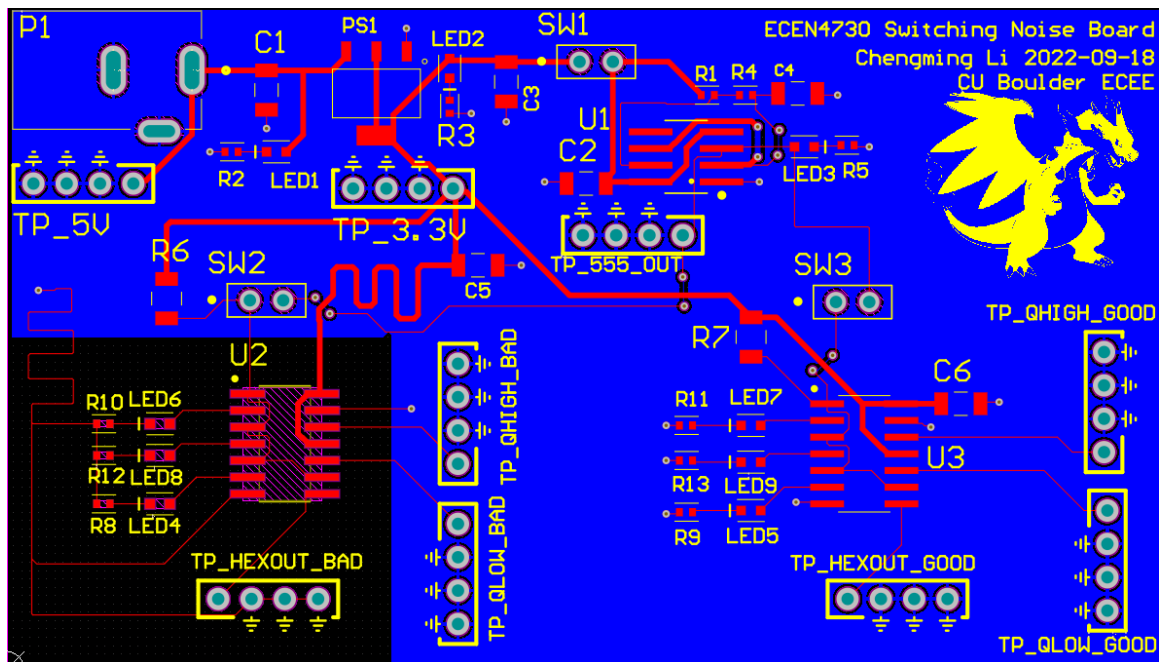
- A picture of my assembled board

2. **What worked**

- Definition of what it means to work
  For what it means to "work",
    1) The LDO can convert 5V to 3.3V
    2) The 555-timer output can generate about 500 Hz and about 50% duty cycle signal
    3) I can observe the noise reduction difference between the good layout and bad layout
    4) Pull-up resistor can successfully isolate the circuit. When the switch is not closed, the corresponding inverter circuit will not work as expected.
    5) Red LEDs light up as the load to three of the switching outputs of each hex inverter.

6) I can measure the Quite High and Quite Low signals from one of the outputs of each hex inverter.
7) Prove the noise effects of long trace to the decoupling capacitors and shared return path.
- What I actually measure to verify my board "work."
  1) The LDO can convert 5v to 3.3V

  2) The 555 timer output can generate about 500 Hz and about 50% duty cycle signal

  3) I can observe the noise reduction difference between the good layout and bad layout

  The left graph shows the switching noise (blue trace) on the 3.3 V rail when the good layout circuit is not connected to the circuit. The switching noise is about 580mV in this case.
  The right graph shows the switching noise(blue trace) on the 3.3V rail when the bad layout circuit is not connected to the circuit. The switching noise is about 108 mV in this case.

  4) Pull-up resistor can successfully isolate the circuit. When the switch is not closed, the corresponding inverter circuit will not work as expected.

  As seen above, the good and bad layouts are successfully isolated from the circuit when either one is not connected to the circuit.

  5) Red LEDs light up as the load to three of the switching outputs of each hex inverter.

As seen in the assembled board, all red LEDs light up.

6) I can measure the Quite High and Quite Low signals from one of the outputs of each hex inverter.
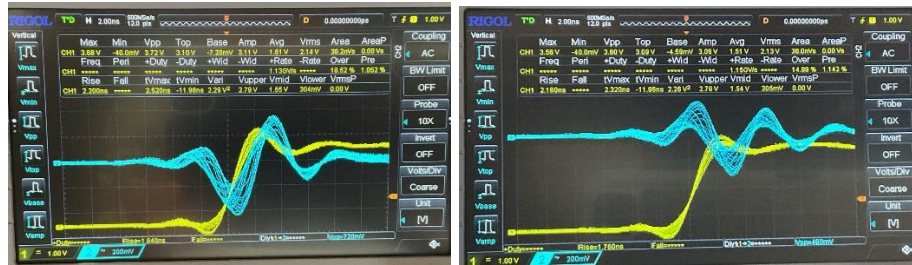
As seen above, the left picture shows the Q_High signal (blue trace) from the good layout inverter.
The right picture shows the Q_Low signal(blue trace) from the good layout inverter.

7) Prove the noise effects of long trace to the decoupling capacitors and shared return path.

As seen in the step 3 pictures, the noise effects are significantly different. Bad layout noise effects are around 5 times good layout noise effects.

- Analysis of the measurements
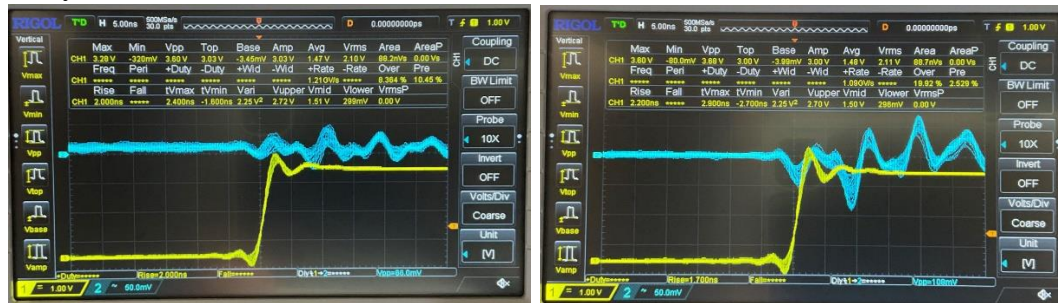
The blue trace on the left displays the switching noise on the 5V rail, which is around 80 mV Vpp. The yellow trace is the trigger source, and it is measured at the output of the inverter.
The blue trace on the right displays the switching noise on the 3.3 V rail, which is around 150mV Vpp. The number is reasonable because the 3.3V is converted from the LDO, which also contributes some effects to the switching noise on the 3.3V rail. Yellow trace is the trigger source, and it is measured at the output of the inverter.
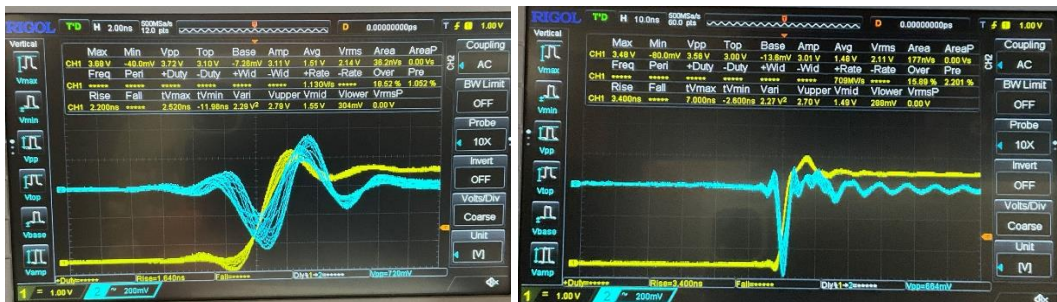
The blue trace on the left picture is the Q_high signal from the good layout, triggered at the output of the inverter from their inverter (Yellow trace). In both pictures, the switching noises are around 800 mV.

On the other hand, the Q_high from the left picture(good layout) has less ringing noise than the right picture. It is due to the Q_high from the right picture(bad layout) having longer trace to the ground than the left picture.
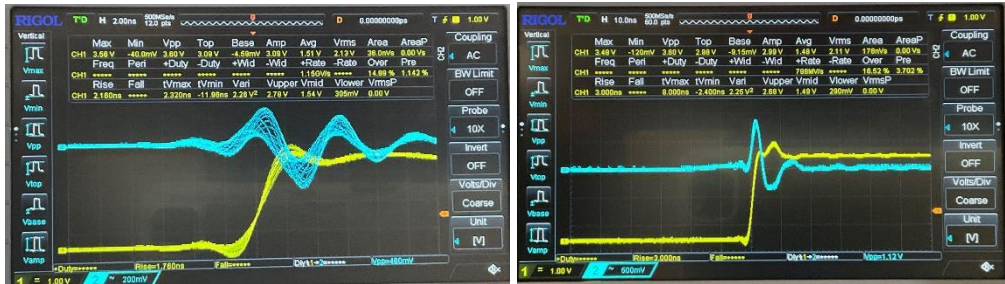

The left picture shows the Q_low from the good layout. The switching noise is about 480 mV.

The right picture shows the Q_low from the bad layout. The switching noise is about 1.12V.

Since the Q_low from the good layout has a decoupling capacitor close the Vcc with a very short path, the noise is significantly reduced. However, the decoupling capacitor in the bad layout is far away from the Vcc pin, and the effects of noise reduction are not significant.

In this experiment, the best layout practice is proved with a closer decoupling capacitor.
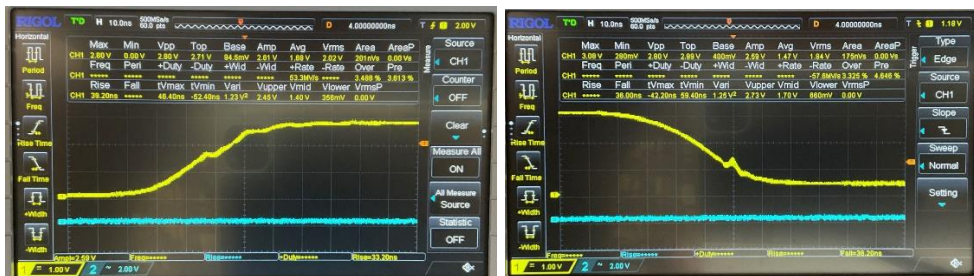
The above pictures show the rise and fall time of the 555 timer output. The rise and fall time of the 555 timer is about 33.2ns.

The above picture shows the rise and fall of the hex inverter output from the bad layout. The rise time is about the 4ns, and the fall time is about the 2ns.

The above picture shows the rise and fall of the hex inverter output from the good layout. The rise time is about 1.4ns, and the fall time is about 1.5ns.

Comparing the rise and fall time of hex inverter output between the good and bad layout, the switching noise from the good layout is not significant. Moreover, the rise and fall time is faster in the good layout.

- Demonstration of best design practices and best measurement practices

  As seen in the right side of the actual layout shown in the first part, the best design practices are having a continuous ground plane in the bottom layer, having non-shared return paths for each component, having decoupling capacitors close to the Vcc of each IC, and having short trace to the decoupling capacitor.

  As seen in the pictures above, the best measurement practices are having a clear signal trace labeled, having integer vertical division and horizontal division on an oscilloscope, and having all position shift in some readable integer positions.

- What did not work

  The Q_high in the good layout portion of the circuit did not work on my board. The Q_high from a good layout has similar switching noise as seen in the Q_high from the bad layout. In other words, the noise is not significantly reduced in the Q_high signal by applying best layout practices.
  After some debugging process, the reason is that they are both connected to the ground and have similar trace lengths. Thus, the switching noise difference between the Q_high from good and bad layout can't be observed clearly.

3. **Analysis of your report**
- What worked and you did well and want to do in future designs
  The pull-up resistor I have is working well, and it successfully isolates either the good layout or the bad layout from the main portion of the circuit. In addition, I have applied good layout practices in the design, which includes the close decoupling capacitor for each IC component, the un-shared return path for each component, and the continuous ground plane in the bottom layer. The continuous ground plane can reduce the effects of crosstalk noises between signals and signals.

- What did not work and what I want to do differently in future designs.
  One thing that doesn't work on board is the Q_high signal because I haven't really applied the bad layout practices in the bad layout section like sharing the return path with other loops. Also, the measurement I did is not good enough since the scaling of signals is not identical, which makes the reader hard to distinguish the difference between the bad layout and the good layout.
- Were there any hard errors- why did they go wrong
  In this design, there are no hard errors. Everything works as I expected in the POR.
- Were there any soft errors that I would like to do differently next time?
  One soft error I had is the Q_high signal in the bad layout portion of the circuit. Since this soft error made intentionally, it would not happen in the next time.