ECEN4730-Lab8-Switching Noise

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1. **Analyze the measurements to compare the switching noise on the good layout and the bad layout**

Figure.1 Rise time of 555 Timer Output

Figure 1 shows the rise time of 555 timer output in the bad layout section. The result is expected since a faster 555 timer (5~6 ns rising time) is used in the circuit.

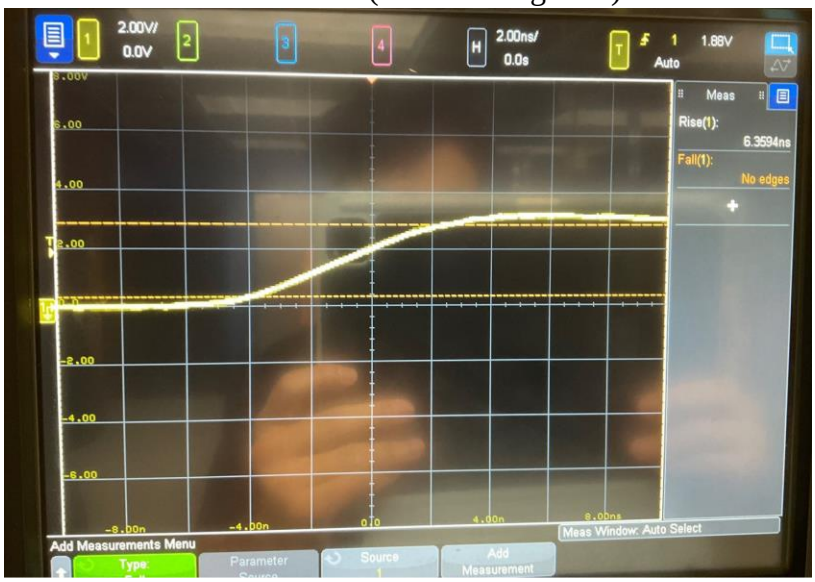

Figure.2 Rise time of Hex Output(Bad-Layout)

Figure 2 shows the rise time of Hex inverter output in the bad layout section. The rise time is 6.35ns, a bit slower than the 555-timer output due to the long latency in the bad layout.

Another measurement, which measures the rise time of the Hex-inverter in the good layout section, has 5.25 as the rise time. And it is reasonable because there is a shorter wire between the 555-timer output and the Hex-inverter input. And, in a good layout, there is a shorter return path, which can reduce the switching noise and give better performance.

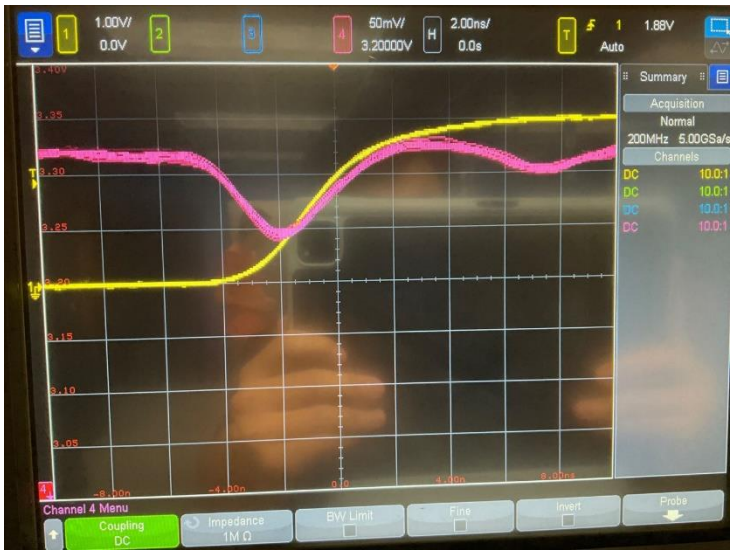

Figure. 3 Q_hi outputs on good layout(pink)

Figure. 4 Q_hi outputs on the bad layout(pink)

Figure 3 shows the good layout's switching noise at the Q_hi output(~75mV drop). Figure 4 shows the bad layout's switching noise at the Q_hi output(0.5V drop). From the magnitude of voltage drop, we can see the benefits of having a good layout. Between the good and bad layout, the good layout has the decoupling capacitor closer to the IC and a shorter return path, and they don’t share the return path.

Figure. 5 Q_Low outputs on the good layout

Figure. 6 Q_Low outputs on the bad layout

Figure 5 shows the good layout's switching noise at the Q_low output(~40mV drop). Figure 6 shows the bad layout's switching noise at the Q_low output(0.4V drop). From the magnitude of voltage drop, we can see the benefits of having a good layout. Between the good and bad layout, the good layout has the decoupling capacitor closer to the IC and a shorter return path, and they don't share the return path.

2. **Features on this board contributed to the reduced noise in the good layout section**

In the good layout section, it has a decoupling capacitor close to the IC, which is an essential factor contributing to noise reduction. The close the decoupling capacitor to the IC, the smaller the switching noise it has. In addition, every path has its return path(ground), which reduces the effect of crosstalk in the circuit. Moreover, the best design practices are applied in this layout, i.e., keeping wire short.

3. **Switching Noise on the 5V and 3.3V rails**

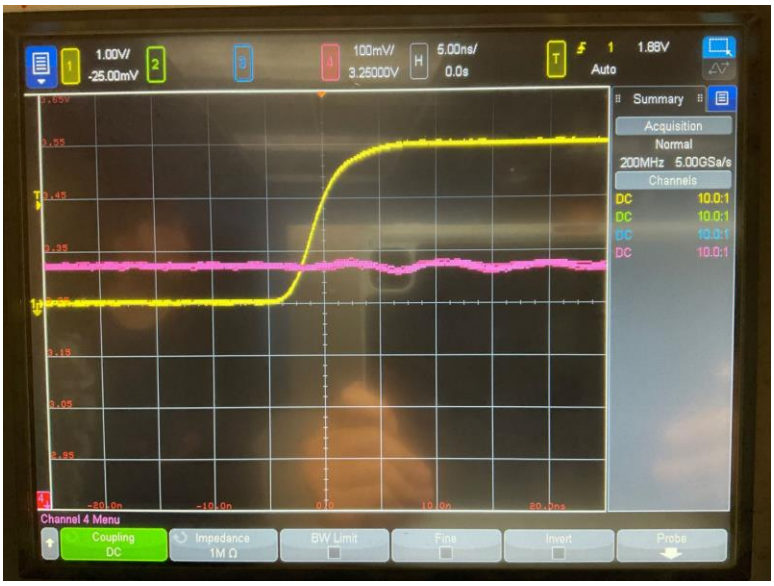

Figure. 7 3.3V rail in the good layout

Figure.8 3.3V rail in the bad layout

Figures 7 and 8 show that the good layout introduces better circuit performance or minor switching noise in the transition edge. In addition, from Figure8, the ringing in the signal is more apparent than the signal in a good layout.

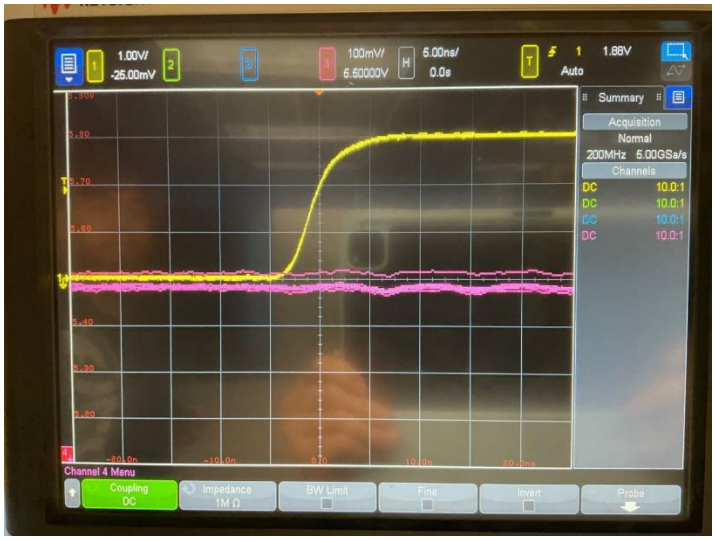

Figure. 9 5V rail in the good layout

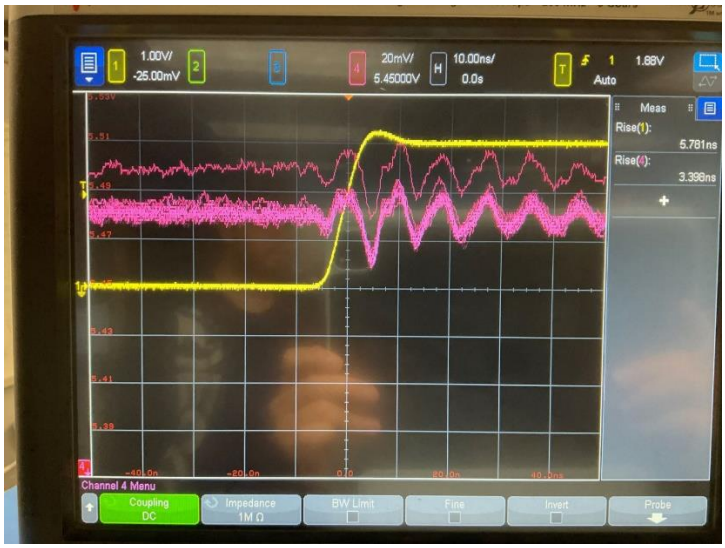

Figure. 10 5V rail in the bad layout

As shown in Figures9 10, the good layout introduces better circuit performance or minor switching noise in the transition edge. In addition, from Figure 10, there is more ringing noise in the signal due to the bad layout of the circuit.

4. Best Design Guidelines

For the best design guidelines, the circuit designer should place the decoupling capacitor close to the IC component, greatly reducing the switching noise. Decoupling capacitors significantly reduce the effect of dI/dt in the circuit. Moreover, keeping the wire short is also essential since it reduces the L(inductance) in the circuit loop. A shorter path means less inductance, reducing the dV/dt at the transition edge. Last but not least, every circuit loop should own its return path(ground), which reduces the effects of crosstalk between two different closed loops.