

**ECE265D**  
**Homework #1**  
**Due 3pm on Jan. 24th (Fri)**

**Prasad Gudem**  
**Adjunct Professor, Electrical and Computer Engineering**

**University of California San Diego**  
**La Jolla, California**

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## **Simulation Conditions & Process Parameters**

- Please save all your schematics as you might reuse them in later assignments (2 & 3).
- Simulation Conditions:
  - Temperature =  $27^{\circ}\text{C} = 300\text{K}$
  - Process corner = Nominal
  - Supply voltage = 1.8V
- Thin-oxide MOS Process Parameters for 65nm: pch/nch (Regular  $V_t$  – PFET/NFET).
  - Effective mobility of electrons =  $400\text{cm}^2/\text{V.s}$
  - Effective mobility of holes =  $250\text{cm}^2/\text{V.s}$
  - Gate oxide capacitance ( $C_{ox}$ ) =  $6\text{fF}/\mu\text{m}^2$
  - Threshold voltage = 450mV
  - $V_E = 10\text{V}/\mu\text{m}$
  - $L_{min} = 60\text{nm}$

## Instructions for the homework

- “Simulate” implies simulate in Cadence and plot the results
- “Calculate” implies show your calculations
- Towards the end of this homework you will complete the design of the DAC for the transmitter.
- It has 4 parts each part focuses on different transistors in the DAC design. Each part starts with a few qualitative kick starter questions that should kick start your thinking process on design. Following which you will go through a series of detailed steps leading to design.
- Each step is listed in one single slide. Place your answer within the slide. We have also provided *place holders* and extra pages. In case you require extra slide please feel free to add them but ensure you map them on Gradescope.
- Map all your slides to question while submitting on Gradescope.
- You can clear the *place holder* (*in italics*) while filling in the content for that particular *place holder*.

# Digital-to-Analog Design Requirements for Transmitter Application

- Type: P-Type, Segmented, Current Steering, Oversampling, Non-Return to Zero, Medium Precision
- Core DAC DC Current = 2mA & DC Supply Voltage = 1.8V
- Output Common-Mode DC Voltage = 0.4V
- Output Load Impedance = 1k Ohm (differential)
- Signal Bandwidth = 5MHz at RF (2.5MHz at Baseband) in B13-LTE (UL: 777 – 787MHz & DL: 746 – 756MHz)
- Modulation = 16QAM
- Sampling Rate = 20x OSR (100MHz)
- Number of Bits = 8
- SNDR = 42dB (DAC only) to support 12.5% EVM Tx system budget
  - SNR > 60dB (Quantization Noise only) & DNL =  $\frac{1}{2}$  LSB
  - IMR3 (differential) > 46dB
  - IMR2 (single-ended) > 46dB
  - Thermal Noise < 10dB below quantization noise
- ACLR = 42dB to support 33dB Tx system budget
  - SFDR > 46dB & INL =  $\frac{1}{2}$  LSB
  - HDR3 (differential) > 46dB
  - HDR2 (single-ended) > 46dB
- LTE RxBN at 60MHz offset = -135dBm/Hz to support -130dBm/Hz Tx system budget
- GPS RxBN at 400MHz offset = -140dBm/Hz to support -130dBm/Hz Tx system budget
- Clock feedthrough & Images

## **Part 1: Design of LSB Current Source [100 points]**

## **Part 1: Notes on Design of LSB Current Source**

- Objective of this Part 1 is to find the sizing of LSB current source transistor given the design choice of 2mA DAC Core current and 200mV overdrive voltage.
- Note: DAC Core current doesn't include the current in the biasing branches. It only includes current in all the core branches ( i.e from LSB to MSB)

# Part 1: Kickstarter Questions - Design of LSB Current

All the questions in this slide are qualitative questions, put your answers very brief.

- Given the design choice of DAC Core current and LSB Current Source transistor's overdrive voltages, can you fine the aspect ratio ( W/L ) of the LSB current source transistor, Yes or No?  $I_d = \frac{1}{2} \mu n \lambda \text{ox} \frac{W}{L} V_{ov}^2$

Yes

( Note: For next two question ignore short channel effects, assume transistors scale well with length )

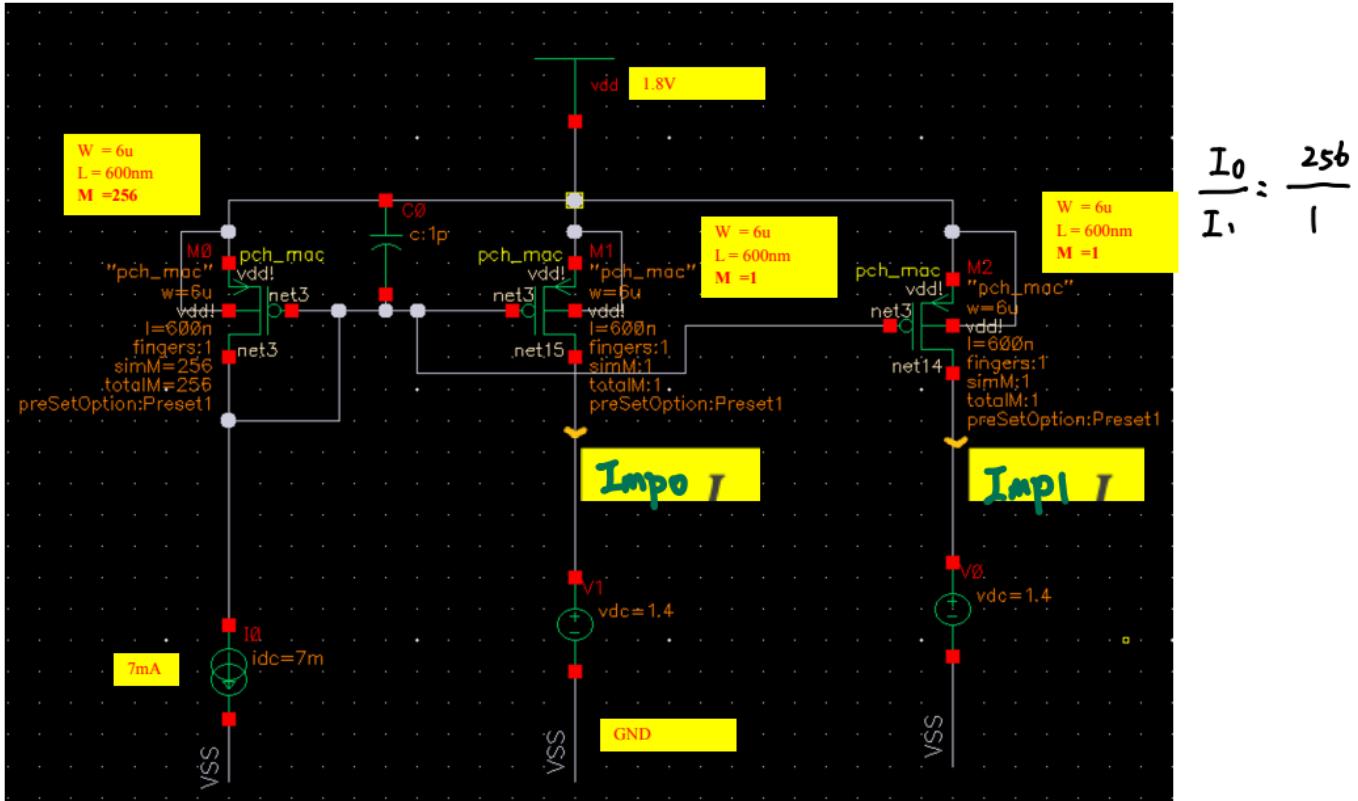
L\_min : minimum possible length; L\_max: maximum possible length

- Given W/L,
  - Why cannot you use L\_min?

The corresponding width would be big, device matching is difficult considering process variation

Big Parasitic Capacitor would be seen, narrow BW, slower response

# Schematics for Part 1



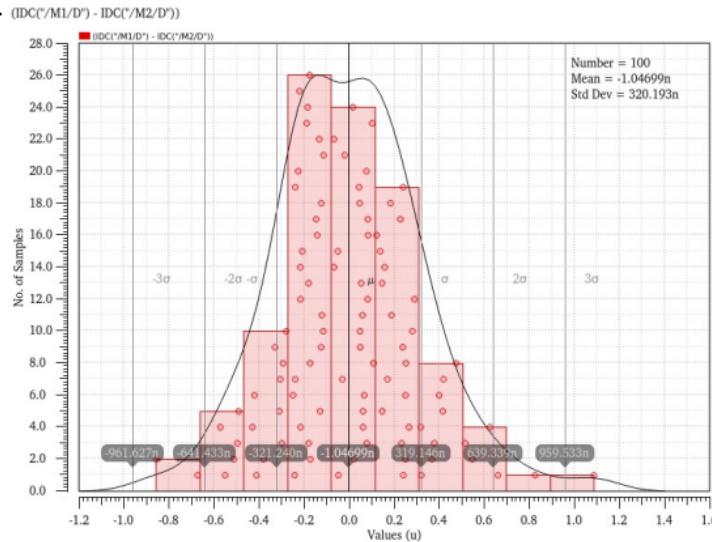
Schematic for part 1

# Step 1

- Run 100 Monte-Carlo DC simulations of PMOS and plot distribution of ( $IMP0 - IMP1$ ): (schematics previous page)
  - $W = 6\mu m, L = 600nm$
  - Overdrive voltage = 200mV
  - $V_{ds} = 400mV$

- **Please monitor your quota, and clear it when required. Please refer to the HW #1 Cadence tutorial.**

- Place your histogram here



## Step 2

- Using the results in step 1, calculate standard deviation in current mismatch of IMP0 by dividing the results in step 1 by  $\sqrt{2}$ . Explain the reason for division by  $\sqrt{2}$ .

$$\text{STD DEV IMP0} = \frac{320.139}{\sqrt{2}} = 226.37 \text{ n}$$

Division by  $\sqrt{2}$  is converting the value to RMS value

### Step 3

- Assuming mismatch is dominated by threshold voltage mismatch, calculate the coefficient of mismatch (AVT) in Pelgrom's law.

Pelgrom's Law:  $\sigma_{VT}^2 = \frac{A^2 VT}{WL}$

$$\frac{\sigma_{I_{DS}}^2}{I_{DS}^2} = \left(\frac{6B^2}{\beta}\right) + \frac{4\sigma_{VT}^2}{(V_{GS}-VT)^2}$$

$V_{DN}=200mV$     $V_t = 450$   
 $V_{GS}=650mV$

$\therefore V_T$  dominates

$$I_{DS} = \frac{7m}{25b}$$

$$\frac{\sigma_{I_{DS}}}{I_{DS}} = \frac{2\sigma_{VT}}{V_{GS}}$$

$$\sigma_{VT} = \frac{\sigma_{I_{DS}} \cdot V_{GS}}{2 I_{DS}}$$

$$= 828 \mu V$$

From Ch.3 pg.26

Variance of  $V_T$  among adjacent transistors reduces inversely with the gate area

In the current DAC design, begin with ① fixed power budget  
 ② fixed  $V_{GS}$  → dictate a fixed current,  $I_{ref}$  and a fixed  $\frac{W}{L}$

$\therefore$  Increase both  $W$  and  $L$  by the same factor.

$\hookrightarrow \uparrow$  Area,  $C_{para}$

$$AVT = \sqrt{(828 \mu V)^2 \cdot 6 \mu A \cdot 600 \Omega}$$

$$= 1.57 \text{ n}$$

## Step 4

- Using the Pelgrom's mismatch coefficient, calculate the area ( $W \cdot L$ ) of the current source transistor to meet  $3\sigma \text{ INL} = \frac{1}{2} \text{ LSB}$ .

$$3 \delta_{\text{INL},\max} < 0.5 \text{ LSB} \quad \text{From Ch.3 pg.45}$$

$$\Rightarrow \delta_{LSB} < \frac{1}{3} \cdot \frac{1}{2^{12}} I_{LSB} \Rightarrow \delta_{LSB} < 1\% [I_{LSB}]$$

$$\frac{\delta_{LSB}}{I_{LSB}} = \frac{2}{V_{DD}} \cdot \frac{A_{VT}}{\sqrt{W_{LSB} \cdot L}} = 0.0208$$

$$\left( \left( \frac{2}{V_{DD}} \right) \cdot \frac{1.57 \text{nA}}{0.0208} \right)^2 = W \cdot L$$

$$\boxed{W \cdot L = 5.69 \cdot 10^{-3} \\ = 0.569 \mu\text{m}^2}$$

## Step 5

- Total Core DAC DC current is 2mA, calculate the cur

$$I_{\text{u}} = \frac{I_{\text{tot}}}{2^n} = 7.8125 \mu\text{A}$$

## Step 6

- Overdrive voltage of 200mV, calculate the W/L of the transistors rather than calculating using model para

$$\frac{W}{L}_{\text{old}} = 26.3 \mu \rightarrow \text{from simulation}$$

$$\frac{I_{D,\text{req}}}{I_{D,\text{old}}} = \frac{7.8125 \mu}{26.3 \mu} = \frac{\frac{W}{L}_{\text{req}}}{\frac{W}{L}_{\text{old}}} = 0.297$$

$$\begin{aligned}\frac{W}{L}_{\text{req}} &= 0.297 \cdot \frac{6 \mu}{600 \text{n}} \\ &= 2.97\end{aligned}$$

## Step 7

- Using the results from step 4 and step 6, calculate the W and L of the LSB current source transistor.

$$\textcircled{1} \frac{W}{L} = 2.97$$

$$\textcircled{2} W \cdot L = 0.569 \mu\text{m}^2$$

\textcircled{1} into \textcircled{2}

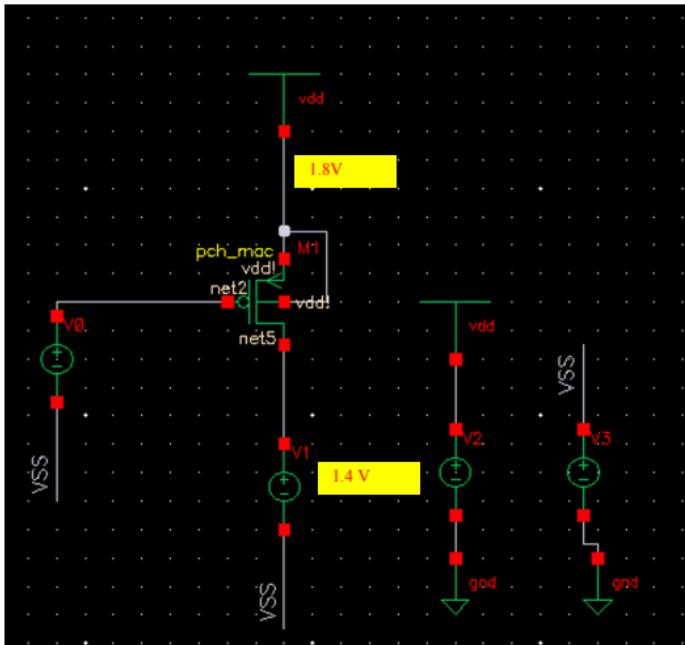
$$2.97 L \cdot L = 0.569 \mu\text{m}^2$$

$$L = 438 \text{ n}$$

$$W = 1.3 \mu$$

## Step 8

- Using the W & L of the LSB current source transistor 200mV. Use the schematic as shown, assume  $V_{th}$



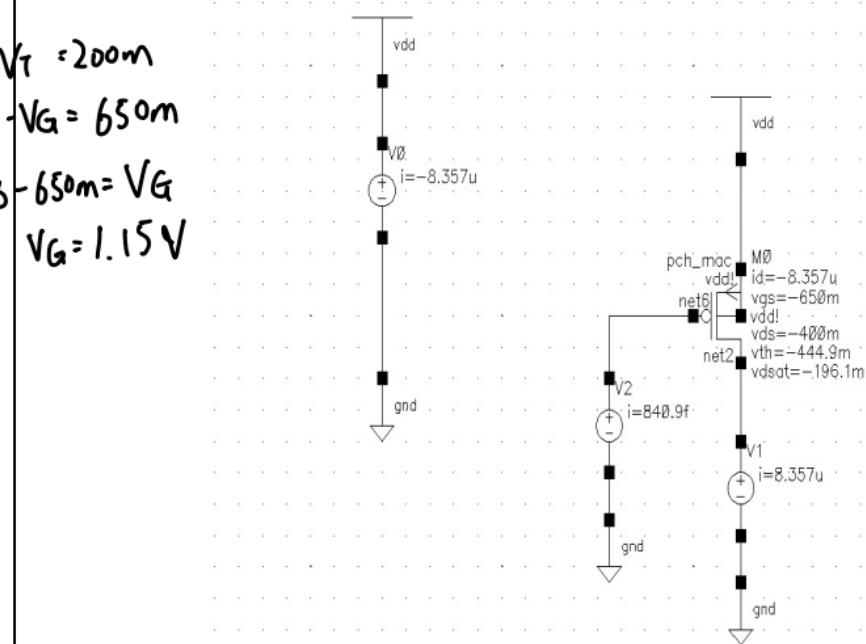
$$V_{SG} - V_T = 200\text{m}$$

$$V_S - V_G = 650\text{m}$$

$$V_S - 650\text{m} = V_G$$

$$V_G = 1.15\text{V}$$

Please you DC operating point annotated schematic below



## Step 9

- In simulation, increase W by a scaling factor “f” and decrease L by the same scaling factor “f” to achieve the desired LSB current while holding W\*L constant to not impact mismatch of the LSB current source (and therefore INL).

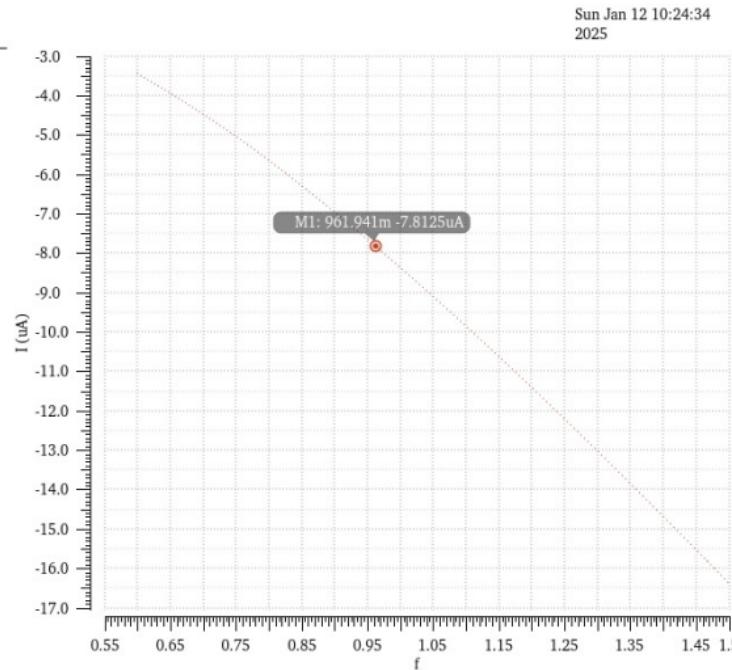
$$f=961 \text{ m. } W \approx 1.25 \mu \text{m. } L=460 \text{ nm.}$$

Show your notes for scaling below, final value of W & L , ( reason out how did you choose/narrow down/find the value of "f")

By adding a variable in W and L  
so We get

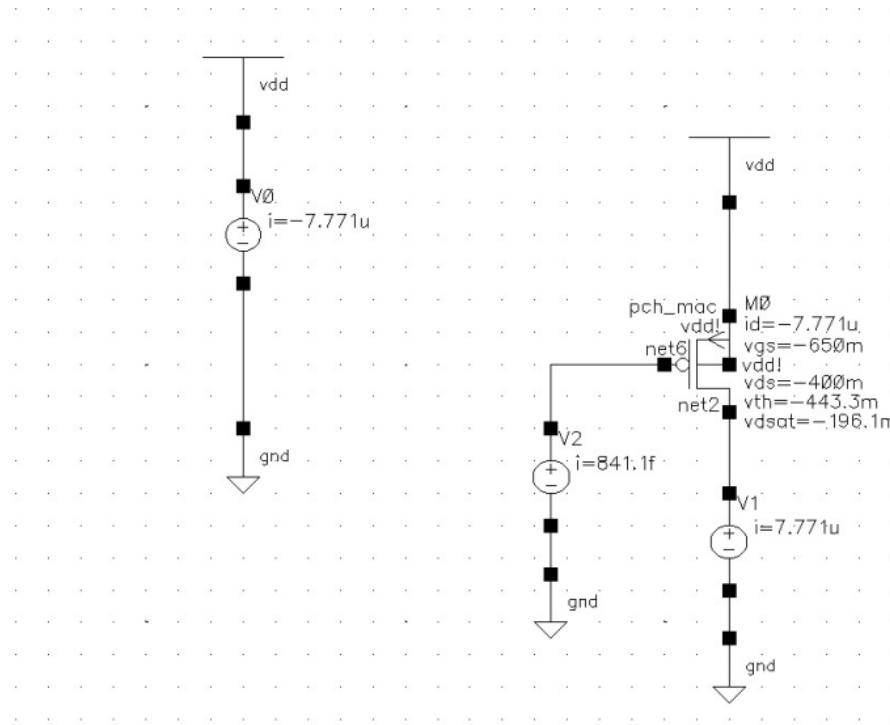
$$W \cdot f + L \cdot \frac{1}{f}$$

And sweep the f to get the  
desired LSB current



# Step 9 – Schematic with annotated DC op point

Place the schematic with DC op point here



$$W = 1.25\mu$$

$$L = 460\text{nm}$$

## Step 10

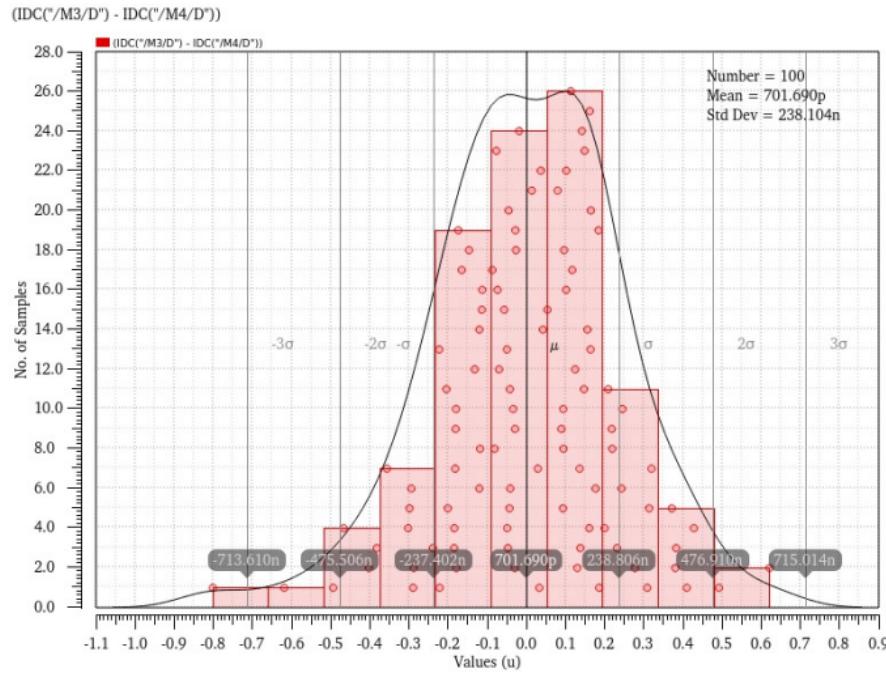
- Re-run Monte-Carlo simulations in step 1 with the current mismatch in terms of fraction of LSB ( $I_{LSB}$ ).

Place your histogram plot here.

$$6L_{SB} < \frac{1}{3} \cdot \frac{I}{2^{n_2}} I_{LSB}$$

$$\frac{6L_{SB}}{I_{LSB}} < 0.0208$$

$$\frac{\frac{238.104n}{T_2}}{7.8125u} = 0.02155$$



## **Part 2: Design of the LSB Cascode [120 points]**

## **Part 2: Notes on Design of LSB Cascode**

- Objective of this Part 2 is to find the sizing of LSB cascode transistor given the constraint to meet the output impedance requirement current and design choice of 200mV overdrive voltage.



## Part 2: Kickstarter Questions - Design of LSB Cascode

All the questions in this slide are qualitative questions, put your answers very brief:

- Given LSB current source and design choice of LSB cascode's transistor overdrive voltage, can you fine the aspect ratio ( W/L ) of the LSB cascode, Yes or No?

Yes

( Note: For next two question ignore short channel effects, assume transistors scale well with length )

L\_min : minimum possible length; L\_max: maximum possible length

- Given W/L,
  - Why cannot you use L\_min?

Hard to do matching

- Why cannot you use L\_max ?

Slow-down the DAC, low speed

## Step 1

- Calculate  $r_o$ , unit of the LSB current source. Use process parameters stated in slide no. 2

$$r_o = \frac{L \cdot V_E}{I_{LSB}} = \frac{460n \cdot \frac{10V}{\mu m}}{7.771u} = 591.95 k\Omega$$

↓  
from  
Part-Step 9

## Step 2

- Calculate co-unit of the LSB current source. Use process parameters stated in slide no. 2

$$\begin{aligned} \text{c}_{d,LSB} &= \left( \frac{1}{3} \right) C_{ox} W_{LSB} L = \frac{1}{3} \cdot 6 \frac{10^{-15}}{10^{-12}} \cdot 1.25\mu \cdot 460 \text{n} \\ &= 1.15 \text{ fF} \end{aligned}$$

### Step 3

- What is the corner frequency of the impedance due to  $r_o$ ,unit and  $c_o$ ,unit? How does it compare with sampling rate of the DAC?

$$f_c = \frac{1}{2\pi r_o c_o} = 233.8 \text{ MHz}$$

$$f_{\text{sample}} = 100 \text{ MHz}$$

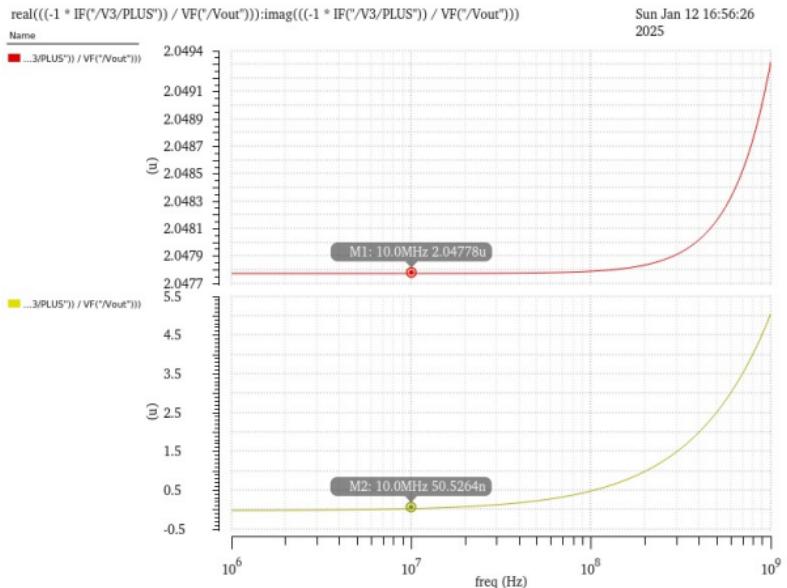
$$f_s > f_c$$

## Step 4 $Z = R + jX$      $X = \frac{1}{j\omega C}$

- Simulate the output admittance of the LSB current source from 1MHz to 1GHz and measure  $r_o$ ,  $c_o$  and corner frequency at the drain of the LSB current source.

$$Y = G + j\beta \rightarrow \frac{1}{R_o} + j\omega C \quad \beta = \omega C \quad C = \frac{\text{Imag}(Y)}{\omega}$$

Place the plot of real and imaginary part of Admittance



Show calculation in this box

$$r_o = \frac{1}{2.0478u} = 488.3k\Omega$$

$$C_o = \frac{50.5264n}{2\pi \cdot 10M}$$

$$= 0.8fF$$

$$f_c = \frac{1}{2\pi r_o C_o}$$

$$= 407.4 MHz$$

## Step 5

- Compare the simulation results in step 4 with calculations in step 1 – 3.

Parameter	Calculated (cal)	Simulated (sim)	% error (sim - cal)/cal * 100
$\gamma_0$	591.95 kΩ	488.3 kΩ	-17.51%
$C_0$	1.15 fF	0.8 fF	-30.4%
$f_c$	233.8 MHz	407.4 MHz	74.25%

Reason out what possibly could have caused the error, if the error is (large i.e > 5%)

$V_E$ ,  $C_{ox}$  is not a linear relationship w.r.t.  $W$  and  $L$



## Step 6

- Using the results in step 4, calculate the highest achievable INL of the DAC in terms of fractions of LSB. Does it meet the DAC INL requirements? (For  $R_L = 500 \Omega$ )

$$INL = \frac{1}{2} LSB$$

$$INL_{\max} < \left(\frac{1}{2}\right) I_{LSB} \Rightarrow \left[ \left(\frac{N}{2}\right)^3 \left(\frac{R_L}{r_{o,unit}}\right)^2 \right] < \left(\frac{1}{2}\right)$$

$$\left[ \left(\frac{256}{2}\right)^3 \cdot \left(\frac{500}{4883k}\right)^2 \right] = 2.2 < \frac{1}{2}$$

It does not meet the DAC INL requirements

## Step 7

- Calculate the  $r_o$  unit of the LSB unit cell of the DAC to meet the INL requirements.

$$\sqrt{\left(\frac{N}{2}\right)^3 \cdot \frac{R_L^2}{\frac{1}{2}}} < r_{o, \text{unit}}$$

$$r_{o, \text{unit}} > 1.024M \Omega$$

## Step 8

- Boosting the output resistance using a cascode to meet INL requirements with margin. Cascode overdrive voltage = 200mV. Calculate the channel length of the cascode to achieve 50x higher  $r_o$ ,unit in step 4 for the LSB current source + cascode.

$$r_{o,unit} \approx r_{ds,cs} \left( g_{m,cas} r_{ds,cas} \right) = 672 M\Omega$$

$$r_{o,unit} \approx \left( \frac{1}{\omega c_{d,cs}} \right) \times \left( g_{m,cas} r_{ds,cas} \right) = 2.3 M\Omega @ 100MHz$$

$$c_{o,unit} = 13 fF / 40 = 0.32 fF \Rightarrow 5 M\Omega @ 100MHz!$$

$$\gamma_0 = \frac{V_E \cdot L}{I_{LSB}}$$

$$\begin{aligned} \textcircled{1} \quad 50 \cdot \gamma_{o,unit} &= \gamma_{o,req} \\ &= 24.415 M\Omega \end{aligned}$$

$$\textcircled{2} \quad \gamma_{o,req} = \gamma_{o,unit} \cdot \left( \frac{2 I_{LSB}}{V_{ov}} \cdot \frac{V_E \cdot L}{I_{LSB}} \right)$$

$$\gamma_{o,req} = \gamma_{o,unit} \left( \frac{2 V_E \cdot L}{V_{ov}} \right)$$

$$\begin{aligned} \textcircled{3} \quad L_{cas} &= \frac{\gamma_{o,req}}{\gamma_{o,unit}} \cdot \frac{V_{ov}}{2V_E} = 50 \cdot \frac{0.2}{2V_E} \\ &= 0.5 \mu \end{aligned}$$

## Step 9

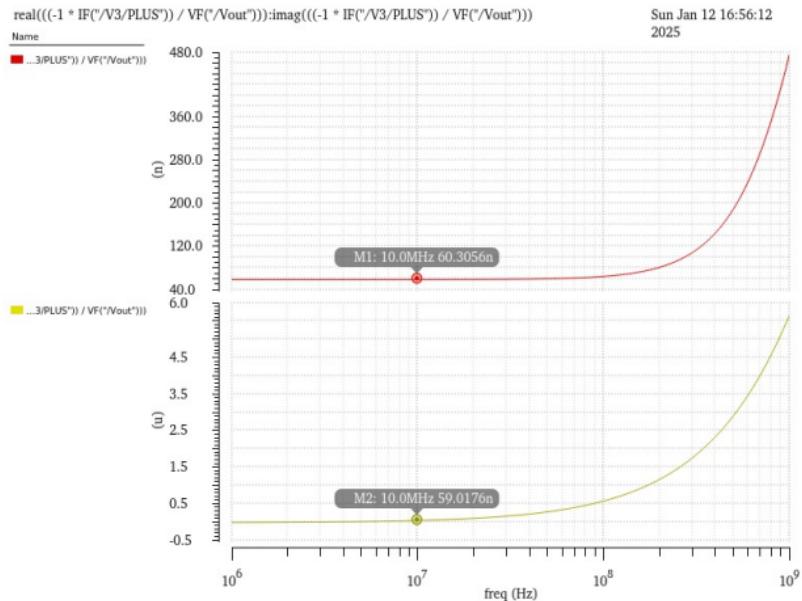
- Calculate the width of the cascode to support the L length determined in step 8. Use scaling of existing like  $\mu_p, C_{ox}$ .

$$\frac{W_{LSB}}{L_{LSB}} = \frac{1.25 \text{ } \mu}{460 \text{ } n} = \frac{W_{cas}}{L_{cas}} \Rightarrow W_{cas} = 1.358 \text{ } \mu$$

# Step 10

- Simulate the output admittance of the LSB current source + cascode from 1MHz to 1GHz with Vds = 400mV for each transistor and calculate ro,unit and co,unit at the drain of the cascode.(Note: Bias the cascode with a DC voltage source, and connect body to the VDD and not to source).

Place the plot of real and imaginary part of Admittance



Show calculation in this box

$$V_{DS} - V_{DS} = V_{S, cas} = 1.4V$$

$$V_{SG} - V_t = 200 \text{ mV} \quad V_t = 450 \text{ mV}$$

$$V_S - V_G = 650 \text{ mV}$$

$$V_S - 650 \text{ mV} = V_G = 0.75$$

$$r_o = \frac{1}{60.3056 \text{ n}} = 16.58 \text{ M}\Omega$$

$$C_0 = \frac{59 \cdot 0.0176}{2\pi \cdot 10 \text{ M}} = 0.94 \text{ fF}$$

$$f_C = \frac{1}{2\pi r_o C_0} = 10.218 \text{ M Hz}$$

## Step 11

- Compare the simulation results in step 10 with target  $r_o, \text{unit}$  in step 8

Simu	$r_o - \text{target}$	error %
16.58 M $\Omega$	24.415 M $\Omega$	-32.84%

Simulation results < target.  $r_o, \text{unit}$  from step 8

## Step 12

- Using the simulation results in step 10, calculate the corner frequency of the impedance of the unit cell.

$$f_C = \frac{1}{2\pi r_0 L_0} = 11.17 \text{ MHz}$$

## **Part 3: Design of the Differential Switch [80 points]**

## Part 3: Kickstarter Questions - Design of Differential

All the questions in this slide are qualitative questions, put your answers very brief.

- Given you have designed LSB current source & Cascode and design choice of Differential switch transistor's overdrive voltage, can you fine the aspect ratio ( W/L ) of it, Yes or No?

Yes

( Note: For next two question ignore short channel effects, assume transistors scale well with length )

$L_{min}$  : minimum possible length;  $L_{max}$ : maximum possible length

- Given  $W/L$ ,
  - Why cannot you use  $L_{min}$ ?

Very Hard to do the matching

- Why cannot you use  $L_{max}$  ?

Big parasitic would be seen , and so slow down the DAC operations

## Step 1

- Calculate the rise/fall time of the switch driver in pico-seconds to meet 10% of sample time at 50% duty cycle target.

$$f_{SR} = 100 \text{ MHz}$$

$$50\% \text{ duty cycle: } 10n \cdot \frac{1}{2} = 5n$$

$$T_r/T_f = 10\% \cdot 5n = 0.5n$$

## Step 2

- Calculate the area of the differential switch to ensure that the 3\*sigma switching time does not vary by more than 10% between the various LSB units.

$$\sigma_{M_d} \approx \left( \frac{\sqrt{2}\sigma_{V_T}}{V_{sw}} \right) T_r = \left( \frac{\sqrt{2} \times 28mV}{400mV} \right) \times 0.5ns = 50ps$$

$$3\sigma_{std} \approx \frac{3\sqrt{2} \cdot V_T}{300m} \cdot 0.5n < 0.1 \cdot 0.5n$$

$$V_T < 0.0071$$

$$\begin{aligned} \sigma_{VT}^2 &= \frac{A_{VT}^2}{WL} \Rightarrow WL = \frac{A_{VT}^2}{\sigma_{VT}^2} = \frac{(1.57mV\cdot\mu m)^2}{(0.0071)^2} \\ &= 4.93 \cdot 10^{-14} \end{aligned}$$

### Step 3

- Calculate W/L of the differential switch assuming an overdrive voltage of 200mV for the differential switch to fully steer the LSB current.

$$I_{LSB} = \frac{1}{2} u_n C_{ox} \frac{W}{L} \cdot V_{ov}^2$$

$$7.8125u = \frac{1}{2} \cdot 250 \cdot 10^{-4} \cdot 6 \frac{10^{-15}}{10^{-12}} \cdot 0.2^2 \cdot \left( \frac{W}{L} \right)$$

$$\frac{W}{L} = 2.6$$

## Step 4

- Using the results in step 2 and step 3, calculate the W and L of the differential switch.

$$\frac{W}{L} = 2.6 \quad W \cdot L = 4.93 \cdot 10^{-14}$$

$$W = 2.6L \quad 2.6L^2 = 4.93 \cdot 10^{-14}$$

$$L = 0.1376 \mu = 137.6 \text{n} \approx 140\text{n}$$

$$W = 0.3583 \mu = 388.3 \text{n} \approx 390\text{n}$$



## Step 5

- Step 5: Build the schematic with the current source + cascode + differential switch (from step 4). Common-mode voltage at the gate of the differential switch is 400mV and the differential swing of 300mV i.e. HI = 550mV and LO = 250mV. Common-mode voltage at the drain of the differential switch (output of the DAC) is 500mV. Simulate the unit cell LSB with HI = 550mV and LO = 250mV to steer the LSB current to one branch of the differential switch. Measure efficiency of current steering in percentage and express the result in fractions of LSB. Determine the total incomplete switching current for DAC at full-scale expressed in fractions of LSB. (note: Connect the body to VDD and not to the source.)

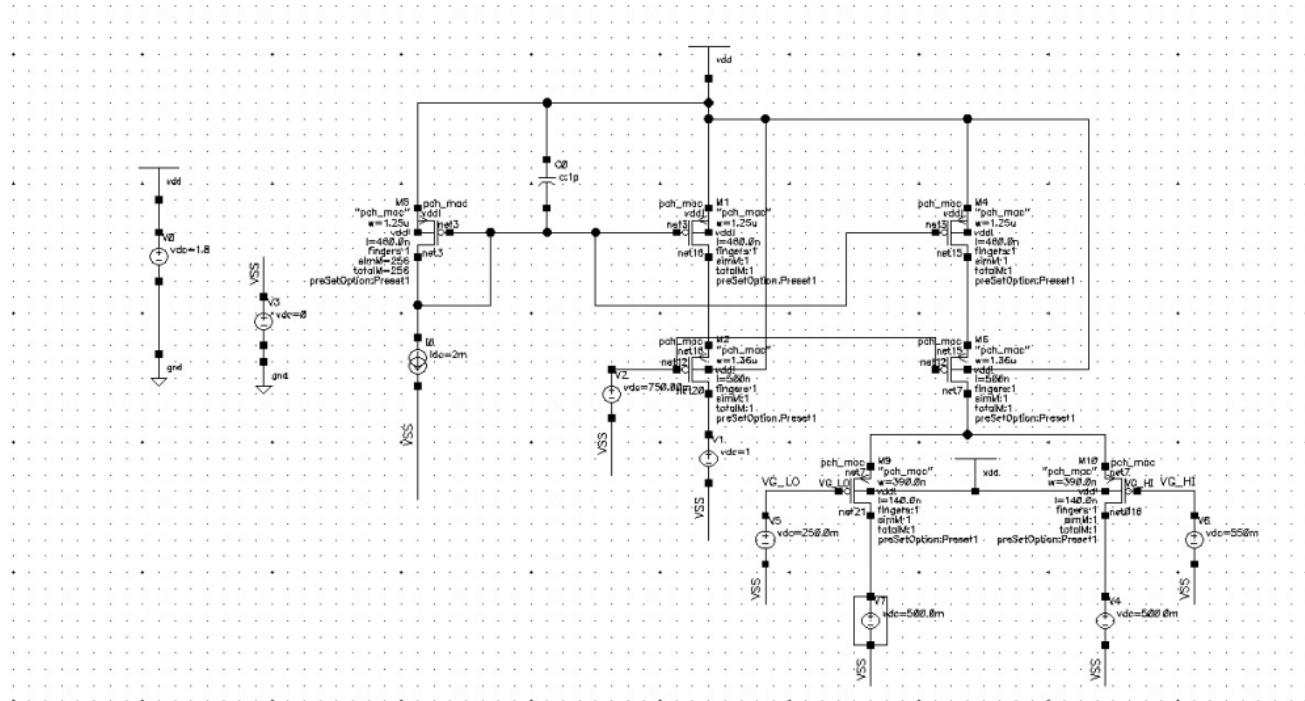
Show your calculations below

$$I = \frac{7.37 \text{ u} \cdot 45.16\text{n}}{7.37 \text{ u}} = 0.9939 \text{ LSB}$$

$$I_{\text{total incomplete}} = \frac{255 \cdot 45.16\text{n}}{7.37 \text{ u}} = 1.5625 \text{ LSB}$$

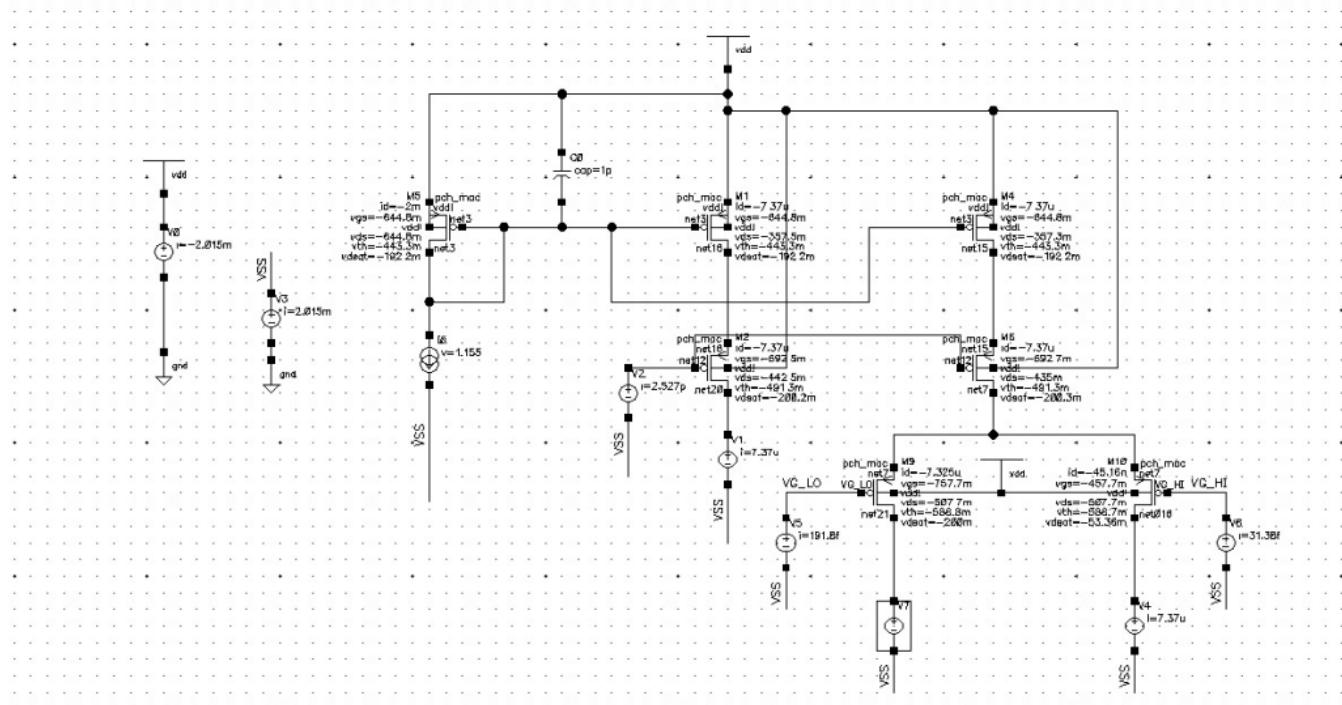
### **Step 5 – Schematic showing component parameters**

- Place your schematic with component parameters here



# Step 5 – Schematic showing DC op

- Place your schematic with DC OP here

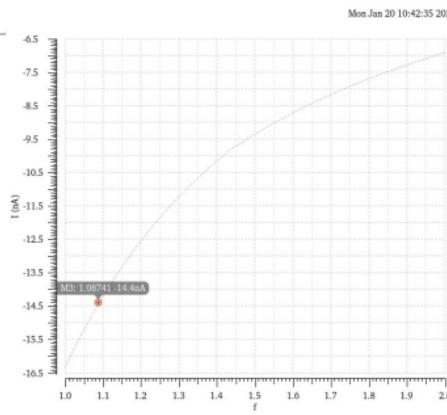
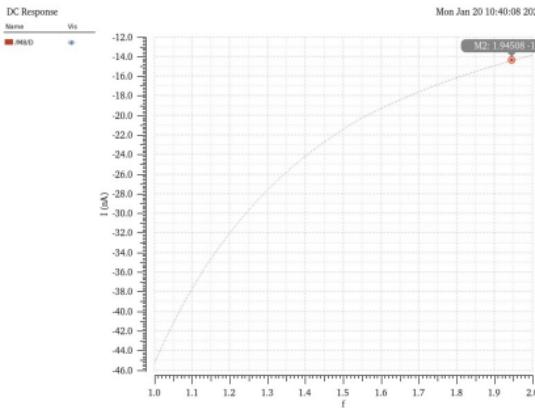


## Step 6

- Step 6: Scale the width of the differential switch to ensure that the total incomplete switching current for DAC at full-scale is < 0.5LSB.

Write your notes on how you scaled the transistors in this slide:

$$W_{sw} = 390n \cdot [0.94508 \cdot 1.0871] \\ = 758 \text{ n}$$



$$0.5 \text{ LSB} = 3.6855 \mu$$

$$\frac{I_{incomplete} \cdot 255}{I_{LSB}} < 0.5$$

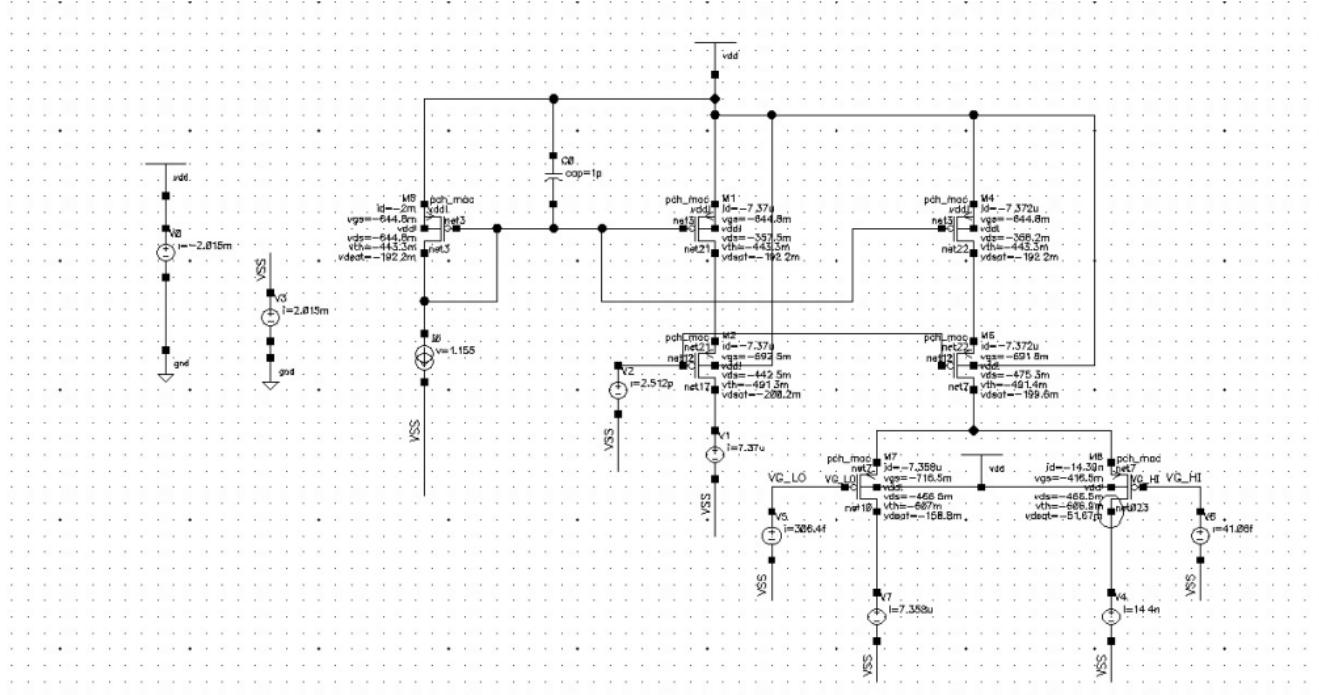
$$I_{incomplete} < \frac{3.6855 \mu}{255} \\ < 14.45 \text{ n.}$$

$$W_{sw} = 758 \text{ n.}$$

$$\approx 760 \text{ n}$$

# Step 6 – Schematic showing DC op

- Place your schematic with DC OP here

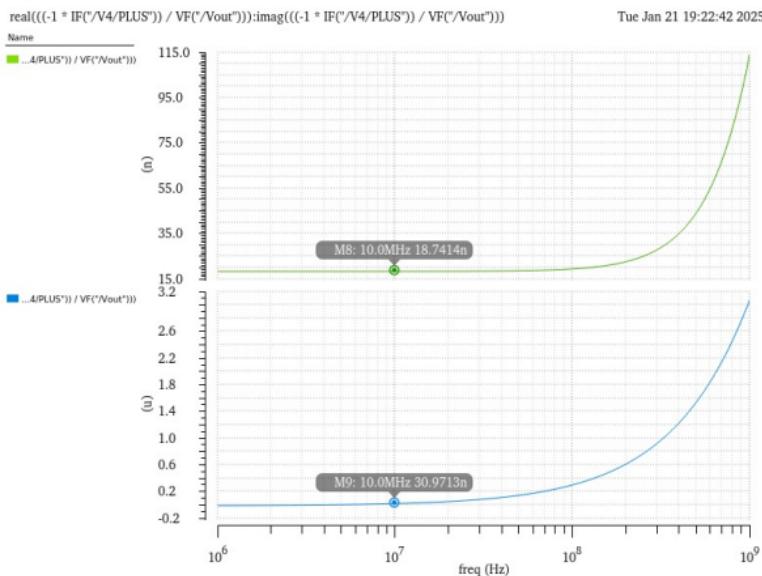


## Step 7

$$\beta = \omega C$$

- Step 7: For the setup in step 6, simulate the output admittance of the LSB unit cell from 1MHz to 1GHz and measure  $r_0$ ,  $\omega_0$ ,  $C_0$  and corner frequency. How do these results compare with the results in part 2, step 10?

Place the plot of real and imaginary part of Admittance



Show calculation, comparison in this box

$$Y_0 = \frac{1}{18.7414n} = 53.35M\Omega > 15.17M\Omega$$

$$C_0 = \frac{\text{Imag}(Y)}{2\pi \cdot f} = \frac{30.9713n}{2\pi \cdot 100m} = 0.493fF < 0.94fF$$

$$f_c = \frac{1}{2\pi Y_0 C_0} = 6.05 \text{ MHz.}$$

$$Y_0_{\text{part2}}.s10 = 15.17M\Omega < 53.35 M\Omega$$

$$C_0_{\text{part2}}.s10 = 0.94fF > 0.493 fF$$

$$f_c_{\text{part2}}.s10 = 11.17 \text{ MHz} > 6.05 \text{ MHz}$$

## Step 8

- Step 8: Calculate the maximum achievable voltage swing on the positive side and negative side at the drain of the differential switch (output of the DAC). Also, calculate the maximum achievable differential voltage swing.

$$V_S = 1.8 \text{ V} - 0.4 - 0.4 = 1 \text{ V}$$

$$V_{LO} = 250 \text{ mV} \quad V_{HI} = 550 \text{ mV} \quad V_G = 400 \text{ mV}$$

$$V_T = 450 \text{ mV}$$

$$V_{OD} = V_{SG(L0)} - V_T$$

$$= (1 - 0.25) - 0.45$$

$$\approx 0.3 \text{ V}$$

$$V_{OD} = V_{SG(HI)} - V_T$$

$$= (1 - 0.55) - 0.45$$

$$= 0.$$

$$V_{D(L0)} = 1 - 0.3 = 0.7 \text{ V} = V_{out\_max}$$

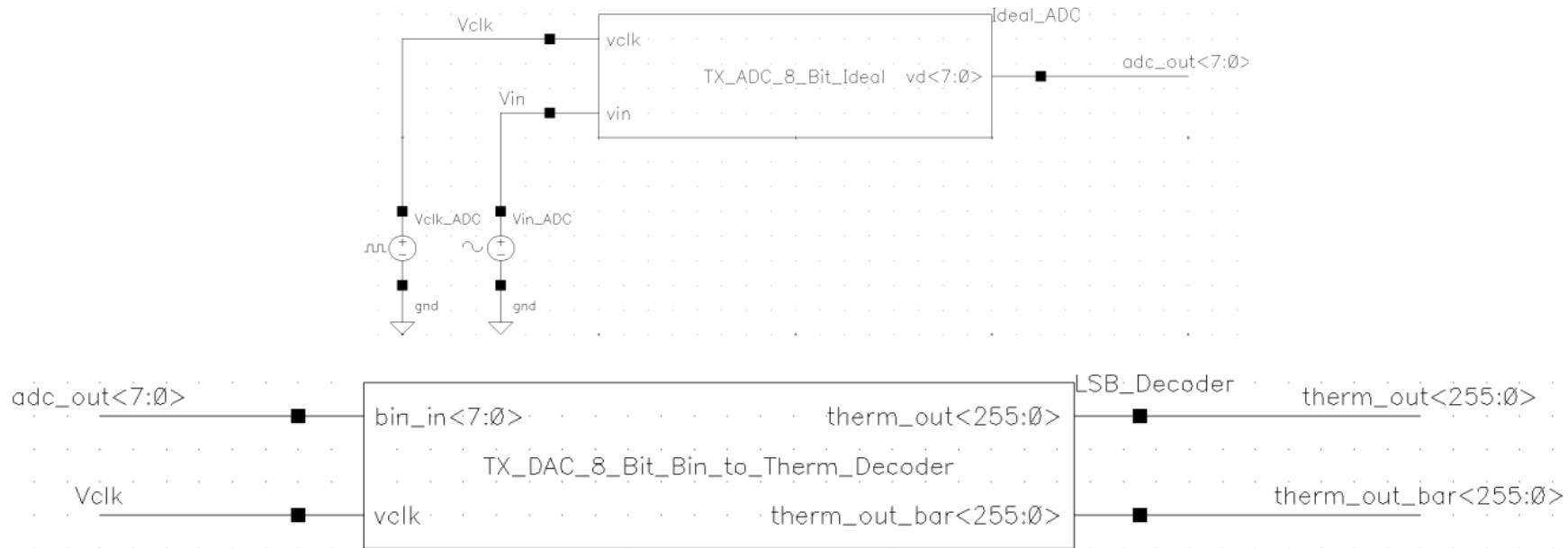
$$V_{out\_min} = 0 \text{ V}$$

$$V_{out\_sw} = \frac{V_{out\_max} - V_{out\_min}}{2} = 0.35 \text{ V.}$$

## **Part 4: Simulation of the Differential Switch Driver [20 points]**

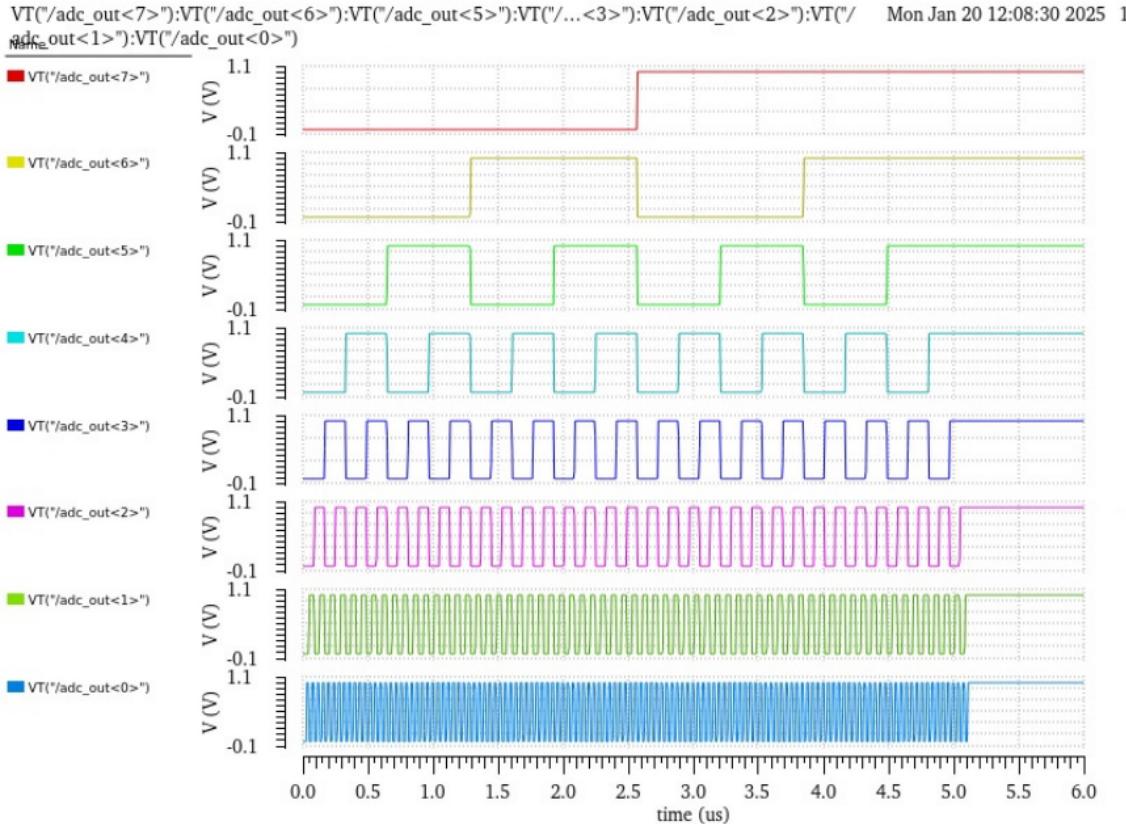
## Part 4: Simulation of the Differential Switch Driver [20 points]

- Run a transient simulation for 1us using the test bench for the switch driver (see below):
  - Signal (VPWL): 0V – 1V in 5.12us
  - Clock (square wave): 100MHz (frequency) & 1V (amplitude)



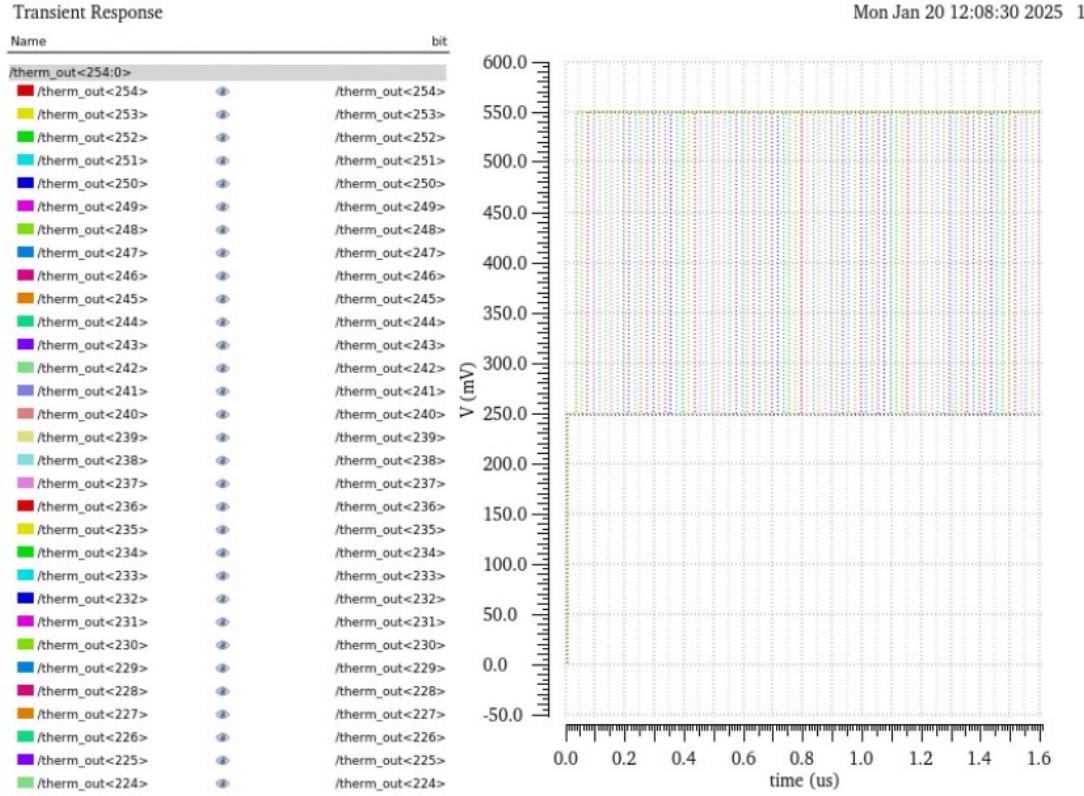
# Step 1

- Plot the time-domain waveforms for the binary output data.



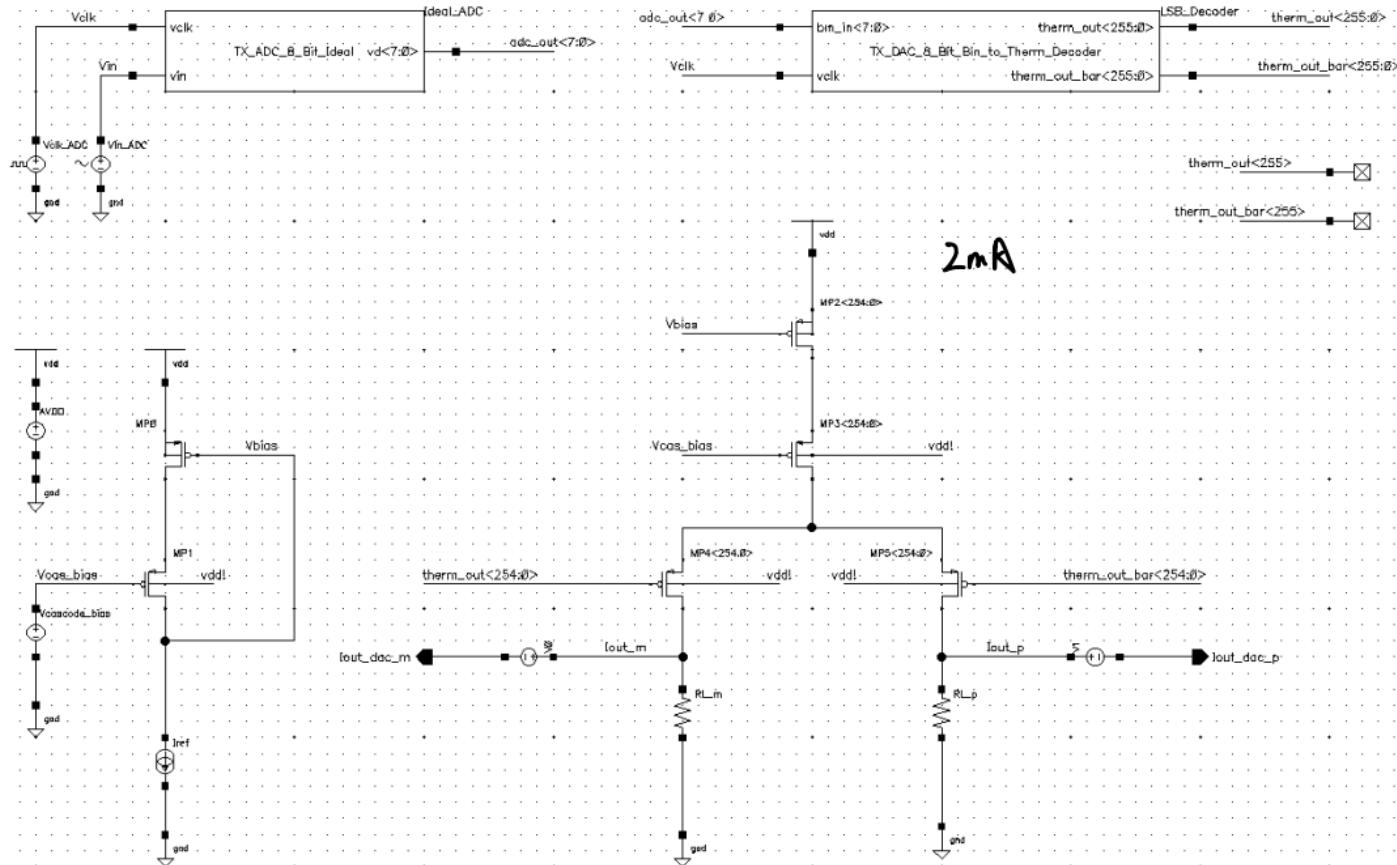
# Step 2

- Step 2: Plot the time-domain waveforms for the thermometer output data.



## **Part 5: Design and Simulation Results of the DAC [110 points]**

# Schematics for Part 5



## Step 1

- Step 1: Build the schematics for 8-bit DAC using the unit cell designed in part 3 and switch drivers in part 4 (see next slide). Use a current mirror that has a bias current ( $I_{ref}$ ) equal to the MSB current. Determine the load resistor value to achieve the desired common-mode voltage of ~~500mV~~<sup>300</sup>.

$$I_{ref} = I_{msb} = 1mA$$

$$R_L = \frac{300m}{1m} = 300\Omega$$

$$\frac{I_{ref}}{I_{unit}} = \frac{x}{1}$$

$$\frac{7.8}{1} = \frac{x}{1}$$

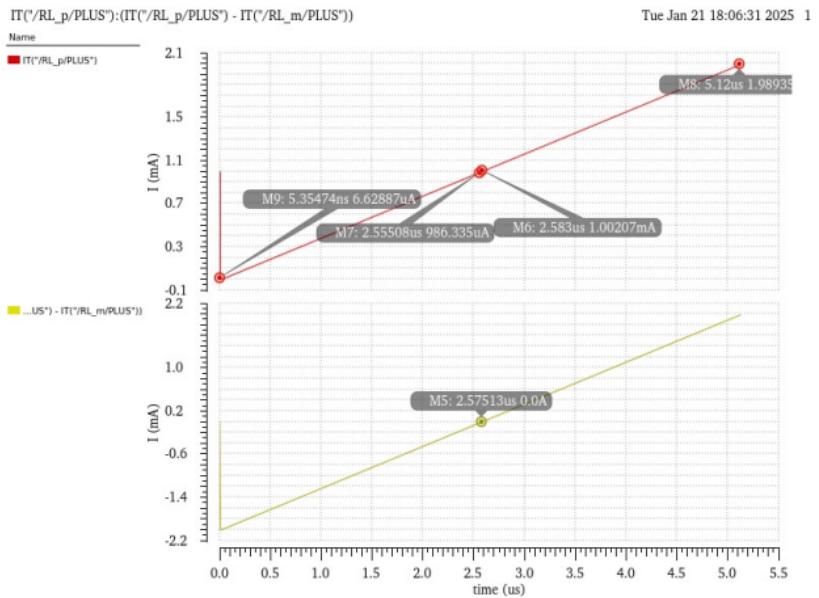
## Step 2

Method 1

Method 2

- Step 2: Simulate the DAC using a ramp (VPWL) of 0V – 1V to generate codes 00000000 to 11111111 and measure DNL and INL for mid-code.

$$\text{Midcode: } \begin{matrix} 0111 & 1111 \end{matrix} \rightarrow \begin{matrix} 0000 & 0000 \end{matrix} \\ = 127 \cdot 7.841 \mu\text{s} \quad = 128 \times 7.841 \mu\text{s}$$



$$\text{DNL} = \frac{\frac{1.062072m - 994.2916u}{1.98935m - 6.62887u}}{255} - 1 \\ = 0.0006 = 0.6 \text{ m LSB}$$

$$\text{INL} = \frac{I_{\text{act}} - I_{\text{ideal}}}{I_{\text{step-ideal}}}$$

$$= \frac{994.2916u - 127 \cdot \frac{1.98935m - 6.62887u}{255}}{1.98935m - 6.62887u}$$

$$= 0.877 \text{ LSB}$$

$$\text{DNL} = \frac{1.062072u - 994.2916u}{7.841 \mu\text{s}} - 1 \\ = -0.0077 \text{ LSB}$$

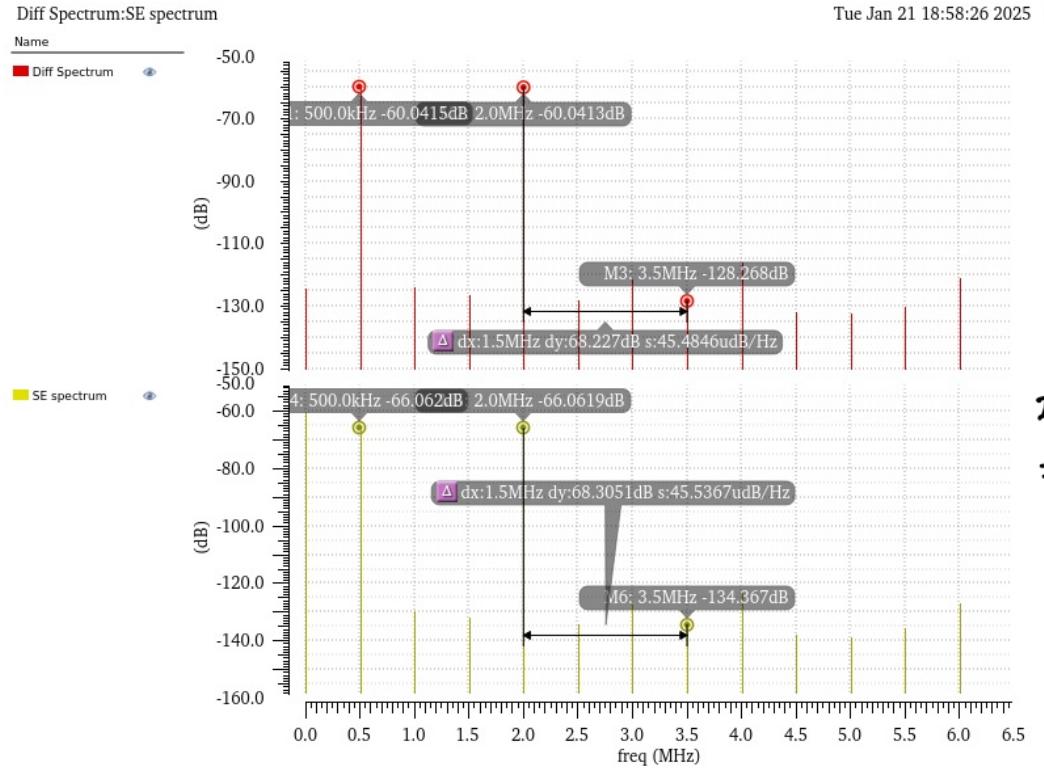
$$\text{INL} = \frac{994.2916u}{7.841 \mu\text{s}} - 127 \cdot 7.841 \mu\text{s} \\ = -0.2 \text{ LSB}$$

## Step 3

- Step 3: Simulate the DAC for a two-tone test using 0.5MHz and 2M sinusoidal tones with an amplitude of 250mV each and common-mode voltage of 500mV (at the input of the Verilog ADC model). Measure the following performance (see remaining slides) 3

# Step 3A: Differential & Single-ended IMR3

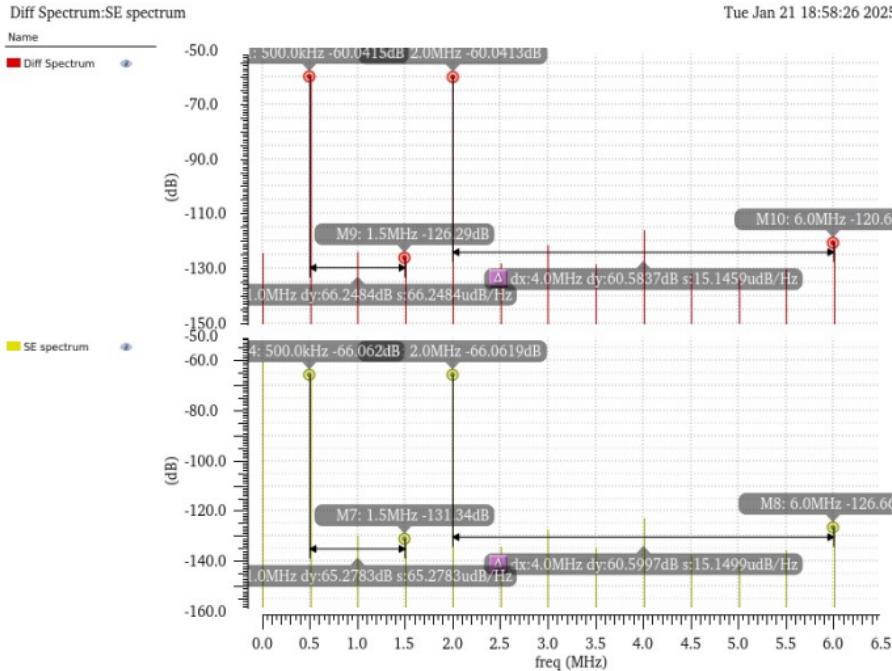
$$IM3.Hi = 2M + 1.5M$$



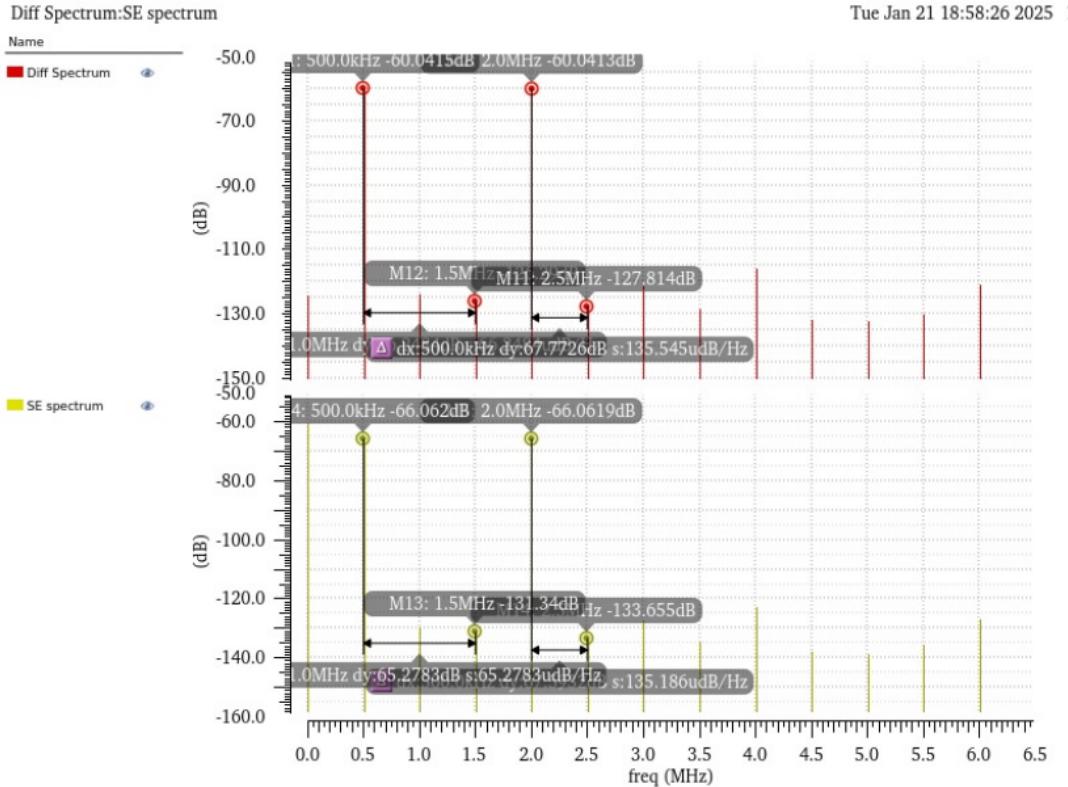
$$\begin{aligned} IMR_3 - \text{diff} \\ = 68.227 \text{ dB} \end{aligned}$$

$$\begin{aligned} IMR_3 - \text{SE} \\ = 68.3051 \text{ dB} \end{aligned}$$

## Step 3B: Differential & Single-ended HDR3



# Step 3C: Differential & Single-ended IMR2



$$0.5 + \Delta M = 2.5M$$

$$t_1 + t_2$$

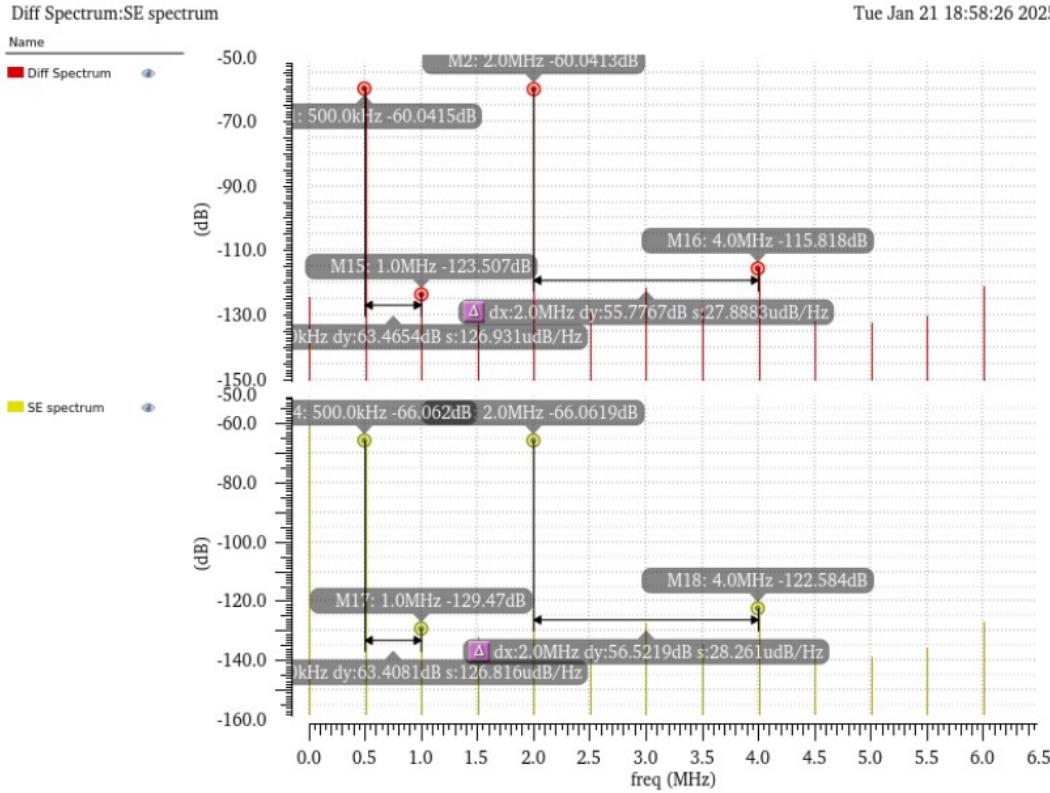
$$t_2 - t_1 = 1.5M.$$

$$\text{IMR}_2 = 67.772 \text{ dB}$$

diff

$$\text{IMR}_{2-\text{SE}} = 67.39 \text{ dB}$$

# Step 3D: Differential & Single-ended HDR2



$$HOR_2 - 2M\_diff = 55.77 \text{ dB}$$

$$HOR_2 - 0.5\_diff = 63.46 \text{ dB}$$

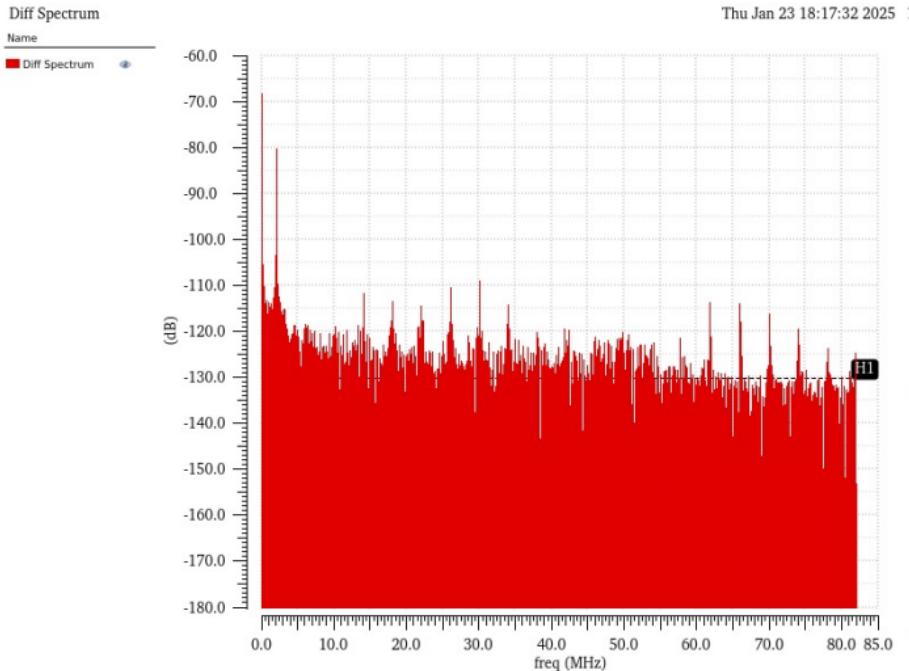
$$HOR_2 - 2M\_SE = 56.52 \text{ dB}$$

$$HOR_2 - 0.5M\_SE = 63.40 \text{ dB}$$

## Step 3E: SNR

- SNR: Use 1/40 of signal frequency as the AM modulation frequency to simulate the quantization noise floor

$$\frac{2M}{40}$$



$$\begin{aligned} \text{SNR} &= -80 - (-130) \\ &= 50 \text{ dB} \end{aligned}$$

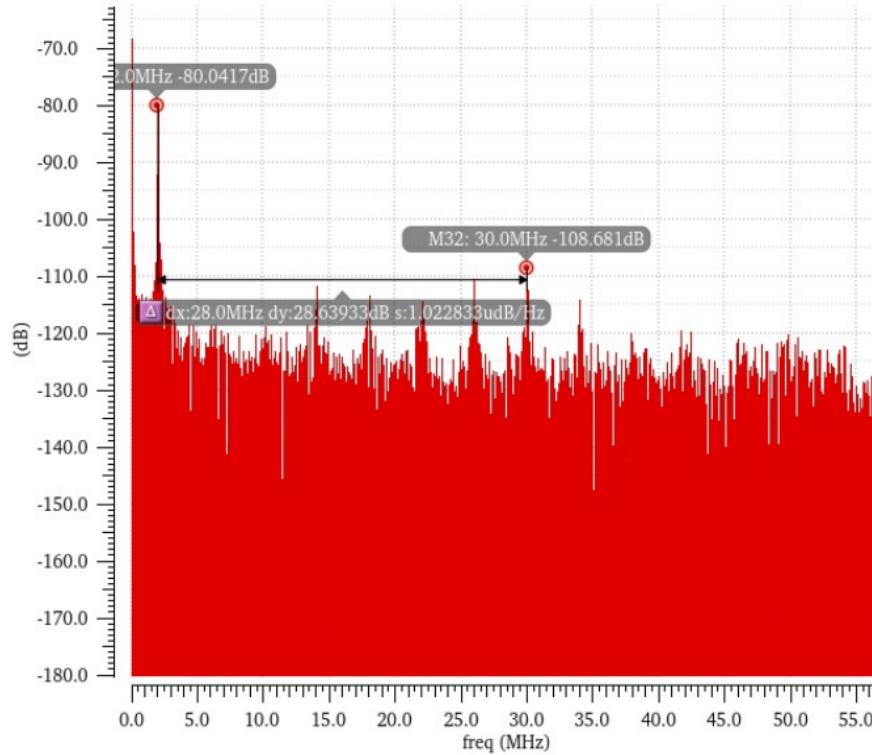
# Step 3F: SFNR

Diff Spectrum

Name

Diff Spectrum

Thu Jan 23 18:17:32 2025 1

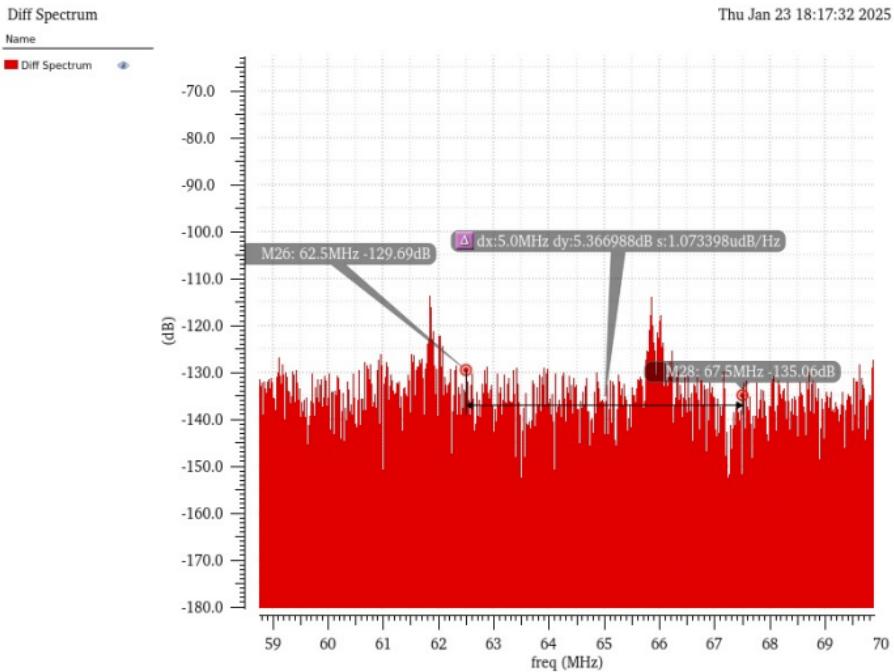


$$SFDR = 28.64 \text{ dB}$$

dith

## Step 3G: Receive Band Noise (RxBN)

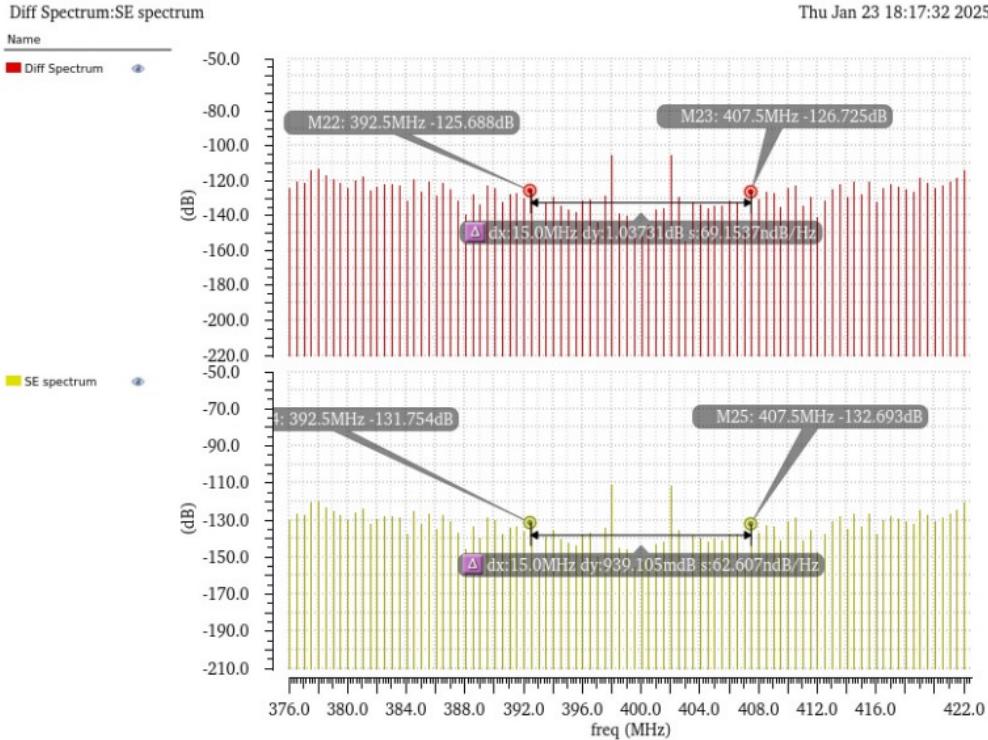
- RxBN at 60MHz offset over 5MHz bandwidth (quantization noise only)



$$132 \text{ dB}/\text{Hz} + 10 \log(5\text{M}) \\ = -65 \text{ dBm}$$

# Step 3H: GNSS Receive Band Noise

- GNSS RxBN at 400MHz over 15MHz bandwidth(quantization noise only)



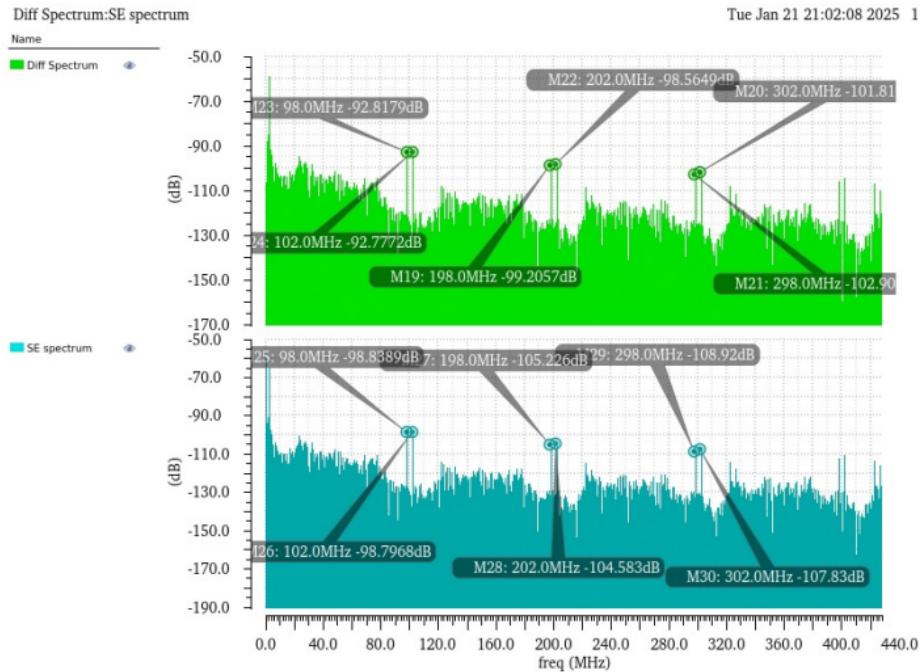
## Step 3I: Images

- Images (1st, 2nd and 3rd) – Differential and Single ended

$$t_{\text{sample}} \cdot f_s = 100M \pm 2M$$

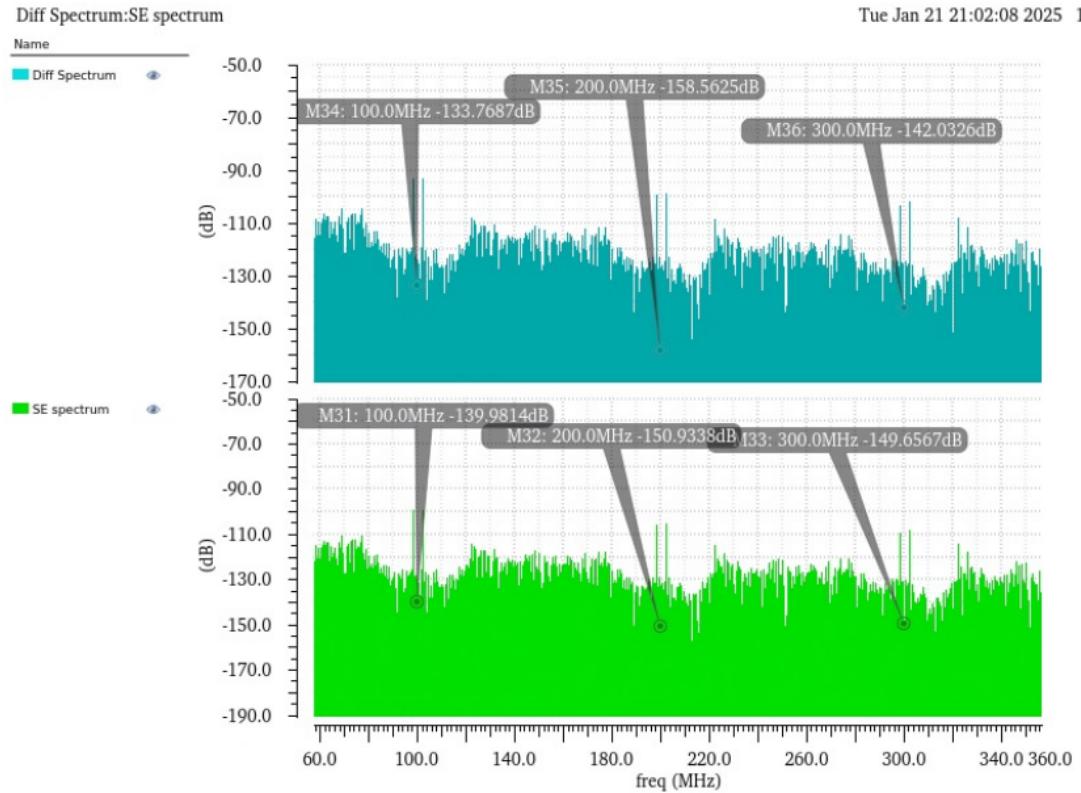
$$2t_{\text{sample}} \cdot f_s = 200M \pm 2M$$

$$3t_{\text{sample}} \cdot f_s = 300M \pm 2M$$



# Step 3J: Clock Feedthrough

- Clock feedthrough (1st, 2nd and 3rd) – Differential and Single-ended



**End**