

ECE265D
Homework #2
Due 11:59pm on Feb. 14th (Friday)

Prasad Gudem
Adjunct Professor, Electrical and Computer Engineering

University of California San Diego
La Jolla, California

Winter 2025

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Updates from version 1

- Part 4, Step 5 clarified.
- Part 5 clarified and typo corrected (there was TIA instead of DAC+BBF).
- **Points division**
 - Part 1, 3rd Chebyshev filter transfer function and design choices – **60 points**
 - Part 2, Simulation of the TIA – **60 points**
 - Part 3, Simulation of the Bi-quad – **80 points**
 - Part 4, Simulation results of the Tx BBF – **90 points**
 - Part 5, Simulation of Tx DAC + BBF – **60 points**

Simulation Conditions & Process Parameters

- Please save all your schematics as you might reuse them in later assignments.
- Simulation Conditions:
 - Temperature = 27C = 300K
 - Process corner = Nominal
 - Supply voltage = 1.8V
- Thin-oxide MOS Process Parameters:
 - Effective mobility of electrons= 500cm²/V.s
 - Effective mobility of holes= 250cm²/V.s
 - Gate oxide capacitance (Cox) = 6fF/ μm^2
 - PMOS Threshold voltage = 450mV
 - NMOS Threshold voltage = 500mV
 - $V_E = 16\text{V}/\mu\text{m}$
 - Lmin = 60nm
- See slides 40 – 41 for schematics

Baseband Filter Design Requirements for Transmitter Application

- Application: LTE B1 (Tx: 1920 – 1980MHz, Rx: 2110 – 2170MHz). GNSS Band: 1575MHz
- Signal Bandwidth = 20MHz at RF (10MHz at Baseband), 16QAM LTE
- DC Current Target < 10mA
- Filter Type: 3rd Order Chebyshev, Active-RC Cascaded Implementation (1-pole + 2-pole Biquad)
- Input Signal = 1mA (SE peak) = 2mA (SE peak-to-peak) = 2mA (DE peak) = 4mA (DE peak-to-peak) to emulate the Tx DAC
- Input Source Impedance = 1M Ohm in parallel with 1pF to emulate the Tx DAC
- Output Signal = 400mV (SE peak) = 800mV (SE peak-to-peak) = 800mV (DE peak) = 1.6V (DE peak-to-peak)
- Output Load Impedance = Noiseless 50 Ohms (differential) to emulate the Tx UpC + Tx DA
- Input Common-Mode DC Voltage = 0.5V
- Output Common-Mode DC Voltage = 0.5V
- In-Band Ripple = 1dB
- Out-of-Band Rejection at Duplex Offset in the Rx Band > 60dB
- Out-of-Band Rejection at GNSS offset > 60dB
- SNDR > 42dB to support 12.5% EVM Tx system budget
- ACLR > 42dB to support 33dB Tx system budget

Part 1, Note 1 – 3: Design of the Tx Baseband Filter Architecture

- Note 1: 10MHz modulated signal is treated as two sinusoidal tones of 0.5mA (single-ended peak) at 5MHz and 9MHz.
- Note 2: Treat IM3 (lower) at 1MHz and IM2 (lower) at 4MHz as contributors to degradation of EVM.
- Note 3: Treat IM3 (upper) at 13MHz and IM2 (upper) at 14MHz as contributors to degradation of ACLR.

Part 1, Step 1: Design of the Tx Baseband Filter Architecture

- Step 1: Assume a passband ripple of 1dB, determine the pole locations of the 3rd Order Chebyshev filter

$$1 \text{ dB ripple} \rightarrow \sqrt{10^{\frac{1}{10}} - 1} \Rightarrow \xi_0 = 0.508$$

$$n=3$$

$$k=1,2,3 \quad k=1 \quad k=2$$
$$w_{nr} : \frac{\pi(2^{k-1})}{2n} = \frac{\pi}{6}, \frac{3\pi}{6}, \frac{5\pi}{6}$$

$$w_{hi} = -\left(\frac{1}{3}\right) \sinh^{-1}\left(\frac{1}{0.508}\right) = -0.476$$

$$b_{nk} = \sin(w_{nr}) \sinh(w_{hi}) = -0.24, -0.494, -0.247$$

$$a_{nk} = \cos(w_{nr}) \cosh(w_{hi}) = 0.966, 0, -0.966$$

$$\frac{s p_{1,2,3}}{w_0} = -0.494, -0.24 + j 0.966, -0.247 - j 0.966$$

Part 1, Step 2: Design of the Tx Baseband Filter Architecture

- Step 2: Express the transfer function of the 3rd order Chebyshev filter as a cascade of 1st order (TIA) and 2nd order (Biquad).

$$\begin{aligned} T(s) &= \frac{1}{\left(1 + \frac{s}{0.494w_0}\right) \cdot \left(1 + \frac{s}{(0.24) + j0.966)w_0}\right) \left(1 + \frac{s}{(0.24) - j0.966)w_0}\right)} \\ &= \frac{1}{\left(1 + \frac{s}{0.494w_0}\right) \left(1 + 2^{0.24} \cdot \left(\frac{s}{0.994w_0}\right) + \left(\frac{s}{0.994w_0}\right)^2\right)} \\ &= \frac{1}{\left(1 + \frac{s}{0.494w_0}\right) \left(1 + \frac{s}{2.01w_0} + \left(\frac{s}{0.994w_0}\right)^2\right)} \end{aligned}$$

Part 1, Step 3: Design of the Tx Baseband Filter Architecture

- Step 3: Determine the real and complex pole frequencies of the TIA and Biquad respectively.

$$f_0 = 10 \text{ MHz}$$

$$f_{p1} = 0.494 \cdot 10 \text{ MHz} = 4.94 \text{ MHz}$$

$$f_{\text{complex}} = 0.994 \cdot 10 \text{ MHz} = 9.94 \text{ MHz}$$

$$\left(\frac{1}{1 + \frac{5 \text{ M}}{4.94 \text{ M}}} + \frac{1}{1 + \frac{9 \text{ M}}{9.94 \text{ M}}} \right)$$

Part 1, Step 4: Design of the Tx Baseband Filter Architecture

- Step 4: Calculate the values of the feedback resistor and the capacitor (R_{f1} and C_{f1}) in the TIA to ensure maximum swing of 500mV (SE peak) at the output of the TIA (for the best noise performance).

$$V_{out} = R_{f1} \cdot (0.5mA @ 5M + 0.5mA @ 9M)$$

$$0.5 = \left(\frac{1}{\left(1 + \frac{5M}{4.94M} \right)} + \frac{1}{\left(1 + \frac{9M}{4.94M} \right)} \right) \cdot 0.5mA \cdot R_{f1} \Rightarrow R_{f1} = 1175 \Omega$$

$$\omega_{p1} = \frac{1}{R_{f1} C_{f1}} \Rightarrow C_{f1} = \frac{1}{4.94M \cdot 1175 \Omega \cdot 2\pi}$$

$$\therefore 27.43 pF$$

Part 1, Step 5: Design of the Tx Baseband Filter Architecture

- Step 5: Input resistor (R_{in}) of the Biquad is 10kOhms, determine the component values (R_1 , R_2 , R_f , C_1 and C_2) of the Biquad under the following constraints:

1. Achieve pole frequencies calculated in step 3

2. Voltage swing at the output of the first opamp is maximized (500mV)

3. Voltage swing at the output of the second opamp is maximized (500mV)

4. $C_1 = C_2$

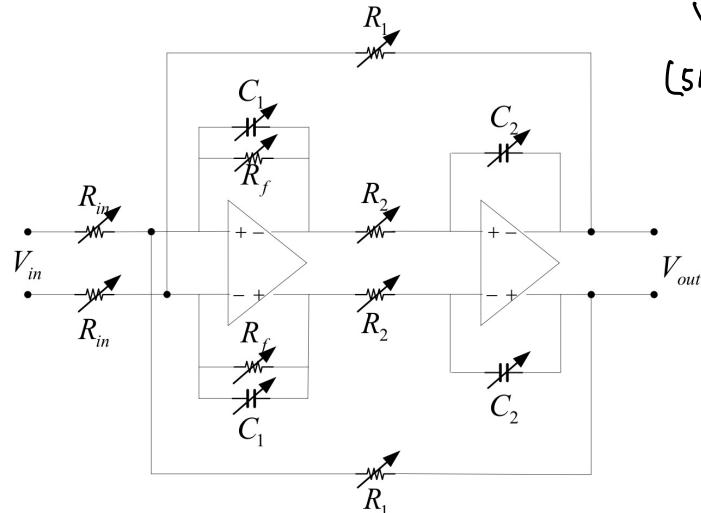
$$\frac{1}{(1 + \frac{s}{0.494\omega_0})(1 + \frac{s}{2.01\omega_0} + (\frac{s}{0.994\omega_0})^2)}$$

$$Q = 2.01$$

$$V_{out} s C_2 = -\frac{V_{in}}{R_2}$$

$$\frac{V_{out}}{V_{in}} = \frac{-1}{s R_2 C_2}$$

$$(5M + 9M) R_2 C_2 = -1$$



$$\frac{V_{out}}{V_{in}} = A_v \left[\frac{1}{1 + \frac{5M}{2.01\omega_0} + (\frac{5M}{0.994\omega_0})^2} + \frac{1}{1 + \frac{9M}{2.01\omega_0} + (\frac{9M}{0.994\omega_0})^2} \right]$$

$$1 = 1.08 A_v$$

$$A_v = 0.925$$

Part 1, Step 5: Design of the Tx Baseband Filter Architecture

- Step 5: Input resistor (R_{in}) of the Biquad is 10kOhms, determine the component values (R_1 , R_2 , R_f , C_1 and C_2) of the Biquad under the following constraints:

1. Achieve pole frequencies calculated in step 3

2. Voltage swing at the output of the first opamp is maximized (500mV)

3. Voltage swing at the output of the second opamp is maximized (500mV)

4. $C_1 = C_2$

$$A_V = 0.925 = \frac{R_1}{R_{in}} \Rightarrow R_1 = 9.25 \text{ k}\Omega$$

$$\omega_0 = \frac{1}{\sqrt{R_1 R_2 \cdot C_1^2}} \Rightarrow 2\pi f_2 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \Rightarrow C_1 = 2.43 \text{ pF}$$

$$\frac{1}{Q\omega_0} = \left(\frac{R_1}{R_f}\right) (R_2 C_2) \Rightarrow \frac{\omega_0}{Q} = \frac{1}{R_f C_1}$$

$$\frac{V_{in}}{V_{out}} = -R_2 \cdot C_2 \cdot s$$

$$= -R_2 \cdot C_2 \cdot 2\pi \cdot (5 \text{ MHz})$$

$$R_2 C_2 = 1.136 \cdot 10^{-8} = \frac{1}{2\pi (14 \text{ MHz})}$$

$$Q = 2.01$$

Summary

$$R_1 = 9.25 \text{ k}\Omega$$

$$R_2 = 4.66 \text{ k}\Omega$$

$$R_f = 9.37 \text{ k}\Omega$$

$$C_1 = C_2 = 2.43 \text{ pF}$$

$$R_f = \frac{1}{\frac{\omega_0}{Q} C_1}$$

$$= 9.37 \text{ k}\Omega$$

Part 1, Step 6: Design of the Tx Baseband Filter Architecture

- Step 6: Determine the gain-bandwidth product (GBW or fT) of the opamp to ensure that the passband ripple is not degraded by more than 0.5dB (Q-enhancement due to finite fT of the opamp).

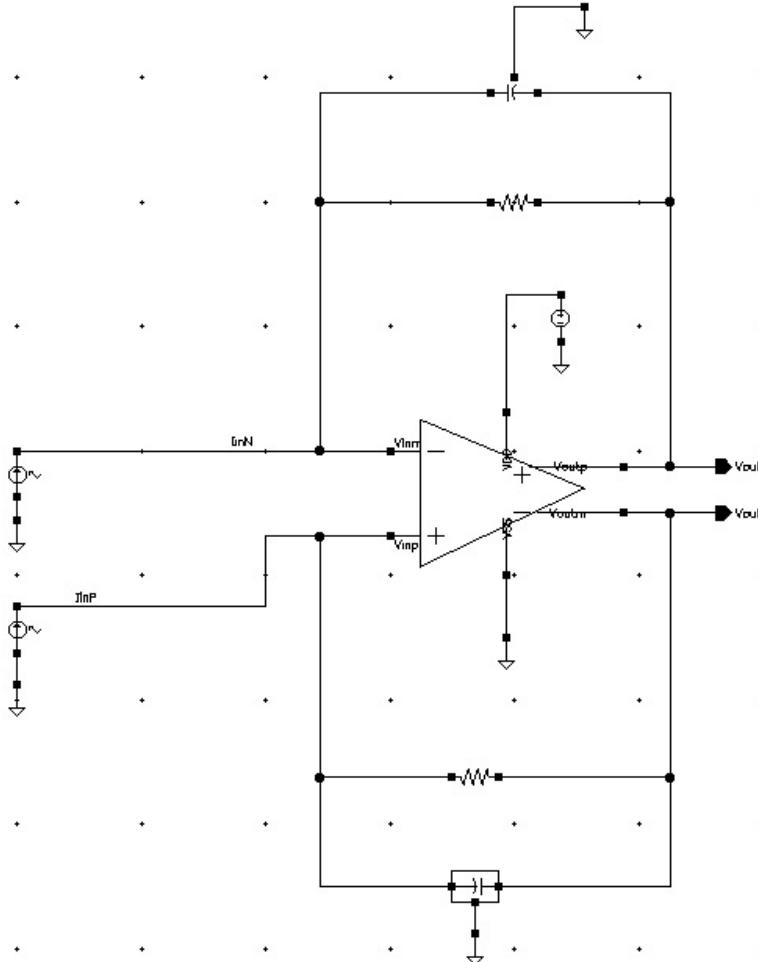
$$\cdot \left(\frac{2Q \cdot f_0}{f_T} \right) = 10^{\frac{0.5}{20}} - 1 \Rightarrow f_T \approx 678 \text{ MHz}$$

$$f_0 = 10 \text{ MHz}$$

$$Q = 2.01$$

Part 2, Step 1: Design and Simulation Results of the TIA

- Step 1: Build the schematics of the TIA using the opamp design in library and drive with 1mA peak ac current source to emulate the Tx DAC at the input of the TIA. Scale up the opamp by 6x. Provide screen shots of the schematics.



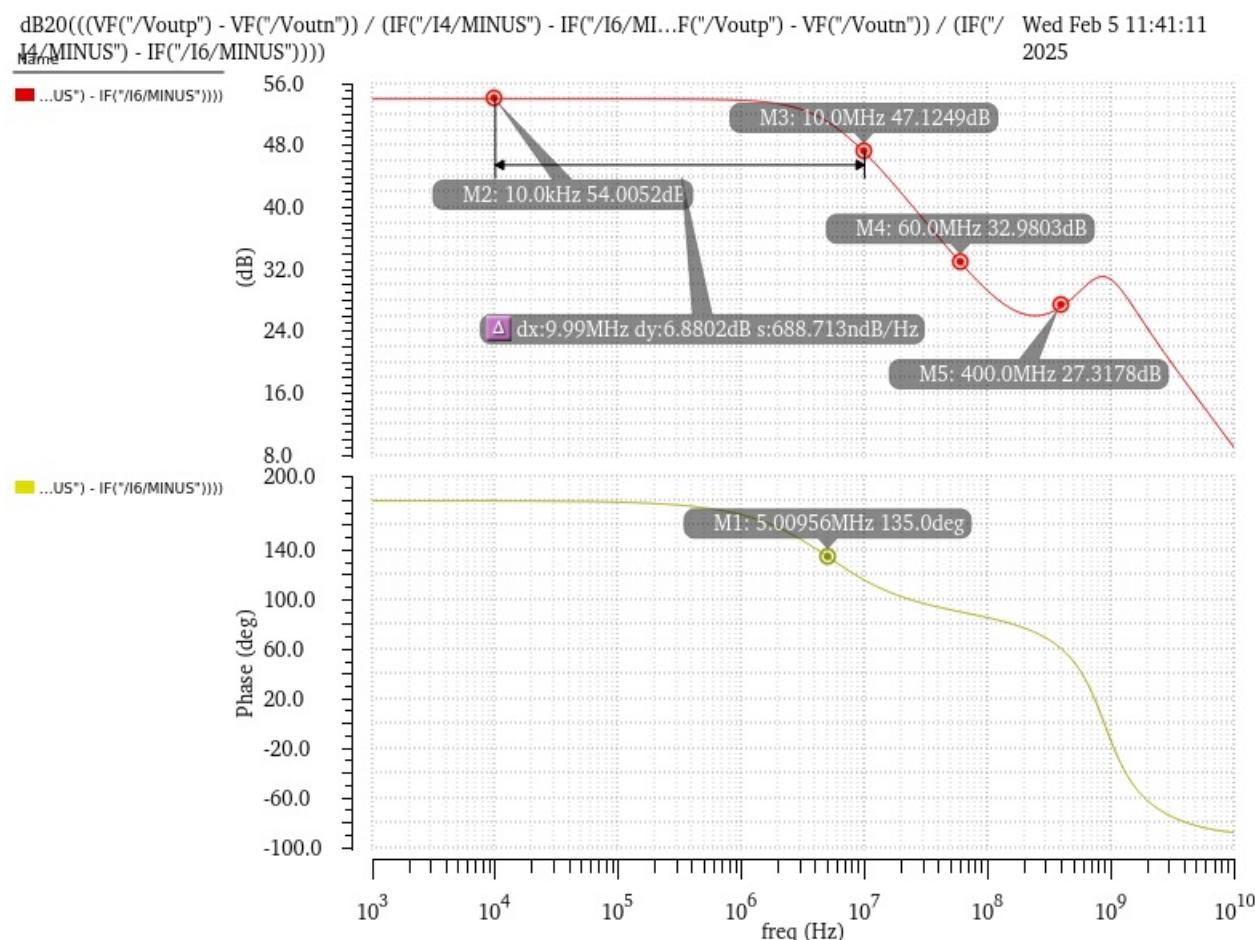
Revised

$$R_f = 1175 \Omega$$

$$C_f = 27.43 \text{ pF}$$

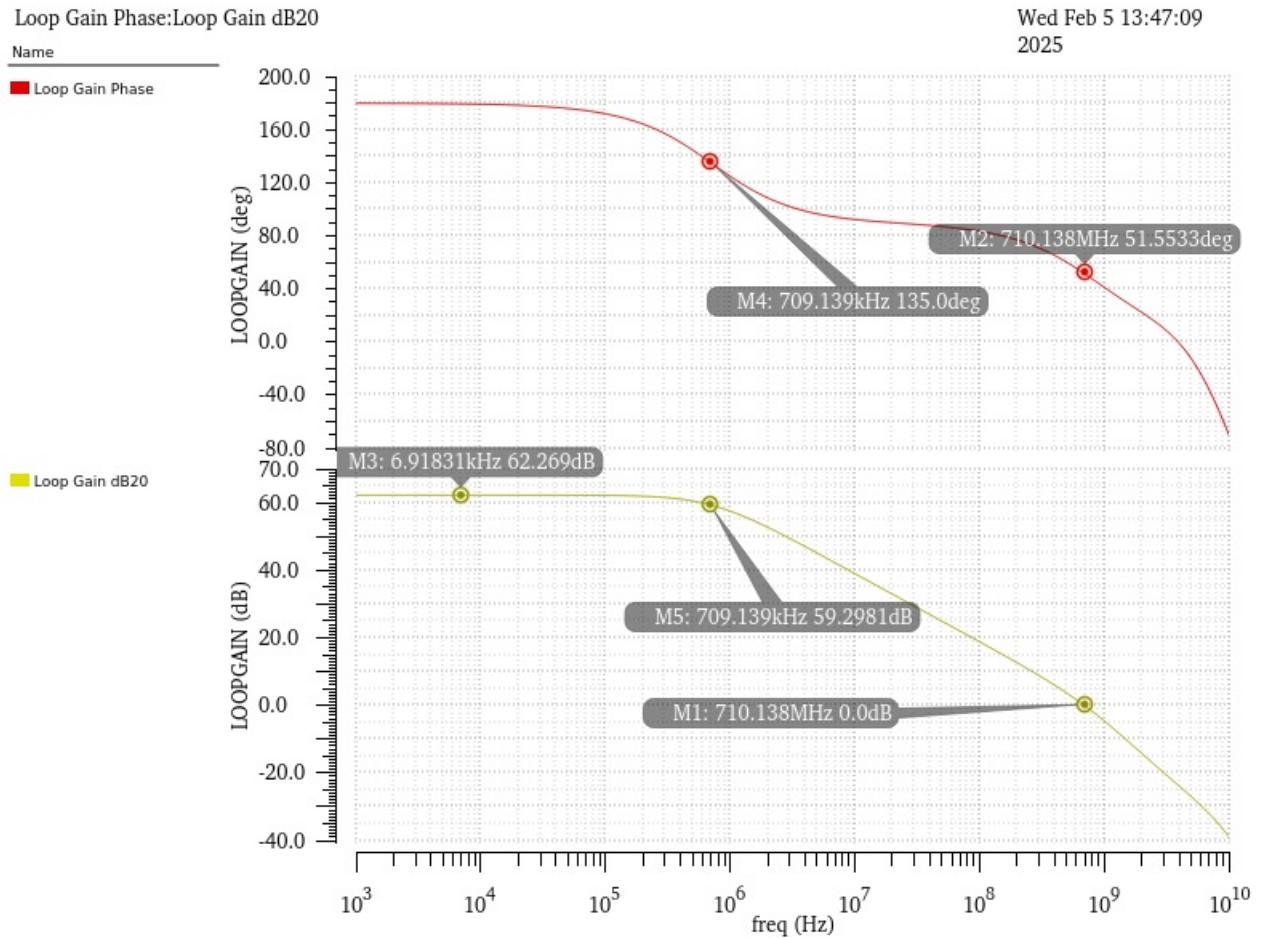
Part 2, Step 2: Design and Simulation Results of the TIA

- Step 2: Simulate the schematics in step 1 and plot the DM gain of the TIA (in Ohms) from 1kHz to 10GHz. Plot and measure the gain variation in the passband (10kHz – 10MHz) and attenuation in the Receive band (60MHz Offset) and GNSS bands (400MHz offset). Also, measure the pole frequency of the TIA.



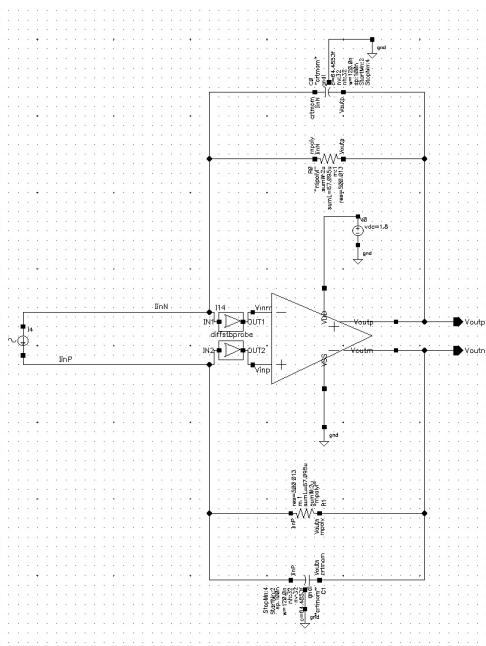
Part 2, Step 3: Design and Simulation Results of the TIA

- Step 3: Simulate the DM loop gain of the TIA, measure and plot the phase margin. Comment on the results for the loop gain and whether the resulting graphs are expected or not.



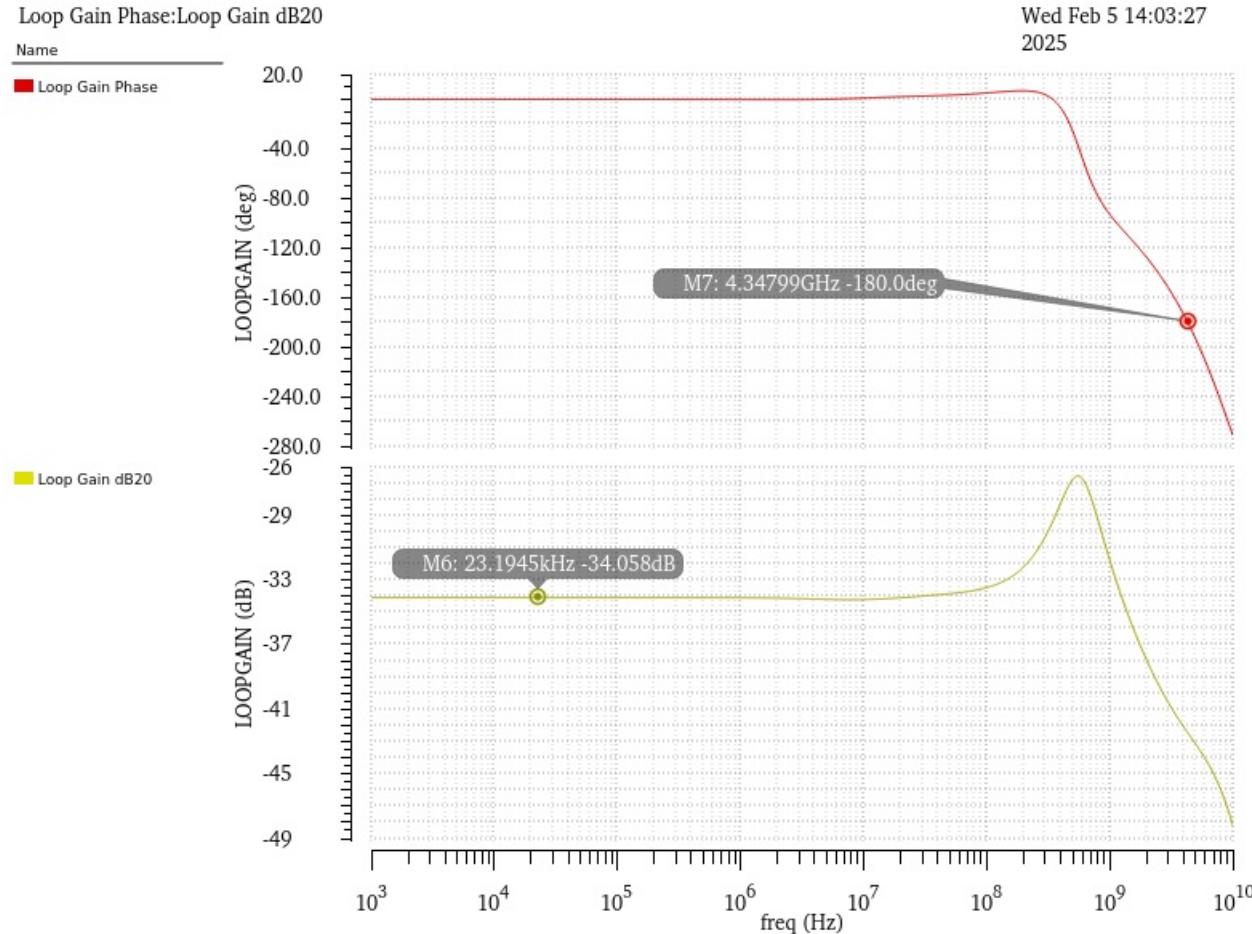
Expected
as closed loop gain < DM loop gain

And TIA itself is
stable with 51° phase margin

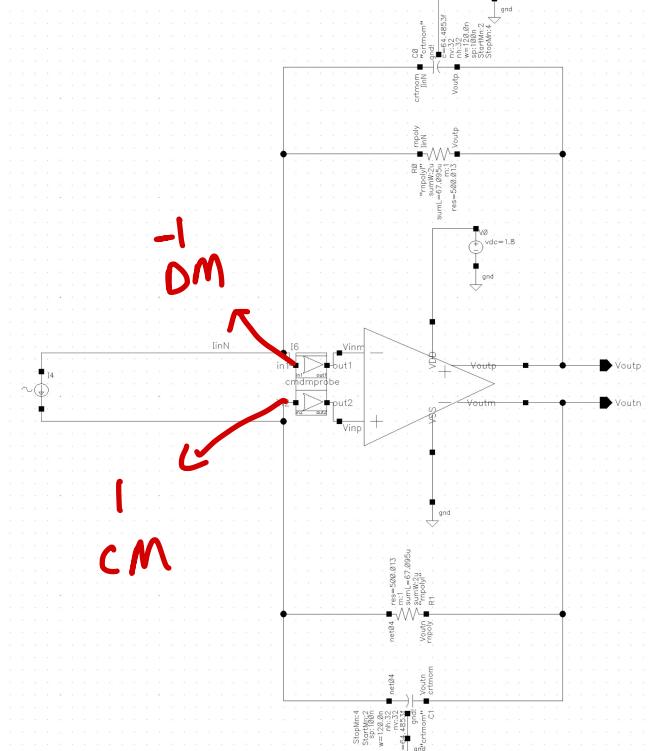


Part 2, Step 4: Design and Simulation Results of the TIA

- Step 4: Simulate the CM loop gain of the TIA, measure and plot the phase margin.



phase margin is not defined
in CM



Part 2, Step 5: Design and Simulation Results of the TIA

- Step 5: Assuming that the opamp doesn't contribute noise, calculate the input referred noise current of the TIA.

$$R_f = 1174 \text{ ohm}$$

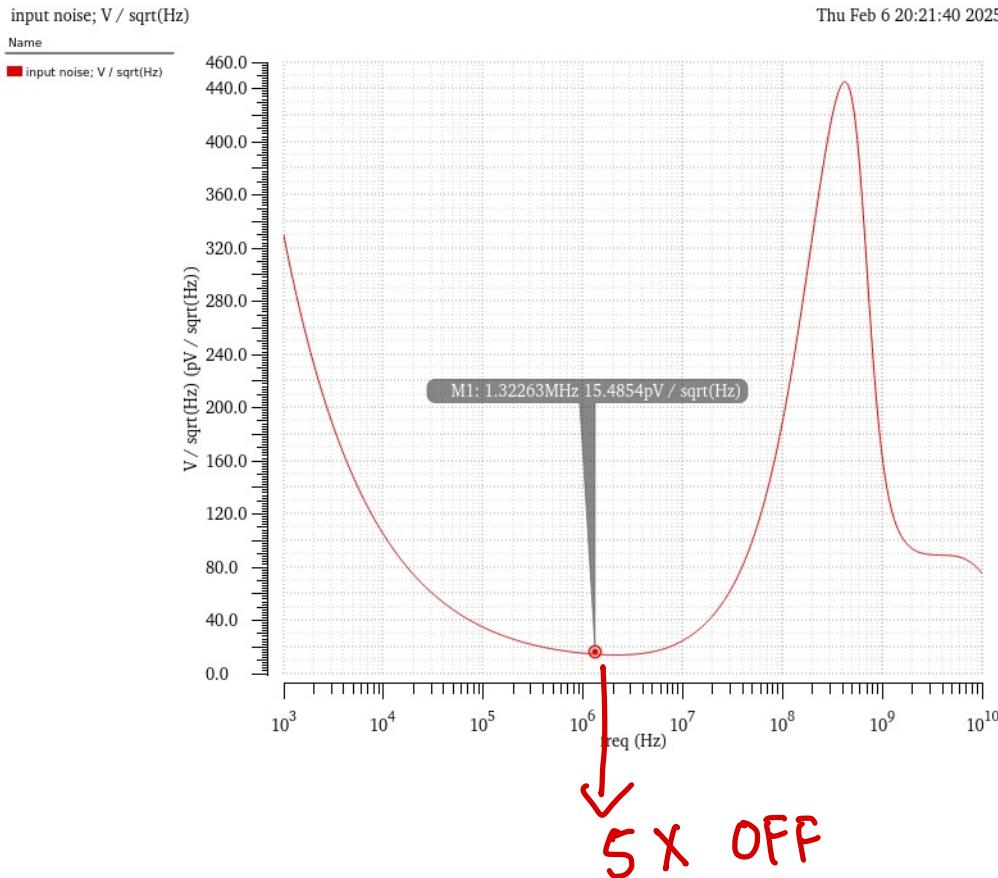
$$T = 300k \quad k = 1.38 \cdot 10^{-23}$$

$$I_{\text{tx-noise}} = \sqrt{\frac{4kT}{R_f}} = 3.755 \text{ pA}/\sqrt{\text{Hz}}$$

$\overline{\frac{V_n}{R}}$

Part 2, Step 6: Design and Simulation Results of the TIA

- Step 6: Simulate the input referred noise current of the TIA and print the noise summary table for the top 20 noise contributors and compare with calculation in step 5.



Device	Param	Noise Contribution	% Of Total
The above noise summary info is for noise data			
Device	Param	Noise Contribution	% Of Total
R3.r1	thermal_noise	4.06579e-11	0.03
R2.r1	thermal_noise	3.72821e-11	0.02
I0\<5\>.R3_20_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_19_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_18_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_17_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_16_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_15_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_14_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_13_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_12_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_11_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_10_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_9_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_8_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_7_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_6_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_5_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_4_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
I0\<5\>.R3_3_.dmy0.rmain	thermal_noise	6.34035e-12	0.00
Integrated Noise Summary (in V^2) Sorted By Noise Contributors			
Total Summarized Noise = 1.58522e-07			
Total Input Referred Noise = 1.77903e-10			
The above noise summary info is for noise data			

Sweep Range

Start-Stop Start Stop

Center-Span

Sweep Type

Points Per Decade

Number of Steps

Add Specific Points

Add Points By File

Output Noise

voltage

Positive Output Node Negative Output Node

Input Noise

current

Input Current Source

Noise Separation

Separate noise into source and gain

Enabled

Options...

Part 3, Step 1: Design and Simulation Results of the Biquad

- Step 1: Build the schematics of the Biquad using the opamp design in part 1-7. Drive the Biquad with 500mV peak ac voltage source to emulate the TIA in front. Provide screen shots of the schematics. Scale up the opamp by 3x.

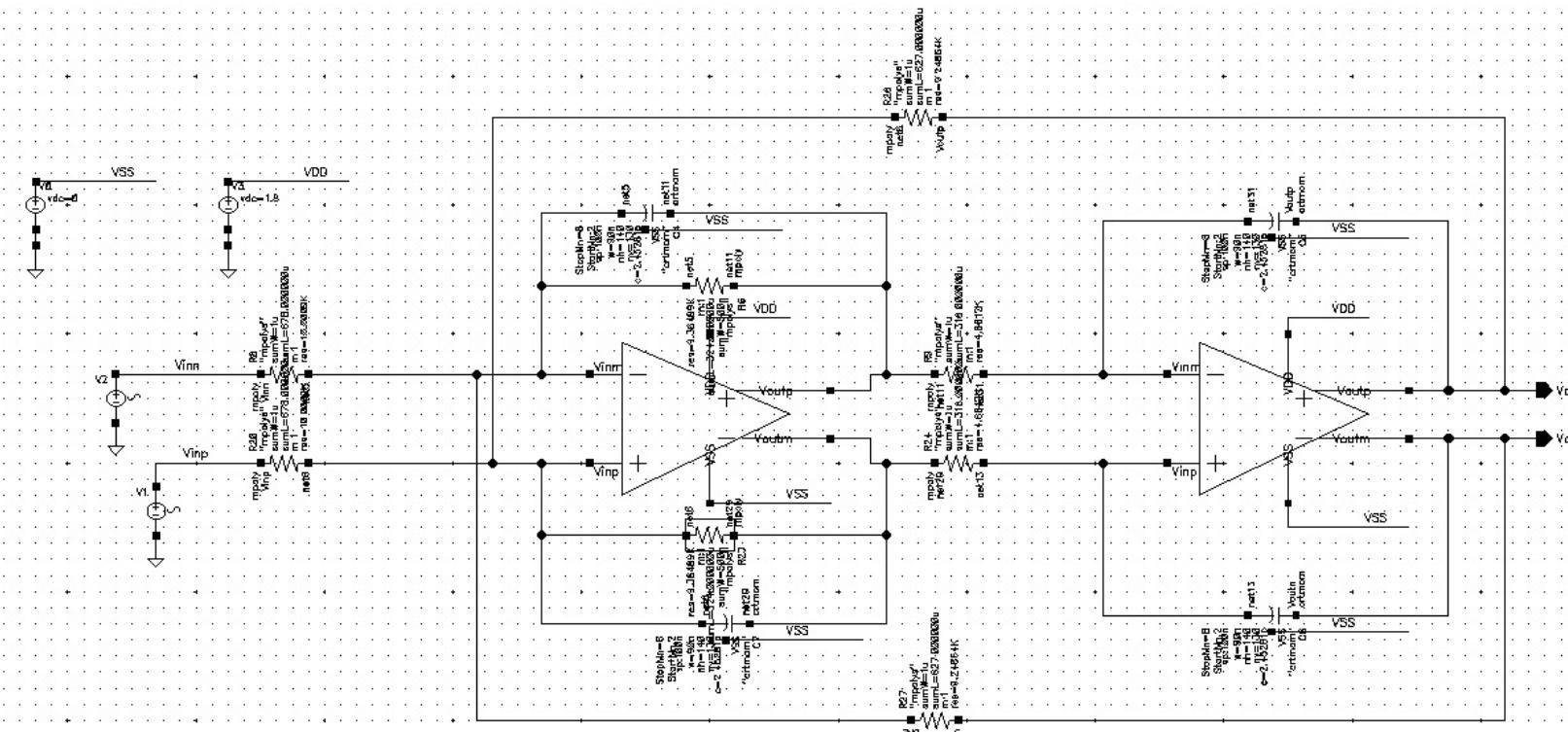
Summary

$$R_1 = 9.25 \text{ k}$$

$$R_2 = 4.66 \text{ k}$$

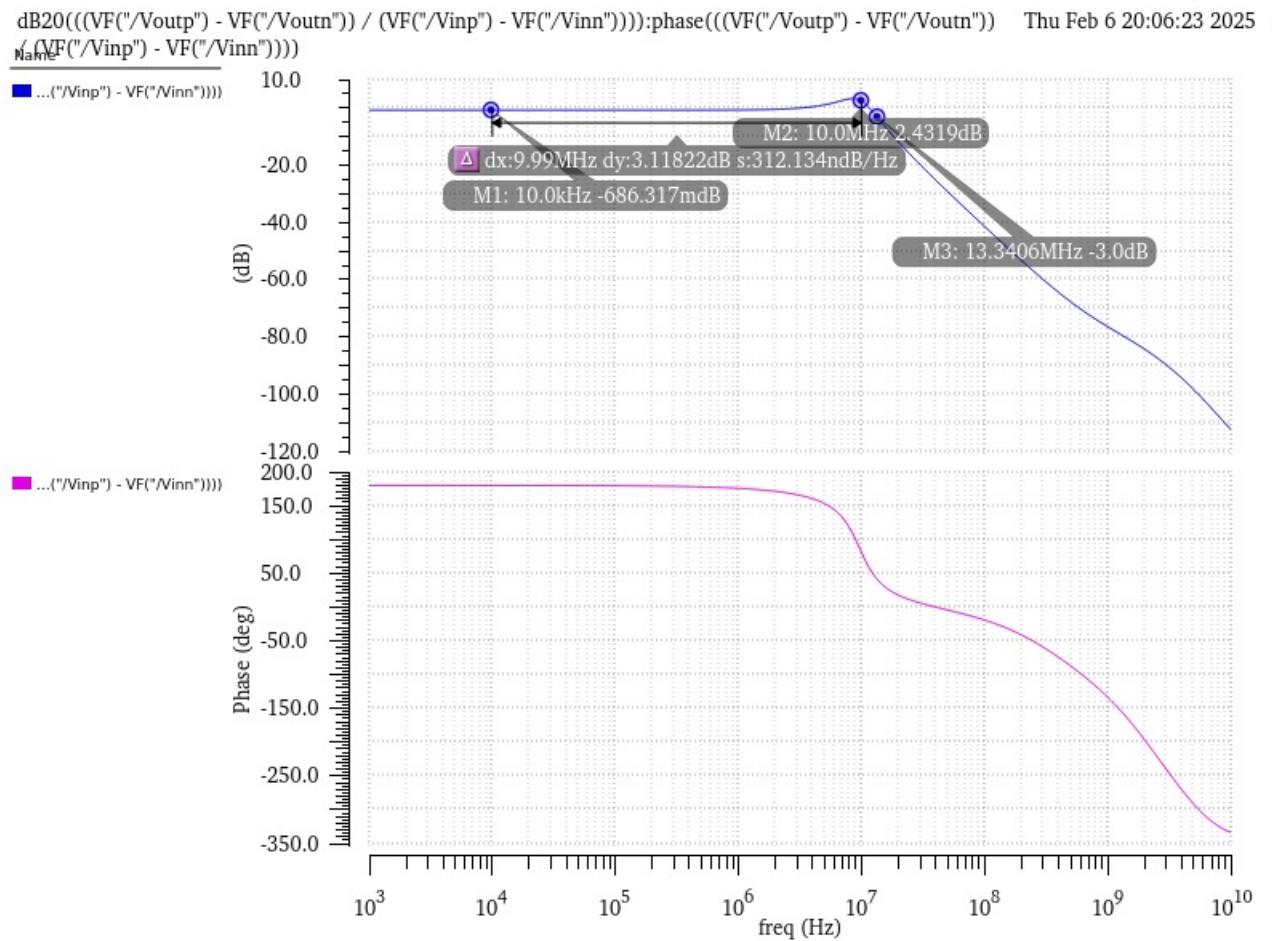
$$R_f = 9.37 \text{ k } \Omega$$

$$C_1 = C_2 = 2.43 \text{ pF}$$



Part 3, Step 2: Design and Simulation Results of the Biquad

- Step 2: Simulate the schematics in step 1 and plot the DM voltage gain of the Biquad from 1kHz to 10GHz. Measure the gain variation (ripple) in the passband (10kHz – 10MHz). Measure the complex pole frequency.

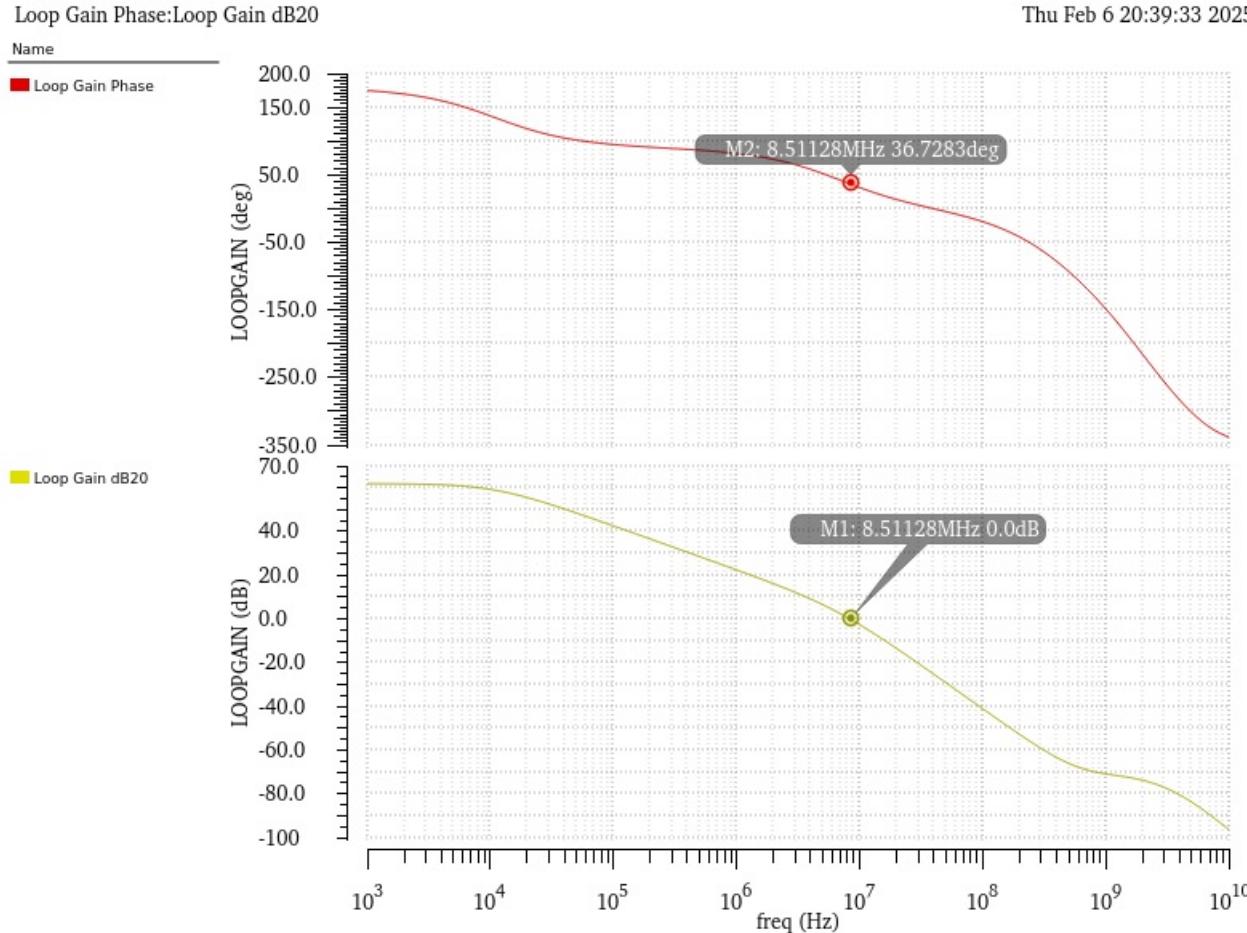


Gain Variation $\approx 3\text{dB}$
Complex Pole @ 13MHz

Part 3, Step 3: Design and Simulation Results of the Biquad

- Step 3: Simulate the DM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin and compare the loop gain to the hand calculated one.

L1



36° Phase Margin

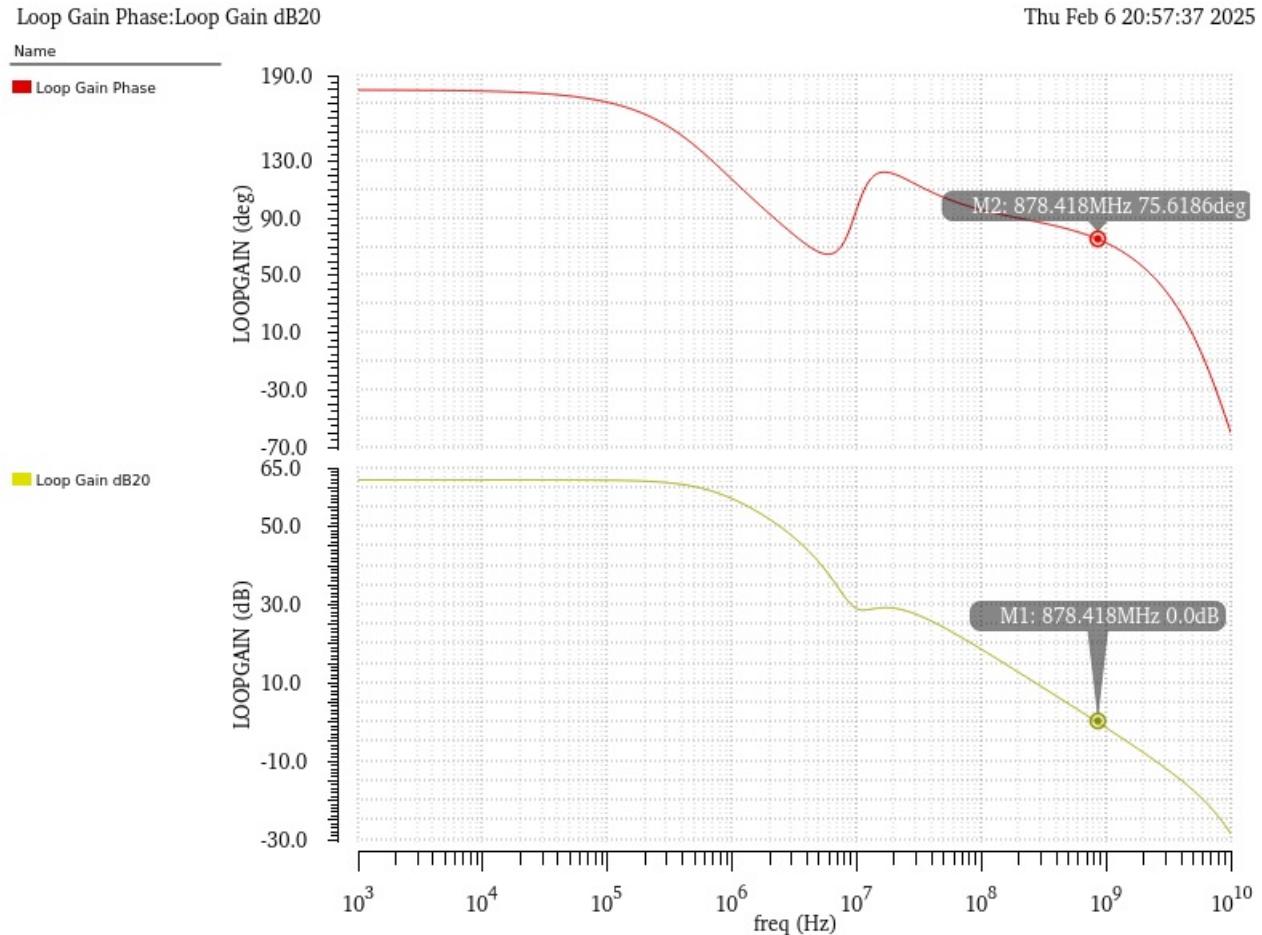
Loop gain Hand calc

$$= \frac{1}{\frac{s}{w_0 Q} \left(1 + \frac{s}{w_0 / Q} \right)}$$
$$= \frac{R_f}{R_2 \cdot R_1} \frac{1}{s C_2 \left(1 + s R_f C_1 \right)}$$

Part 3, Step 3: Design and Simulation Results of the Biquad

- Step 3: Simulate the DM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin and compare the loop gain to the hand calculated one.

L2



75° Phase Margin

Loop gain

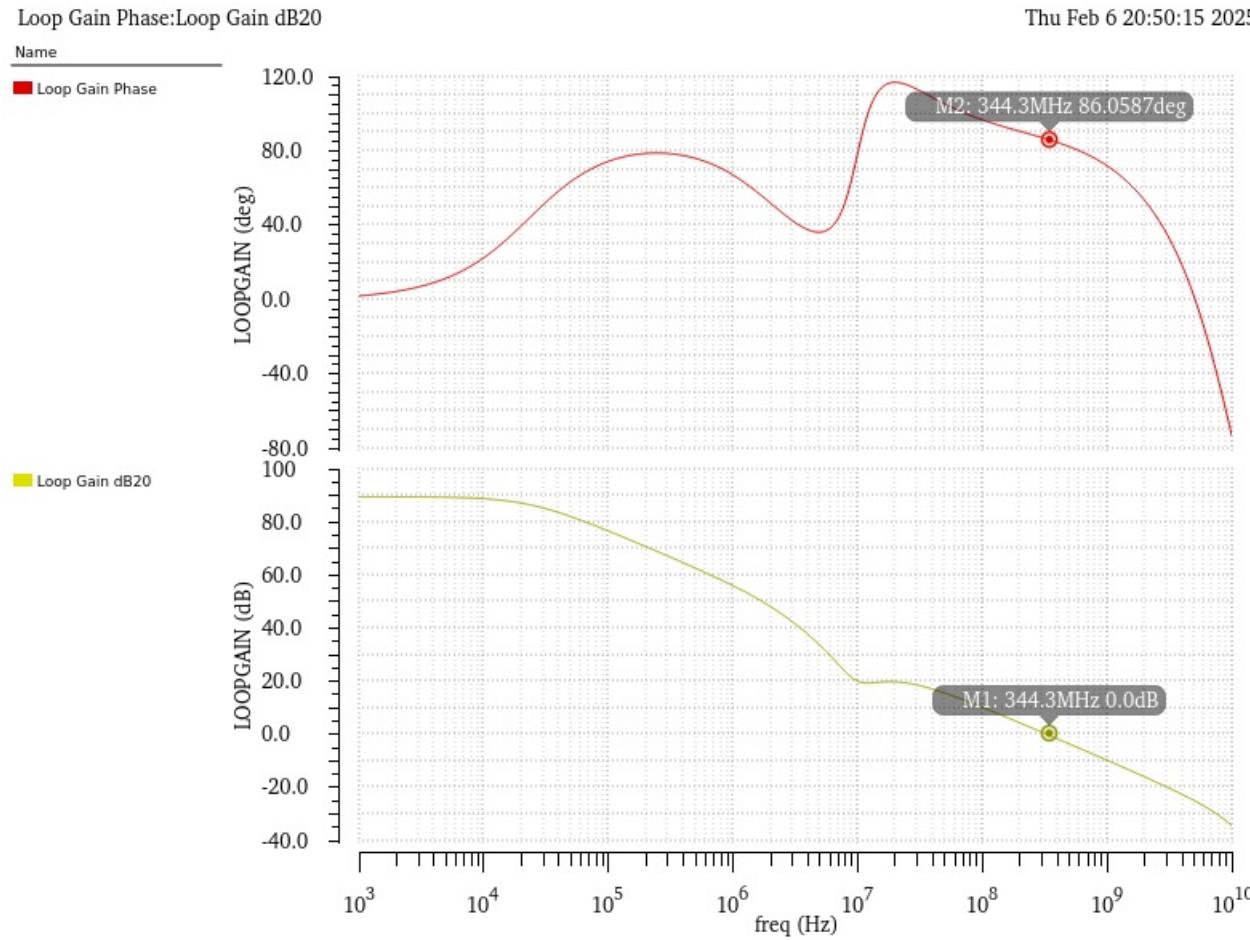
$$= - \left(\frac{R_{in} || R_1 || R_f}{R_1} \right) \left(\frac{W_t}{s} \right) \left(\frac{1}{R_2 C_2 s} \right)$$

$$\left[1 + \frac{s}{\omega_n} + \left(\frac{s}{\omega_n} \right)^2 \right]$$

Part 3, Step 3: Design and Simulation Results of the Biquad

- Step 3: Simulate the DM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin and compare the loop gain to the hand calculated one.

L3



86° Phase Margin.

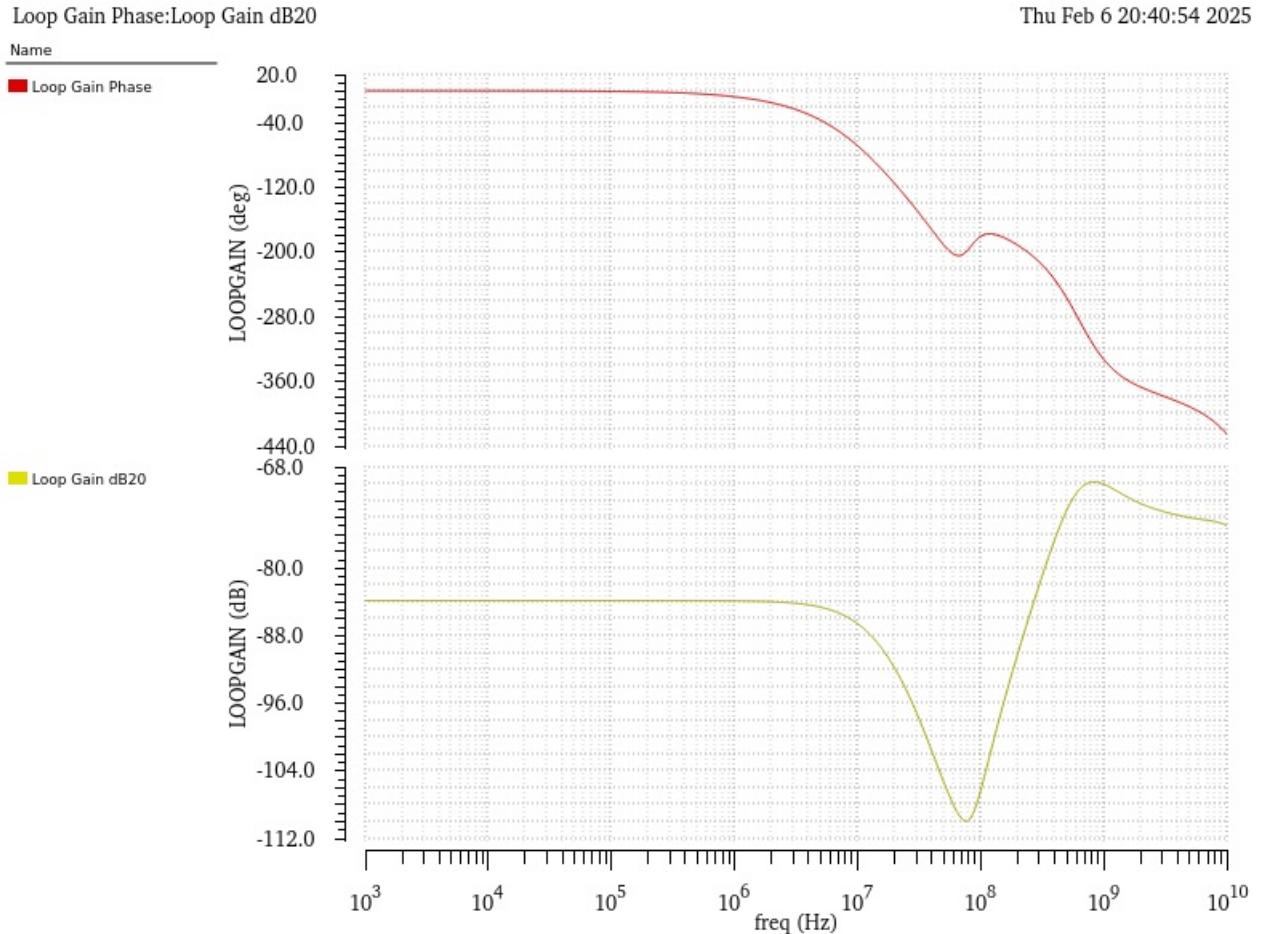
Loop gain Hand calc

$$= \frac{\frac{R_f}{R_i} \left[1 + \frac{s}{\omega_{n0}} + \left(\frac{s}{\omega_0} \right)^2 \right]}{\frac{s}{w_t} \left(1 + R_2 (2s) \right) \left(1 + \frac{s}{\omega_{n0}} \right)}$$

Part 3, Step 4: Design and Simulation Results of the Biquad

- Step 4: Simulate the CM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin.

L1

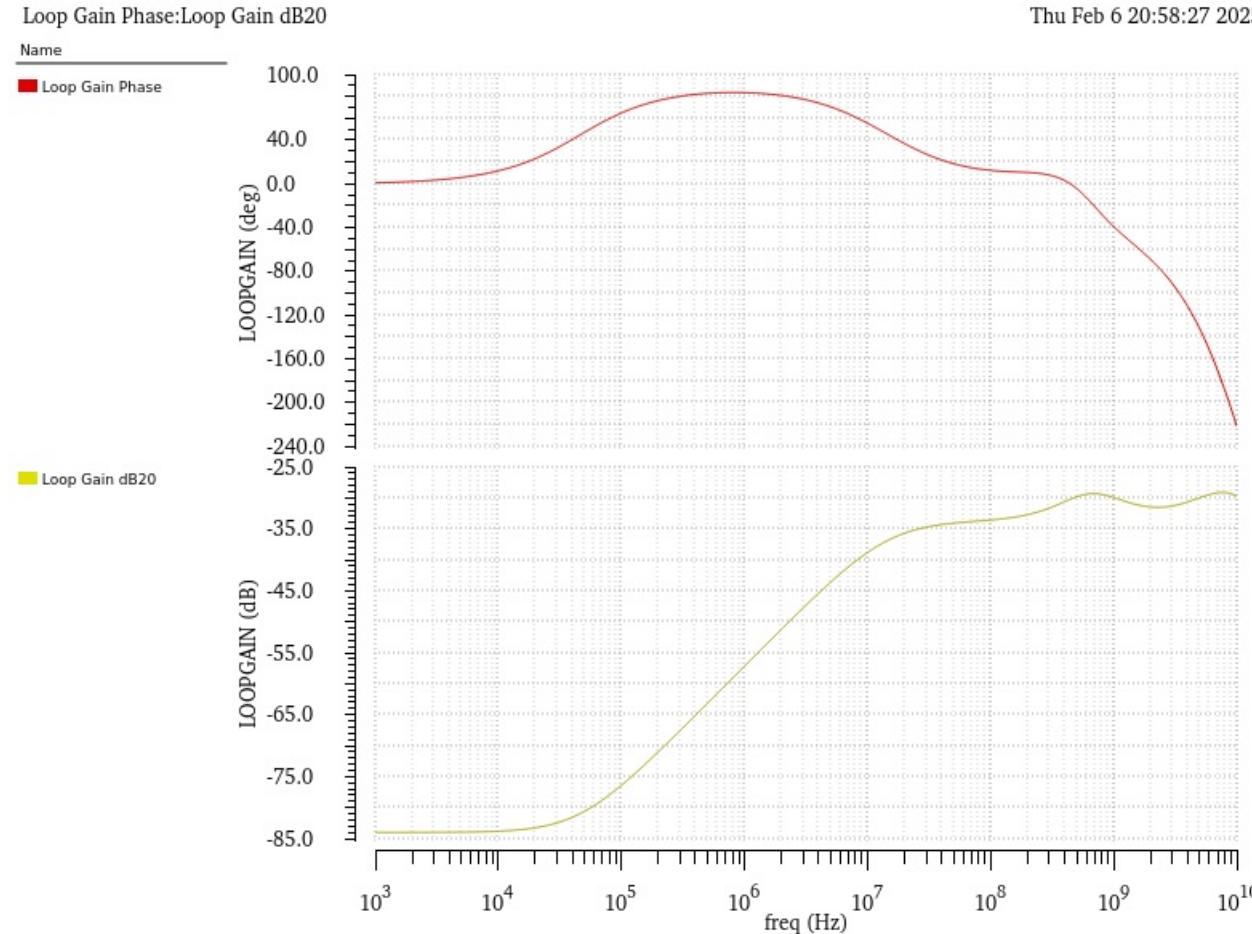


Phase margin is not defined.

Part 3, Step 4: Design and Simulation Results of the Biquad

- Step 4: Simulate the CM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin.

L2



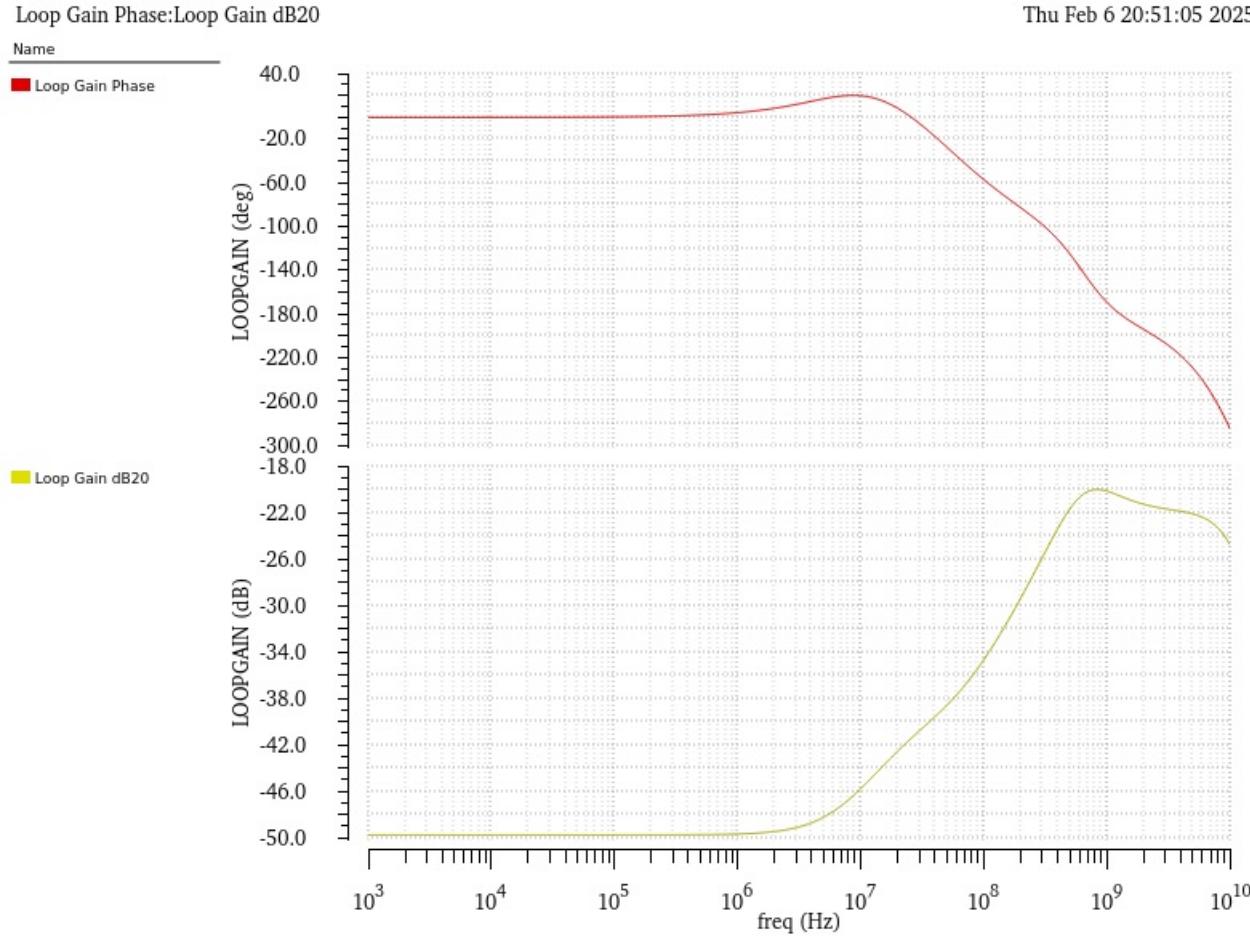
Phase Margin
is not defined

Part 3, Step 4: Design and Simulation Results of the Biquad

- Step 4: Simulate the CM gain for loop 1, 2 and 3 of the Biquad. Plot and measure the phase margin.

L3

Phase Margin undefined



Part 3, Step 5: Design and Simulation Results of the Biquad

- Step 5: Calculate the input referred noise voltage of the Biquad, calculate the input referred noise current referring to the input of the TIA.

$$\overline{V_{n,IRN}}_{\text{Biquad}} = \frac{\overline{V_{n,R_{IN}}}}{\frac{R_1}{R_{in}}} + \frac{\overline{V_{n,R_1}}}{\frac{R_1}{R_{in}}} = \frac{\sqrt{4kT R_{in}}}{\frac{R_1}{R_{in}}} + \frac{\sqrt{4kT R_1}}{\frac{R_1}{R_{in}}} = 27.3 \text{ nV}/\sqrt{\text{Hz}}$$

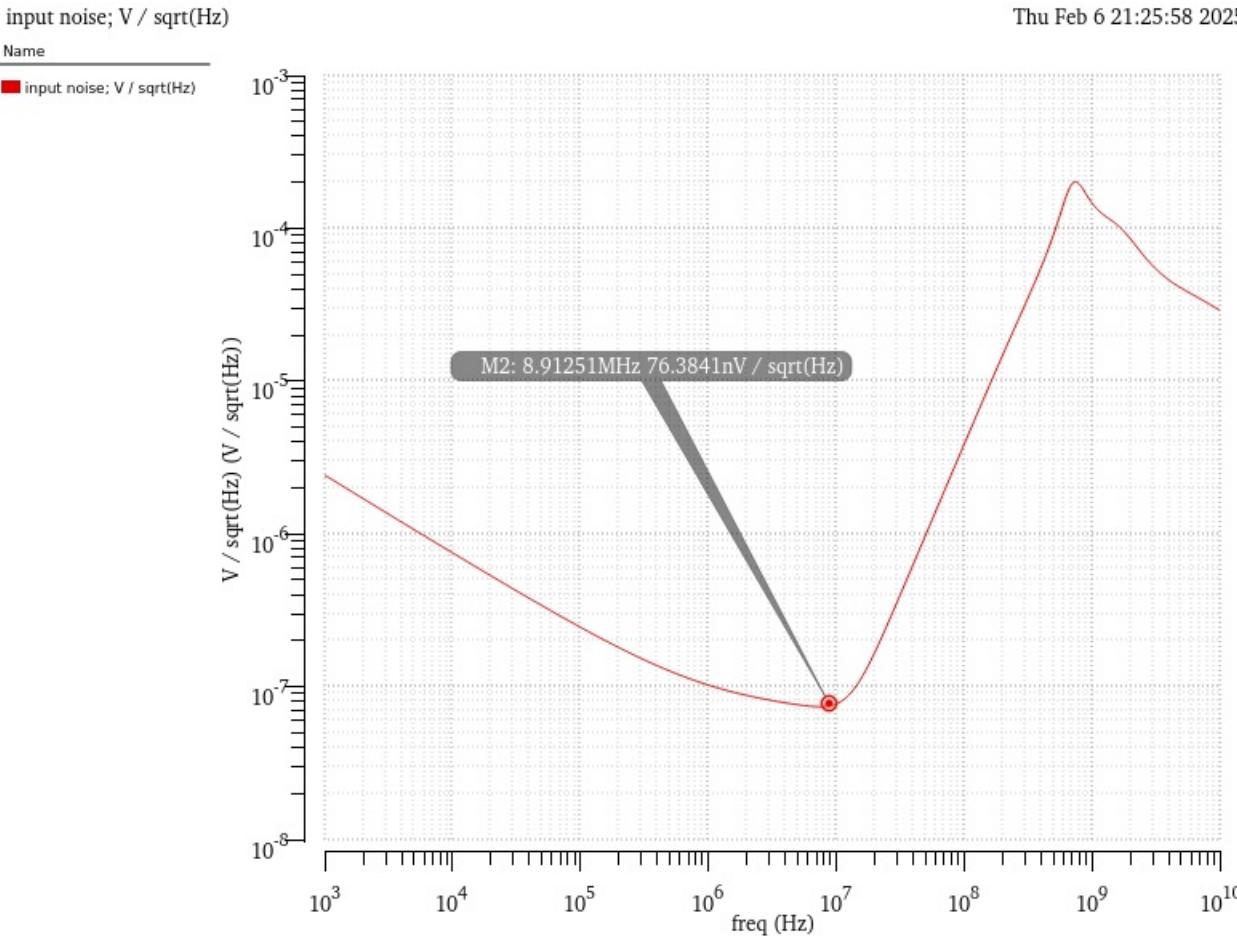
$$\overline{I_{n,IRN_TIA}} = \frac{\overline{V_{n,IRN,Biquad}}}{R_f-TIA} + \frac{\overline{V_{n,R_f-TIA}}}{R_f-TIA} = 27 \text{ pA}/\sqrt{\text{Hz}}$$



$$\frac{\sqrt{4kTR_f-TIA}}{R_f}$$

Part 3, Step 6: Design and Simulation Results of the Biquad

- Step 6: Simulate the input referred noise voltage of the Biquad and print the noise summary table for the top 25 noise contributors.



Results Display Window

Window Expressions Info Help

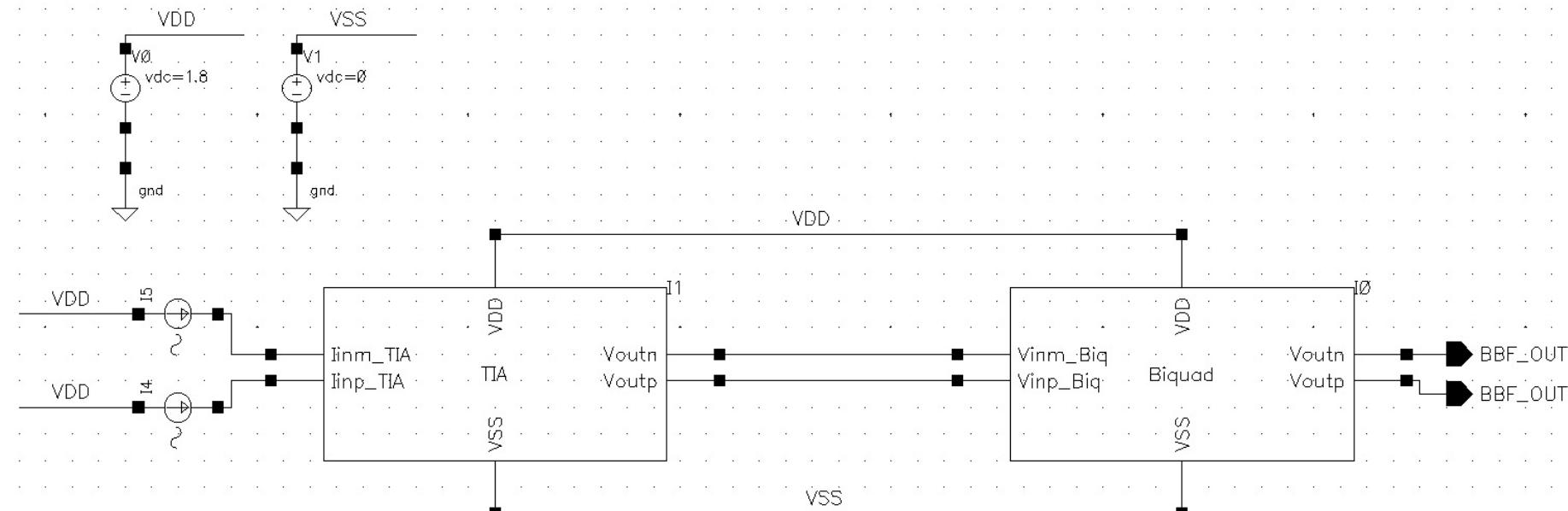
cadence

Device	Param	Noise Contribution	% Of Total
R30.r1	thermal_noise	1.29219e-16	4.78
R9.r1	thermal_noise	1.26044e-16	4.66
/I11<0>/M1	id	1.02958e-16	3.81
/I11<1>/M1	id	1.02958e-16	3.81
/I11<2>/M1	id	1.02958e-16	3.81
/I11<0>/M6	id	1.02191e-16	3.78
/I11<1>/M6	id	1.02191e-16	3.78
/I11<2>/M6	id	1.02191e-16	3.78
R31.r1	thermal_noise	7.87827e-17	2.91
R32.r1	thermal_noise	7.87519e-17	2.91
R29.r1	thermal_noise	7.77929e-17	2.88
R28.r1	thermal_noise	7.77928e-17	2.88
/I11<0>/M2	id	7.62178e-17	2.82
/I11<1>/M2	id	7.62178e-17	2.82
/I11<2>/M2	id	7.62178e-17	2.82
/I11<0>/M0	id	7.62109e-17	2.82
/I11<1>/M0	id	7.62109e-17	2.82
/I11<2>/M0	id	7.62109e-17	2.82
R33.r1	thermal_noise	7.28681e-17	2.70
R34.r1	thermal_noise	7.28678e-17	2.70
/I11<0>/M1	fn	2.97953e-17	1.10
/I11<1>/M1	fn	2.97953e-17	1.10
/I11<2>/M1	fn	2.97953e-17	1.10
/I11<0>/M6	fn	2.95733e-17	1.09
/I11<1>/M6	fn	2.95733e-17	1.09

Spot Noise Summary (in V^2/Hz) at 10M Hz Sorted By Noise Contributors
Total Summarized Noise = 2.70359e-15
Total Input Referred Noise = 6.17746e-15
The above noise summary info is for noise data

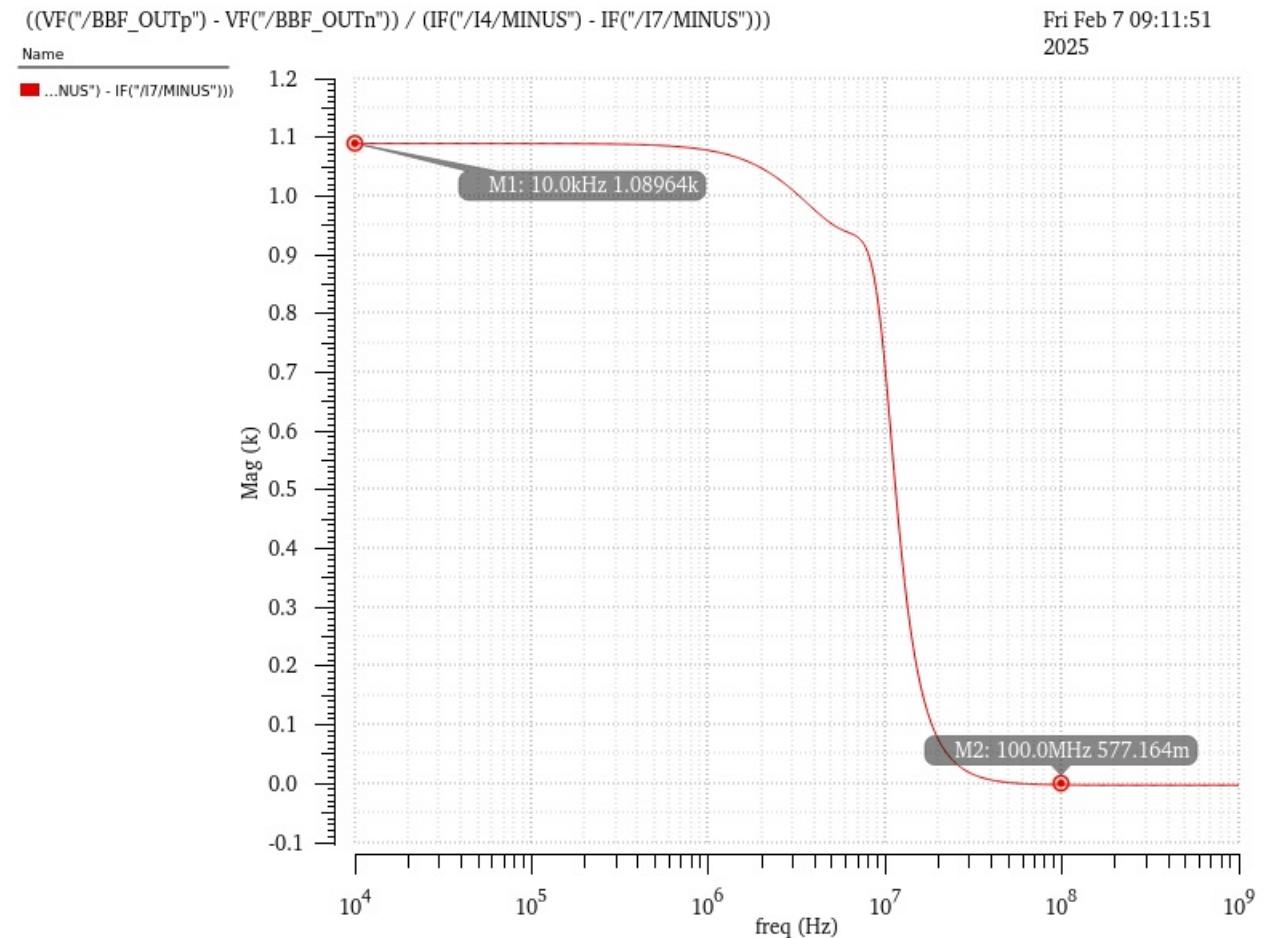
Part 4, Step 1: Design and Simulation Results of the BBF

- Step 1: Build the schematics of the BBF using the design in part 3 and 4 and drive with 1mA peak ac current source connected to Vdd to emulate the Tx DAC at the input of the TIA. Provide screen shots of the schematics.



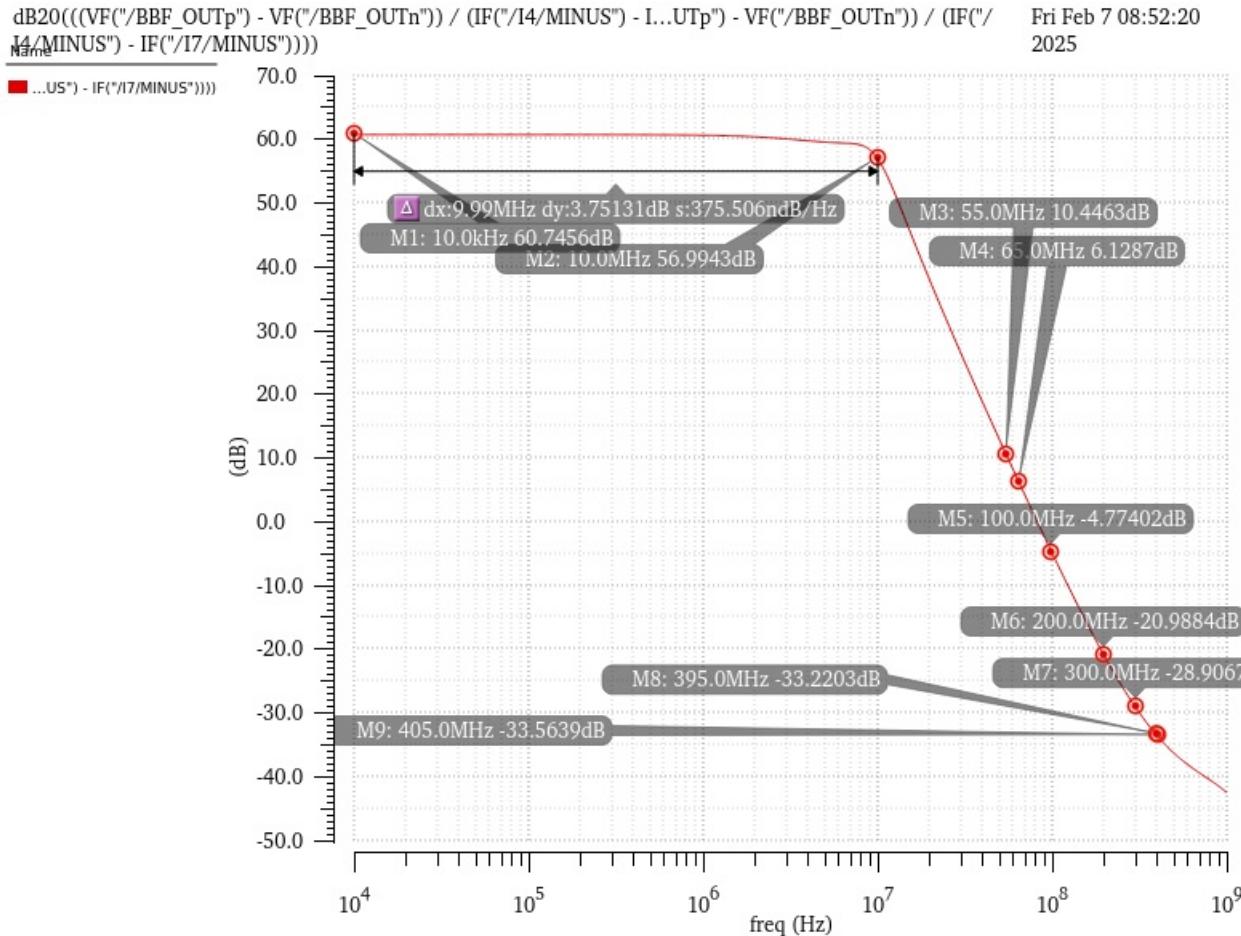
Part 4, Step 2: Design and Simulation Results of the BBF

- Step 2: Simulate the schematics in step 1 and plot the gain of the BBF (in Ohms) from 10kHz to 1GHz.



Part 4, Step 3: Design and Simulation Results of the BBF

- Step 3: Measure the following performance and compare with the design targets:
 - Gain variation (ripple) in the passband (10kHz – 10MHz) 10m Hz BW
 - Rejection in the Receive Band (60MHz offset) $55 - 65\text{M}$
 - Rejection in the GNSS Band (400MHz offset) $395 - 405\text{M}$
 - Rejection of 1st, 2nd and 3rd DAC images/clock feedthrough (SR = 100MHz)



Gain variation : 3.75dB

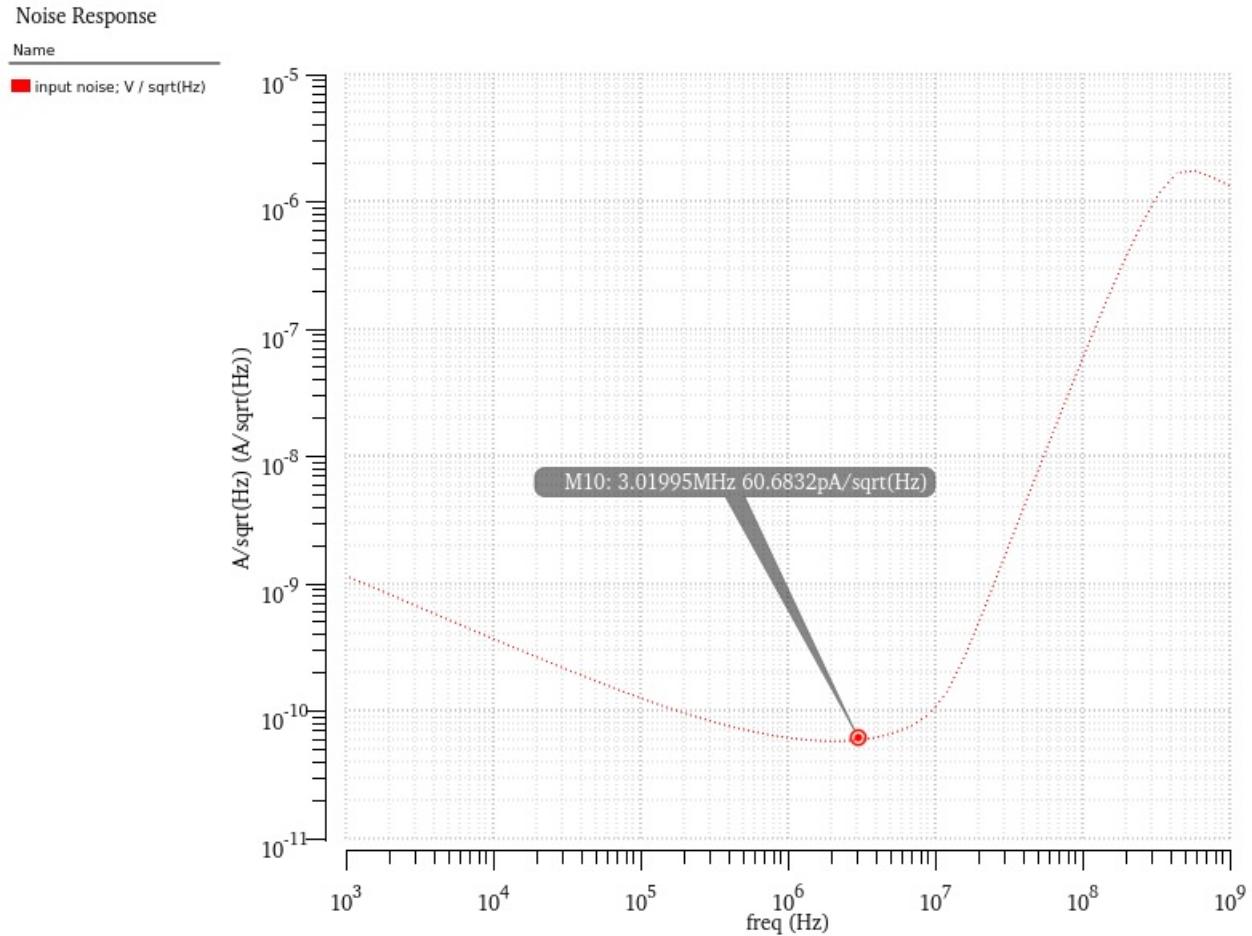
Rejection in Rx band: $55\text{M} \leftrightarrow 65\text{M}$
 $50\text{ dB} \leftrightarrow 54\text{ dB}$

Rejection in GNSS : 93dB

Rejection of DAC clock feed through
 1st 2nd 3rd
 64 dB 80 dB 88 dB

Part 4, Step 4: Design and Simulation Results of the BBF

- Step 4: Simulate the input referred noise current of the BBF and print the noise summary table for the top 25 noise contributors.



Device	Param	Noise Contribution	% Of Total
I0.R31.r1	thermal_noise	5.80312e-17	5.50
I0.R32.r1	thermal_noise	5.80029e-17	5.50
I0.R29.r1	thermal_noise	5.73112e-17	5.44
I0.R28.r1	thermal_noise	5.7289e-17	5.43
I0.R34.r1	thermal_noise	5.36674e-17	5.09
I0.R33.r1	thermal_noise	5.36467e-17	5.09
I0.R30.r1	thermal_noise	4.51657e-17	4.28
I0.R9.r1	thermal_noise	4.32535e-17	4.10
/I0/I10<0>/M23	id	1.98932e-17	1.89
/I0/I10<1>/M23	id	1.98932e-17	1.89
/I0/I10<2>/M23	id	1.98932e-17	1.89
/I0/I10<0>/M23	fn	1.683e-17	1.60
/I0/I10<1>/M23	fn	1.683e-17	1.60
/I0/I10<2>/M23	fn	1.683e-17	1.60
/I0/I10<0>/M18	id	1.44831e-17	1.37
/I0/I10<1>/M18	id	1.44831e-17	1.37
/I0/I10<2>/M18	id	1.44831e-17	1.37
/I0/I10<0>/M19	id	1.43777e-17	1.36
/I0/I10<1>/M19	id	1.43777e-17	1.36
/I0/I10<2>/M19	id	1.43777e-17	1.36
/I0/I11<2>/M2	id	1.40221e-17	1.33
/I0/I11<1>/M2	id	1.40221e-17	1.33
/I0/I11<0>/M2	id	1.40221e-17	1.33
/I0/I11<2>/M0	id	1.40164e-17	1.33
/I0/I11<1>/M0	id	1.40164e-17	1.33

Spot Noise Summary (in V^2/Hz) at 5M Hz Sorted By Noise Contributors
 Total Summarized Noise = 1.05436e-15
 Total Input Referred Noise = 4.63233e-21
 The above noise summary info is for noise data

Part 4, Step 5a: Design and Simulation Results of the BBF

- Step 5a: Simulate the BBF using 5MHz and 9M sinusoidal current sources with differential peak to peak value of 800uA each and measure the following large signal performance (i.e., choose input to get 1.6V differential peak to peak swing at the output):

$$HD_3 \text{ } 13\text{M} \approx -70.5 \text{ dB}$$

- A) HD3, IM3: calculate IIP3 and HDR3 $HD_3 \text{ } 1\text{M} \approx -82 \text{ dB}$

$$IM_3 = 54 \text{ dB}$$

Gain @ 5M-9M $\approx 56 \text{ dB}$

$$-70 \text{ dB} - 56 \text{ dB} = -126 \text{ dB}$$

$$IM_3 \text{ input-referred} = 20 \log (400u) - (-126)$$

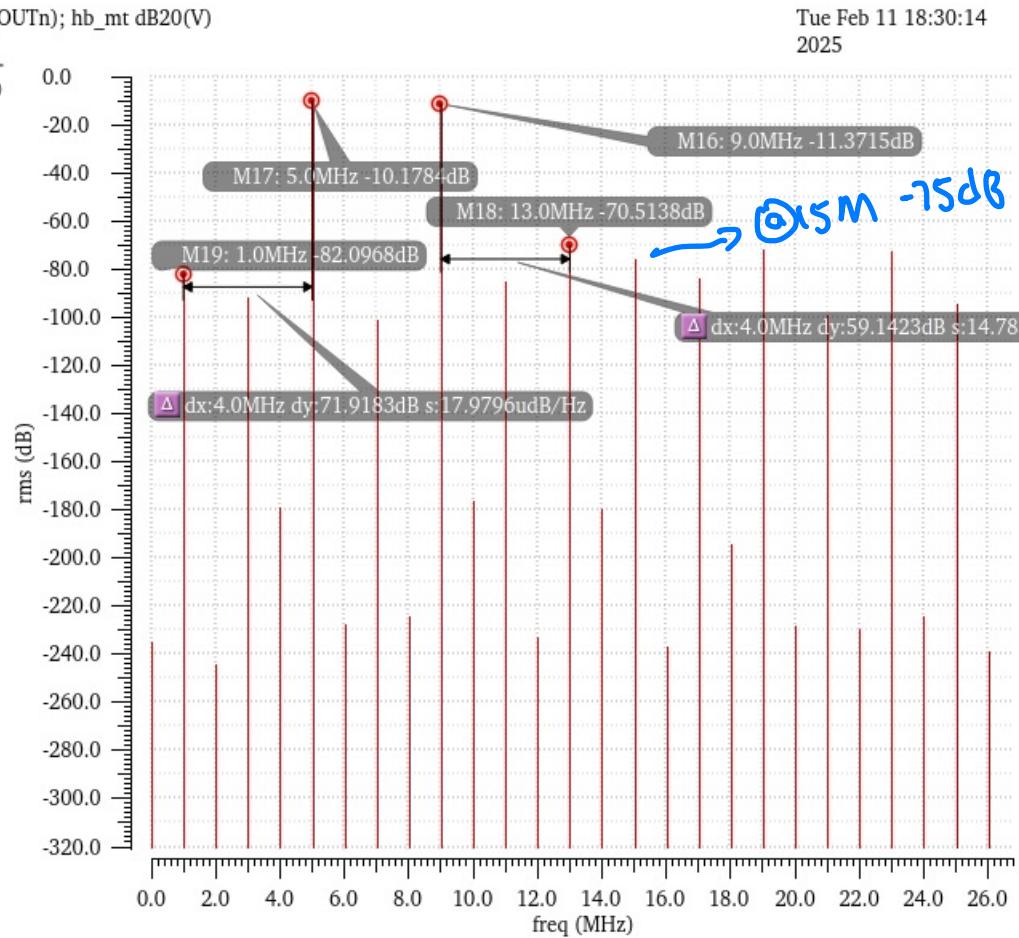
$$= 58$$

$$IIP_3 = 20 \log 400u + \frac{58}{2}$$

$$= -38.45 \text{ dB}$$

$$HDR_3(5\text{M}) = -10 - (-75) = 65 \text{ dB}$$

$$HDR_3(9\text{M}) = -11 - (-78) = 67 \text{ dB}$$



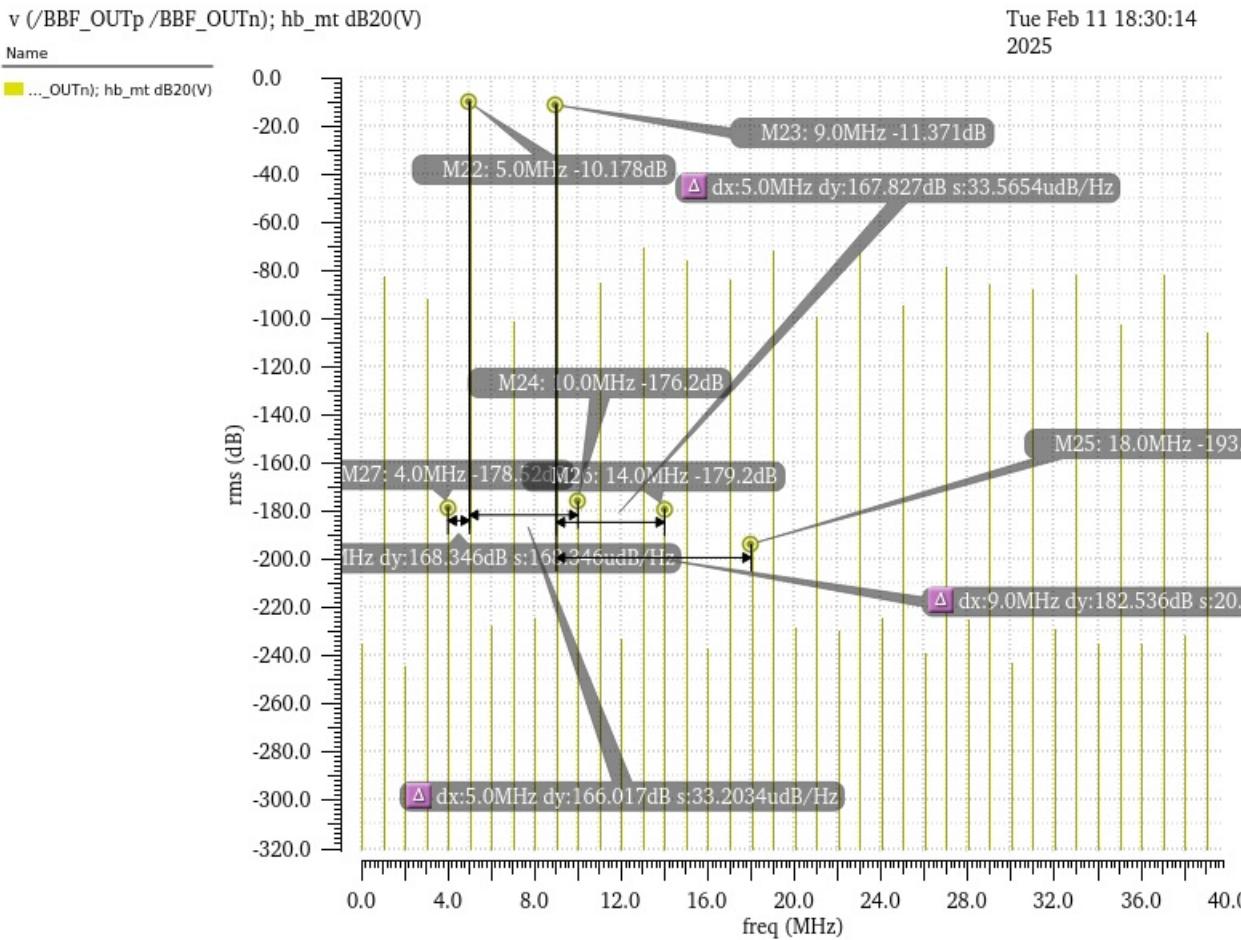
Part 4, Step 5b: Design and Simulation Results of the BBF

- Step 5b: Simulate the BBF using 5MHz and 9M sinusoidal current sources with differential peak to peak value of 800uA each and measure the following large signal performance (i.e., choose input to get 1.6V differential peak to peak swing at the output): $HD_2(14M) = -179.43$ $HD_2(4M) = -178dB$
 - B) Differential HD2, IM2 & calculate IIP2 and HDR2

$$HDR_2(5M) = -10 - (-193) = 183 \text{ dB}$$

$$HDR_2(9M) = -11 - (-176) = 165 \text{ dB}$$

$$IM_2 = -11 + 179 = 168 \text{ dB}$$



Gain @ 5M-9M $\approx 56 \text{ dB}$

$$-178 \text{ dB} - 56 \text{ dB} = -234 \text{ dB}$$

$$IM_2 \text{ input-referred} = 20 \log(400u) - (-234)$$

$$= 166 \text{ dB}$$

$$IIP_2 = 20 \log(400u) + \frac{IM_2}{2}$$

$$= 15 \text{ dB A}$$

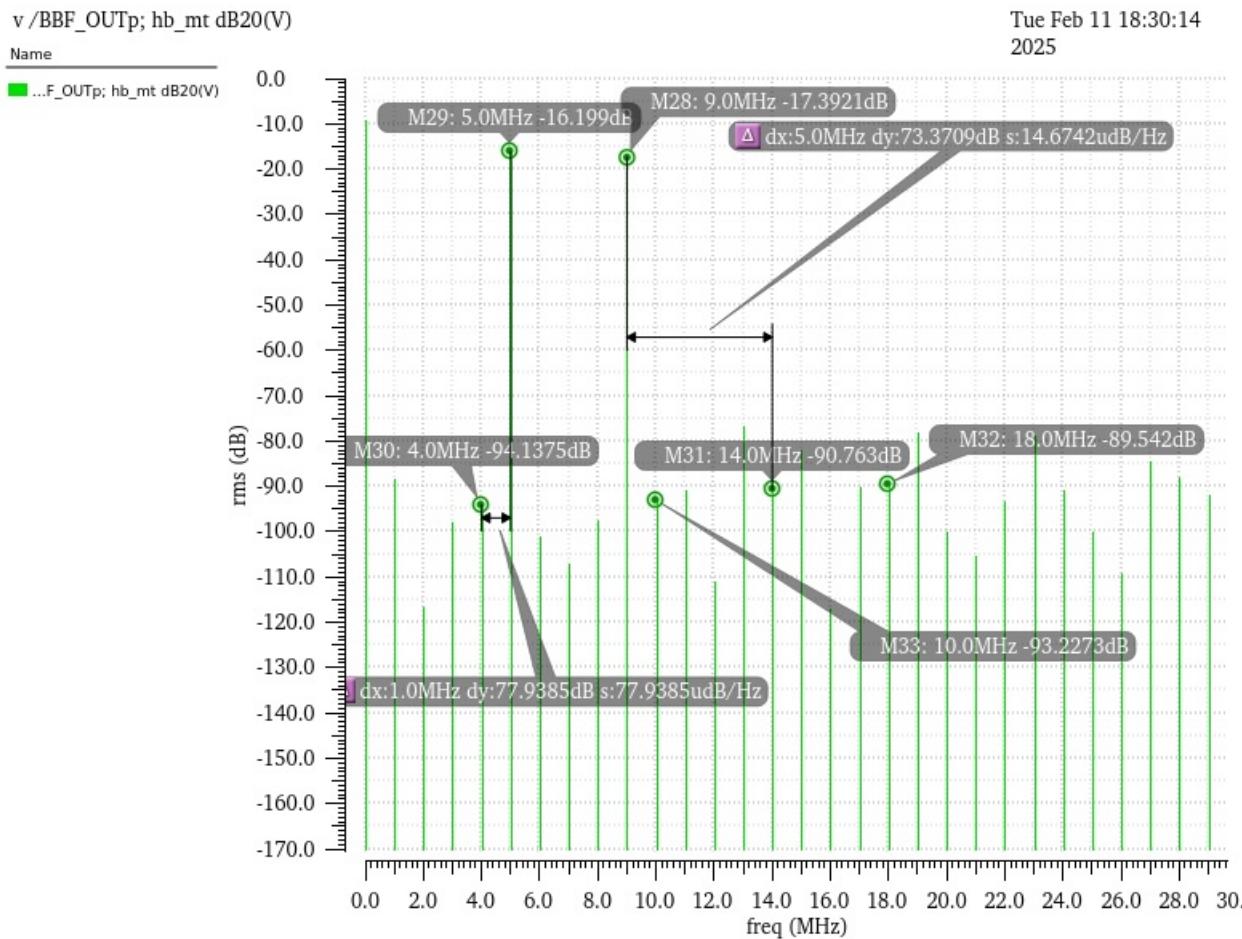
Part 4, Step 5c: Design and Simulation Results of the BBF

- Step 5c: Simulate the BBF using 5MHz and 9M sinusoidal current sources with differential peak to peak value of 800uA each and measure the following large signal performance (i.e., choose input to get 1.6V differential peak to peak swing at the output):
 - C) Single-ended HD2, IM2 & calculate IIP2 and HDR2

$$H02(10M) = -93 \text{ dB} \quad H0R_2(4M) = 78 \text{ dB}$$

$$H02(18M) = -89 \text{ dB} \quad H0R_2(14M) = 73 \text{ dB.}$$

$$IM2 = -17 - (-90) = 73 \text{ dB}$$



$$\text{Gain @ } 5\text{M-9M} \approx 56 \text{ dB}$$

$$-90 \text{ dB} - 56 \text{ dB} = -146 \text{ dB}$$

$$IM2_{\text{input-referred}} = 20 \log(400u) - (-146)$$

$$= 78 \text{ dB}$$

$$IIP_2 = 20 \log(400u) + \frac{IM2}{2}$$

$$= -28.96 \text{ dB A}$$

Part 4, Step 5d: Design and Simulation Results of the BBF

- Step 5d: Simulate the BBF using 5MHz and 9M sinusoidal current sources with differential peak to peak value of 800uA each and measure the following large signal performance (i.e., choose input to get 1.6V differential peak to peak swing at the output):
 - D) SNR

Not good metrics for Baseband filter

Part 4, Step 5e: Design and Simulation Results of the BBF

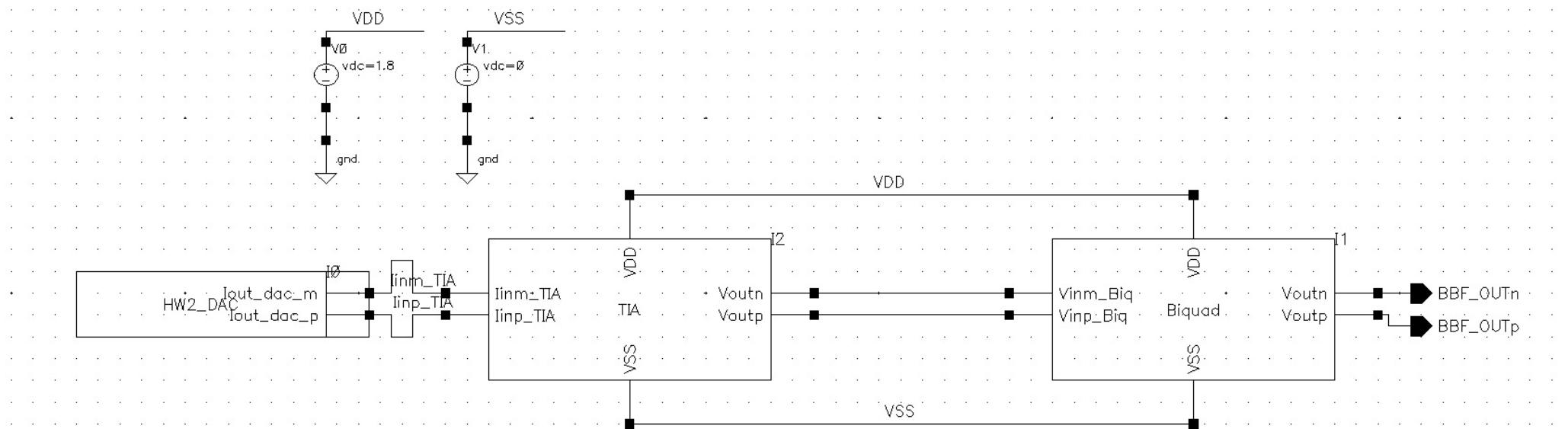
- Step 5e: Simulate the BBF using 5MHz and 9M sinusoidal current sources with differential peak to peak value of 800uA each and measure the following large signal performance (i.e., choose input to get 1.6V differential peak to peak swing at the output):
 - E) SFDR

Not good metrics for Baseband filter

Part 5, Step 1: Design and Simulation Results of the DAC + BBF

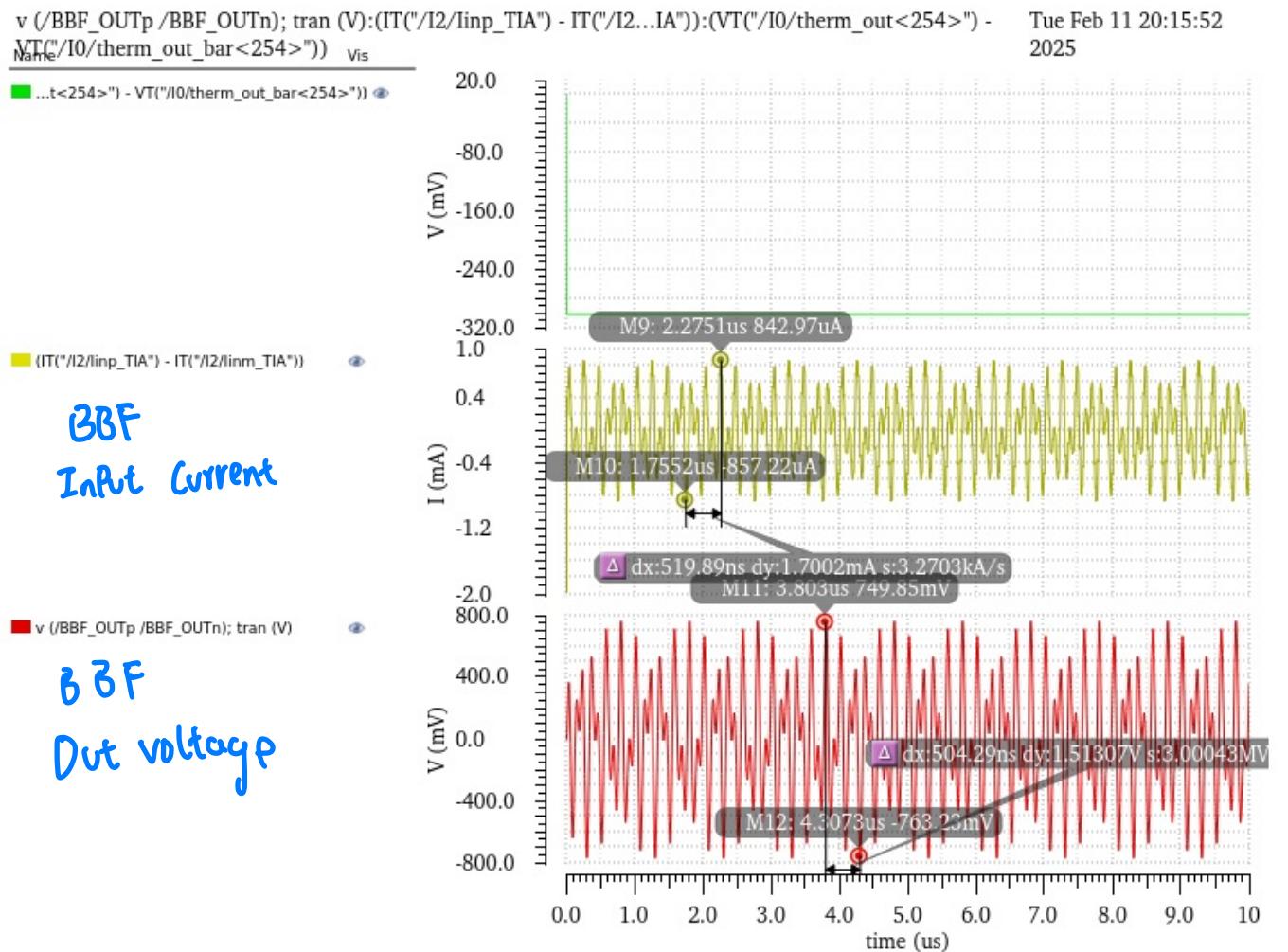
- Step 1a: Build the schematics of the DAC + BBF. Provide screen shots of the schematics.
 - Note: Replace the 300-ohm resistors used in HW #1 with 500-ohm (you needn't answer here but may think why)

↳ To have better interface
between DAC and BBF
Align the DC level



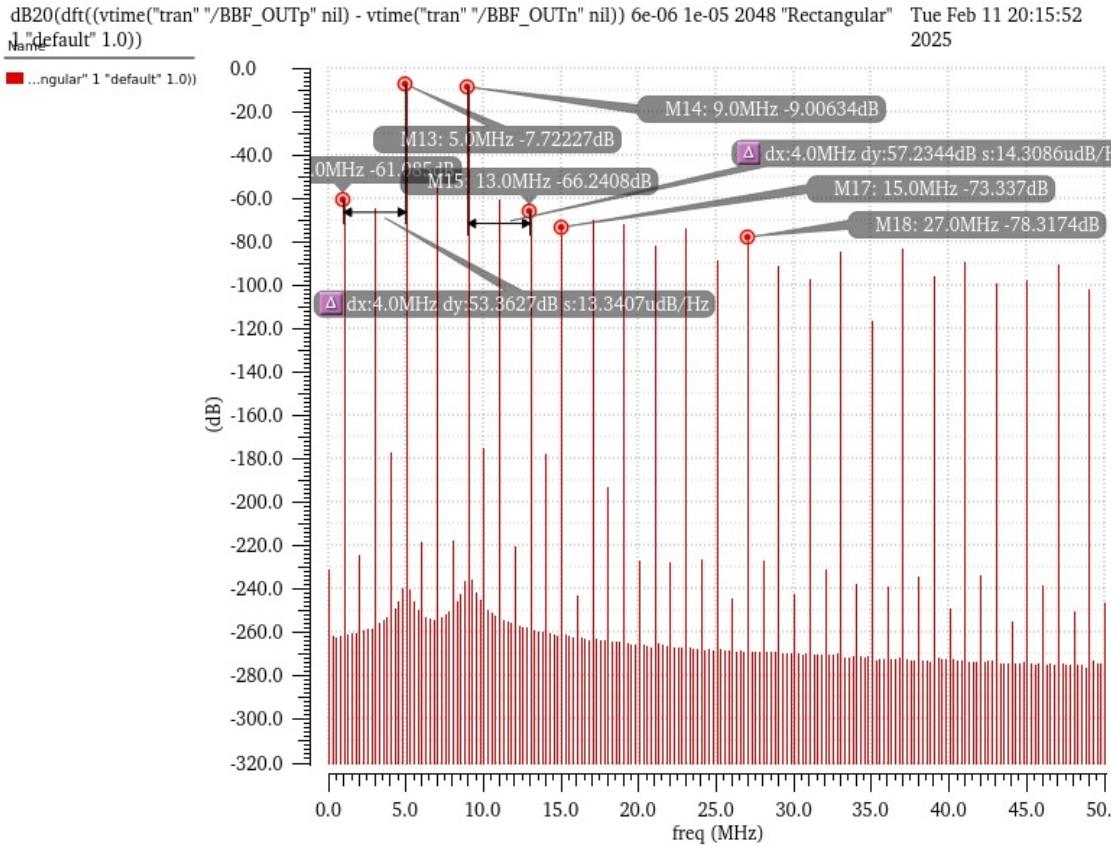
Part 5, Step 1: Design and Simulation Results of the DAC + BBF

- Step 1b: Simulate DAC+BBF and plot the following signals differentially (Input voltage to obtain the same input current as previous part):
 - DAC input voltage, DAC Output current (=BBF input current), BBF output voltage in time domain



Part 5, Step 2a: Design and Simulation Results of the DAC + BBF

- Step 2a: Simulate DAC+BBF measure the following large signal performance (Input voltage to obtain the same input current as previous part):
 - A) HD3, IM3 & calculate Inband-IIP3 & SNR



$$HD3(15\text{MHz}) = -73\text{dB}$$

$$HD3(27\text{MHz}) = -78\text{ dB}$$

$$IM3_H = 57\text{dB}$$

$$IM3_L = 53\text{ dB}$$

Gain @ 5m-9M $\approx 56\text{dB}$

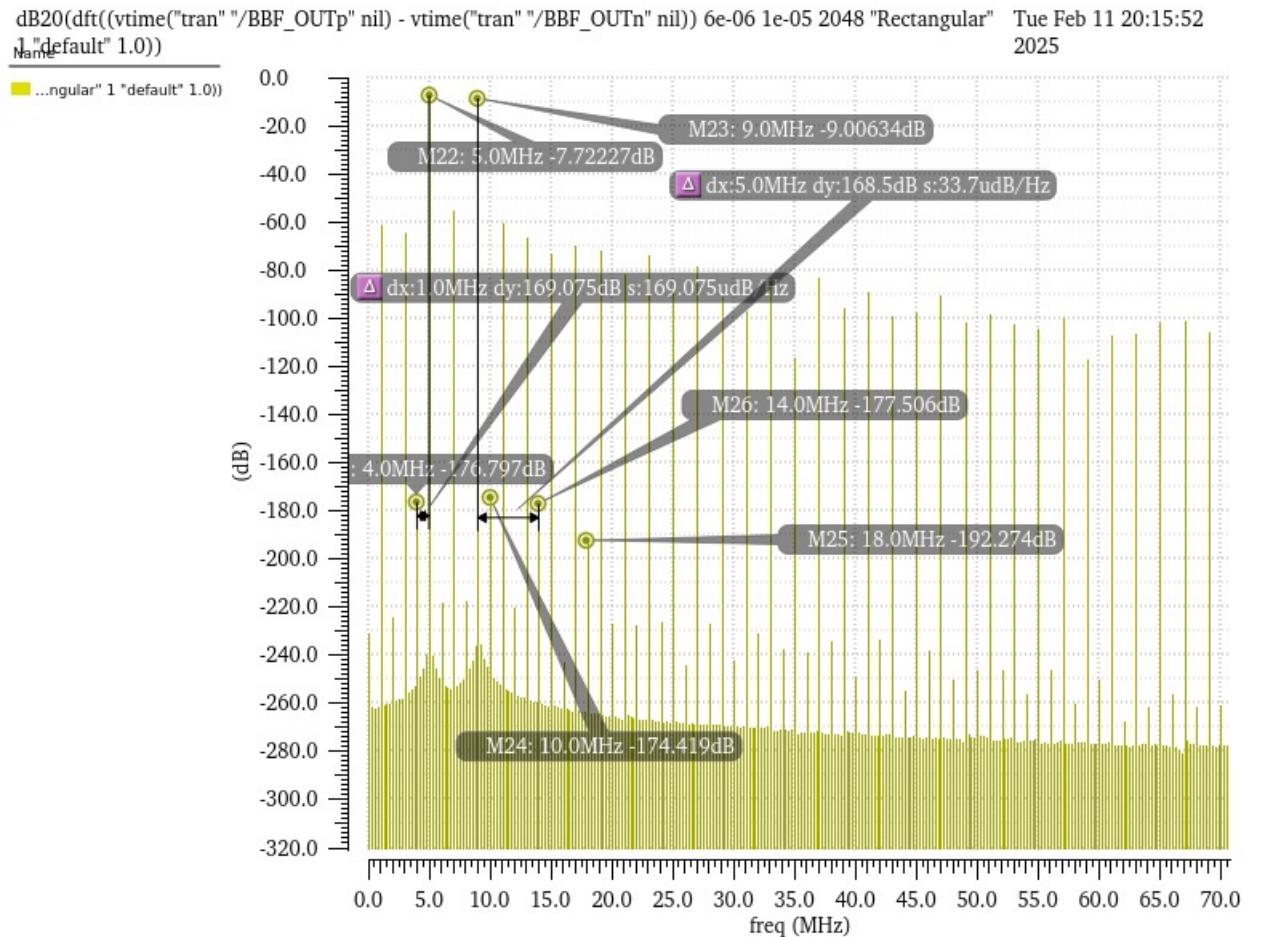
$$-61\text{ dB} - 56\text{dB} = -117\text{ dB}$$

$$\begin{aligned} IM_3 \text{ input-referred} &= 20\log(400u) - (-117) \\ &= 49\text{ dB} \end{aligned}$$

$$\begin{aligned} IIP_3 &= 20\log(400u) + \frac{IM^2}{2} \\ \text{input-reff.} &= -43\text{ dB A} \end{aligned}$$

Part 5, Step 2b: Design and Simulation Results of the DAC + BBF

- Step 2b: Simulate DAC+BBF measure the following large signal performance (Input voltage to obtain the same input current as previous part):
 - B) Differential HD2, IM2 & calculate Inband-IIP2



$$HD_2(10M) \approx -174 \text{ dB}$$

$$HD_2(18M) = -192 \text{ dB}$$

$$IM_{2\text{ Low}} = 169 \text{ dB} \quad IM_{2\text{ High}} = 168 \text{ dB}$$

Gain @ 5M-9M $\approx 56 \text{ dB}$

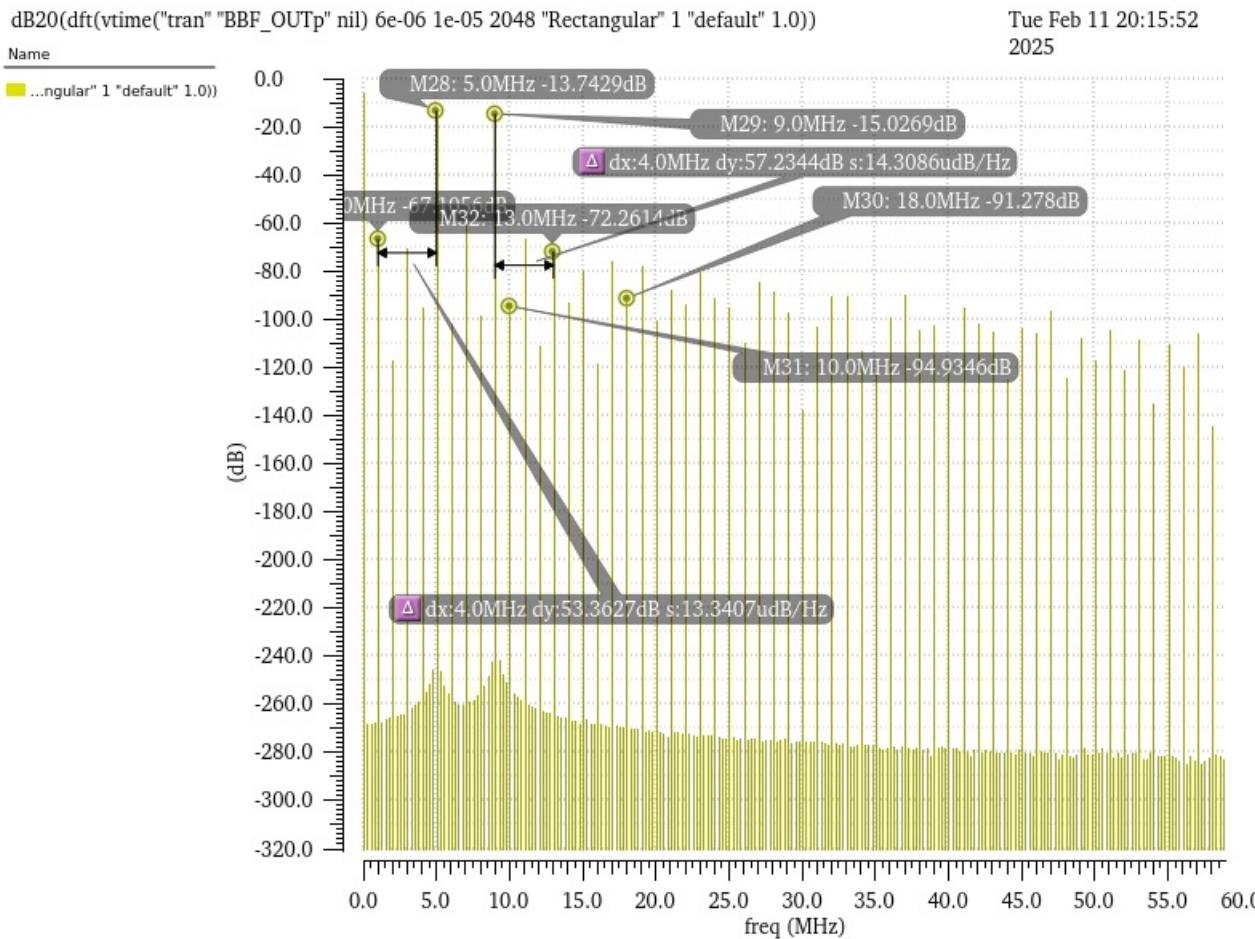
$$-176 - 56 = -232 \text{ dB}$$

$$\begin{aligned} IM_{2\text{ input.refered}} &= 20 \log(400u) - (-) \\ &= 164 \text{ dB} \end{aligned}$$

$$\begin{aligned} IIP_2 &= 20 \log(400u) + \frac{IM_3}{2} \\ &= 14 \text{ dB} \end{aligned}$$

Part 5, Step 2c: Design and Simulation Results of the DAC + BBF

- Step 2c: Simulate DAC+BBF measure the following large signal performance (Input voltage to obtain the same input current as previous part):
 - C) Single-ended HD2, IM2 & calculate Inband-IIP2



$$HD_2(10M) = -95 \text{ dB}$$

$$HD_2(18M) = -91.3 \text{ dB}$$

$$IM_2.H_i = 57 \text{ dB} \quad IM_2.L_O = 53 \text{ dB}$$

$$\text{Gain @ } 5M-9M \approx 56 \text{ dB}$$

$$-67 - 56 = -123$$

$$IM_2.\text{input referred} = 20 \log(400u) - (-123)$$

$$= 55 \text{ dB}$$

$$IIP_2.\text{input referred} = 20 \log(400u) + \frac{IM_2}{2}$$

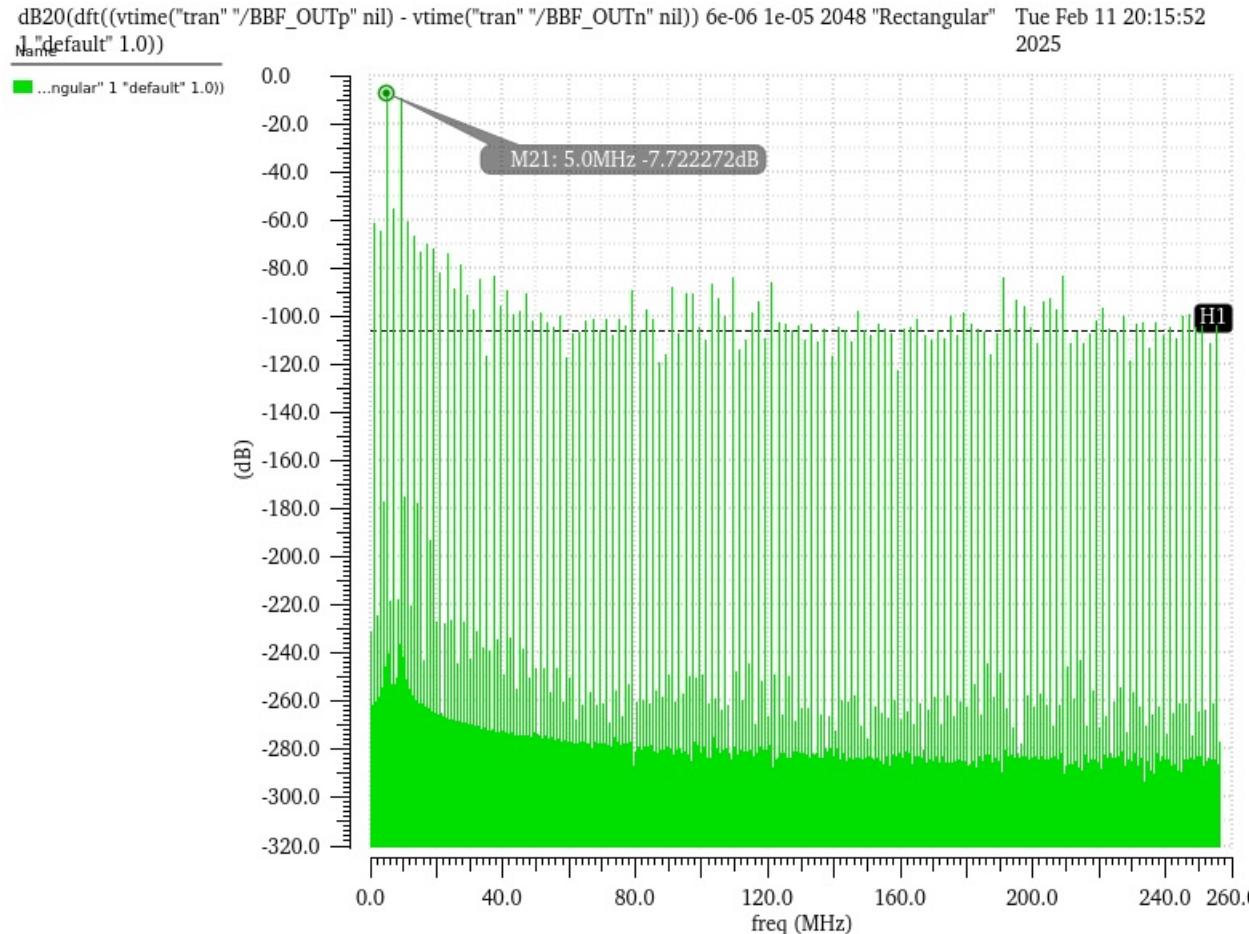
$$= -40 \text{ dB.}$$

Part 5, Step 2d: Design and Simulation Results of the DAC + BBF

- Step 2d: Simulate DAC+BBF measure the following large signal performance (Input voltage to obtain the same input current as previous part):

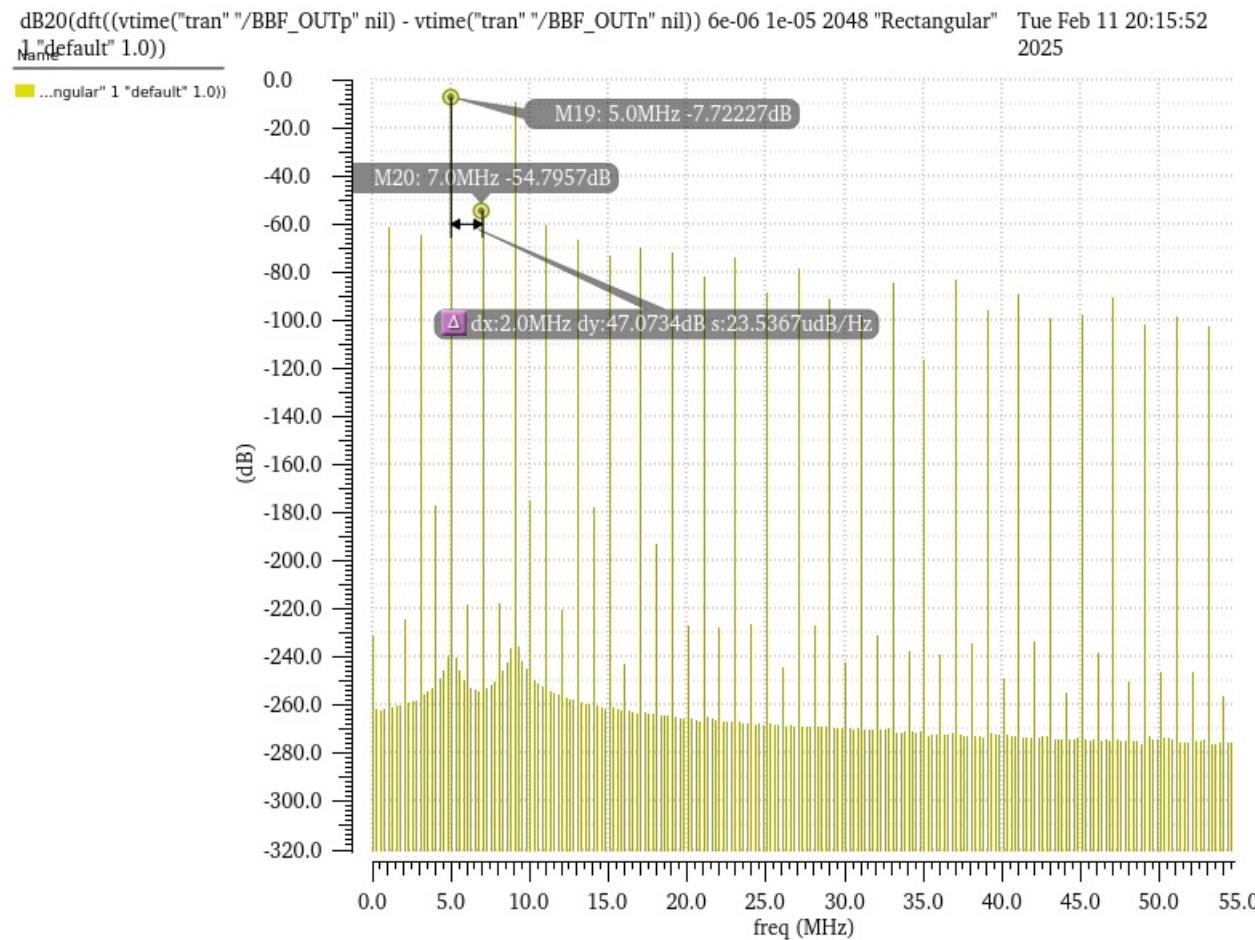
- D) SNR

$$SNR = -74\beta - (-106) = 99 \text{ dB.}$$



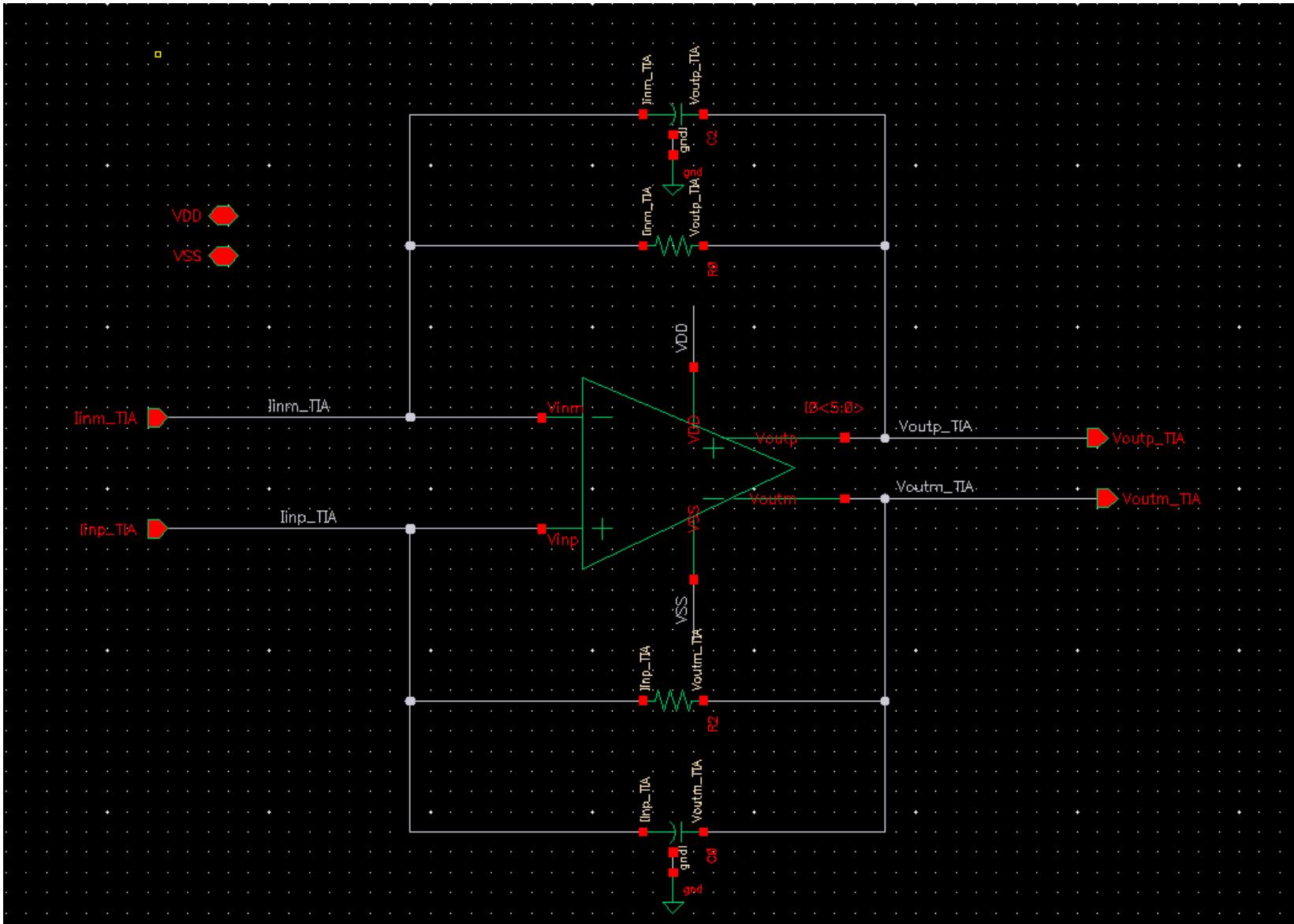
Part 5, Step 2e: Design and Simulation Results of the DAC + BBF

- Step 2e: Simulate DAC+BBF measure the following large signal performance (Input voltage to obtain the same input current as previous part):
 - E) SFDR

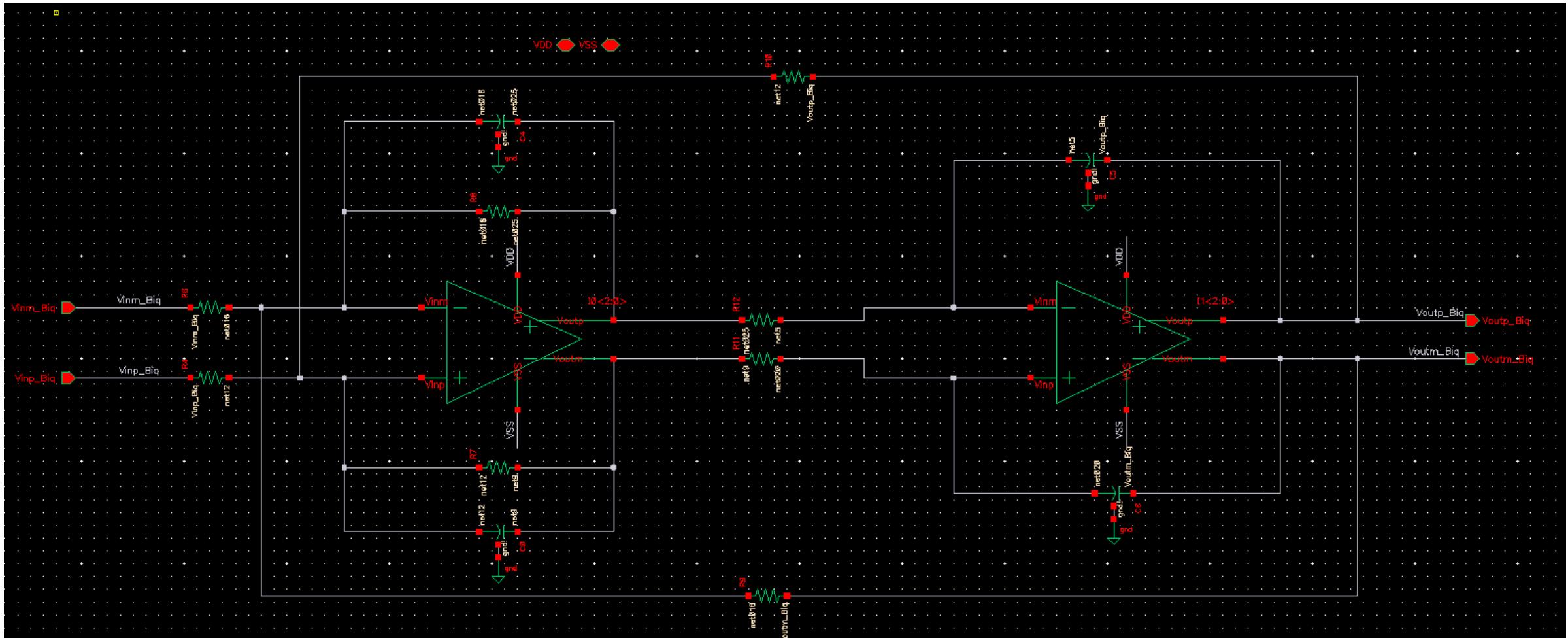


$$SFDR = 47 \text{ dB}.$$

Schematics of the TIA



Schematics of the Biquad



End