

ECE265D
Homework #3
Due 11:59pm on Mar. 7th (Fri)

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Simulation Conditions & Process Parameters

- Please save all your schematics
- Simulation Conditions:
 - Temperature = 27C = 300K
 - Process corner = Nominal
 - Supply voltage = 1.8V
- Thin-oxide MOS Process Parameters:
 - Effective mobility of electrons= 500cm²/V.s
 - Effective mobility of holes= 250cm²/V.s
 - Gate oxide capacitance (Cox) = 6fF/ um²
 - PMOS Threshold voltage = 450mV
 - NMOS Threshold voltage = 500mV
 - VE = 16V/um
 - Lmin = 60nm
- Schematics are provided for your reference.

Upconverter Design Requirements for Transmitter Application

- Application: LTE B1 (Tx: 1920 – 1980MHz, Rx: 2110 – 2170MHz). Use 2GHz for LO for simplicity.
GNSS Band: 1575MHz
- Signal Bandwidth = 20MHz at RF (10MHz at Baseband), 16QAM LTE
- Upconverter Type: 25% duty-cycle LO NMOS passive mixer
- Input Signal Source Impedance = Series 10 Ohm resistance (differential) to emulate the Tx BBF
- Input Signal Source = 400mV (SE peak) = 800mV (SE peak-to-peak) = 800mV (DE peak) = 1600mV (DE peak-to-peak) to emulate the Tx BBF
- Output Load Impedance = 60fF capacitance (SE) to emulate the input of the Tx DA
- Output Signal (approximate) = 400mV (SE peak) = 800mV (SE peak-to-peak) = 800mV (DE peak) = 1.6V (DE peak-to-peak);
- Input Common-Mode DC Voltage = 500mV (Tx BBF is DC coupled to UpC)
- Output Common-Mode DC Voltage = 0V (UpC output is AC coupled to Tx DA)
- Gain $> -6\text{dB}$
- Out-of-Band Gain at Duplex Offset (190MHz) in the Rx Band $< -6\text{dB}$
- Out-of-Band Gain at GNSS offset (345MHz) $< -6\text{dB}$
- SNDR $> 42\text{dB}$ to support 12.5% EVM Tx system budget
- ACLR $> 42\text{dB}$ to support 33dB Tx system budget

Question 1: Design of the Tx UpC

- Note 1: 20MHz LTE (10MHz I/Q) modulated signal is treated as two sinusoidal tones of 150mV (single-ended peak) at 5MHz and 9MHz.
- Note 2: Treat IM3 (lower) at 1MHz and IM2 (lower) at 4MHz as contributors to degradation of EVM.
- Note 3: Treat IM3 (upper) at 13MHz and IM2 (upper) at 14MHz as contributors to degradation of ACLR.

Question 1: Design of the Tx UpC – Step 1

Step 1: Calculate the optimal bias voltage for the gate, source, body, nwell and substrate, and LO swing voltage to minimize the resistance of the triple-well thin-oxide NMOS UpC switch considering the following requirements:

Input common-mode voltage = 500mV ;

Voltage swing = 0V

Vgs in ON stage = TDDB (1.6V)

Vgs in OFF stage = Vth – 400mV (measure Vth of the NMOS in linear region in simulation)

Use nmos_rf_6t for transistor model Use nmos_rf_6t for transistor model. For measuring V_th use transistor at L = Lmin, Wf = 3um and nf = 10

$$V_{gs,Hi} = 1.6V \quad V_{gs,LO} = 575mV - 400mV = 175mV.$$

$$\boxed{V_{LO\ swing} = 1.6 - 175mV \\ = 1.425V.}$$

$$\boxed{V_s = V_D = 500mV; \quad V_{G,High} = V_{gs,Hi} + V_s \\ = 2.1V}$$

$$\begin{aligned} V_{G,LO} &= V_{gs,LO} + V_s \\ &= 175mV + 0.5V = 675mV \end{aligned}$$

$$\boxed{V_{LO,Bias} = \frac{1}{4} V_{G,High} \quad \frac{3}{4} V_{G,LO} = 1.03V}$$

$$\boxed{V_{psub} = 0V}$$

$$\boxed{V_{nwell} = V_{DD} = 1.8V}$$

Question 1: Design of the Tx UpC - Step 2

- Step 2: Calculate the optimal bias voltage for the gate, source, body, nwell and substrate, and LO swing voltage to minimize the resistance of the triple-well thin-oxide NMOS UpC switch considering the following requirements:
 - Input common-mode voltage = 500mV
 - Voltage swing = 300mV (single-ended peak)
 - V_{gs} (max) in ON stage = TDDB $\rightarrow 1.6V \rightarrow 175mV$
 - V_{gs} (max) in OFF stage = $V_{th} - 400mV$ (measure V_{th} of the NMOS in linear region in simulation)

$$V_s = V_D = 0.5 \pm 0.3V \rightarrow 0.2V - 0.8V$$

$$V_{LO\ swing} = 1.6 - 175mV \\ = 1.425V.$$

$$V_{nwell} = V_{DD} = 1.8V$$

$$V_{psub} = 0V$$

$$V_{body} = 500mV$$

$$V_{G, High} = V_{gs, high} + V_s \\ = 1.6 + 0.2 = 1.8V$$

$$V_{G, LO} = V_{gs, LO} + V_s \\ = 175mV + 0.2 = 375mV$$

$$V_{LO-Bias} = \frac{1}{4} \cdot 1.8 + \frac{3}{4} \cdot 375mV = 0.73125V$$

Question 1: Design of the Tx UpC – Step 3

- Step 3: Calculate V_{gs} (max) and V_{gs} (min) for ON state and V_{gs} (max) and V_{gs} (min) for OFF state of the NMOS UpC switch to meet the requirements in step 2.

$$V_{gs\ max - DN} = 1.8V - 0.2 = 1.6V$$

$$V_{gs\ min - DN} = 1.8V - 0.8 = 1V$$

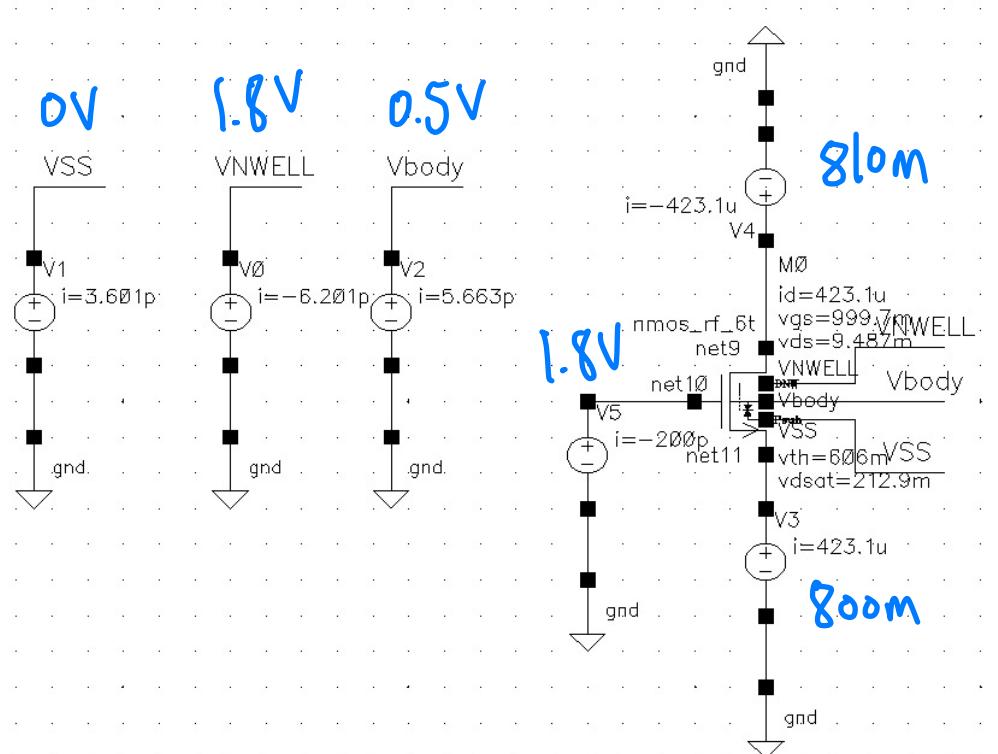
$$V_{gs\ max - OFF} = 375m - 0.2 = 175mV$$

$$V_{gs\ min - OFF} = 375m - 0.8 = -0.425V$$

Question 1: Design of the Tx UpC - Step 4

- Step 4: Consider $L = L_{min}$, $W_f = 3\text{um}$ and $n_f = 10$. Bias the NMOS UpC switch under the ON stage with V_{gs} (min) calculated in step 3 and simulate the maximum ON resistance of the NMOS UpC switch using a V_{ds} of 10mV.

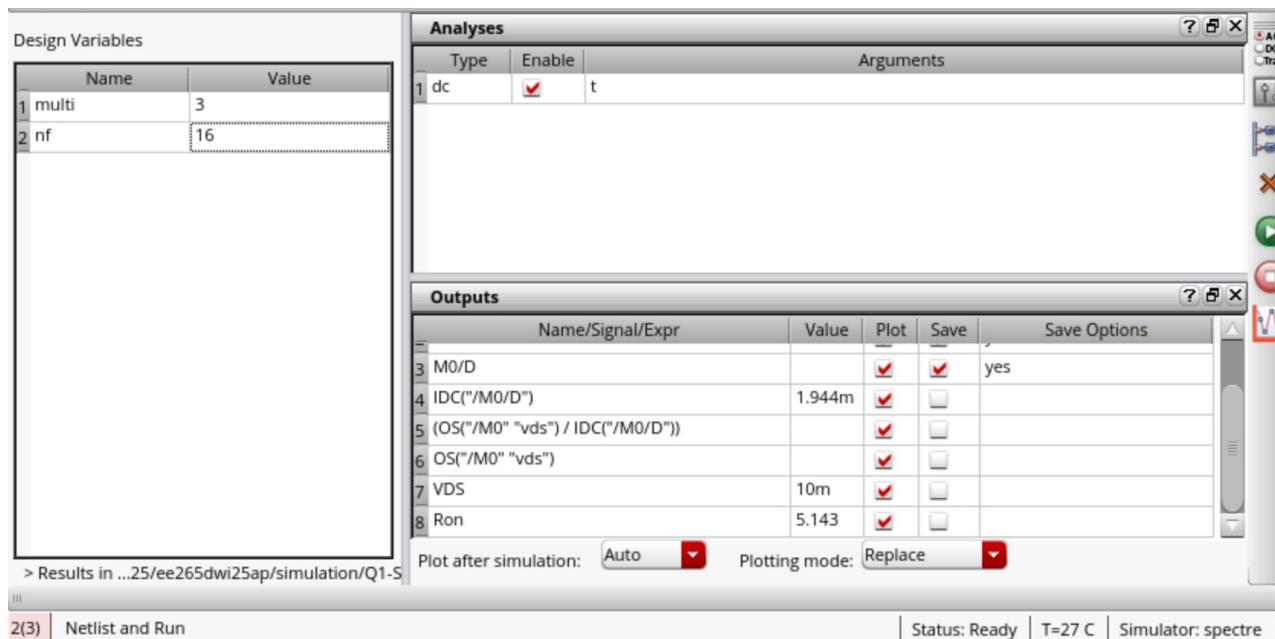
$$V_g = 1.8 \quad V_s = 0.8 \text{ V}$$



$$R_{on} = \frac{V_{ds}}{I_0} = 23.63 \text{ }\Omega$$

Question 1: Design of the Tx UpC – Step 5

- Step 5: From the simulation results in step 4, determine the approximate “nf” and “m” of the NMOS UpC switch required to achieve a resistance of 5 ohms for the UpC switch. Simulate the maximum ON resistance of the NMOS UpC switch using a Vds of 10mV. (Maximum nf allowed = 32)

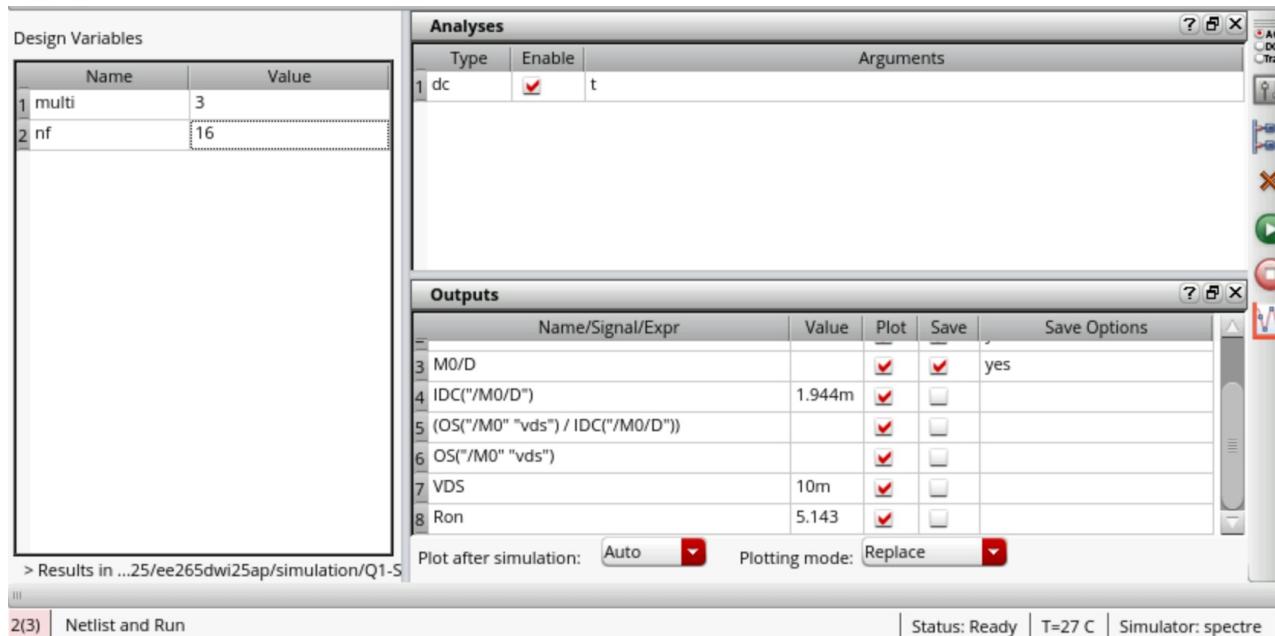


$$nf = 16$$

$$m = 3$$

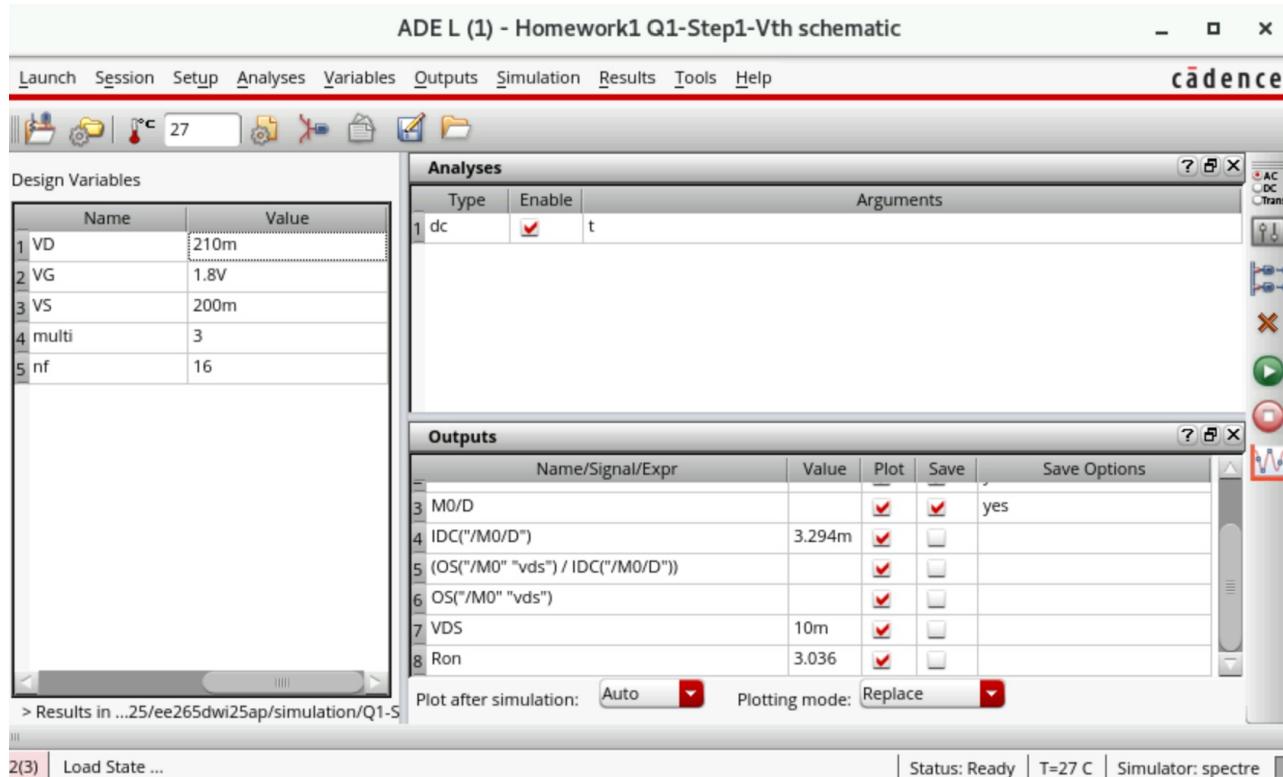
Question 1: Design of the Tx UpC – Step 5

- Step 5: From the simulation results in step 4, determine the approximate “nf” and “m” of the NMOS UpC switch required to achieve a resistance of 5 ohms for the UpC switch. Simulate the maximum ON resistance of the NMOS UpC switch using a Vds of 10mV. (Maximum nf allowed = 32)



Question 1: Design of the Tx UpC – Step 6

- Step 6: Using a process similar to what is described in step 4, simulate the minimum ON resistance of the NMOS UpC switch.



ON stage

V_{gs}- max

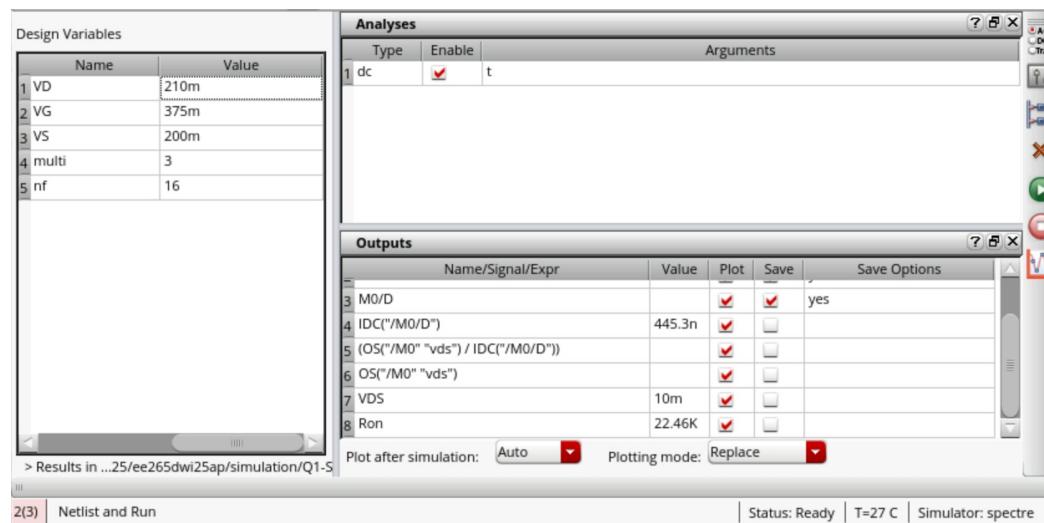
$$V_g = 1.8$$

$$V_s = 0.2 \quad V_0 = 0.21$$

$$R_{on} = 3.036 \Omega$$

Question 1: Design of the Tx UpC – Step 7

- Step 7: Using the UpC switch size in step 5 and using the process similar to what is described in step 4 and 6, simulate the minimum OFF resistance and maximum OFF resistance of the UpC switch.



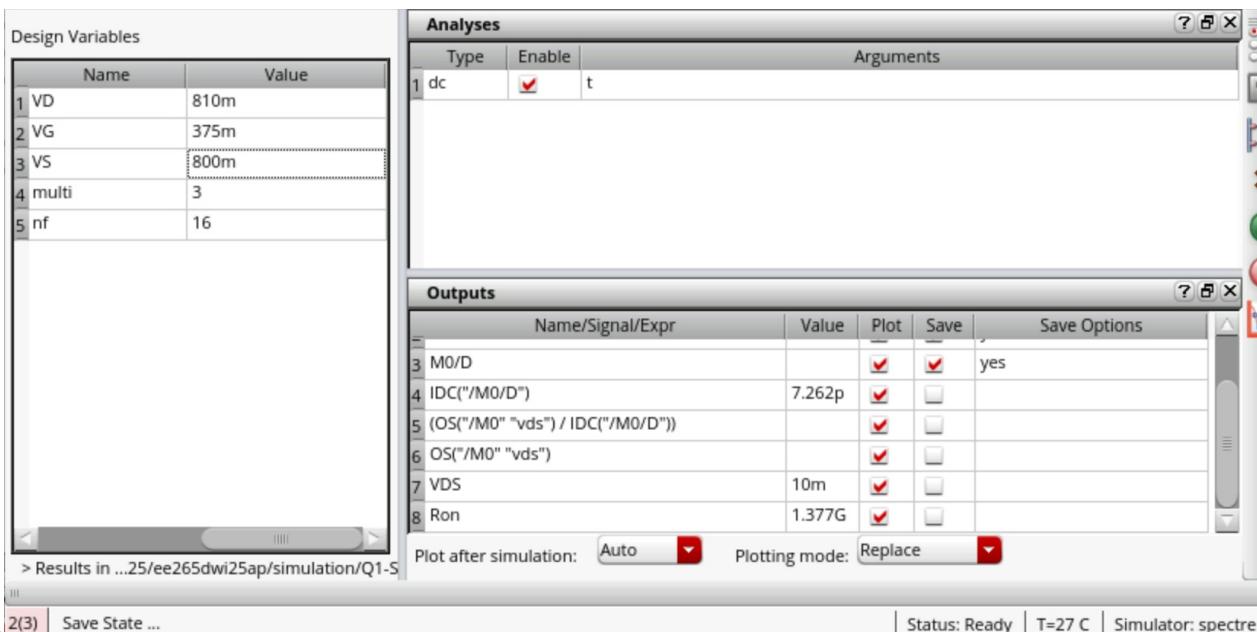
Minimum OFF

$$V_G = 375\text{m}$$

$$V_S = 0.2$$

$$V_D = 0.21$$

$$R_{on,min} = 22.46 \text{ k}\Omega$$



Maximum OFF

$$V_G = 375\text{m}$$

$$V_S = 0.8$$

$$V_D = 0.81$$

$$R_{on,max} = 1.377\text{G }\Omega$$

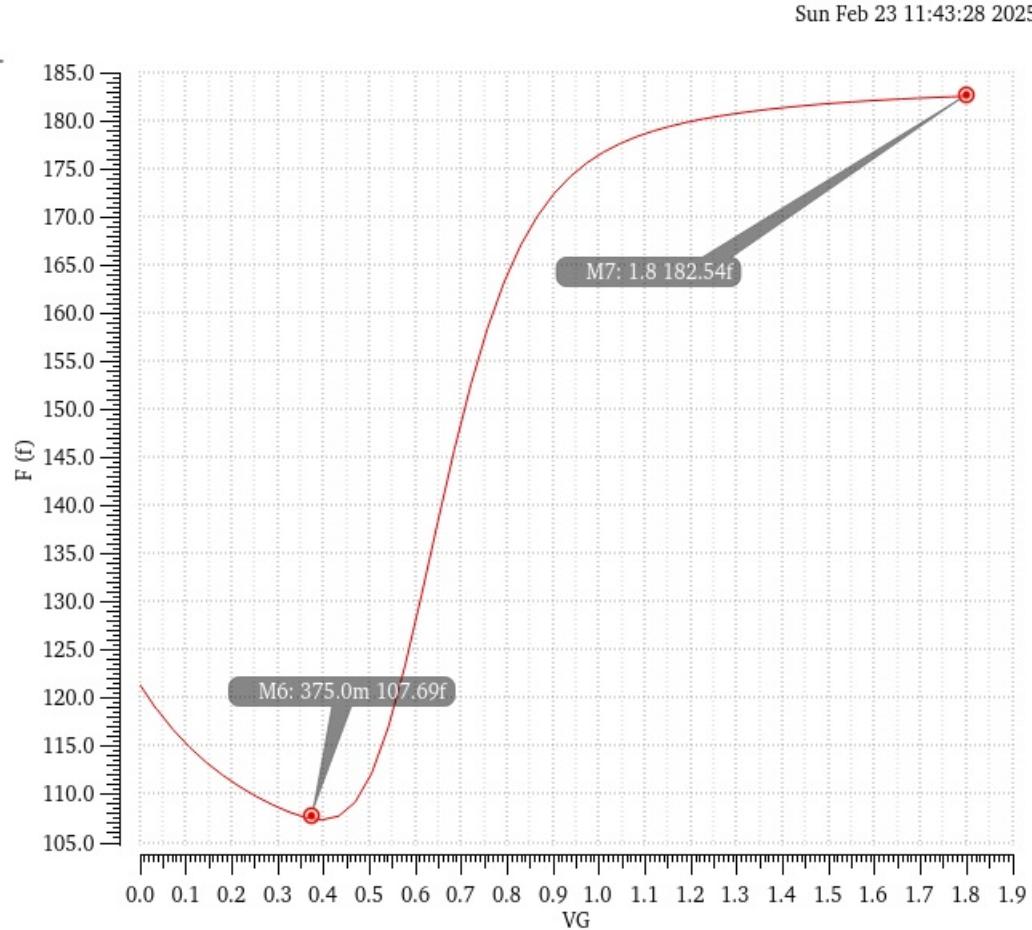
Question 1: Design of the Tx UpC – Step 8

- Step 8: Using the results in steps 5, 6 & 7, determine minimum Roff / maximum Ron.

$$\frac{R_{off-min}}{R_{on-max}} = \frac{22.46k}{5.143} = 4367$$

Question 1: Design of the Tx UpC – Step 9

- Step 9: Using the UpC switch size in step 5, simulate and measure the maximum gate capacitance of the NMOS UpC switch in ON state and minimum gate capacitance of the NMOS UpC switch in OFF state.



DN - state

$$V_g = 1.8 \text{ V}$$

$$V_s = V_D$$

$$C_{gg, \max} = 182.54 \text{ fF}$$

OFF

$$V_g = 375 \text{ mV}$$

$$V_s = V_D$$

$$C_{gg, \min} = 107.69 \text{ fF}$$

Question 1: Design of the Tx UpC –Step 10

- Step 10: Using the results in step 9, calculate the AC coupling capacitor required to ensure >95% of the LO voltage swing is transferred to the gate of the NMOS UpC switch.

$$\frac{\frac{1}{2\pi f_{LQG}}}{\frac{1}{2\pi f_{LQG}} + \frac{1}{2\pi f_{AC}}} = \frac{\frac{1}{C_{QG}}}{\frac{1}{C_{QG}} + \frac{1}{C_{AC}}} > 95\%$$

↓

use 96%
in calculation $\Rightarrow C_{AC-Coupl} = 4.4 \text{ pF}$

Question 1: Design of the Tx UpC – Step 10

- Step 10: Using the results in step 9, calculate the AC coupling capacitor required to ensure 95% of the LO voltage swing is transferred to the gate of the NMOS UpC switch.

$$\frac{\frac{1}{2\pi f_{LQG}}}{\frac{1}{2\pi f_{LQG}} + \frac{1}{2\pi f_{AC}}} = \frac{1}{c_{QG} + \frac{1}{C_{AC}}} > 95\%$$

↓
use 96%
in calculation $\Rightarrow C_{AC-Coupl} = 4.4 \text{ pF}$

Question 1: Design of the Tx UpC – Step 11

- Step 11: Using the results in step 9, calculate the DC coupling resistor required to ensure > 95% of the AC current from the LO is used to charge the gate of the NMOS UpC switch.

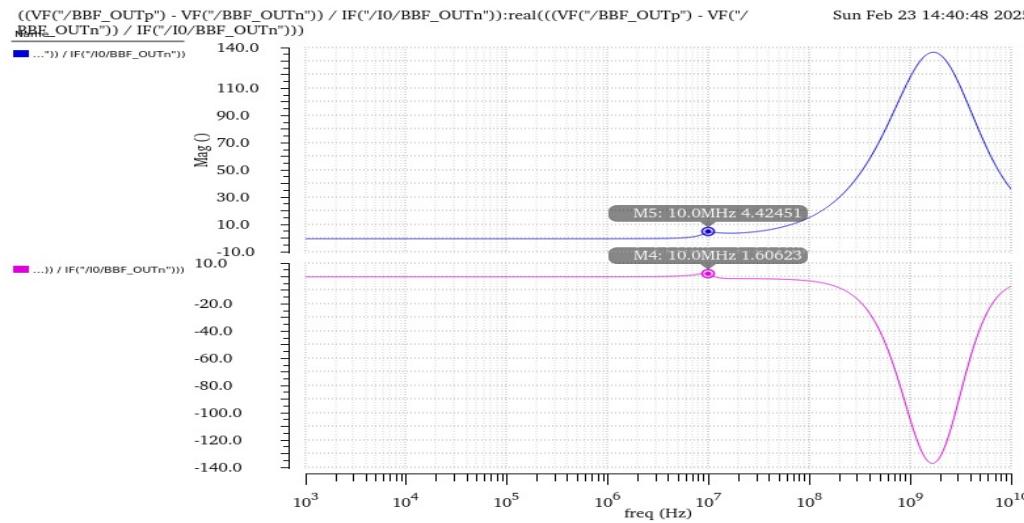
$$I_{R_{DL}} + I_{C_{gg}} = I_{AC}$$

$$R_{DL} \cdot 0.04 + \frac{1}{2\pi f L_{gg}} \cdot 0.96 = 1$$

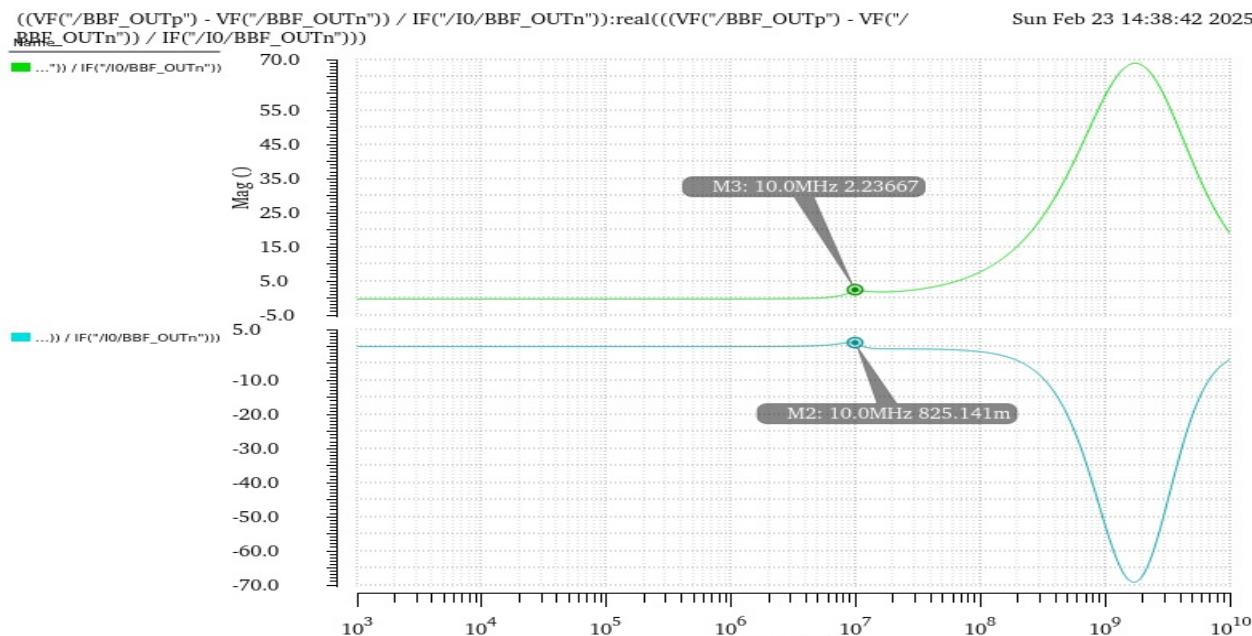
$$R_{DL} = 10.44k \approx 11k.$$

Question 1: Design of the Tx UpC – Step 12

- Step 12: Simulate and measure the output impedance of the Tx BBF. Scale the last stage opamp in the Tx BBF by 2x (to drive the UpC). Simulate and measure the output impedance of the Tx BBF. Comment on how the real part of the impedance changes by scaling the final opamp in the BBF.



before scaling



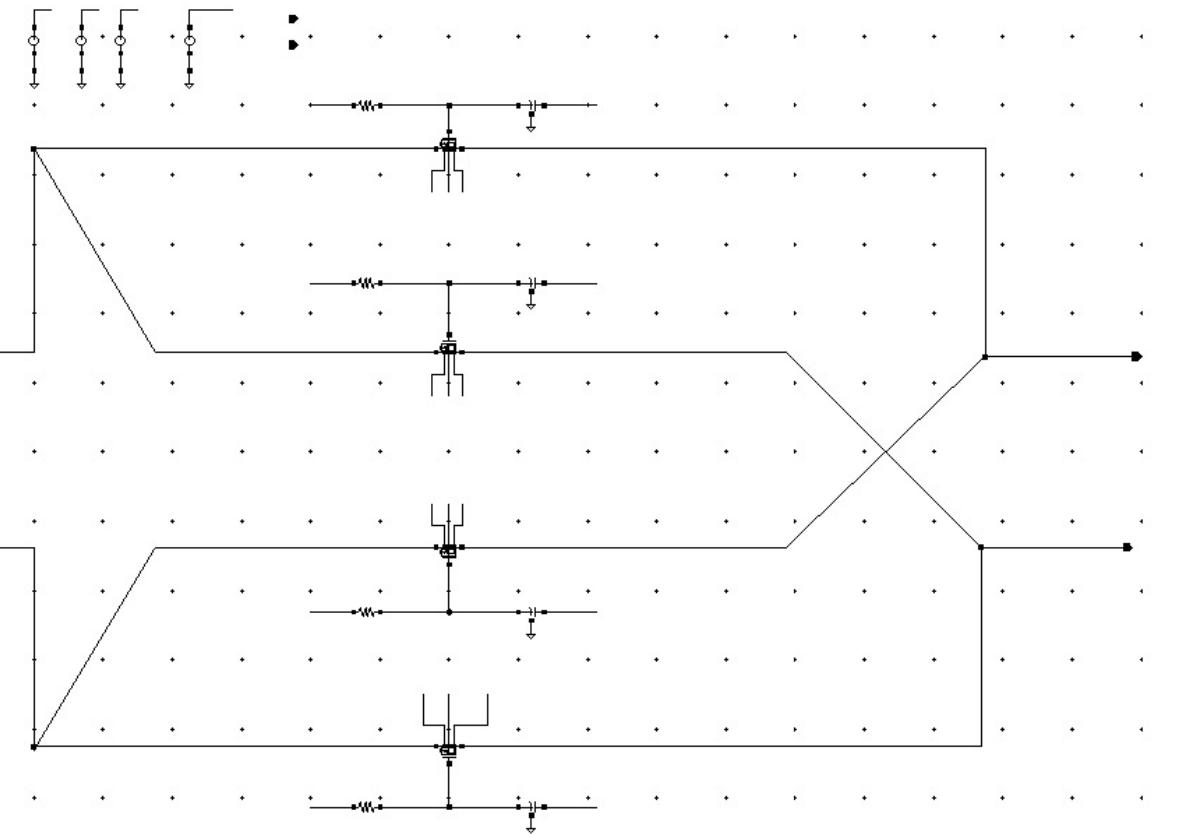
after scaling

Real part of the impedance
decrease due to increasing of
drive ability.

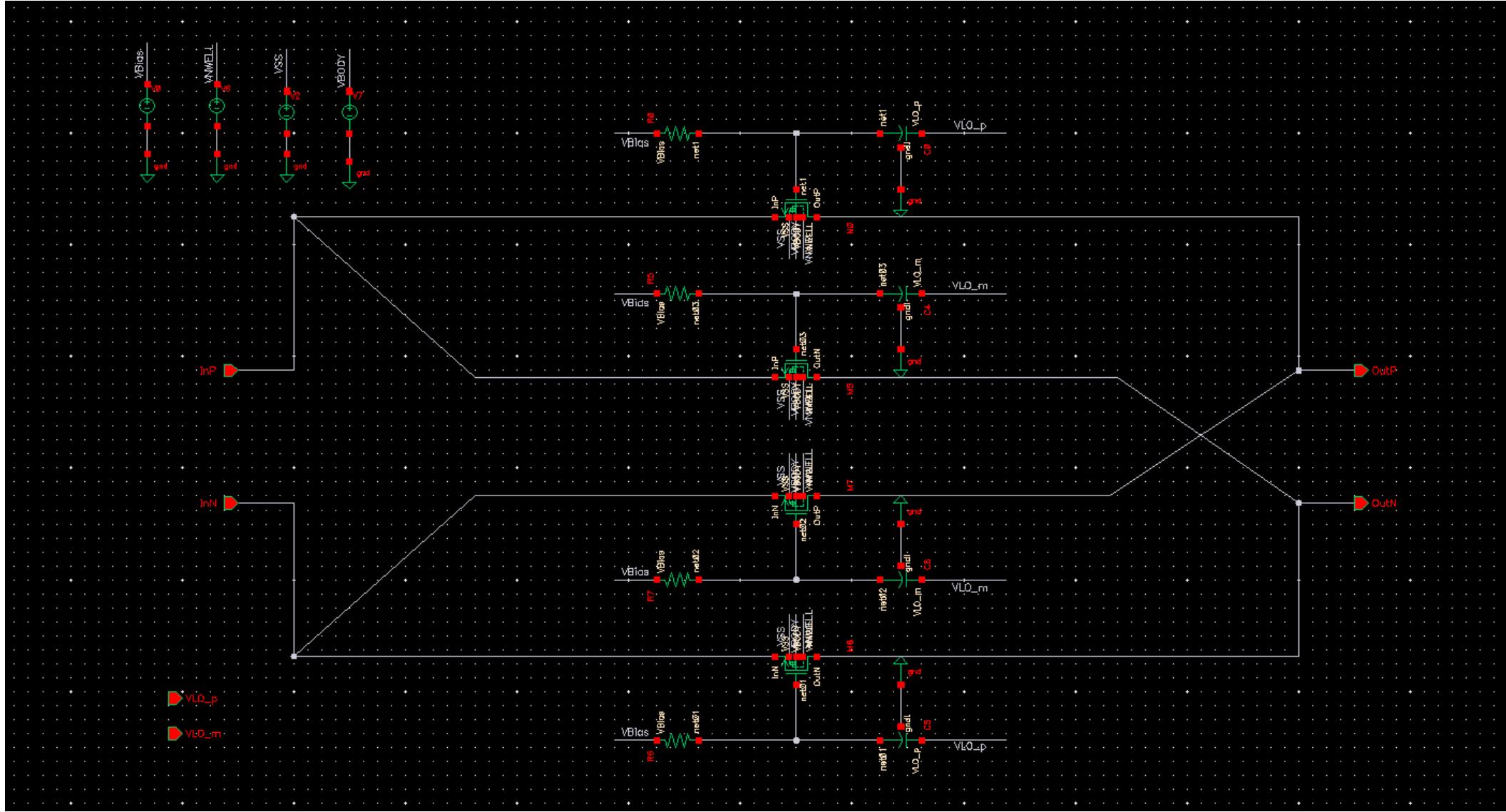
Question 1: Design of the Tx UpC Step 13

- Step 13: Using the results in steps 1 – 11 build the schematics of a double balanced passive UpC using: (include a screen shot)
 - PDK components for transistors, capacitors and resistors,
 - For modelling inputs and output use ideal components for resistors and caps
 - Ideal voltage/current sources for biasing
 - UpC input source: Tx BBF modelled as voltage source in series with a resistance to model the Tx BBF from step 12
 - UpC output load: DA modelled as 60fF capacitor

$$\frac{825}{2} = 412.5$$

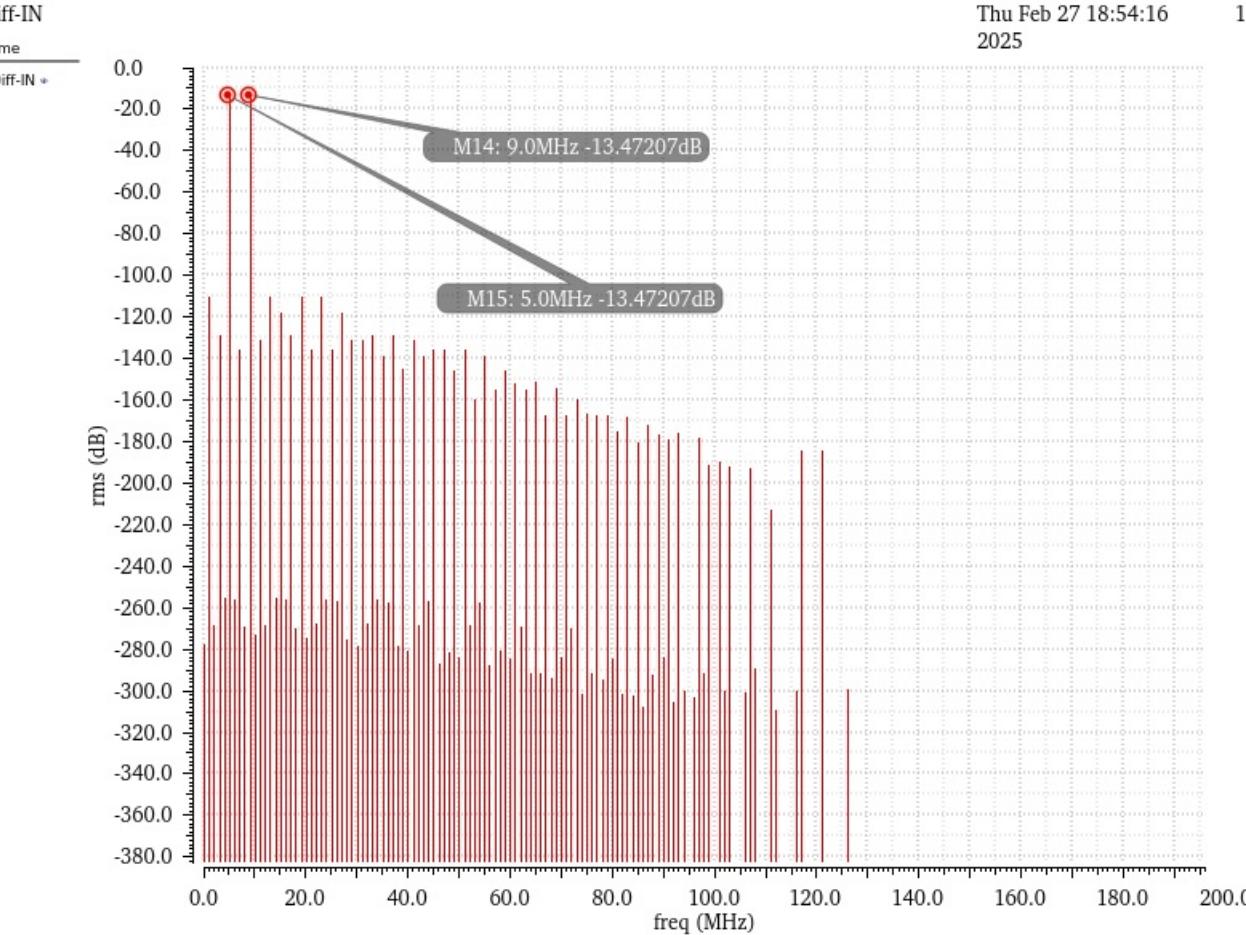


Schematics of the Upconverter (UpC)



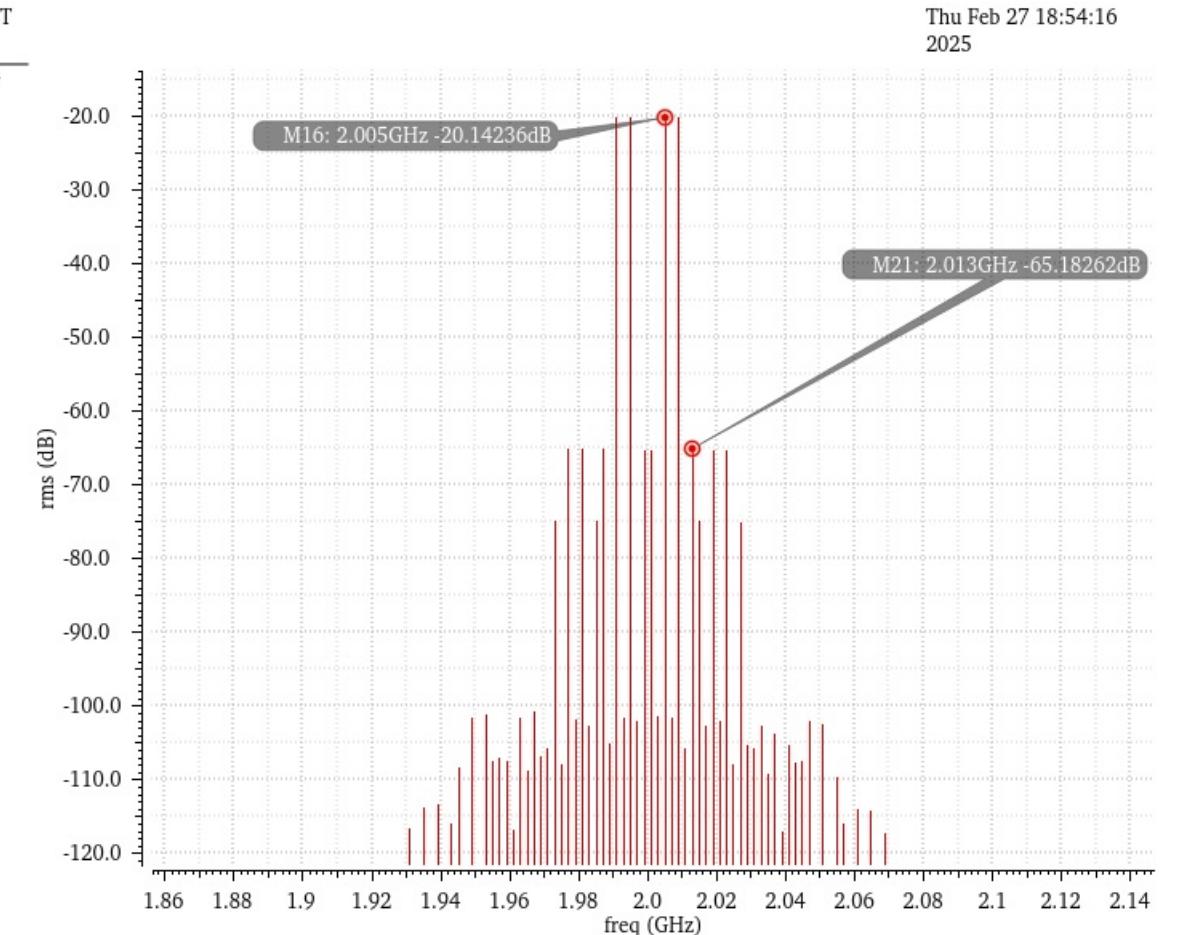
Question 1: Design of the Tx UpC Step 14

- Step 14: Simulate the UpC schematics in step 13 and measure: (HB)
 - Differential Input Voltage Spectrum



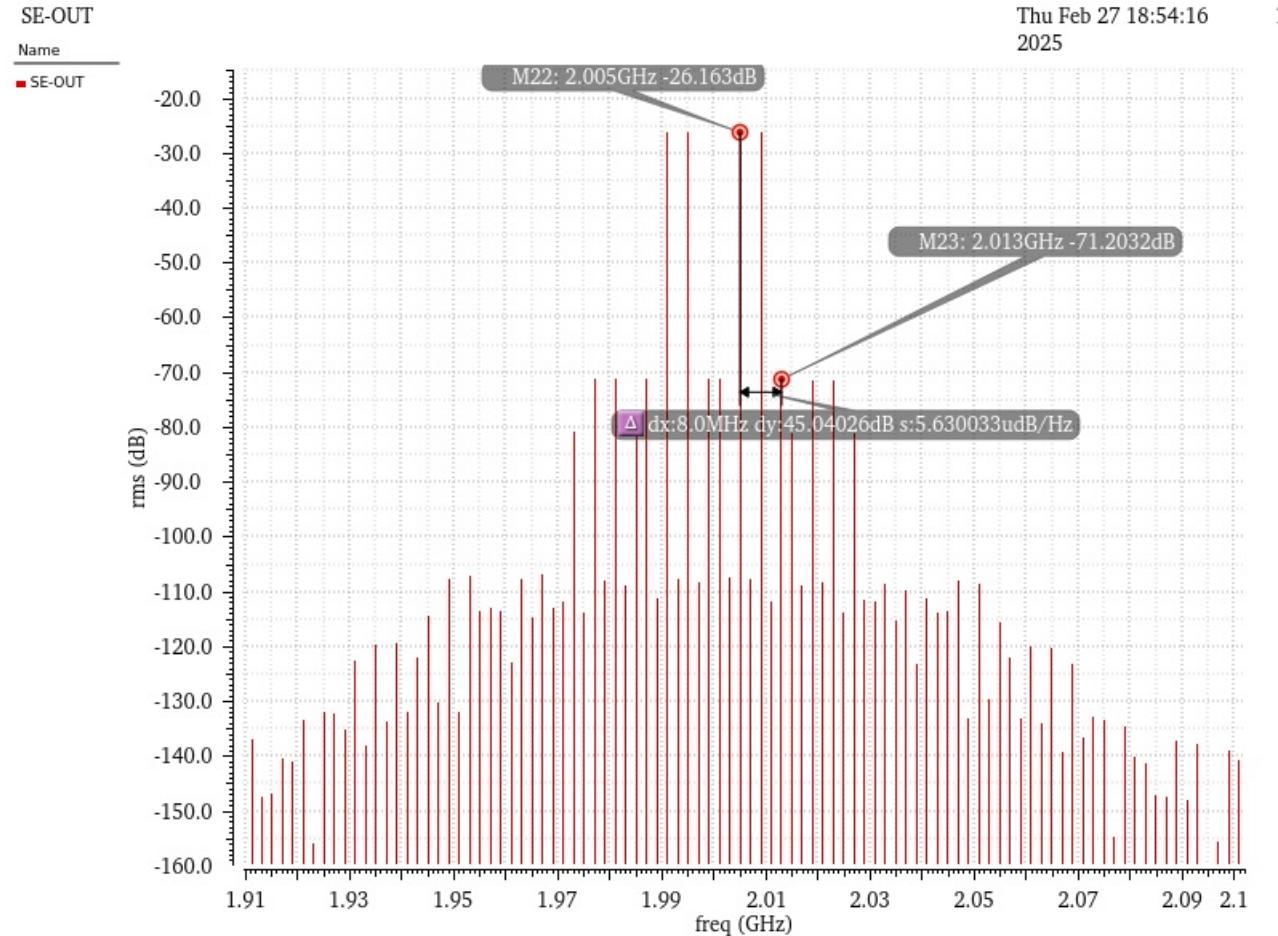
Question 1: Design of the Tx UpC – Step 14

- Step 14: Simulate the UpC schematics in step 13 and measure: (HB)
 - Differential Output Voltage Spectrum



Question 1: Design of the Tx UpC –Step 14

- Step 14: Simulate the UpC schematics in step 13 and measure: (HB)
 - Single-Ended Output Voltage Spectrum



Question 1: Design of the Tx UpC – Step 14

- Step 14: Simulate the UpC schematics in step 13 and measure: (HB)

○ Input tone – Baseband: -13.5 dB Diff in

○ Input tone – RF: -20 dB Diff in

○ Voltage Gain/Loss (Differential): $-20.14 + 13.5 = -6.64 \text{ dB}$

○ HDR3/IMR3 (Differential)

○ HDR3 (5MHz tone): 54.6 dB (@ 2.015 GHz)

○ HDR3 (9MHz tone): 54.7 dB (@ 2.027 GHz)

○ IMR3 (13MHz tone): 45 dB

○ IMR3 (1MHz tone): 45 dB

○ HDR2/IMR2 (Single Ended)

○ HDR2 (5MHz tone): 209 dB 2.01G

○ HDR2 (9MHz tone): 209 dB 2.018

○ IMR2 (14MHz tone): 187 dB

○ IMR2 (4MHz tone): 187 dB

○ In-Band-SDR: 45 dB

○ ACLR: 45 dB

Question 2: Design of the Tx DA

- Step 1: Determine the gate bias voltage of the CS NMOS input transistor to ensure a minimum overdrive voltage of 100mV in presence of the input voltage swing of 200mV (single-ended peak).

$$v_{th\text{-NMOS}} - v_t = 500\text{mV}$$

$$V_{out\min} = V_{GS} - V_{th}$$

$$100\text{ mV} = V_G - V_{swing} \xrightarrow{200\text{mV}} 0 - 500\text{ mV}$$

$$V_G = 800\text{ mV}$$

Question 2: Design of the Tx DA

- Step 2: Determine the drain voltage of the CS NMOS input transistor to ensure that the CS NMOS input transistor is in saturation at maximum input voltage swing of 200mV (single-ended peak). Ensure that the NMOS input transistor is at least 100mV away from the edge of saturation.

$$V_{DS} \geq V_{DD} + 100mV$$

$$V_D \geq 800mV + 200mV - V_t + 100mV$$

$$V_D \geq 600 \text{ mV}$$

Question 2: Design of the Tx DA

- Step 3: Assume that the size of the cascode NMOS transistors is the same as the CS NMOS transistor, determine the gate bias voltage of the cascode to ensure CS NMOS input transistors remains in saturation at maximum input voltage swing of 200mV.

$$V_{G_cas} = V_{Dmin} + V_{Dmin} + V_t = 600m + 600m + 560m$$

\swarrow
thick-oxide
NMOS

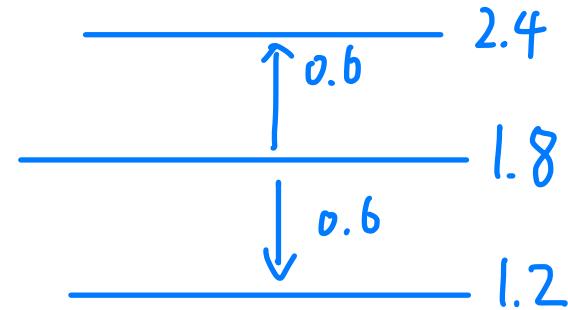
$$= 1.76V$$

$$V_{G_cas} = 1.76V$$

Question 2: Design of the Tx DA

- Step 4: Assume a supply voltage of 1.8V, determine the maximum voltage swing at the drain of the cascode NMOS transistor to ensure it stays in saturation at maximum input voltage swing of 200mV (single-ended peak).

$$V_{D_swing} = 1.8 - 0.6 - 0.6 = 0.6 \text{ V}$$



Question 2: Design of the Tx DA

- Step 5: Assume that 50% of the power is lost in the DA, determine the power generated by the DA in mW to deliver +6dBm to a to an external 50 Ohm load.

Because it's differential . 2x Power is delivered.

$$6\text{dBm} = 4\text{mW} \rightarrow \text{from Diff DA}$$
$$\downarrow \div 2$$

$$2\text{mW} \rightarrow \text{from SE}$$
$$\downarrow 50\% \text{ Loss}$$

4mW → SE DA generated.

6dBm

Question 2: Design of the Tx DA

- Step 6: Using the information in step 5, determine the current swing (SE Peak) at the drain node of the cascode stage of DA.

$$P_L = \frac{1}{2} V_{max} I_{max}$$

$$V_{max} = 0.6 \text{ V}$$

$$I_0^{\frac{6}{10}} m = \frac{1}{2} \cdot 0.6 \cdot I_{max}$$

$$I_{max} = 13.27 \text{ mA}$$

Question 2: Design of the Tx DA

- Step 7: Bias current in the CS NMOS transistor is 30% higher than the current swing determined in step 6 (driven by linearity requirements). Determine the DC bias current in each branch of the differential CS NMOS DA.

$$I_{Bias} = 13.2 \text{ mA} \cdot 1.3 = 17.25 \text{ mA}$$

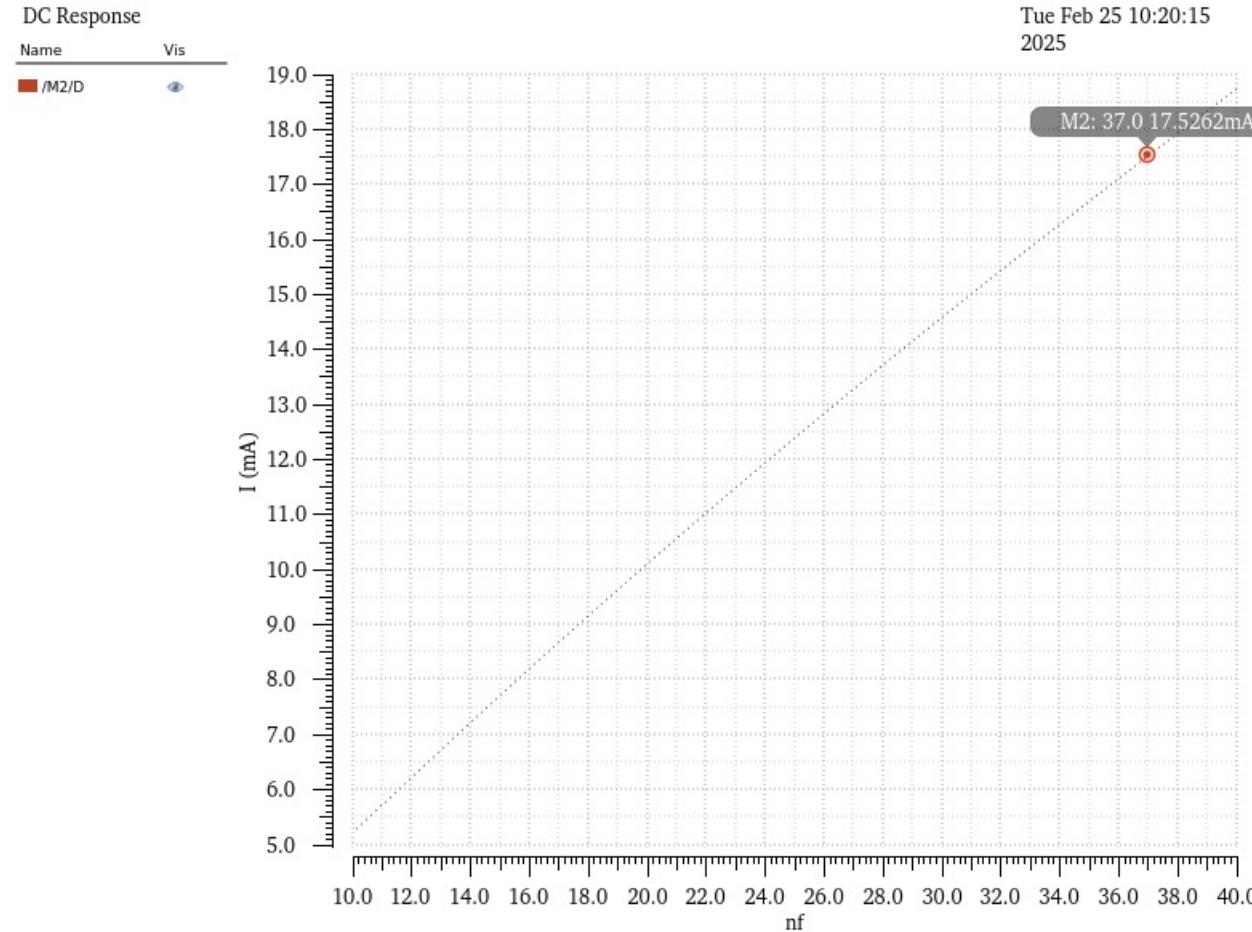
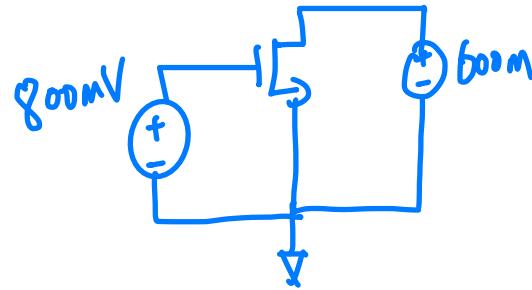
Question 2: Design of the Tx DA

- Step 8: Using the voltage swing in step 4 and current swing in step 6, determine the load line resistance.

$$R_{\text{load, opt}} = \frac{V_{\text{max}}}{I_{\text{max}}} = \frac{0.6}{13.27 \text{ mA}} = 45 \Omega$$

Question 2: Design of the Tx DA

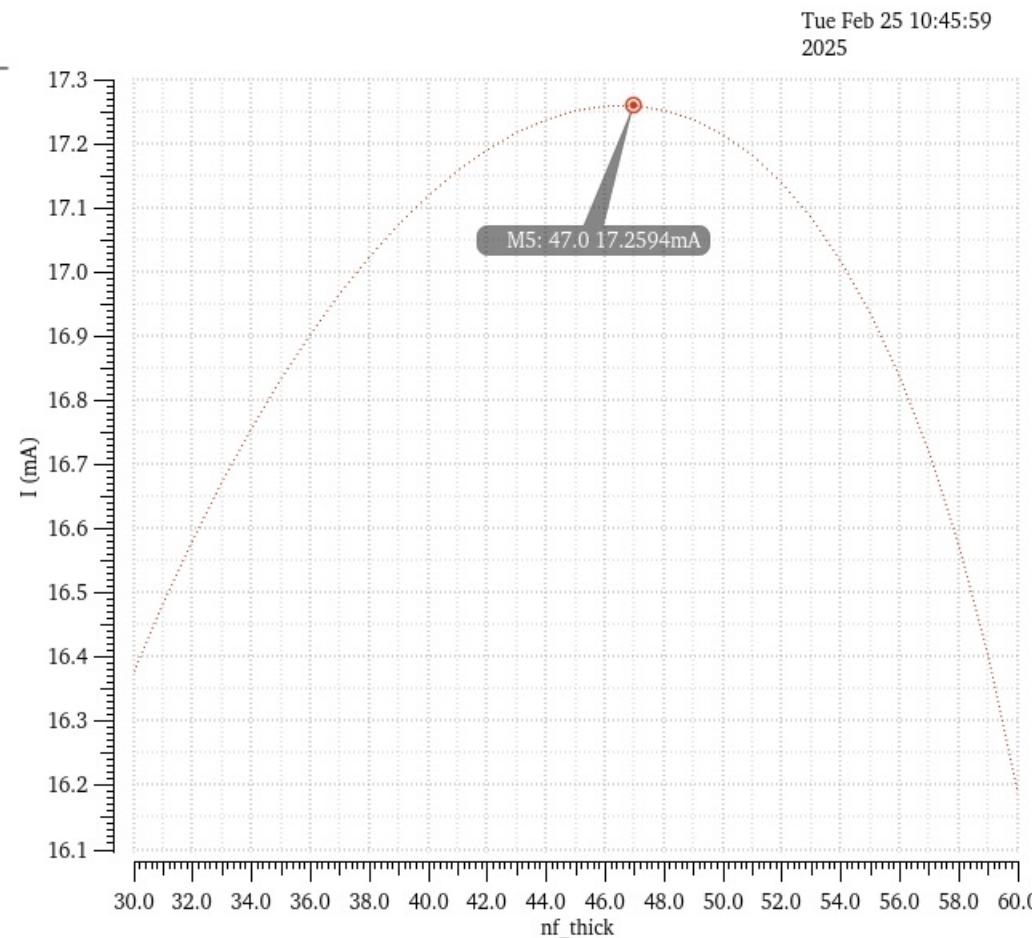
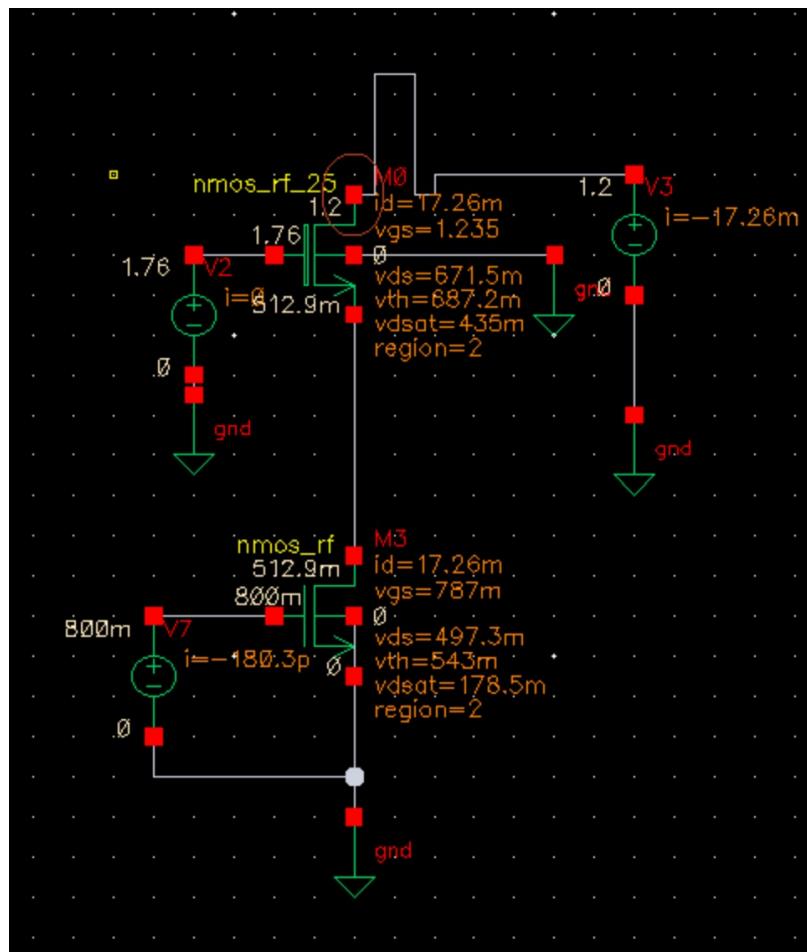
- Step 9: Using the information in step 1 (gate bias voltage) and step 7 (DC current), determine the size (N_f) of the CS NMOS input transistor ($L = L_{min}$, $W_f = 3\mu m$, N_f).



$N_f = 37$

Question 2: Design of the Tx DA

- Step 10: Assume the use of a thick-oxide transistor for the cascode. Determine the size ($L = L_{min}$, $W_f = 4\mu m$, $N_f?$) of the cascode transistor to meet the same overdrive voltage requirements as the CS NMOS input transistor.



N_f_thick
= 47

Question 2: Design of the Tx DA

- Step 11: Determine AC coupling capacitance at the input of the CS NMOS transistors to ensure >95% of the input signal gets coupled to the CS NMOS input transistor.

$$C_{gg_nmos_in} = 103.22 \text{ f}$$

$$\frac{\frac{1}{C_{gg}} + \frac{1}{C_{AC}}}{\frac{1}{C_{gg}}} > 0.95 \Rightarrow C_{AC} = 2 \text{ pF}$$

Question 2: Design of the Tx DA

- Step 12: Determine DC bias resistance used to bias the CS NMOS transistors to ensure < 5% of the input signal gets wasted in the bias resistor.

5

$$0.05 \cdot R_{bias} + 0.95 \cdot \frac{1}{2\pi f L_{gg}} = 1$$

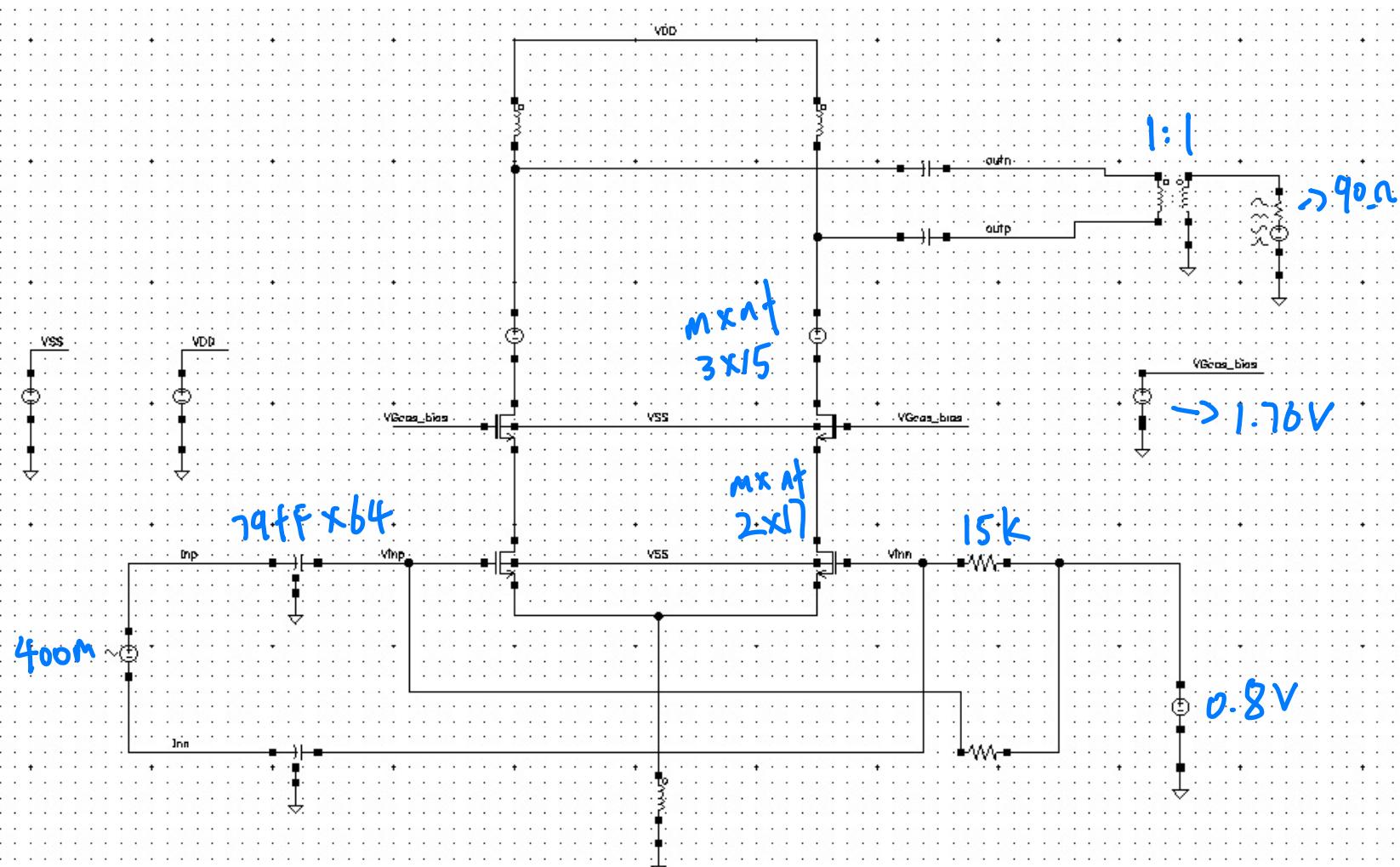
$$f = 2.005 \text{ GHz}$$

$$R_{bias} = 14.6 \text{ k}\Omega$$

Question 2: Design of the Tx DA

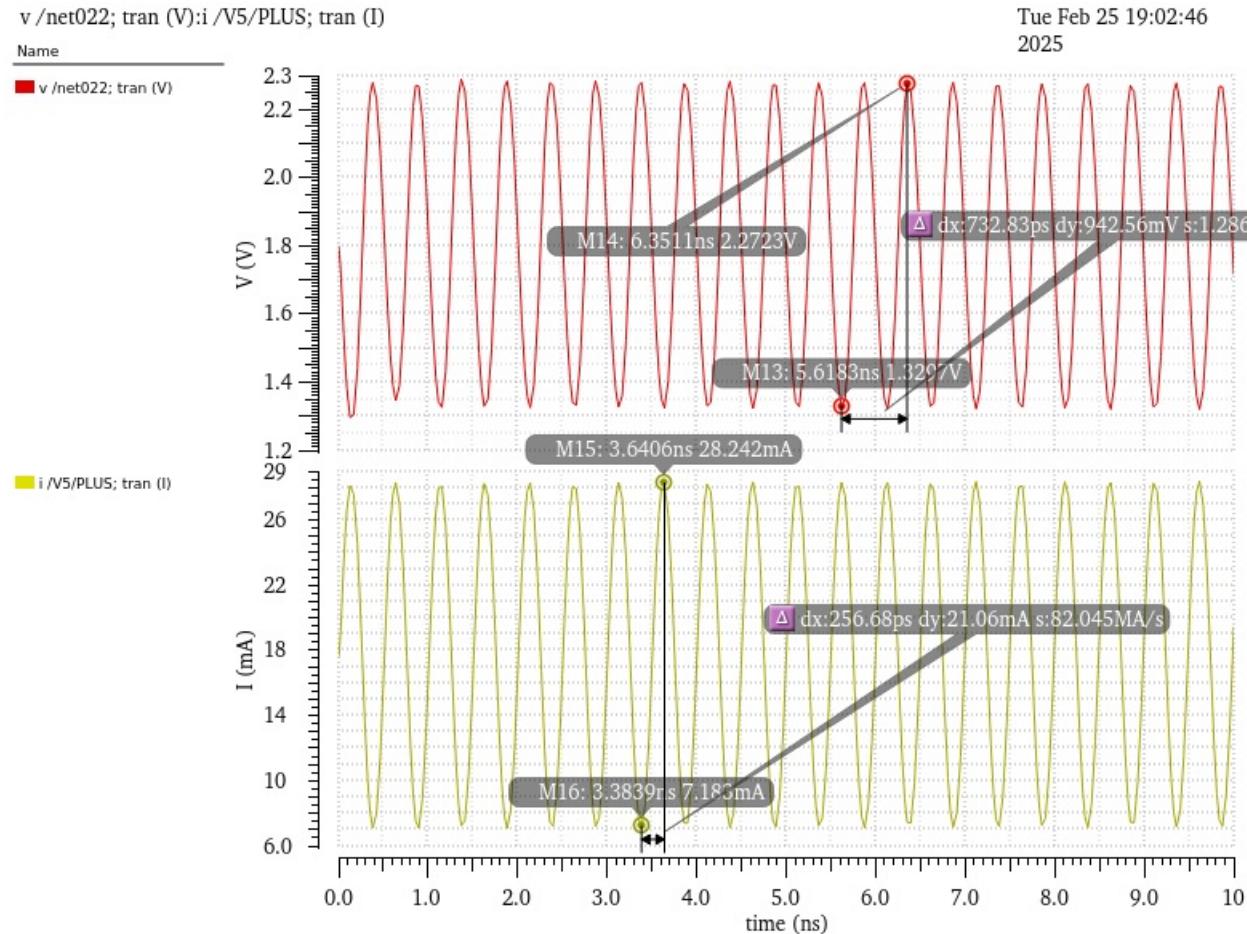
- Step 13: Using the results in steps 1 – 12 build the schematics of a driver amplifier using: (include a screen shot). Modify the gate bias voltage of the cascode and device widths as necessary to meet the specifications laid out in Step 2 (drain bias voltage) and Step 7 (bias current)

- PDK components 1
- Ideal voltage/curre
- DA input source: I
- DA output load: R_L
- 100nH ideal induct
- 100pF ideal AC co
- Use nmos_rf_25 fc



Question 2: Design of the Tx DA

- Step 14: Simulate the DA and compare the DC current in step 7, Single ended AC current swing in step 6, and Single ended Voltage swing in Step 4.



SE - Voltage = 471mV

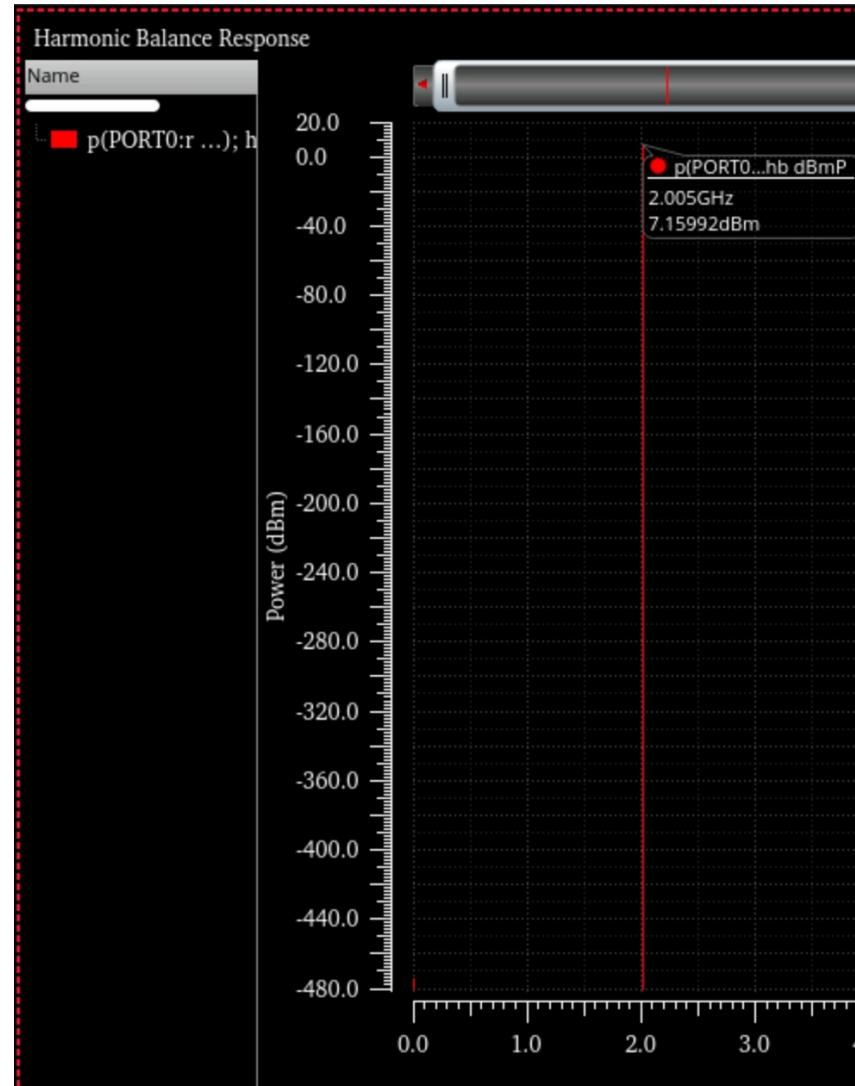
SE - Current = 10.5mA

DC - Current = 17.66mA

Name/Signal/Expr	Value	Plot
1 v /net022; tran (V)	wave	<input checked="" type="checkbox"/>
2 i /V5/PLUS; tran (I)	wave	<input checked="" type="checkbox"/>
3 IDC("/M1/D")	17.66m	<input checked="" type="checkbox"/>

Question 2: Design of the Tx DA

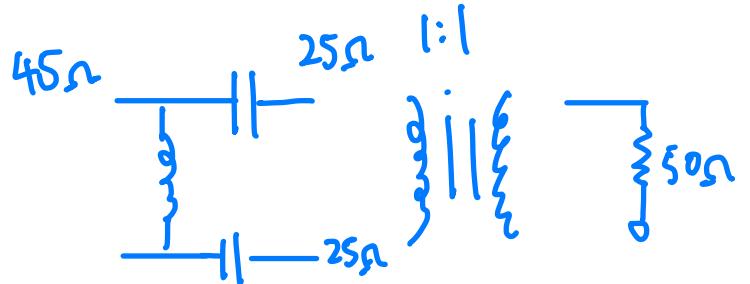
- Step 15: Simulate and measure the output power delivered to the load.



7.16 dBm

Question 2: Design of the Tx DA

- Step 16: Calculate the inductance and capacitance required to convert the optimal load line resistance (differential) to 50Ohms.



$$R_S = 45\Omega$$

$$R_L = 25\Omega$$

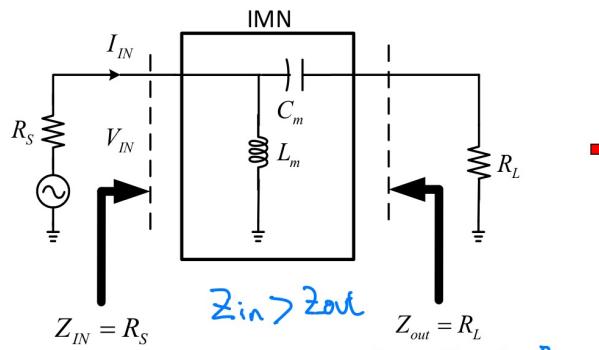
$$\omega = 2\pi \cdot 2.005G$$

In P0k
↑

$$Q_n = 0.89$$

$$L_m = \frac{1}{Q_n} \frac{R_S}{\omega} = 4nH \quad \times 2 = 8nH$$

$$C_m = \frac{1}{Q_n} \cdot \frac{1}{\omega R_L} = 3.56 \text{ pF}$$



$$Z_{in} > 2R_L$$

$$Q_n = \sqrt{\frac{R_S - R_L}{R_L}}$$

Up from R_L to R_S

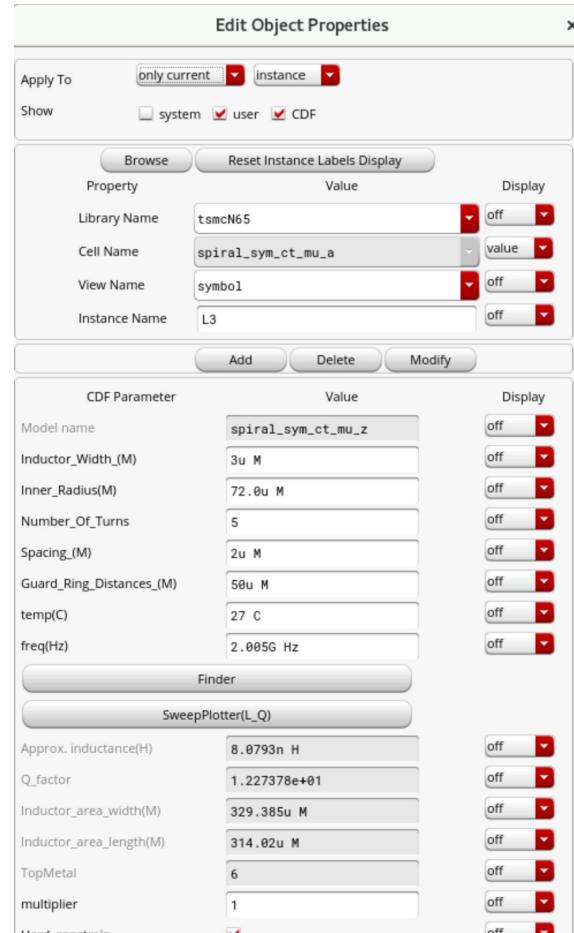
$$L_m = \frac{R_S R_L}{\omega \sqrt{R_L (R_S - R_L)}} = \frac{1}{Q_n} \left(\frac{R_S}{\omega} \right)$$

$$C_m = \frac{1}{\omega \sqrt{R_L (R_S - R_L)}} = \frac{1}{Q_n} \left(\frac{1}{\omega R_L} \right)$$

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Question 2: Design of the Tx DA

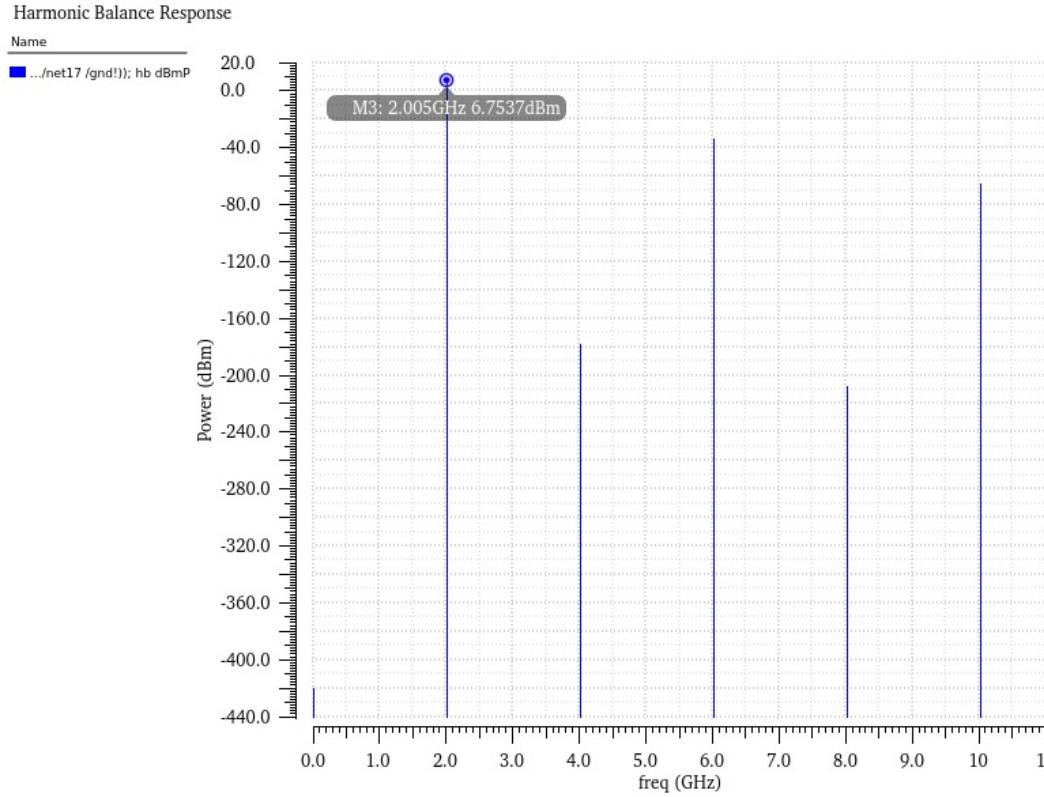
- Step 17: Replace the ideal inductor with a symmetric center tapped PDK inductor with the inductance calculated from Step 16. Replace the ideal capacitor with a PDK capacitor and tune the value in simulation to cancel out the imaginary part of the impedance. Replace the load resistor with a 1:1 ideal transformer to transform into a single ended 50 Ohm port. Report the parameters of the inductor used.



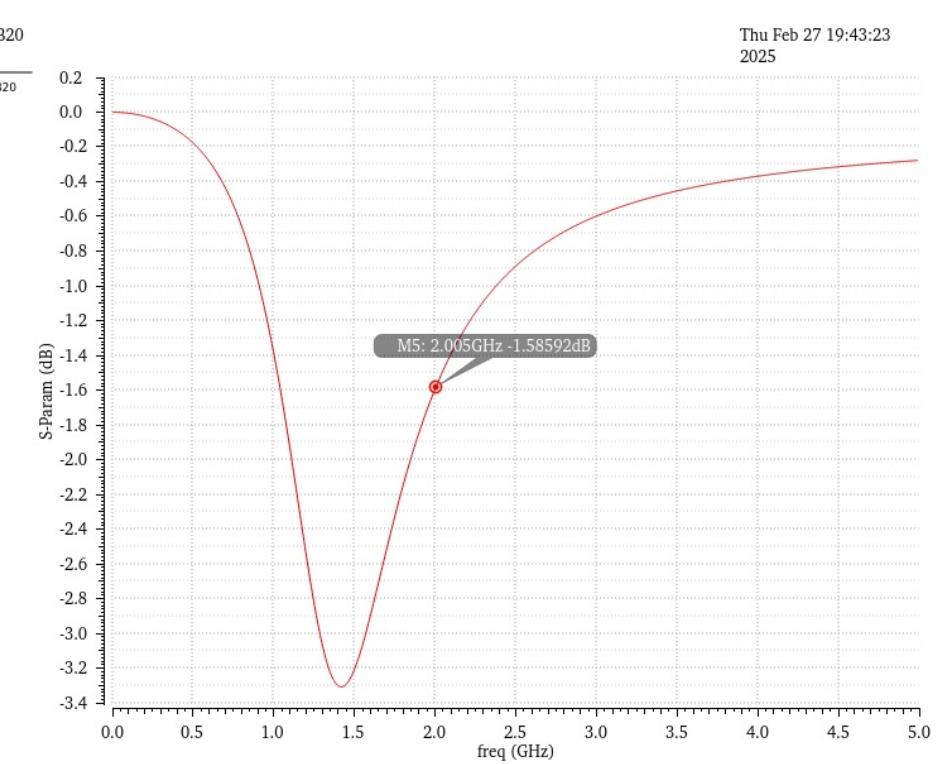
Question 2: Design of the Tx DA

- Step 18: Re-simulate the power delivered to the load. Simulate the output return loss (S_{22}).

Power

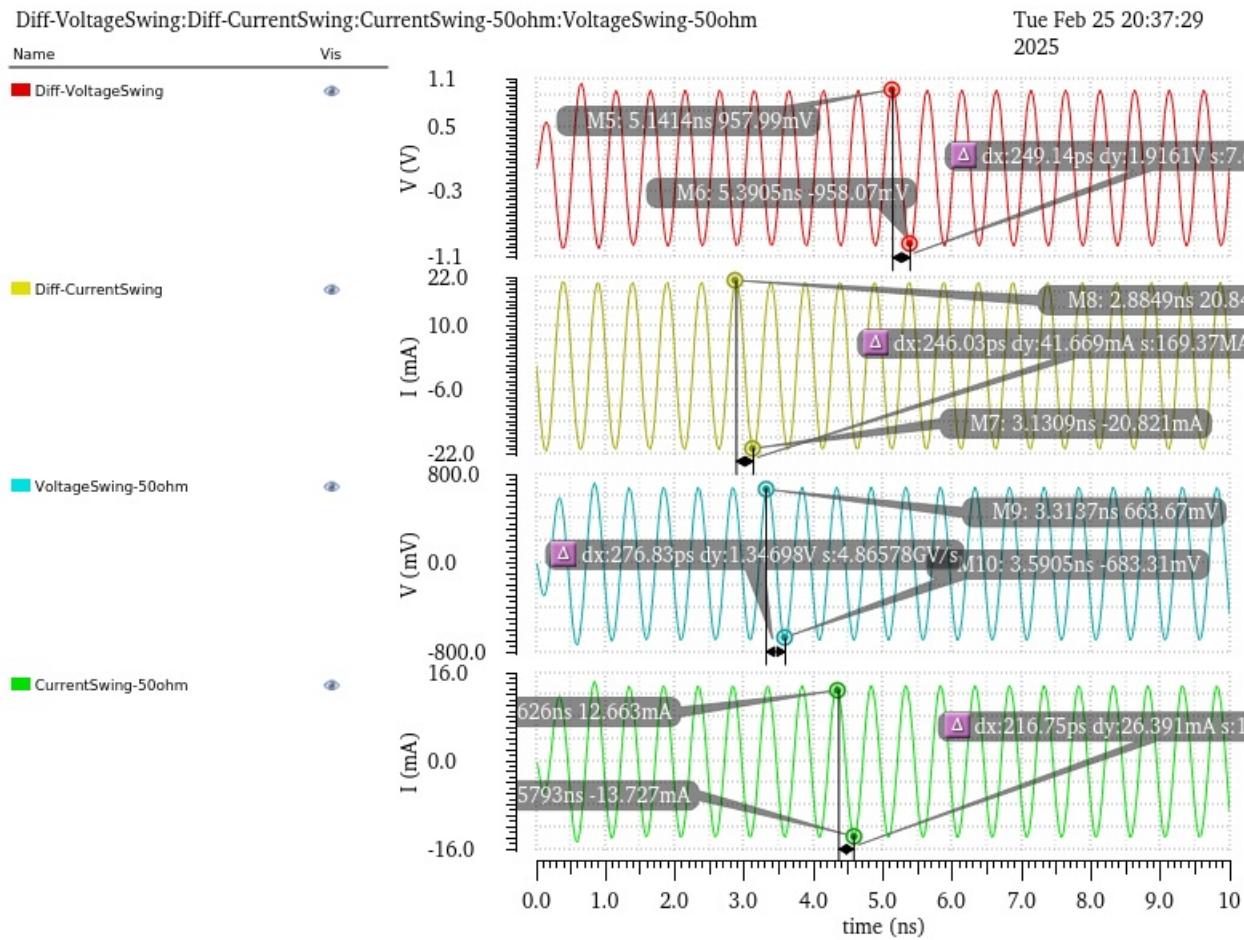


S_{22}



Question 2: Design of the Tx DA

- Step 19: Simulate and measure the Differential current swing, voltage swing at the drain node of the cascode stage of DA and at the 50 ohm load, output power delivered to the 50 ohm load. Optimize the design as necessary.



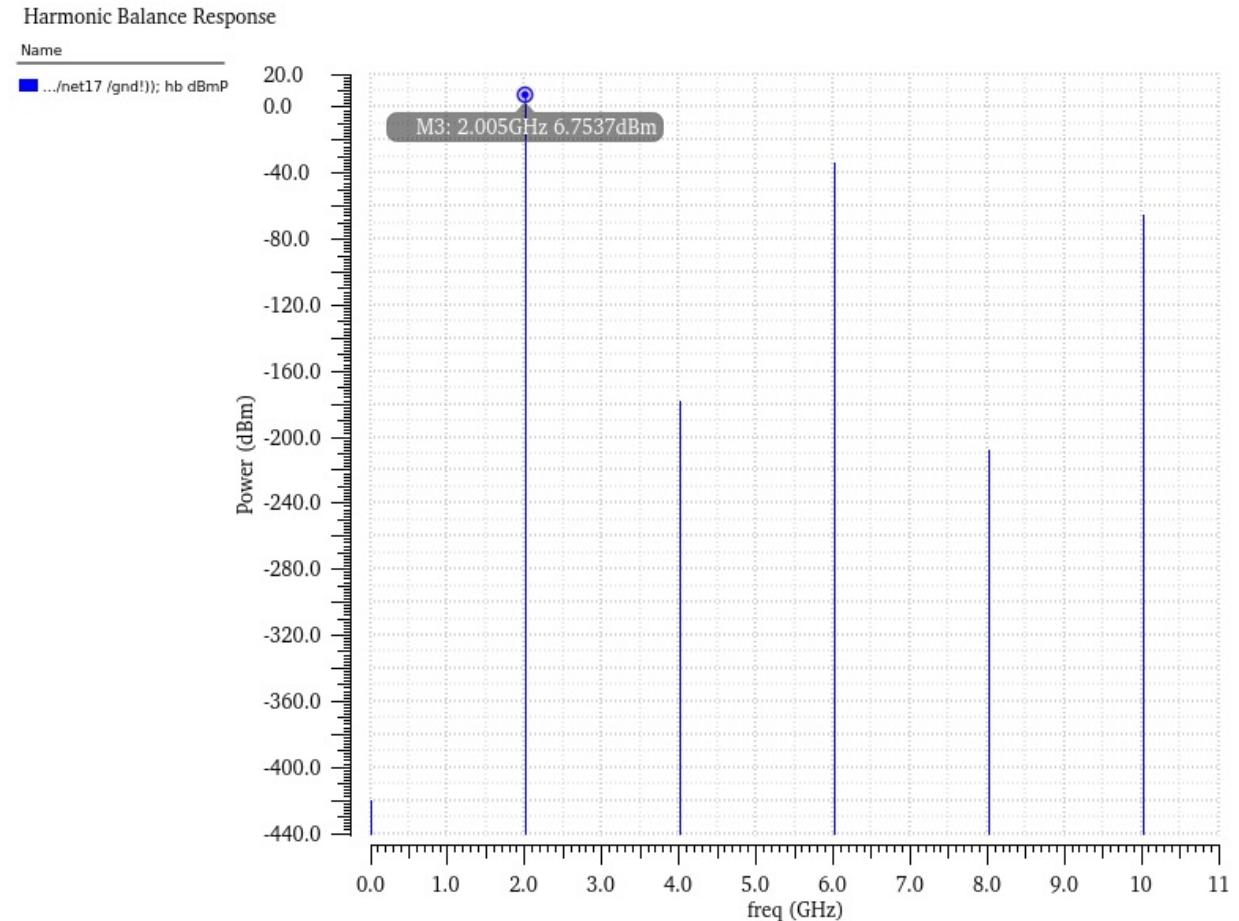
Diff Peak
Voltage swing ~ 958 mV
Current swing ~ 20.8 mA

@ 50 ohm Load Peak
Voltage swing ~ 660 mV
Current swing ~ 13 mA

Question 2: Design of the Tx DA

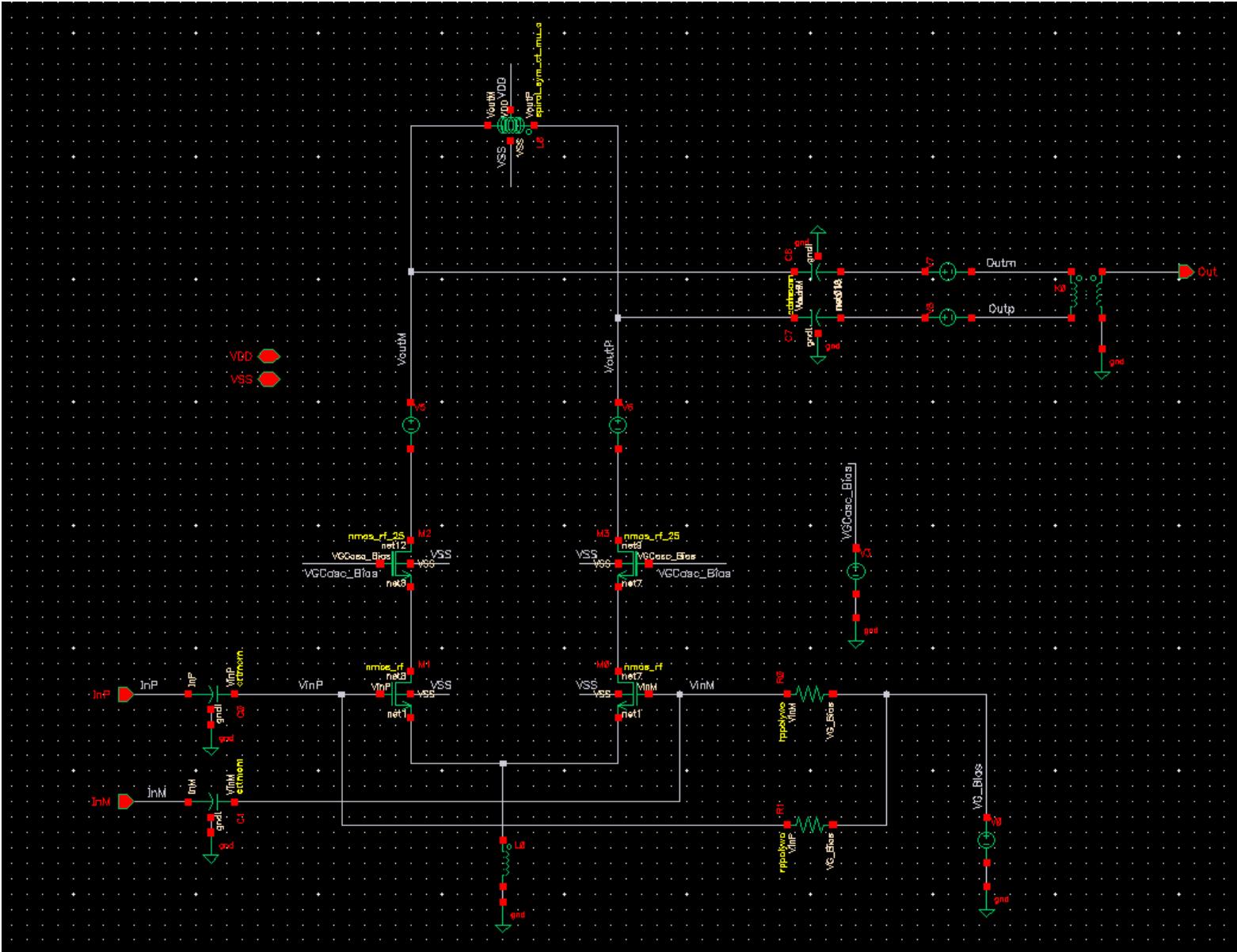
- Step 19: Simulate and measure the Differential current swing, voltage swing at the drain node of the cascode stage of DA and at the 50 ohm load, output power delivered to the 50 ohm load. Optimize the design as necessary.

Output power

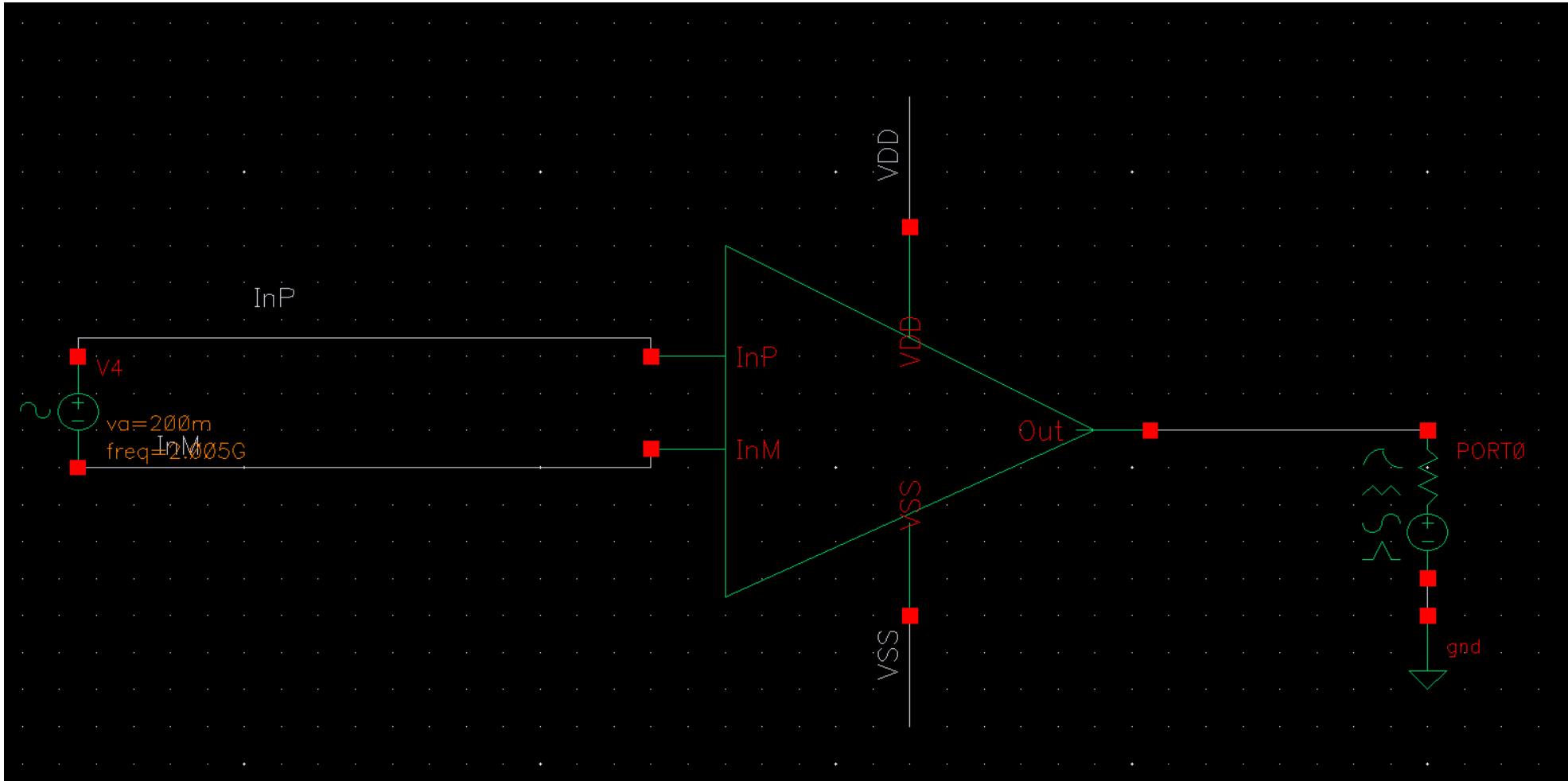


2

Schematics of the Driver Amplifier (DA)

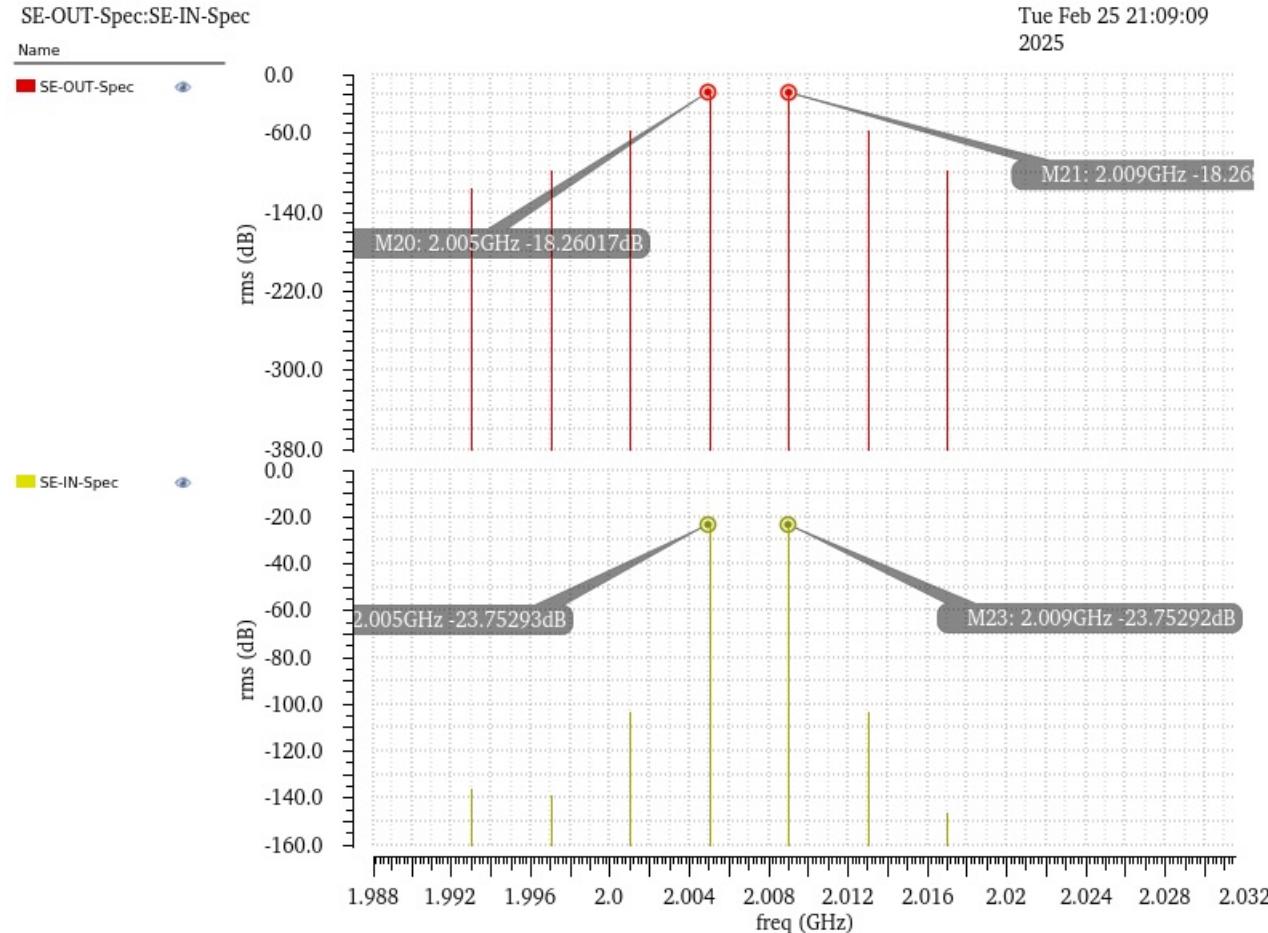


Schematics of the DA Testbench



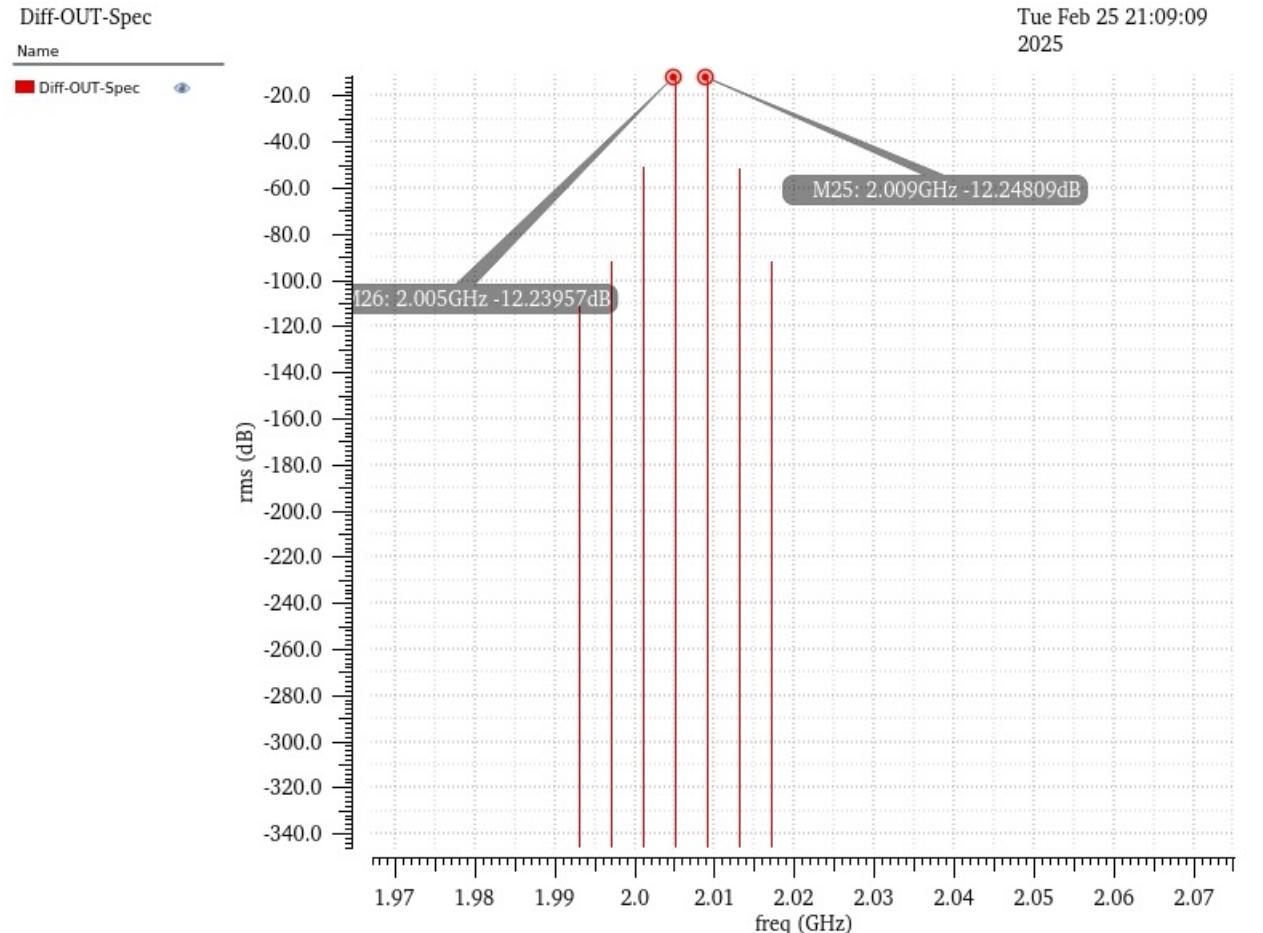
Question 2: Design of the Tx DA

- Step 20: Simulate the DA schematics in and measure:
 - Input/Output Voltage Spectrum(Single-Ended)



Question 2: Design of the Tx DA

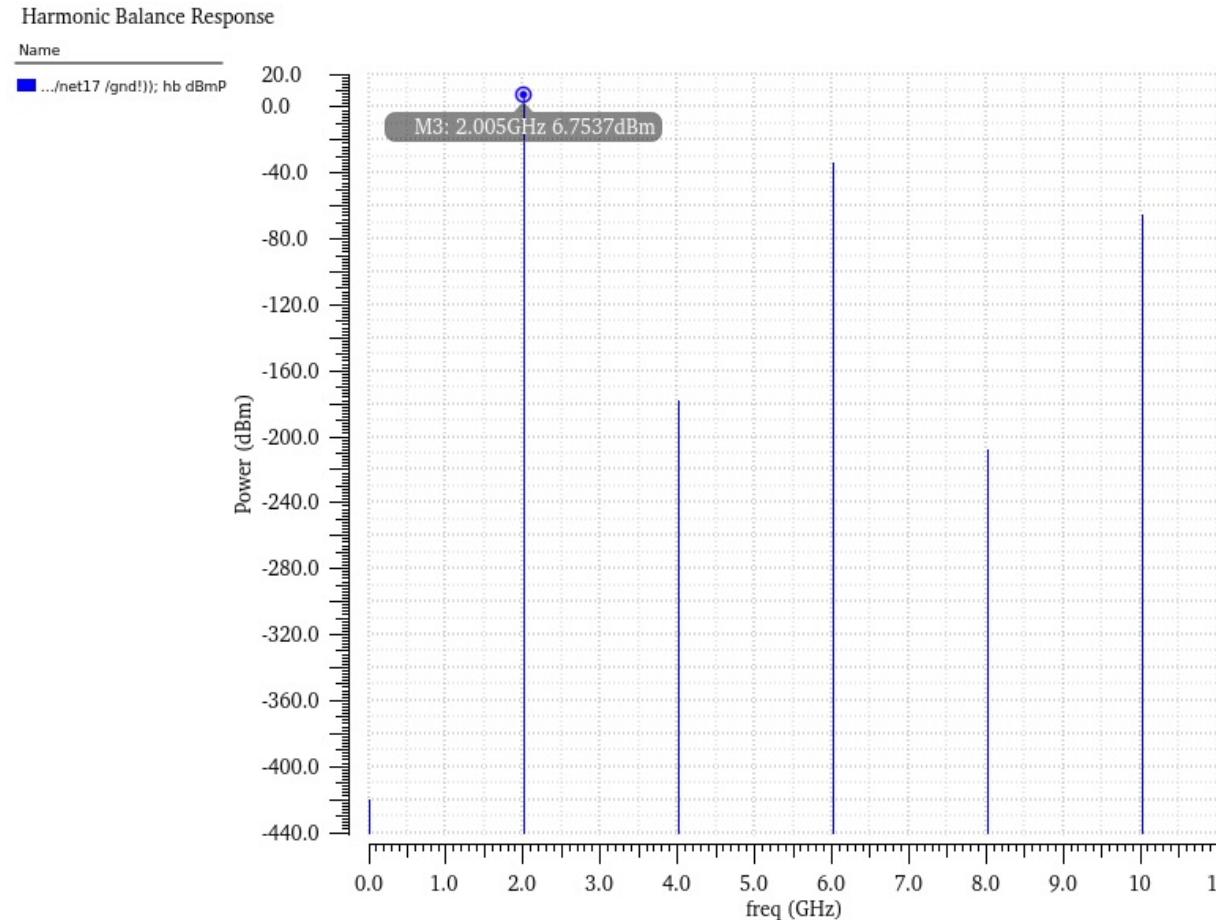
- Step 20: Simulate the DA schematics in and measure:
 - Output Voltage spectrum(Differential)



Question 2: Design of the Tx DA

- Step 20: Simulate the DA schematics in and measure:
 - Output Power Spectrum(Differential)

2



Question 2: Design of the Tx DA

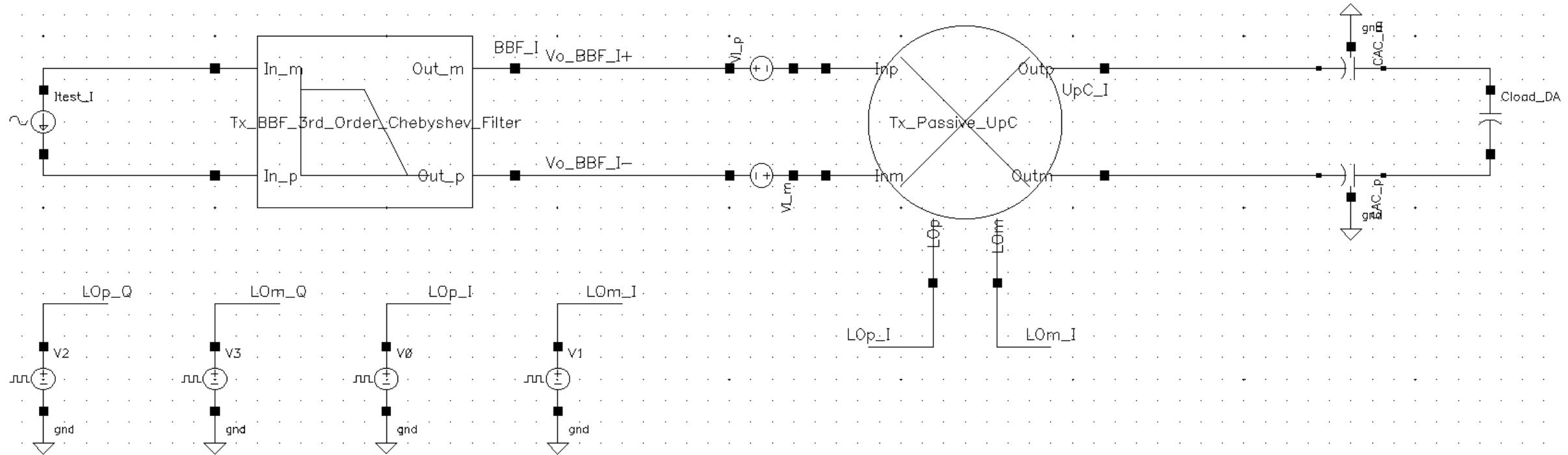
- Step 20: Simulate the DA schematics in and measure:
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2

Voltage Gain	5.5 dB
Output 5MHz Tone	-12.24 dB
Output 9MHz Tone	-12.24 dB.
IMR3	38dB
IMR2	48 dB
SDR	38 dB
ACLR	38 dB
notes if any	

Note: For SDR check maximum distortion In Band while for ACLR is maximum distortion product out of Band

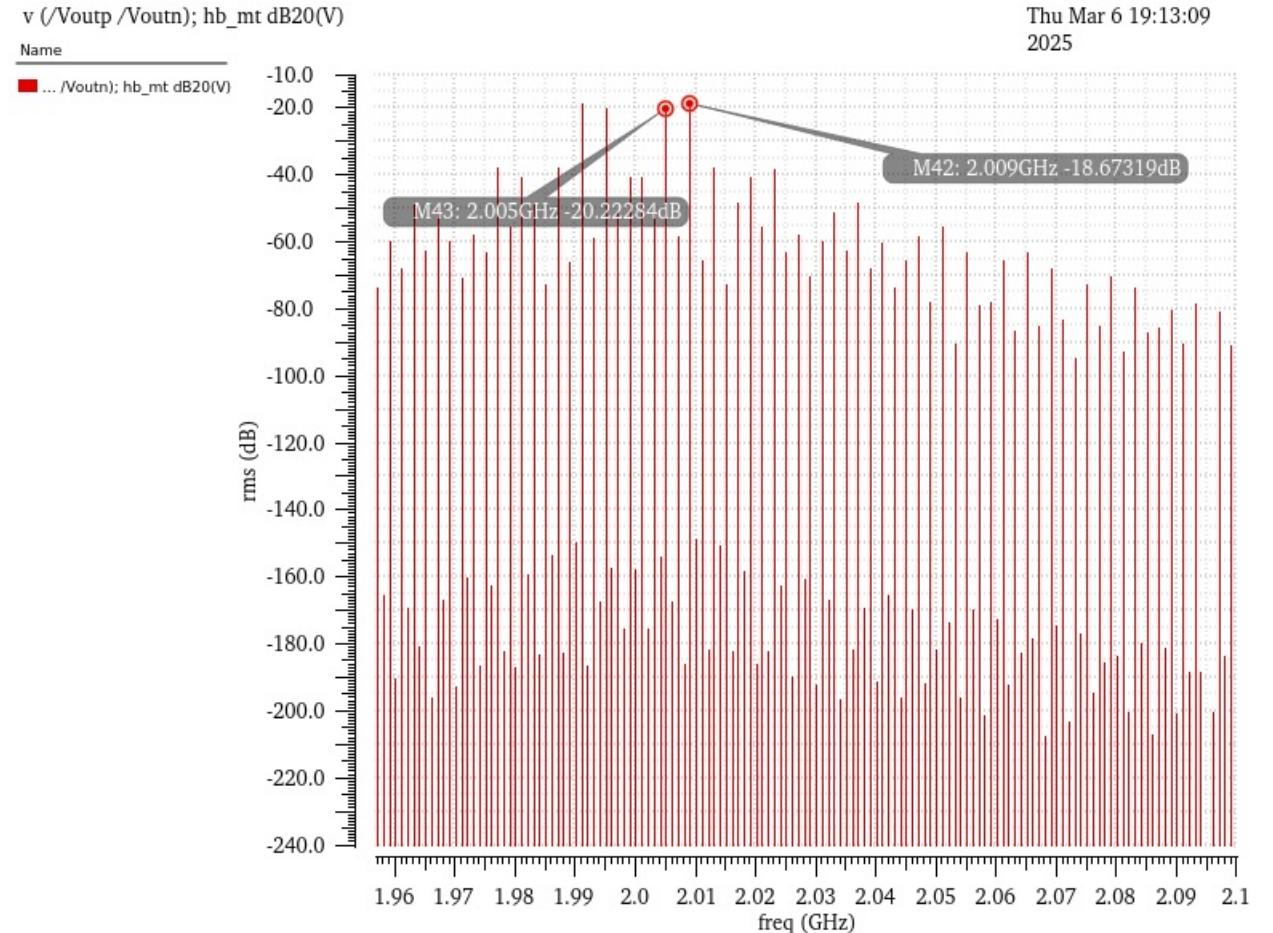
Question 3: Tx BBF + UpC (I-Channel) – Part 1

- Simulate the Tx BBF + UpC and measure: (Input Current = maximum allowed per design)
 - Output voltage (differential)
 - HDR3/IMR3 (differential)
 - HDR2/IMR2 (single-ended) and subtract 30dB for expected differential results
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2



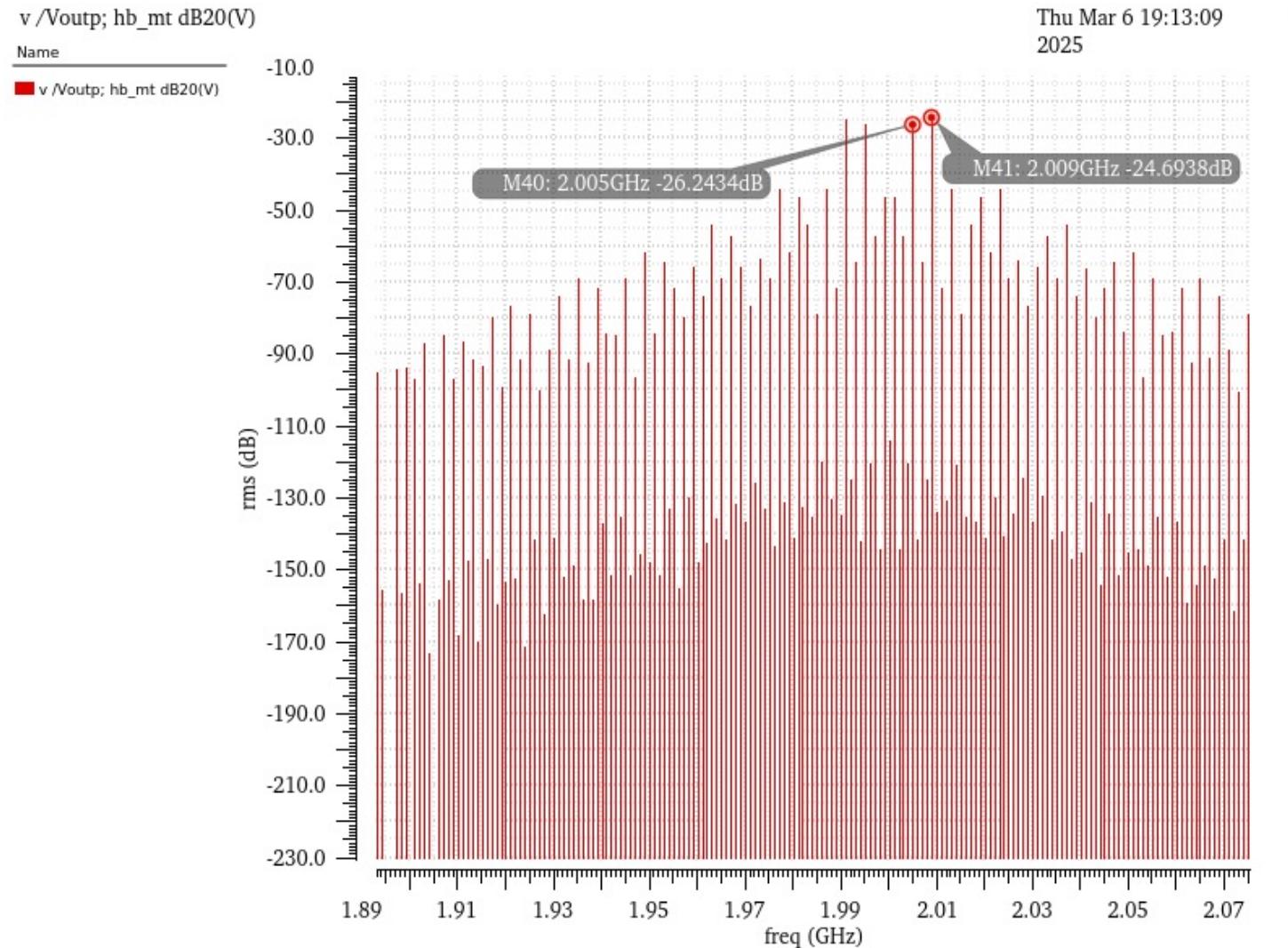
Question 3: Tx BBF + UpC (I-Channel) – Part 1

- Simulate the Tx BBF + UpC and measure: (Input Current = maximum allowed per design)
 - Output Voltage Spectrum (Differential)



Question 3: Tx BBF + UpC (I-Channel) – Part 1

- Simulate the Tx BBF + UpC and measure: (Input Current = maximum allowed per design)
 - Output Voltage Spectrum (Single-Ended)



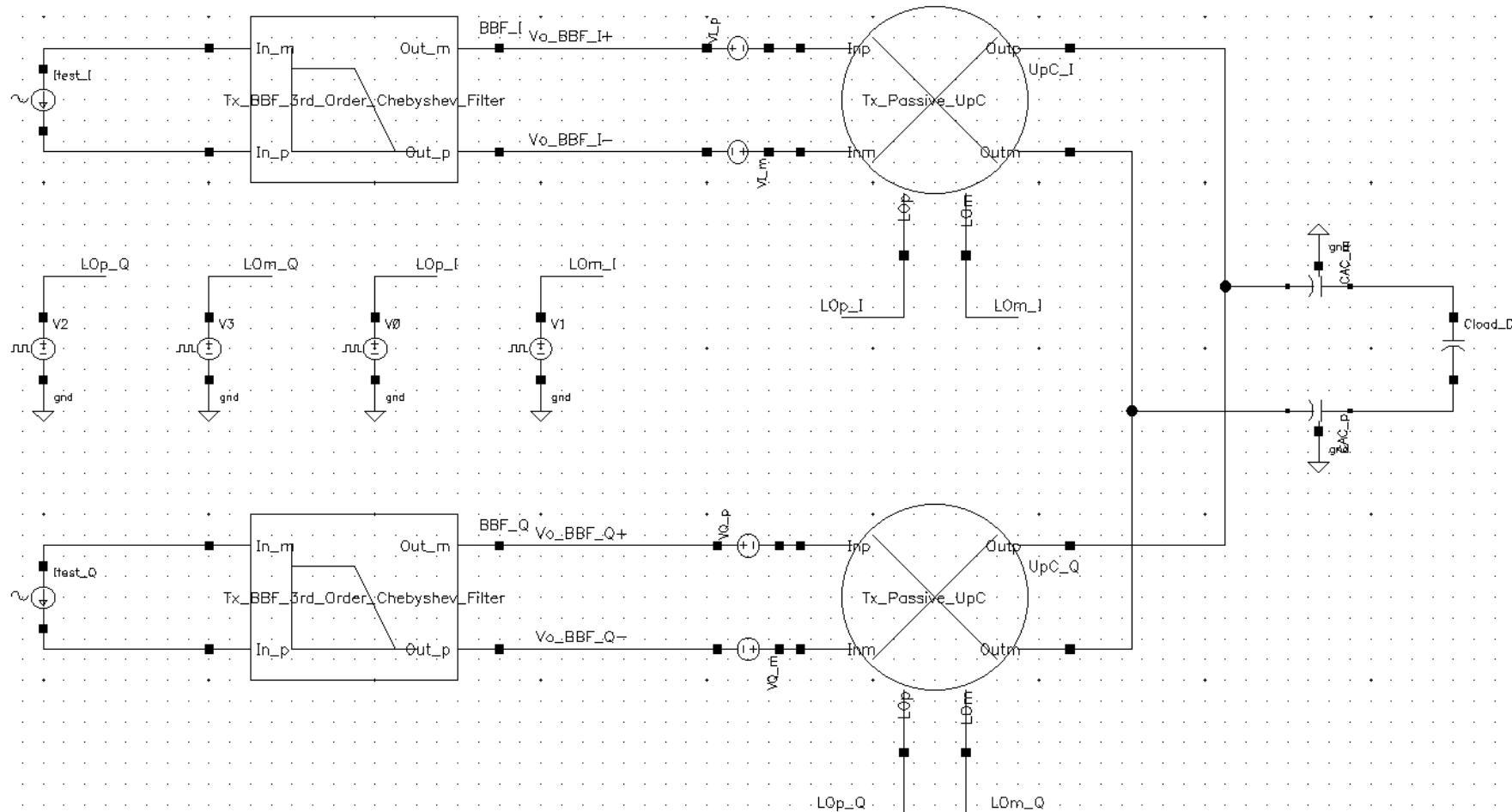
Question 3: Tx BBF + UpC (I-Channel) – Part 1

- Simulate the Tx BBF + UpC and measure: (Input Current = maximum allowed per design)
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2

	Single-Ended Output	Differential Output
Output Signal (5MHz Tone)	-26 dB	-20 dB
Output Signal (9MHz Tone)	-24 dB	-18 dB
HDR2 (5MHz Tone)	108 dB	129 dB
HDR2 (9MHz Tone)	111 dB	139 dB
HDR3 (5MHz Tone)	52 dB	52 dB
HDR3 (9MHz Tone)	39 dB	39 dB
IMR3	19 dB	19 dB
IMR2	96 dB	131 dB
SDR	19 dB	19 dB
ACLR	19 dB	19 dB
Notes, if any		

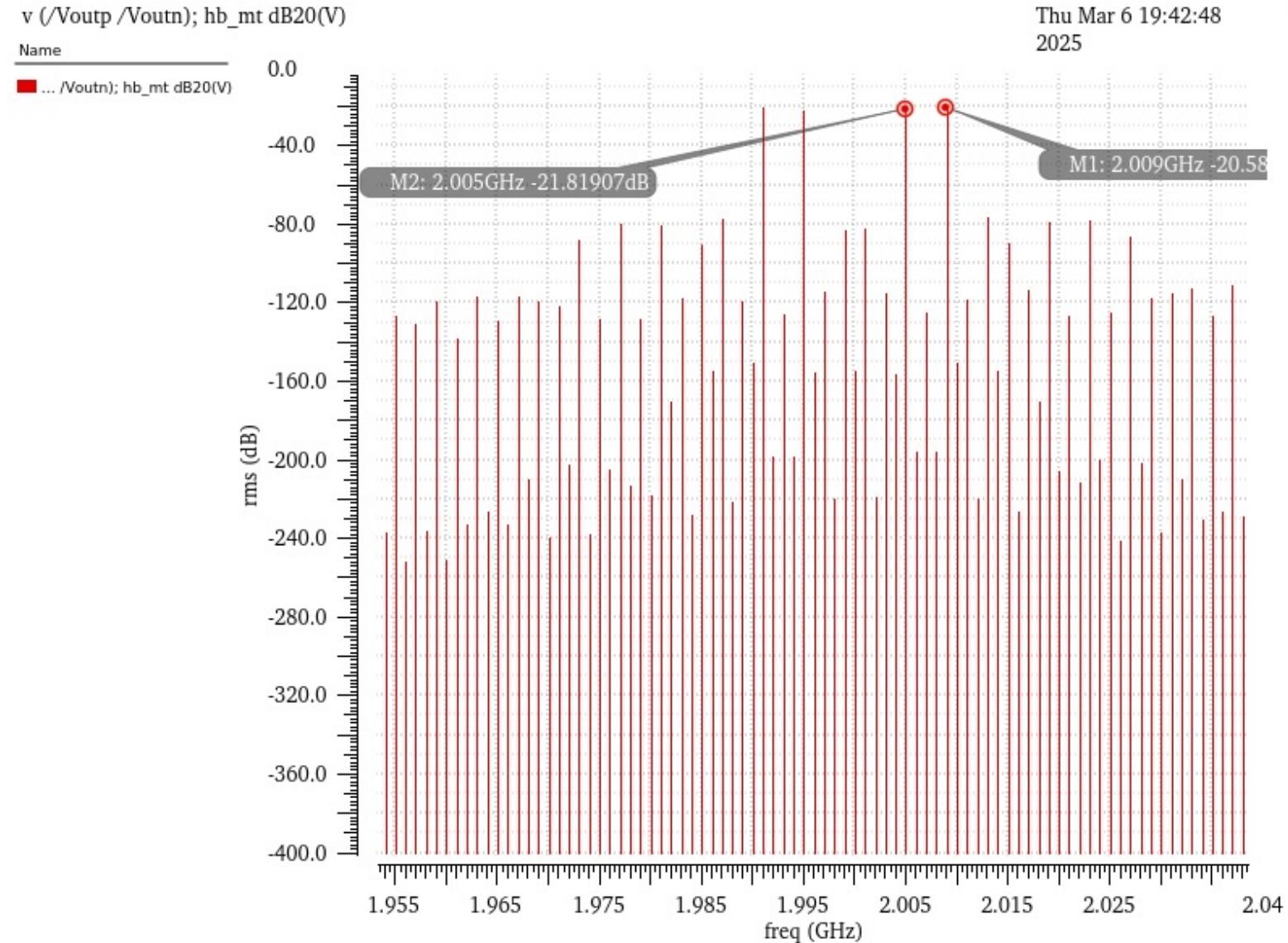
Question 3: Tx BBF + UpC (I + Q Channels) – Part 2

- Simulate the Tx BBF + I/Q UpC and measure: (Input Current = maximum allowed per design)
 - Output voltage (differential)
 - HDR3/IMR3 (differential)
 - HDR2/IMR2 (single-ended) and subtract 30dB for expected differential results
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2



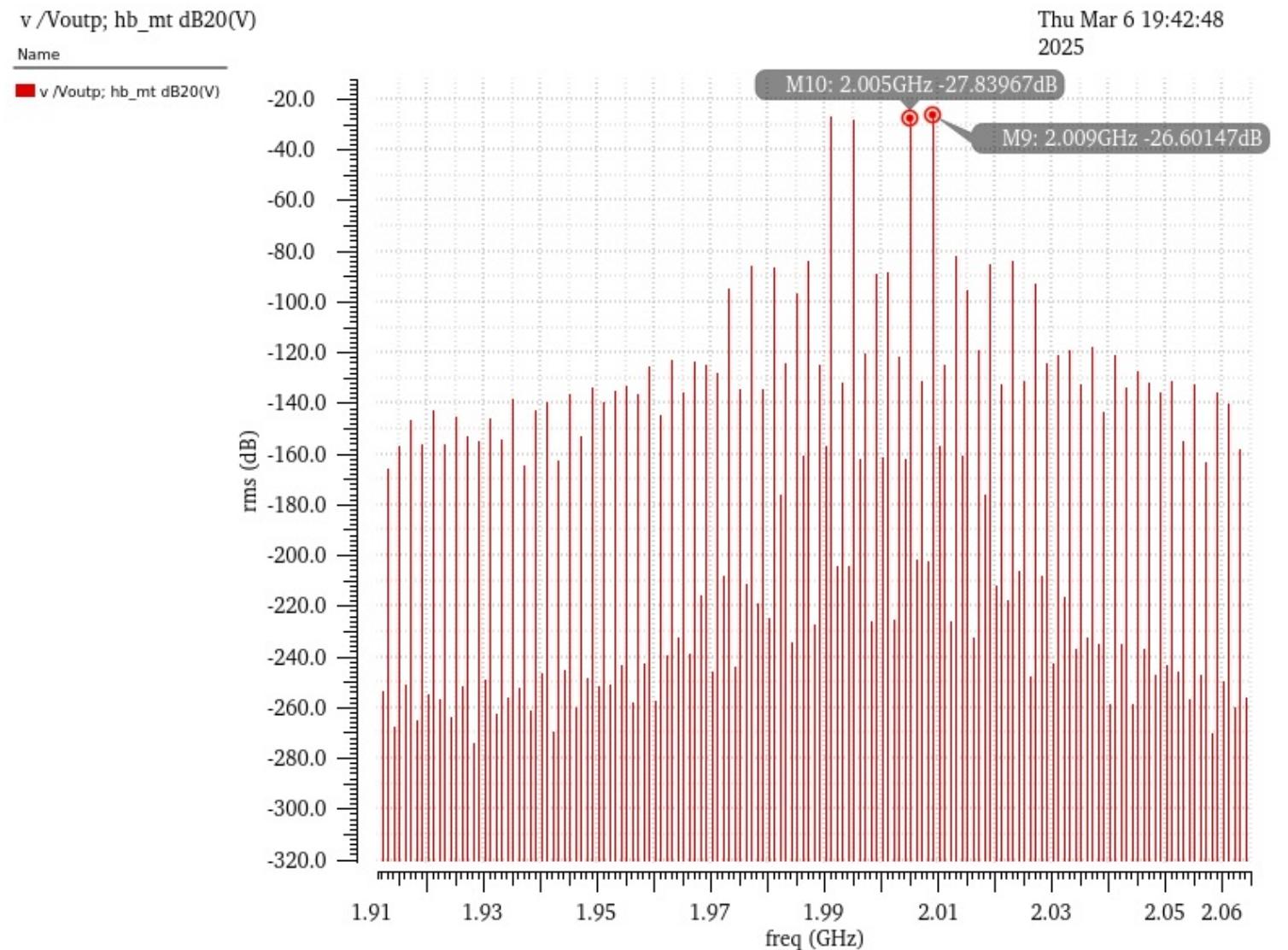
Question 3: Tx BBF + UpC (I + Q Channels) – Part 2

- Simulate the Tx BBF + I/Q UpC and measure: (Input Current = maximum allowed per design)
 - Output Voltage Spectrum (Differential)



Question 3: Tx BBF + UpC (I + Q Channels) – Part 2

- Simulate the Tx BBF + I/Q UpC and measure: (Input Current = maximum allowed per design)
 - Output Voltage Spectrum (Single-Ended)



Question 3: Tx BBF + UpC (I + Q Channels) – Part 2

- Simulate the Tx BBF + I/Q UpC and measure: (Input Current = maximum allowed per design)

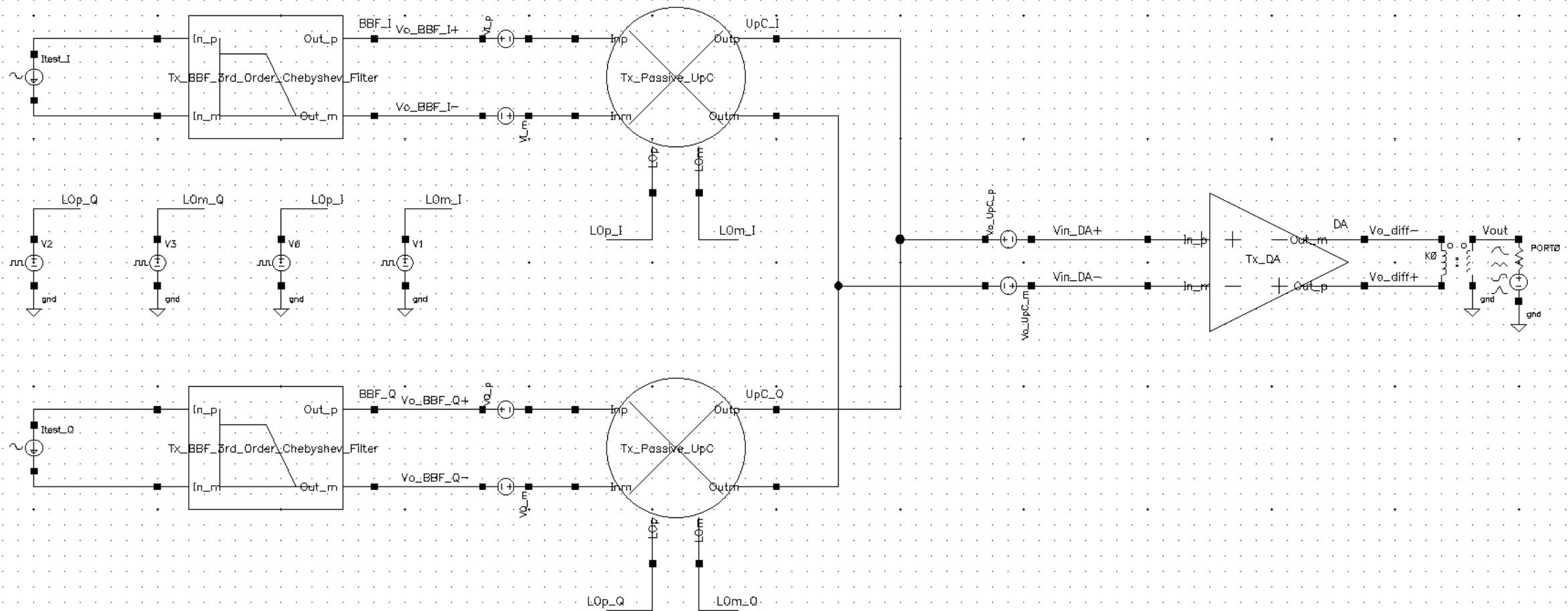
- SDR and ACLR from HDR3/IMR3 and HDR2/IMR2

I only see 6dB difference between SE and diff
in terms of even harmonics

	Single-Ended Output	Differential Output
Output Signal (5MHz Tone)	-27.8 dB	-21.8 dB m
Output Signal (9MHz Tone)	-26.6 dB	-20.6 dB m
HDR2 (5MHz Tone)	128 dB	128+30=158 dB
HDR2 (9MHz Tone)	149 dB	149+30=179 dB
HDR3 (5MHz Tone)	67 dB	67 dB
HDR3 (9MHz Tone)	65 dB	65 dB
IMR3	55 dB	55 dB
IMR2	133 dB	133+30=163 dB
SDR	55 dB	55 dB
ACLR	55 dB	55 dB

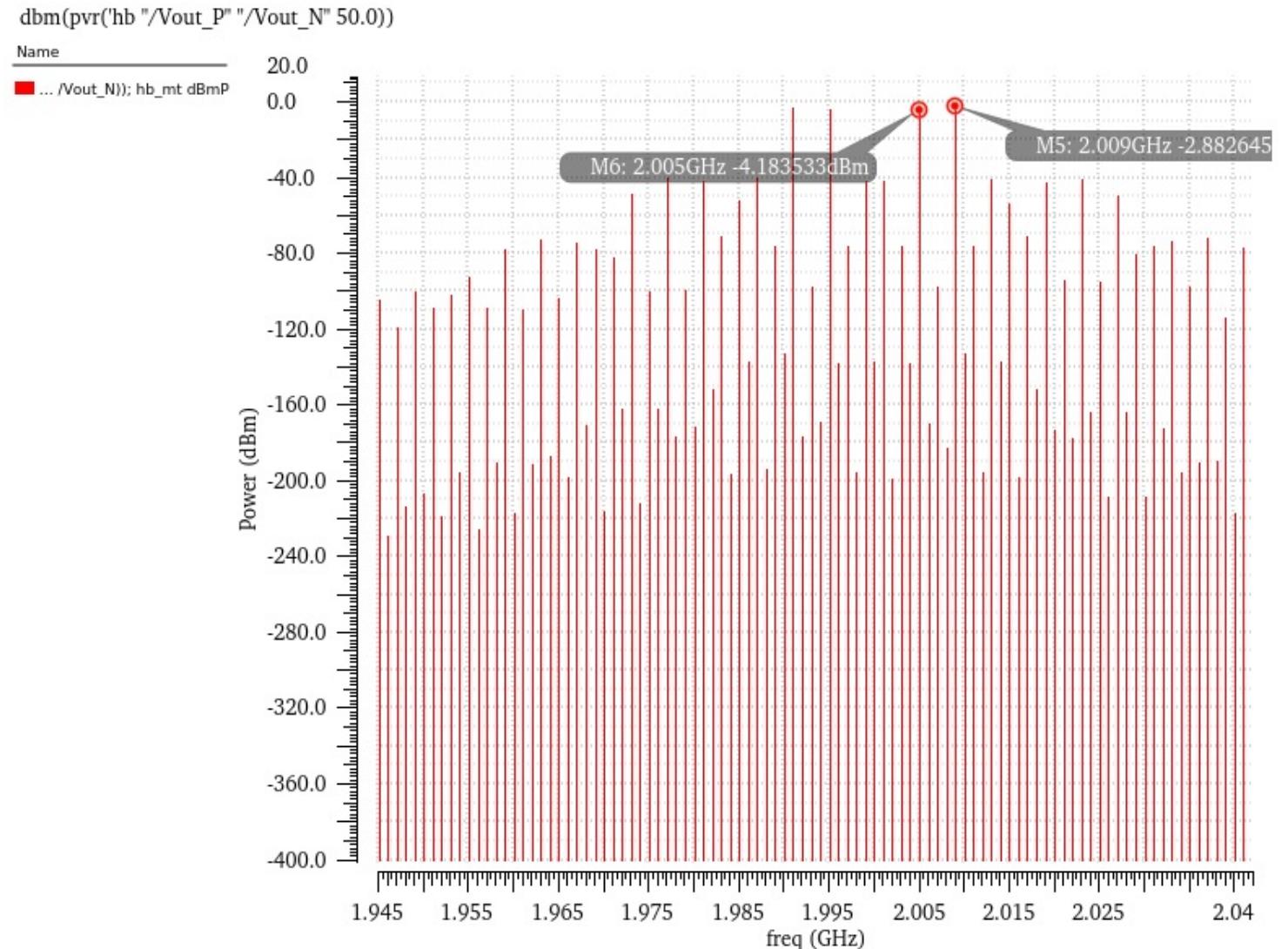
Question 3: Tx BBF + UpC (I + Q Channels) + DA – Part 3

- Simulate the Tx BBF + I/Q UpC + DA and measure: (Input Current = maximum allowed per design)
 - Output power
 - HDR3/IMR3
 - HDR2/IMR2 (single-ended) and subtract 30dB for expected differential results
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2



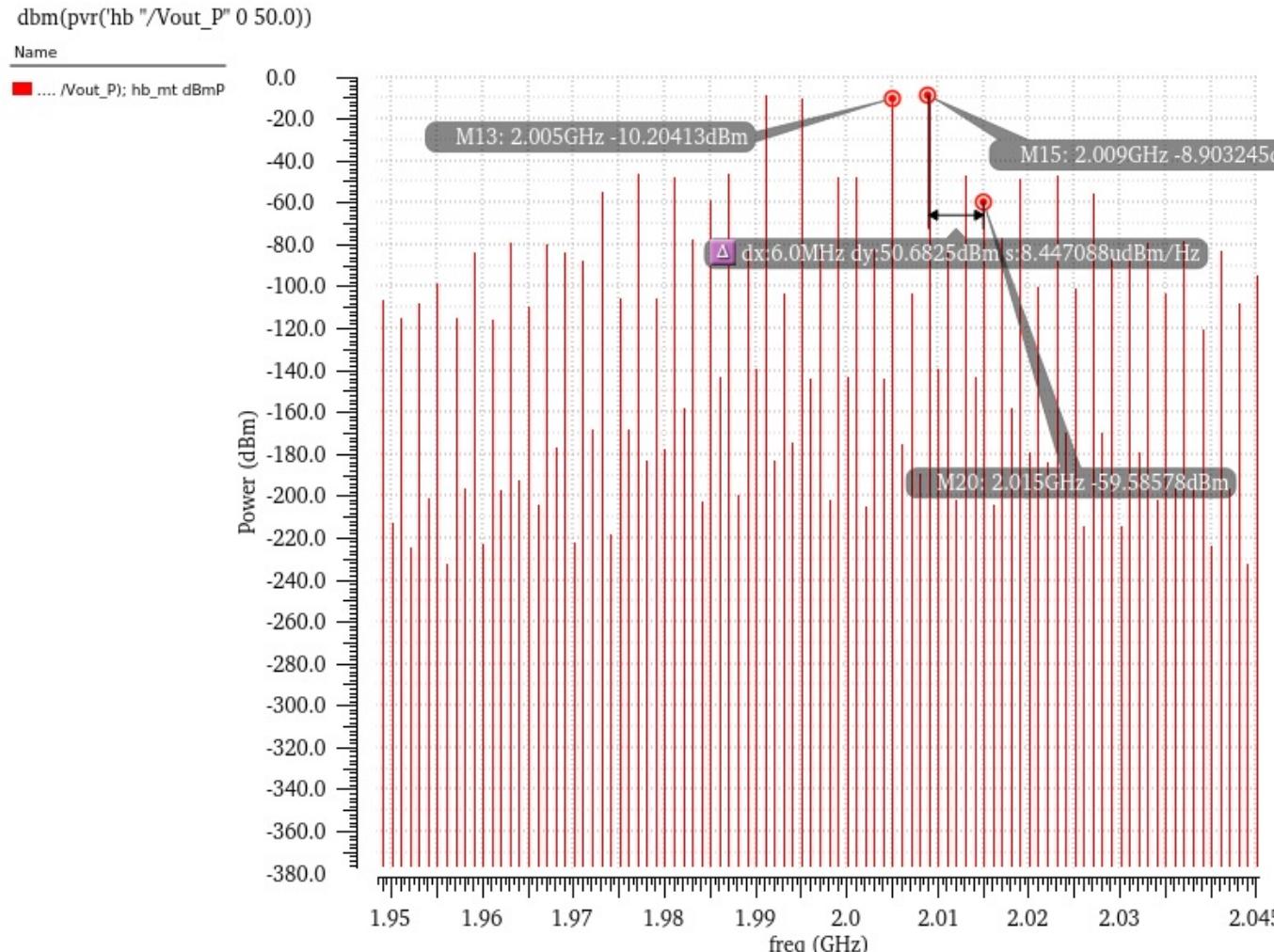
Question 3: Tx BBF + UpC (I + Q Channels) + DA – Part 3

- Simulate the Tx BBF + I/Q UpC + DA and measure: (Input Current = maximum allowed per design)
 - Output Power Spectrum (Differential)



Question 3: Tx BBF + UpC (I + Q Channels) + DA – Part 3

- Simulate the Tx BBF + I/Q UpC + DA and measure: (Input Current = maximum allowed per design)
 - Output Power Spectrum (Single-Ended)



Question 3: Tx BBF + UpC (I + Q Channels) + DA – Part 3

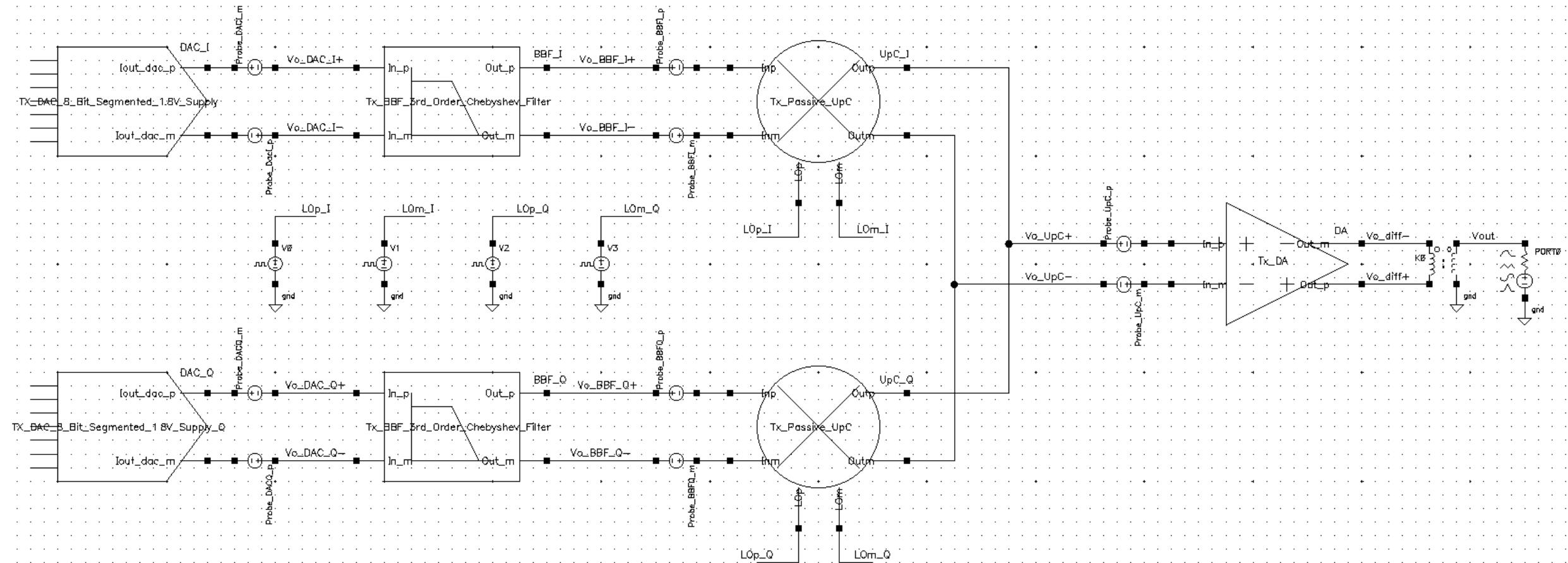
- Simulate the Tx BBF + I/Q UpC + DA and measure: (Input Current = maximum allowed per design)
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2

	Single-Ended Output	Differential Output
Output Signal (5MHz Tone)	-10 dBm	-4 dBm
Output Signal (9MHz Tone)	-8.9 dBm	-2.8 dBm
HDR2 (5MHz Tone) 4.01G	51 dB	195 dB
HDR2 (9MHz Tone) 4.018G	50 dB	193 dB
HDR3 (5MHz Tone) 6.015G	75 dB	75 dB
HDR3 (9MHz Tone) 6.018G	71 dB	71 dB
IMR3	37 dB	37 dB
IMR2	50.6 dB	134 dB
SDR	37 dB	37 dB
ACLR	37 dB.	37 dB

Question 3: Tx DAC + Tx BBF + UpC (I + Q Channels) + DA – Part 4

- Simulate the Tx DAC + Tx BBF + I/Q UpC + DA with a single-tone input and measure: (Input voltage to obtain the same input current as previous part)

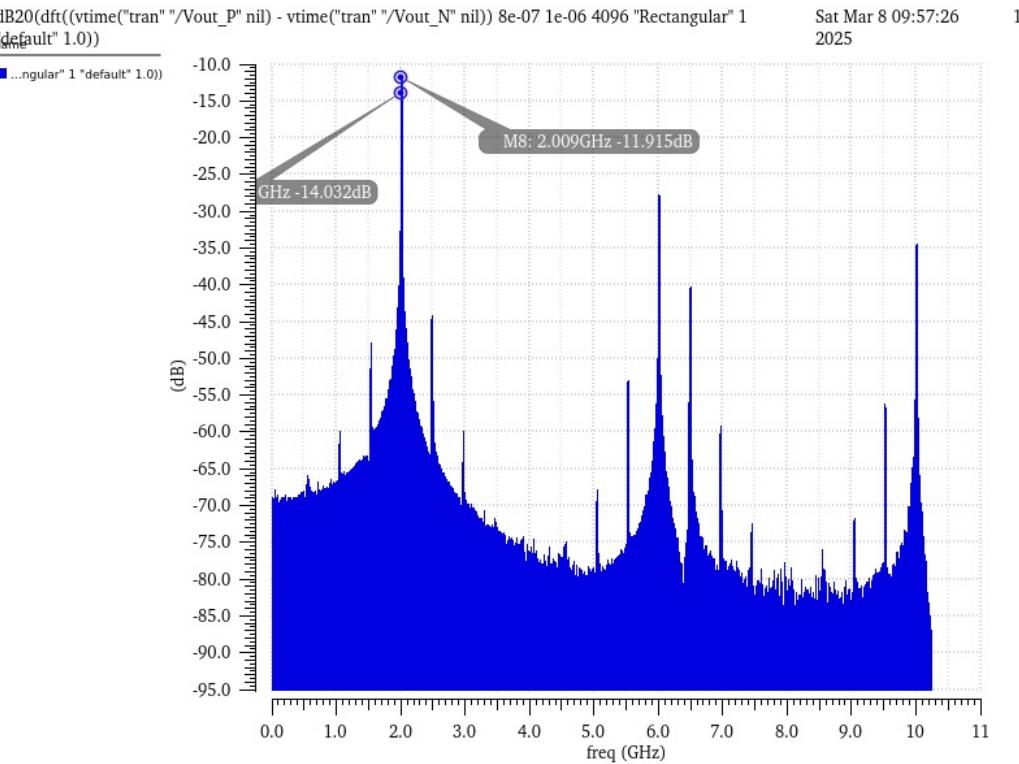
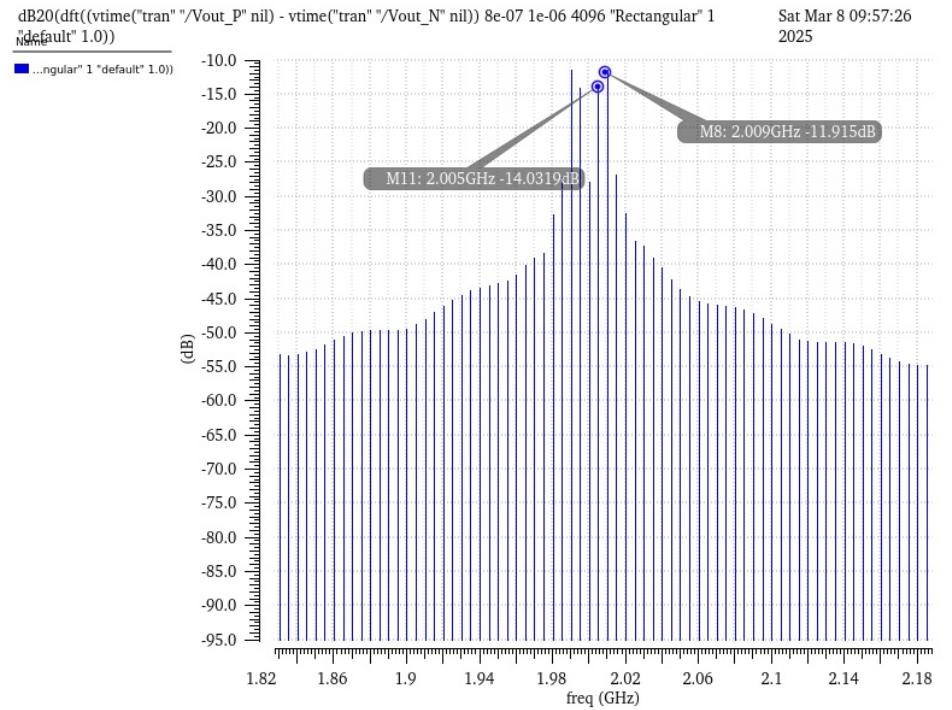
- Output power
- HDR3
- HDR2 (single-ended) and subtract 30dB for expected differential results
- SDR and ACLR from HDR3 and HDR2



Question 3: Tx DAC + Tx BBF + UpC (I + Q Channels) + DA – Part 4

- Simulate the Tx DAC + Tx BBF + I/Q UpC + DA with a single-tone input and measure: (Input voltage to obtain the same input current as previous part)

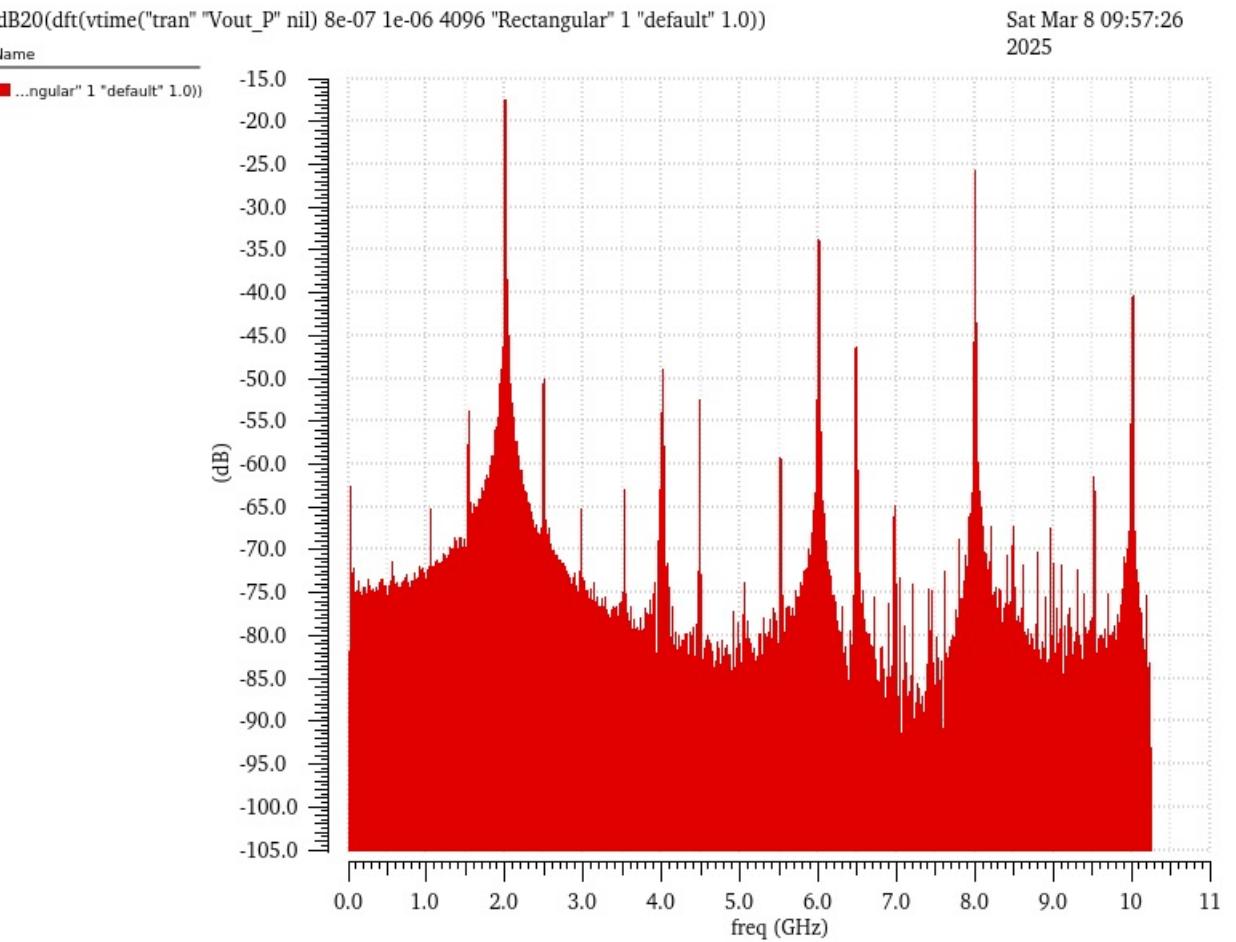
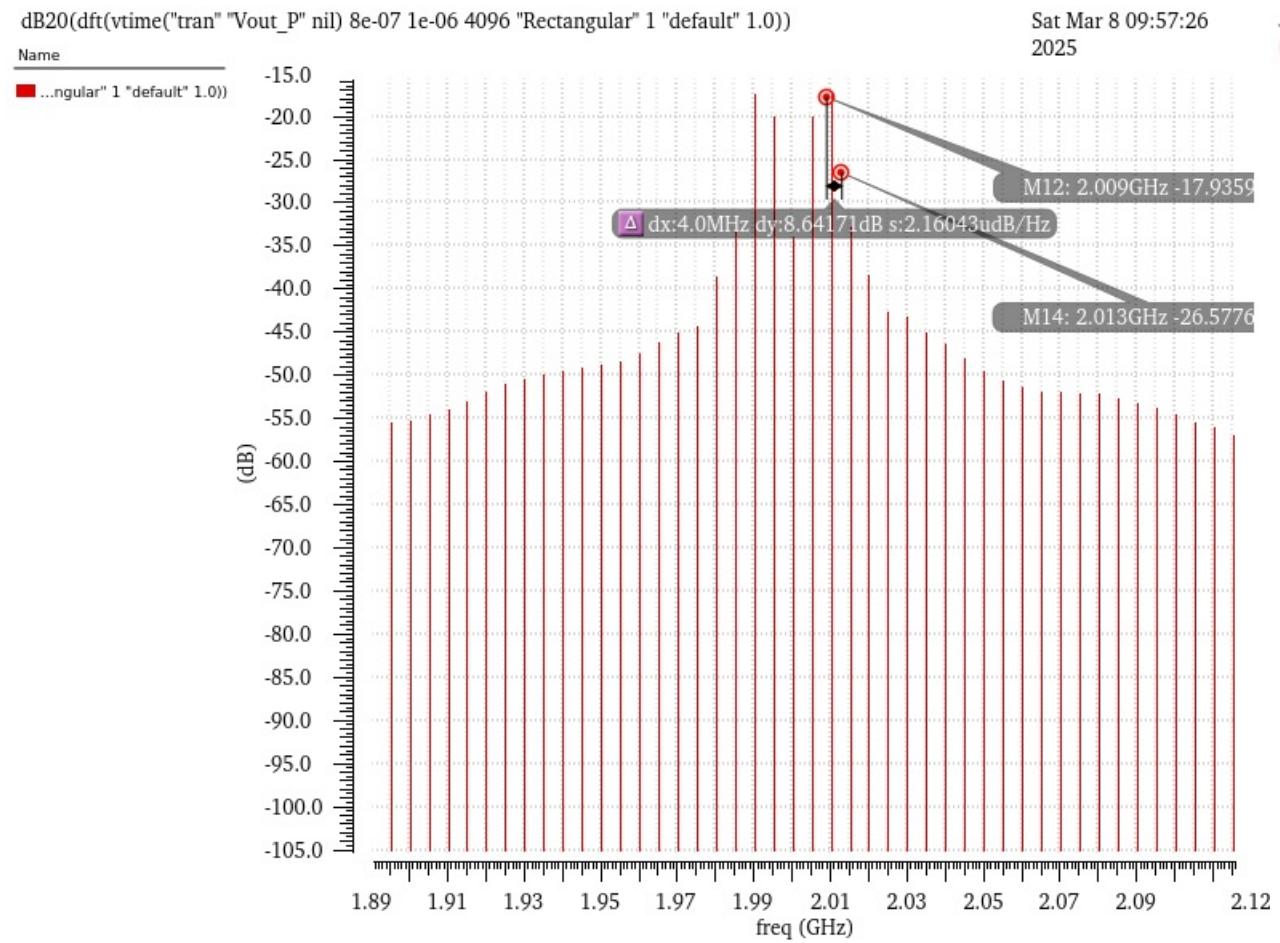
- Output Voltage Spectrum (Differential)



Question 3: Tx DAC + Tx BBF + UpC (I + Q Channels) + DA – Part 4

- Simulate the Tx DAC + Tx BBF + I/Q UpC + DA with a single-tone input and measure: (Input voltage to obtain the same input current as previous part)

- Output Voltage Spectrum (Single-Ended)



Question 3: Tx DAC + Tx BBF + UpC (I + Q Channels) + DA – Part 4

- Simulate the Tx DAC + Tx BBF + I/Q UpC + DA and measure: (Input Current = maximum allowed per design)
 - SDR and ACLR from HDR3/IMR3 and HDR2/IMR2

	Single-Ended Output	Differential Output
Output Signal (5MHz Tone)	-20 dBm	-14 dBm
Output Signal (9MHz Tone)	-18 dBm	-12 dBm
HDR2 (5MHz Tone) 4.01	44 dB	54 dB
HDR2 (9MHz Tone) 4.018	38.6 dB	56 dB
HDR3 (5MHz Tone) 6.015	28.4 dB	28.3 dB
HDR3 (9MHz Tone) 6.027	39 dB	38.9 dB
IMR3	8.64 dB	8.65 dB
IMR2 4.014	38.8 dB	63.8 dB
SDR	8.64 dB	8.65 dB
ACLR	8.64 dB	8.65 dB

End