ECE 283 Lab1 Design Review

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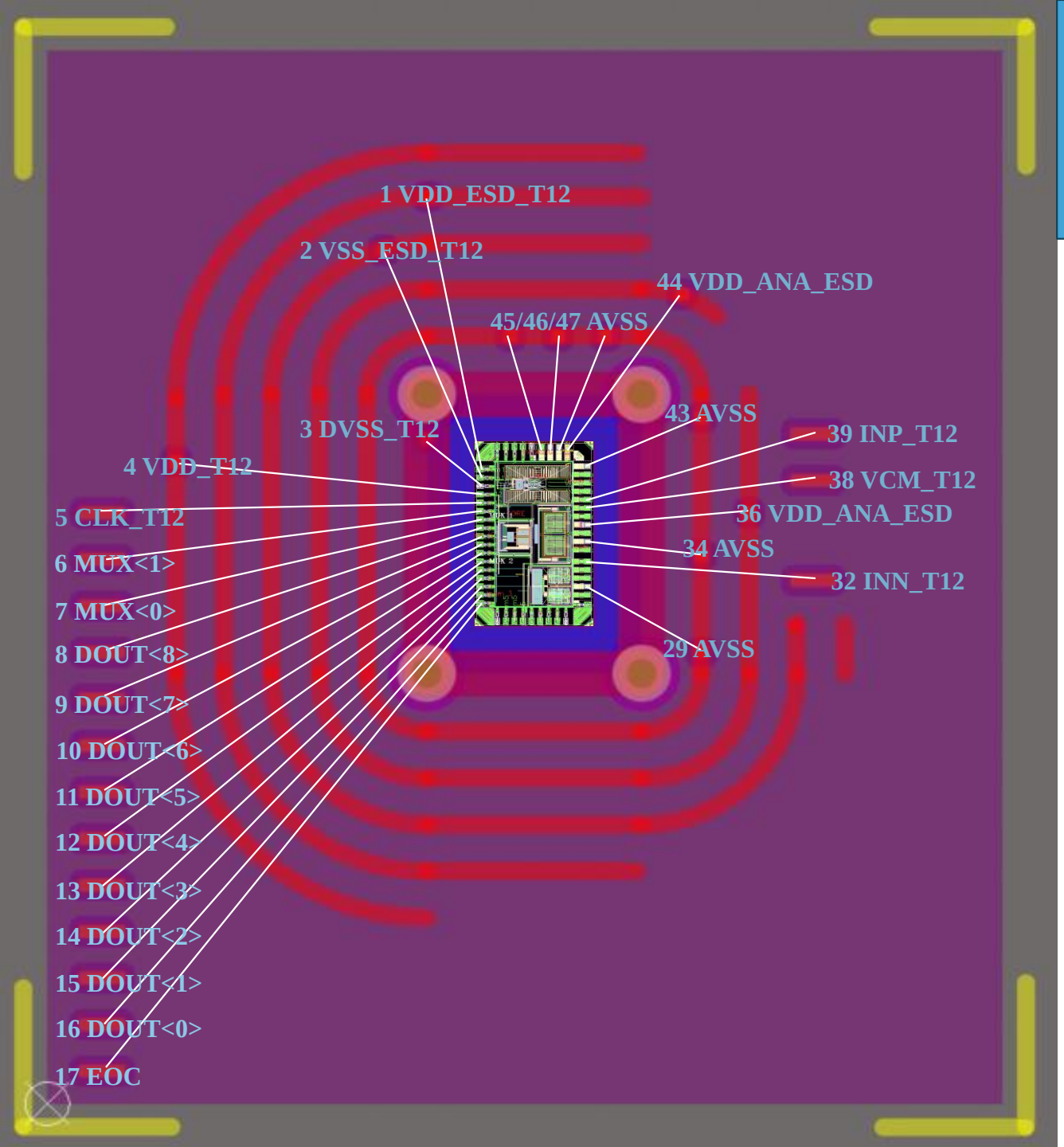
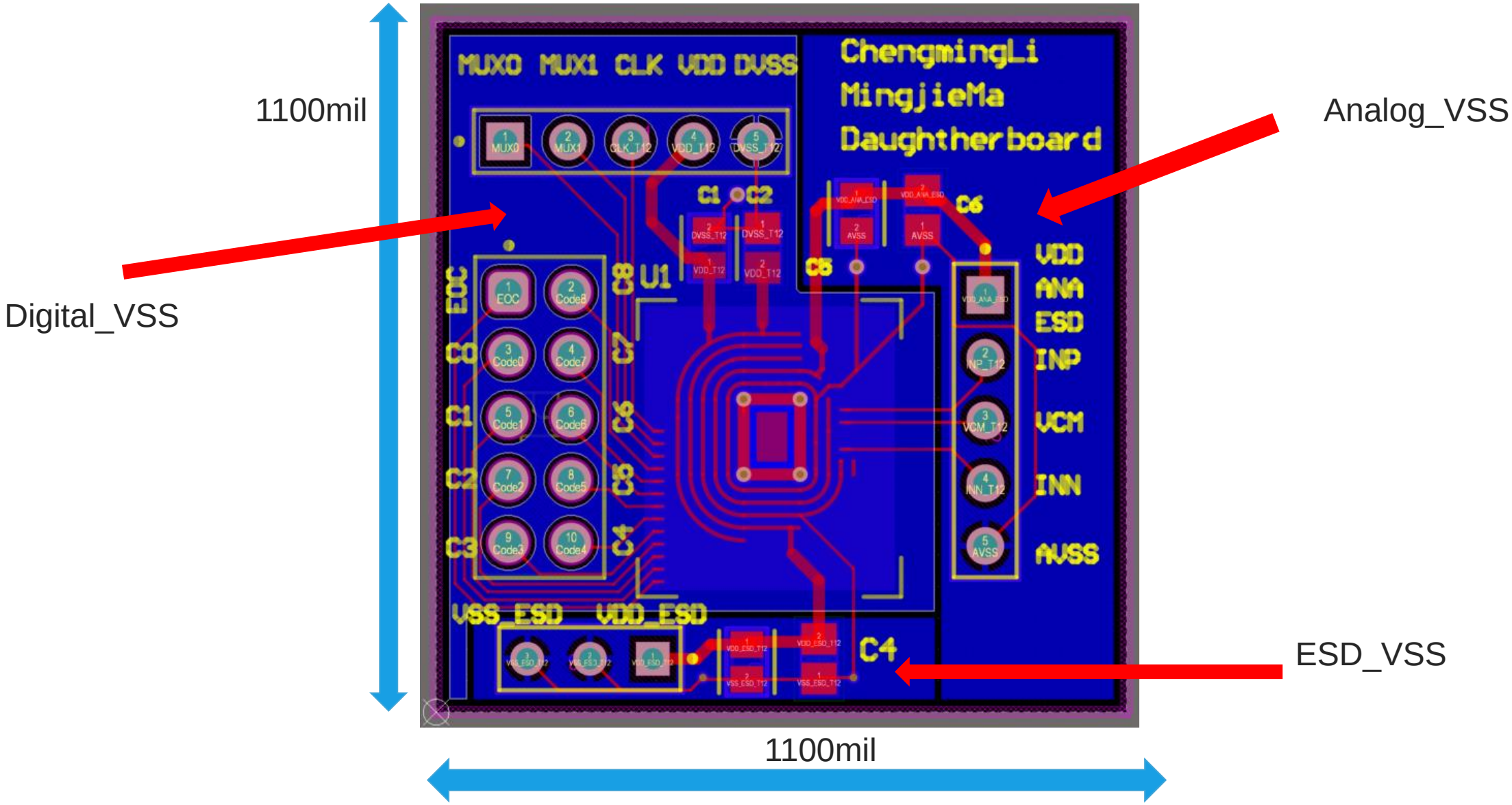
Chip Package and Wire bonding Diagram

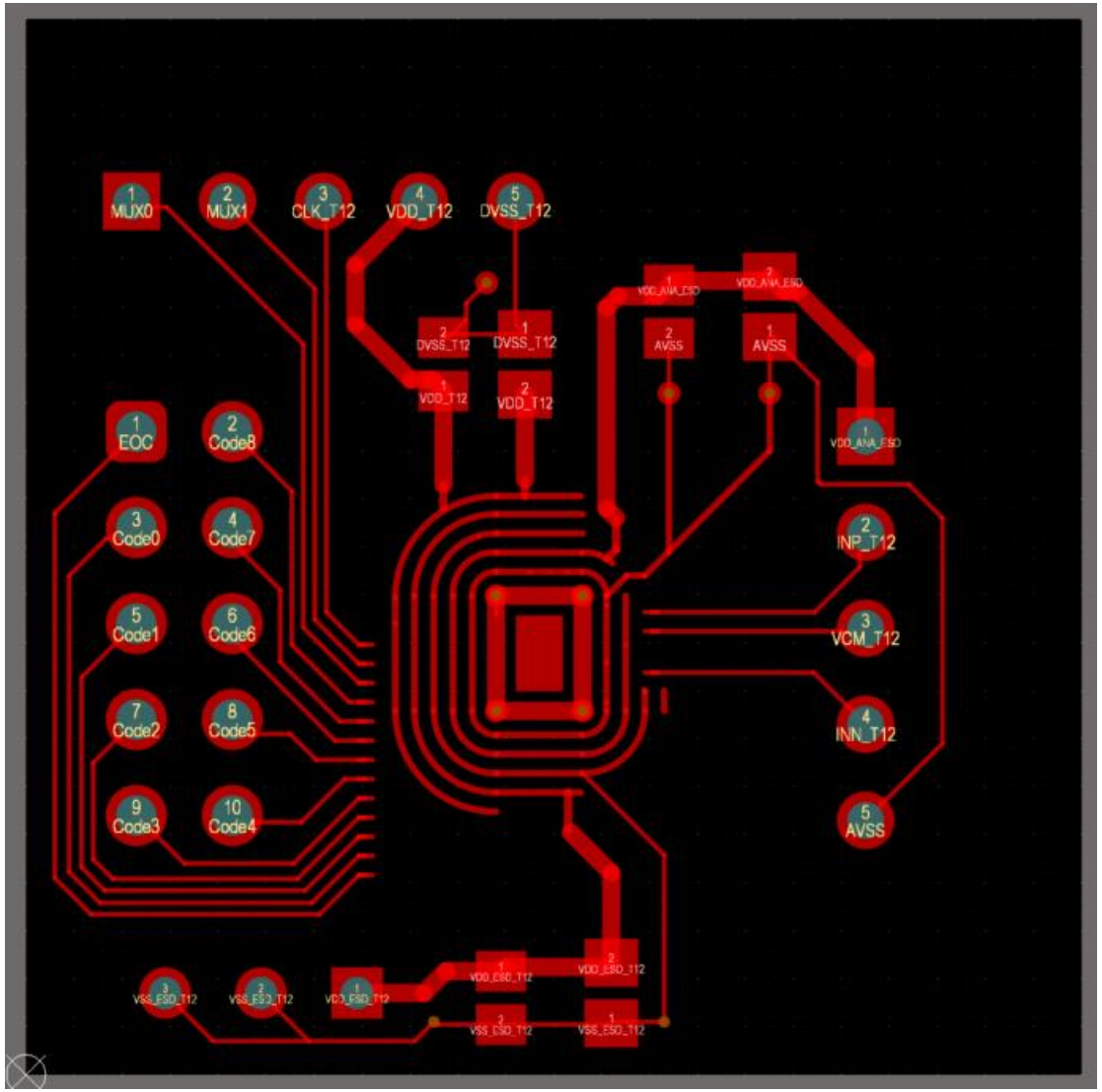


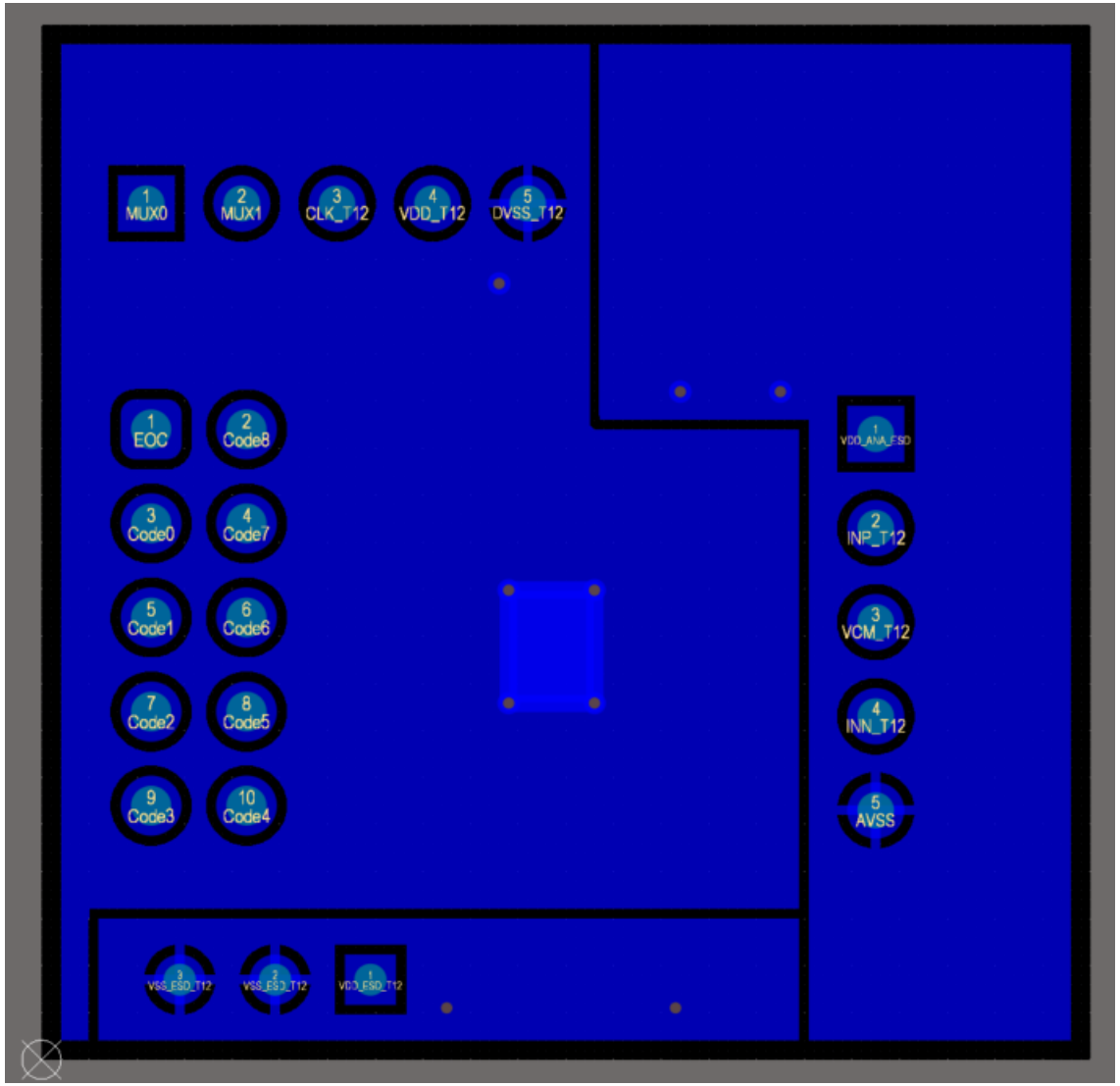
Pin Number	Type	Description
1	Power	VDD_ESD
2	Power	VSS_ESD
3	Power	DVSS_T12
4	Power	VDD_T12
5	Digital Input	CLK_T12
6/7	Digital Input	MUX_SEL
8 - 16	Digital Output	ADC_RESULT
17	Digital Output	EOC
19/34/43/45/46/47	Power	AVSS
32	Analog Input	INN_T12
36/44	Power	VDD_ANA_ESD
38	Analog Input	VCM_T12
39	Analog Input	INP_T12

DaughterBoard Layout

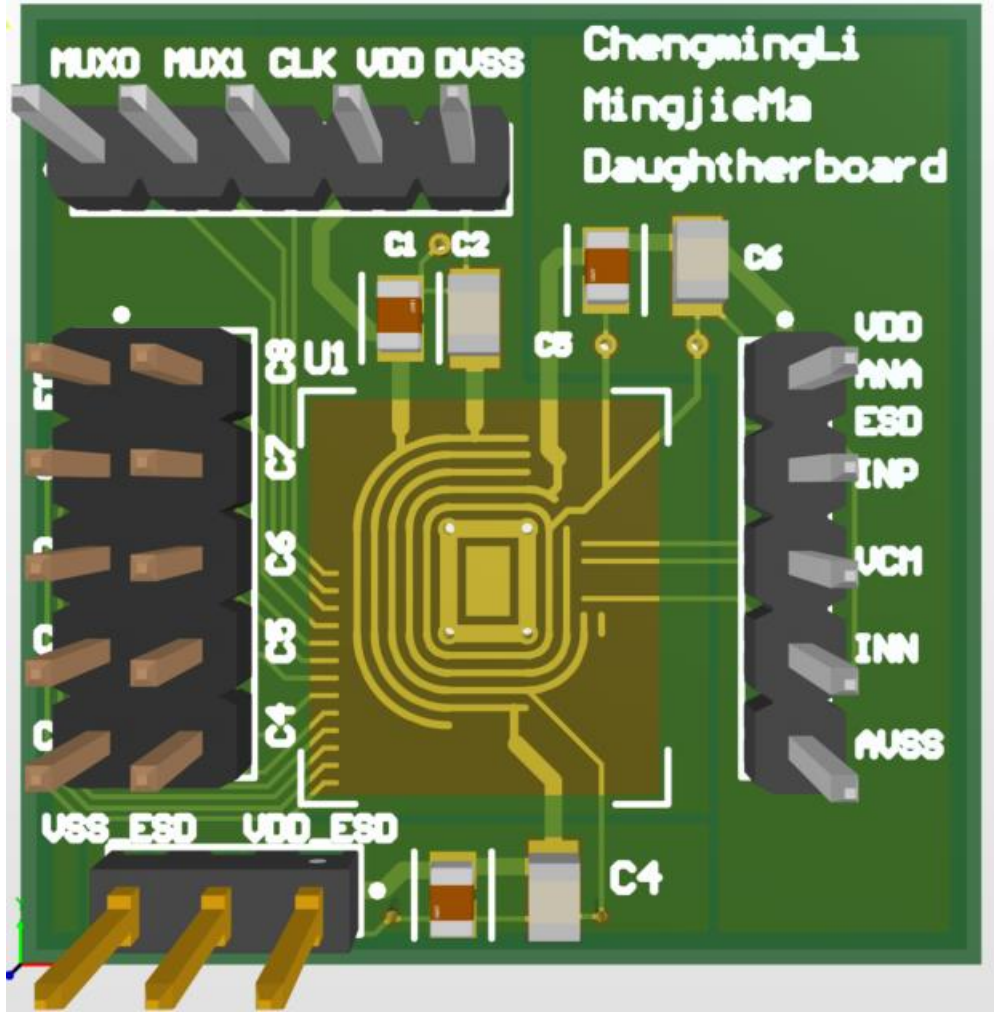


DaughterBoard Layout





DaughterBoard 3D View

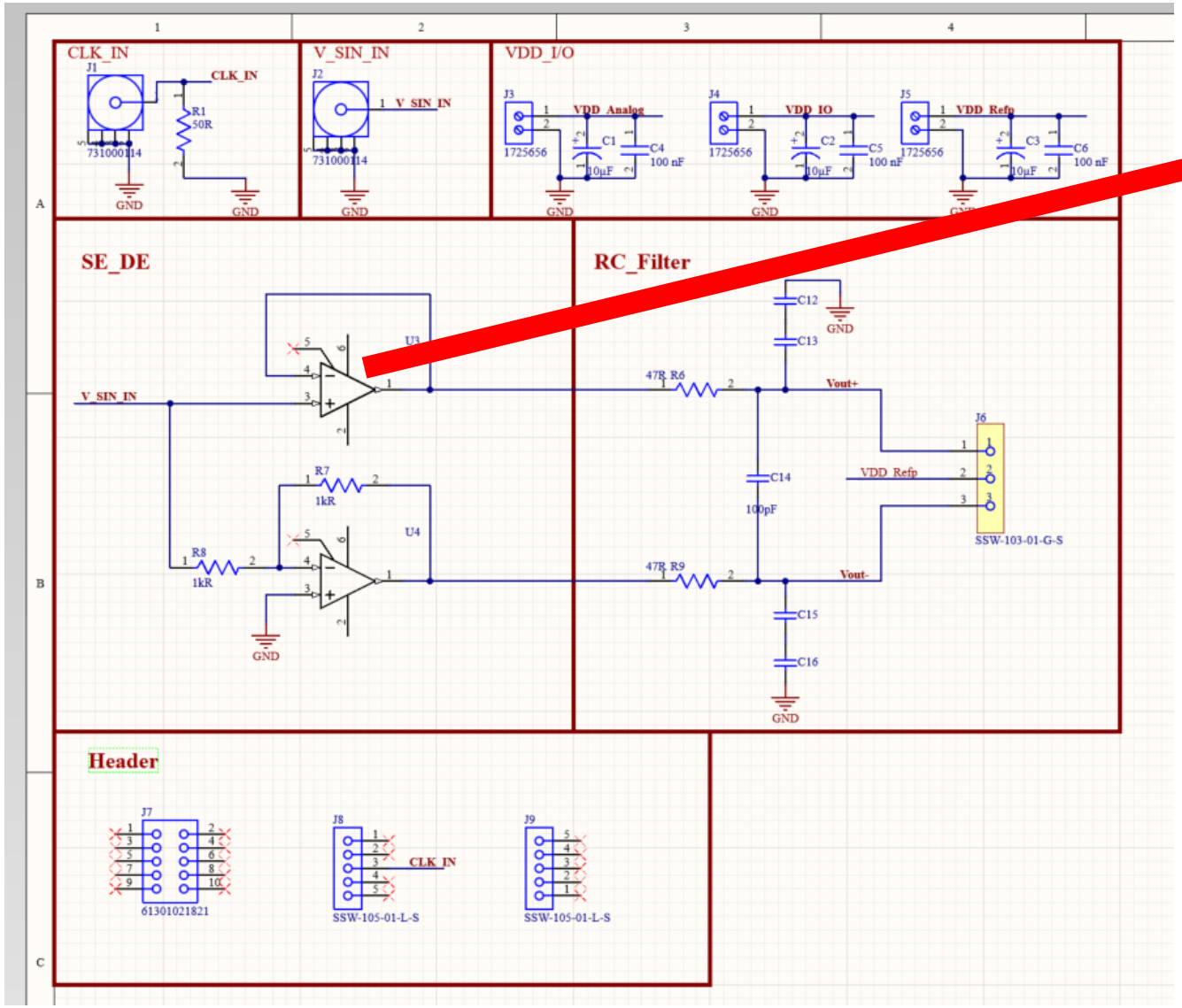


Top Layer: Signal Only
Bottom Layer: 3 VSS

Decap: 100nF and 1 uF, 0805
Try to put them as close as possible to the IC VDDs

Header: 100 mil pitch, but there is a danger of mismatching the position in the motherboard.
Solution: Record the coordinates of each corner of each header

Schematic - motherboard

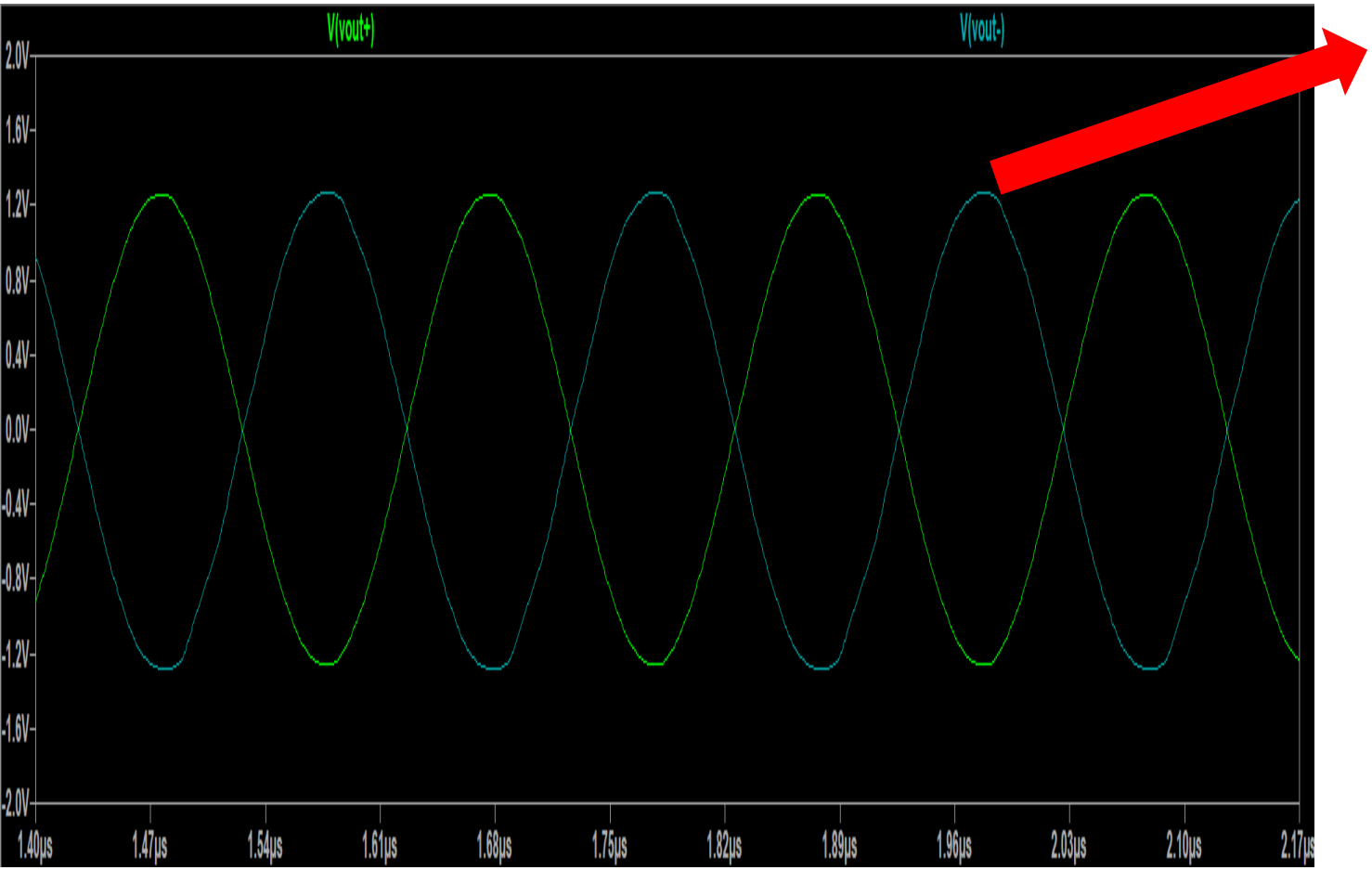


Opamp: LMH6611MKENOPB

- Gain Bandwidth Product - 135 MHz
- -3db Bandwidth - 365 MHz
- Voltage - Input Offset 74 µV
- CMRR - min 79dB, typ 98 dB
- PSRR – min 81dB, typ 96 dB

- Question: what other specs should I consider in terms of linearity?

LTspice – SE-DE Simulation

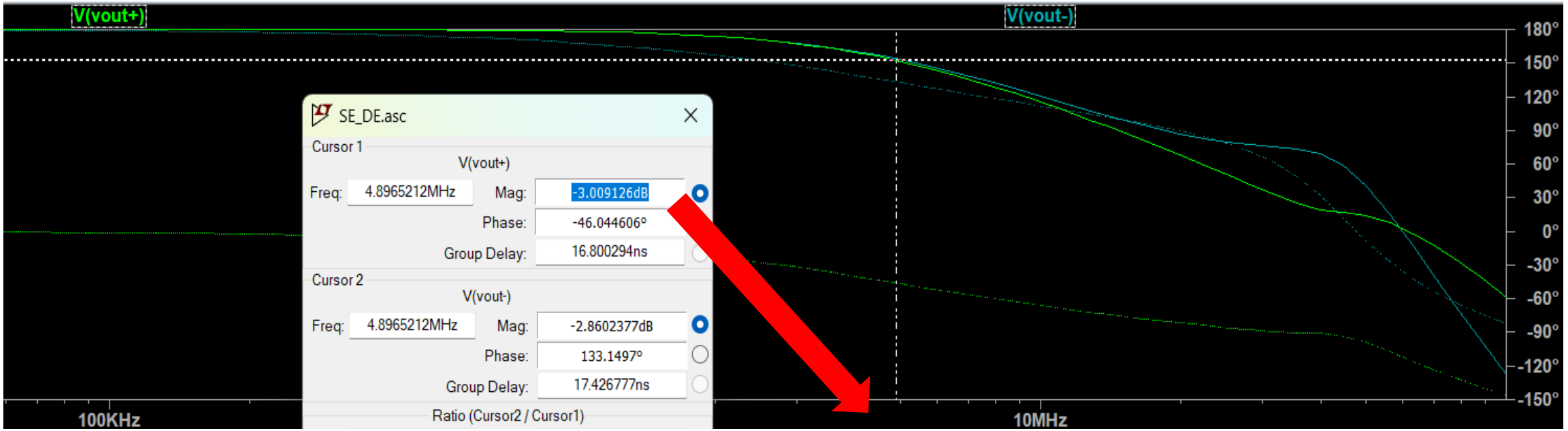


SEDE Output after RC filter

- Vp – 1.2V (1.8V input)
- Rfilter – 47 ohm
- Cfilter to gnd: 0.5nF
- Cfilter_common: 0.1nF

- Question: should we worry about the attenuation?

LTspice – SE-DE Simulation

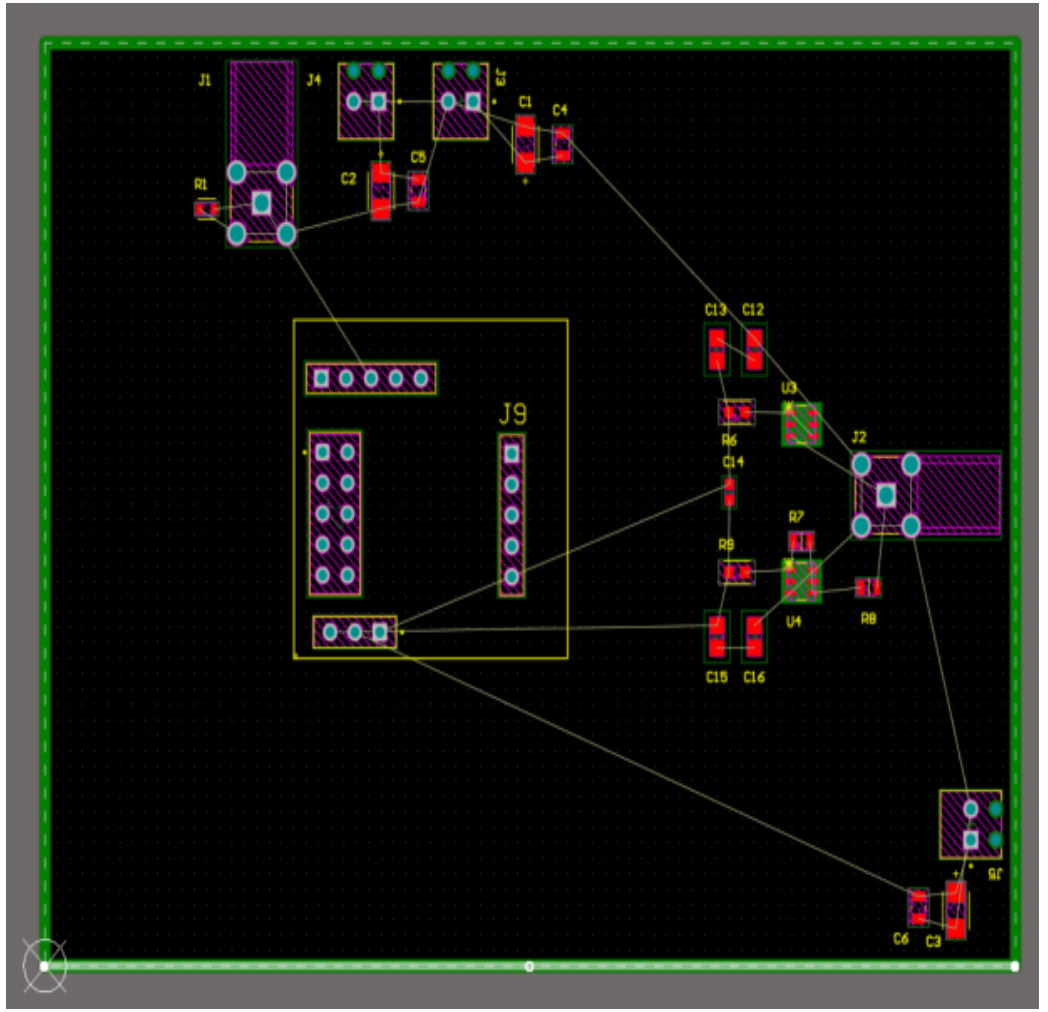


SEDE AC Ouput

- -3dB at 4.89MHz

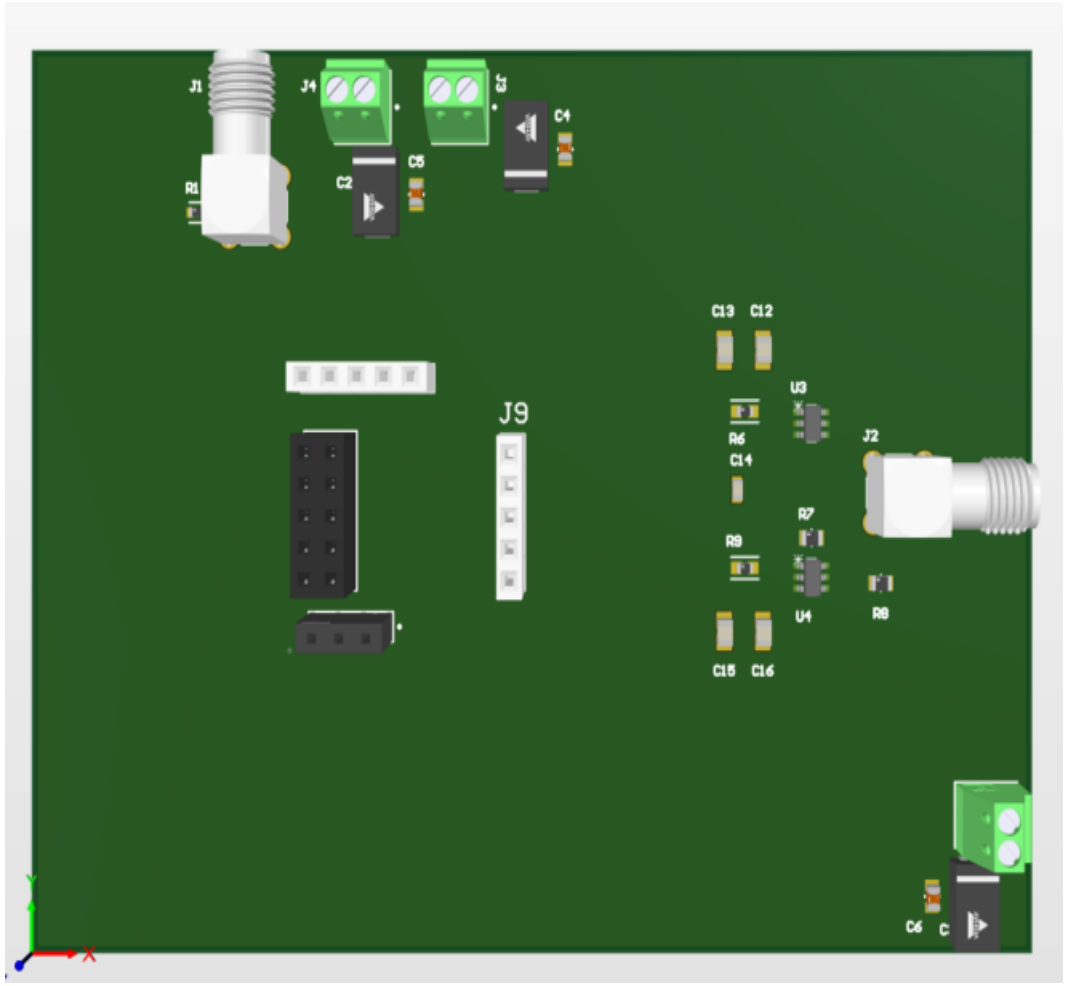
- Question: is this ok?

MotherBoard Layout



Not finished yet

MotherBoard 3D View



Not finished yet

Q & A