ECE266 Lab1

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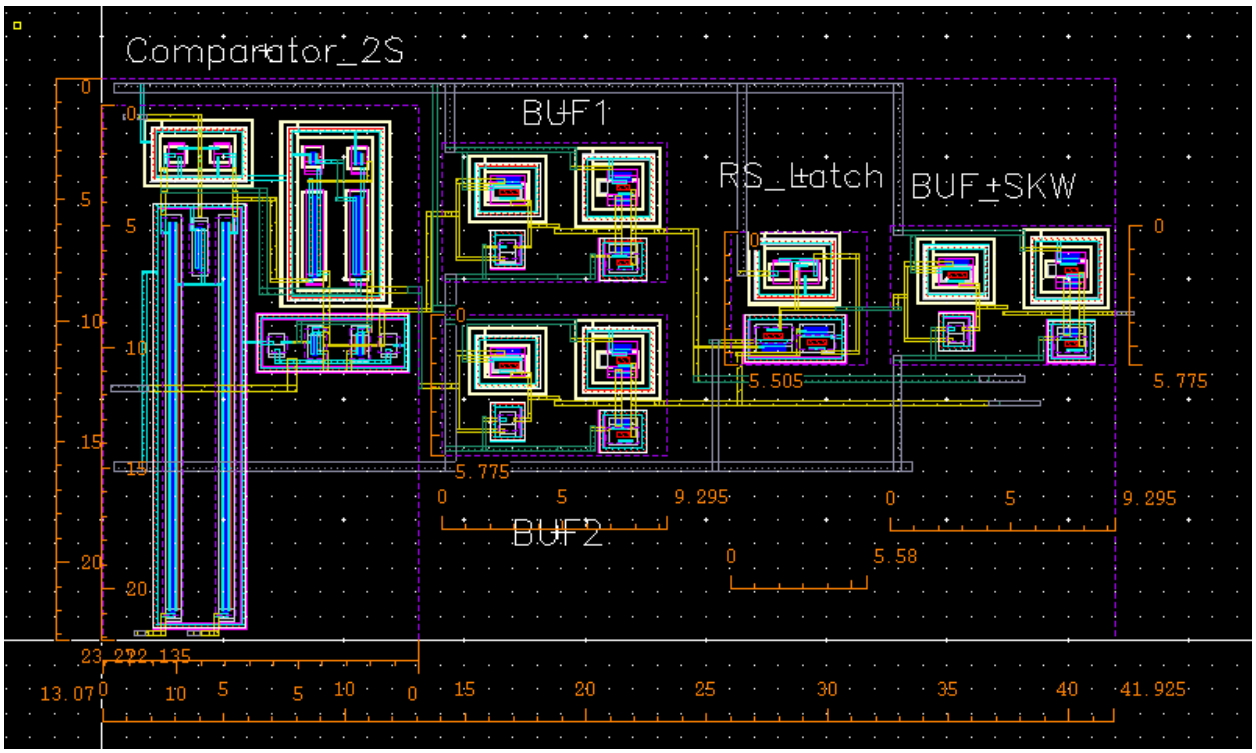
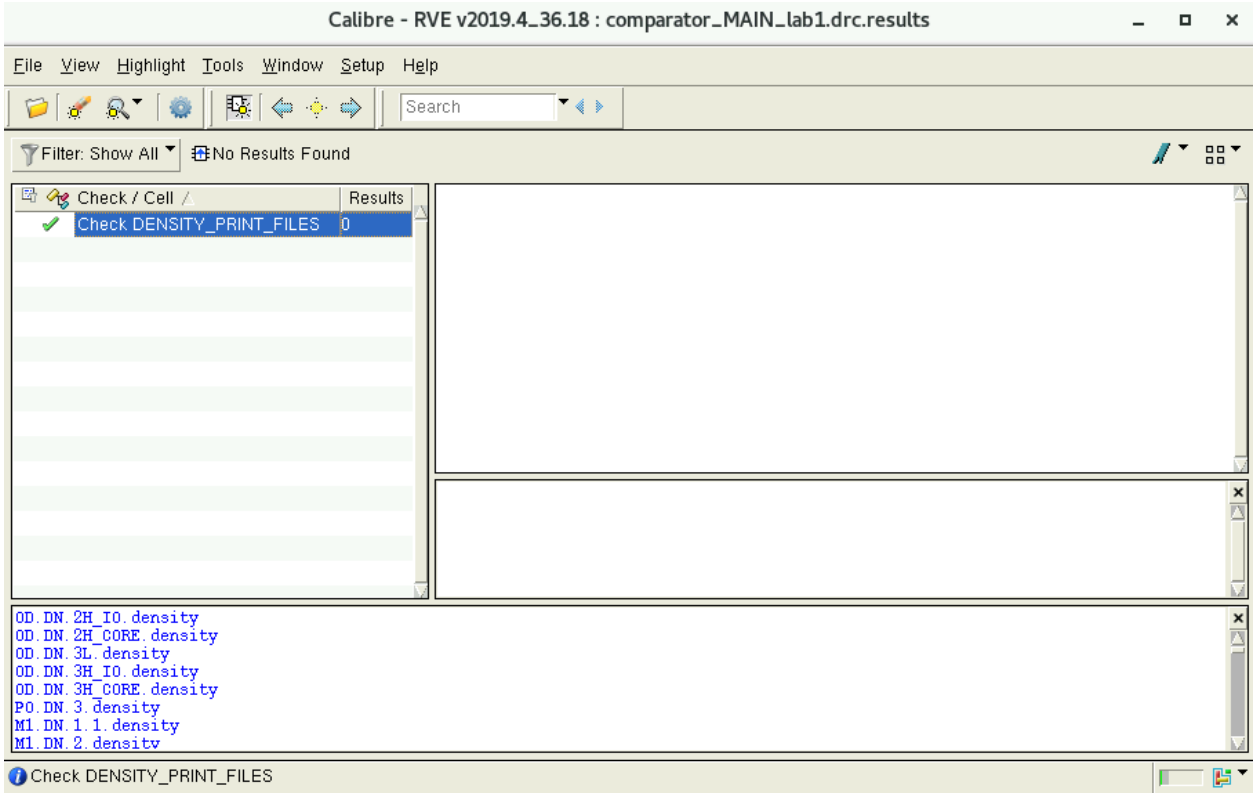
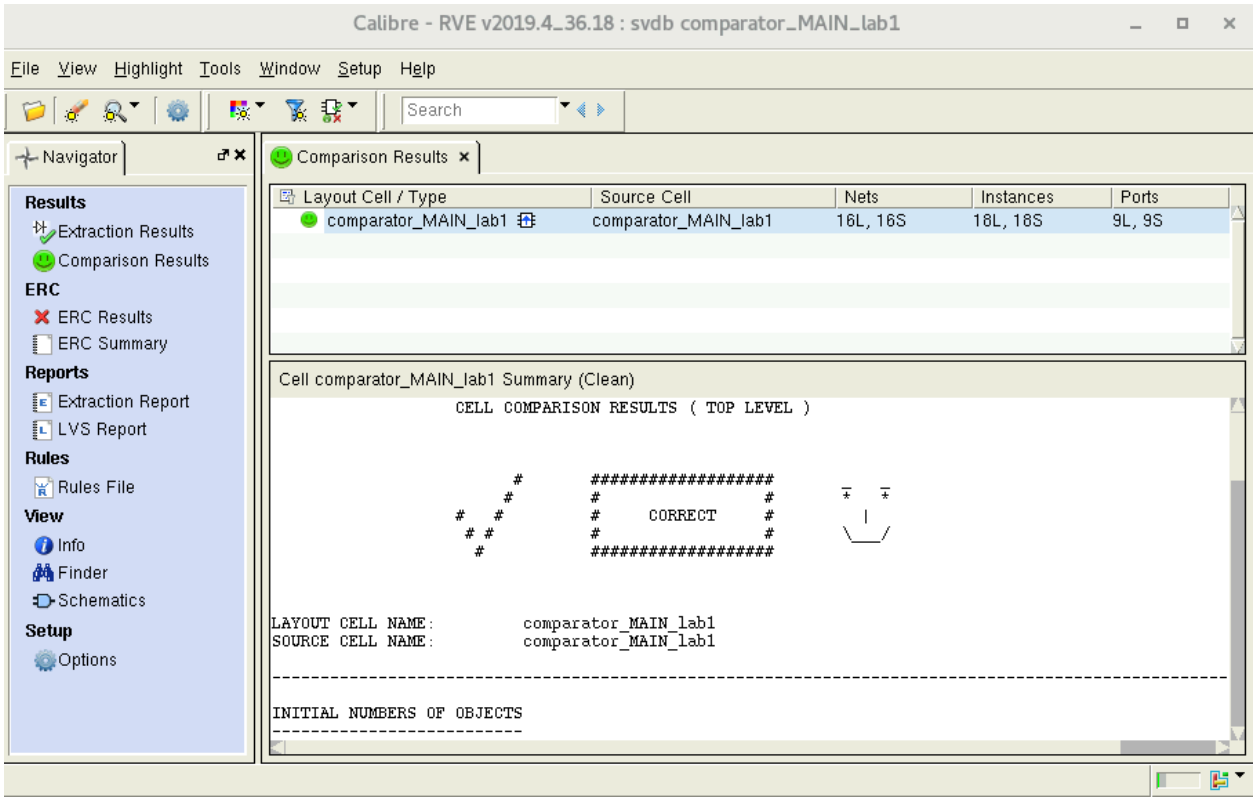
Layout


Comparator_2S
BUF1
RS_Latch
BUF_SKW
BUF2
5.775
5.505
9.295
5.58
41.925

DRC Result Summary



LVS Result Summary



Comments and conclusions

1. I started the design from the inverter as it is the easiest one to layout. And this layout took me a fair amount of time to get familiar with the tools, how to place the vias and wires, floorplanning and running the DRC and LVS checks. The first inverter layout took me 6 iterations to figure out the basics of tool usage and avoiding the drc violation.
2. Then, the layouts after the inverter went smoothly as I began to understand what I should do and what I shouldn't do to pass the DRC and LVS checks. The most difficult part was the comparator as it had more transistors and complex designs. Thus, the "comparator" stage also took me a while to finish the floor planning and wiring strategy.
3. My approach to the floor planning was to keep matching each transistor as where it should be, shown in the schematic. Sometimes I need to flip the transistor upside down to make wiring easier for the Drain and Source. And For the pin placement, I have tried to match their position as well. And VDD always on the top, VSS always on the bottom of the entire layout. But, I realized this at a very late stage. So it made my layout a little messy.
4. Something I learned from this lab are:
    a. Guard ring needs to be placed for the transistors who need the best performance, like the current mirror, differential pair, etc. And always be careful about what the annotation says in the schematic. It includes information about when the Guard ring needs to be placed for sure. On the other hand, a guard ring is not required for every device.
    b. PR boundary, it needs to be placed for every cell. Quote from Darshan's piazza "it is a good practice to have boundaries for all the cells. It helps you to reserve space if more than one people work on the same level"
    c. Poly contact, it may be a good idea to place poly contact both on top and bottom for the wider device in order to reduce the resistance.
5. Something I didn't learned very well from this lab are:
    a. The best design layout practice! Similarly to PCB layout, there are always some good rules of thumb, which we always need to follow. But, I couldn't get the bad layout choices vs. good layout choices from this lab.
    b. Metal usage, are there any rules I should follow? Like for the odd number of metal, should I place them horizontally, and even metal vertically?