ECE 283 Lab3 Design Review

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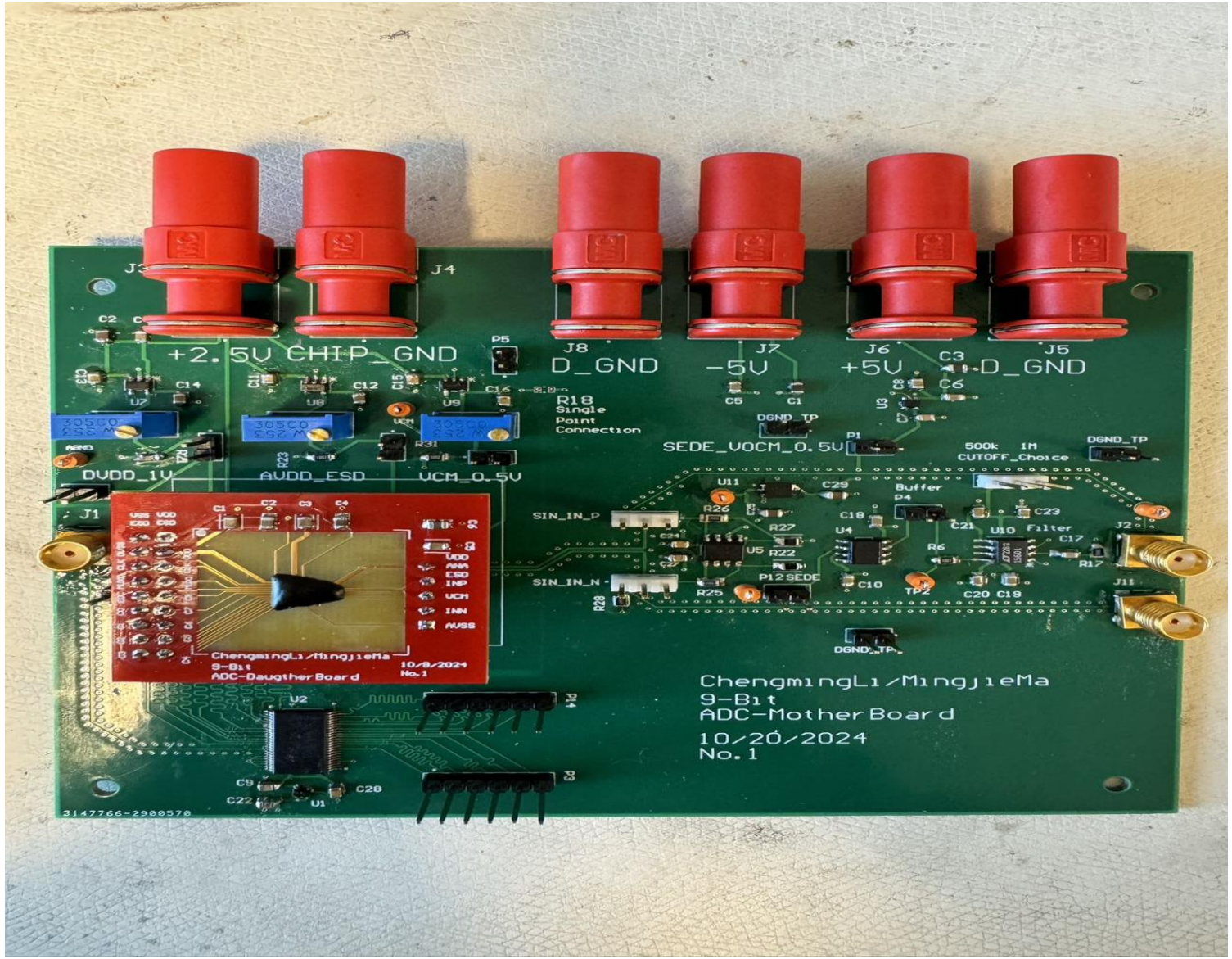
MotherBoard + DaugtherBoard

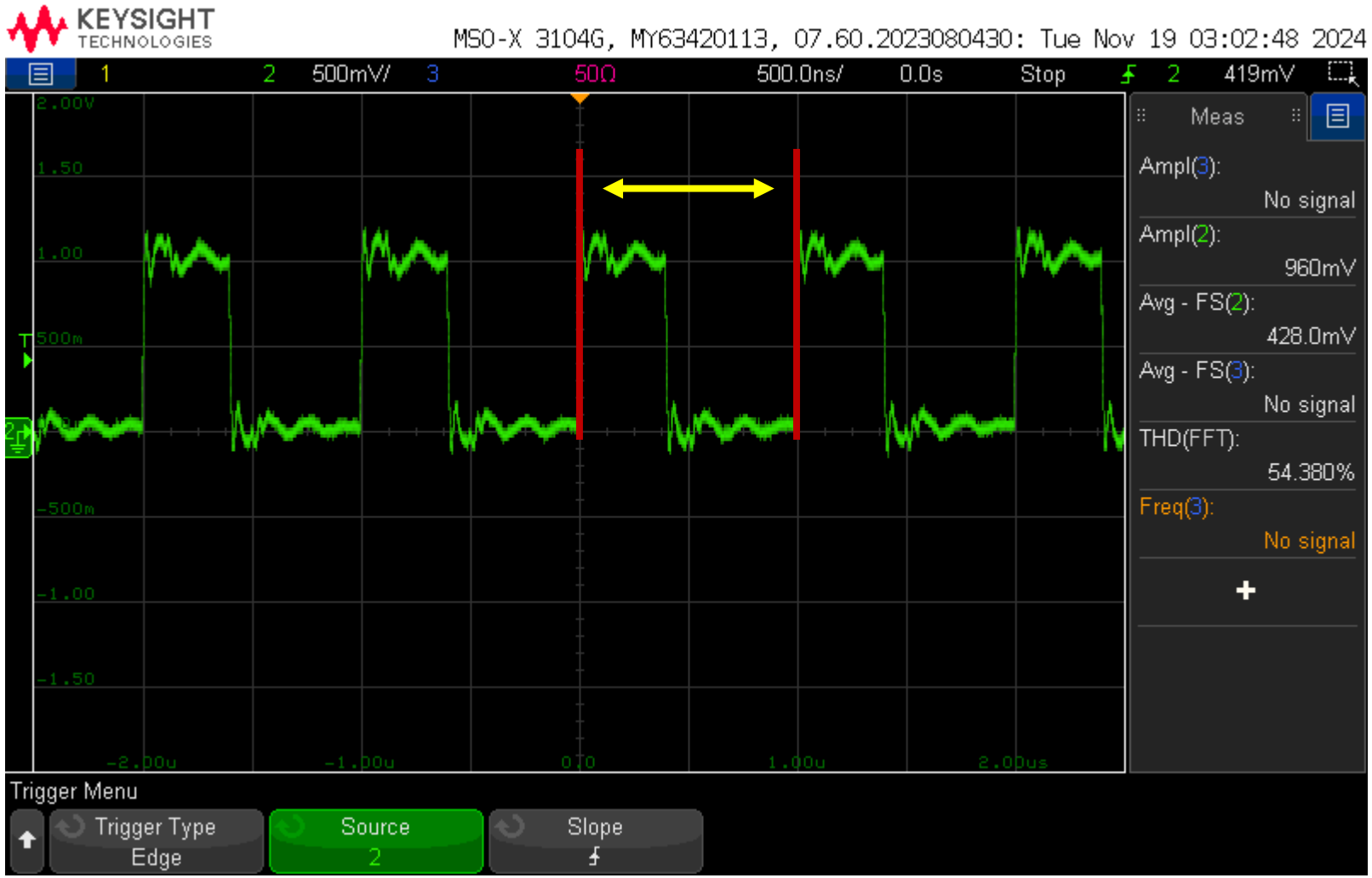


1. Modularized the Design
    1. By having jumper between each IC
2. Testability
    1. Jumper for GND for easy probeing
    2. Grab & Probe
3. Configurability
    1. Potentiometer for tweaking the perfect Vcm, AVDD, AVDDESD

MotherBoard + DaugtherBoard BringUp TestPlan

Test No.	Test Plan	What Components	What Exepect to Se	Status	Notes
	Power Supply Test				
0	Produce -5 V and 5 V on breadboard	Breadboard and Power supply with 3 separate power supply	Neg 5V and Pos 5V	Pass	
1	After connecting 2.5V, Measure the LDO U7 U8 U9's output	U7, U8, U9	1.5V @ Pin 5 of LDOS	Pass	
2	After connecting -5 V and 5V, makre sure power vias are shown 5V and -5Vcorrectly	3-Pins Jumer near the Vsin_IN_NP	Pos 5V on the leftmost pin and Neg 5V on the rightmost	Pass	
3	LDO U3 regulated down from 5V to 2.5	P1 Jumer Right Most Pin	2.5V on P1 rightmost	Pass	
4	LDO U11 regulated down from 2.5V to 0.5V	Jumer head in P1, U11's Pin 1 and 2, and TP	0.5V on TP	Pass	
5	Tweak Potentiometer U7 to get 1V for DVDD	Potentiometer near U7, Jumer Top pin	1V DVDD @ Jumer Top Pin	Pass	
6	Tweak Potentiometer U8 to get 1V for AVDDESD	Potentiometer near U8, Jumer Top pin	1V AVDD_ESD @Jumer Top Pin	Pass	
7	Tweak Potentiometer U9 to get 0.5V VCM	Potentiometer near U9, Jumer left pin	0.5V VCM @Jumper Left Pin	Pass	
	Sig_IN Test				
0	Connect 200K Hz Offset 0V, Amp 0.4V Sine wave into J2	J2 SMA, TestPoint Near J2	200K Hz Offset 0V, Amp 0.4V Sine wave	Pass	
1	U10(LPF) Connect to 1M filter choice 200K Hz Offset 0V, Amp 0.4V Sine wave shows up at P4, no distortion	U10 filter choice jumer, jumper head, P4 right pins, TP2	200K Hz Offset 0V, Amp 0.4V Sine wave into J2	Pass	
2	Connect P4 Jumer, siganal go through U4 buffer and measure P12 Output	U4, P12 rightmost Pin	200K Hz Offset 0V, Amp 0.4V Sine wave	Pass	
3	U5(SE_DE) signal coming from P12, Measure SIN_IN_P and SIN_IN_N Sig property	P12 Jumer head SIN_IN_P header and SIN_IN_N header right most pin	SIN_P: 200K Hz Offset 0.5V, Amp 0.4V Sine wave SIN_N: 200K Hz Offset 0.5V, Amp 0.4V Sine wave, 180 out of phase	Pass	
	Digital Test				
0	CLK Connect to J1	J1		Pass	
1	MUX Choice	Used female to female jumer to connect the MUX choices		Needed to verify	MUX0: 0, MUX1: 1

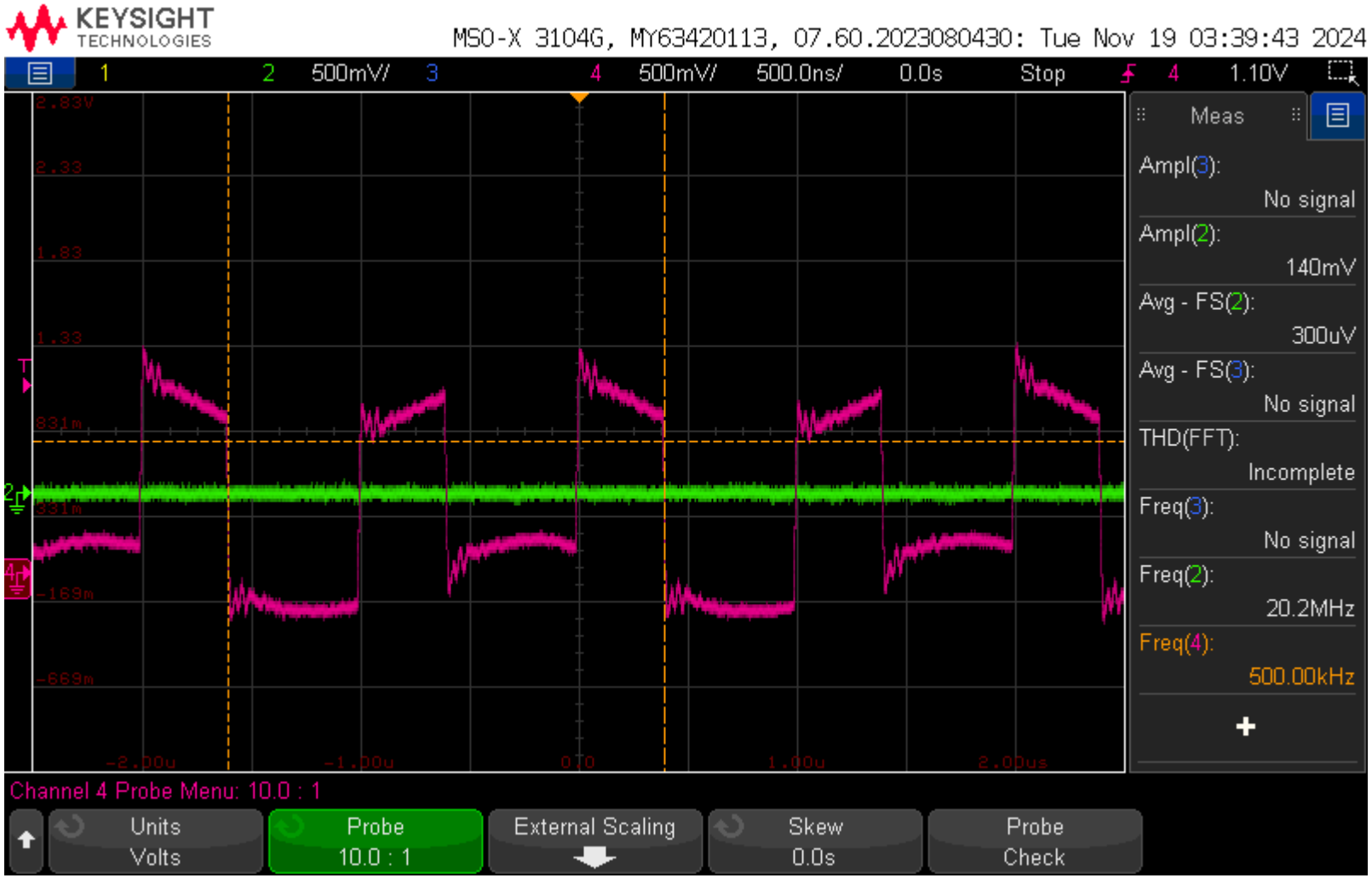
Current Issue 1.0



Period: 1u s
Freq; 1M Hz
CLK_IN

1. Connect the CLK onto the board
2. 1MHz, 0.5V Offset, 1 Vpp

Current Issue 1.1

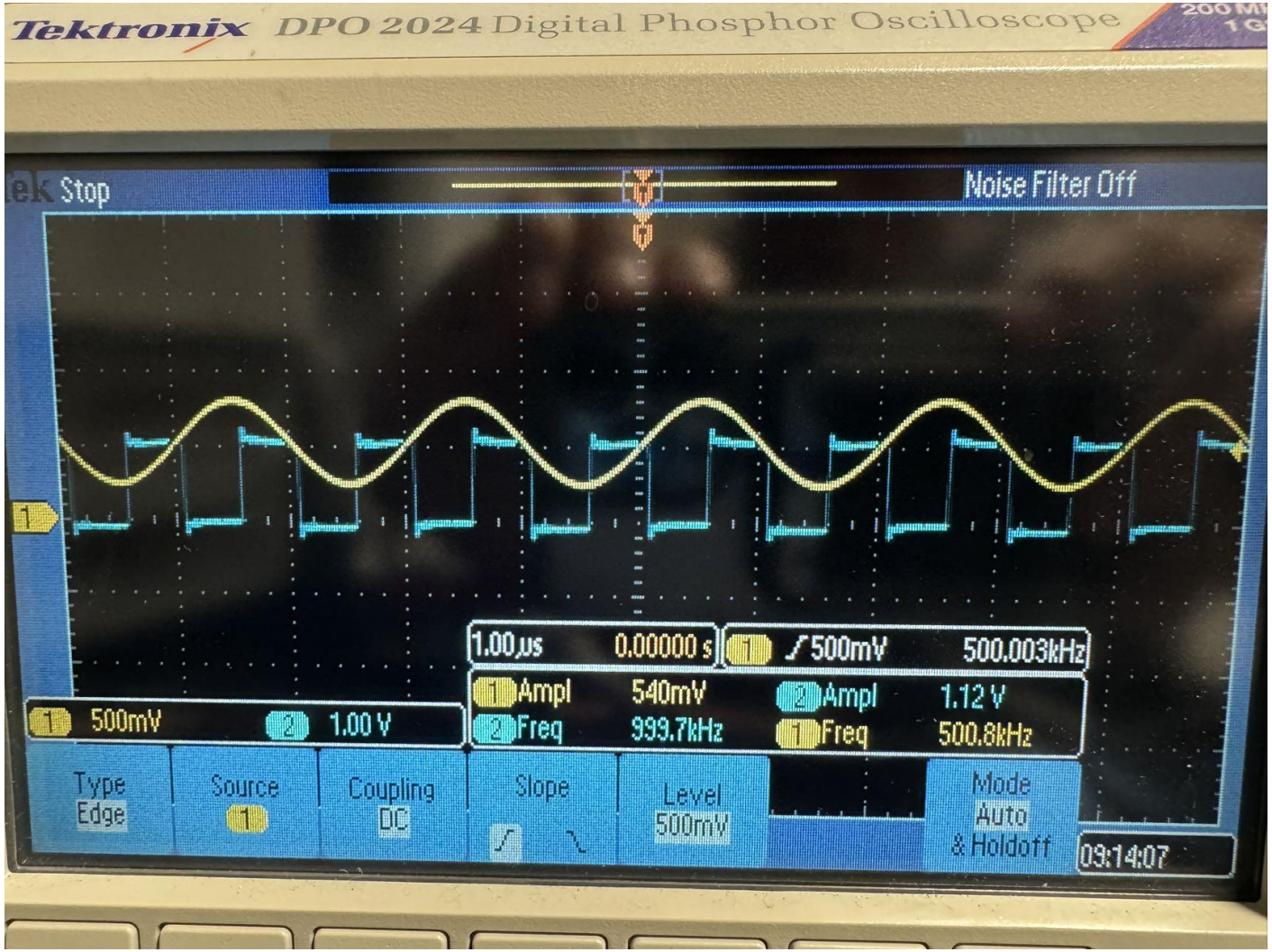


CLK_IN

1. Then connect the sine wave on to the board
2. 500kHz, 0V offset, 500m Vpp

3. Sin_IN drags the CLK frequency downs to 500KHz

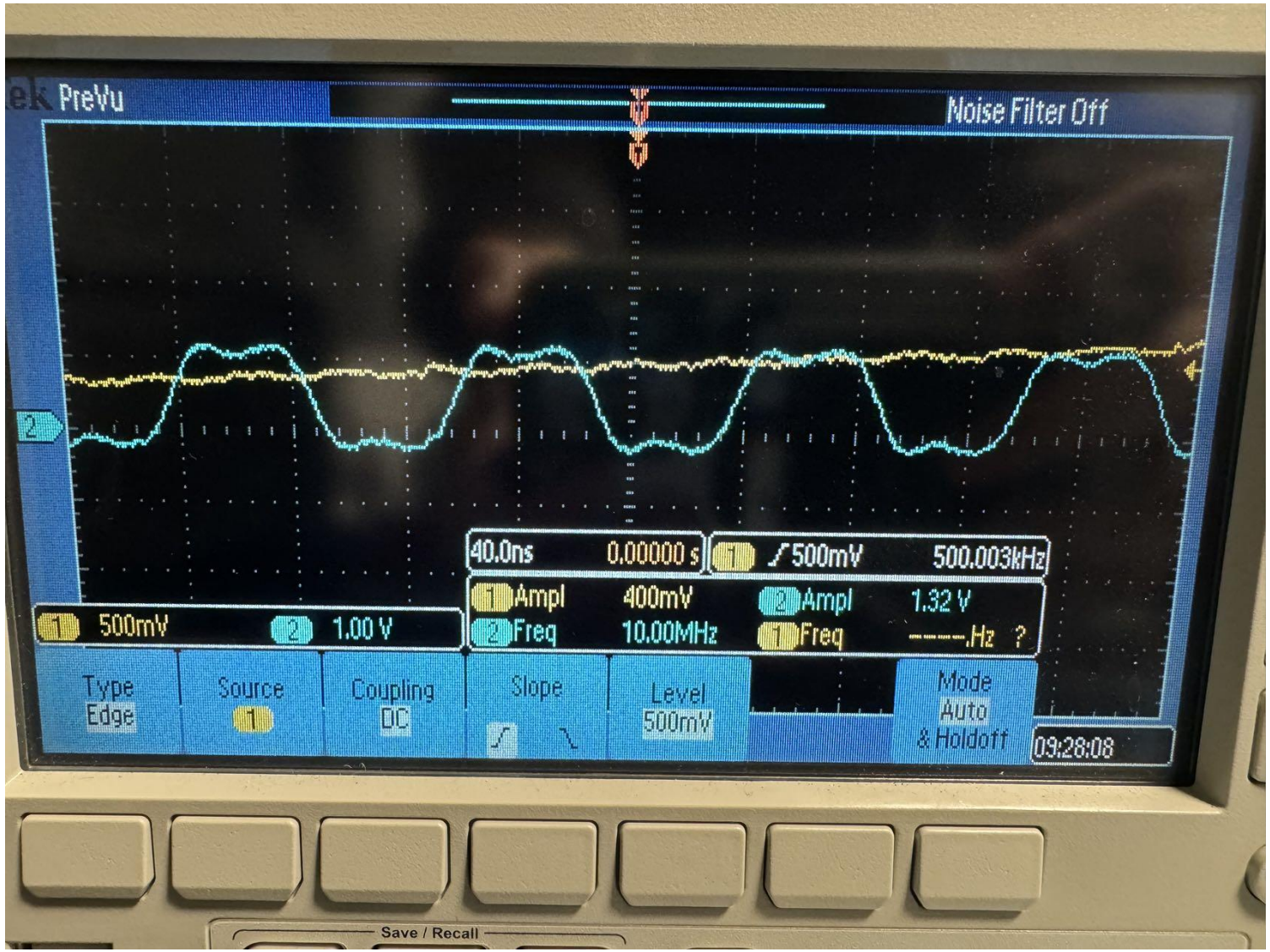
Current Issue 1.2 However…



SE_DE_POS: 0.5V offset, 0.5Vpp
CLK_IN: 0.5V offset, 1Vpp

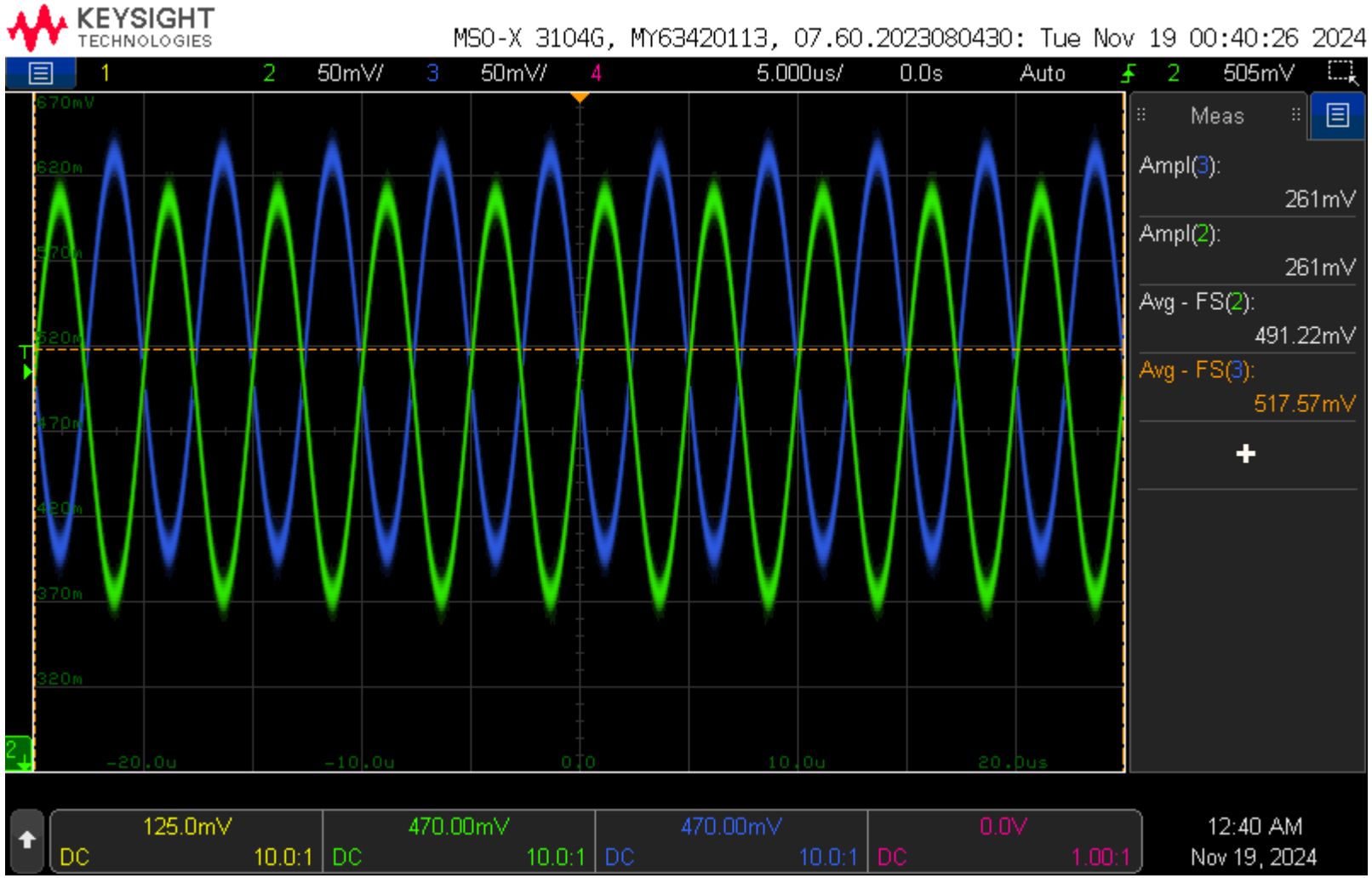
1. We tried Mingjie's Lab instrument
2. Everything looks good as expected
3. Had saved all the probes, function generator, oscilloscope, and power supply setup.
4. Will give another attempt on Wednesday in our 266B's Lab

Current Issue 2



1. Some distortion @ 10MHz CLK_IN
2. Adding lots of noise on SIN IN

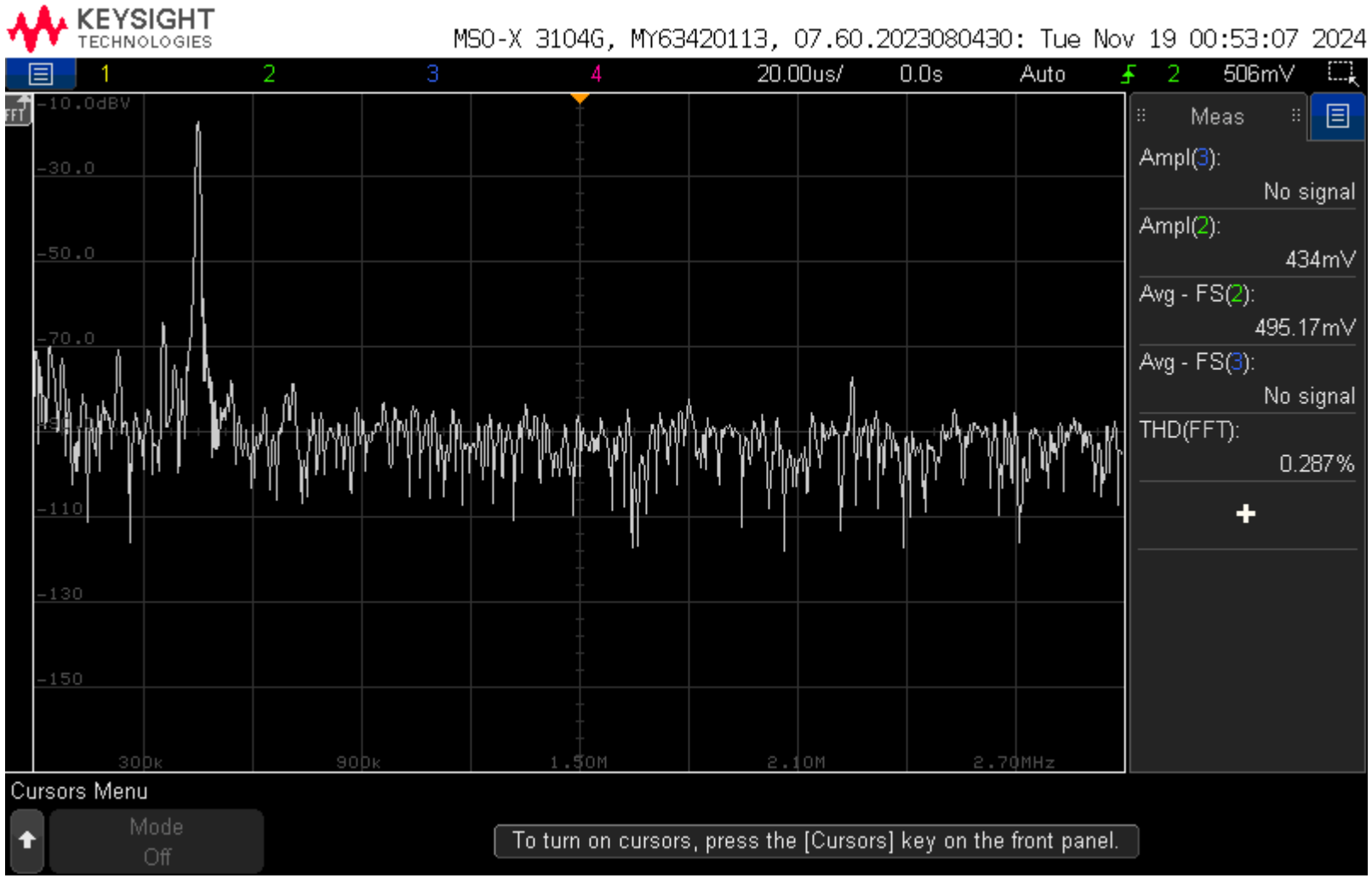
Current Issue 3 - SEDE



SE_DE_POS
SE_DE_NEG

1. Different DC offset after SE-DE
2. But similar Vpp Amplitude

FFT – one of SINE



1. -15 dBV @ fundamental frequency
2. Other tones are below -70 dBV

ADC_Test_Questions

1. What data needs to be saved to plot SNR, THD, etc…
    1. Digital code file from oscilloscope
    2. FFT Data from oscilloscope
    3. what else?