ECE 266 Lab3 Design Review

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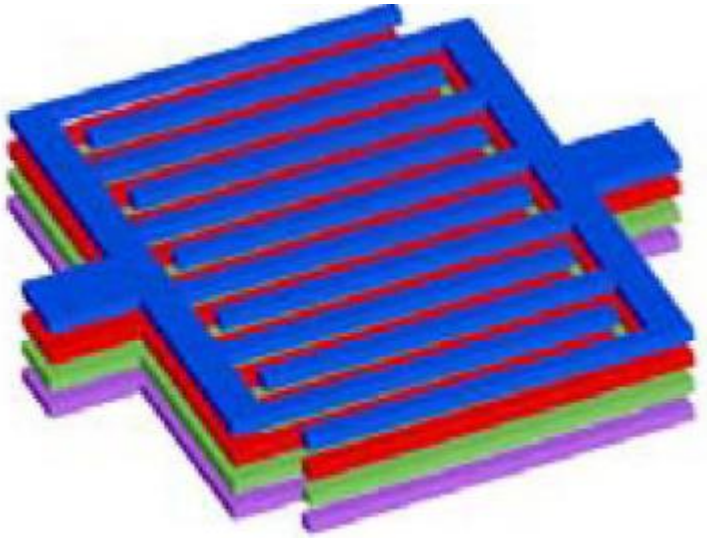
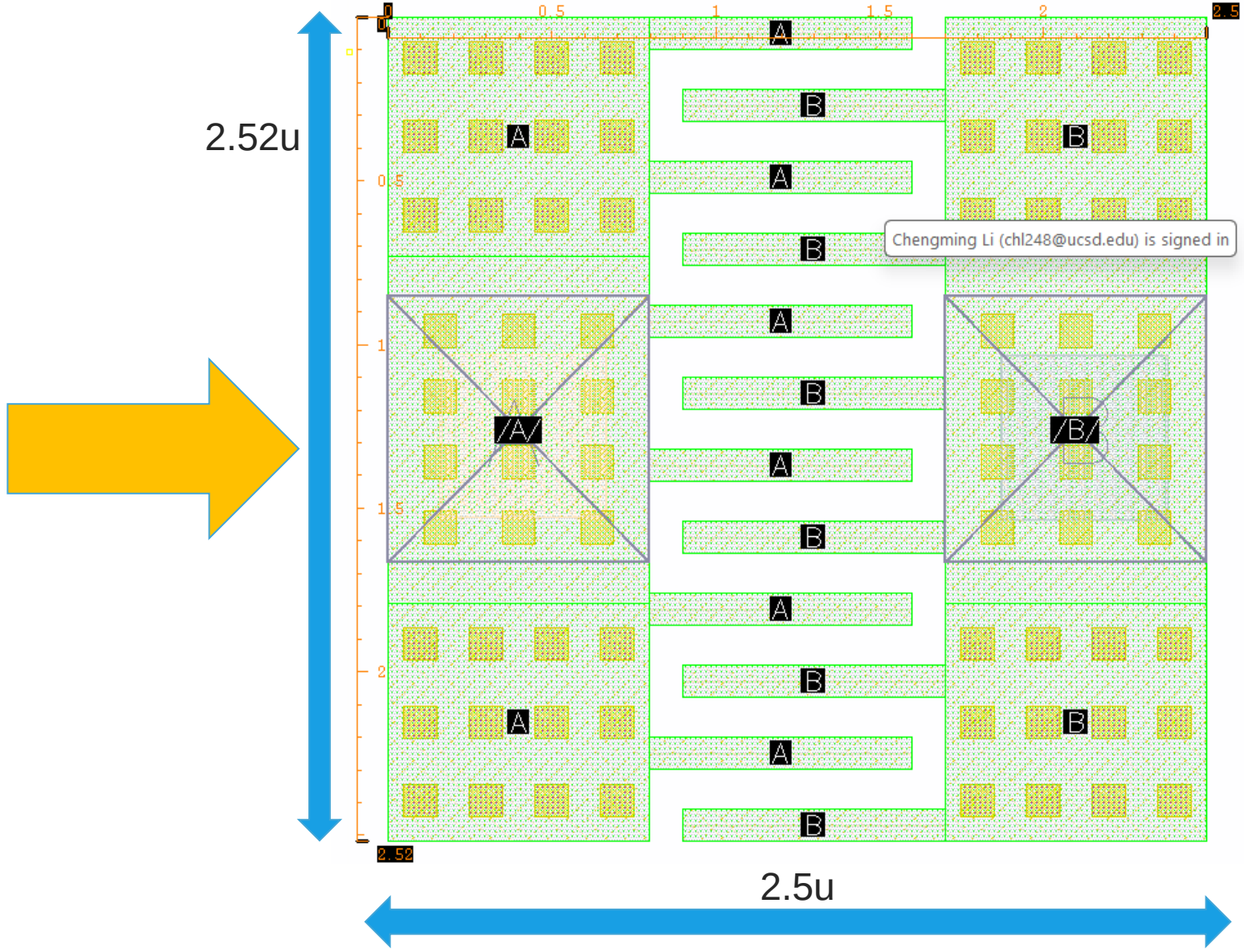
uCAP Layout

Layer: M1 to M7 stack up

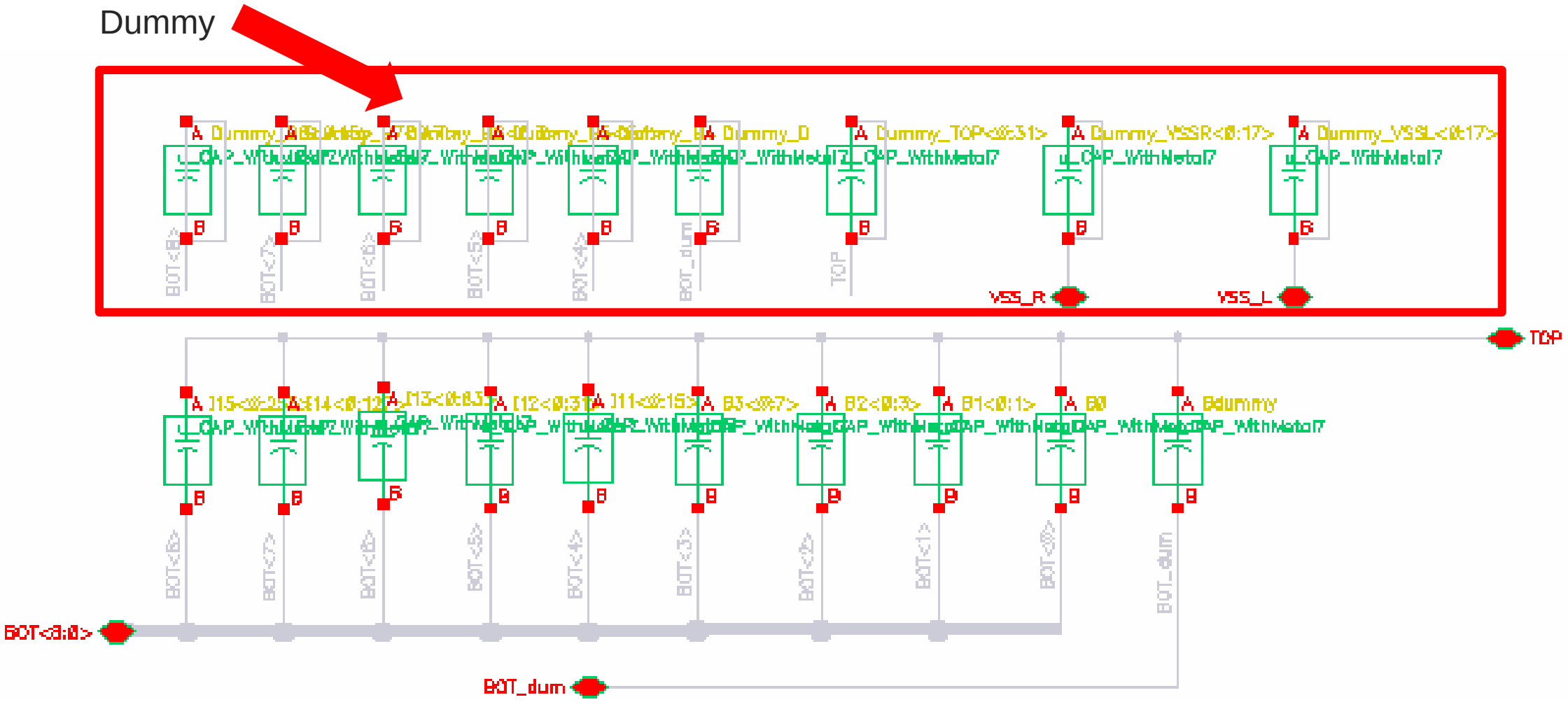
Size: 2.5u by 2.52u

CC: 5fF





Schematic-singleDAC(cap bank)



Metal Width vs. Current

- How much current we need?
  - Q = CV
  - $\frac{dQ}{dt} = I = C \times \frac{dV}{dt}$
  - $\int Idt = \int CdV$
  - $I\Delta t = C \times VDD$
  - $I(per\ unit\ Cap) = \frac{C \times VDD}{\Delta t} = \frac{5fF \times 1}{1.65us} = 3n\ A$
  - $I(per\ column) = 3n\ * 16 = 48n\ A$

- How wide of the trace should be?(Read from PDK doc)
  - M1(0.4um): 0.57 mA
  - M2 – M7 (0.4um): 0.72 mA
  - M2 – M8 (0.8um): 1.47 mA

singleDAC(cap bank) Floorplan – Common Centroid

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	2	2	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	1	1	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	D	0	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	2	2	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Bit	B0	B1	B2	B3	B4					
CC(fF)	10.14	21.8	44.04	58.25	101.5					
Ratio		2.145	2.02	1.322	1.74					

singleDAC(cap bank) Floorplan

D_VSS	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	1	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	1	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	0	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	D	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_7	D_7	D_7	D_7	D_6	D_6	D_5	D_5	D	D_4	D_6	D_6	D_7	D_7	D_7	D_7	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_VSS

Bit	B0	B1	B2	B3	B4					
C+CC(fF)	6.4994	12.333	23.683	45.248	86.676					
Ratio		1.898	1.920	1.910	1.916					

RCX Cap Table

No.	Layout Net	Source Net	C Total (F)	CC Total (F)	C+CC Total (F)
1	BOT<0>	BOT<0>	1.02960E-15	6.79001E-15	7.81962E-15
2	BOT<1>	BOT<1>	1.59393E-15	1.27679E-14	1.43618E-14
3	BOT<2>	BOT<2>	2.93767E-15	2.58180E-14	2.87557E-14
4	BOT<3>	BOT<3>	5.43015E-15	5.11647E-14	5.65949E-14
5	BOT<4>	BOT<4>	1.09642E-14	9.56543E-14	1.06618E-13
6	BOT<5>	BOT<5>	2.15877E-14	1.88712E-13	2.10300E-13
7	BOT<6>	BOT<6>	4.38039E-14	3.69387E-13	4.13191E-13
8	BOT<7>	BOT<7>	8.65712E-14	7.25979E-13	8.12550E-13
9	BOT<8>	BOT<8>	1.70076E-13	1.40478E-12	1.57486E-12
10	BOT_dum	BOT_DUM	2.35177E-15	7.57801E-15	9.92978E-15
11	TOP	TOP	2.99117E-13	2.73160E-12	3.03072E-12
12	VSS_L	VSS_L	2.11706E-14	3.46606E-15	2.46367E-14
13	VSS_R	VSS_R	2.11610E-14	3.47787E-15	2.46389E-14

Find Nets: Coupling to: All Nets Specified Nets

BOT<6> BOT<7>

Type	Count	Total	Source
C	1	8.65712E-14	
CC	9	7.25979E-13	
BOT<0>	1	6.03087E-17	BOT<0>
BOT_dum	1	4.69659E-16	BOT_DUM
BOT<2>	1	8.18673E-16	BOT<2>
BOT<3>	1	1.14413E-15	BOT<3>
BOT<4>	1	2.47462E-15	BOT<4>
BOT<5>	1	4.49197E-15	BOT<5>
BOT<6>	1	9.23773E-15	BOT<6>
BOT<8>	1	2.77877E-14	BOT<8>
TOP	1	6.79494E-13	TOP

Layout Net: BOT<7> Source Net: BOT<7> Capacitors: C (1 C, C=8.65712E-14)

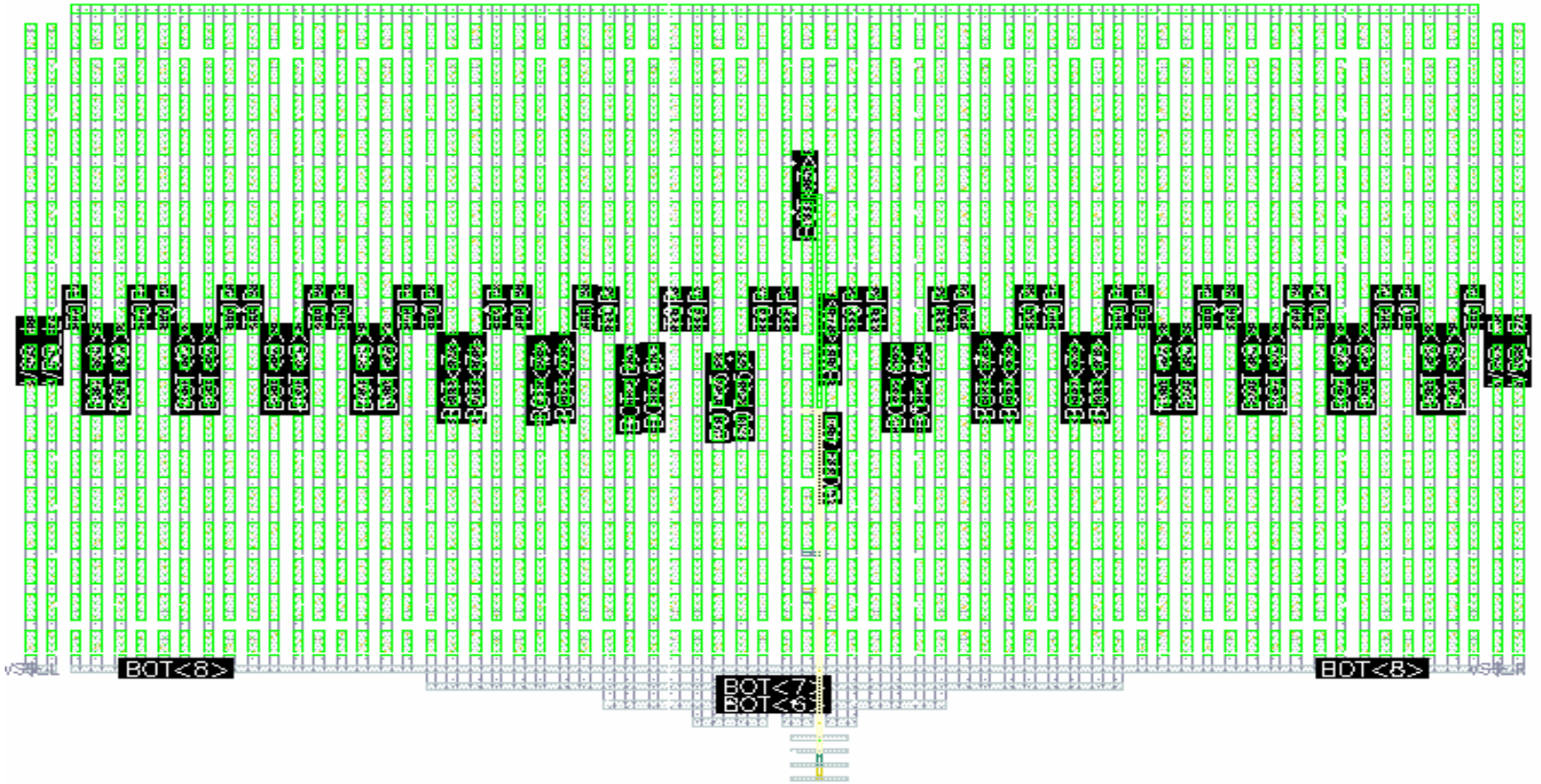
No.	Value (F)
1	8.65712E-14

Example:
Bot7
C: 86.5f F
CC:
1)Top 679.49f F
2)Bot6: 27.7 f F

Layout - singleDAC – Bit0123 - center

Non-symmetry

Bit 0:3 (M1, M3, M5, M7) overlapping



76.74u

121.97u

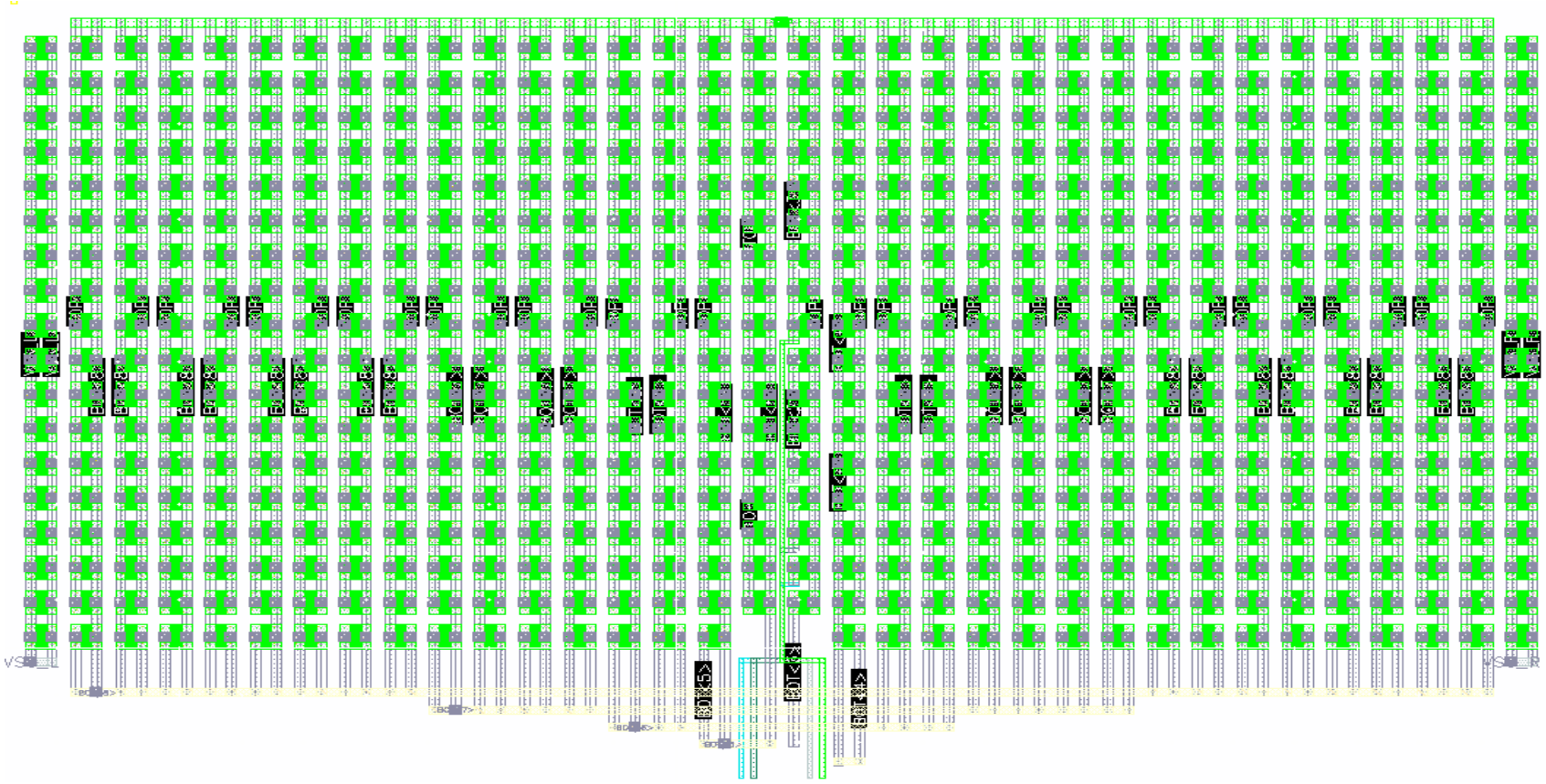
Layout - singleDAC – Remove2Dummy

Pro:

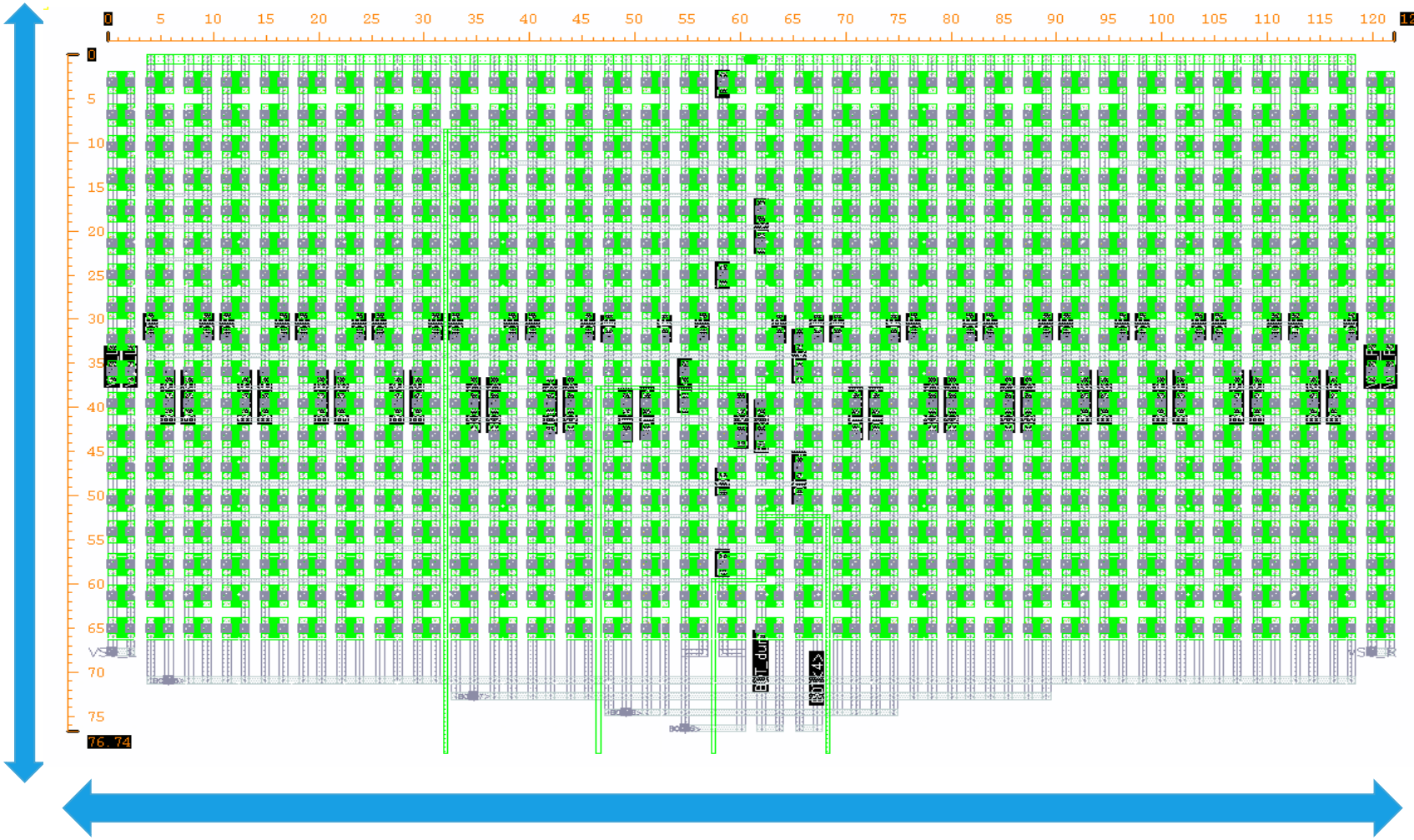
- Symmetry
- Less CC between Bits and
- Less CC effects to the Dummy for bit0

Cons:

- Sensitive to C(w.r.t substrate)
- Sensitive to the length of Bit 0:3
- Non-binary routing



Layout - singleDAC – Robust C+CC



Improvement:

- Higher metal used for M0:3
- Binary routing
- Robust C+CC sensitivity

RCX Cap Table

Bit	B0	B1	B2	B3	B4	B5	B6	B7	B8
C+CC(fF)	7.819	14.36	28.755	56.594	106.62	210.30	413.19	812.55	1574.86
Ratio		1.84	2.00	1.97	1.88	1.97	1.96	1.97	1.94

Appendix – Old Version uCap