ECE 283 Lab3 Final Design Review

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Agenda

1. Project Background & Introduction
2. Test-Performance Overview
3. Chip Design Review in Cadence
4. Chip-Testing Review
5. Takeaway

Project Background & Introduction

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Project Background & Introduction

1. ECE266A - 9-bit high speed(Fs = 10M Hz) SAR ADC
    1. Layout-focus Design
        1. Comparator, CDAC, Digital logic, Non-overlapping clock generator, switches
    2. Mega-Chip combinations
        1. 4 groups of chip into one BIG CHIP
        2. Dummy fill, seal ring, custom pads, custom-DeCaps, wavier submission
2. ECE266B – SAR ADC Testing
    1. PCB Design
        1. Mother(4-Layer) and daughterboard(2-Layer) combination
        2. Custom ADC chip footprint + Wirebonding Diagram
    2. Soldering & Assembly
        1. 0604 & 0802 Surface mount soldering
    3. Device characterization & Test - Automation
        1. Test Automation using Keysight instruments in Python
        2. Data processing and plotting in MatLab

Test - Performance Overview

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Test - Specs Overview

Speces	Performance
$SNDR_{peak}$ @ 1kHZ	50.23 dB
$SFDR_{peak}$ @ 1kHZ	61.45 dB
SNR_{peak} @ 1kHZ	50.68 dB
$THD_{2,peak}$ @ 1kHZ	78.36 dB
$THD_{3,peak}$ @ 1kHZ	61.45 dB

Chip Design Review in Cadence

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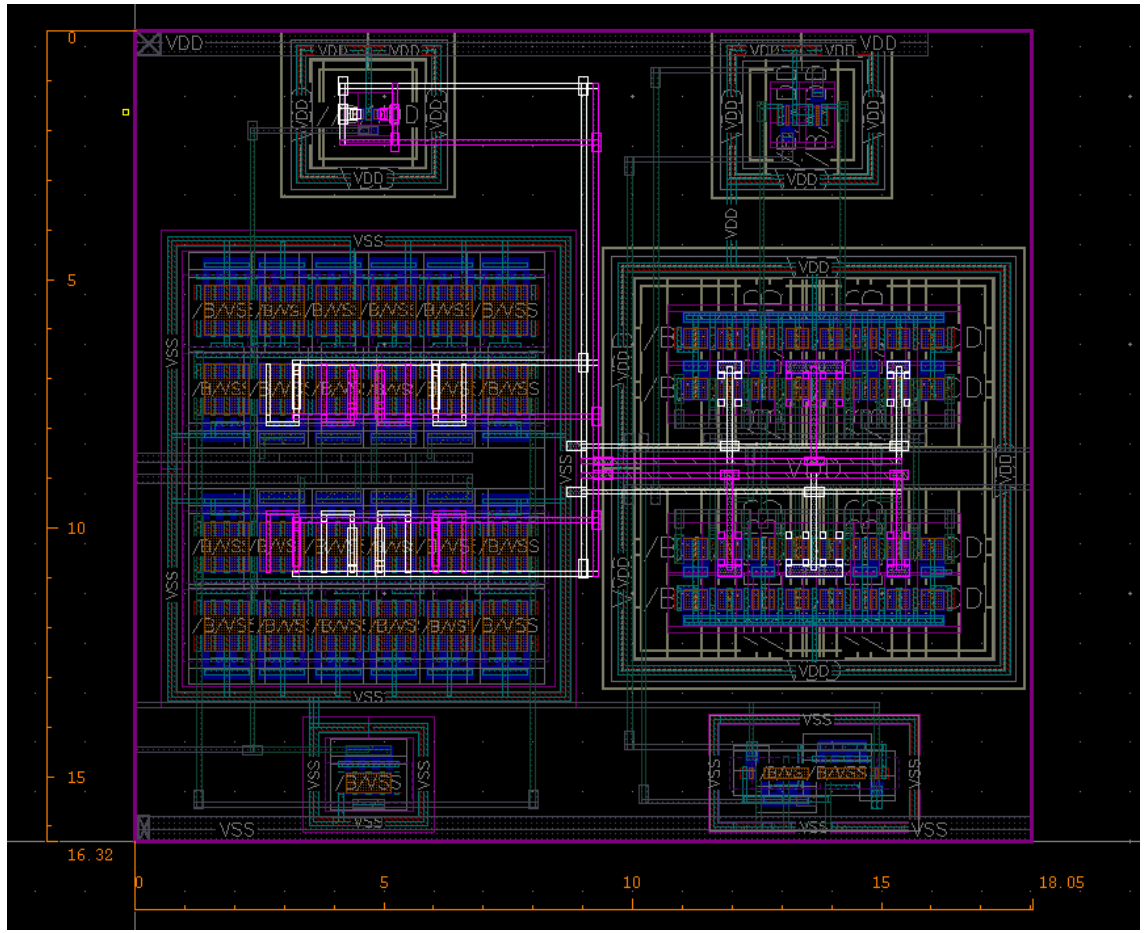
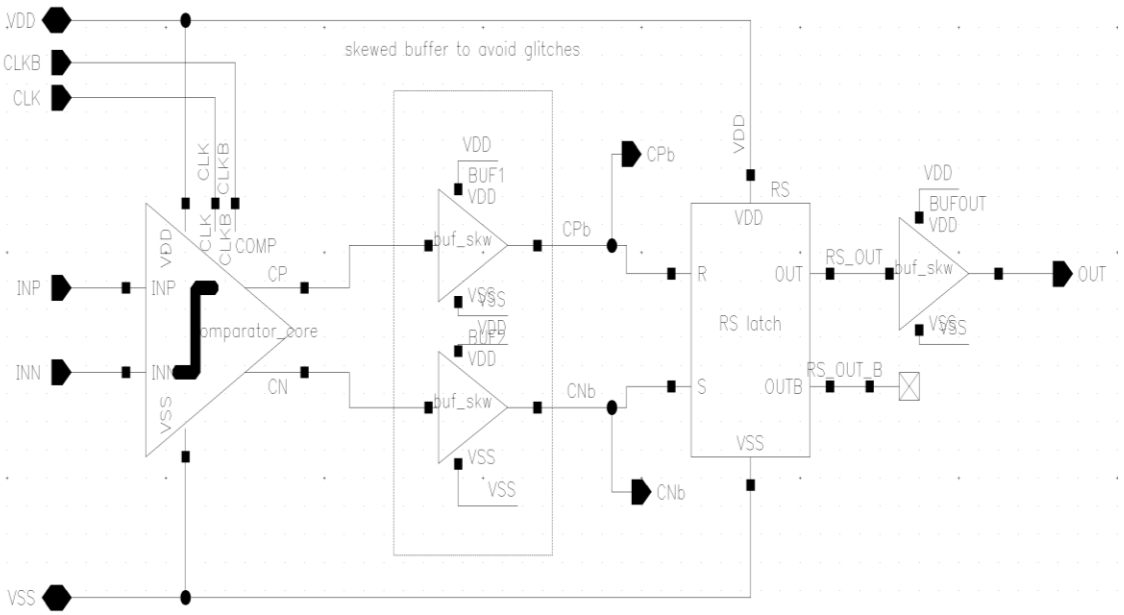
Comparator Remarks

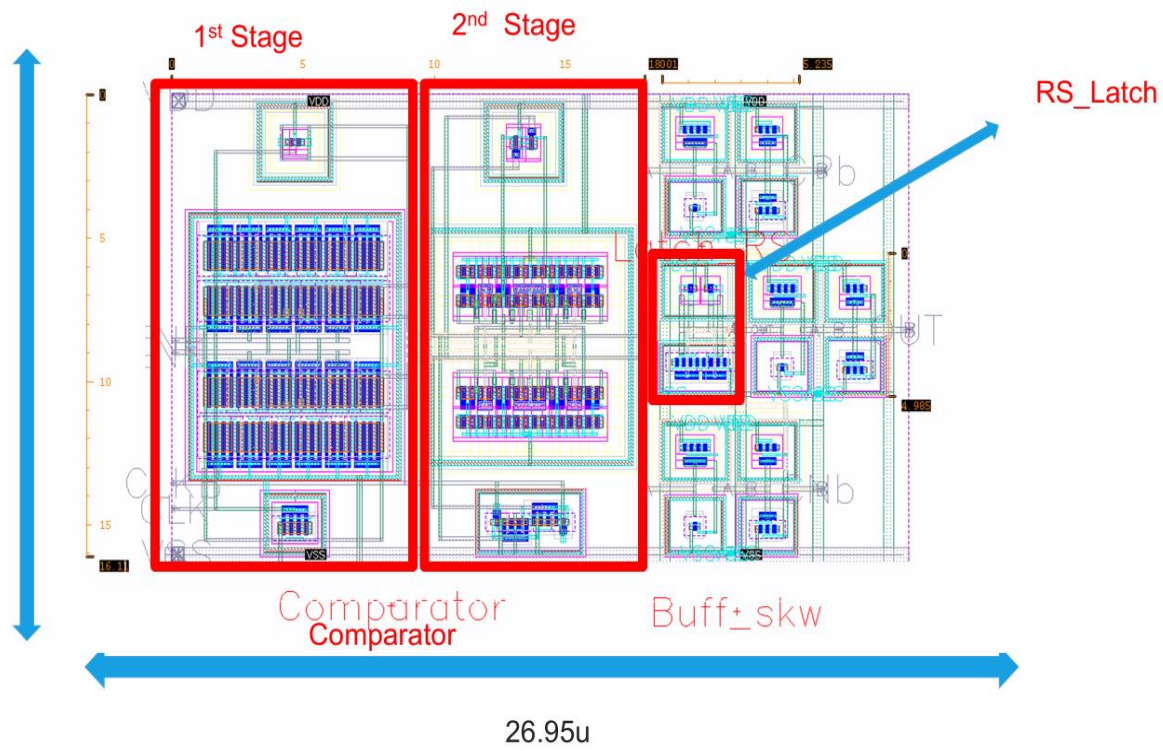


- Symmetry layout in differential pair
- Achieved 90uV offset in the differential pairs

Source Net	C+CC (F)	Difference(%)
FP(Hightlight)	9.8649f	
FN(Highlight)	9.89668f	-0.32%
CP	6.76178f	
CN	6.68441f	1.144%
INP	5.42497f	
INN	5.40371f	0.39%

Comparator Layout



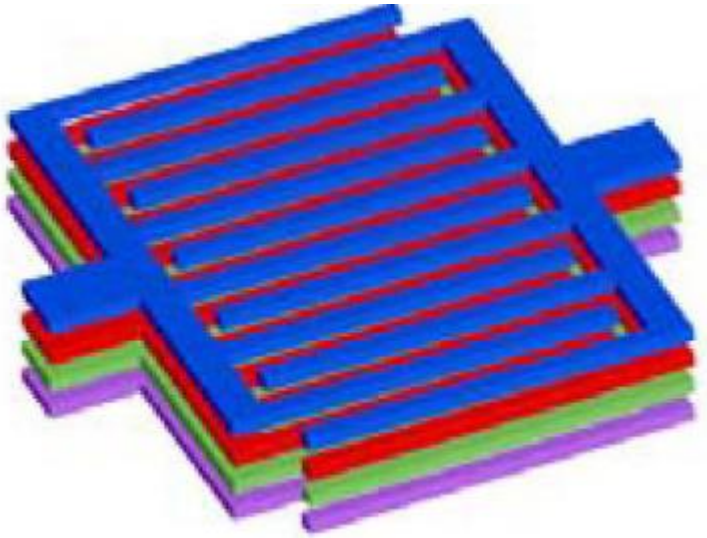


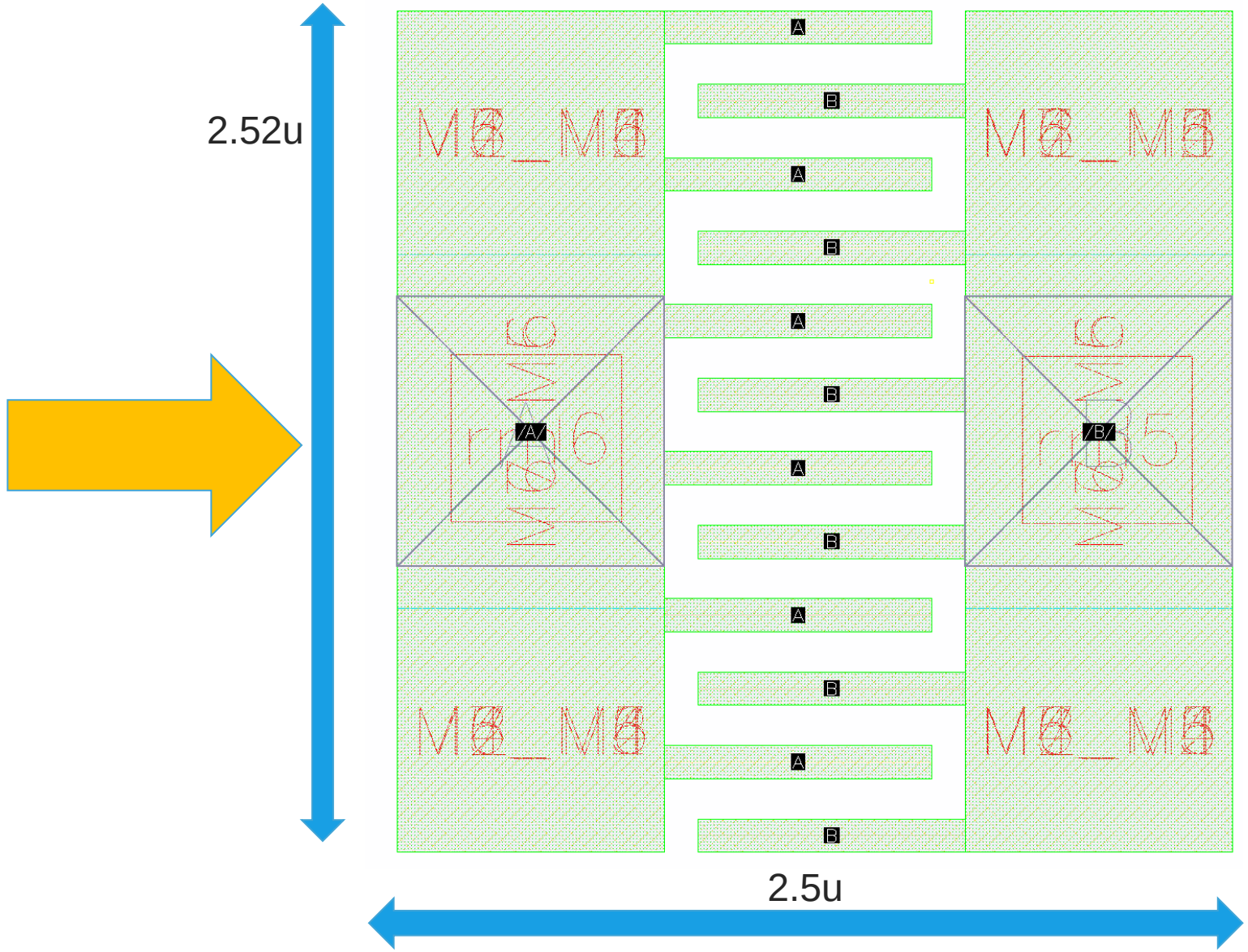
Custom unit Cap Remarks

Layer: M1 to M7 stack up

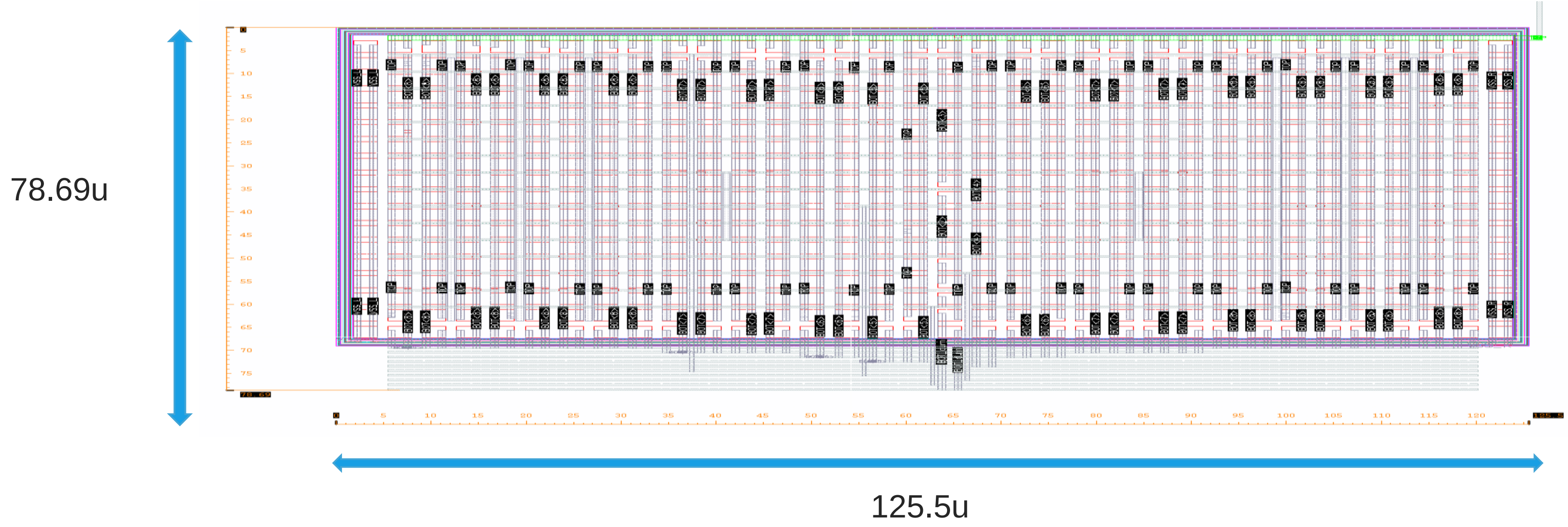
Size: 2.5u by 2.52u

CC: 5fF





CDAC Remarks -1



D_VSS	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
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D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	1	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
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D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	0	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	D	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_7	D_7	D_7	D_7	D_6	D_6	D_5	D_5	D	D_4	D_6	D_6	D_7	D_7	D_7	D_7	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_VSS

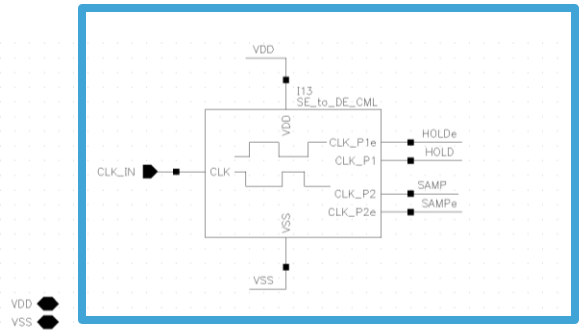
CDAC Remarks -2

Bit TopP	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51874	11.0181	21.9972	44.1238	88.179	176.362	352.691	705.664	1413.44
Ratio		1.9996	3.9859	7.9952	15.9781	31.9569	63.9080	127.866	256.116

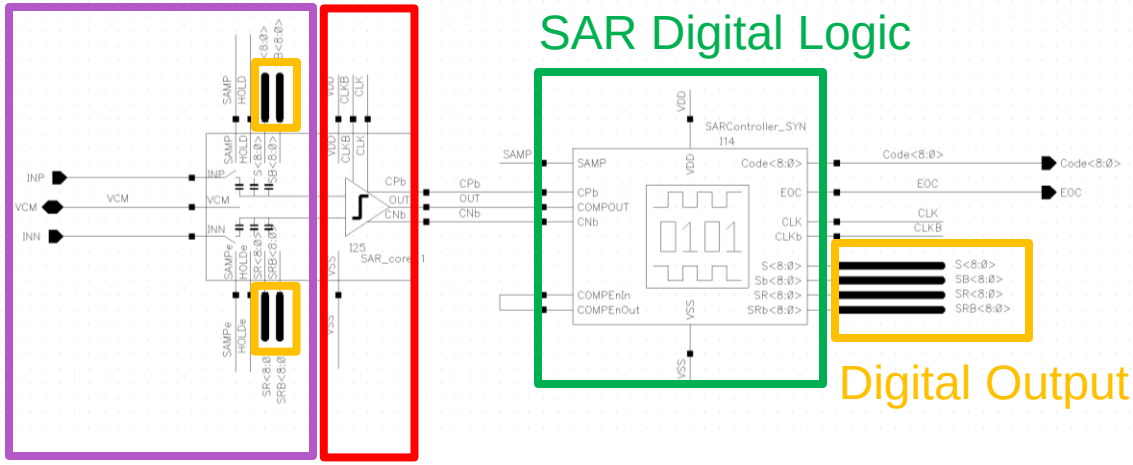
Bit TopN	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51138	11.0222	21.9988	44.1662	88.2156	176.425	352.801	705.712	1413.26
Ratio		1.9998	3.9915	8.0136	16.0060	32.0110	64.0131	128.046	256.425

Final Layout – SAR-ADC

SE-DE-Nonoverlapping Generator



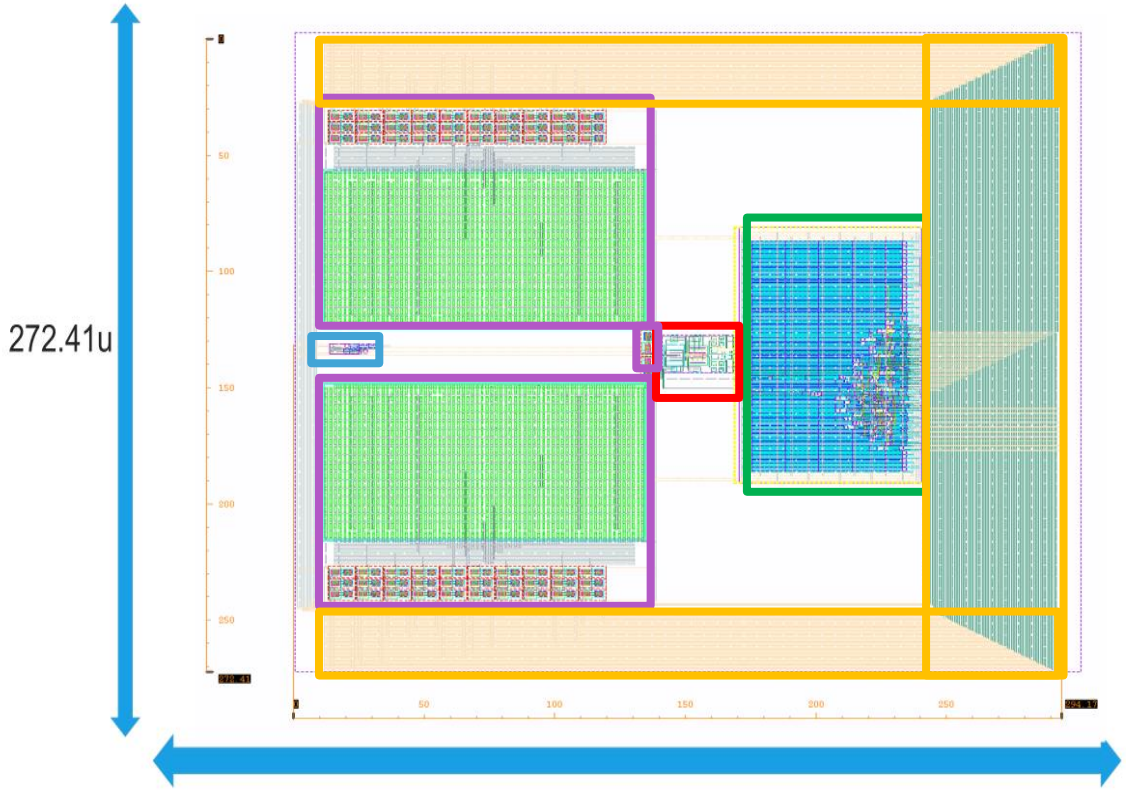
SAR Digital Logic



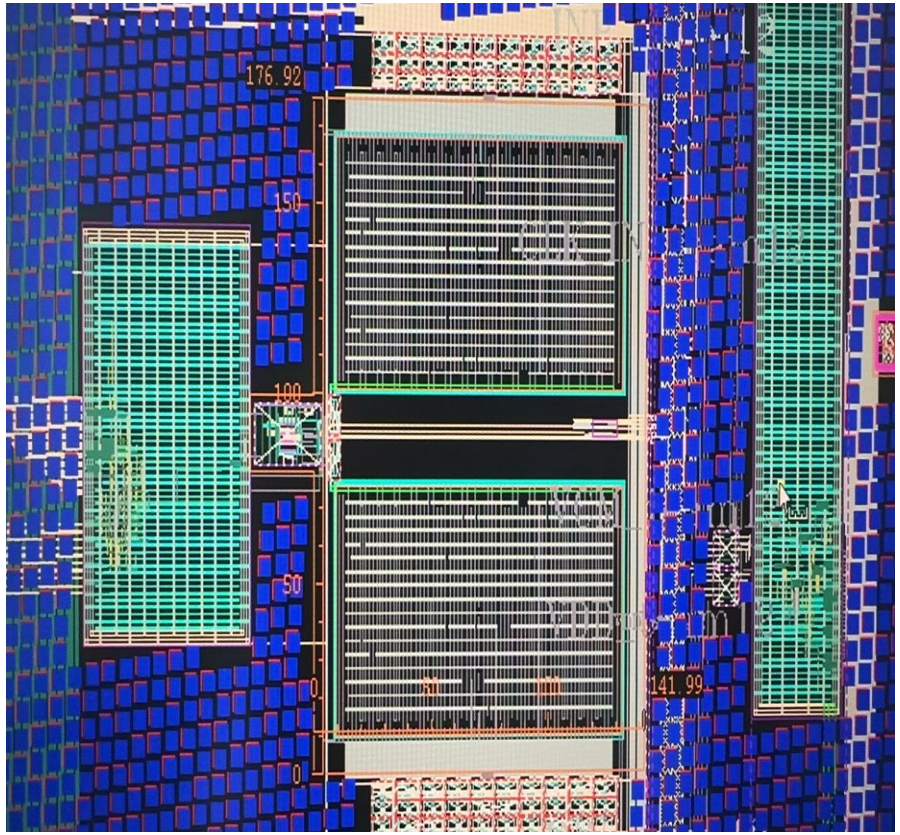
Digital Output

CDAC & Switch Array

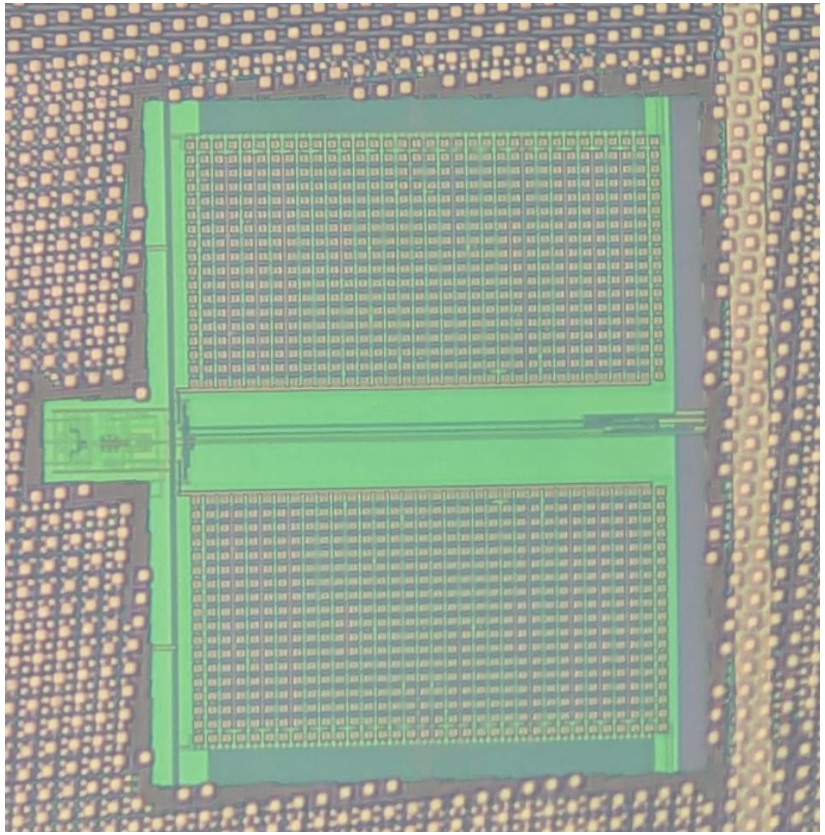
Comparator



Final Layout – SAR-ADC after Dummy Fill



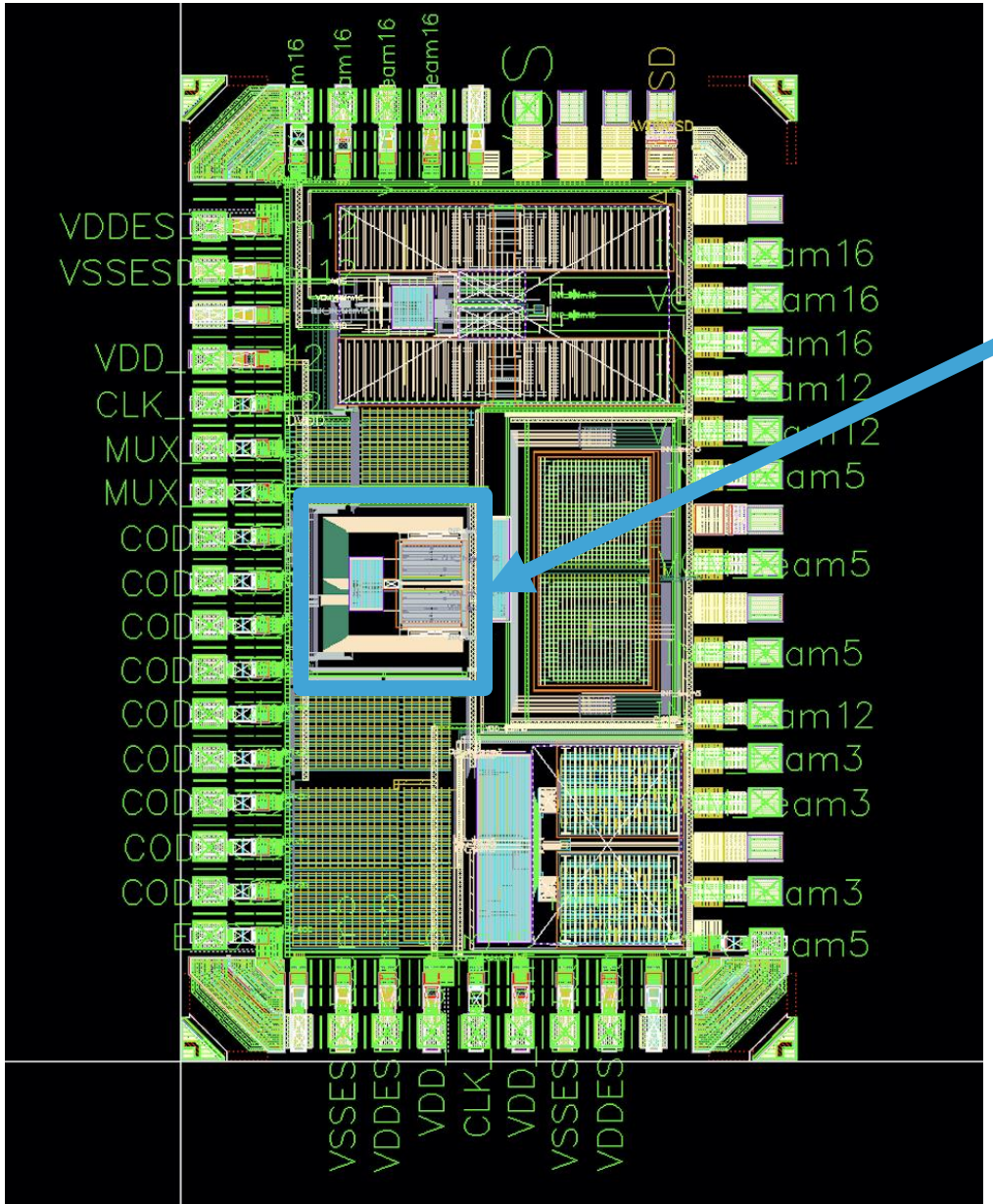
Layout after dummy fill



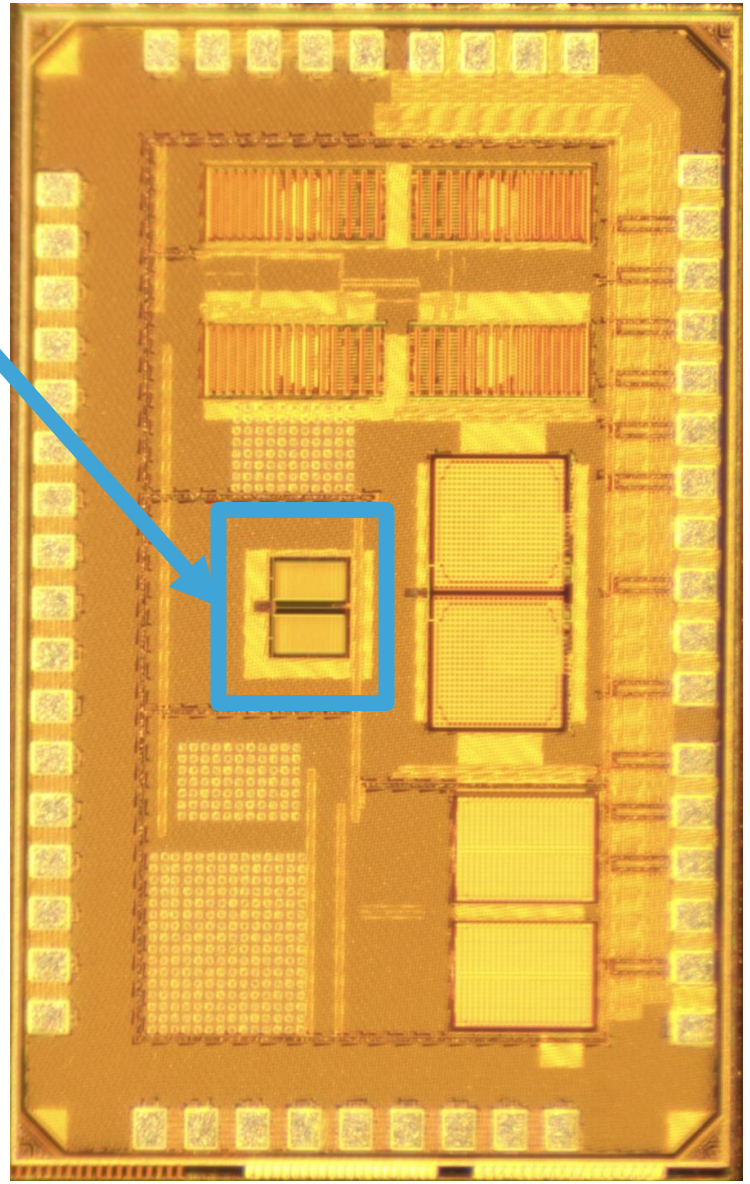
Die Photo

SNR: 52.3 dB after dummy fill

Mega Group 2 Chip Photos



Location of our SAR Core



Chip-Testing Review

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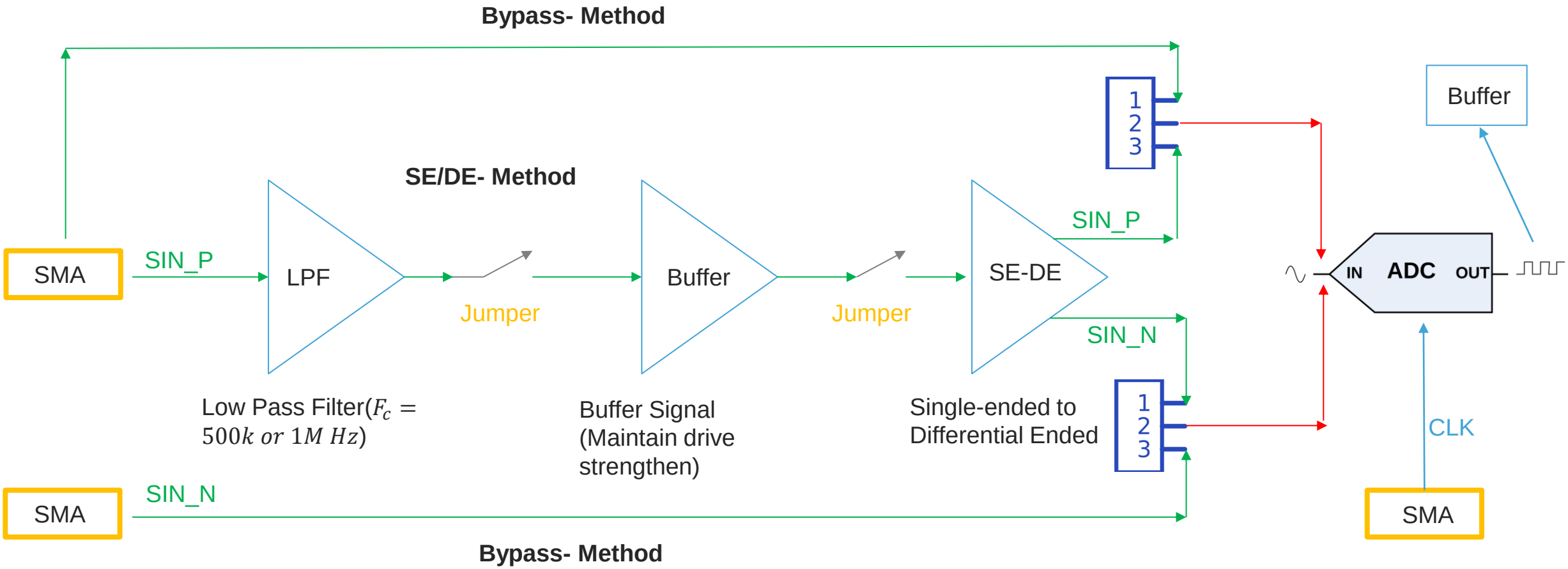
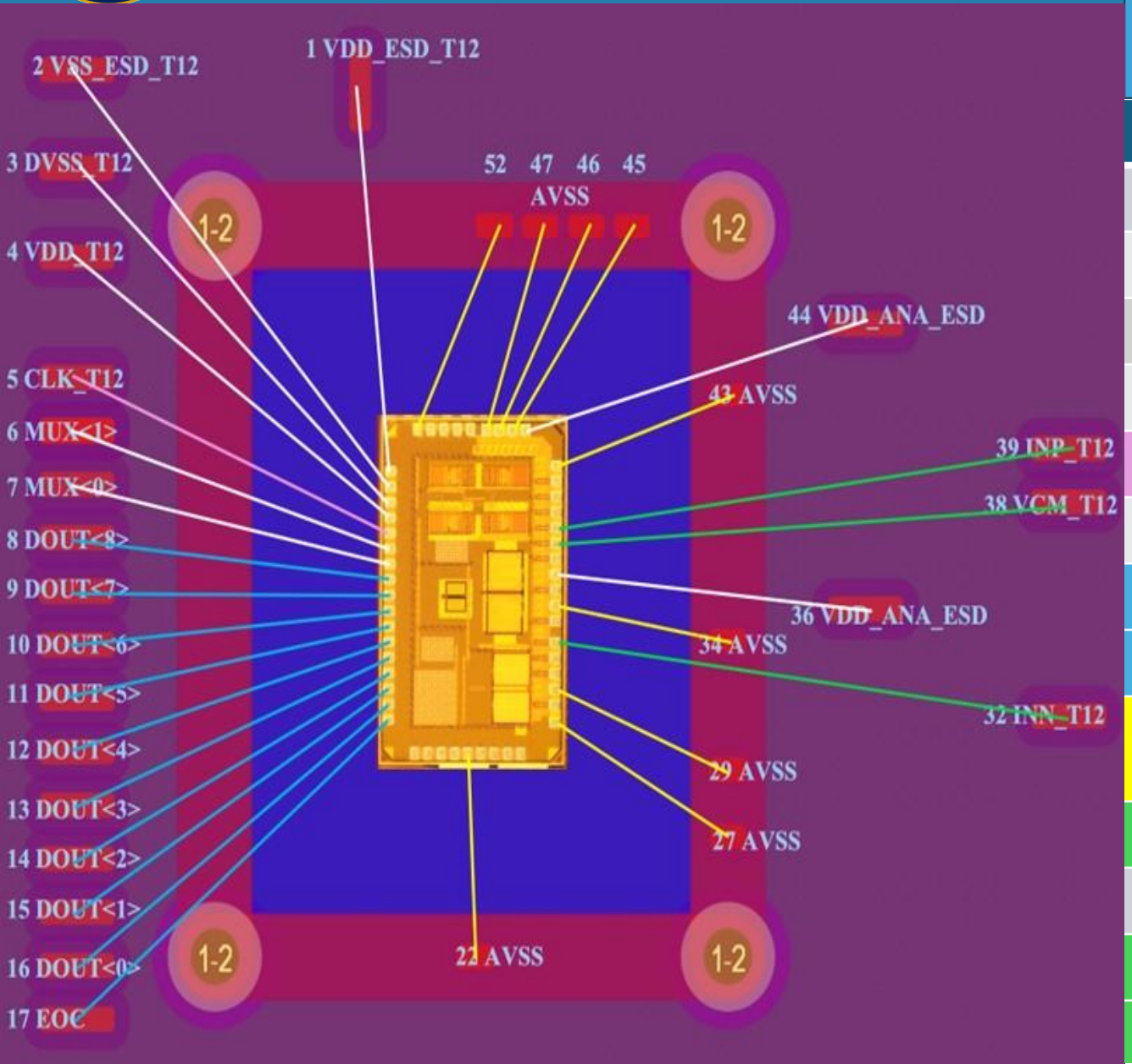
MotherBoard BlockDiagram

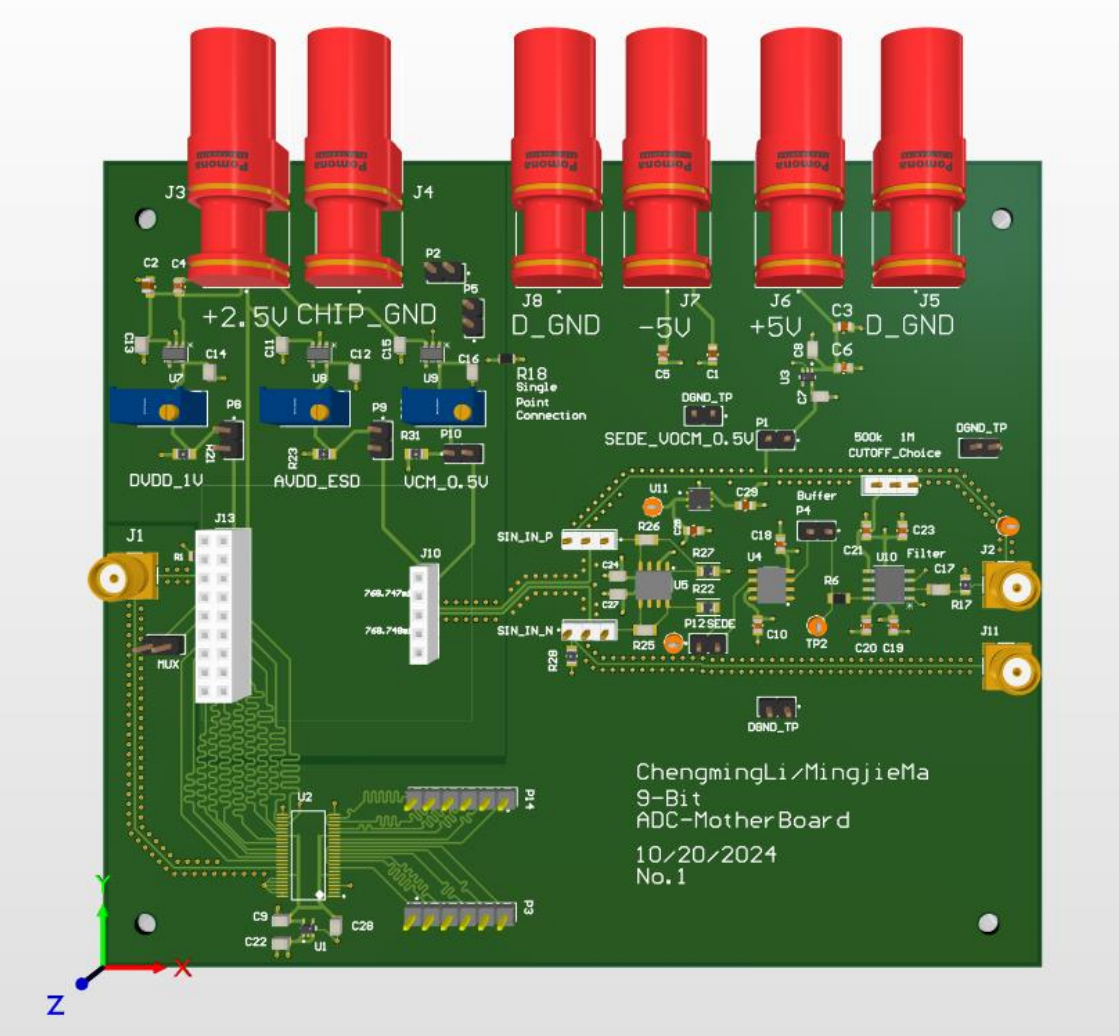


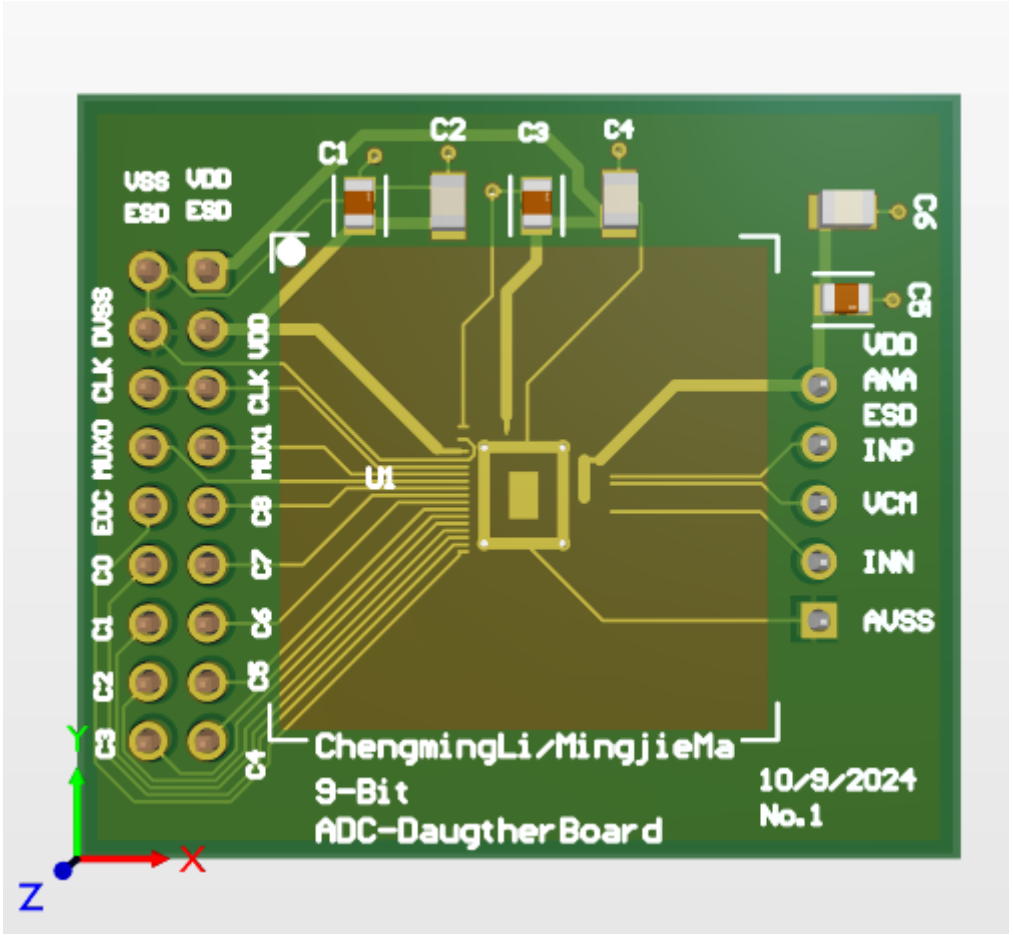
Chip Package and Wire bonding Diagram



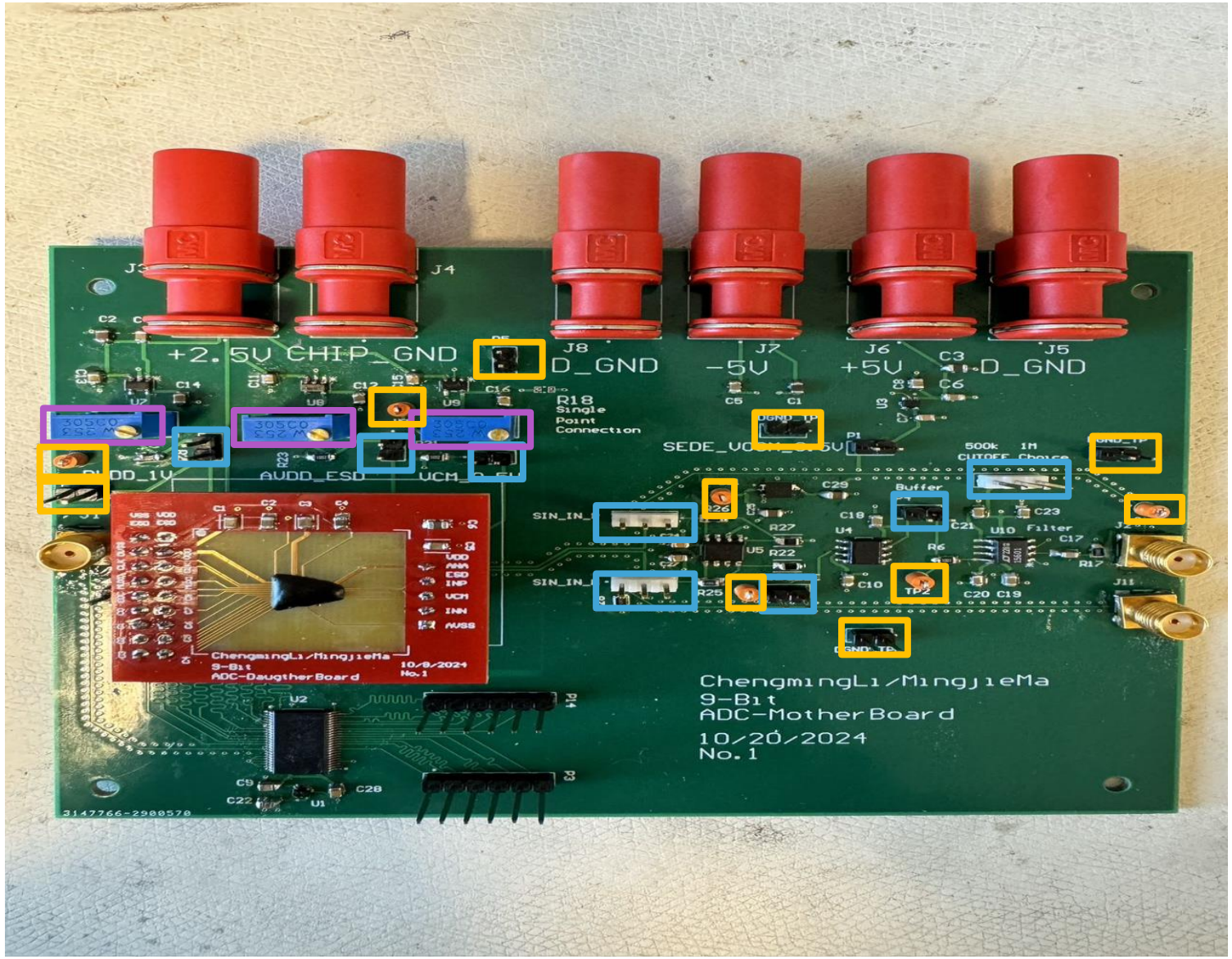
Pin Number	Type	Description
1	Power	VDD_ESD
2	Power	VSS_ESD
3	Power	DVSS_T12
4	Power	VDD_T12
5	Digital Input	CLK_T12
6/7	Digital Input	MUX_SEL
8 - 16	Digital Output	ADC_RESULT
17	Digital Output	EOC
22/27/29/34/43/45/ 46/47/52	Power	AVSS
32	Analog Input	INN_T12
36/44	Power	VDD_ANA_ESD
38	Analog Input	VCM_T12
39	Analog Input	INP_T12

MotherBoard + DaugtherBoard 3D





MotherBoard + DaugtherBoard



1. Modularized the Design
    1. By having jumper between each IC
    2. For debugging
    3. SE-DE / ByPass Options
2. Testability
    1. Jumper for GND for easy probeing
    2. Grab & Probe
3. Configurability
    1. Potentiometer for tweaking the perfect Vcm, AVDD, AVDDESD
4. 4-Layer Stack
    1. Signal
    2. DGND + AGND
    3. +5V
    4. -5V

Board Bring-up Checklist

Test No.	Test Plan	What Components	What Exepect to See	Status	Notes
	Power Supply Test				
0	Produce -5 V and 5 V on breadboard	Breadboard and Power supply with 3 separate power supply	Neg 5V and Pos 5V	Pass	
1	After connecting 2.5V, Measure the LDO U7 U8 U9's output	U7, U8, U9	1.5V @ Pin 5 of LDOS	Pass	
2	After connecting -5 V and 5V, makre sure power vias are shown 5V and -5Vcorrectly	3-Pins Jumer near the Vsin_IN_NP	Pos 5V on the leftmost pin and Neg 5V on the rightmost	Pass	
3	LDO U3 regulated down from 5V to 2.5	P1 Jumer Right Most Pin	2.5V on P1 rightmost	Pass	
4	LDO U11 regulated down from 2.5V to 0.5V	Jumer head in P1, U11's Pin 1 and 2, and TP	0.5V on TP	Pass	
5	Tweak Potentiometer U7 to get 1V for DVDD	Potentiometer near U7, Jumer Top pin	1V DVDD @ Jumer Top Pin	Pass	
6	Tweak Potentiometer U8 to get 1V for AVDDESD	Potentiometer near U8, Jumer Top pin	1V AVDD_ESD @Jumer Top Pin	Pass	
7	Tweak Potentiometer U9 to get 0.5V VCM	Potentiometer near U9, Jumer left pin	0.5V VCM @Jumper Left Pin	Pass	
	Sig_IN Test				
0	Connect 200K Hz Offset 0V, Amp 0.4V Sine wave into J2 SM	J2 SMA, TestPoint Near J2	200K Hz Offset 0V, Amp 0.4V Sine wave	Pass	
1	U10(LPF) Connect to 1M filter choice 200K Hz Offset 0V, Amp 0.4V Sine wave shows up at P4, no distortion	U10 filter choice jumer, jumper head, P4 right pins, TP2	200K Hz Offset 0V, Amp 0.4V Sine wave into J2	Pass	
2	Connect P4 Jumer, siganal go through U4 buffer and measure P12 Output	U4, P12 rightmost Pin	200K Hz Offset 0V, Amp 0.4V Sine wave	Pass	
3	U5(SE_DE) signal coming from P12, Measure SIN_IN_P and SIN_IN_N Sig property	P12 Jumer head SIN_IN_P header and SIN_IN_N header right most pin	SIN_P: 200K Hz Offset 0.5V, Amp 0.4V Sine wave SIN_N: 200K Hz Offset 0.5V, Amp 0.4V Sine wave, 180 out of phase	Pass	
	Digital Test				
0	CLK Connect to J1	J1		Pass	
1	MUX Choice	Used female to female jumer to connect the MUX choices		Pass	MUX0: 1, MUX1: 0

1. By knowing what to expect after each IC
2. Actual vs. Expect
3. Handy to debug the problem

Test Setup Documentation

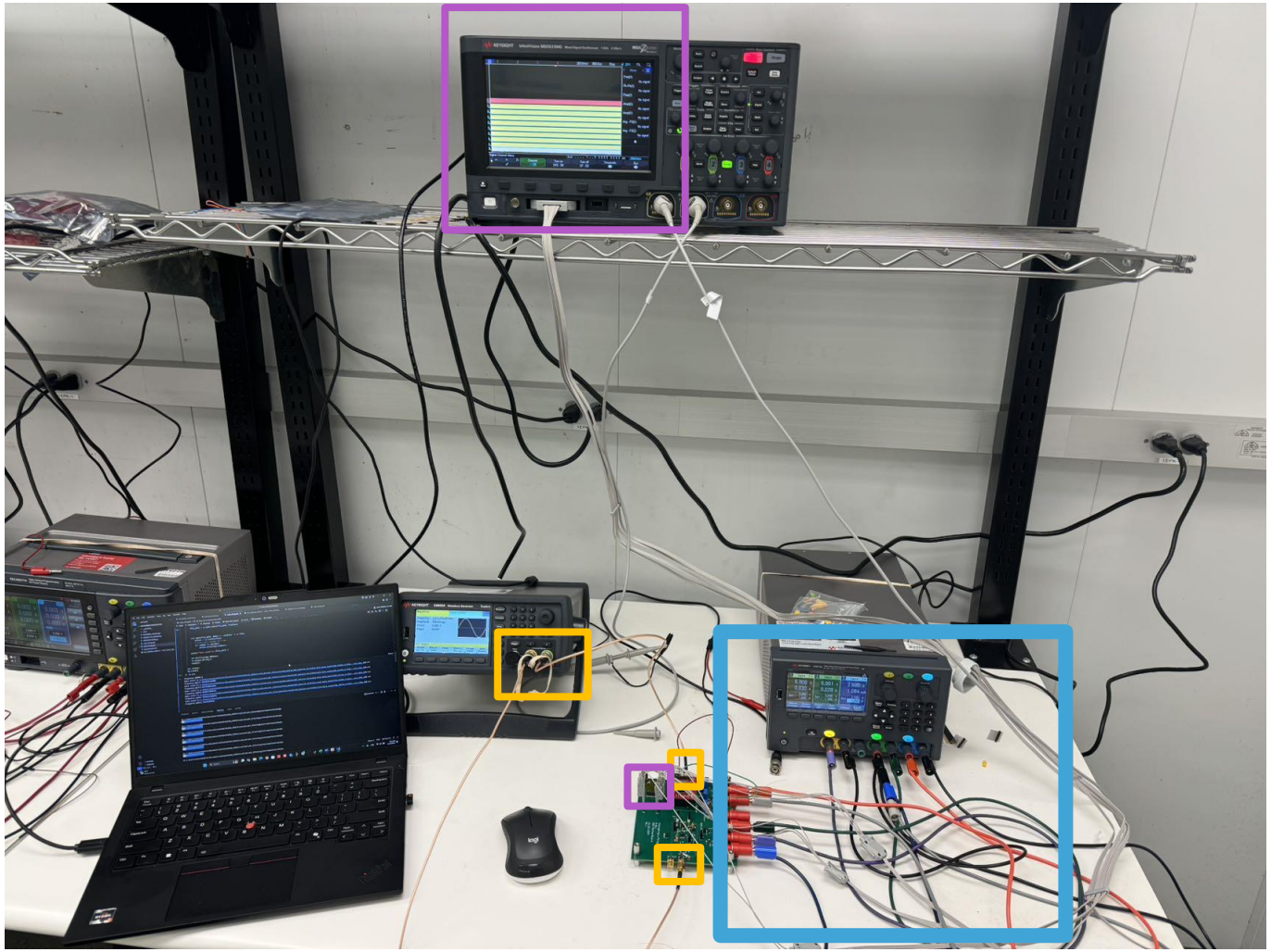
SE-DE Test Setup

1. Power Supply
    a. 1 channel is used as 5V, 0.2A
    b. 1 channel is used as -5V, 0.2A
    c. 1 channel is used as 2.5V, 0.2A
2. Function Generator
    a. SIN Input - Channel 1
        i. High-Z Load
        ii. 1Vpp
        iii. 0 V offset
        iv. Frequency at 1KHz as initial
    b. Clock Input – Channel2
        i. High-Z Load
        ii. 2.5 Vpp
        iii. 1.25 Offset
        iv. Frequency at 1MHz
        v. Duty Cycle 50%
    c. Sync Both Channels every time the parameters are changed
3. Oscilloscope
    a. Time Base 1ms/div
    b. Digital Bus1
        i. Digital Code 0-8 (C0-8)
        ii. Digital Code 11 - End of Code (EOC)
        iii. Trigger Level 1.8V
        iv. Turns off Others
    c. Trigger Source
        i. EOC, D11 Rising Edge
        ii. Possibly CLK from Function Generator OR CLK from buffer
    d. Collect data
        i. Stop or Single
        ii. MSB First
        iii. ASCII format
        iv. Maximum Points

Bypass Setup

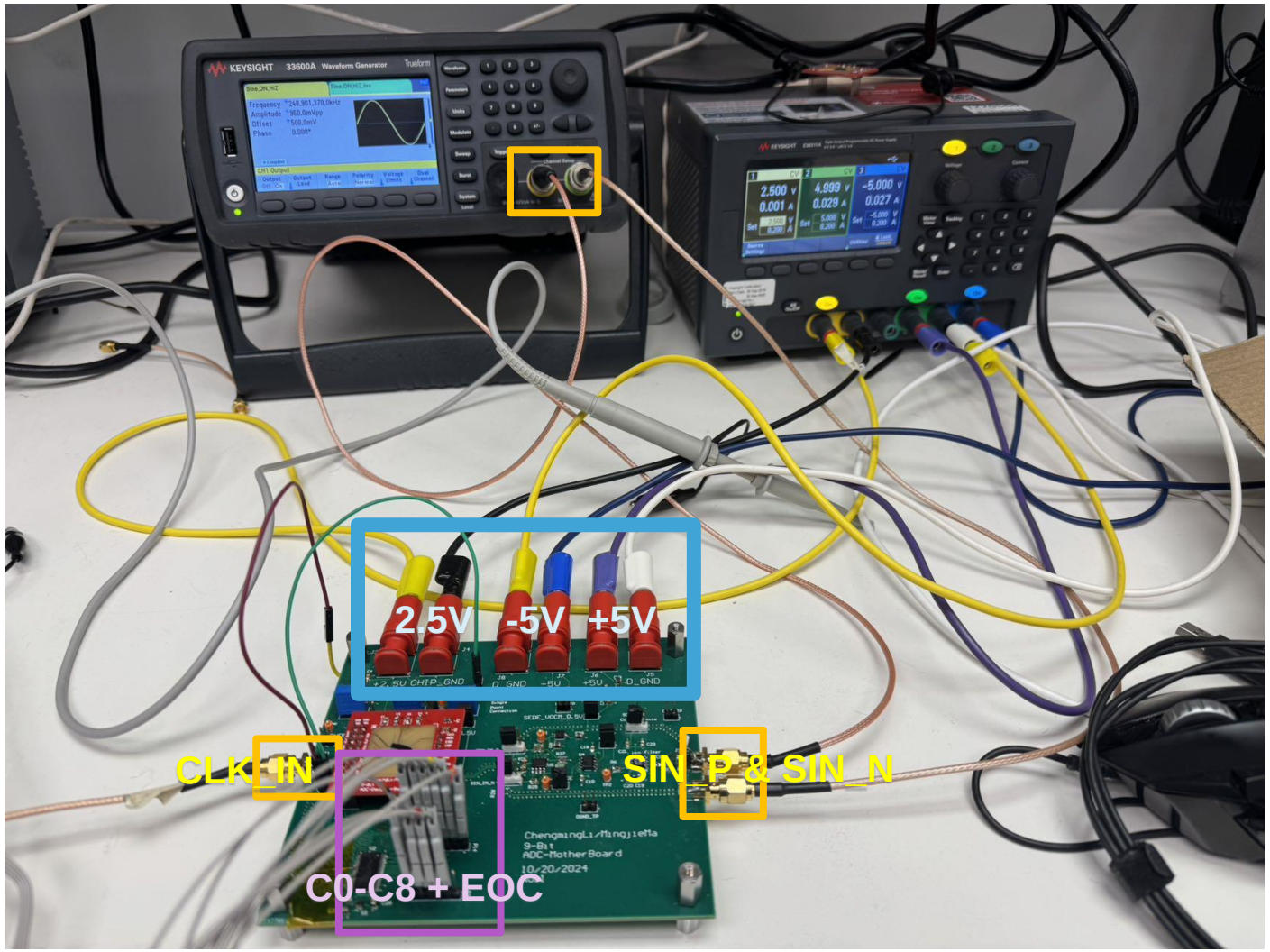
1. Power Supply
    a. 1 channel is used as 5V, 0.2A
    b. 1 channel is used as -5V, 0.2A
    c. 1 channel is used as 2.5V, 0.2A
2. Function Generator
    a. SIN Input - Channel 1
        i. High-Z Load
        ii. 1Vpp
        iii. 0 V offset
        iv. Frequency at 1KHz as initial
    b. SIN Input Inverted - Channel 2
        i. Polarity Inverted
        ii. High-Z Load
        iii. 1Vpp
        iv. 0 V offset
        v. Frequency at 1KHz as initial
    c. Sync Both Channels every time the parameters are changed
3. Oscilloscope
    a. WaveGen used as CLK
        i. Load – Infinity
        ii. Frequency – 1M
        iii. Amplitude 2.5V
        iv. Offset – 1.25V
        v. Duty Cycle 50%
    b. Time Base 1ms/div
    c. Digital Bus1
        i. Digital Code 0-8 (C0-8)
        ii. Digital Code 11 - End of Code (EOC)
        iii. Trigger Level 1.8V
        iv. Turns off Others
    d. Trigger Source
        i. EOC, D11 Rising Edge
        ii. Possibly CLK from Function Generator OR CLK from buffer
    e. Collect data
        i. Stop or Single
        ii. MSB First
        iii. ASCII format
        iv. Maximum Points

Test Automation Setup - 1



1. Power Supply
    1. +5V, -5V, and 2.5V
2. Function Generator
    1. CLK & SIN INPUT
3. Oscilloscope
    1. Digital Analyzer
    2. Digital Output
4. 4-Layer Stack
    1. Signal
    2. DGND + AGND
    3. +5V
    4. -5V

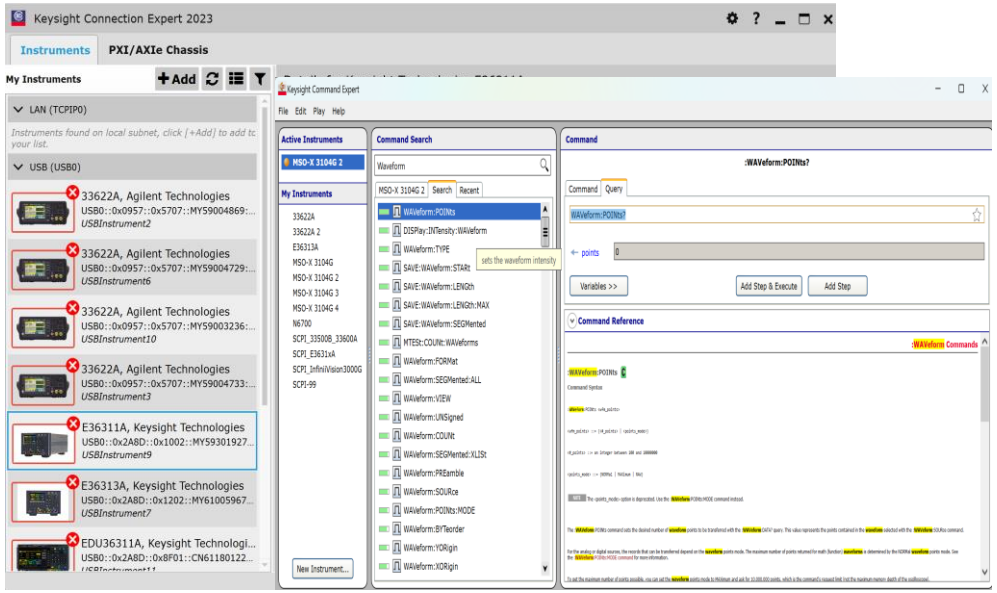
Test Automation Setup - 2



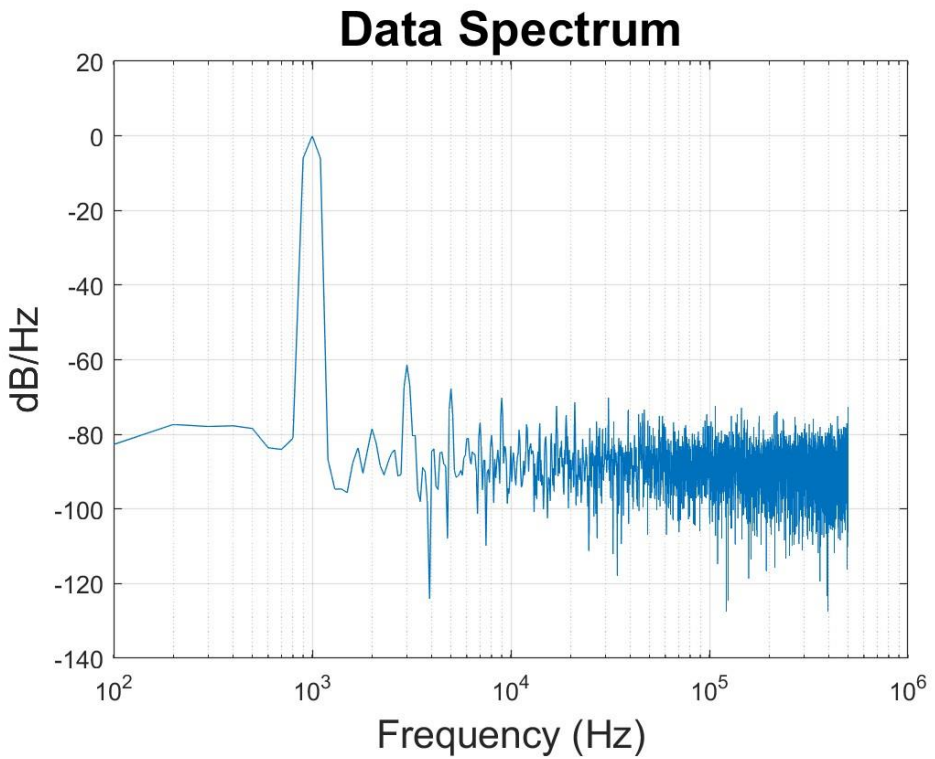
1. Power Supply
    1. +5V, -5V, and 2.5V
2. Function Generator
    1. CLK & SIN INPUT
3. Oscilloscope
    1. Digital Analyzer
    2. Digital Output

Test Automation Code Prep

1. Keysight Connection Expert & Keysight Command Expert
    1. Extremely accelerate the code development time
    2. And check if the instrument is there
2. Python Test Automation
    1. Function Generator
        1. Freq_coupling', 'FuncGenConnect', 'Load__setup', 'PWM_setup', 'Polarity_invert', 'Sin_setup', 'Sync_phase', 'UnitVpp_setup', 'Voltage_coupling', 'output_OFF', 'output_ON
    2. PowerSupply
        1. 'Channel_Select', 'Current_Setup', 'Output_OFF', 'Output_ON', 'PowerSupply_Connect', 'Voltage_Setup'
    3. Oscilloscope
        1. 'DigitalDisplay_ON', 'Digitalizer_ON_OFF', 'Oscilloscope_Connect', 'Oscilloscope_RUN', 'Oscilloscope_SetBUS', 'Oscilloscope_Single', 'Oscilloscope_Stop', 'Oscilloscope_TimeBase', 'Oscilloscope_Trigger_Dchan', 'Oscilloscope_Trigger_External', 'Oscilloscope_WGen_Square', 'Oscilloscope_WGen_Square_OFF', 'Oscilloscope_WGen_Square_ON', 'Save_waveform', 'SetDigital_Threshold'
3. Code Version Control
    1. GitHub
        1. Never lost what I did on "Yesterday"



Peak SNDR Plot



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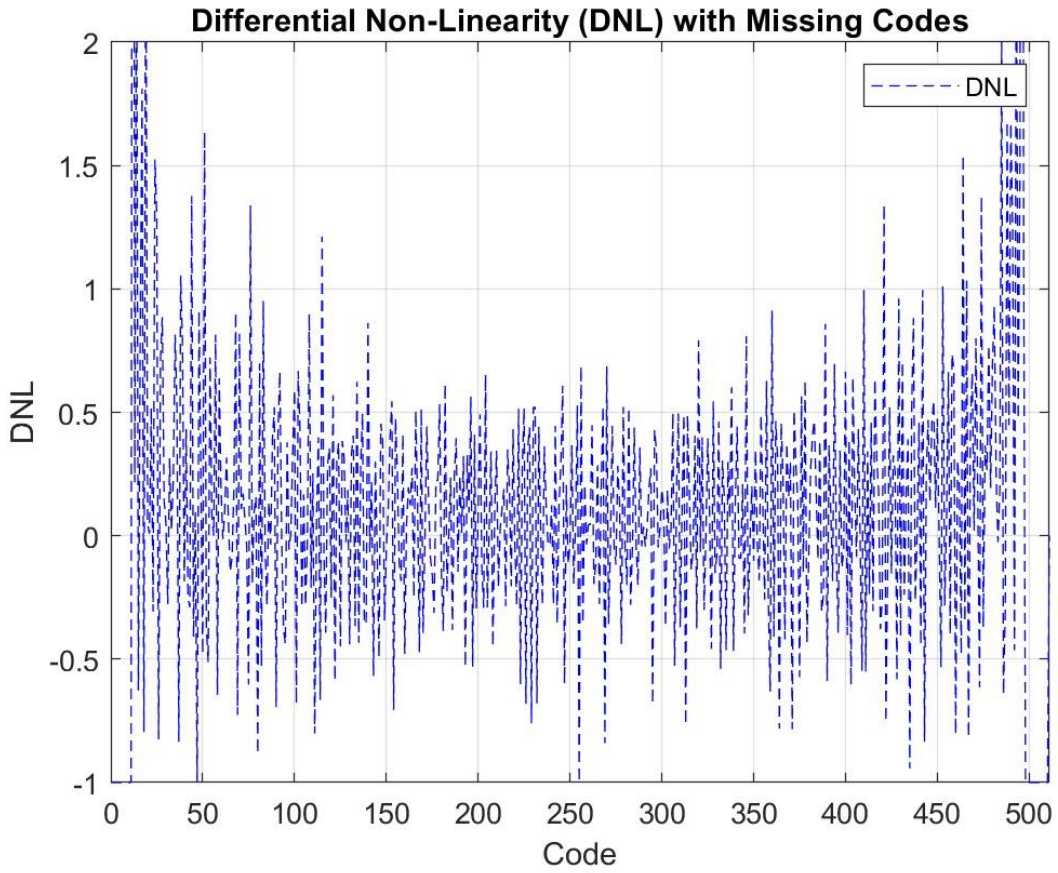
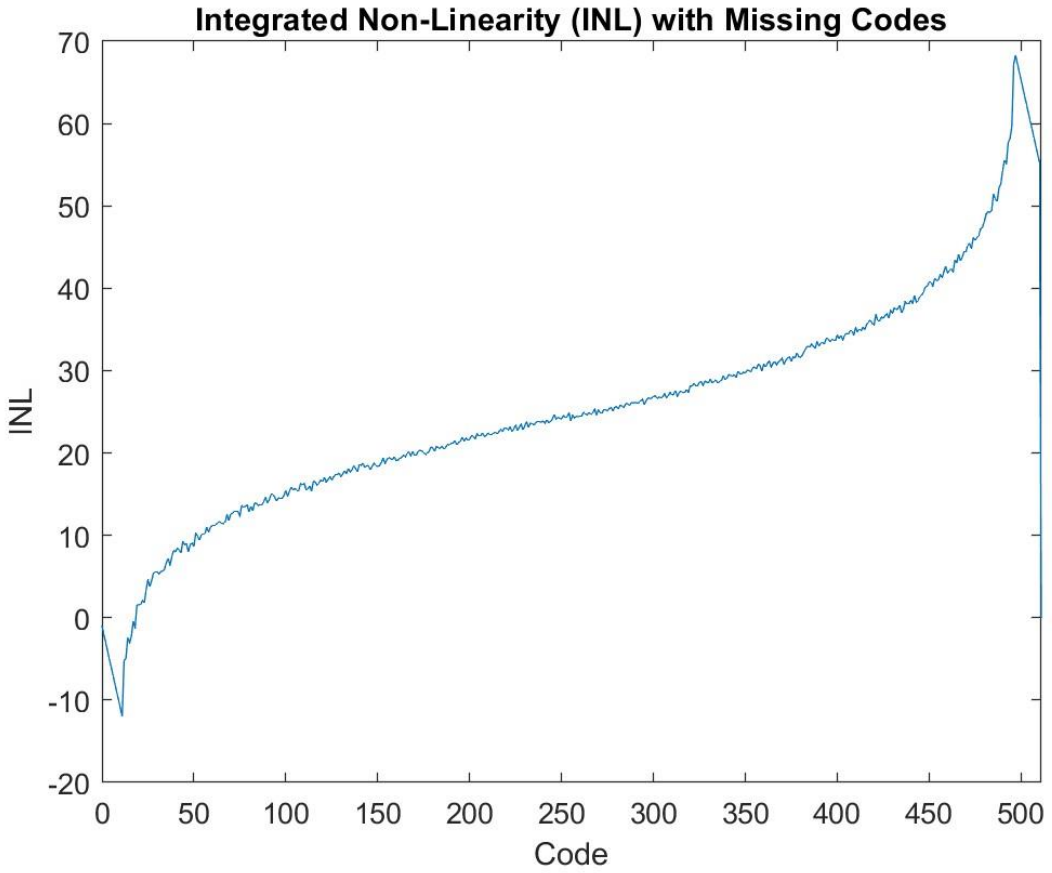
$SFDR_{peak}$ @ 1kHZ	61.45 dB
SNR_{peak} @ 1kHZ	50.68 dB
$THD_{2,peak}$ @ 1kHZ	78.36 dB
$THD_{3,peak}$ @ 1kHZ	61.45 dB

INL & DNL Plot


Differential Non-Linearity (DNL) with Missing Codes
DNL
DNL
Code
2
1.5
1
0.5
0
-0.5
-1
0
50
100
150
200
250
300
350
400
450
500


Integrated Non-Linearity (INL) with Missing Codes
INL
Code
70
60
50
40
30
20
10
0
-10
-20
0
50
100
150
200
250
300
350
400
450
500

Future Work

1. Improve the code to make coherent sampling using: $\frac{f_{in}}{f_{sample}} = \frac{\#\ integer\ cycles}{\#\ FFT\_points}$
    1. By adjusting the input frequency f_{in}
    2. By grabbing enough cycles, no more no less (ideally prime number)
    3. By grabbing 2^x data points
2. Rework the mother and daughter board
    1. Putting more decaps to filter-out the supply noise
    2. Make it to be plugging-in and direct-use Eval-Board
3. Bypass the fronted-end module

Takeaway

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Takeaway

1. Always Always Always document everything
2. Simple Eval-board Design = Robust Debuggability & Reconfigurality
3. Cross-check everything with partners

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- MegaGroup2
  - Putting everything together in the Mega-Chip
- Apple
  - For sponsoring this projects, buying the chips, PCBs, components,etc
- Keysight
  - Instruments, instrument command & connection expert