ECE266 Lab3

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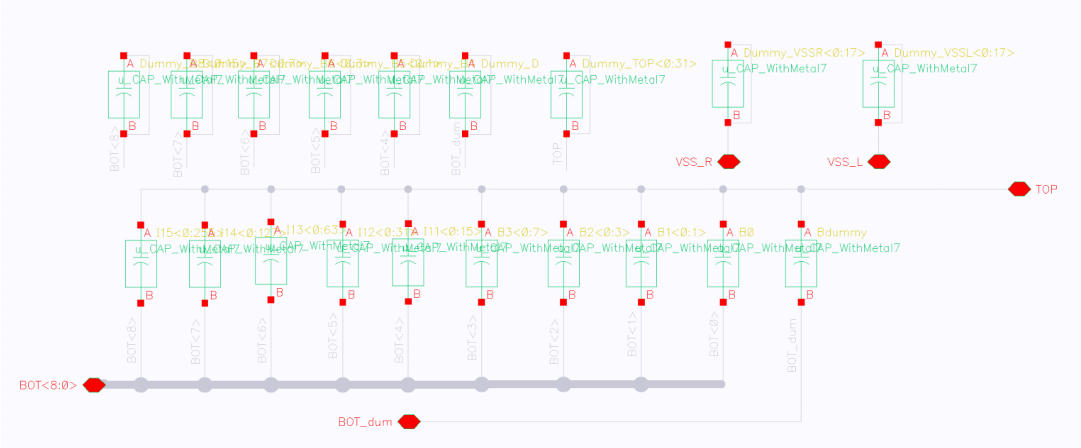
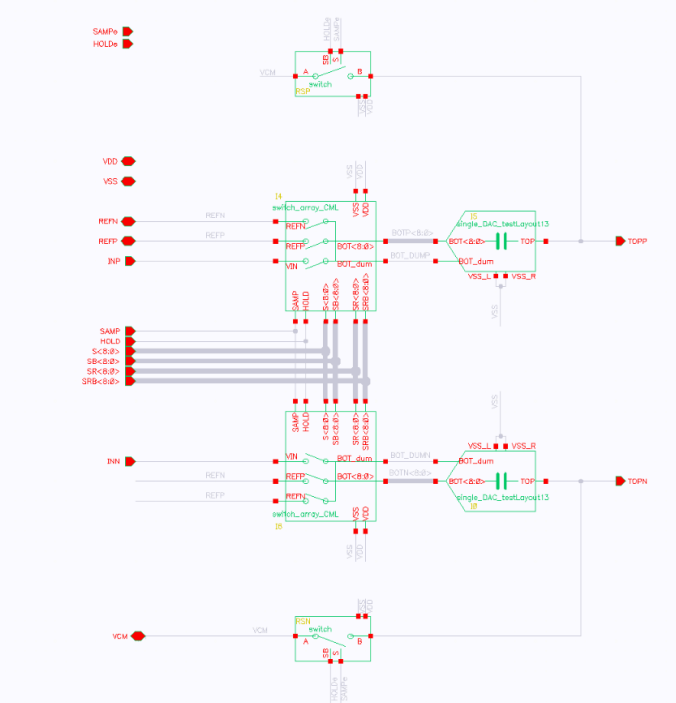
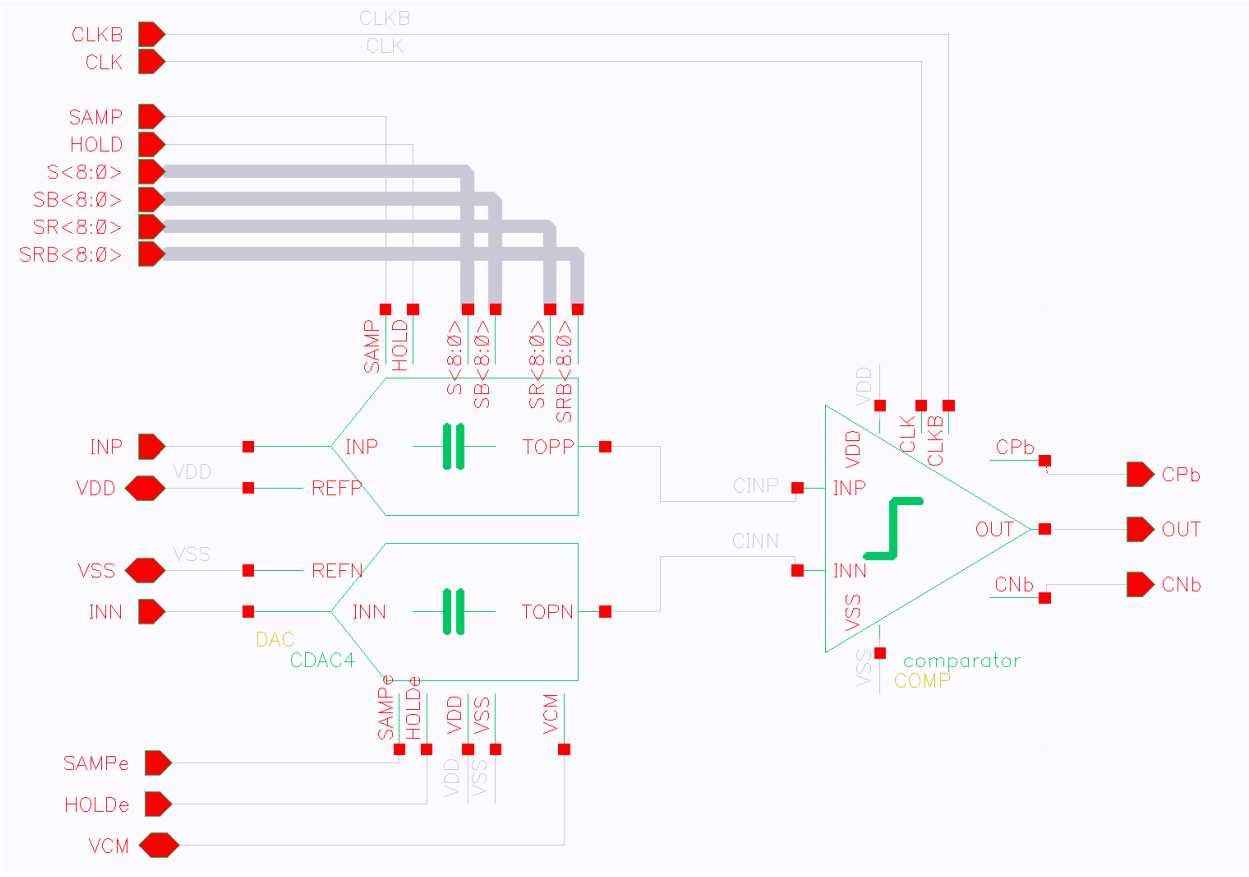
Schematic



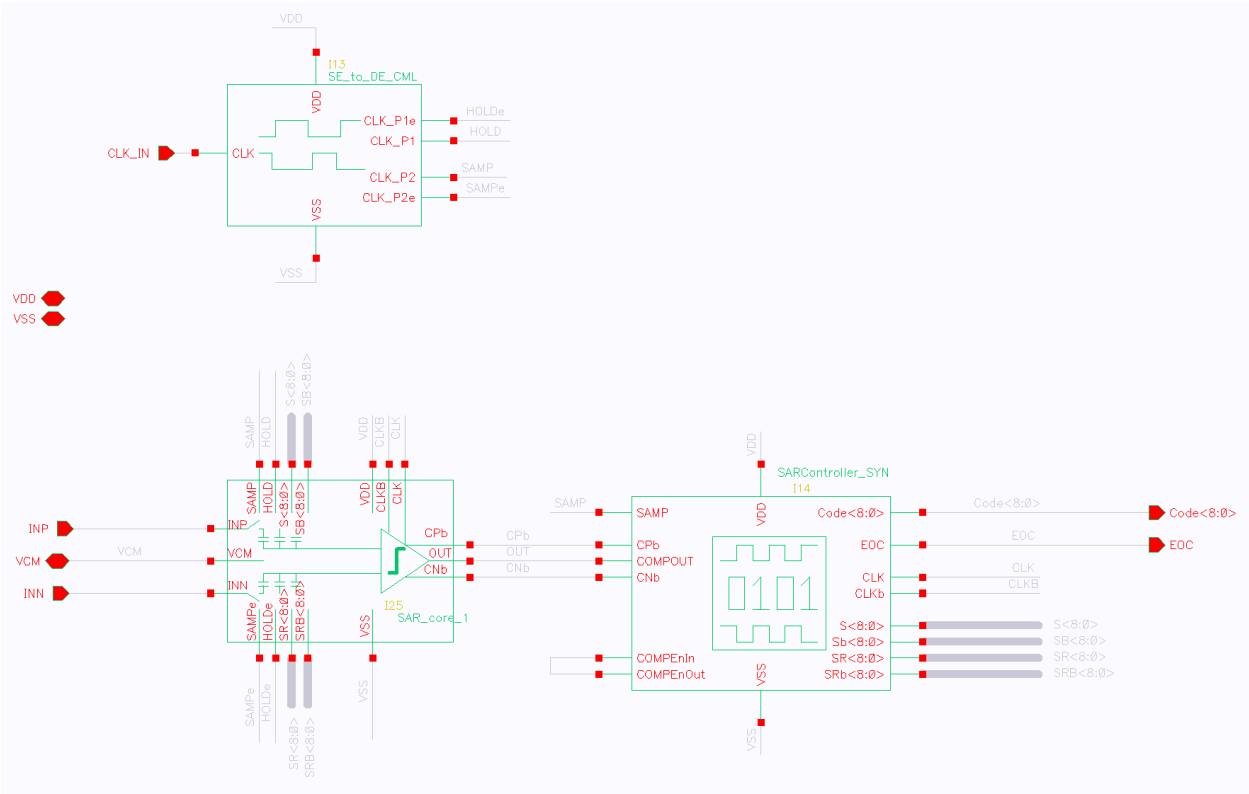
SingleDAC_Schematic with dummies



CDAC_Schematic

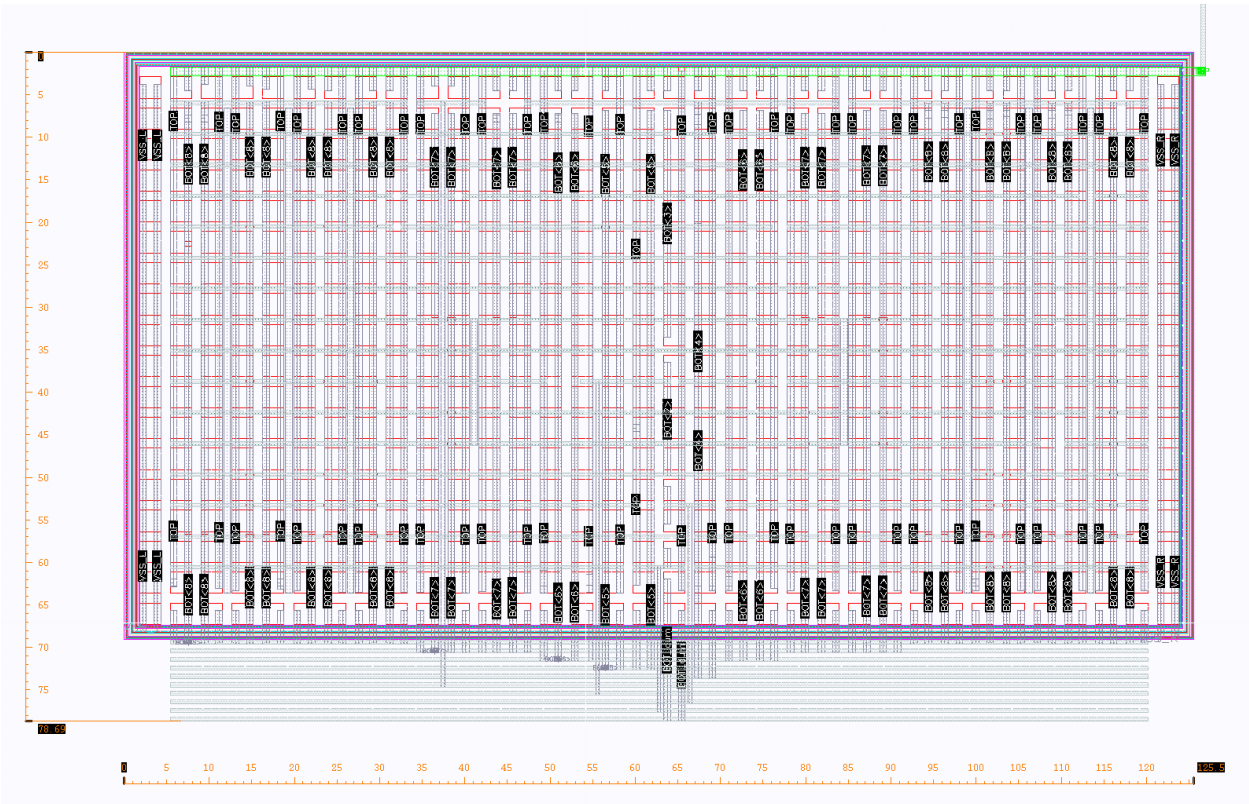


SAR_Core Schematic



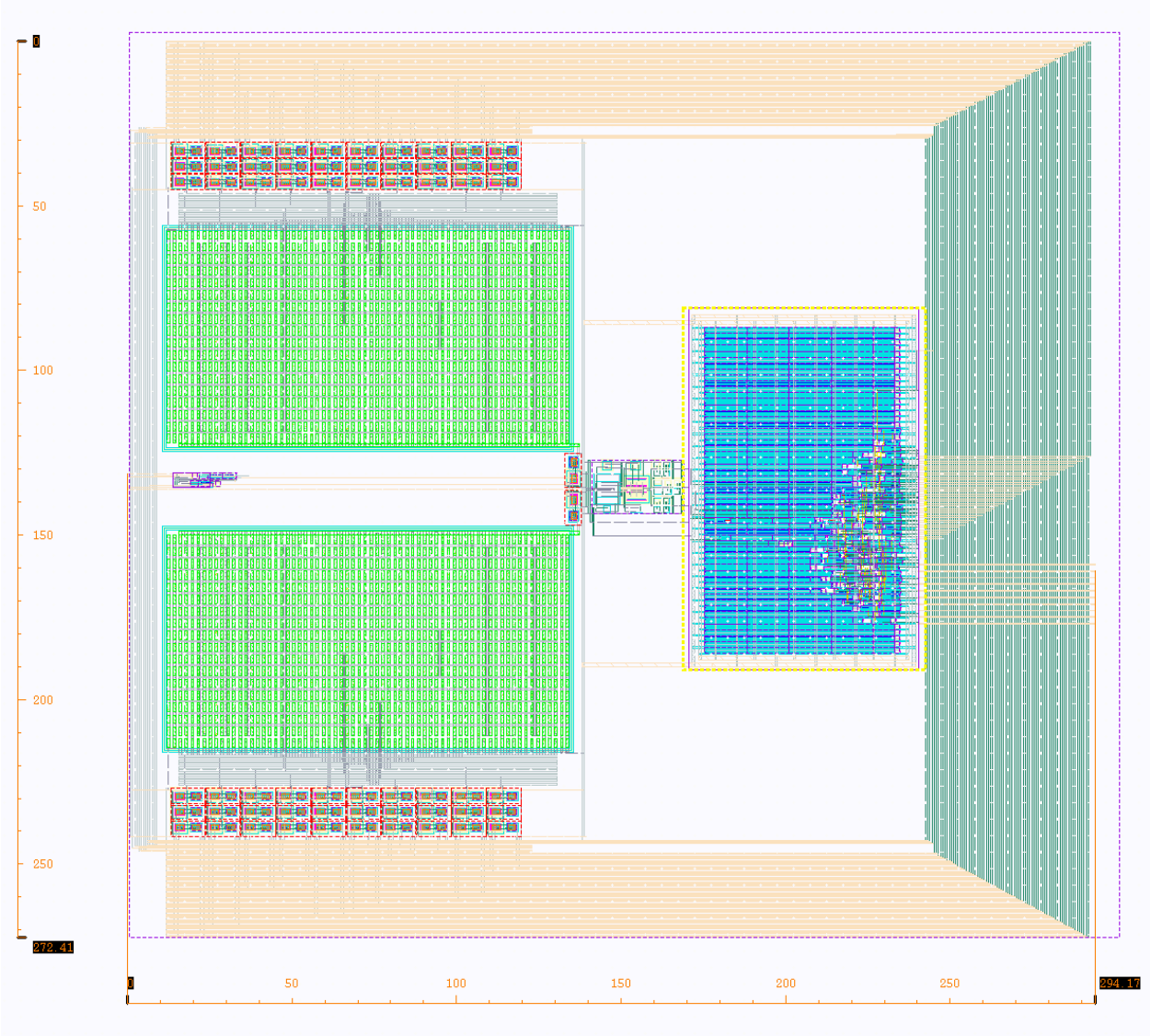
SAR_ADC Schematic

Picture of DAC Layout



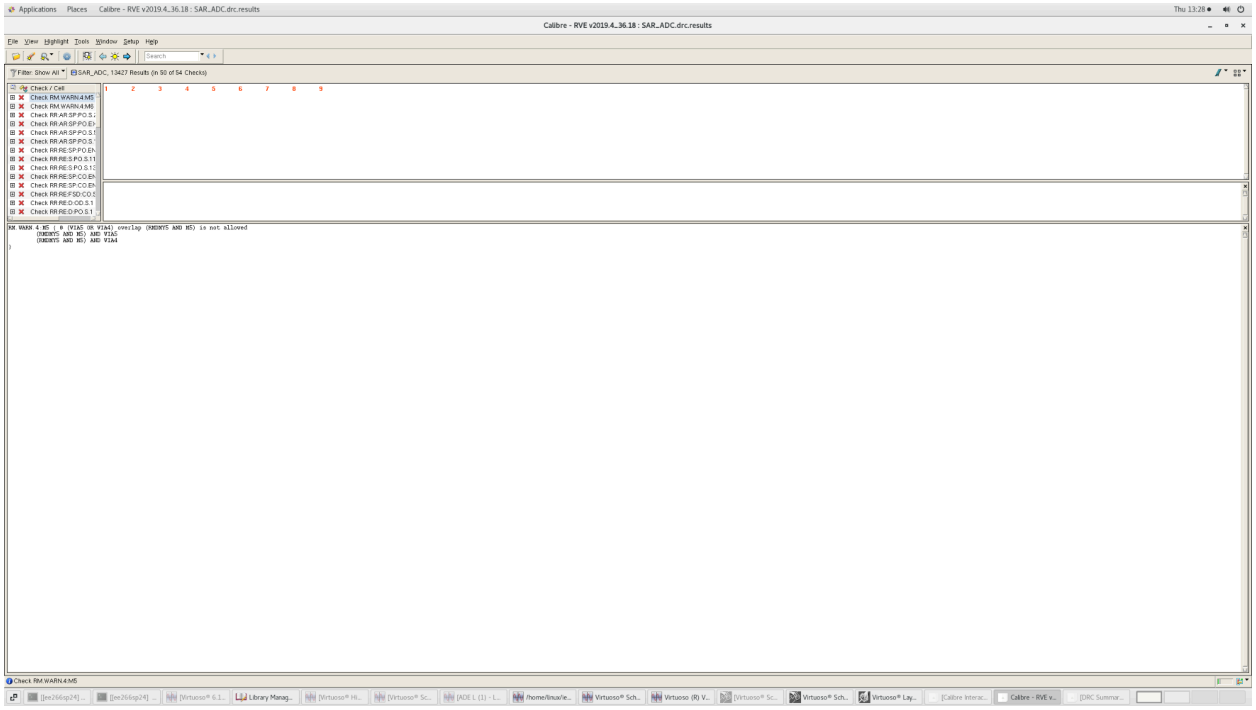
Single DAC Layout(9bits, 78.69*125.5)

Picture of SAR ADC Layout



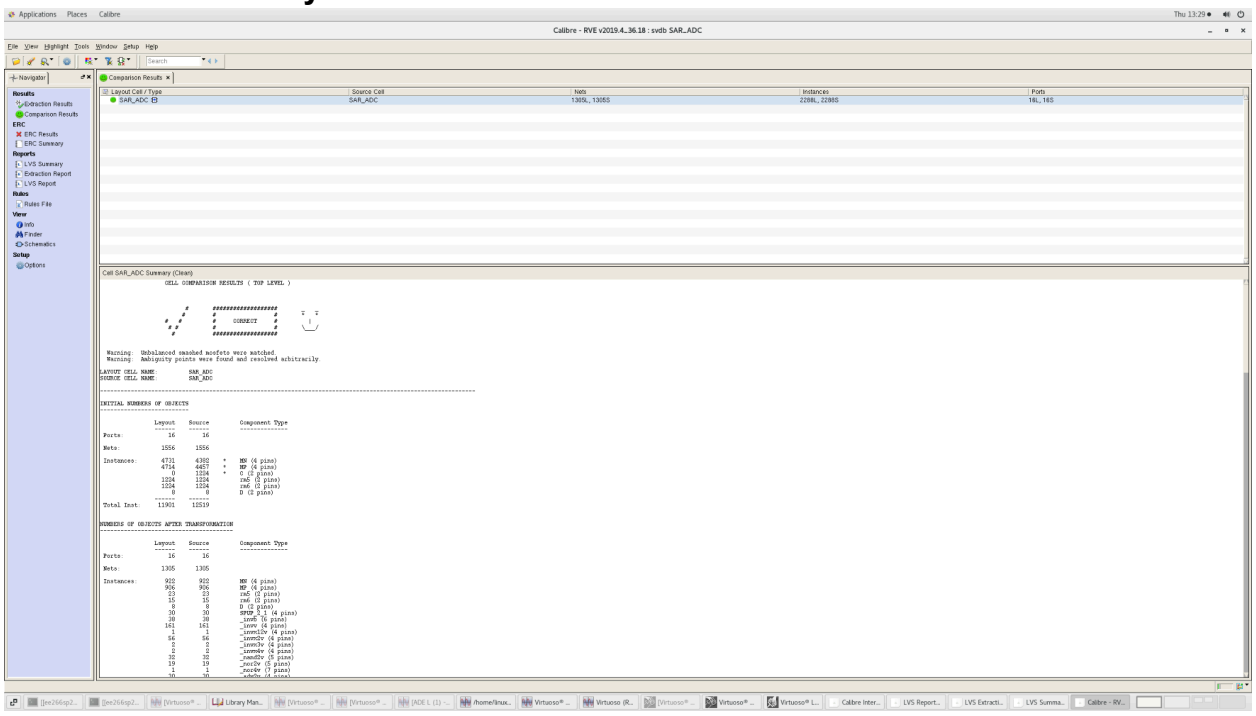
SAR_ADC Layout (294.17 * 272.41)

DRC Result Summary



RR Errors are ignored in the layout

LVS Result Summary



Parasitic coupling caps between B0-B9 to Top/Bottom

SingleDAC

Bit	0	1	2	3	4	5	6	7	8
CC(fF)	5.4927	10.9854	21.9704	43.9449	87.8852	175.769	351.532	703.085	1406.15
Ratio		2	3.99	8.00	16.000	32.00	63.99	128.00	256.00

SAR_Core

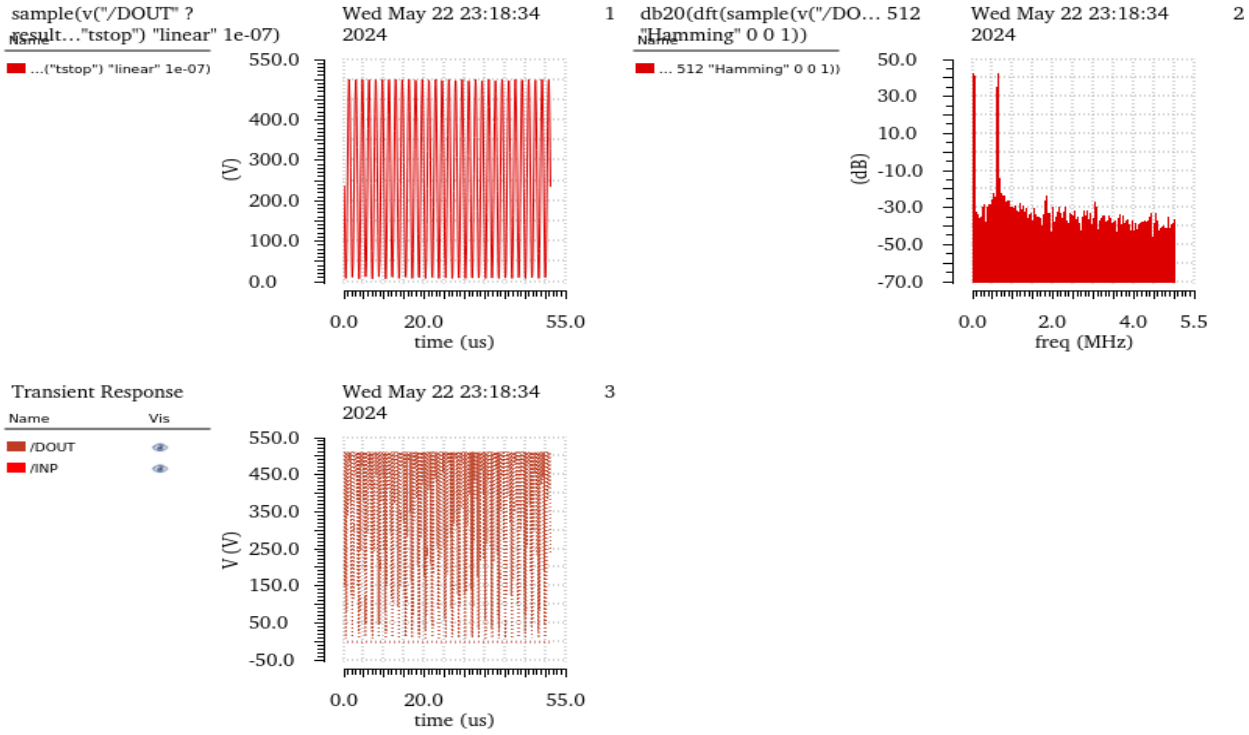
Top P

Bit	0	1	2	3	4	5	6	7	8
CC(fF)	5.5187	11.0182	21.9978	41.0338	88.082	176.21	352.332	705.239	1413.18
Ratio		1.9965	3.986	7.97895	15.9605	31.929	63.84283	127.7898	256.069

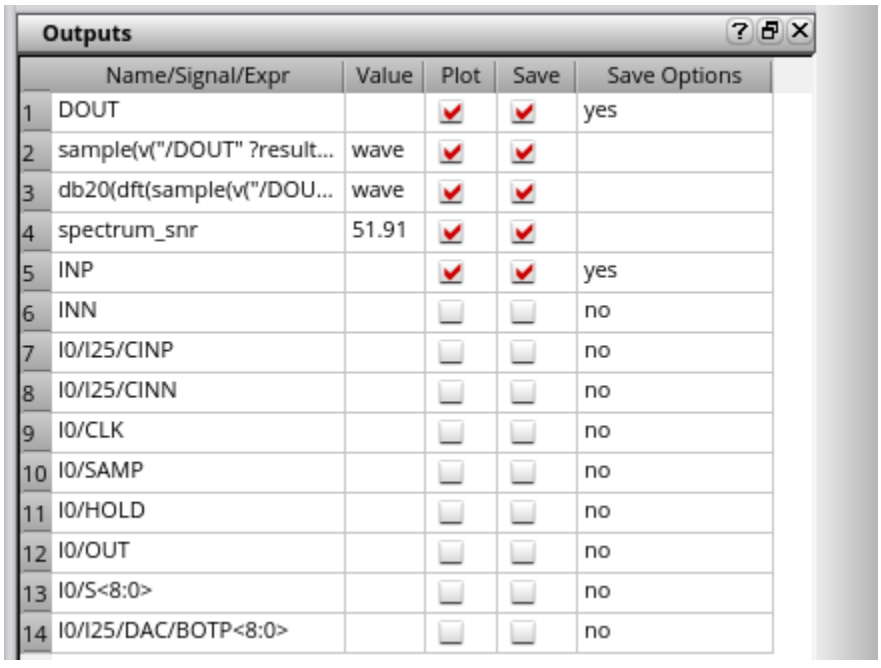
Top N

Bit	0	1	2	3	4	5	6	7	8
CC(fF)	5.5113	11.0223	21.9987	44.0749	88.1173	176.271	352.44	705.293	1413.41
Ratio		1.999	3.9915	7.997	15.988	31.983	63.947	127.97	256.45

Simulation Results from Extracted Layout



SAR_ADC Extracted Layout Simulation Result



Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	DOUT		☑	☑	yes
2	sample(v("/DOUT" ?result...	wave	☑	☑	
3	db20(dft(sample(v("/DOU...	wave	☑	☑	
4	spectrum_snr	51.91	☑	☑	
5	INP		☑	☑	yes
6	INN		☐	☐	no
7	I0/I25/CINP		☐	☐	no
8	I0/I25/CINN		☐	☐	no
9	I0/CLK		☐	☐	no
10	I0/SAMP		☐	☐	no
11	I0/HOLD		☐	☐	no
12	I0/OUT		☐	☐	no
13	I0/S<8:0>		☐	☐	no
14	I0/I25/DAC/BOTP<8:0>		☐	☐	no

SAR_ADC Extracted Layout Output Result

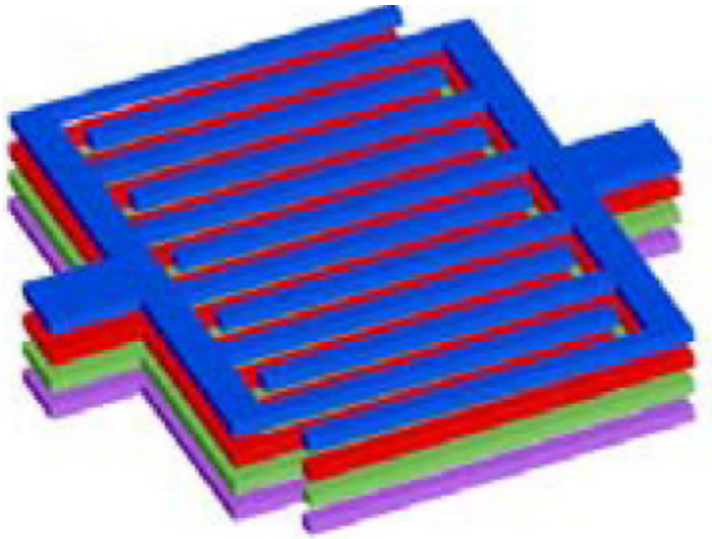
Comments and conclusions

1. We started the design from the Unit Cap as it is the most important layout that will affect the size of the capacitor array. And this layout took us a fair amount of time to finalize the size down to 2.5u*2.52u and keeping 5fF unit capacitance.
2. Then we started the layout of the capacitor array, which also went through 15+iterations to finalize the ratio of each bit to the top plate. This process actually helped us to understand the concept of Coupling Capacitance(CC) and Coupling(C) refer to ground deeply. In addition, it built our understanding of what's the important capacitor that really decides the ratio of each bit, and it is the CC between the bottom and the top plate. However, there is one other capacitor that will also affect the performance of SAR_ADC, and it is the C(top) refers to the ground. If this value is too large,it will attenuate the signal for a bit
3. Afterward, we started the layout of CDAC, SAR Core and SAR ADC. It also took multiple iterations of floor plans to minimize the difficulty of routing and improve the signal integrity by using shielding between digital and analog signals. Moreover, we have also tried our best to lay out the P Single DAC and N Single DAC to make sure there is a perfect match. The final results of unit cap CC(Top to Bot 0) ends up with 0.007 difference
4. The last thing we did was the Digital synthesis, and the only modification we made were the locations of IO pins to easy the routing from the other parts of the circuit
5. The first technique we applied was the compensation metal. This is the technique that we used to mitigate the ratio mismatch between bit0-9 (Expected 2, 4, 6, 8, 16, 32, 64, 128, 256). By using this technique, the bits ratio will be matched down to 2% referred to the expected CC value.
6. The second technique we applied was adding the dummy capacitors. This is the technique that we used to mitigate the process variation on the boundary capacitor. Every single capacitor is sensitive to the environment effects from the other parts of layout. By using dummy capacitors, we made sure that the top plate and bottom plate are connected to the same node, i.e. same potential. So that the capacitors wouldn't be turned on and brought extra effects to the capacitor array and ratio of bit0 to bit 9.
7. The third technique we applied was shielding, we adopted them in the place where digital signal and analog signal are close, digital and digital, and crossover of sensitive signal lines. Two shielding methods were applied. One is parallel shielding for the parallel digital signal lines , and (digital and analog). Another is the vertical shielding for the sensitive signal lines. By applying shielding methods, the signal integrity is greatly promised in out layout design.
8. Something I learned from this lab are:
    a. Guard ring needs to be placed for the transistors who need the best performance, like the current mirror, differential pair, etc. And always be careful about what the annotation says in the schematic. It includes information about when the Guard ring needs to be placed for sure. On the other hand, a guard ring is not required for every device.
    b. How SAR ADC works, how important it is the ratio of each bit refer to bit0

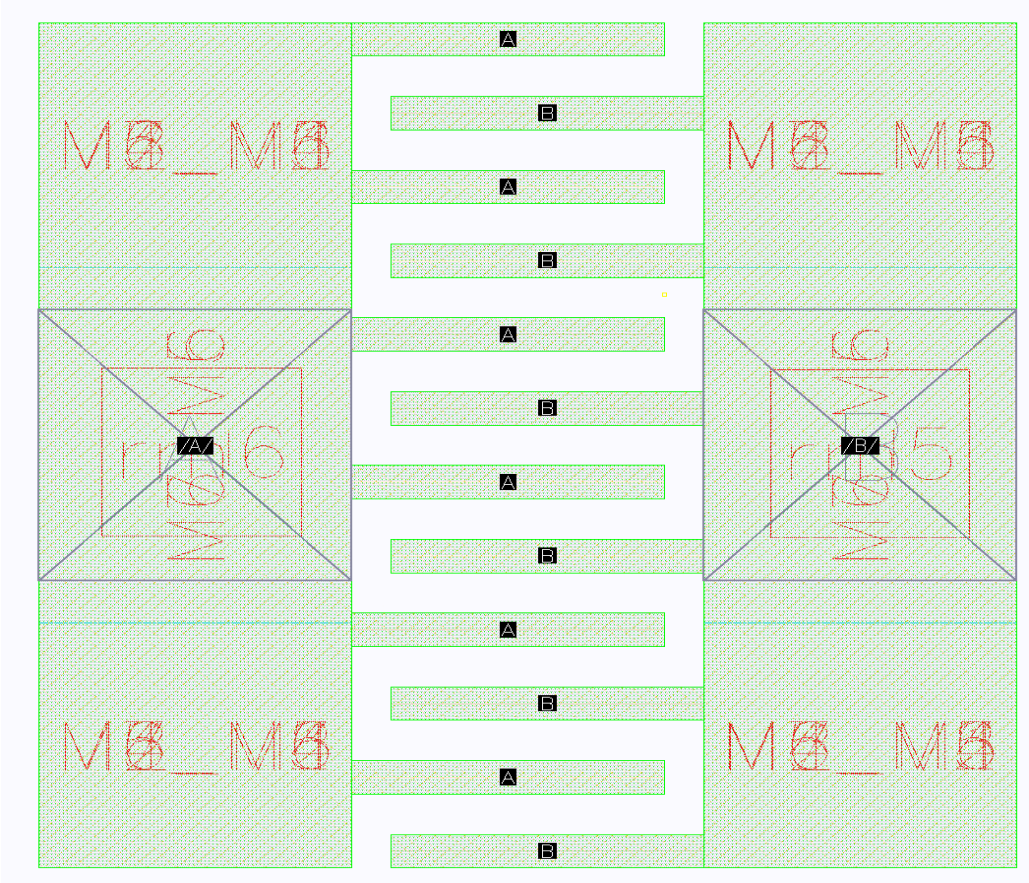
c. The most important capacitor in the DAC design is the CC(Bottom to Top plate), and the second important capacitor is the C at top node which refers to the ground, which will attenuate the signal swing for a bit, but it's still not desirable.
d. Other capacitors, which are not mentioned, will contribute to the power consumption of the entire SAR_ADC design. If the power spec is the requirement of the design, tiny capacitance capacitors are required, and trade-off tiny capacitors are the extra amount of work dealing with CC to get the good ratio.
e. Symmetry layout design in both x-axis and y-axis. Symmetrical design is unique to achieve the matching. Such design makes sure each pair of devices see the similar amount of capacitance and resistance. And so, the difference between devices will be mitigated in the layout-wise.
f. Redundant metal extension, In our second iteration layout, we expanded some of the metals to match the metal length of the other devices, so that a similar amount of R+C will be seen.
g. Even number metal layer should go horizontally, and the odd number metal layer should go vertically. This would maximize the layout spacing usage.
h. Larger metal width for the VDD/VSS connection
i. Digital Synthesis process
j. Better floorplanning mindset is from Top to Bottom level, but not from Bottom to Top

9. Something I didn't learned very well from this lab are:
    a. How SAR ADC schematics works in detail.

Appendix



Customized unit cap structure



Unit Cap Layout