9-bit, 10-MSPS, SAR-ADC

1 FEATURES

- 9-bit resoolution
- 10 Mega sample per second
- 4-channel ADCs available
- Single +1V VDD Operation and +2.5V ESD Protection
- 1 pair of differential Inputs
- 1 input as common mode voltage
- Two-STATE +2.5V Digital Outputs
- 10-bit Output (C0-C8 + EOC)
- 65nm TSMC process
- Detailed chip-packaging and eval-board design included

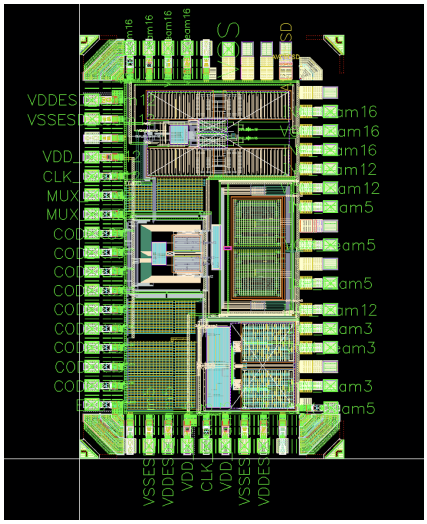
2 Applications

- University course chip-tape-out design
- SAR-ADC study for beginner
- Chip-packaging study for beginner
- Evaluation-board design for beginner
- Video Digitization
- Personal Computer Video Cameras

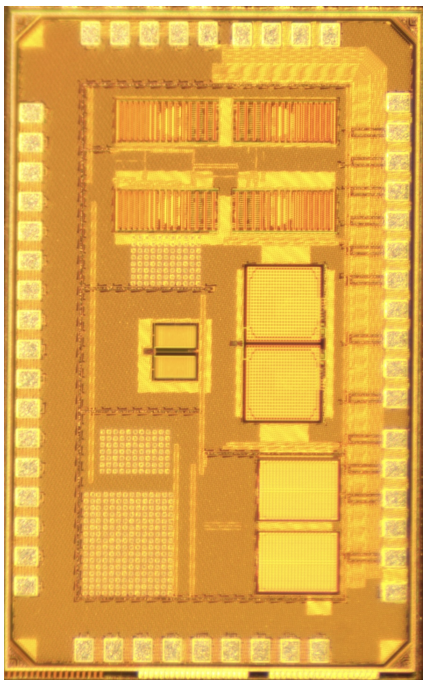
3 Description

- This is a 9-bit resolution, up to 10MSPS, 4-channel SAR-architecture analog-to-digital converter (ADC).
- 4 channel ADCs are available up to the wirebonding - configuration
- Single-ended Input / Differential Inputs options are available up to eval-board configuartion
- 10-bits Digital output (Code 0-8 + End of Conversion)
- Average 400uW power consumption per channel.
- Average 48dB SNDR performance
- The circuit works with + 1V VDD.
- +2.5V is needed to power up the ESD protection, and level shifter for digital pads
- Can be operates up to 1.2 V for best performance
- Detailed instructions of wire-bonding is provided
- Detailed instructions of evaluation-board is provided
- Detailed instructions of performance characterization is provided
- This chip is taped out for studying the SAR-ADC operation, best practice of Layout.techniques, chip-eval PCB design, and performance-characterization.
- UCSD-ECE266-MegaGroup2-Team12-ChengmingLi/MingjieMa's ADC as 1 of 4 ADC channel will be evaluated and demonstrated.

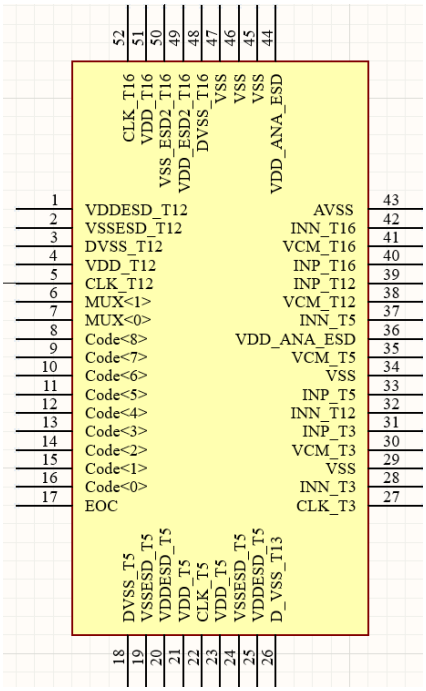
4 Chip Layout Photo



5 Die Photo

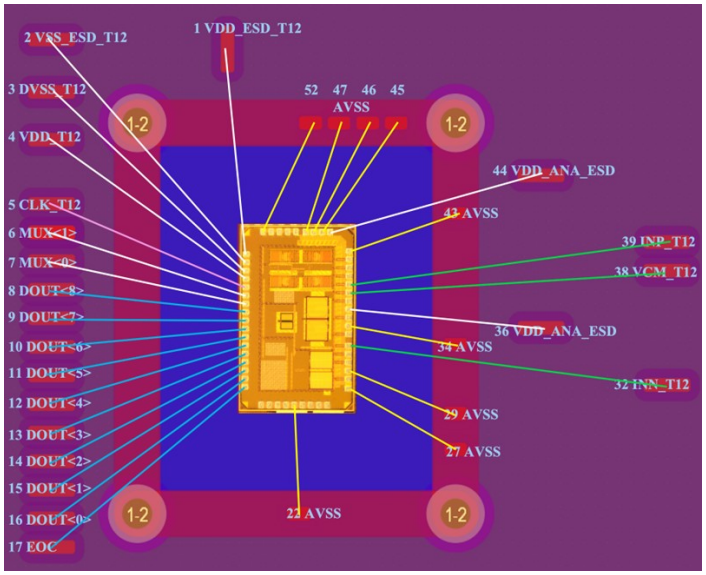


6 4-Channel-Pinout information



Pin	Signal	Voltage-Level
1/20/25/49	VDD_{ESD}	2.5V
36/44	$VDD_{AnalogESD}$	2.5V
2/19/24/50	VSS_{ESD}	0V
3/18/26/48	VSS_{Ditial}	0V
43	VSS_{Analog}	0V
29/34/45/46/47	VSS	0V
4/21/23/51	VDD	1V
5/22/27/52	CLK	PWM-2.5V
6/7	$MUX1/MUX0$	2.5V
8-17	$DigitalOutput$	2.5V
28/32/37/42	INN	SIN-1V
29/35/38/41	VCM	0.5V
31/33/39/40	INP	SIN-1V

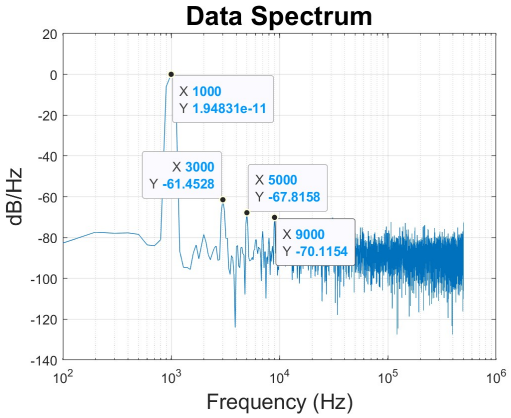
7 Team-12 PinOUT



8 CONVERTER ELECTRICAL CHARACTERISTICS

The following specifications apply to AVDD = DVDD = + 1 VDC, VDD_{ESD} = 2.5V, MUX0 = +1 VDC, MUX1 = 0 VDC, INP = 1.02V_{sin}, INN=1.02V(180° out of phase of INP), f_{in} = **1k-100kHz** ,VCM = 0.5V ,CLK = 2.5, V_{pwm}, $f_{clk} = 1MHz$. Peak performance is evaluated at f_{in} = **1kHz**

Parameter	Typ	Max
SNR	33dB	51dB
SNDR	33dB	50dB
SFDR	41dB	61dB



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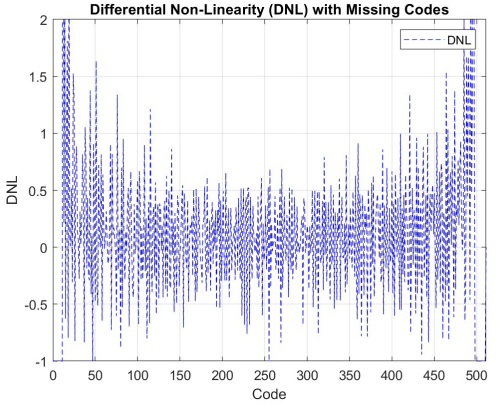

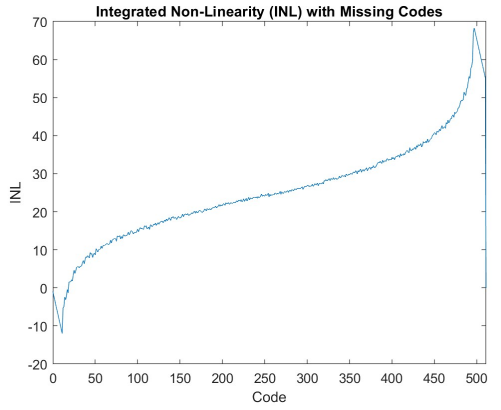

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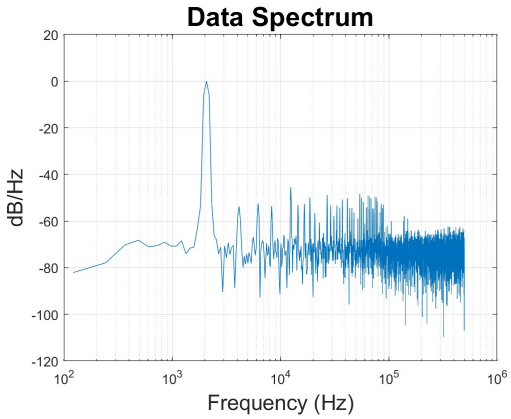
- SNR = 33.924 dB, SNDR = 32.811 dB, SFDR = 52.445 dB, HD2 = 53.740 and HD3 = 52.445



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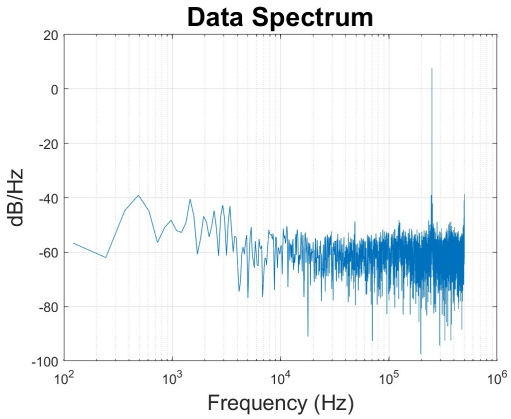
- SNR = 30.600 dB, SNDR = -7.255 dB, SFDR = 40.562 dB, HD2 = 58.906 and HD3 = 40.562



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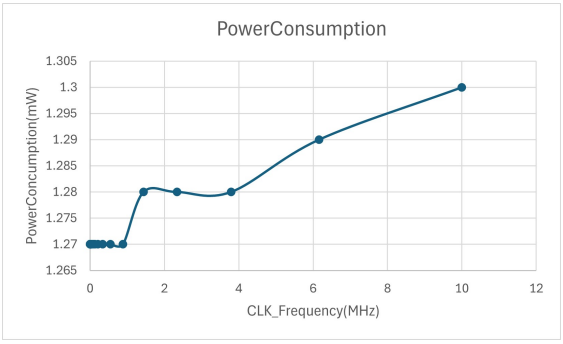
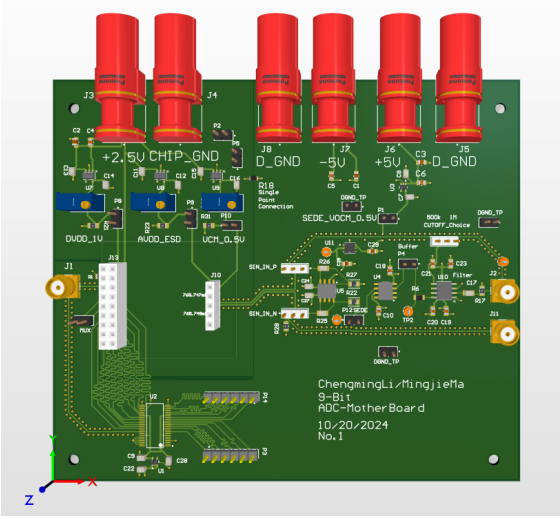
- Peak power consumption = 1.3 mA at f_{clk} = 10 MHz

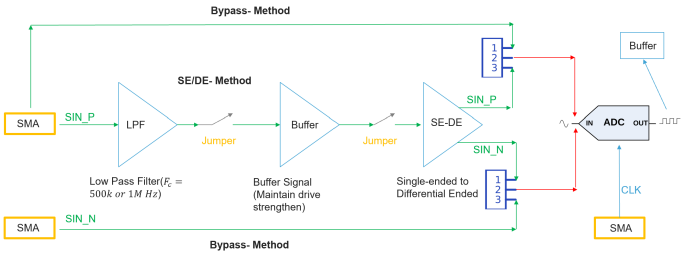


9 Mother-Board-Guidance

Following are the motherboard design



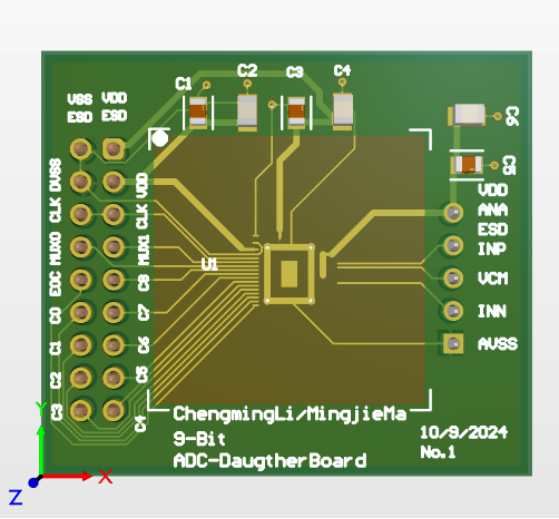
High-Level-Block Diagram is as follows:



- **Provided the above solution is overdesigned the evaluation board, use with caution**.
- The Bypass/SE-DE Method is provided. Bypass Method provides better performance
- It is recommended to add another differential RC-filter after the SE-DE output and before the ADC differential inputs.
- The recommended cutoff frequency is 500kHz. Please make the resistor to be in the range between 20 ohm to 50 ohm.
- **For best evaluation, it is highly recommended to just put an differential RC filter, between the input from function generator and ADC inputs, and used it as charging sharing circuit.**
- Additionally, ADC output is needed to buffed by an external Buffer IC with supply voltage 2.5V.

10 Daughter-board Guidance

Following are the Daughter-board design



- **Please add at least 5 different De-coupling capacitors on-board to minimize the fluctuation of IC-VDD.**
- In our design, 600mV_{pp} is seend after powered up. This is primarily coming from the CLK input-coupling.
- We have ran the fft of chip-VDD, multi-harmonics of CLK are seen.
- **It is highly recommended to connect the entire chip's pads out using wire-bonding, and ground the unused pads afterward.**
- Floating pads may cause unexpected behavior, wire-bonding all pads out for safety.