ECE266 Lab1

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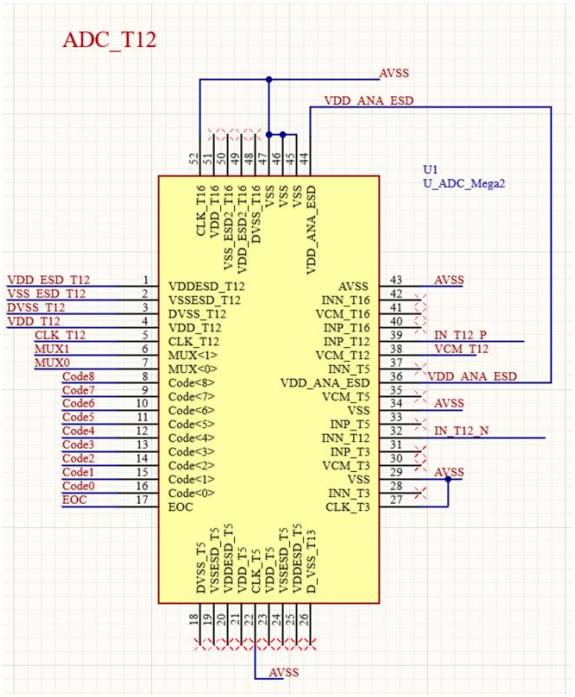


Figure 1: IC Pins name and location

Pin Number	Type	Direction	Purpose
1	Power	Input	Activate ESD for chip power supply
2	Power	Input	Activate ESD for chip power supply
3	Power	Input	Digital Ground for the chip
4	Power	Input	Power supply for the chip
5	Digital	Input	Clk determine the sampling frequency for the chip
6/7	Digital	Input	ADC core's selection signal
8-16	Digital	Output	Output digital signals
17	Digital	Output	Digital signals to illustrate the end of conversion
22/27/29/34/43/45/46 /47/52	Power	Input	Analog Ground for the chip
32	Analog	Input	Differential input signal – negative one
36/44	Power	Input	Activate ESD for chip input side
38	Analog	Input	Common mode for the Chip (DC biasing)
39	Analog	Input	Differential input signal – positive one

Table 1: IC Pins detailed description

As shown in Figure 1 and Table 1, the defined pins' location and related parameters. Since the chip has four ADC core, and we are only focus on testing one of them, it is unnecessary to wire bonding all ADC cores' input. Instead, we only wire bonding the targeted Core, meanwhile, we float other cores unsensitive analog input, and short the sensitive CLK digital input pad to ground to avoid any potential interfere.

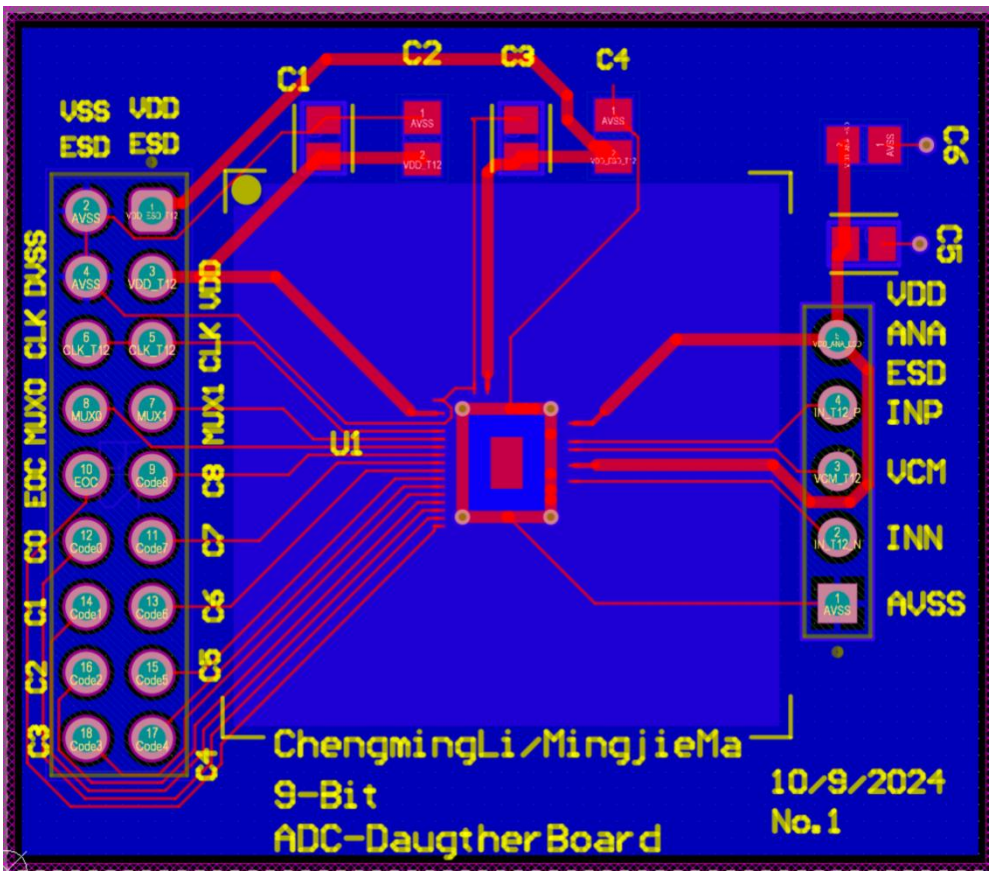


Figure 2: Layout of the daughterboard PCB

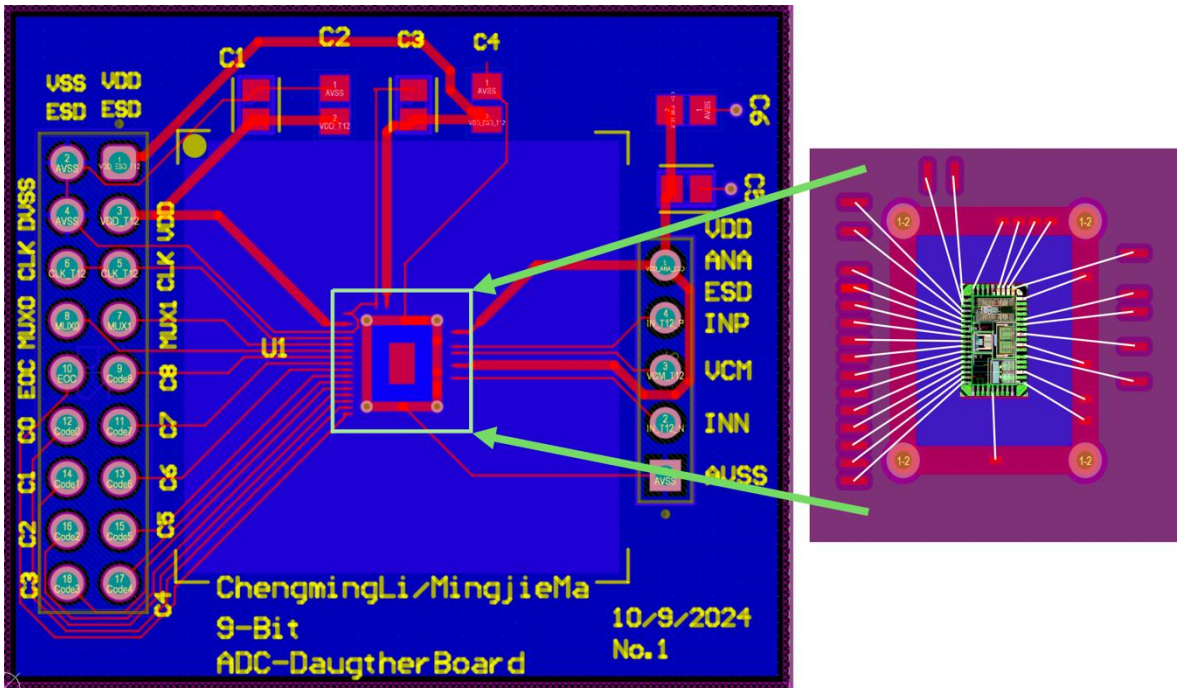


Figure 3: Location of the Chip package on the daughterboard PCB

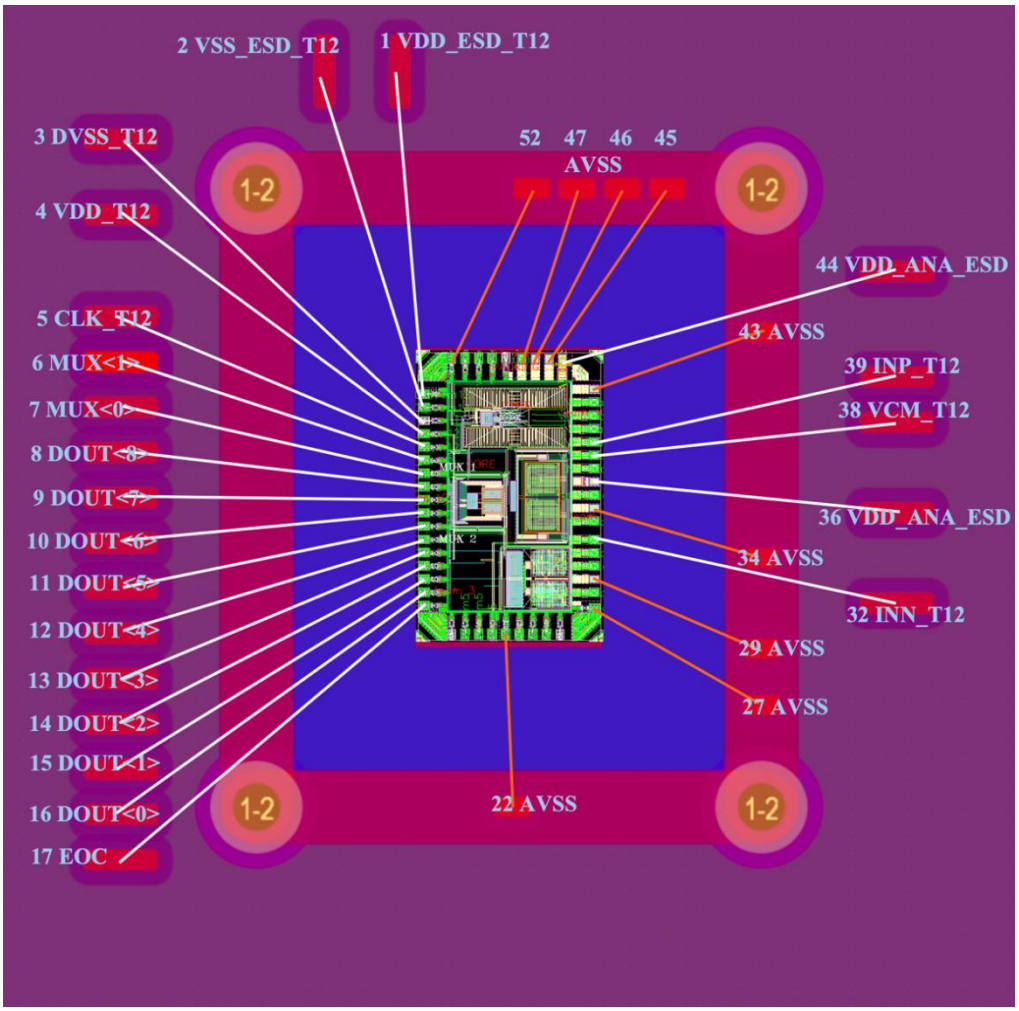


Figure 4: Wire Bonding Diagram

Pin Number	Type	Description
1	Power	VDD_ESD
2	Power	VSS_ESD
3	Power	DVSS_T12
4	Power	VDD_T12
5	Digital Input	CLK_T12
6/7	Digital Input	MUX_SEL
8 - 16	Digital Output	ADC_RESULT
17	Digital Output	EOC
22/27/29/34/43/45/46/47/52	Power	AVSS
32	Analog Input	INN_T12
36/44	Power	VDD_ANA_ESD
38	Analog Input	VCM_T12
39	Analog Input	INP_T12

Table 2: Wire Bonding pad parameters description

Figure 4 illustrates the wire bonding locations, where we are trying to put analog input as close as possible to avoid the parasitic components that the bonding line brought. The inner circle is the Analog ground for the chip which requires down bonding, and all digital ouput pins are locates at the right side.

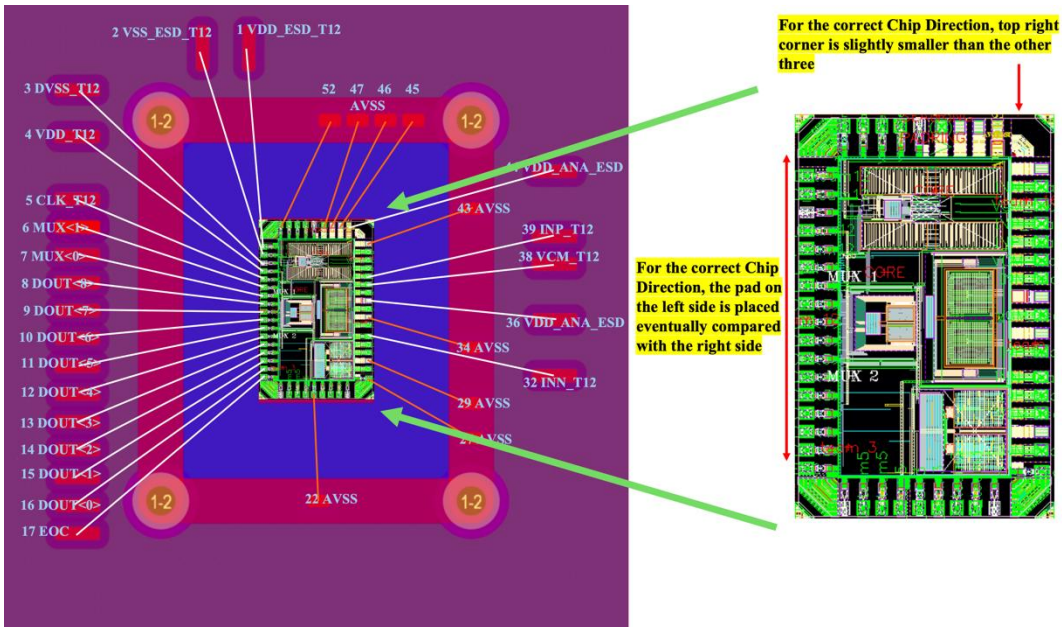


Figure 4: Location of the Chip to the chip package and comments for the chip direction

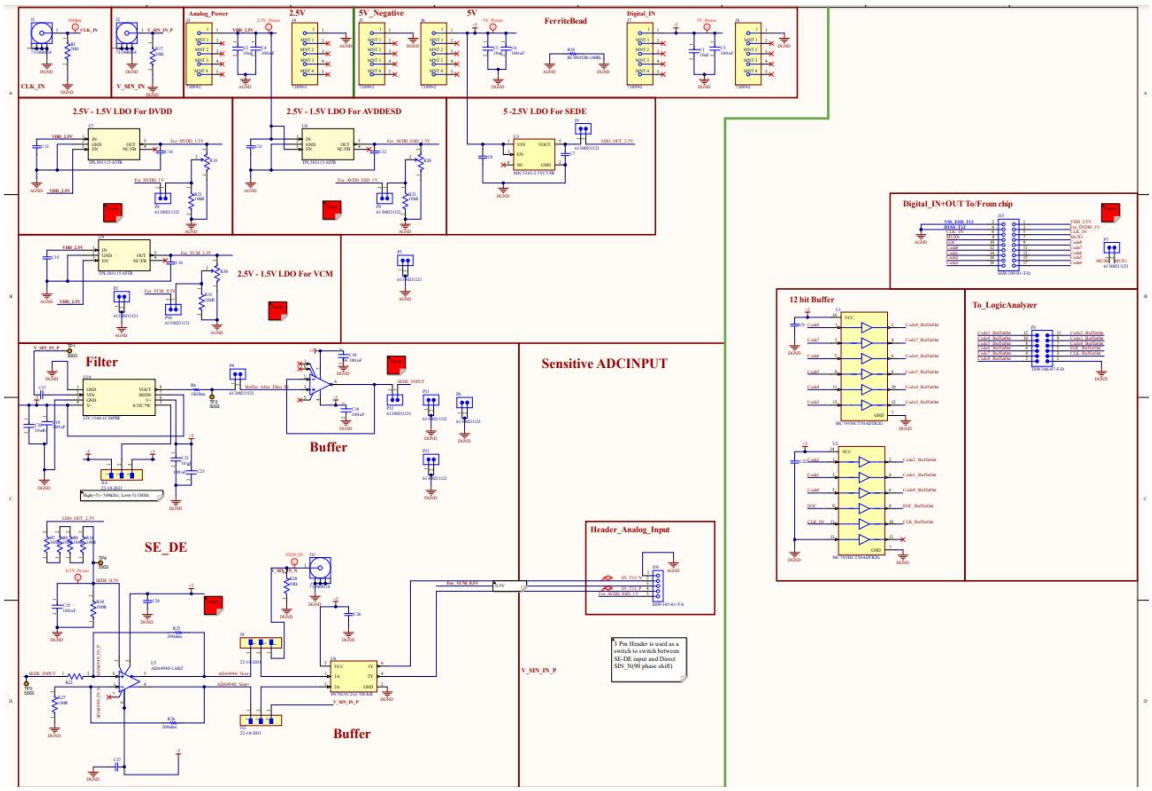


Figure 5: Schematic of MotherBoard

Layout of MotherBoard

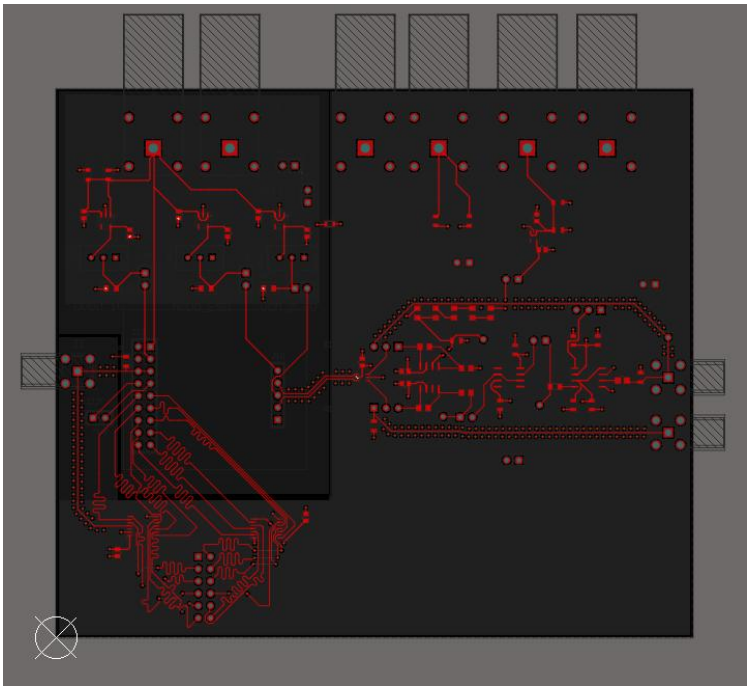


Figure 6: Top Layer

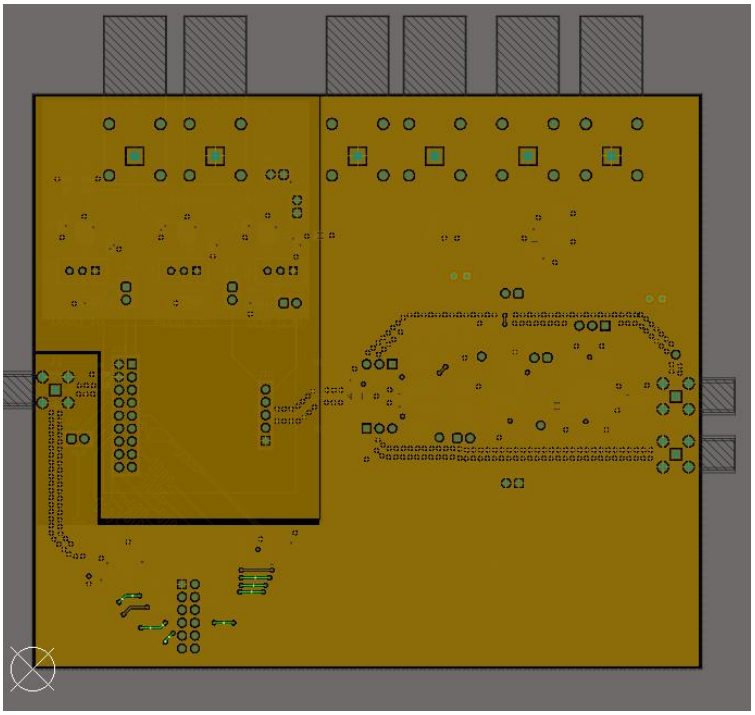


Figure 7: 2nd Layer-GND, CHIP_GND AND Passive_Component_GND

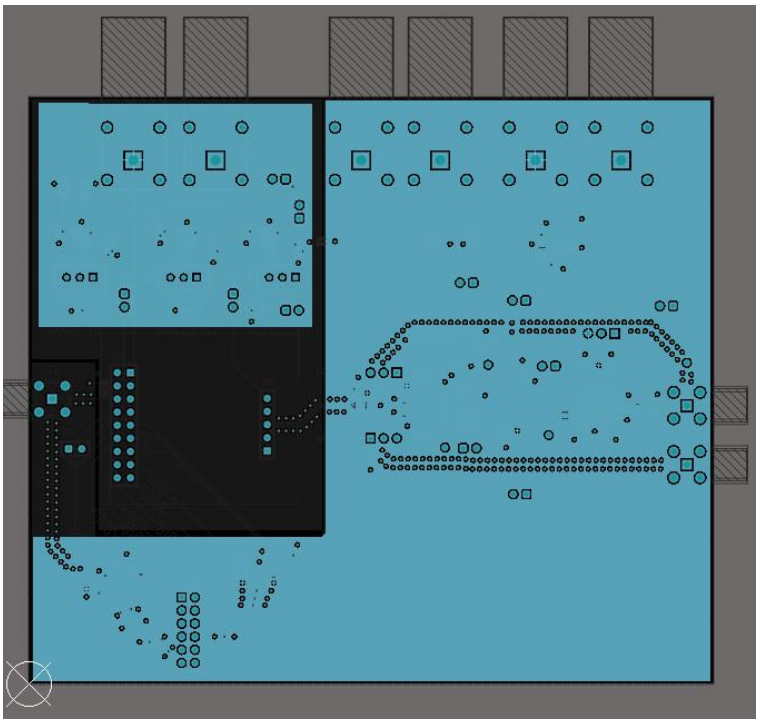


Figure 8: 3rd Layer - 2.5V VDD for Analog, 5V VDD for all other external peripherals

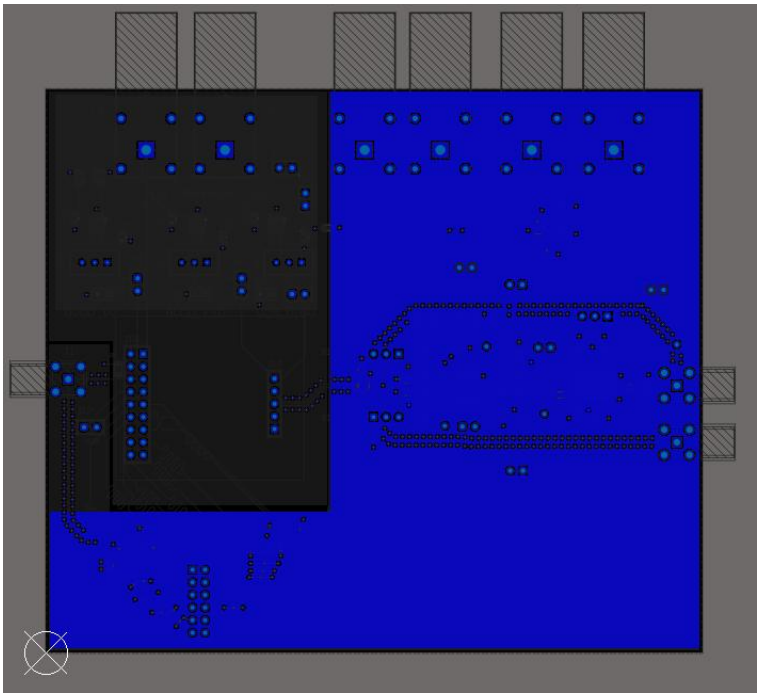


Figure 9: 4th Layer - -5V VDD

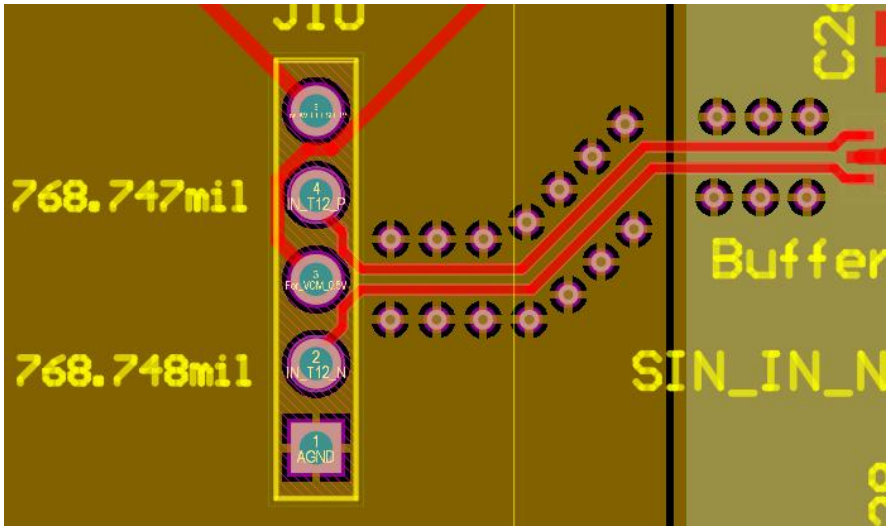


Figure 10: Differential Length for INP INN

Code_Length
INPUT_Signal

10 Nets (0 Highlighted)

Name	Node...	Signal Lengt...	Tot...	Rou...	Unrou...
Code0	2	1789.29	0	1790.8	0
Code1	2	1789.291	0	1791.1	0
Code2	2	1789.29	0	1791.1	0
Code3	2	1778.599	0	1780.6	0
Code4	2	1789.291	0	1789.2	0
Code5	2	1789.29	0	1789.2	0
Code6	2	1789.291	0	1790.8	0
Code7	2	1789.291	0	1790.8	0
Code8	2	1789.291	0	1791.2	0
EOC	2	1789.291	0	1789.5	0

Figure 11: ADC output Code Length

BUFFEROUT_Length
CLK
Code_Length
INPUT_Signal

10 Nets (0 Highlighted)

Name	Node...	Signal Lengt...	Tot...	Rou...	Unrou...
Code0_BufferOut	2	1376.065	0	1377.5	0
Code1_BufferOut	2	1387.356	0	1389.0	0
Code2_BufferOut	2	1383.369	0	1385.4	0
Code3_BufferOut	2	1382.539	0	1384.0	0
Code4_BufferOut	2	1387.356	0	1389.1	0
Code5_BufferOut	2	1387.356	0	1439.8	0
Code6_BufferOut	2	1387.356	0	1391.0	0
Code7_BufferOut	2	1387.356	0	1389.7	0
Code8_BufferOut	2	1387.356	0	1389.0	0
EOC_BufferOut	2	1395.049	0	1396.5	0

Figure 12: ADC Output after Buffer Length

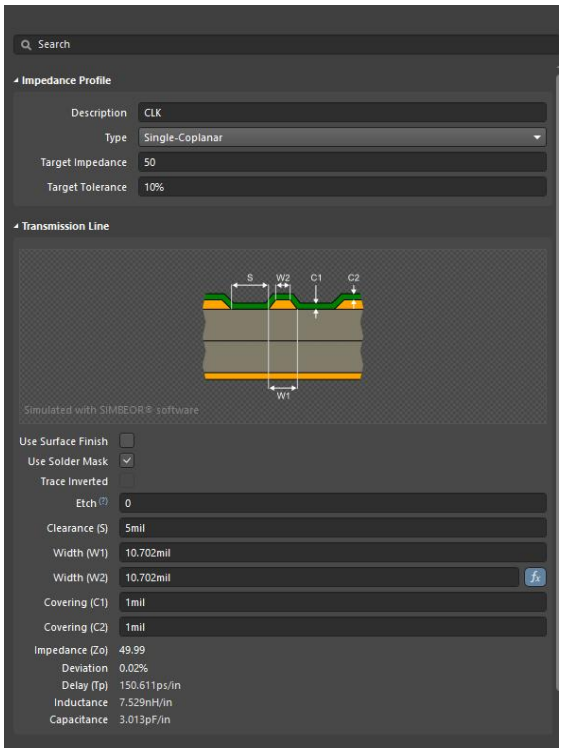


Figure 13: Impedance Profile

3D View of motherboard

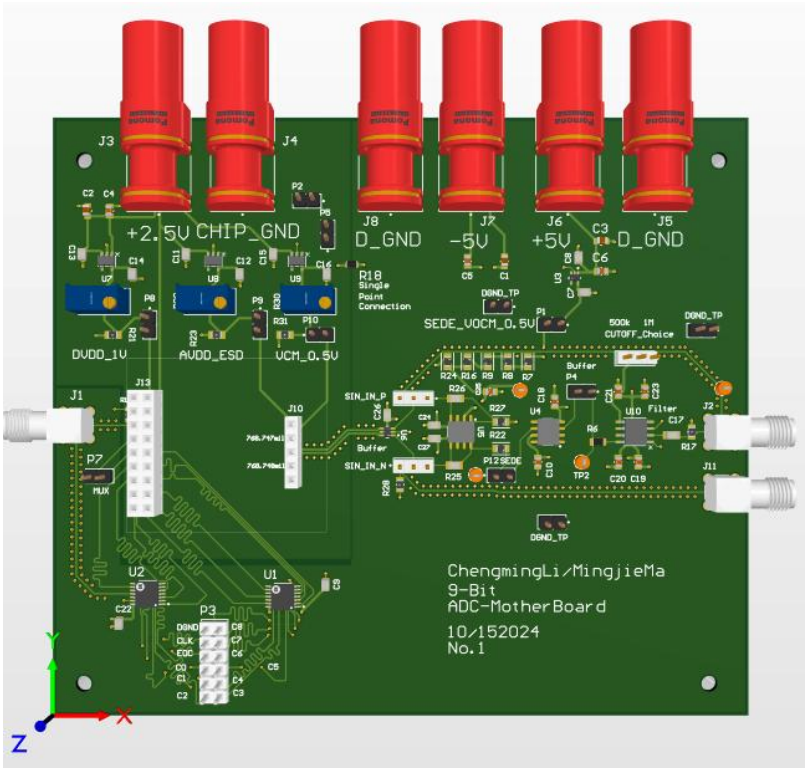


Figure 14: Top side of the motherboard

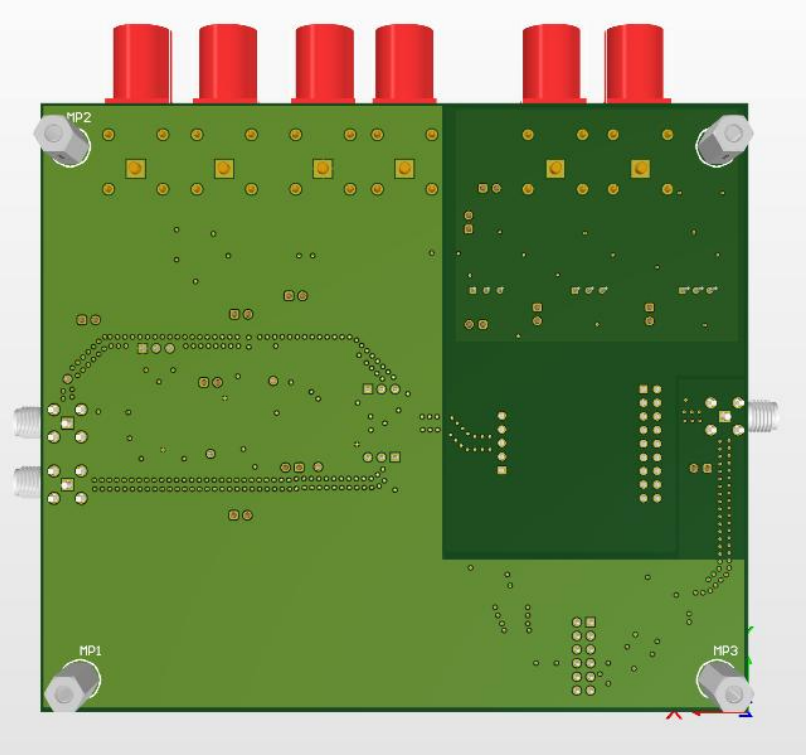
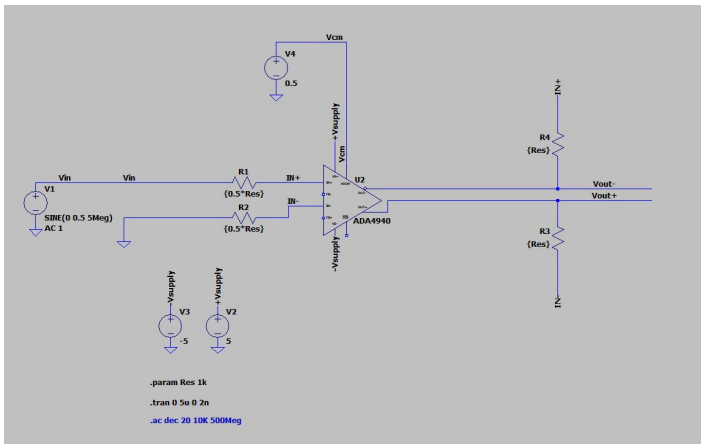
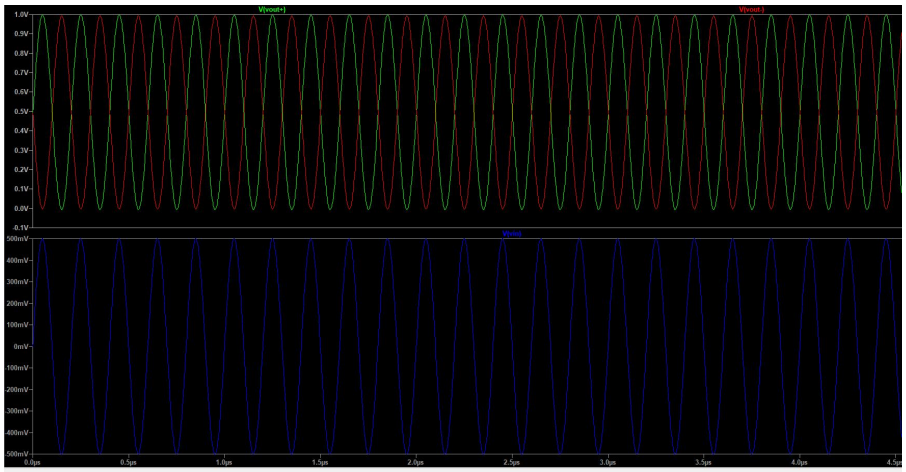


Figure 15: Back side of the motherboard

Design Explanation:

1. **Modularized Design**: between each module, we have put a jumper between. We envision to provide better debug capability in the board testing. This separates the entire system, so we can probe the signals point by point.
2. **Ground Plane Strategy**: They happened at 2nd layer, one on the top left is for the **CHIP_GND(Analog GND)**, and the remaining part is for the **DIGITAL_GND**. And they connect to each other at a single point near the power port. We tried to put the single connection far away from the digital circuit, i.e. ADC output, SEDE signal chain(LPF-Buffer-SEDE-Buffer)
3. **LTspice Verification**: We done the LTspice simulation for our SE-DE chip for proof of concept

a. 

b. 

c. Green and Red are the output, Blue is the input

4. Transmission Line & Shielding:
    a. In the mother board, we treated the CLK signal as Transmission Line and terminated it with 50 ohm shunt resistor, and put via shielding around it. This provides better signal integrity, and also reduces the radiation effect from the CLK signal. I.e. shunt the E-field of CLK to GND (Low impedance path)
    b. Similar ideals are also applied to INP and INN signals. The 50 ohm impedance profile provides us W = 10.702mil and S = 5mil. Meanwhile, these traces are routed with differential traces. INP has 768.747mil, INN has 768.748mil

Components Selection:

Filter: LTC1560-1CS8PBF
Buffer: LT1360CS8
Single End to Differential End Converter (ED DE): ADA4940-1ARZ
Low Dropout Regulator (LDO): (1) TPL503115 (2) MIC5365-2.5YC5-TR
Potential meter: 3296W-1-253LF

So, in order to test the ADC chip smoothly, we create some passive components circuit to support it. First, before the signal moving into the ADC, we need a system that provide (1) efficient drive strength to drive the ADC chip due to its large cap array, (2) differential signals with 0.5v common mode to make sure the rail-to-rail input signal swing, (3) effective and reasonable low pass filter to prevent high frequency's signals to alias back.

In order to satisfy the three main purpose list above, we use a system as:
Anti-Aliasing Filter -- Buffer -- Single end to Differential end converter -- Buffer
The filter we choose LTC1560-1CS8PBF can adjust its bandwidth by a pin called 0.5fc/fc. When this pin is connected to high voltage level which is 2.5v here, the cut off frequency is 500 kHz, while connect it to low voltage level which is -2.5v, the bandwidth is extended to 1M Hz. This phenomenon is exactly what we want. In the Cadence simulation, we are using a 605 kHz sinusoid wave, so the 500 kHz bandwidth can give us a similar simulated result fortunately. The 1 MHz bandwidth is also the maximum cutoff frequency that is in stock online to measure the high frequency performance.
The filter is also DC decoupling, with maintained the AC signal. The AC signal then go into the SE DE: ADA4940-1ARZ which is a fully differential amplifier (FDA). Compared with SE DE that is consist of an inverting op amp and a non-inverting op amp; the FDA is always suitable to high frequency operation and no need for input dc biased.
The buffer is used as recommended in datasheet to maximum the drive strength.

In order to get a high performed Chip power supply, we decided to make the voltage supply from the voltage source to pass through a LDO first, to remove any noise or digital interfere. TPL503115 is a LDO that convert 2.5v into 1.5v. The reason why we do not convert it to 1v which is the Chip required voltage directly is we are considering some voltage loss during the transmission line and the not 100 precented precise regulated output voltage. Instead, we use a potential meter to form a voltage divider. The potential meter is 25 kohm with 25 turns, which means 1 turn represent 1 kohm. We will combine it with a 1 kohm resistor to precisely provide the 1v and 0.5v power supply to the chip. If we are facing some voltage loss, or undesired test result based on in sufficient voltage supply, we can also use the potential meter to provide a voltage that is slightly beyond 1v or 0.5v.

MIC5365-2.5YC5-TR is straightforward to convert 5v voltage source to 2.5v voltage that power all passive chips on PCB. Also, since the ESD power is not that sensitive, so we will power them from the voltage source directly instead use the potential meters.