ECE266 Lab2

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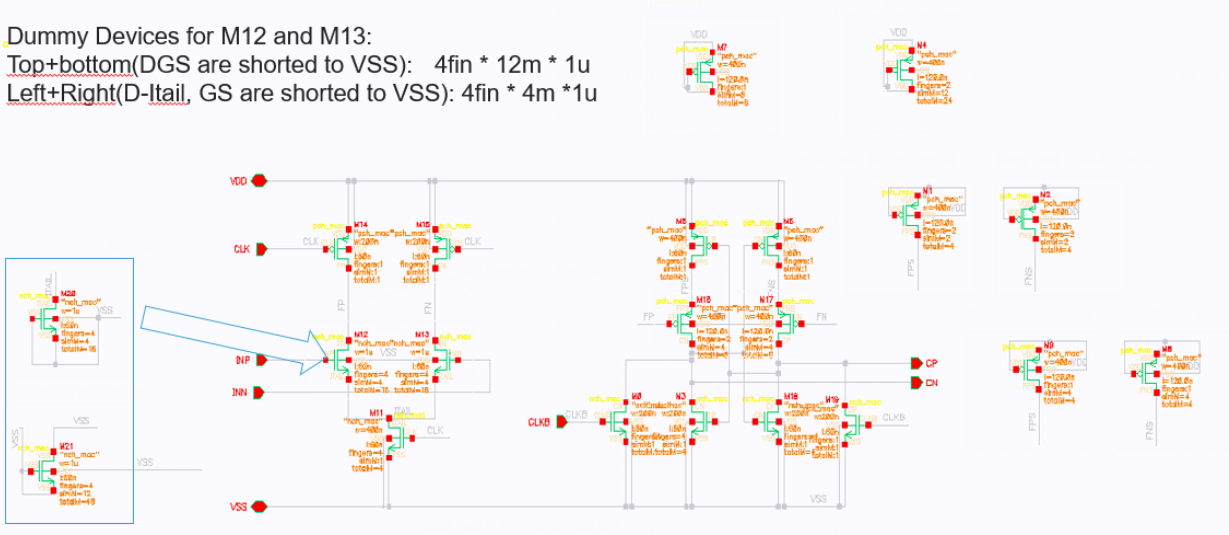
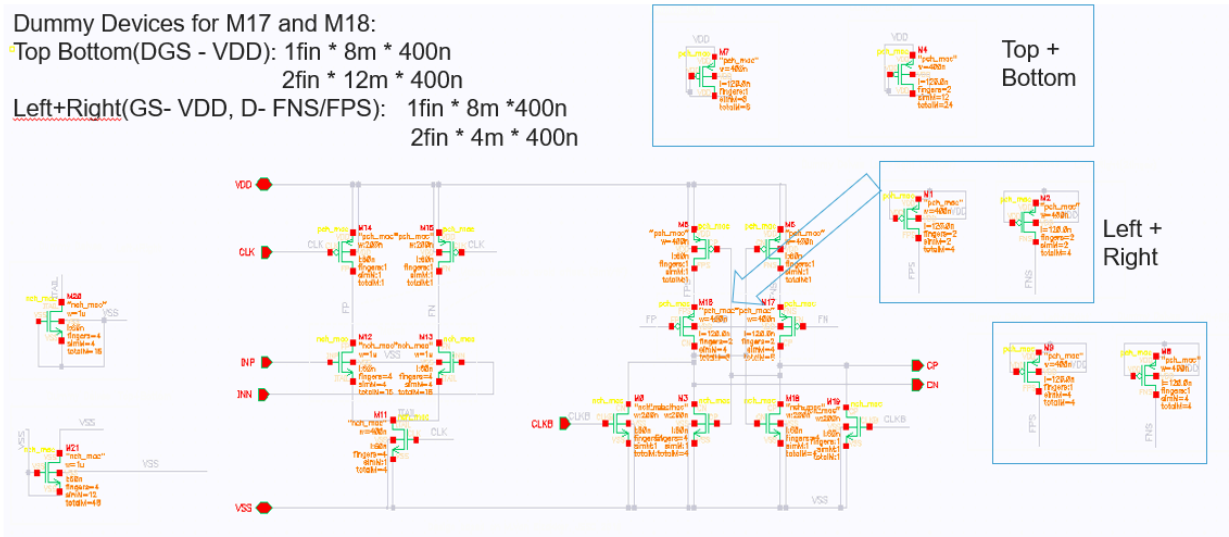
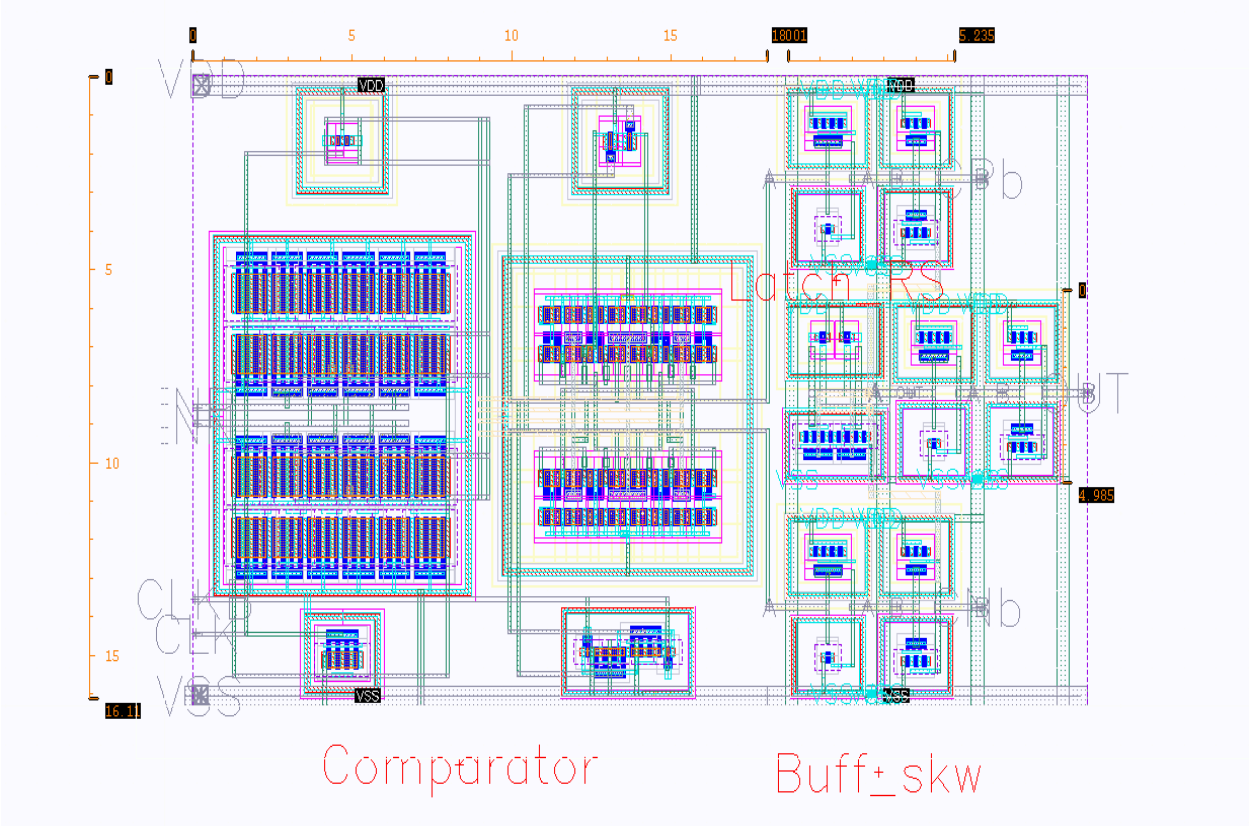
Schematic

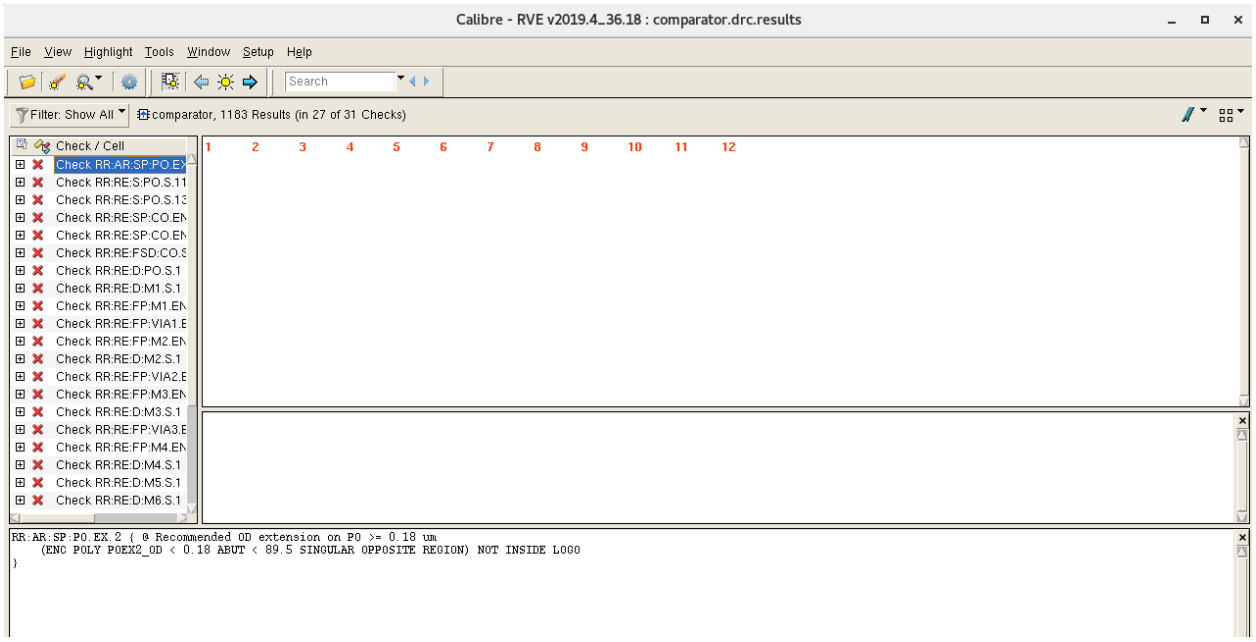

Dummy Devices for M12 and M13:
Top+bottom(DGS are shorted to VSS): 4fin * 12m * 1u
Left+Right(D-Itail, GS are shorted to VSS): 4fin * 4m *1u
VDD
CLK
INP
INN
VSS
CLKB
CP
CN


Dummy Devices for M17 and M18:
Top Bottom(DGS - VDD): 1fin * 8m * 400n
2fin * 12m * 400n
Left+Right(GS- VDD, D- FNS/FPS): 1fin * 8m *400n
2fin * 4m * 400n
Top +
Bottom
Left +
Right
VDD
CLK
INP
INN
VSS
CLKB
CP
CN

Layout

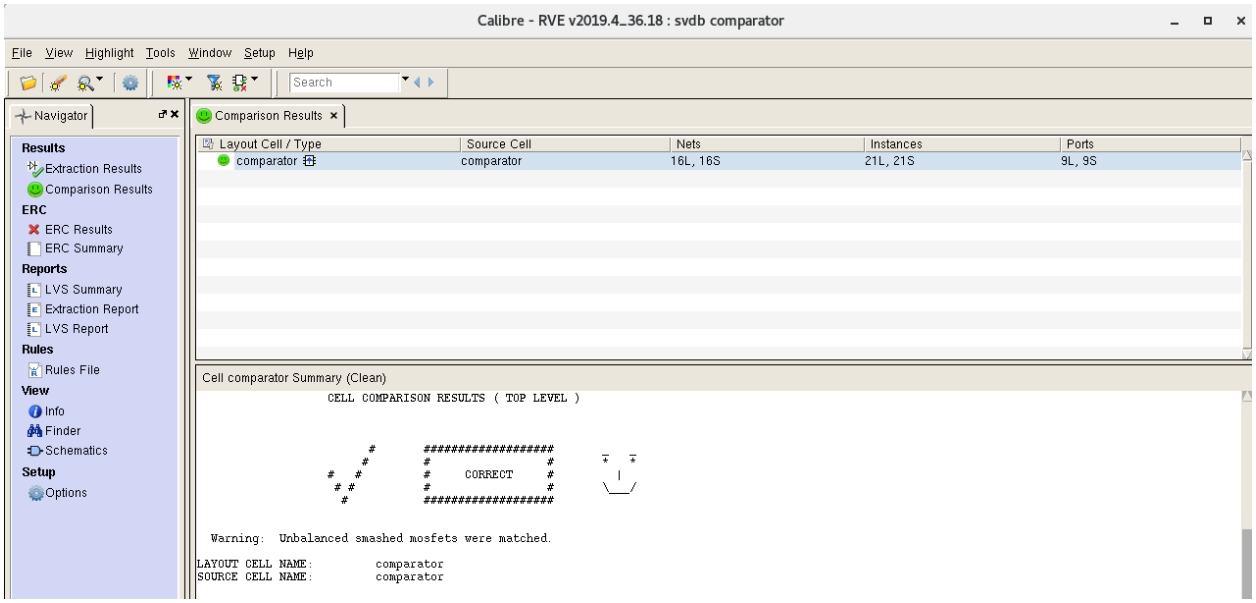


DRC Result Summary



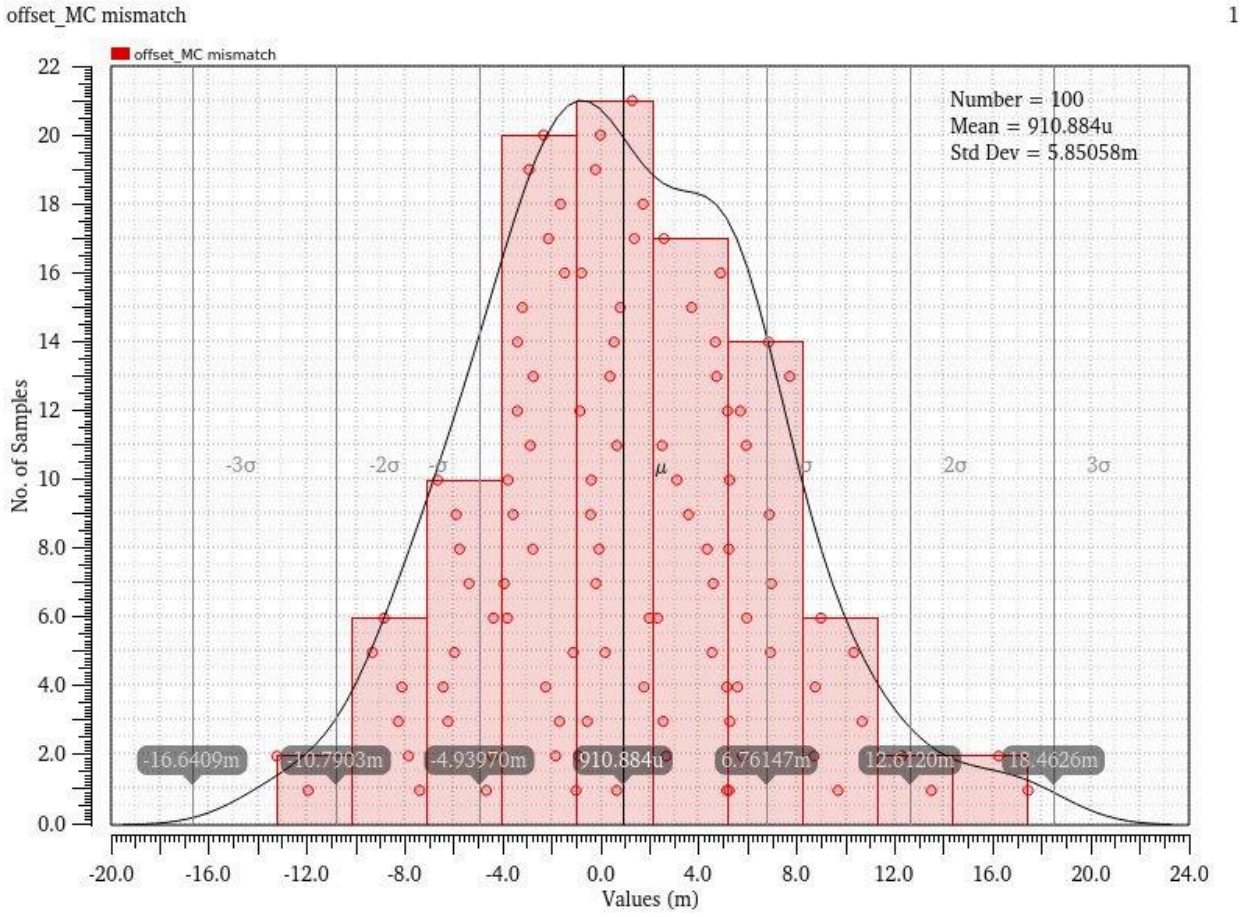
RR Errors are ignored in the layout

LVS Result Summary



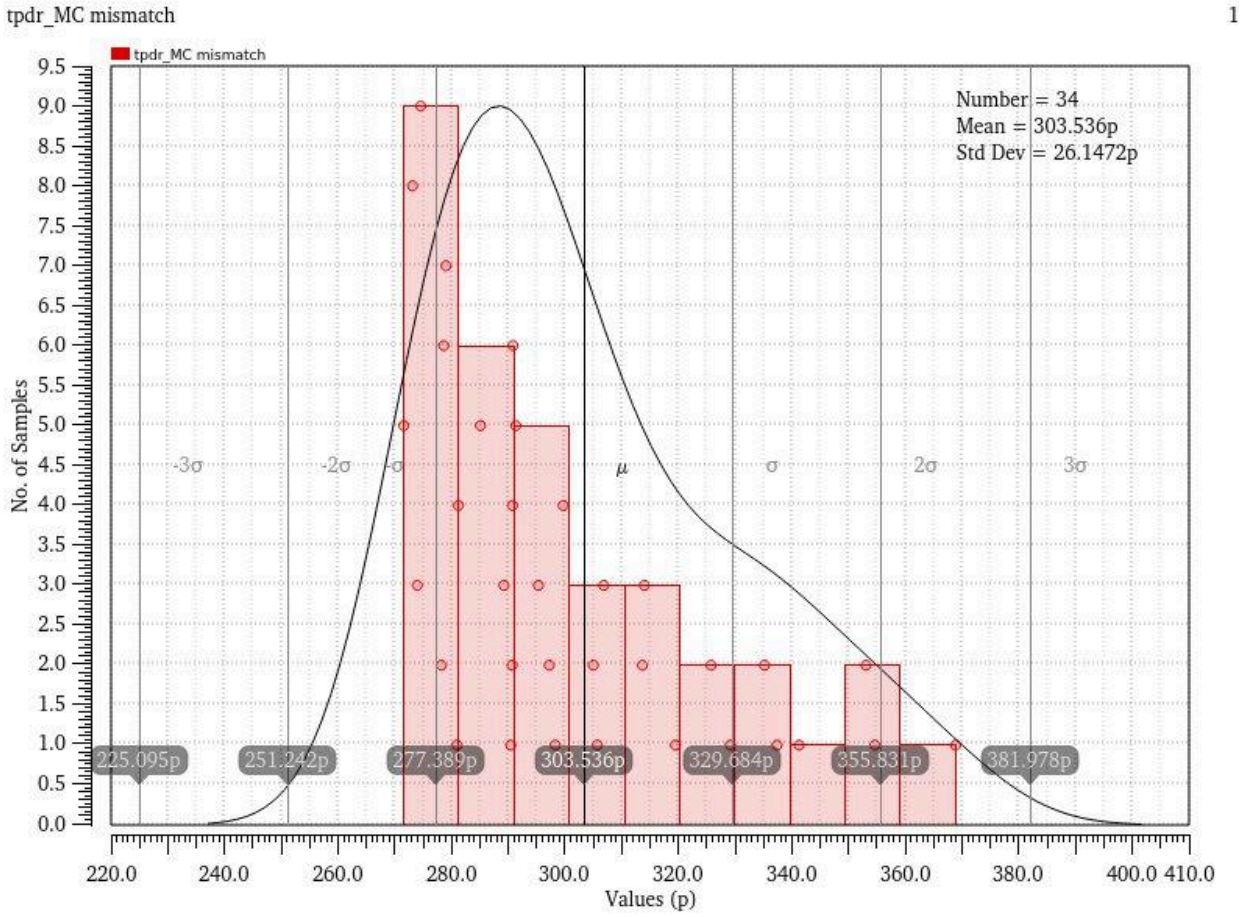
Input-referred offset

Test Corners	TT	FF	SS
#1 Iteration(C+CC)	5.545m	6.725m	4.428m
#2 Iteration (C+CC)	509.8u	-170.7u	705.9u
#2 Iteration(R+C+CC)	740.4u	269.2u	386.4u
Lab1(R+C+CC)	2.787m	-9.271m	3.307m



Propagation delay

Test Corners	TT	FF	SS
Lab2(R+C+CC)	323.6p	265.4p	455.9p
Lab1(R+C+CC)	255.1p	200.3p	344.1p



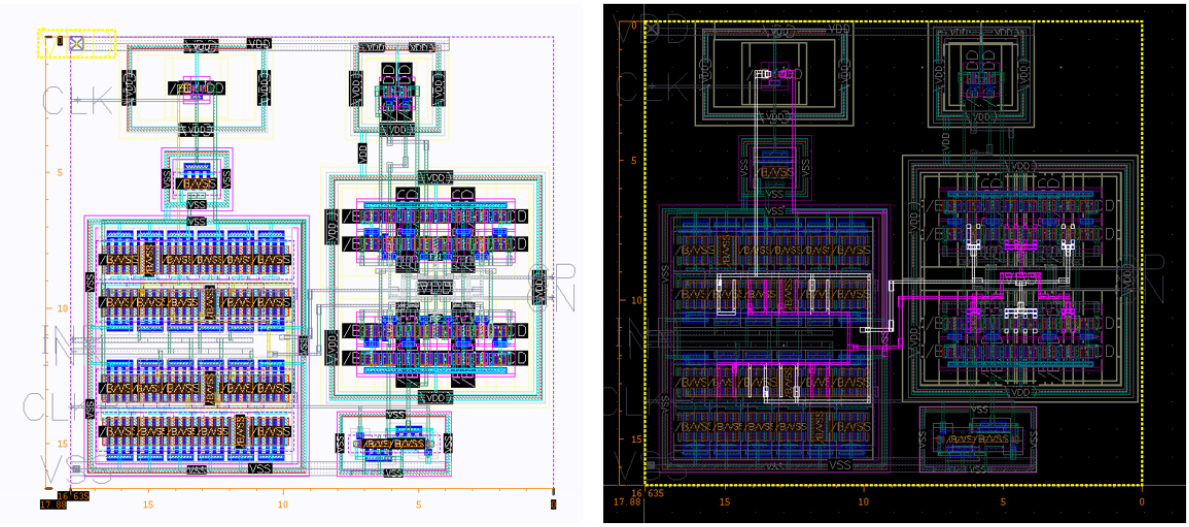
Comments and conclusions

1. We started the design from the comparator_core as it is the most important layout that will affect the circuit performance, input-referred offset and propagation delay. And this layout took us a fair amount of time and two iterations to meet the specs requirement.The first iteration of the layout doesn't have a very symmetrical metal flowing on the pairs of nodes. And we realized that after we failed the specs simulation. In the second iteration, we were able to figure out the root cause of mismatch on the node pairs "FP and FN", and passed the specs simulation and requirement.
2. The first technique we applied was fingering. In the first and second stages of the comparator, M12, M13, M17 and M18 transistors were very wide. And the wide area of the drain and source will increase the parasitic capacitance tremendously, which will affect the propagation delay and overall layout area. Then we decided to fingering down the M12 and M13 transistors into this combination(4f*4m*1u), and M17 and M18 into (2f*4m*400n). As a result, the comparator layout was shrunk and smaller compared to the lab1 we have.
3. The second technique we applied was the common-centroid. This is the technique that we used to mitigate and average out the process variations, or mismatch, between the devices M12 and M13, and M17 and M18. By using this technique, the transistors' performance will be matched to minimize the input referred offset. And the common-centroid pattern we used is "1st row ABBA, 2nd row BAAB". In this pattern, both devices A and B will get the equal effects of process variation.
4. The third technique we applied was adding the dummy devices. This is the technique that we used to mitigate the process variation on the boundary devices. Usually, on the boundary devices, they receive very different doping compared to the devices close to the middle. These dummy devices are back-annotated and added around the M12, M13, M17 and M18. For the Top and bottom side of the dummy devices, the DGSB terminals are all shorted to VDD/VSS depending on the type of device. And the left and right side of the dummy devices GSB are all shorted to VDD/VSS, but the drain is shorted to an intermediate node, depending on whether the node is important for the overall circuit performance or not.

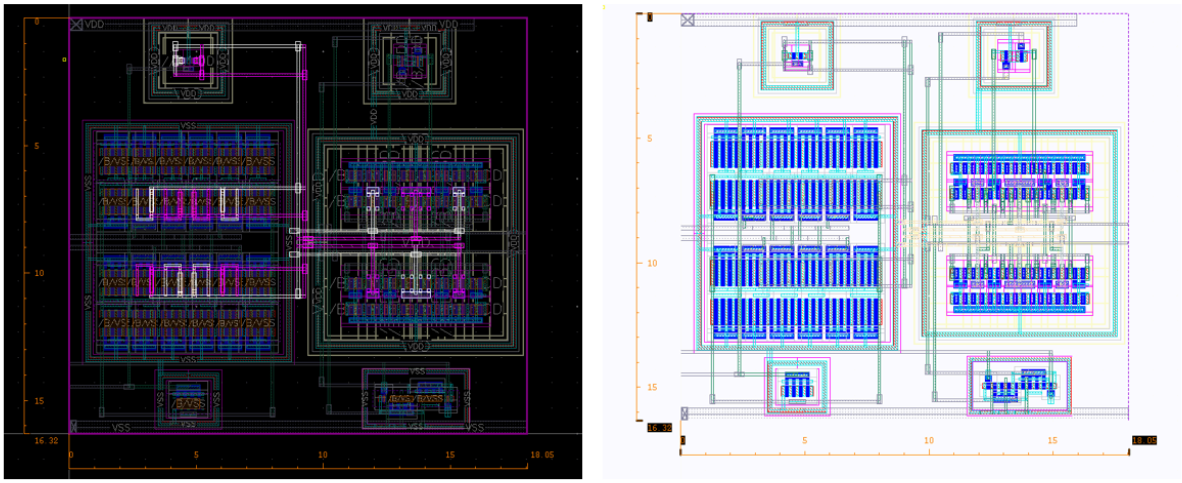
5. Something I learned from this lab are:
    a. Guard ring needs to be placed for the transistors who need the best performance, like the current mirror, differential pair, etc. And always be careful about what the annotation says in the schematic. It includes information about when the Guard ring needs to be placed for sure. On the other hand, a guard ring is not required for every device.
    b. By using the fingering, common-centroid and dummy devices, the process variation will be mitigated and averaged out to each device. These techniques are unique to the sensitive pair of devices. Most often, for example, the input referred offset, we focus on more about the (R+C+CC) difference between the pair, other than the absolute value.

    c. Symmetry layout design in both x-axis and y-axis. Symmetrical design is unique to achieve the matching. Such design makes sure each pair of devices see the similar amount of capacitance and resistance. And so, the difference between devices will be mitigated in the layout-wise.
    d. Redundant metal extension, In our second iteration layout, we expanded some of the metals to match the metal length of the other devices, so that a similar amount of R+C will be seen.
    e. Even number metal layer should go horizontally, and the odd number metal layer should go vertically. This would maximize the layout spacing usage.
    f. Using ADE XL to run the process corner and Monte Carlo simulation
    g. Larger metal width for the VDD/VSS connection
6. Something I didn't learned very well from this lab are:
    a. The best design layout practice! Similarly to PCB layout, there are always some good rules of thumb, which we always need to follow. But, I couldn't get the bad layout choices vs. good layout choices from this lab.

Appendix



First iteration of Design, FP and FN



Second iteration of Design, FP and FN