ECE266 Lab4

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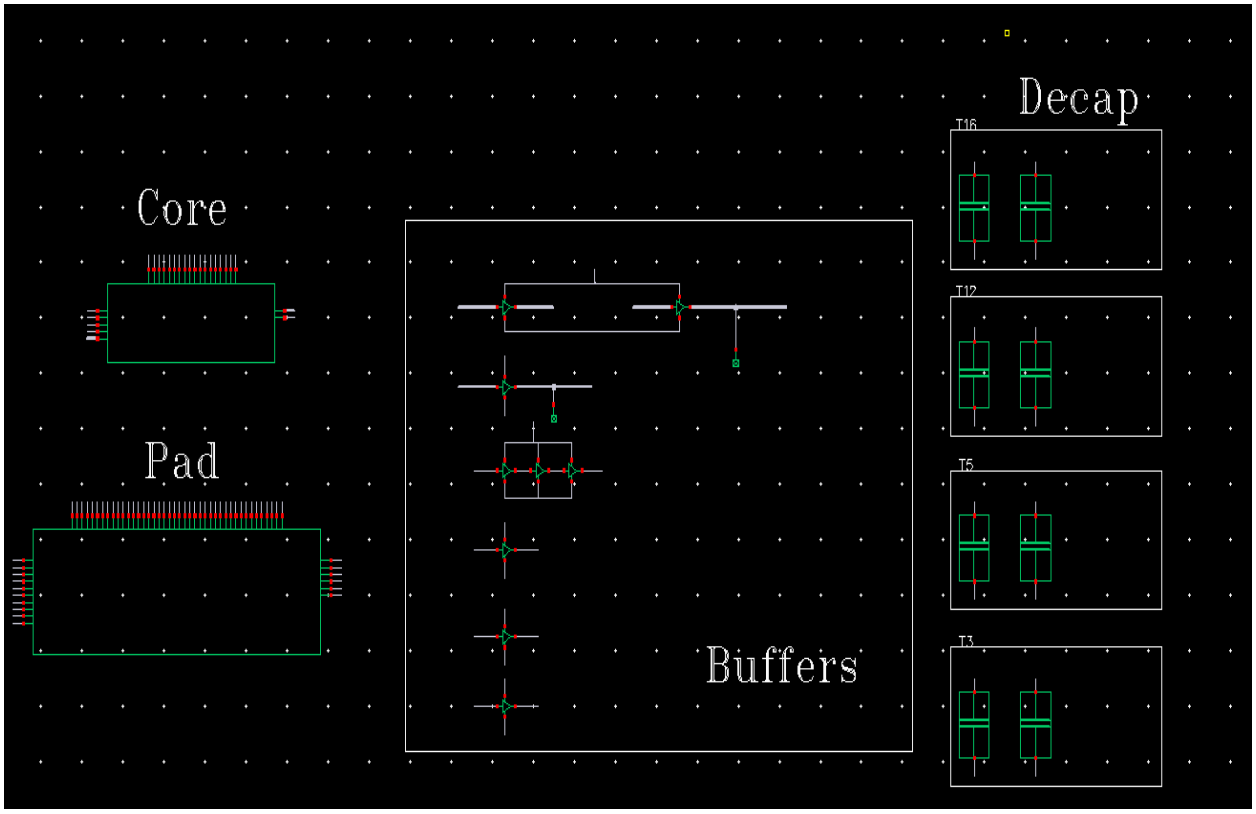
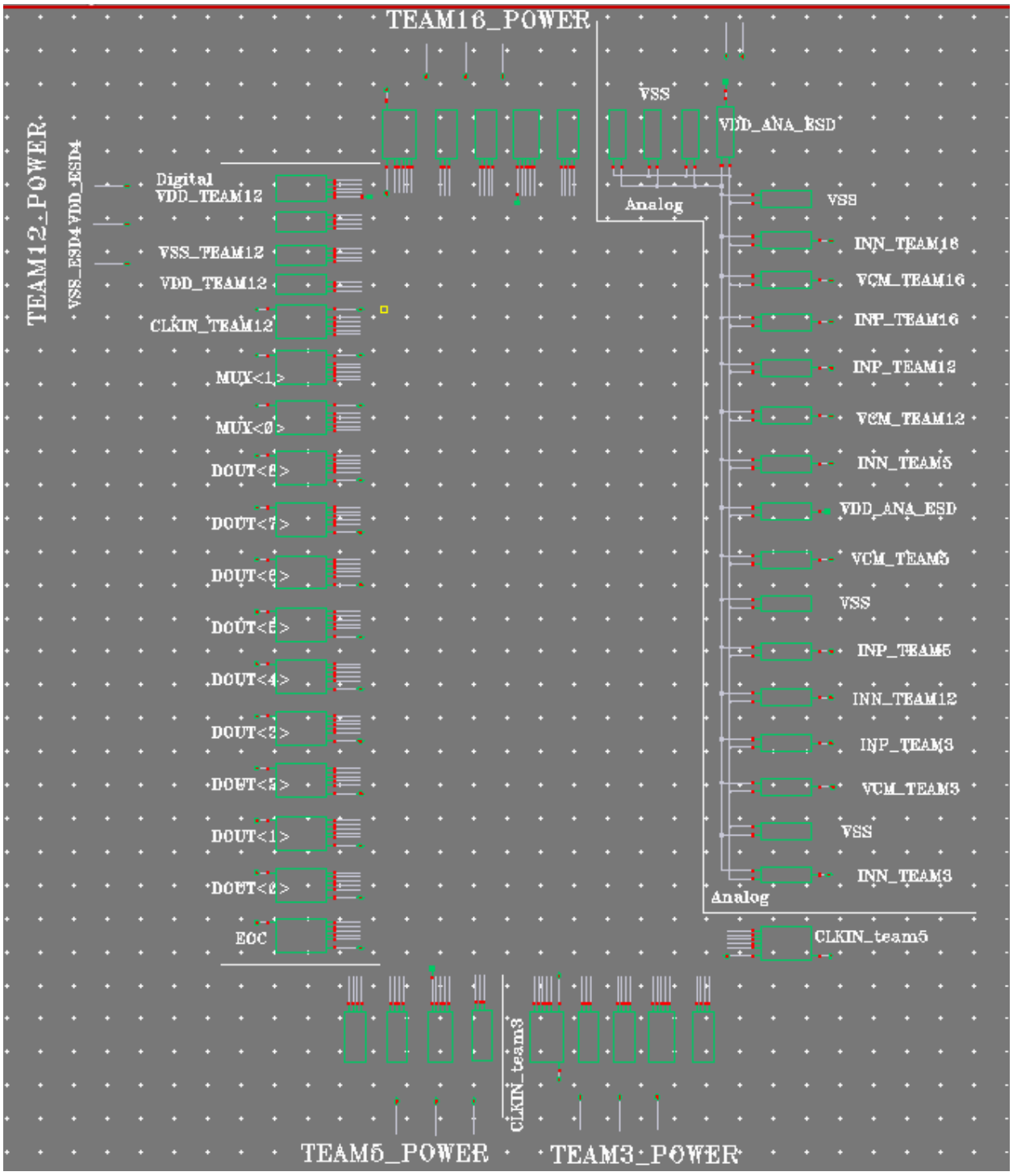
Top Level Schematic



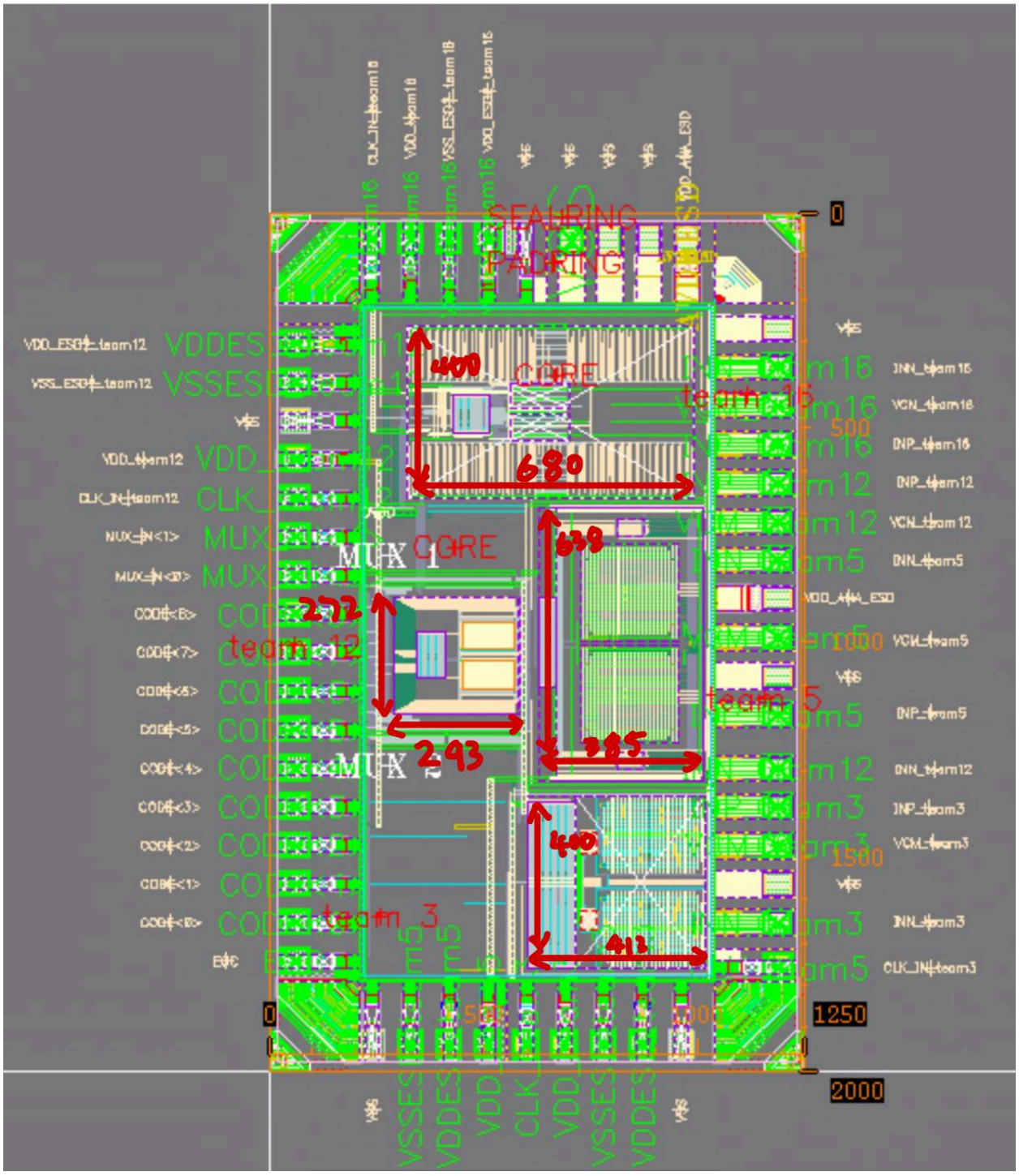
Top Schematic

Schematic of Pad Ring



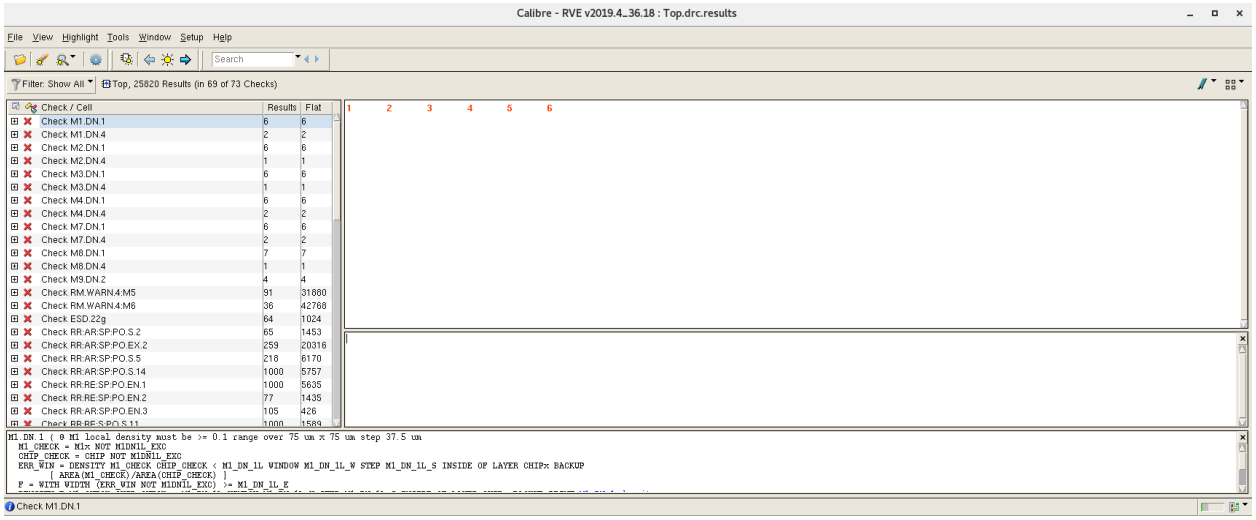
Pad Ring Schematic

Picture of Top-level Layout



Top Level Layout (294.17 * 272.41)

DRC Result Summary

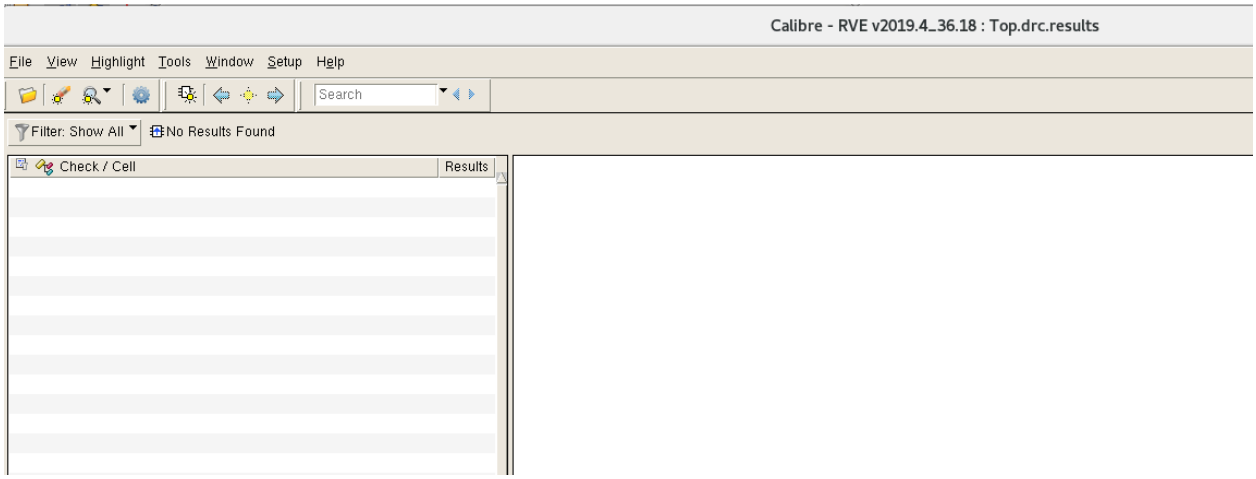


Note: Our mega group2 is thinking of waiving M2-M9. This is the DRC result before we fill out the M1 Metal.(Deadline of this report is 5PM Fri 07/06). At this time stamp, we still have 1 group that didn't finish their M1 local dummy fill. So the M1 DN is still shown in the above.

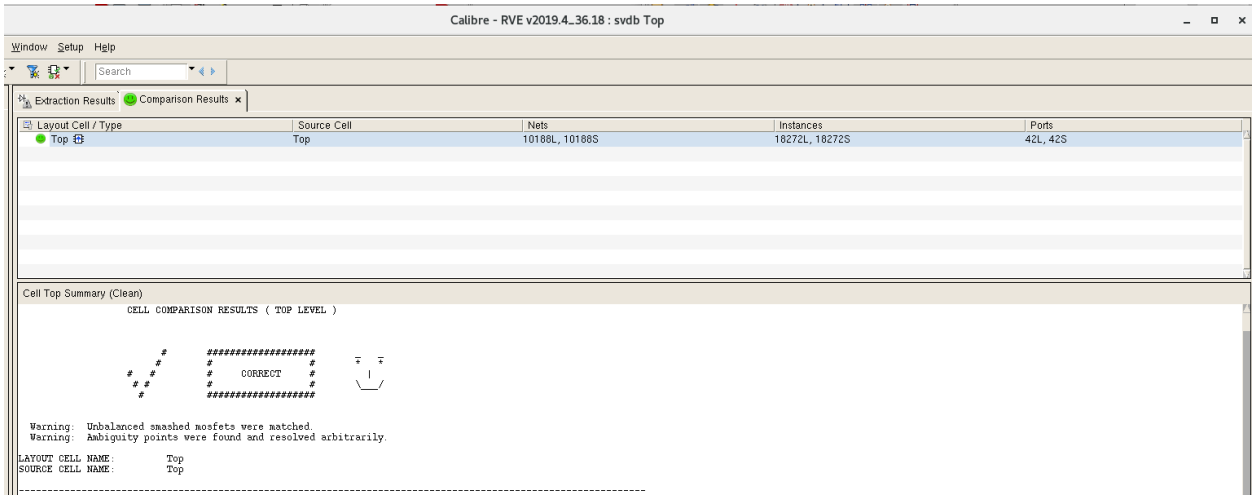
Ideally, the M1 DN error will be gone. And M2-M9 DN are expected to be there.

RR Errors are ignored in the layout

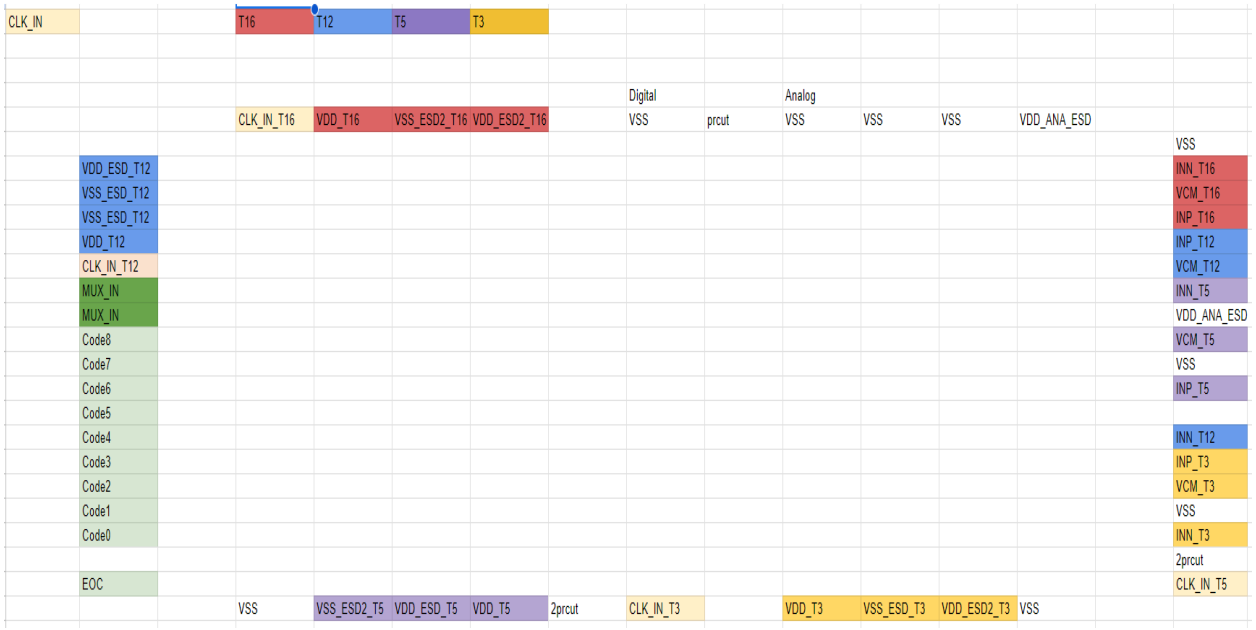
ANT Summary


Calibre - RVE v2019.4_36.18 : Top.drc.results
File View Highlight Tools Window Setup Help
Search
Filter: Show All
No Results Found
Check / Cell
Results

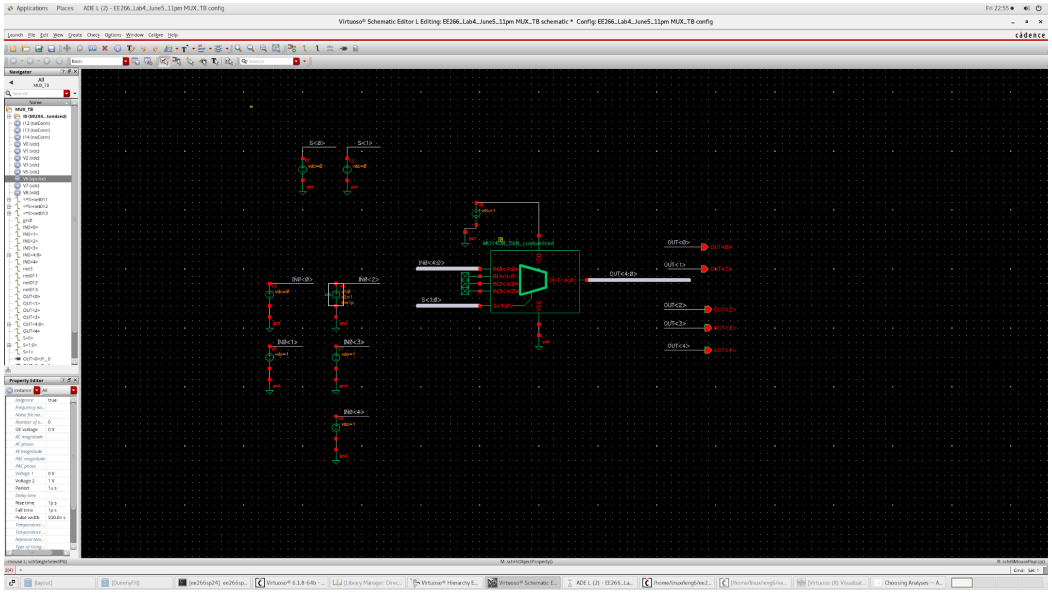
LVS Result Summary

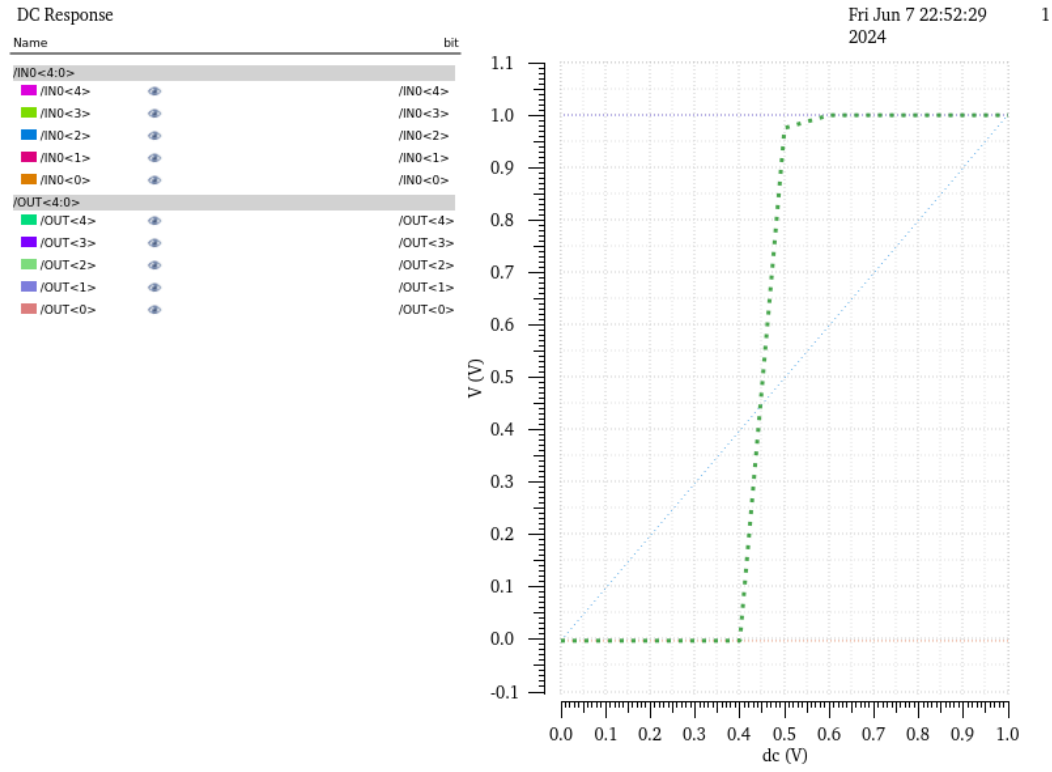


Documenting padding frame

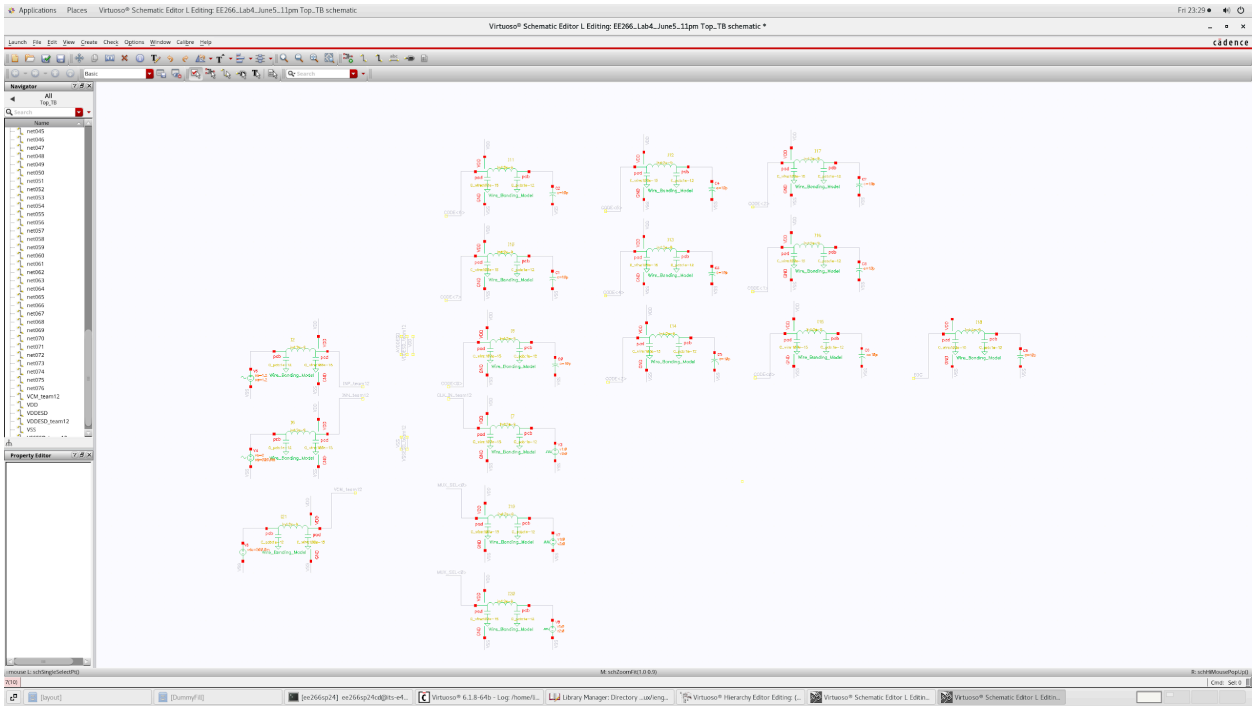


Top-level simulation with pin-model





MUX TB Circuit

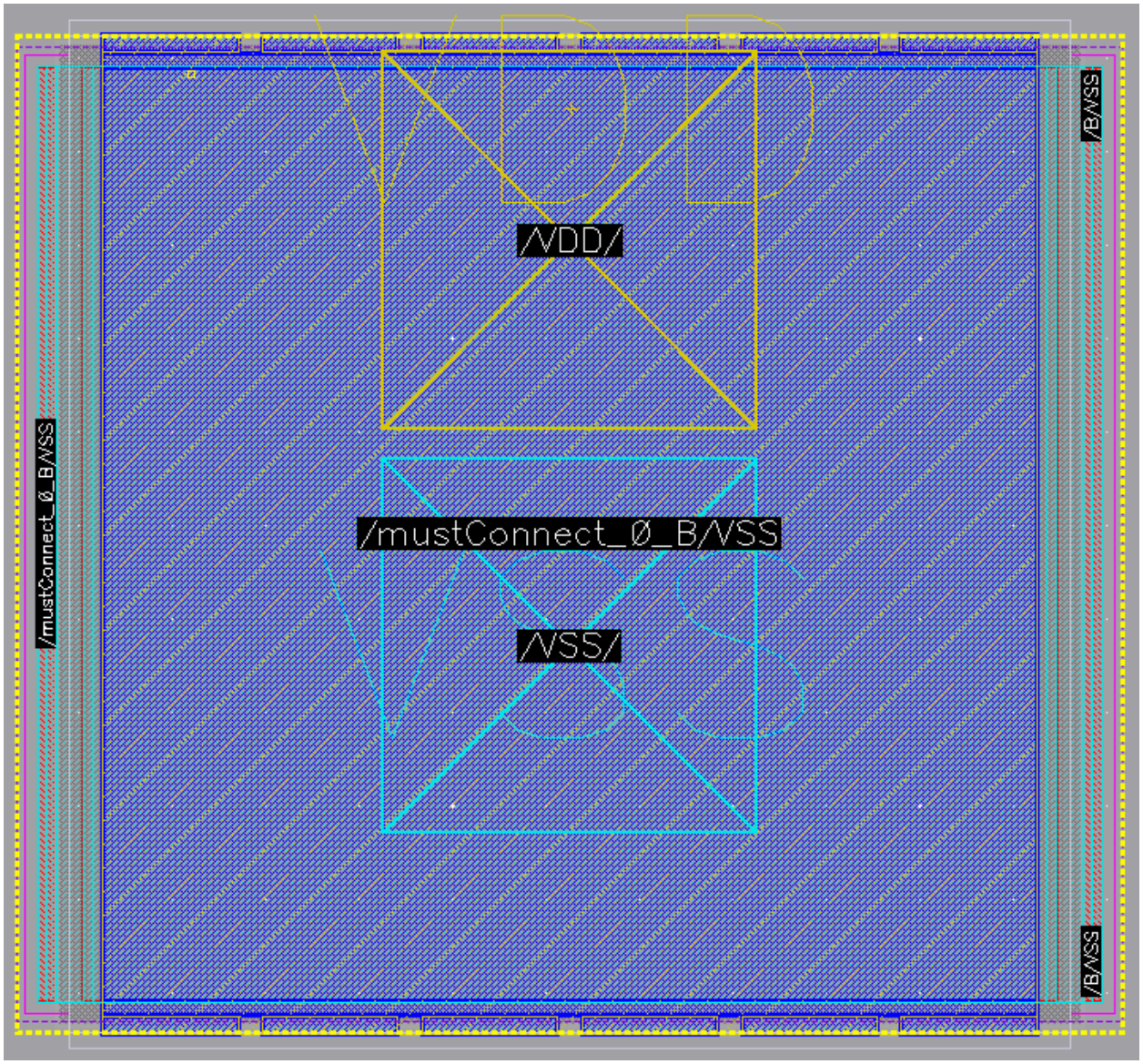


Top Level TB schematic

Comments and conclusions

1. Conclusions
    a. Mega group2 divided up the work into padring, seal ring, core level, floorplanning, top level routing, decap, mixer, buffer, and dummy filling
    b. We started developing the work from top to bottom, and cleaned the drc and lvs at each level. So at the top level, the DRC and LVS were much easier to resolve.
    c. Our sub-group is responsible for padring connections, decap design and routing, seal ring design, and waiver presentation preparation.
    d. For padring connection, we realized how different it is between the analog pad and digital pad. And how the pad will be powered through the pad ring. This is a very good experience learning the mechanism of IO Pad
    e. For Decap design, we use a very wide and thick gate oxide transistor-capacitor with w=10u and l = 10u. The decap filling helps a lot in solving the Density problem in M1 and M2.
    f. Seal ring, we know how to build a mosaic and how the delta x and y can be tweaked to fulfill the requirement. Originally there are some overlapping DRC, and we were able to fix it by tweaking the #of mosaic and delta x to fix it
    g. This is our group's first time preparing the waiver presentation slices. It is a good learning experience to understand why and how we need this. It's good preparation for the future tape out.
2. Something I learned from this lab are:
    a. The design methodology needs to be from top to bottom, which makes it easier to route and clean drc and lvs errors.
    b. The mechanism of IO Pads. And how to customize the pad ring for our circuit specific use.
    c. Creating Decap will be useful for both circuit-purpose as reducing IO drop in the rails and Density-error purpose.
    d. Understanding the need and purpose of Seal rings during chip manufacturing.
    e. How to do dummy filling and using a dummy exclusion layer in the layout.
    f. Waiver presentation slices.
    g. Streaming in and back the gds file with dummy filling.
    h. How dummy filling affect the ratio of Capacitor DAC
    i. Team work

Appendix



Customized 10u Decap