ECE 266 Lab3 Design Review

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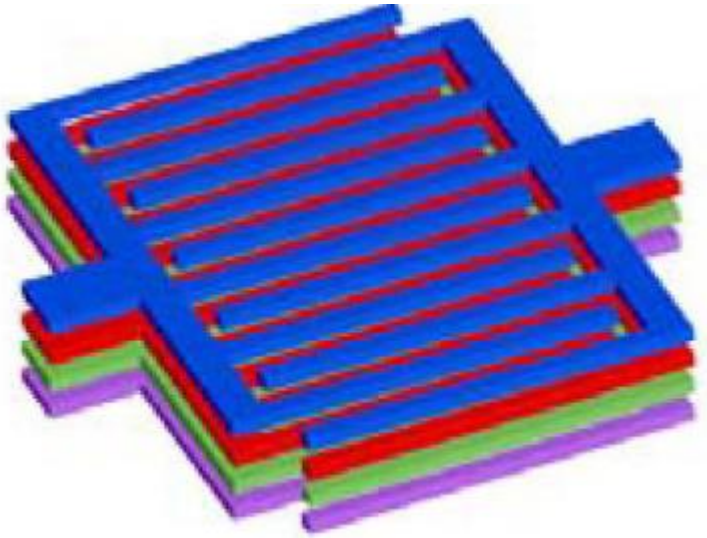
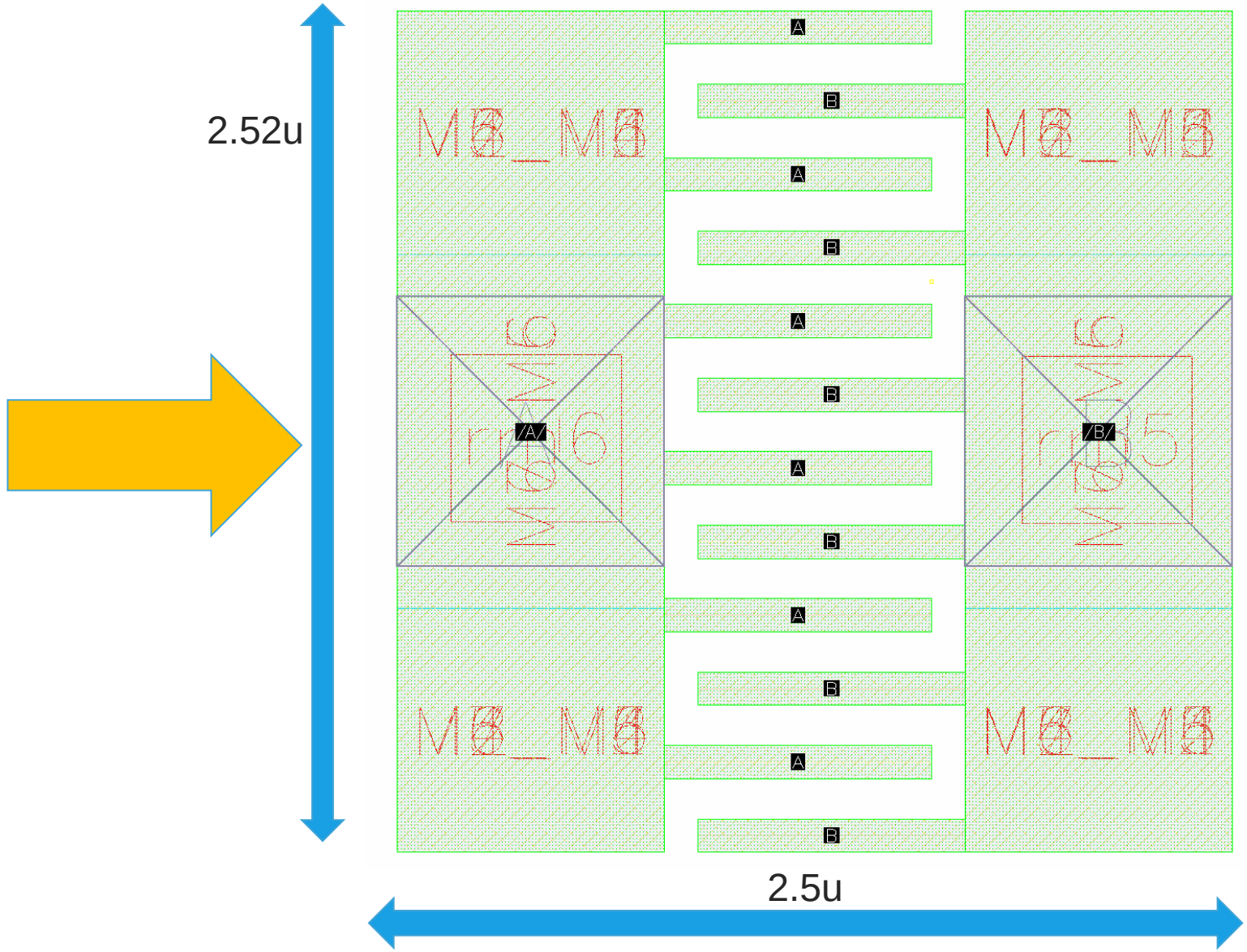
uCAP Layout

Layer: M1 to M7 stack up

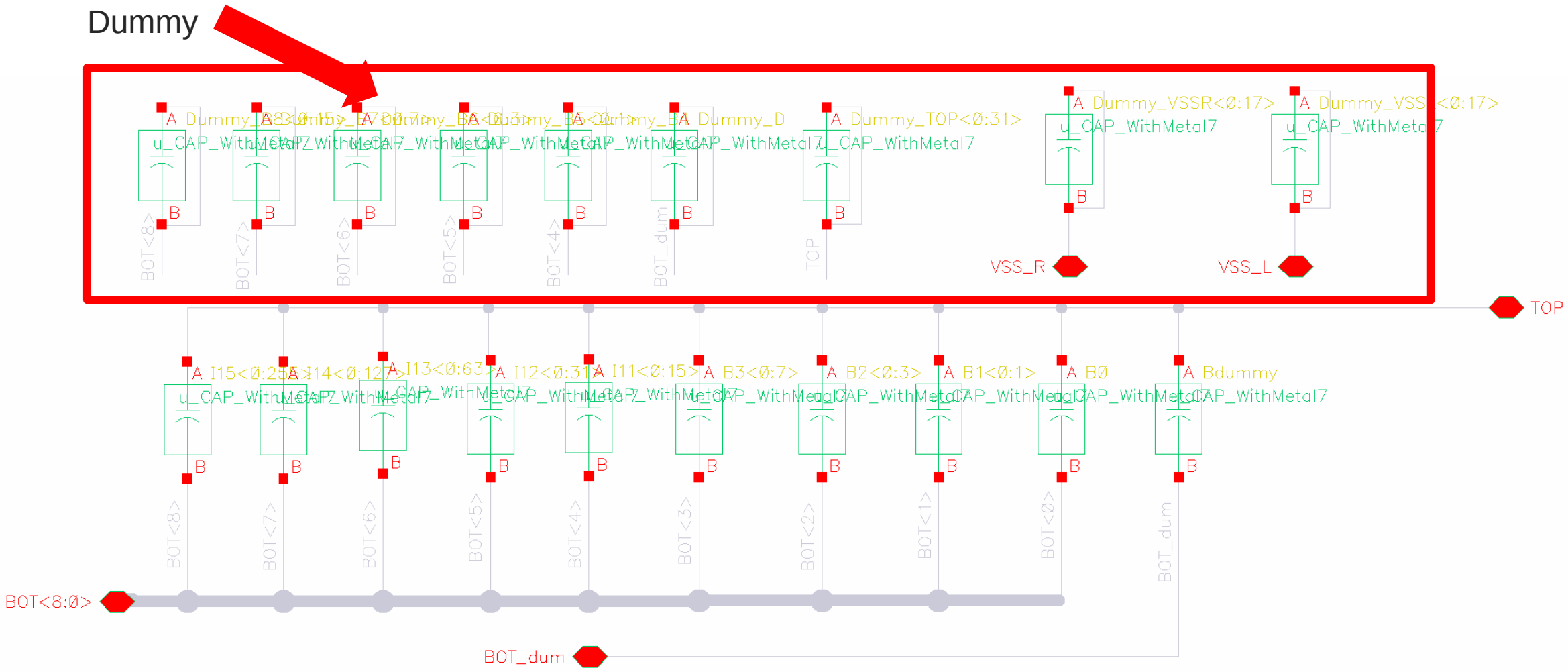
Size: 2.5u by 2.52u

CC: 5fF





Schematic-singleDAC(cap bank)



Metal Width vs. Current

- How much current we need?
  - Q = CV
  - $\frac{dQ}{dt} = I = C \times \frac{dV}{dt}$
  - $\int Idt = \int CdV$
  - $I\Delta t = C \times VDD$
  - $I(per\ unit\ Cap) = \frac{C \times VDD}{\Delta t} = \frac{5fF \times 1}{1.65us} = 3n\ A$
  - $I(per\ column) = 3n\ * 16 = 48n\ A$

- How wide of the trace should be?(Read from PDK doc)
  - M1(0.4um): 0.57 mA
  - M2 – M7 (0.4um): 0.72 mA
  - M2 – M8 (0.8um): 1.47 mA

singleDAC(cap bank) Floorplan – Common Centroid

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	2	2	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	1	1	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	D	0	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	2	2	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	3	3	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	4	4	5	6	6	8	8	8	8	8	8	8	8	8	8	8	8	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

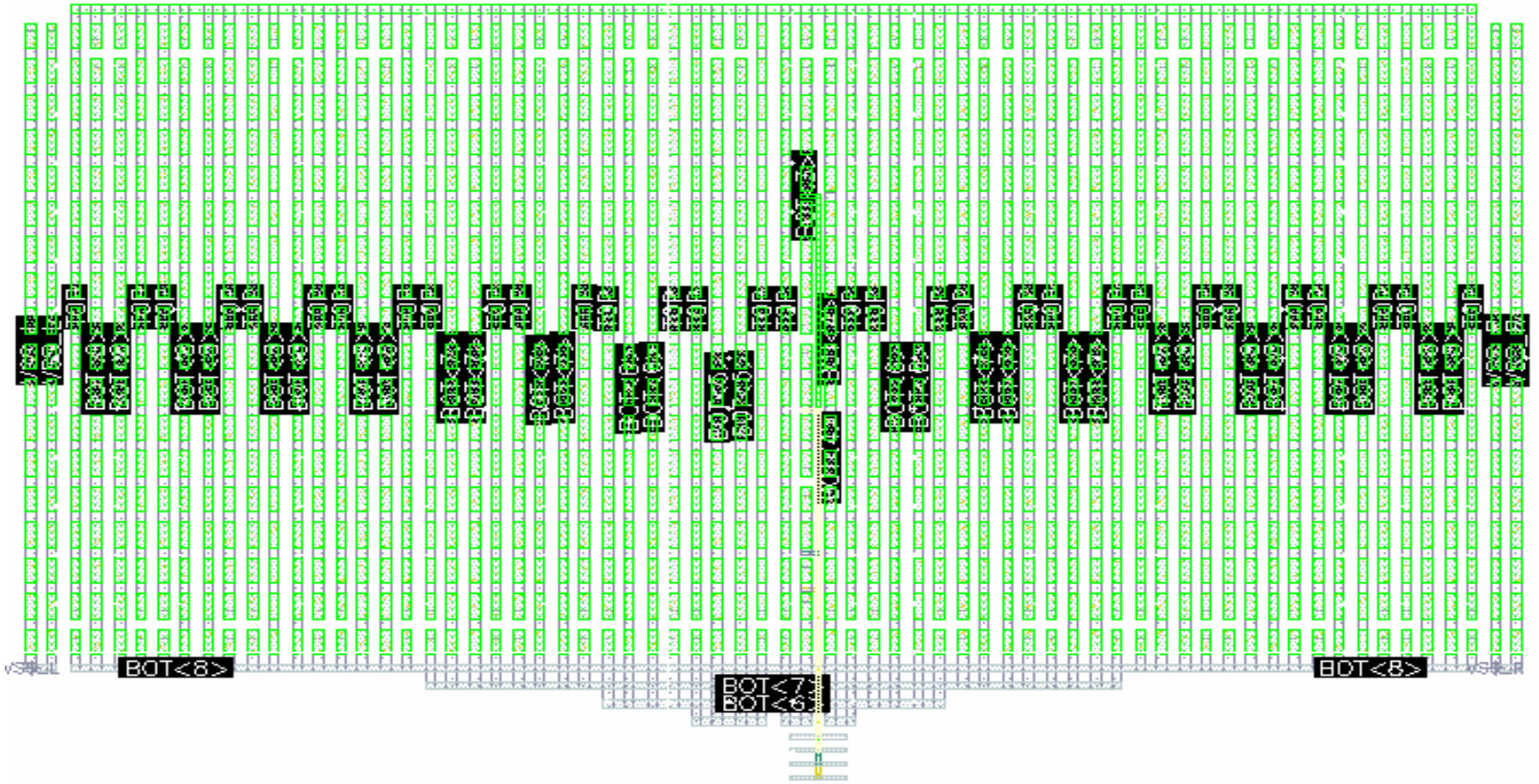
Bit	B0	B1	B2	B3	B4					
CC(fF)	10.14	21.8	44.04	58.25	101.5					
Ratio		2.145	2.02	1.322	1.74					

- The ratio doesn’t match, the floorplan is not used

Layout Iteration1 - singleDAC – Bit0123 - center

Non-symmetry

Bit 0:3 (M1, M3, M5, M7) overlapping



76.74u

121.97u

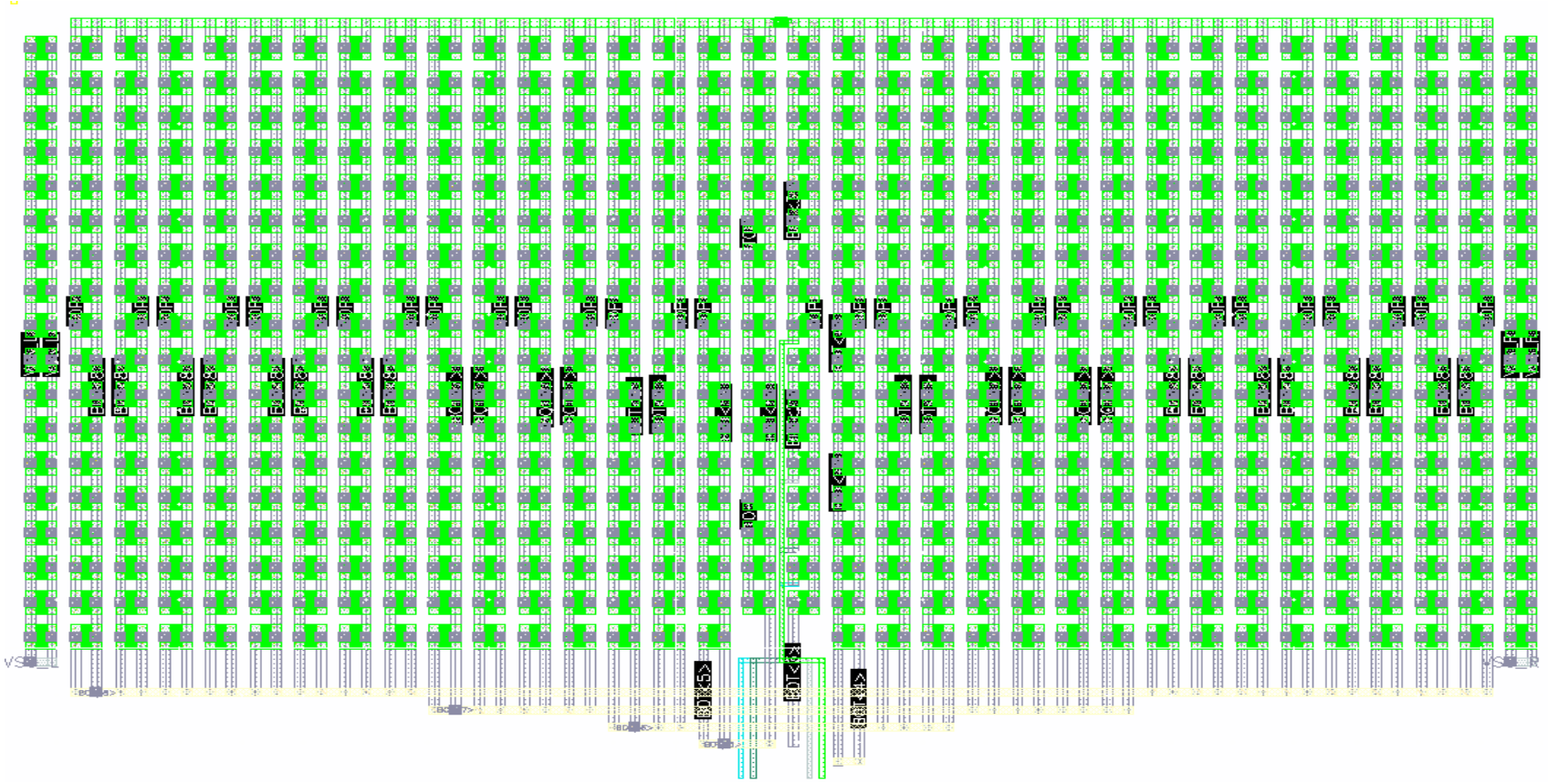
Layout Iteration2 - singleDAC – Remove2Dummy

Pro:

- Symmetry
- Less CC between Bits and
- Less CC effects to the Dummy for bit0

Cons:

- Sensitive to C(w.r.t substrate)
- Sensitive to the length of Bit 0:3
- Non-binary routing

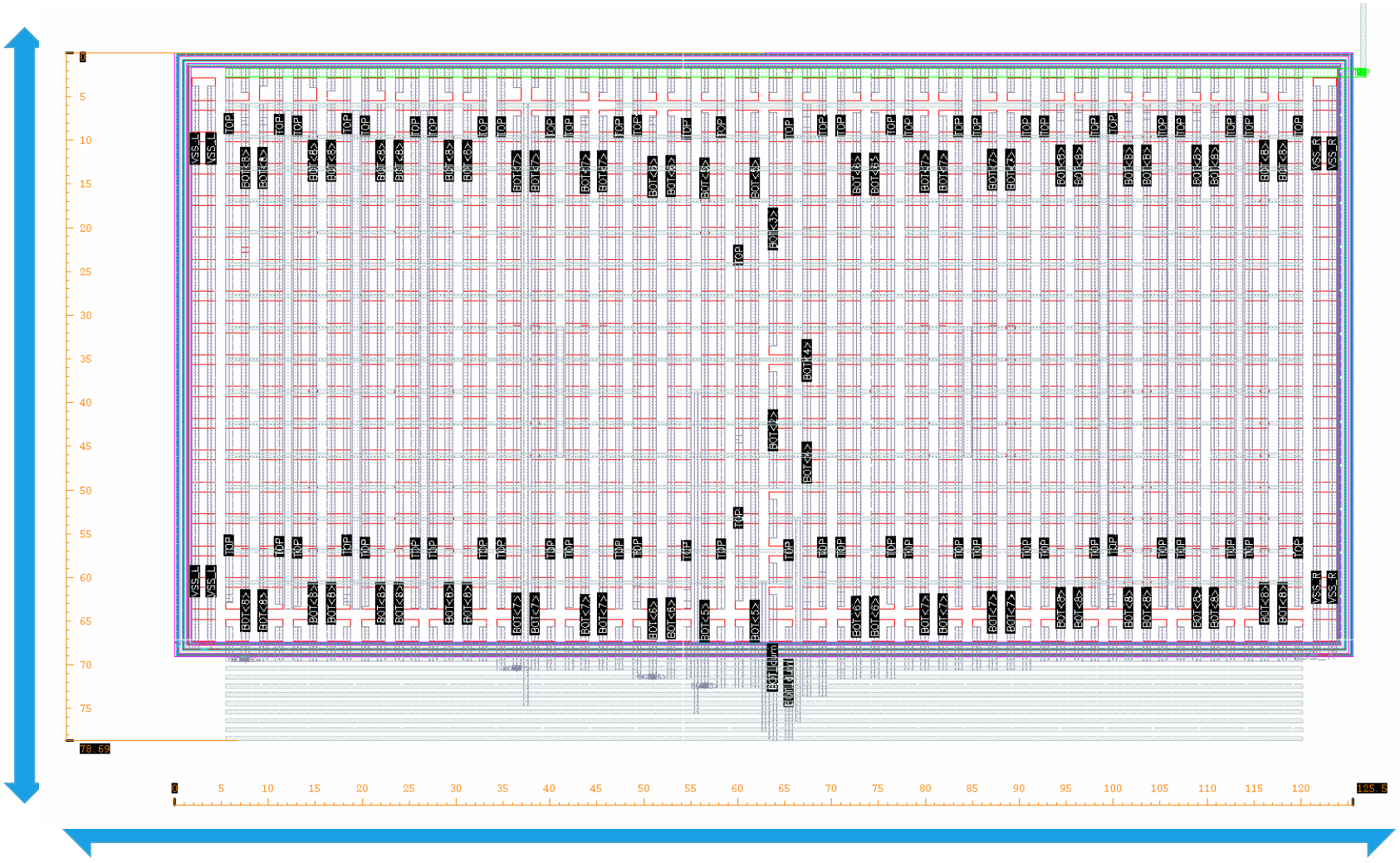


Final singleDAC(cap bank) Floorplan

D_VSS	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_Top	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	3	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	2	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	1	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	1	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	0	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	8	8	8	8	8	8	8	8	7	7	7	7	6	6	5	5	D	4	6	6	7	7	7	7	8	8	8	8	8	8	8	8	D_VSS
D_VSS	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_7	D_7	D_7	D_7	D_6	D_6	D_5	D_5	D	D_4	D_6	D_6	D_7	D_7	D_7	D_7	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_8	D_VSS

Bit	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.4927	10.985	21.970	43.944	87.885	175.77	351.53	703.08	1406.1
Ratio		2	3.9999	8.000	16.000	32.000	63.999	128.00	256.00

Final Layout – single DAC



Improvement:

- Higher metal used for each bits
- Binary routing
- Compensation Capcitor to make perfect 2^n ratio

CDAC RCX Cap Table

Bit TopP	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51874	11.0181	21.9972	44.1238	88.179	176.362	352.691	705.664	1413.44
Ratio		1.9996	3.9859	7.9952	15.9781	31.9569	63.9080	127.866	256.116

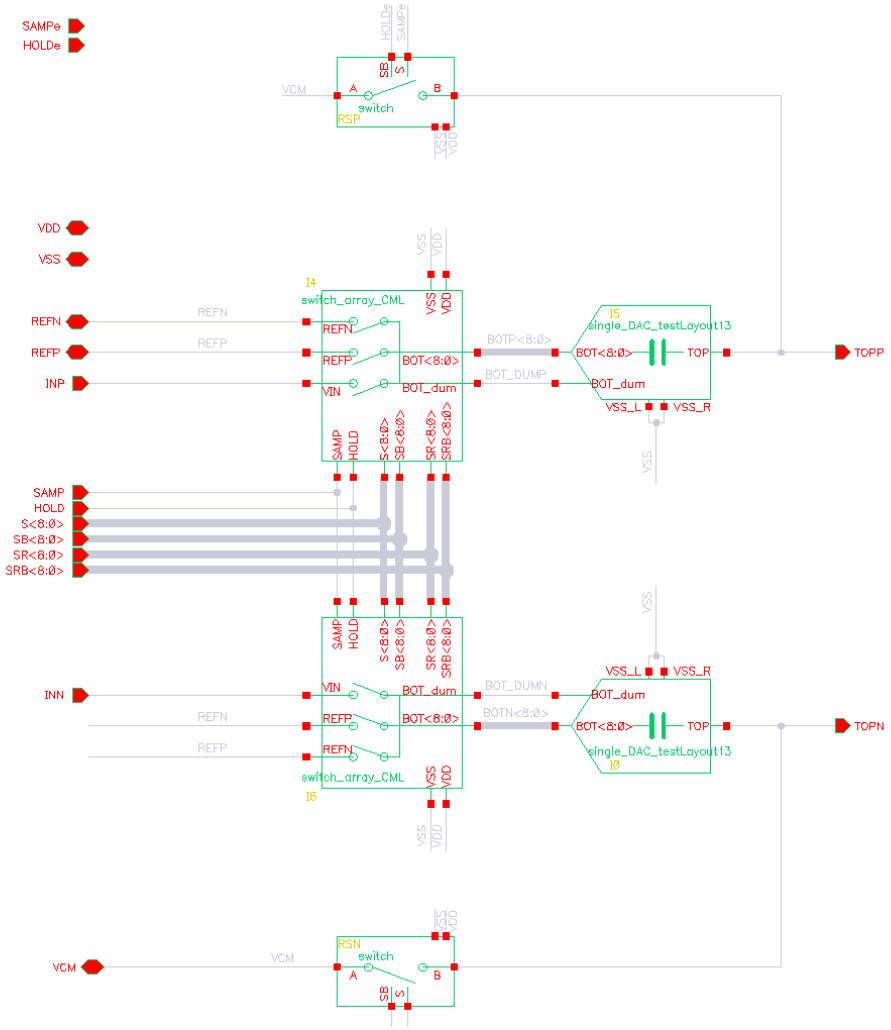
Bit TopN	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51138	11.0222	21.9988	44.1662	88.2156	176.425	352.801	705.712	1413.26
Ratio		1.9998	3.9915	8.0136	16.0060	32.0110	64.0131	128.046	256.425

SAR-Core RCX Cap Table

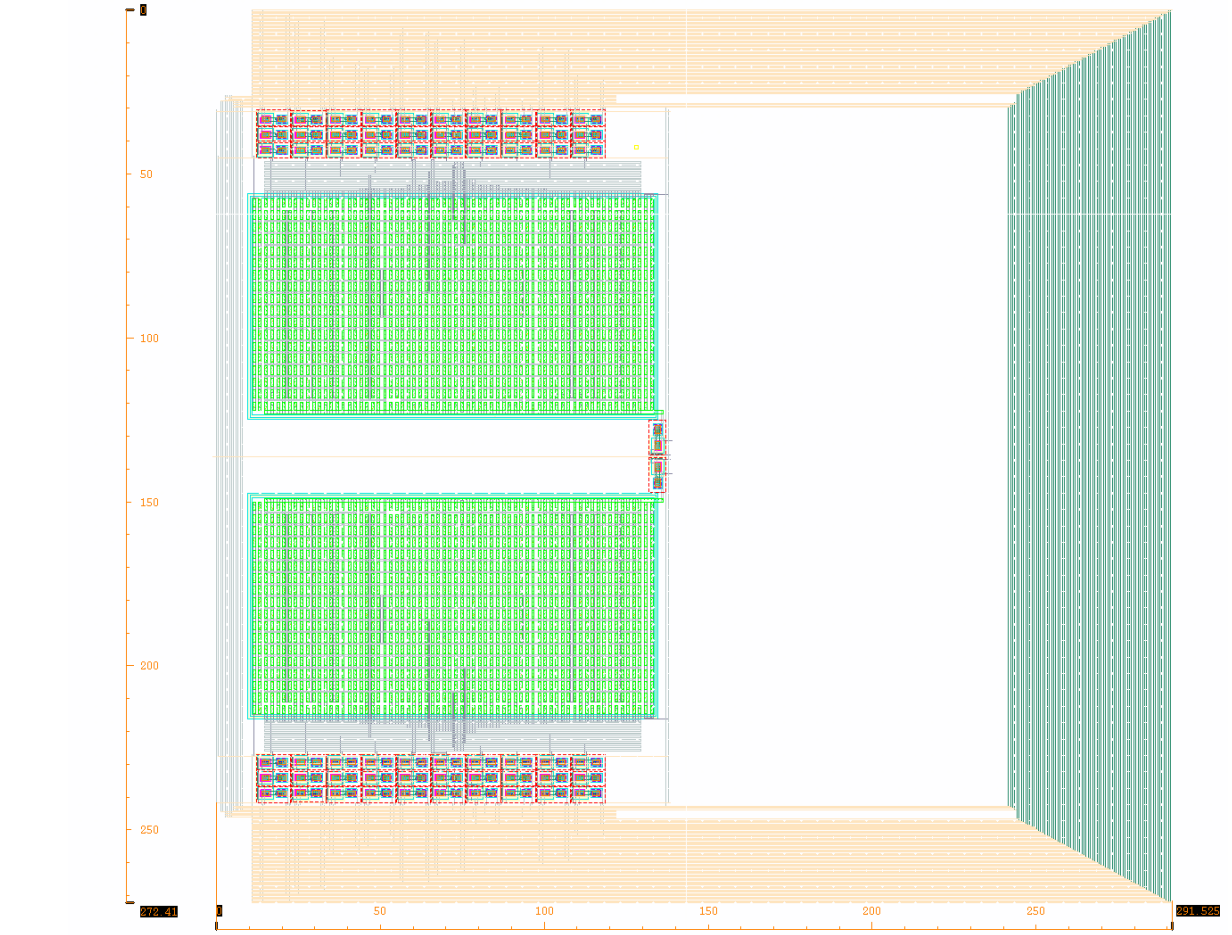
Bit TopP	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51874	11.0182	21.9978	44.0338	88.082	176.21	352.332	705.239	1413.18
Ratio		1.9965	3.9860	7.9789	15.9605	31.9293	63.8428	127.789	256.069

Bit TopN	B0	B1	B2	B3	B4	B5	B6	B7	B8
CC(fF)	5.51137	11.0222	21.9987	44.0749	88.1173	176.271	352.44	705.293	1413.41
Ratio		1.9999	3.9915	7.997	16.0060	31.9831	63.9478	127.970	256.453

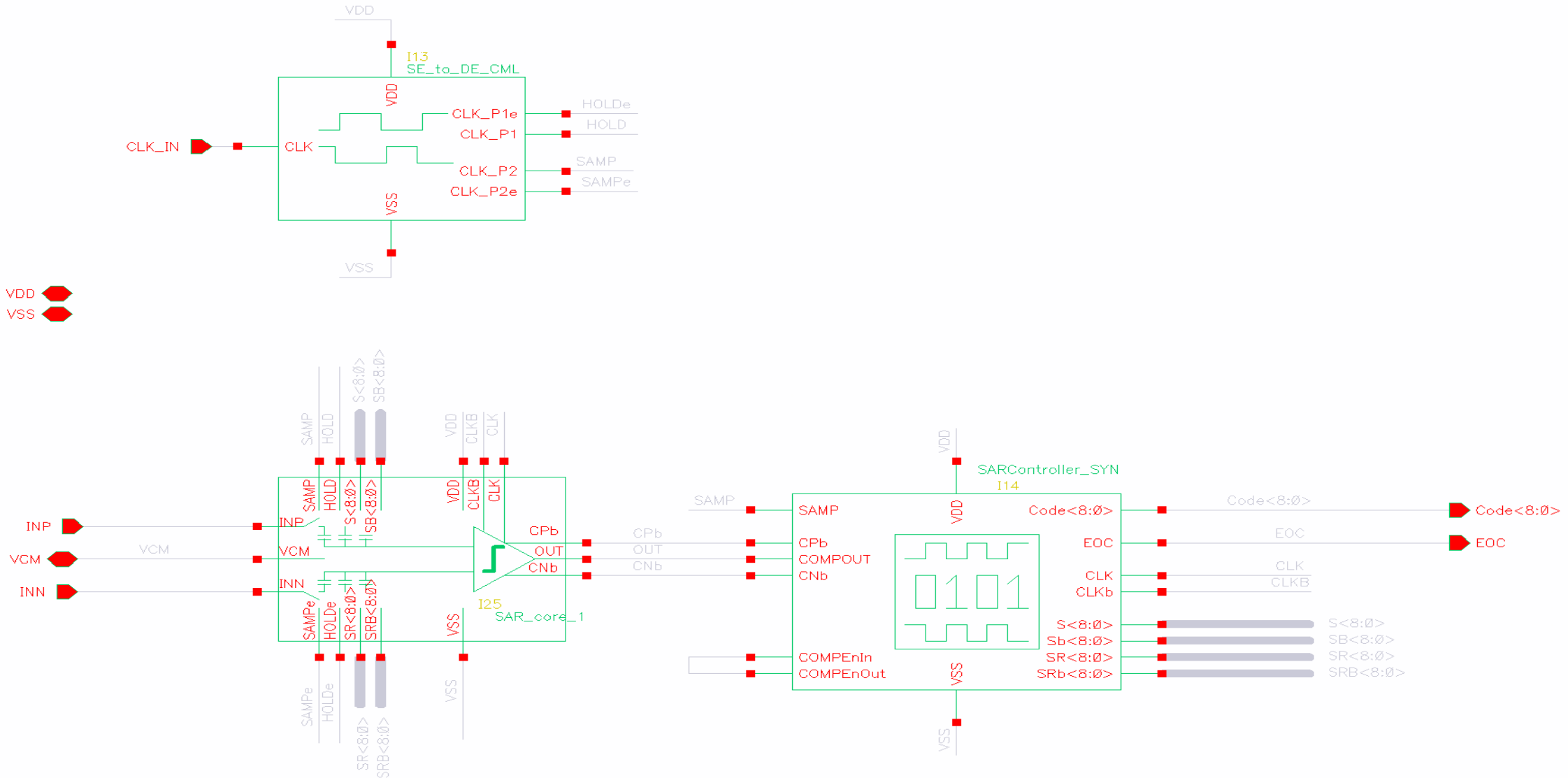
Schematic – CDAC



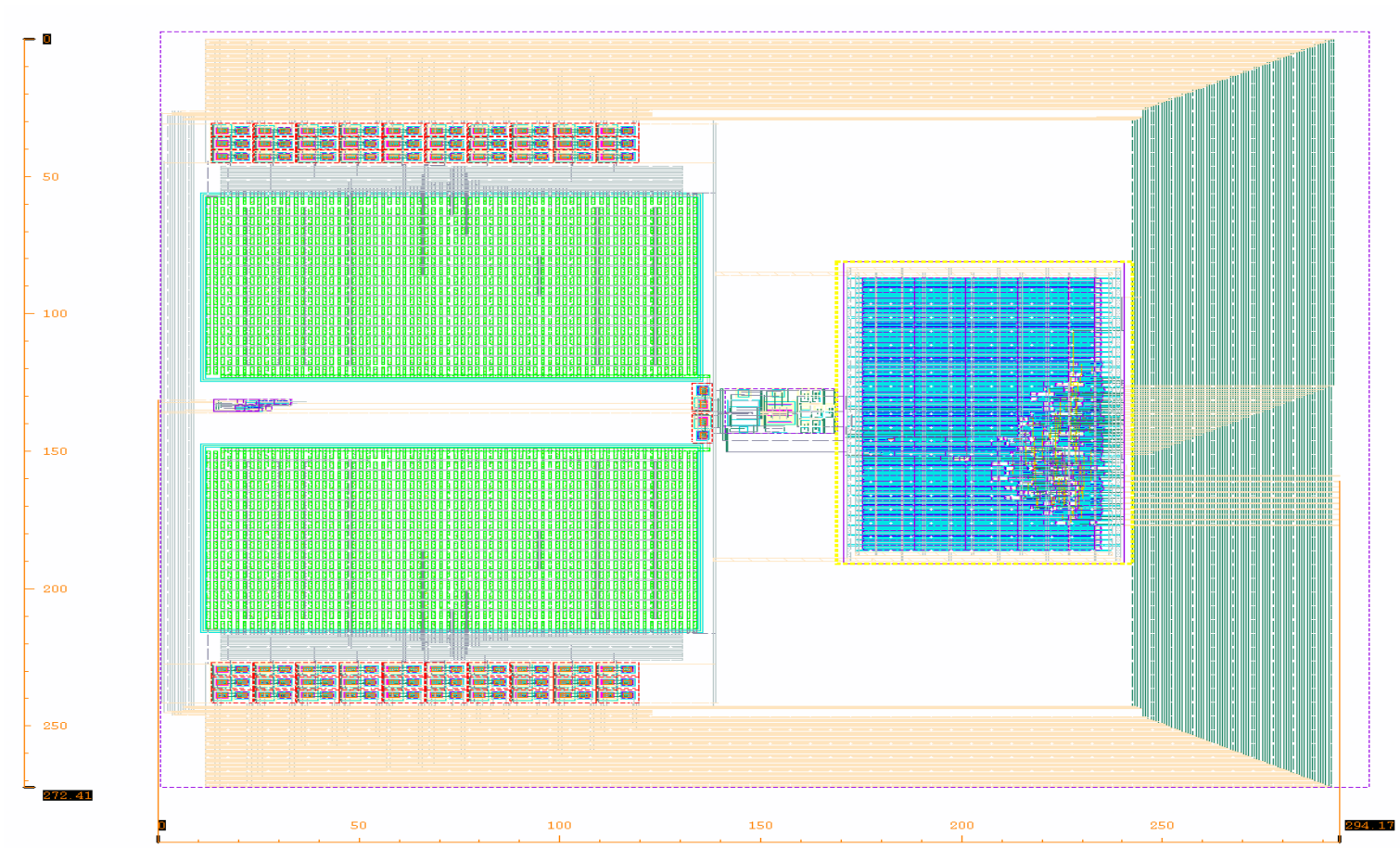
Final Layout – CDAC



Schematic – SAR ADC



Final Layout – SAR-ADC



Simulation Result – SAR_ADC

Outputs

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	DOUT		☑	☑	yes
2	sample(v("/DOUT" ?result...	wave	☑	☑	
3	db20(dft(sample(v("/DOU...	wave	☑	☑	
4	spectrum_snr	51.91	☑	☑	
5	INP		☑	☑	yes
6	INN		☐	☐	no
7	I0/I25/CINP		☐	☐	no
8	I0/I25/CINN		☐	☐	no
9	I0/CLK		☐	☐	no
10	I0/SAMP		☐	☐	no
11	I0/HOLD		☐	☐	no
12	I0/OUT		☐	☐	no
13	I0/S<8:0>		☐	☐	no
14	I0/I25/DAC/BOTP<8:0>		☐	☐	no