# SE-DE Test Setup

1. Power Supply
   1. 1 channel is used as 5V, 0.2A
   2. 1 channel is used as -5V, 0.2A
   3. 1 channel is used as 2.5V, 0.2A
2. Function Generator
   1. SIN Input - Channel 1
      1. High-Z Load
      2. 1Vpp
      3. 0 V offset
      4. Frequency at 1KHz as initial
   2. Clock Input – Channel2
      1. High-Z Load
      2. 2.5 Vpp
      3. 1.25 Offset
      4. Frequency at 1MHz
      5. Duty Cycle 50%
   3. **Sync Both Channels every time the parameters are changed**
3. Oscilloscope
   1. Time Base 1ms/div
   2. Digital Bus1
      1. Digital Code 0-8 (C0-8)
      2. Digital Code 11 - End of Code (EOC)
      3. Trigger Level 1.8V
      4. Turns off Others
   3. Trigger Source
      1. EOC, D11 Rising Edge
      2. **Possibly CLK from Function Generator OR CLK from buffer**
   4. Collect data
      1. Stop or Single
      2. MSB First
      3. ASCII format
      4. Maximum Points

# Bypass Setup

1. Power Supply
   1. 1 channel is used as 5V, 0.2A
   2. 1 channel is used as -5V, 0.2A
   3. 1 channel is used as 2.5V, 0.2A
2. Function Generator
   1. SIN Input - Channel 1
      1. High-Z Load
      2. 1Vpp
      3. 0 V offset
      4. Frequency at 1KHz as initial
   2. SIN Input Inverted - Channel 2
      1. Polarity Inverted
      2. High-Z Load
      3. 1Vpp
      4. 0 V offset
      5. Frequency at 1KHz as initial
   3. Sync Both Channels every time the parameters are changed
3. Oscilloscope
   1. WaveGen used as CLK
      1. Load – Infinity
      2. Frequency – 1M
      3. Amplitude 2.5V
      4. Offset – 1.25V
      5. Duty Cycle 50%
   2. Time Base 1ms/div
   3. Digital Bus1
      1. Digital Code 0-8 (C0-8)
      2. Digital Code 11 - End of Code (EOC)
      3. Trigger Level 1.8V
      4. Turns off Others
   4. Trigger Source
      1. EOC, D11 Rising Edge
      2. Possibly CLK from Function Generator OR CLK from buffer
   5. Collect data
      1. Stop or Single
      2. MSB First
      3. ASCII format
      4. Maximum Points