Digital Integrated Circuits
Homework #2

Due 2 hours before the next lecture

Problem 1: Equivalent Resistance

Consider NMOS device with W = 240nm and L = 100nm (effective L = 70nm). Using the resistor averaging technique discussed in class, and parameters below, calculate R_{on} as V_{DD} changes from 0.4V to 1V in steps of 0.2V. Compare the results of your hand calculations with simulation results in Table 2.

Use following parameters for hand calculations:

$\lambda = 0.795\ V^{-1}$
$k' = 129.5\ \mu A/V^2$
$L_{eff} = 70$ nm
$V_{th} = 0.168$ V
$V_{dsatn} = 0.3$ V

Table 2: R_{on} (Analytical vs. Simulation)

R_{on}	I_{DSAT} (µA)	Analytical Model (R_{eq})	Simulation 2-point avg
$V_{DD} = 0.4V$			27.8 kΩ
$V_{DD} = 0.6V$			9.0 kΩ
$V_{DD} = 0.8V$			6.5 kΩ
$V_{DD} = 1.0V$			5.0 kΩ

Problem 2: Inverter in Subthreshold

The inverter below, operates with $V_{DD} = 0.175V$ and is composed of $V_{Tn} = |V_{Tp}| = 0.20V$ devices. They can be described by the subthreshold voltage-current relation. The devices have identical I_S and n, (n=1.5 and kT/q=26mV).

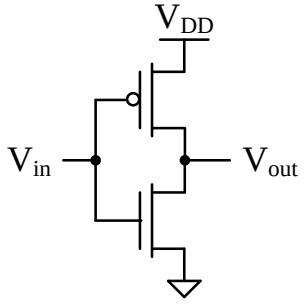


Figure 2: Inverter in Subthreshold.

2A Calculate the **switching threshold (V_M)** of this inverter.

If the equation is difficult to solve, plot both sides and find the intersection point for a numerical answer.

2B Calculate **V_{IL}** and **V_{IH}** of the inverter.

You may find piecewise-linear approximation helpful.

<u>Problem 3:</u> MOS Capacitance

Use the following table.

Assumptions:

$|V_{TH}| = 0.2V$ for both NMOS and PMOS

For the purpose of capacitance calculation (only), treat velocity saturation as saturation

Param.	**C_{ox} [fF/μm^2]**	**C_o [fF/μm]**
NMOS	15	0.27
PMOS	14	0.25

3A What is the t_{ox} (nm) of the NMOS transistor?

3B Consider a PMOS biased with $V_G = V_D = V_S = V_B = 0V$
Assume W = 480 nm, L = 120nm, $L_D = L_S = 240nm$
Calculate the following capacitances:

(B1) Gate-to-Channel capacitance (C_{GC})

(B2) Gate-to-Source capacitance (C_{GS})

3C Consider an NMOS biased with $V_G = V_D = 0.8V$, $V_S = V_B = 0V$
Assume W = 240 nm, L = 120nm, $L_D = L_S = 240nm$
Calculate the following capacitances:

(C1) Gate-to-Channel capacitance (C_{GC})

(C2) Gate-to-Source capacitance (C_{GS})

Clearly indicate your final formulas and circle/highlight your answers.

Problem 4: Computing Capacitance

Consider the circuit in Figure 4. Calculate the total equivalent capacitance on node X as it charges from 0 to $V_{DD}/2$.

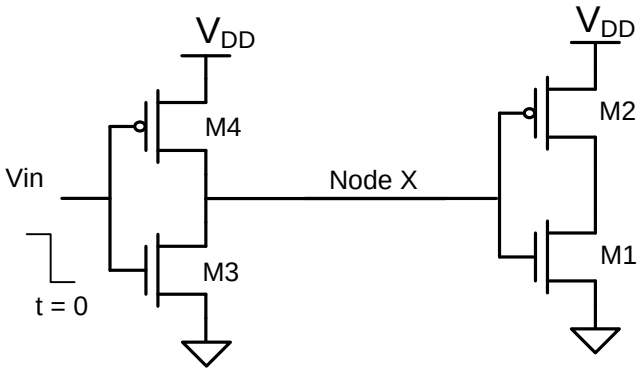


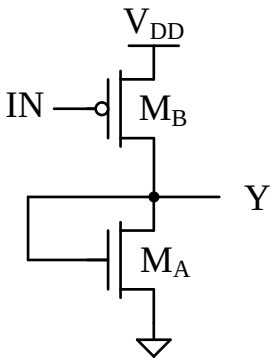
Figure 4

You can use the following capacitance values in your calculations:

C_{db_NMOS} = 0.06 fF, C_{db_PMOS} = 0.10 fF
C_{gd_NMOS} = 0.14 fF, C_{gd_PMOS} = 0.26 fF
C_{g1} = 0.16 fF, C_{g2} = 0.30 fF

Problem 5: VTC

Consider the inverter below, with the input at the gate of the PMOS and a diode-connected NMOS.



Device parameters:

V_{TN} = 0.2 V, V_{TP} = −0.2 V
V_{DSATN} = $|V_{DSATP}|$ = 0.3 V
k'_n = 130 μA/V^2
k'_p = −100 μA/V^2
$(W/L)_A$ = 1
$(W/L)_B$ = 4
λ = 0, γ = 0 for both transistors
V_{DD} = 1 V

(a) Calculate V_Y for V_{IN} = 0 V.

V_Y =

(b) Calculate V_Y for V_{IN} = V_{DD}.

V_Y =

(c) Ignoring the results from (a) and (b), calculate switching threshold V_M for the inverter. Is V_M expected to be greater or smaller than 0.5V? (circle the correct answer)

V_M > 0.5 V **V_M > 0.5 V**

Briefly explain why:

What are the modes of operation for M_A and M_B?

M_A :	**M_B :**

Calculate the value of V_M.

V_M =