Digital Integrated Circuits
Homework #4

Due 2 hours before the next lecture

Problem 1: Gate Sizing of a Multi-Stage Network

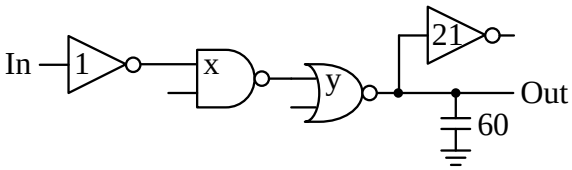

Figure 1

Consider the multi-stage logic shown in Figure 1. The numbers represent relative input gate capacitance. For example, the inverter with "1" has input capacitance of C_{in}, the inverter with "21" has input capacitance of $21C_{in}$ because it is 21 times as wide. Output is loaded with 60 C_{in}.

1A Find the minimum delay from input to output using logical effort.

1B Find the size of the NAND and NOR gates x and y (NAND has input capacitance xC_{in} and NOR has input capacitance yC_{in}) that minimize the delay from input to output.

Problem 2: CMOS Logic & Logical Effort

(a) Design $F = \overline{A + BC + D}$ in Static CMOS. Draw the schematic and size all the transistors such that the worst-case resistance is equal to that of a unit-sized inverter (W_P:W_N = 2:1).

(draw your initial circuit below)

(revise you circuit as to minimize delay when inputs transition in the following order: A, C, D, B)

Parasitic delay, ***p*** =

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(b) Find the logical effort for all the inputs in your design in part (a)?

g_A =
g_B =
g_C =
g_D =

Problem 3: Sizing for Performance and Energy

Assume the inverters are implemented in standard CMOS and have symmetrical VTC. Assume $C_{intrinsic} = C_{gate}$ ($\gamma = 1$). Equivalent resistance and input capacitance of the unit-sized ($S = 1$) inverter are R and C, respectively. Sizing factor $S \geq 1$. t_{p0} is the parasitic delay of a unit inverter.

a. Pick the best sizing factors S_2 and S_3 to minimize propagation delay from *In* to *Out*. What is the minimum delay (in terms of t_{p0})?

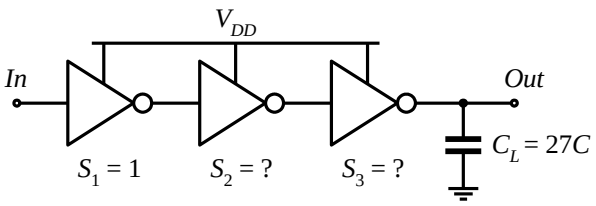

Fig. 3a

S_2 =	**S_3 =**
t_p =	

b. Pick the best sizing S_2 and S_3 to minimize energy consumption. You may assume square wave input with period T. What is the total energy taken from V_{DD} (ignore energy for driving the input *In*) for a full cycle ($0 \rightarrow 1$, $1 \rightarrow 0$)?

S_2 =	**S_3 =**
E_{cycle} =	

c. For inverters in Fig. 3c, pick the best sizing factors S_2 and S_3 to minimize propagation delay. What is the minimum delay (in terms of t_{p0})?

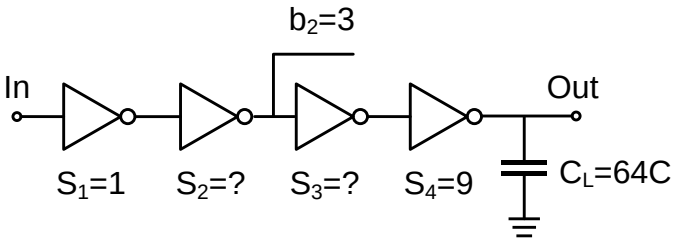

Fig. 3c

S_2 =
S_3 =
t_p =