Personal Reflection

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In this workshop, I started with learning delay model, power model, CMOS logic, Pass transistor logic, sizing of logic gates, logical effort, buffer chain, multi-stage logic networks and all kinds of adders. Among of these materials, calculating logic effort, parasitic effort and delay of circuit network are my favorite topic.

In these topics, logic effort and parasitic effort are something that I didn't learn from my school. And these two terms are used to estimate and calculate delay in a CMOS circuit. And it can help us in selection of gates for a given function and sizing gates to achieve minimum delay. One interesting topic, included in these topics, is sizing optimization, which used to reduce energy consumption in the design. And one important rule about sizing I learned from the lecture and office hours: doubled the size of transistor if they were in series and stayed the same if they were in parallel. This rule helps me a lot when I was working on my weekly homework.

In addition, the final project is where I learned most about the digital circuit design. Starting from the basic design of circuit topology, I began to learn how to simplify some digital logic in the circuit. For example, half adder in 2's complement converter circuit, it is not necessary to implement a complete half adder, instead it be implemented as some simplify digital logic by realizing the result of XOR with input 1 as an inverter Beyond that, the key point of this design is that Vdd optimization and sizing optimization. Energy minimization is also the topic I never get a chance learned from my school. Taking either one of them is not enough to minimize energy consumption of circuit network. Energy consumption is minimized when both methods are applied in the design. In our design, energy is reduced to 56.5% of original energy consumption. Among these two methods, Vdd optimization contribute more impact than sizing impact. Because, when only Vdd optimization is applied in the design, energy consumption is reduced 40% of original energy consumption.

At the end, it is a great experience of learning digital circuit design from the practical sides, like designing a real circuit and analyzing energy consumption of design. Furthermore, this workshop provides me a great opportunity to learn CMOS logic and PTL logic deeper than what I know from my semiconduction course. Overall, the workshop leads me into a new world of digital circuit design and makes me feel more like a real-world circuit designer.