Q1

Problem 1: Gate Sizing of a Multi-Stage Network

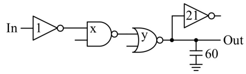


Figure 1

Consider the multi-stage logic shown in Figure 1. The numbers represent relative input gate capacitance. For example, the inverter with "1" has input capacitance of C_{in}, the inverter with "21" has input capacitance of $21C_{in}$ because it is 21 times as wide. Output is loaded with 60 C_{in}.

1A Find the minimum delay from input to output using logical effort.

1B Find the size of the NAND and NOR gates x and y (NAND has input capacitance xC_{in} and NOR has input capacitance yC_{in}) that minimize the delay from input to output.

$g_{inv} = 1$ $\qquad h_1 \ \frac{x}{1}$

$g_{NAND} = \frac{4}{3}$ $\qquad h_2 \ \frac{y}{x}$

$g_{NOR} = \frac{5}{3}$ $\qquad h_3 \ \frac{60}{y}$

$P_{inv} = 1$

$P_{NAND} = 2$ $\qquad P_{NOR} = 2$

1A $\quad f = (GBH)^{\frac{1}{3}}$ $\qquad b = \frac{60+21}{60} = B = 1.35$

$$= \left(1 \cdot \frac{4}{3} \cdot \frac{5}{3} \cdot 1.35 \cdot \frac{60}{1}\right)^{\frac{1}{3}} = (63.572)^{\frac{1}{3}} = 3.99$$

Minimum Delay: $D_{min} = N \cdot f + P = \sum(g_i h_i + p_i)$

$$= 3 \cdot 3.99 + (1+2+2) = 16.97$$

1B:

y: NOR: $\frac{5}{3} \cdot \frac{60}{3.99} = 25.06 \ C_{in}$

x: NAND: $\frac{4}{3} \cdot \frac{25.06}{3.99} = 8.37 \ C_{in}$

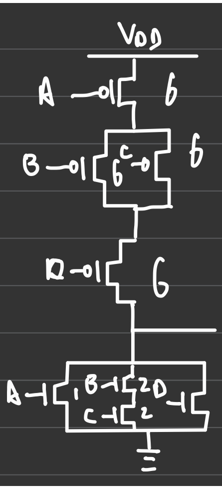
Problem 2: CMOS Logic & Logical Effort

$W_p : W_n = 2:1$

(a) Design $F = \overline{A + BC + D}$ in Static CMOS. Draw the schematic and size all the transistors such that the worst-case resistance is equal to that of a unit-sized inverter (W_P:W_N = 2:1).

(draw your initial circuit below)

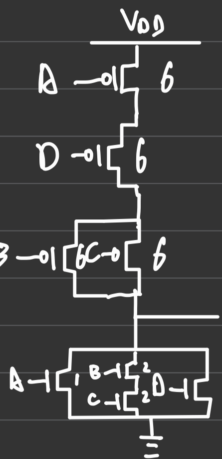
(revise you circuit as to minimize delay when inputs transition in the following order: A, C, D, B)



$$P = \frac{6 + (1+2+1)}{3} = \frac{10}{3}$$

$F = \overline{A+BC+D}$

$\Rightarrow$



$$P = \frac{6+6+(1+2+1)}{3} = \frac{16}{3}$$

$F = \overline{A+BC+D}$

(b) Find the logical effort for all the inputs in your design in part (a)?

g_A =
g_B =
g_C =
g_D =

$g_A = \frac{7}{3}$

$g_B = \frac{8}{3}$

$g_C = \frac{8}{3}$

$g_d = \frac{7}{3}$

Problem 3: Sizing for Performance and Energy

Q3

a. Pick the best sizing factors S_2 and S_3 to minimize propagation delay from *In* to *Out*. What is the minimum delay (in terms of t_{p0})?

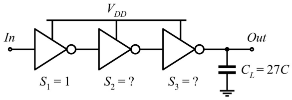


Fig. 3a

$S_2 = 9$	$S_3 = 27$
$t_p = 12t_{p0}$	

$$F = \frac{C_L}{C_{in}} = 27$$

$$f^* = (27)^{\frac{1}{3}} = 3$$

$$\boxed{\begin{aligned} S_2 &= 3^2 = 9 \\ S_3 &= 3^3 = 27 \end{aligned}}$$

$$t_p = N t_{p0} \left(1 + \sqrt[N]{F}/\gamma\right) = 3 \cdot t_{p0}(1+3) = \boxed{12 t_{p0}}$$

b. Pick the best sizing S_2 and S_3 to minimize energy consumption. You may assume square wave input with period T. What is the total energy taken from V_{DD} (ignore energy for driving the input *In*) for a full cycle (0→1, 1→0)?

$S_2 = 1$	$S_3 = 1$
$E_{cycle} = 32CV_{DD}^2$	

when they are all 1, i.e. $S_2 = S_3 = 1$

$$C_{tot} = C_{int,s1} + C_{gate\,s2} + C_{int,s2} + C_{gate,s3} + C_{int,s3} + C_L$$
$$= 1 + 1 + 1 + 1 + 1 + 27$$
$$= 32\,C$$

$$E_{cycle} = \boxed{32C\,V_{DD}^2}$$

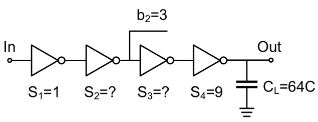


Fig. 3c

$S_2 =$ 2.8379
$S_3 =$ 5.0538
$t_p =$ 17.51tpo

$$\frac{1}{s_2}(s_3+3)$$

$$9 s_3^{-1}$$

$$(s_3+3)\, s_2^{-1}$$

$$-(s_3+3)\, s_2^{-2}$$

$$t_p = (1+s_2) + \left(1+\frac{s_3+3}{s_2}\right) + \left(1+\frac{9}{s_3}\right) + \left(1+\frac{64}{9}\right)$$

Taking partial derivative with respect to s_2 and s_3

s_2: $\quad 1 - \dfrac{s_3+3}{s_2^2} \Rightarrow 1 = \dfrac{s_3+3}{s_2^2} \qquad \left(\dfrac{s_3^2}{9}\right)^2 = s_3+3$

s_3: $\quad \dfrac{1}{s_2} - \dfrac{9}{s_3^2} \Rightarrow \dfrac{1}{s_2} = \dfrac{9}{s_3^2} \qquad 9s_2 = s_3^2 \qquad s_2 = \dfrac{s_3^2}{9}$

$$\boxed{s_3 \approx 5.0538 \qquad s_2 = 2.8379}$$

$$t_p = \left[(1+2.8379) + \left(1+\frac{5.0538}{2.8379}\right) + \left(1+\frac{9}{5.0538}\right) + \left(1+\frac{64}{9}\right)\right] t_{po}$$

$$= 17.51\, t_{po}$$