

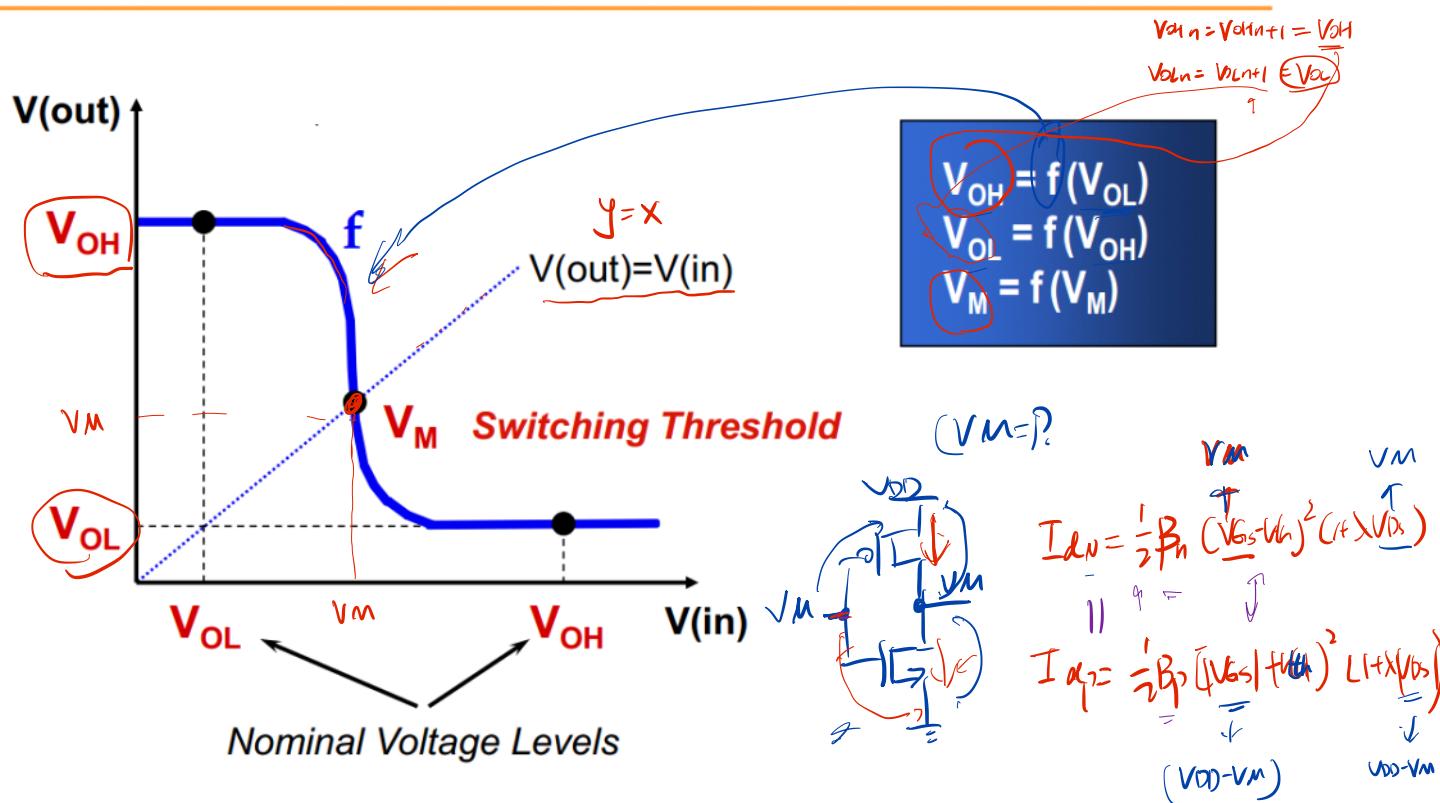
GEC Workshop | 2022  
**Discussion 2**

# Digital Integrated Circuits

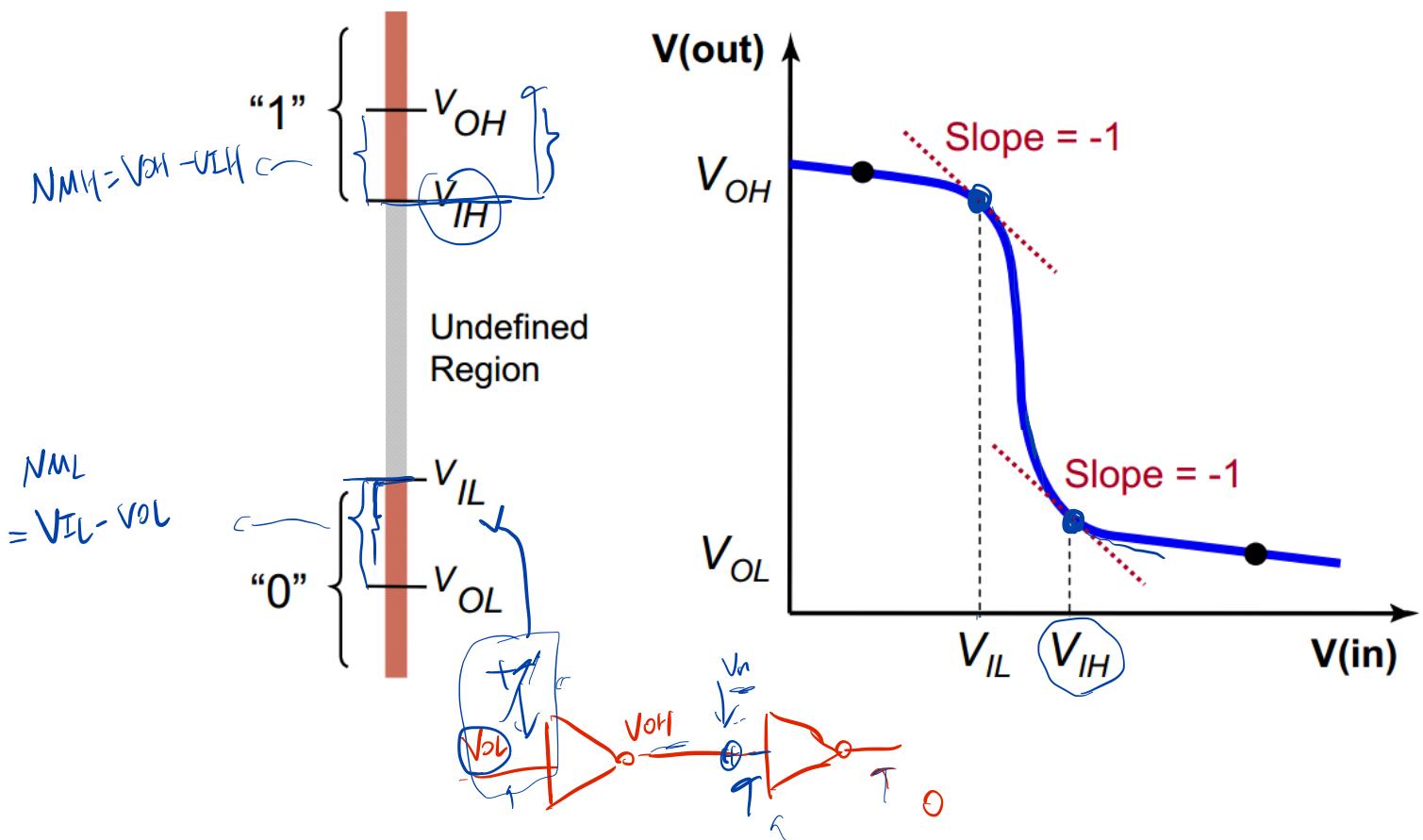


**Mentor: Sida (Star) Li**  
*UCLA Electrical & Computer Eng.*

# DC Operation: Voltage Transfer Characteristic



## Mapping Between Analog and Digital Signals



## Computing Equivalent Resistance (2/2)

### ◆ Method 2: simple averaging

- The averaging works because of approximately linear dependence of  $I_{DS}$  on  $V_{DS}$  (recall the CLM model)

$$R_{on} = \frac{1}{2} \left( \underbrace{\frac{V_{DD}}{I_{DSAT} \cdot (1 + \lambda V_{DD})}}_{R_0} + \underbrace{\frac{V_{DD}/2}{I_{DSAT} \cdot (1 + \lambda V_{DD}/2)}}_{R_{mid}} \right)$$

$k' \frac{W}{L} \left[ (V_{DD} - V_T) V_{DSAT} - \frac{V_{DSAT}^2}{2} \right]$   
 $\uparrow$   
 $V_{GS}$

fixed L  
 $\Rightarrow R_{on} \sim \frac{1}{W}$

$$R_{on} \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)$$

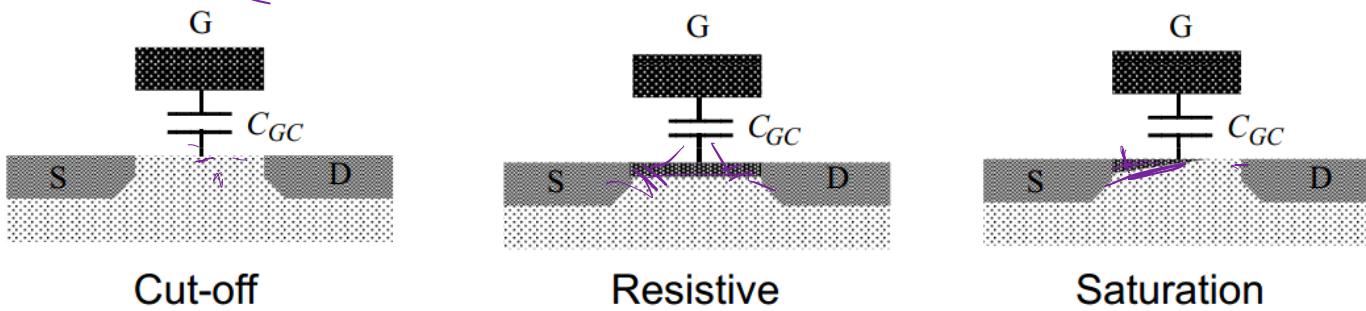
**Use this formula for hand analysis**

Zo



$$R_{on} = k \cdot \frac{L}{W}$$

# **Summary: #1: Gate-Channel Capacitance**



Operation Region	$C_{GCB}$	$C_{GCS}$	$C_{GCD}$
<b>Cutoff</b>	$C_{ox}WL_{eff}$	0	0
<b>Triode</b>	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
<b>Saturation</b>	0	$(2/3)C_{ox}WL_{eff}$	0

*Textbook: page 109*

$$\text{Off/Lin} \rightarrow C_{\text{gate}} = C_{\text{ox}} \cdot \underline{W} \cdot L_{\text{eff}}$$

$$\text{Sat} \rightarrow C_{\text{gate}} = (2/3) \cdot C_{\text{ox}} \cdot W$$

$$L_d = 120\text{nm}$$

$$2C_d = 15 \text{ nm}$$

$$\rightarrow L_{eff} = 0.09 \mu$$

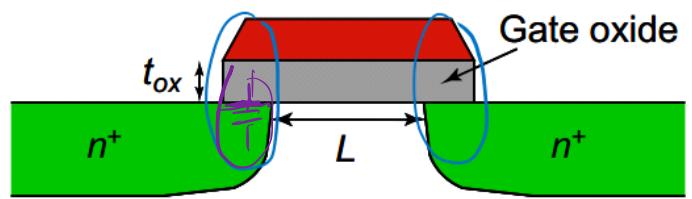
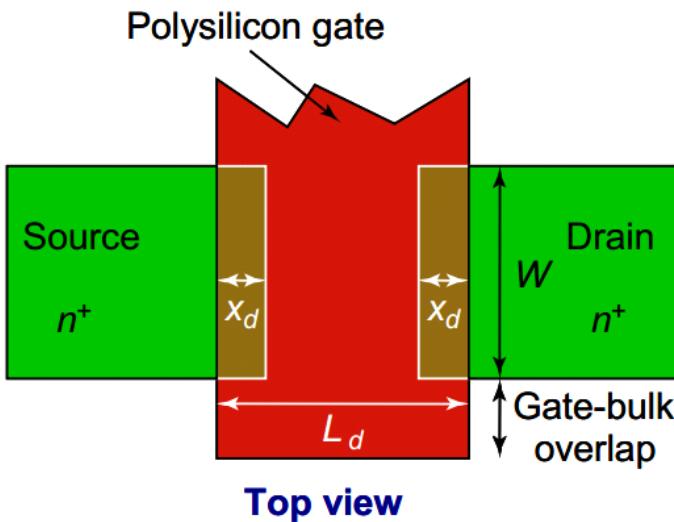
$$- \text{eff} \quad \omega = 0.24 \mu\text{m}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \approx 15 \frac{fF}{\mu m}$$

## Digital ICs

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## #2: Gate Overlap Capacitance



Cross section

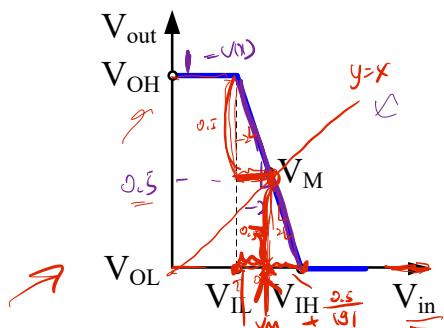
$$C_o = \underbrace{C_{ox} \cdot x_d}_{0.225} \cdot \frac{15}{0.015}$$

$$\text{Off/Lin/Sat} \rightarrow C_{GSO} = C_{GDO} = C_o \cdot \cancel{W} \xrightarrow[0.2\mu]{e.g.} 0.05 \text{ fF}$$

$$C_g = C_{Gc} + C_o = 0.2 \text{ fF} \xrightarrow[\text{(prev. slide)}]{S+D \text{ overlap}} + 0.05 \times 2 = \underline{\underline{0.3 \text{ fF}}}$$

$$\overbrace{C_{GS}}^q = \overbrace{C_{GCS}}^{\uparrow} + \overbrace{C_{GSO}}$$

## Practice Problem1 -- VTC



This figure shows the voltage transfer characteristic (VTC) of a standard CMOS inverter. Note that VTC is approximated with a straight line between  $V_{in} = V_{IL}$  and  $V_{in} = V_{IH}$ .

Parameters:

$$V_{DD} = 1 \text{ V}, V_{OH} = 1 \text{ V}, V_{OL} = 0 \text{ V}, V_M = 0.5 \text{ V}.$$

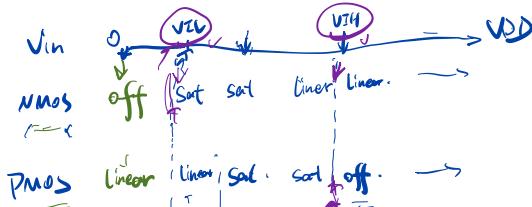
- (a) Determine  $V_{IL}$  and  $V_{IH}$  given that the gain around the  $V_M$  point is  $g = -2$ .

$$V_M = f(V_M) = 0.5 \text{ V}$$

$$V_{IH} = V_M + \frac{V_M - V_{OL}}{|g|} = 0.5 + \frac{0.5}{2} = 0.75 \text{ V}$$

$$V_{IL} = V_M - \frac{V_{OH} - V_M}{|g|} = 0.5 - \frac{1 - 0.5}{2} = 0.25 \text{ V}$$

- (b) Determine  $V_{TN}$  and  $V_{TP}$  assuming that the NMOS transistor is strictly off for  $V_{GS} < V_{TN}$  and the PMOS transistor is strictly off for  $V_{GS} > V_{TP}$ .



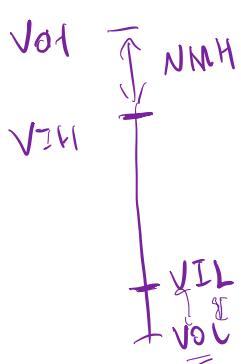
$$V_{IL} = V_{THN} = 0.25 \text{ V}$$

$$|V_{Gp}| = |V_{DD} - V_{IH}| - |V_{Tp}| = 0$$

$$\begin{aligned} |V_{DD} - V_{IH}| &= |V_{Tp}| \\ &= |-0.75| = 0.75 \end{aligned}$$

$$V_{Tp} = -0.75 \text{ V}$$

- (c) Determine the High and Low noise margins of the inverter.

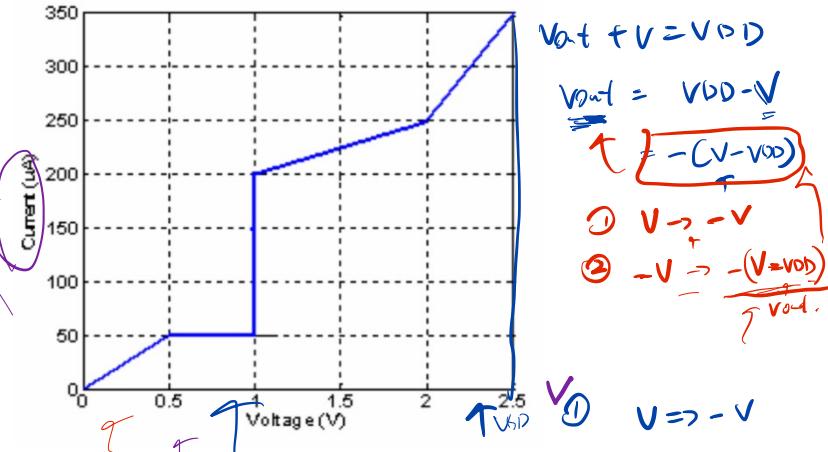
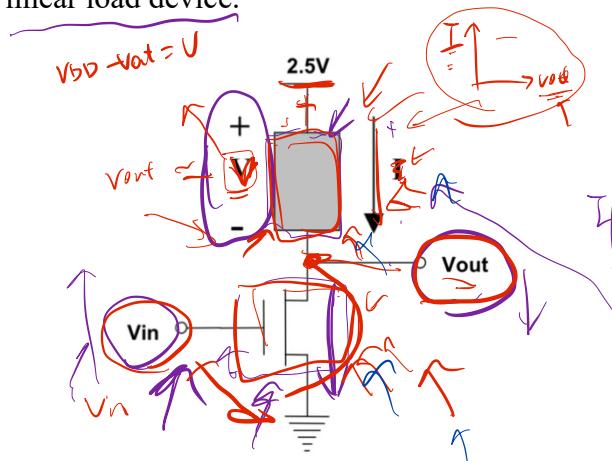


$$V_{OH} - V_{IH} = V_{NMH} = -0.75 = 0.25 \text{ V}$$

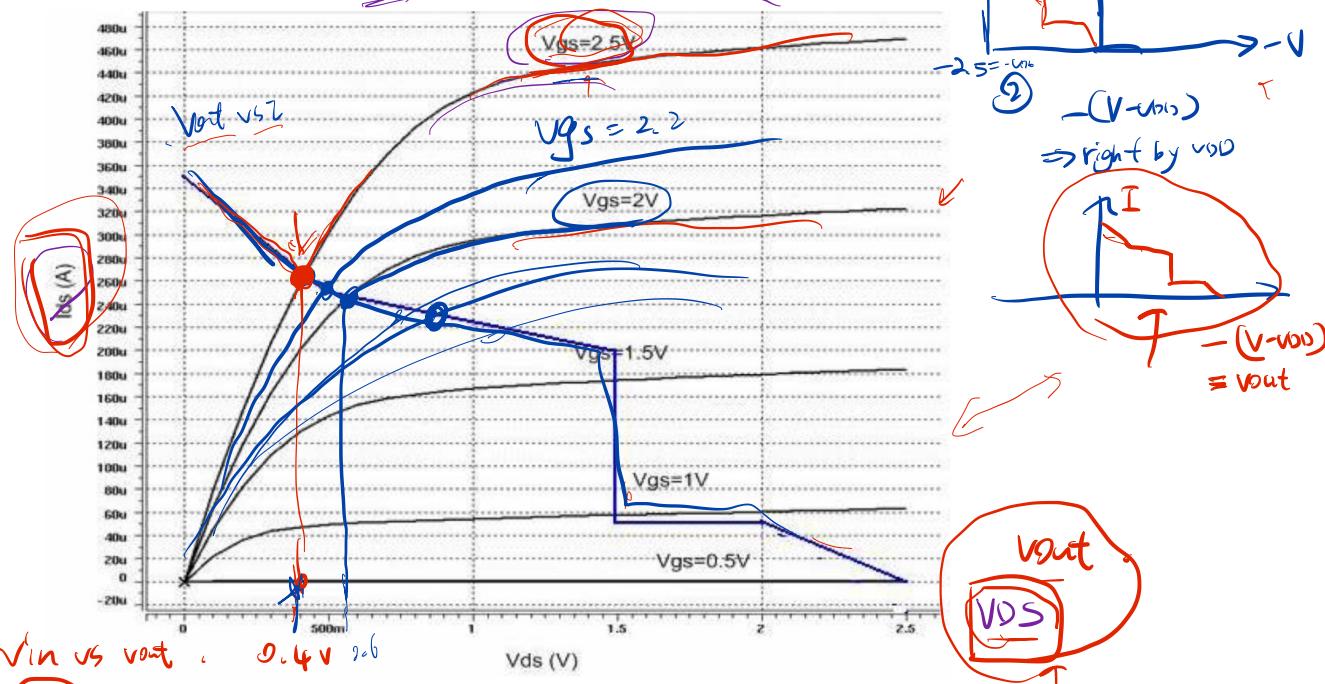
$$V_{IL} - V_{OL} = V_{NML} = 0.25 - 0 = 0.25 \text{ V}$$

## Practice problem2. Find $V_{OH}$ , $V_{OL}$ and $V_M$

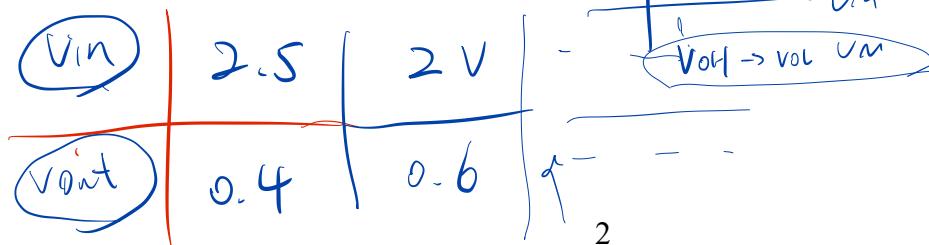
The circuit below features an NMOS transistor that is coupled with a non-linear load device represented by the shared box. Accompanying the figure is the I-V characteristic for this non-linear load device.



Of course, we also have the family of I-V curves of our NMOS transistor given below:



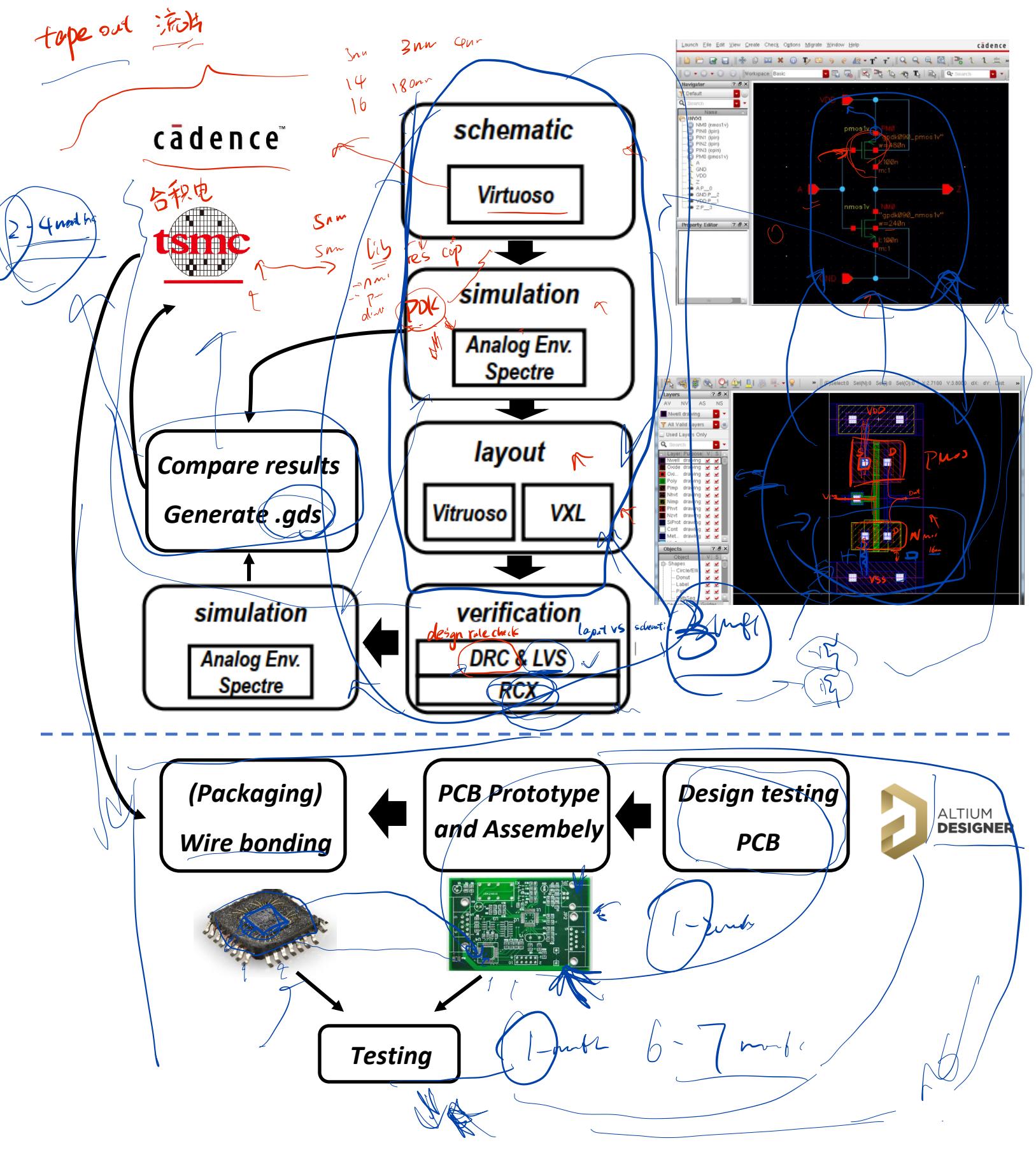
Draw the VTC for this circuit. Determine (or estimate, if necessary, from your VTC) the following parameters:  $V_{OH}$ ,  $V_{OL}$  and  $V_M$ .







# Analog Integrated Circuits Design Flow



# Digital integrated circuit design flow

