# A[53.7] $FO4_{(1V)}$,[183.02] $E_{u(1V)}$ 4-bit Absolute Value Detector

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# Design Summary

- 1a) Circuit topology, 1b) Circuit Style

  -(2 to 1 Mux + Simplified Half Adder + 3bit MSB to LSB Comparator )

  -static CMOS, XOR, AND, and OR

  -Moderate Area, Regular and Intuitive design. Simplified Half Adder uses less logic gates than normal Half Adder

- 2) Sizing + Vdd optimization / Sizing impact
  - Delay increase: [50]% out of 50%
  - Energy reduction : [27.58]% out of 50%
- 3) Sizing + Vdd optimization / $V_{DD}$ impact
  - Delay increase: [50]% out of 50%
  - Energy reduction : [40]% out of 50%
- 4) Sizing + Vdd optimization / *combination* impact
  - Delay increase: [50]% out of 50%
  - Energy reduction : [56.5]%

# Design Preview

- 1. Decide the sign of given input , i.e., compared input bit 3($A_3$) with logic 0.

One input with $A_3$ and another input connects to ground.

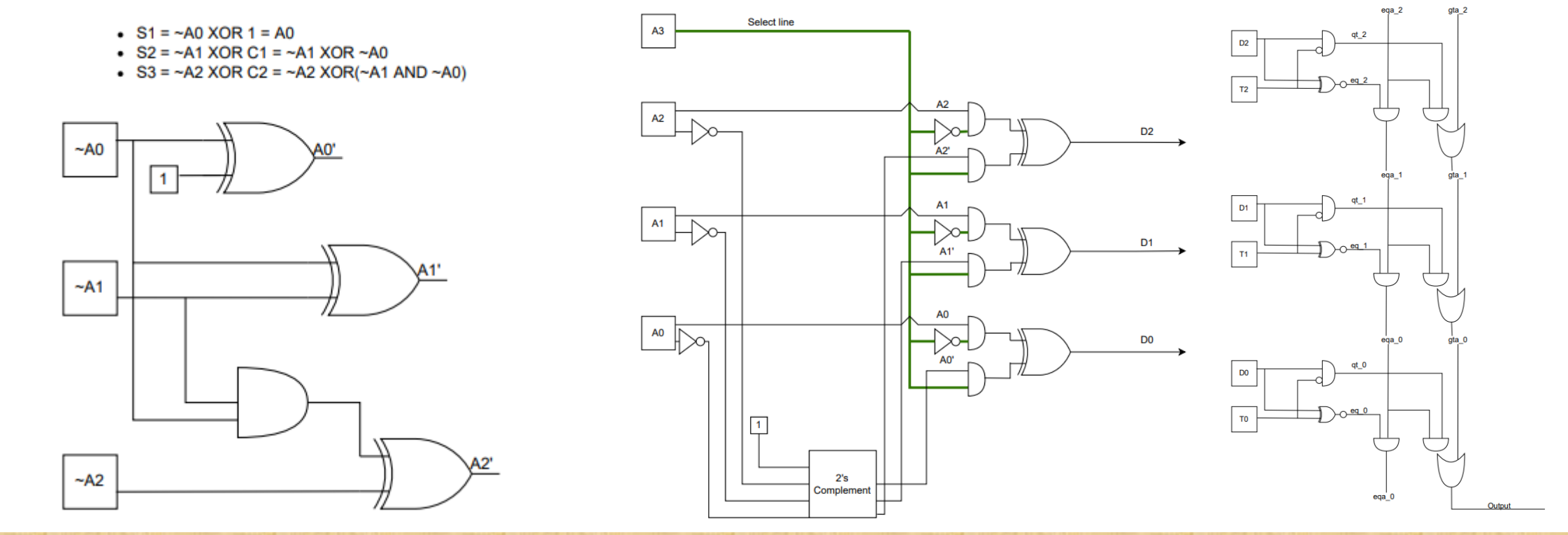
- 2. Building a 3 bit 2's complement circuit, decision done by the step 1.

Output 3-bit magnitude

- 3. Output from step 2 and compared it with given threshold value(3-bit comparator).

# Design Topology & Reasoning

- Schematic

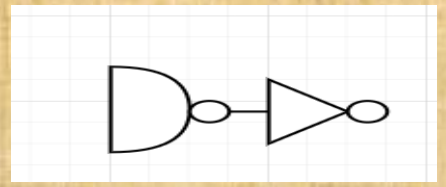



- Simplified Half Adder

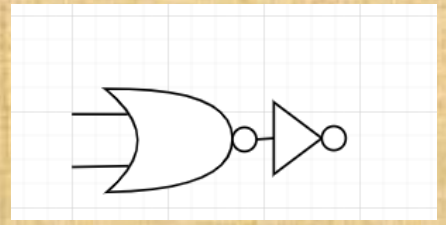
2-1 Mux(2's Complement refers figure 1) 3-bit Comparator

# Design Topology (Continuing)

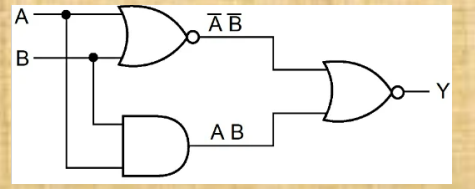
- AND gate can be implemented as below



- OR gate can be implemented as below



- XOR gate can be implemented as below



# Design Topology & Reasoning

- Reasoning

  -This is an intuitive design, and we got ideas from combinational logic.

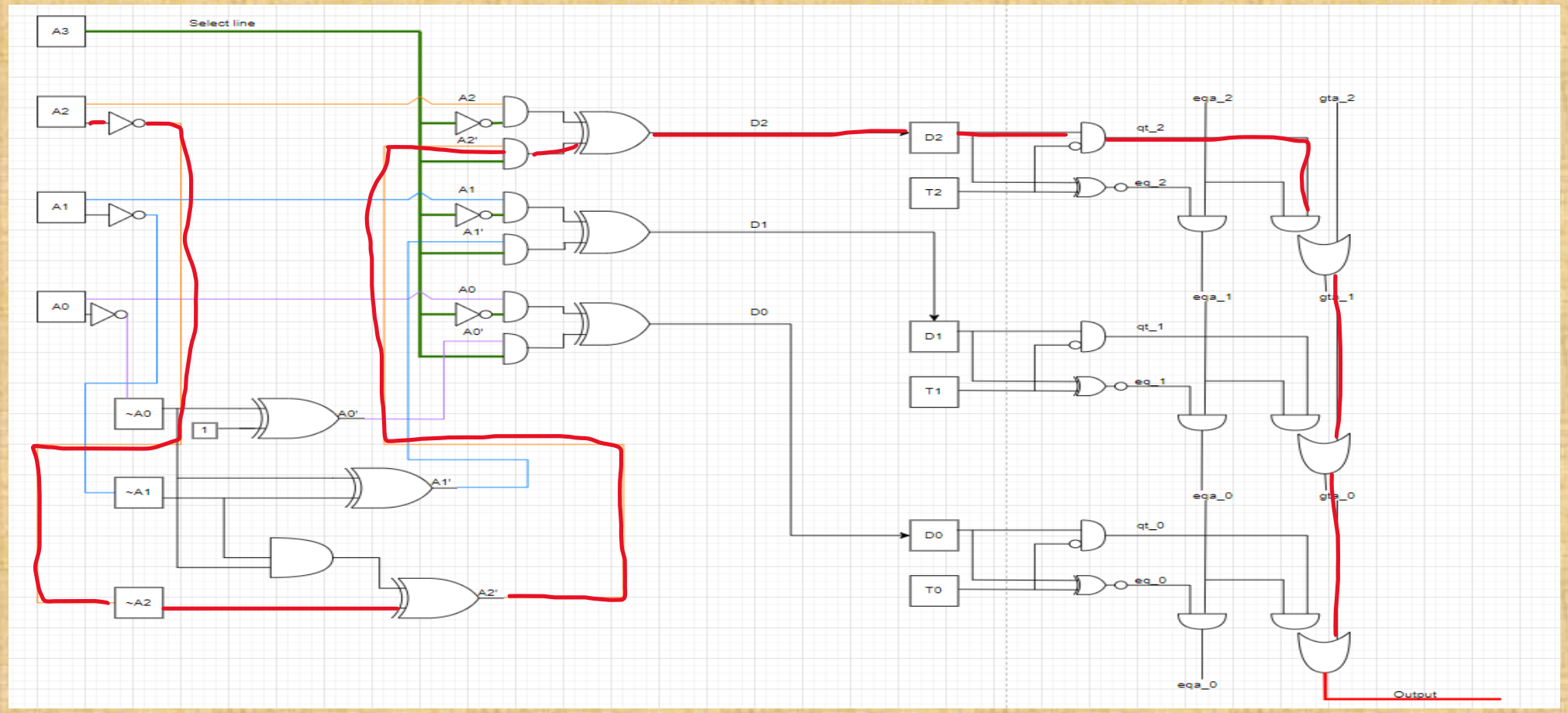
  -Beyond that, we made a little improvement on the Half-Adder design, which uses less logic gates and so transistors. Thus, it saves energy from the design perspective.

- Other options

  - We have considered the full adder, ripple adder, etc. But we thought it was not necessary to put a full adder into the design, since we were not designing an ALU to do a very complex calculation. And main goal of this design is saving energy and with less transitors

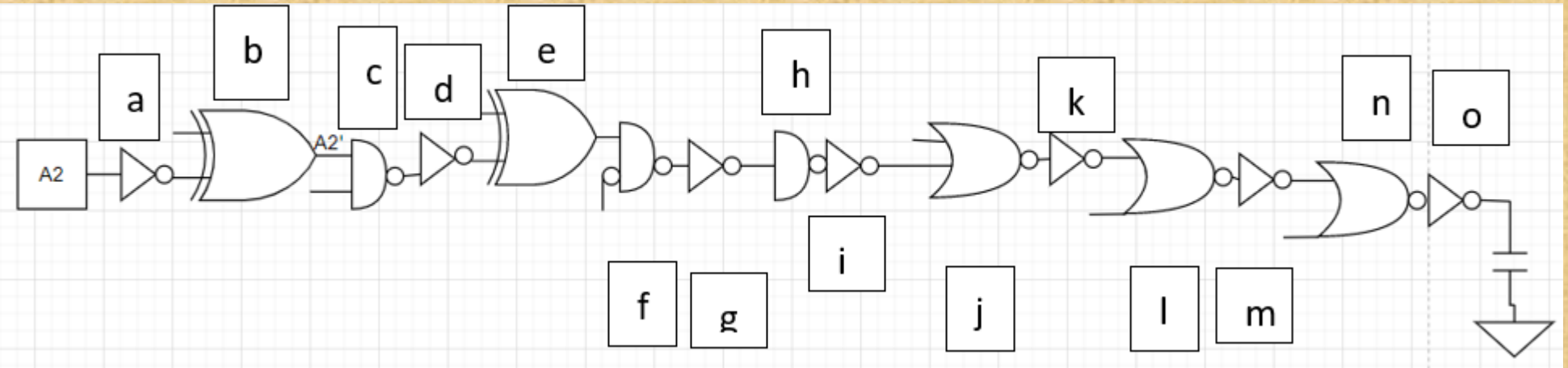
# Critical Path Analysis

- Highlight Critical Path



# Critical Path Gate Sizing Approach

- Show sizing optimization of the critical path




- Sizing of each stage : $C_{in} = g \times C_{out}/f^*$

| a = 1 | b = 1.78 | c = 0.79 | d = 1.05 | e = 1.88 | f = 0.83 | g = 1.11 | h = 1.98 |
|---|---|---|---|---|---|---|---|
| i = 2.64 | j = 4.69 | k = 5 | l = 8.9 | m = 9.49 | n = 16.9 | o = 18 | |

# Critical Path Gate Sizing Approach (Continuing)

- $C_{out} = 32 \;\; C_{in} = 1$
- Parasitic delay: $p_{XOR} = \frac{6.5\times4+4.3\times4}{6.5+4.3} = 4; p_{NAND} = \frac{6.5\times2+4.3\times2}{6.5+4.3} = 2; p_{NOR} = \frac{6.5\times2+4.3\times2}{6.5+4.3} = 2$
- Logic effort: $g_{XOR} = \frac{6.5\times4+4.3\times4}{6.5+4.3} = 4; g_{NAND} = \frac{6.5+4.3\times2}{6.5+4.3} = 1.4; g_{NOR} = \frac{6.5\times2+4.3}{6.5+4.3} = 1.6$

- G = 1*4*1.4*1*4*1.4*1*1.4*1*1.6*1*1.6*1*1.6*1=179.83
- B=1
- H = 32/1 = 32
- Path effort F = GHB = 179.83*32*1 =5754.9
- **Stage effort: $f^* = \sqrt[15]{F}$ 1.78**
- Min delay = $15 \times f^* + (1+4+2+1+4+2+1+2+1+2+1+2+1+2+1) =$ **53.7**
- **Ctot = 183.02**
- **Energy = $C_{tot} * V_{dd}^2$ = 183.02*$1^2$**

# Sizing & $V_{DD}$ Energy Minimization

- Sizing impact
  - By using excel model provided in the lecture, $E_{tot}$ drops down to 132.54, as 1.5* $Delay_{min}$

| stage | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | load | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| size | 1 | 1.20 | 1.49 | 1.84 | 2.27 | 2.78 | 3.37 | 4.04 | 4.77 | 5.48 | 6.08 | 6.36 | 5.93 | 4.16 | 0.00 | 32 | | |
| | | | | | | | | | | | | | | | | | | |
| Energy | 2.20 | 2.69 | 3.33 | 4.11 | 5.05 | 6.15 | 7.41 | 8.81 | 10.25 | 11.57 | 12.44 | 12.28 | 10.09 | 4.16 | 32.00 | | Etot | 132.54 |

- Vdd impact
  - $Dmin = \frac{K*Vdd}{(Vdd-0.2)^2} = 53.64 = \frac{K*Vdd}{(Vdd-0.2)^2}$
  - K = 34.33
  - $1.5 * Dmin = \frac{53.64*Vdd'}{(Vdd-0.2)^2}$
  - Vdd' = 0.775
  - **Energy = $C_{tot}*V_{dd}^2 = 183.02 \times 0.775^2 = 109.93$**
- Combination impact
  - **Energy = $C_{tot}*V_{dd}^2 = 132.54 \times 0.775^2 = 79.61$**

# Sizing vs. $V_{DD}$ Optimization ?

- How did you decide about relative contribution of sizing and VDD in your overall delay increase?
  - Calculated energy consumption using either sizing optimization or Vdd optimization.
  - Estimated the energy reduction in these two methods.
  - Greater energy reduction is the better way to reduce energy in the design

- Vdd optimization is the better way for this design, since it reduces 40% energy when delay is 1.5 times minimum delay

- We end up 56.5% energy reduction when both optimization are applied

# Discussion & Summary

- Three most important features of our design
  - 1. Simplified Half-Adder Circuit
  - 2. Intuitive Design
  - 3. 3bit Comparator,  from MSB to LSB, using gt and eq signal.

- Given another chance, 3 things you would do different
  - 1. Trying using PTL
  - 2. Calculate other paths' delay
  - 3. We have little problem in our excel solver, as one of the stage effort is 0. But we can't figure out the cause of this problem. I think we could do it better if there is more time provided

# Q&A