

GEC Workshop | 2022
Discussion 5

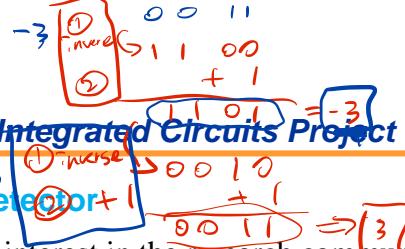
Digital Integrated Circuits



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$$\begin{array}{c}
 \text{Inputs: } 0, 0, 1, 1, -2 \\
 \text{Operations: } 0 \cdot (-2^3) + 0 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0 \\
 = 0 + 0 + 2 + 1 = 3
 \end{array}$$

Digital Integrated Circuits Project



$$\begin{array}{c}
 \text{Inputs: } 1, 1, 0, 1 \\
 \text{Operations: } -2^3 + 2^2 + 2^1 + 2^0 \\
 = -8 + 4 + 1 = -3
 \end{array}$$

Appendix A – Absolute-value Detector

Spike-sorting algorithms have gained interest in the research community with the recent advancements in neural signal acquisition systems. For your project, you are to design one of the commonly used spike-detection algorithms, named Absolute-value detection.

Figure A-1 shows the basic diagram for an Absolute-value detector. The inputs (shown in blue) are given to you (See the design constraints for more detail). The Absolute-value detector (shown in black) is to be designed and implemented by you.

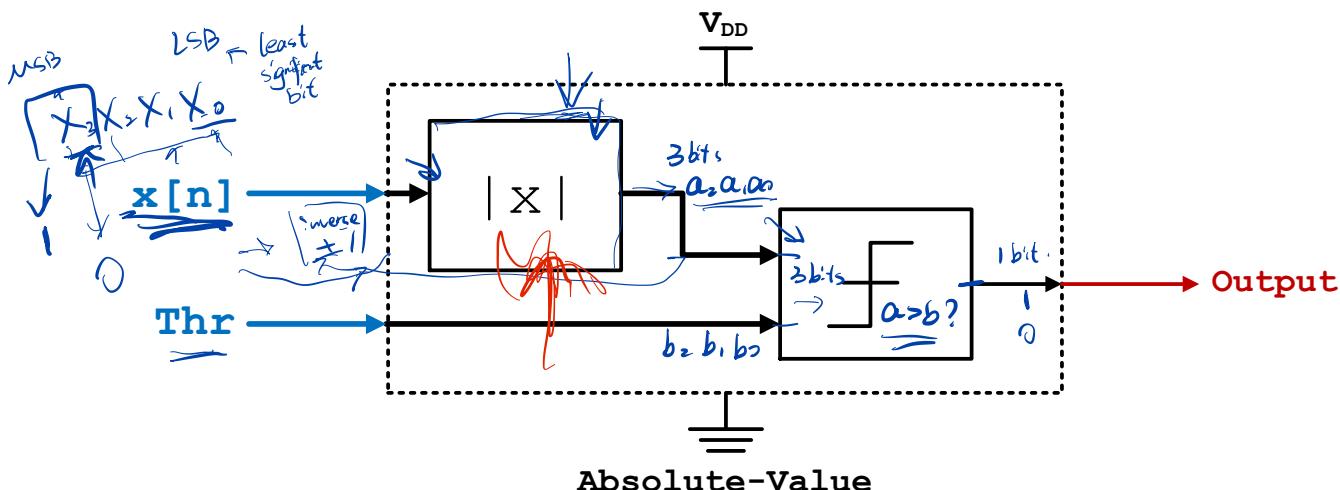


Figure A-1

As shown above there are two main components to the absolute-value detection.

- (i) finding the magnitude (absolute value) of your neural signal ($x[n]$) and
- (ii) comparing the magnitude to the given threshold value (Thr).

If the magnitude of your signal is greater than the threshold output should display a "1" (high logic value), otherwise the output should be a "0" (low logic value).

Appendices B and C provide some background and references for the design of Absolute-value and comparator blocks, respectively.

Absolute Value Circuit

- Understand what the circuit does

 - Truth table

- Options

 - Mux based adder
 - Mux based combinational logic
 - Combinational logic

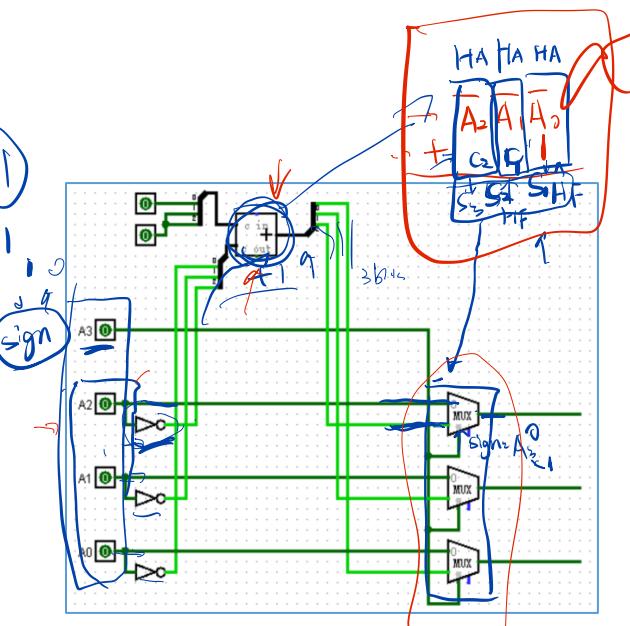


Figure 2: Mux based adder

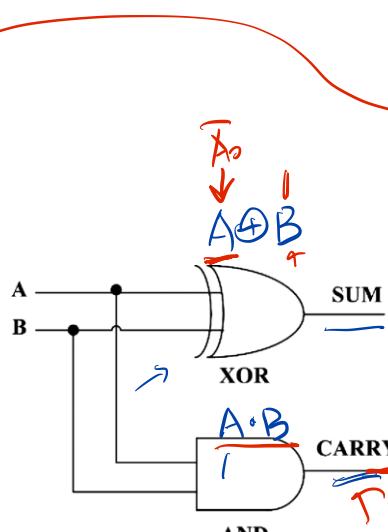
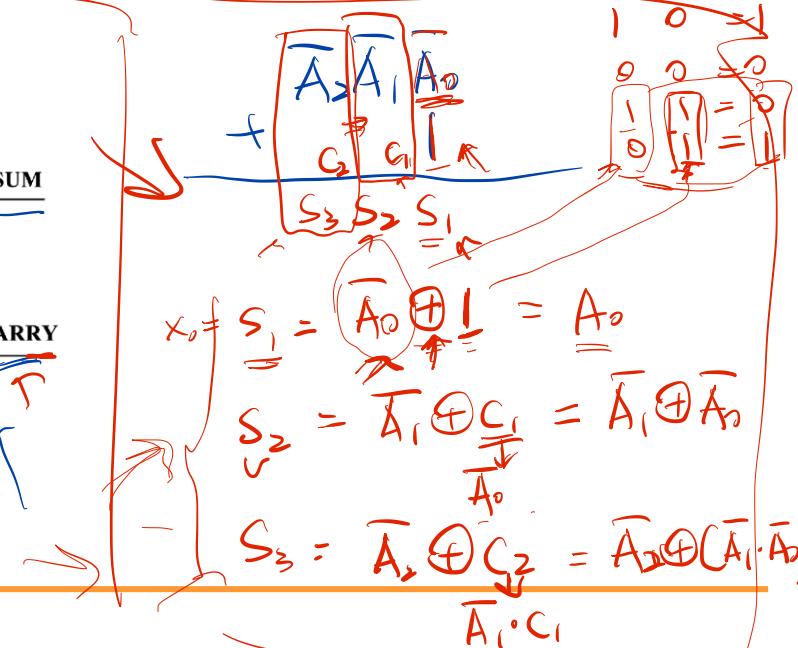


Figure 3: Half adder

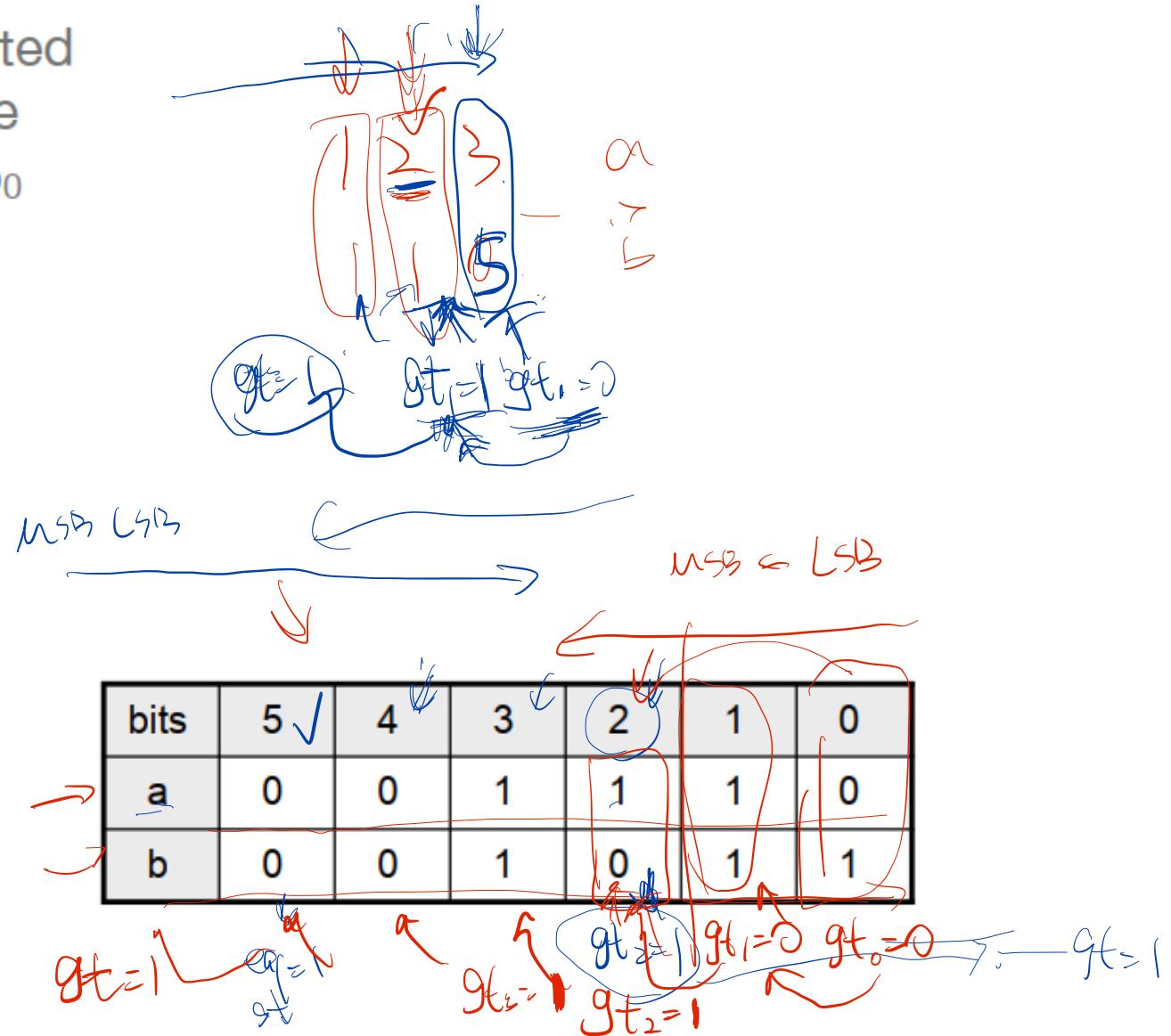
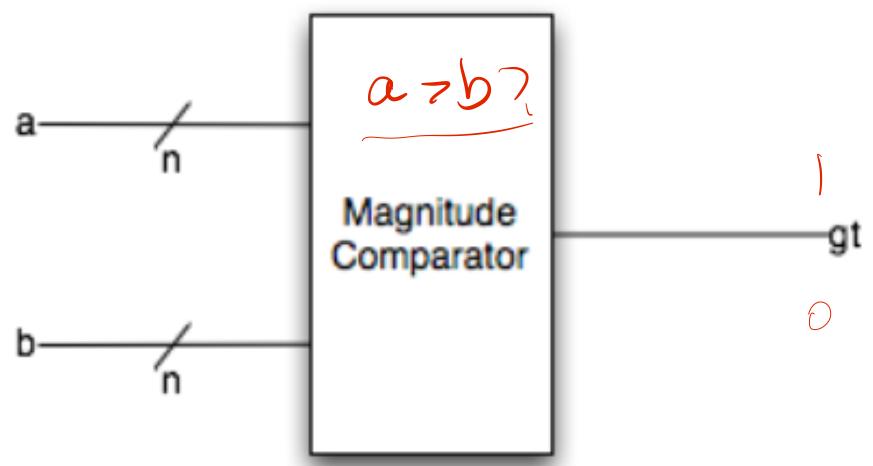
A3	A2	A1	A0	X3	X2	X1	X0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	1	0	0	0	0	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	0
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

Figure 1 : Truth table of absolute value



Magnitude Comparator

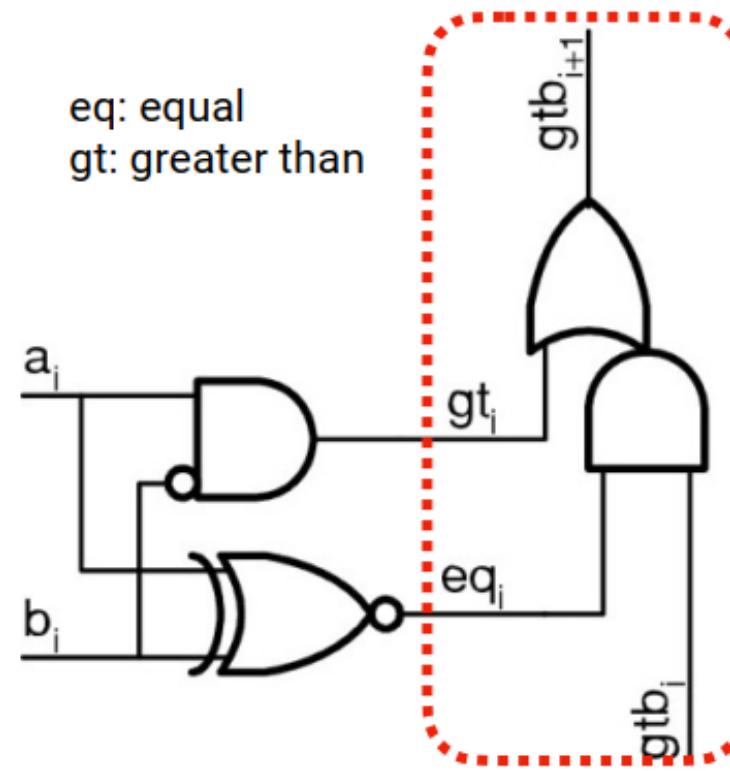
- $gt=1$ iff the (binary) value represented by $a_{n-1} a_{n-2} \dots a_0$ is greater than the value represented by $b_{n-1} b_{n-2} \dots b_0$
- **Bitslice** an example ...
 - ▶ $a: 001110, b: 001011$



Magnitude Comparator

- $gt=1$ iff the (binary) value represented by $a_{n-1} a_{n-2} \dots a_0$ is greater than the value represented by $b_{n-1} b_{n-2} \dots b_0$
- $gtb_i = 1$ indicates that for 0 through $i-1$ input a is greater than b

gtb_i	eq_i	gt_i	gtb_{i+1}
1	1	0	1
1	0	1	1
1	0	0	0
0	1	0	0
0	0	1	1
0	0	0	0

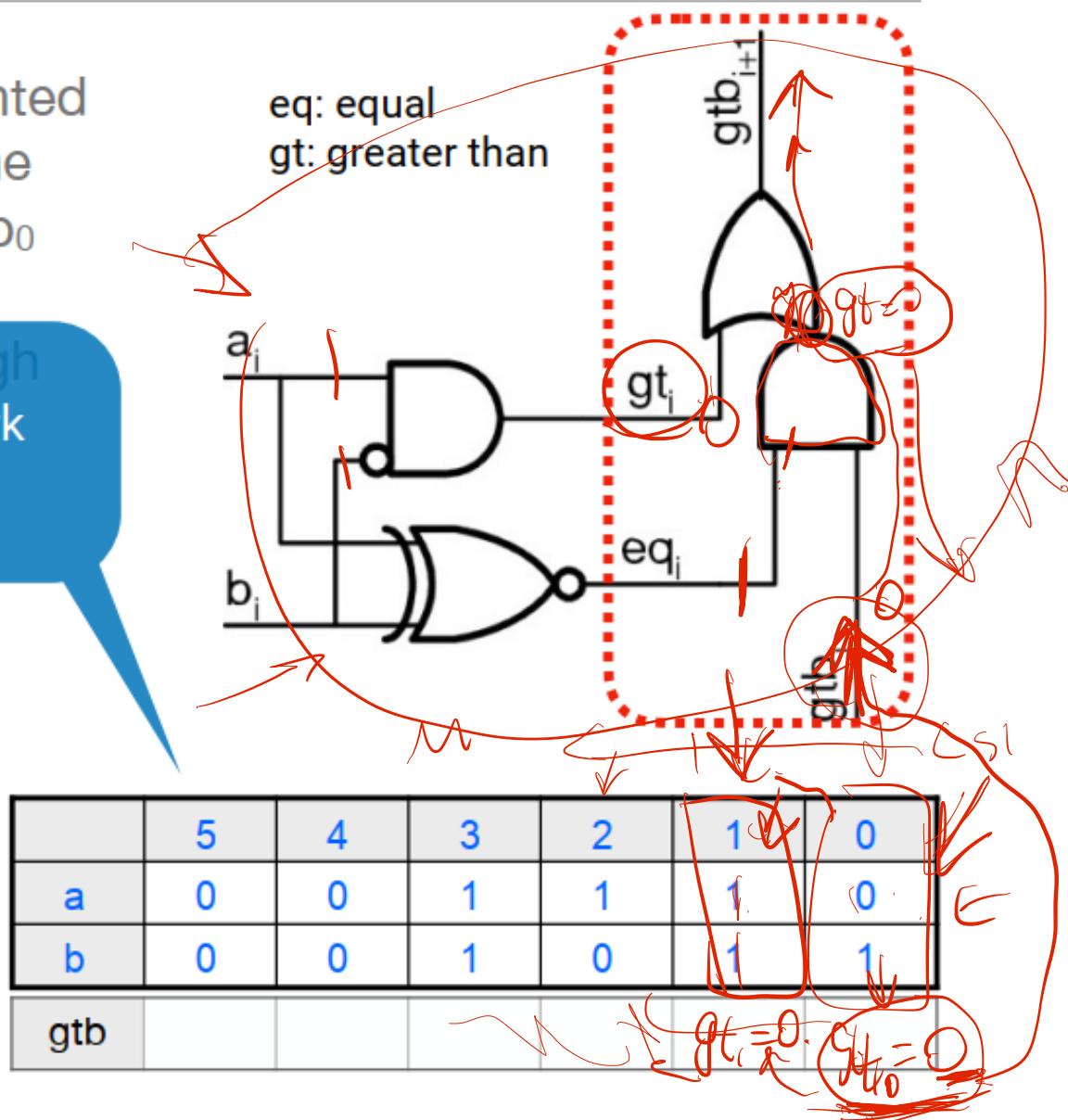


Magnitude Comparator

- $gt=1$ iff the (binary) value represented by $a_{n-1} a_{n-2} \dots a_0$ is greater than the value represented by $b_{n-1} b_{n-2} \dots b_0$

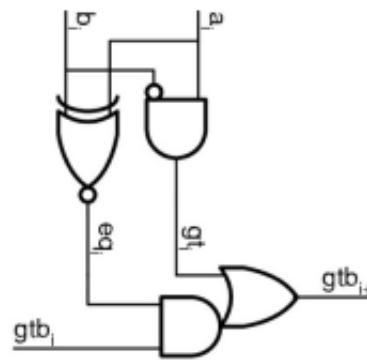
- $gtb_i = 1$ indicates that for 0 through $i-1$ input a is greater than b
Can you work out this row?

gtb_i	eq_i	gt_i	gtb_{i+1}
1	1	0	1
1	0	1	1
1	0	0	0
0	1	0	0
0	0	1	1
0	0	0	0



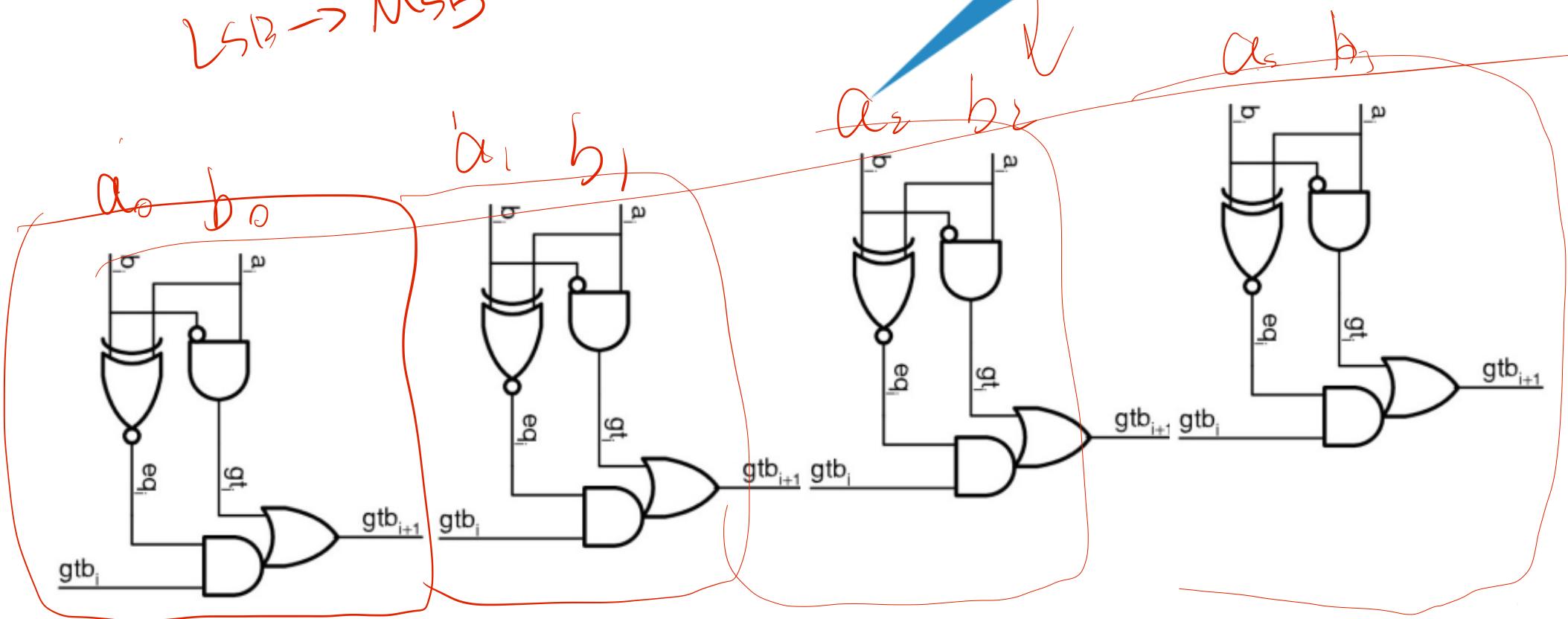
Magnitude Comparator

- What's next? 🧑
- Connect them!



🧑 Problem and improvement?

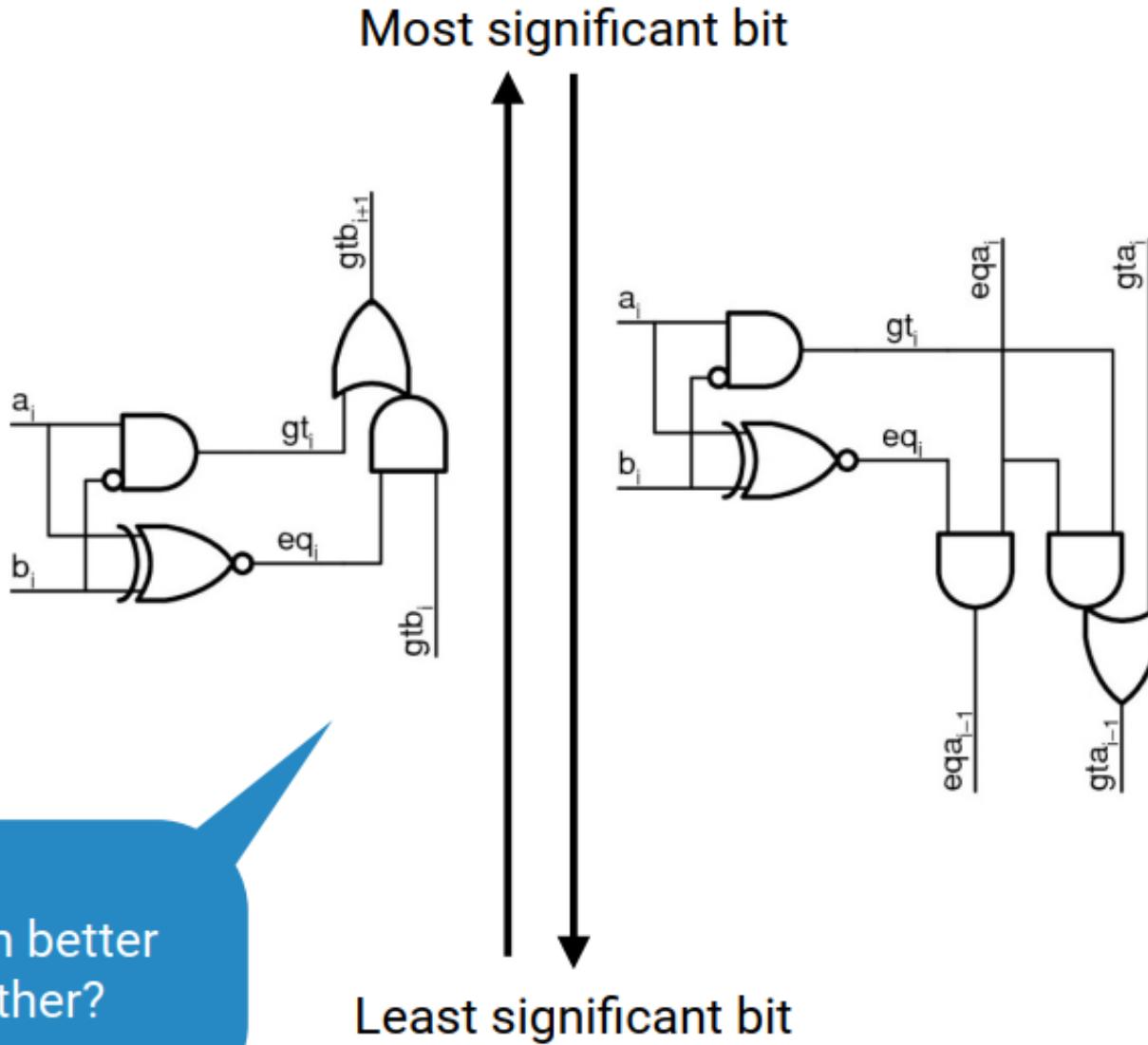
LSD \rightarrow MSB



Magnitude Comparator: an alternate design

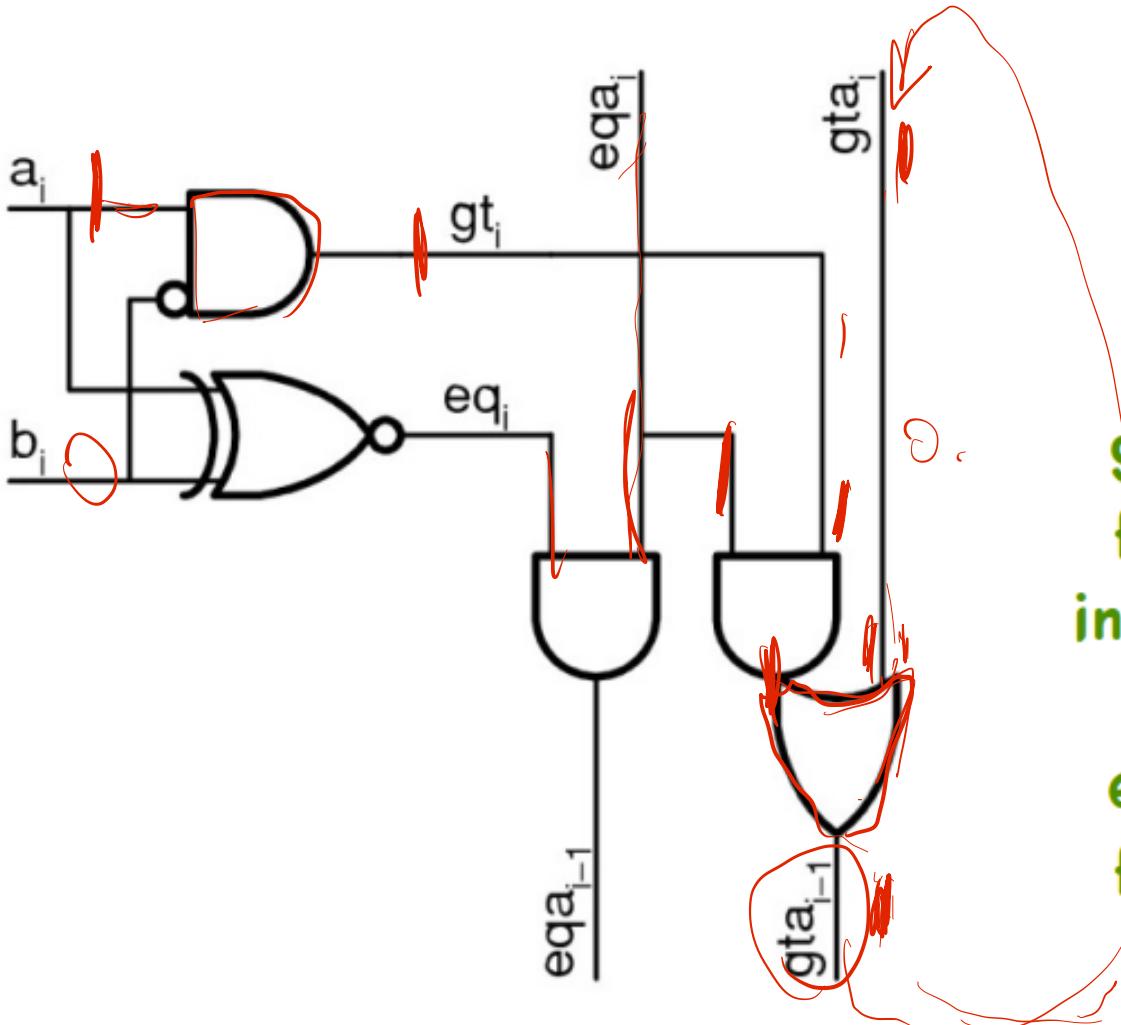
- The design so far assumes bitslicing from the least to the most significant bits
- What if we want to go from the most to the least significant bit?
- Main difference: once gta is true in one bitslice, all following bitslices have gta set as well

Is one design better than the other?



Going from Most to Least Significant Bit

MSB \rightarrow LSB



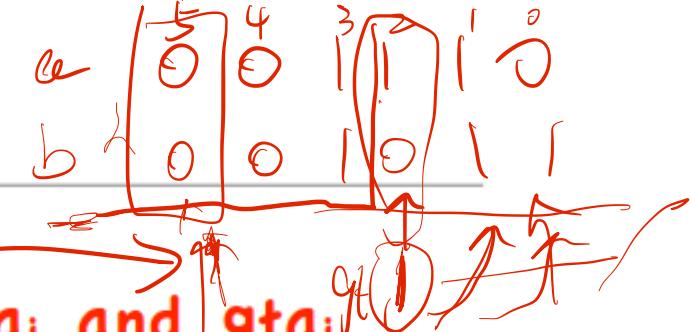
What do eqa_i and gta_i indicate?

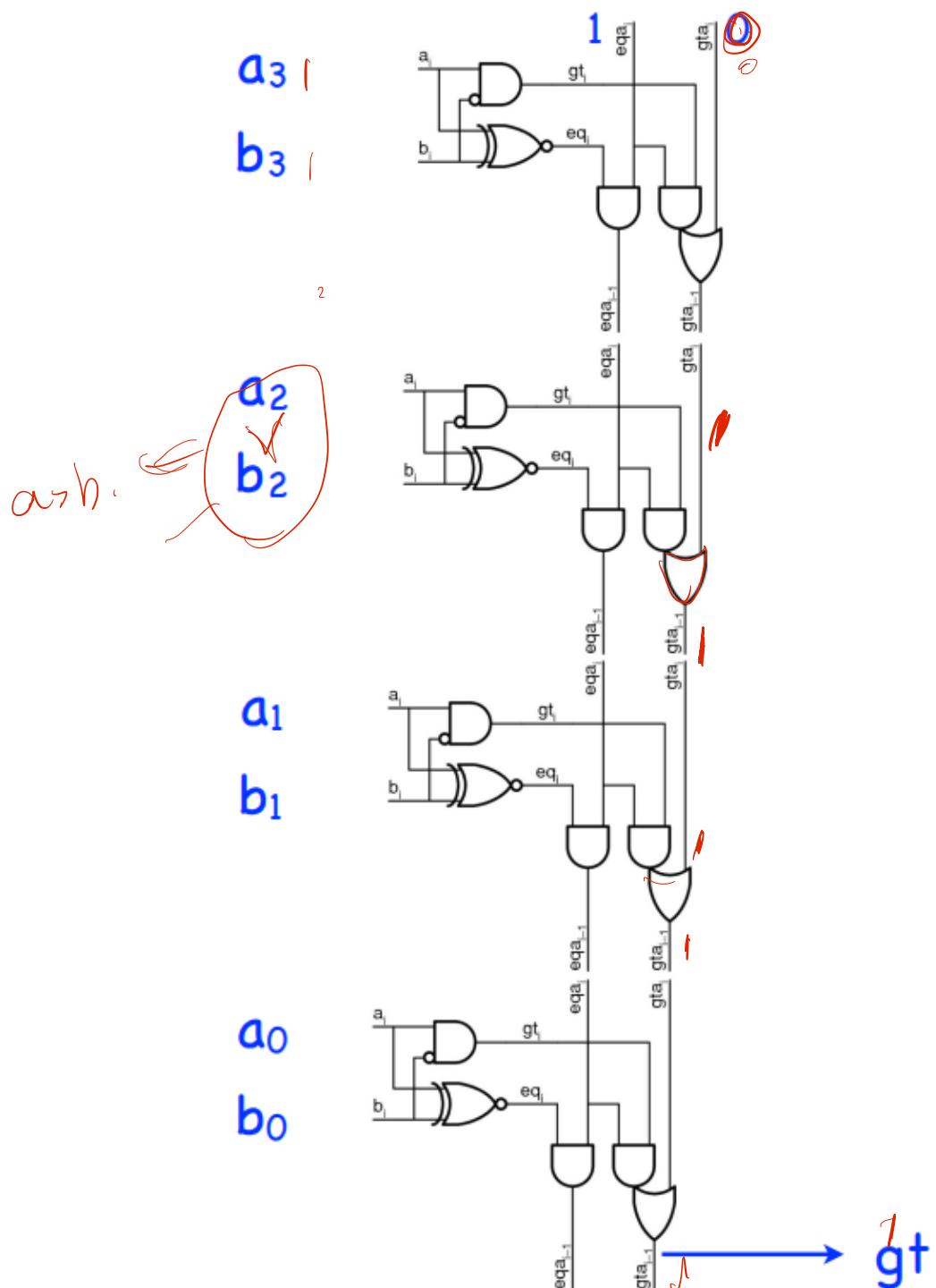
$$\begin{cases} a > b \\ = 0 \end{cases}$$

Answer:

$gta_i == 1$ indicates that for bit $i+1$ through $n-1$ input a is greater than b.

$eqa_i == 1$ indicates that for bit $i+1$ through $n-1$ input a is equal to b.





Once gta is set in one bitslice, all following bitslices have gta set as well.

General Logical Effort formulation

$$\text{Delay} = \sum_{i=1}^N (p_i + g_i \cdot h_i)$$

Stage effort: $f_i = g_i \cdot b_i \cdot h_i$

Path electrical effort: $H_{path} = C_{out}/C_{in}$

Path logical effort: $G_{path} = g_1 g_2 \dots g_N$

Branching effort: $B_{path} = b_1 b_2 \dots b_N$

Path effort $F_{path} = G_{path} \cdot H_{path} \cdot B_{path}$

Branching

Path delay $D = \sum D_i = \sum P_i + \sum G_i \cdot H_i$

Optimum Effort per Stage

When each stage bears the same effort:

$$f^N = \prod g \cdot h = \text{PathEffort} \geq G \cdot B \cdot H$$

$$g \cdot h_i = f = \sqrt[N]{\text{PathEffort}}$$

Fanout of each stage: $h_i = f/g_i$

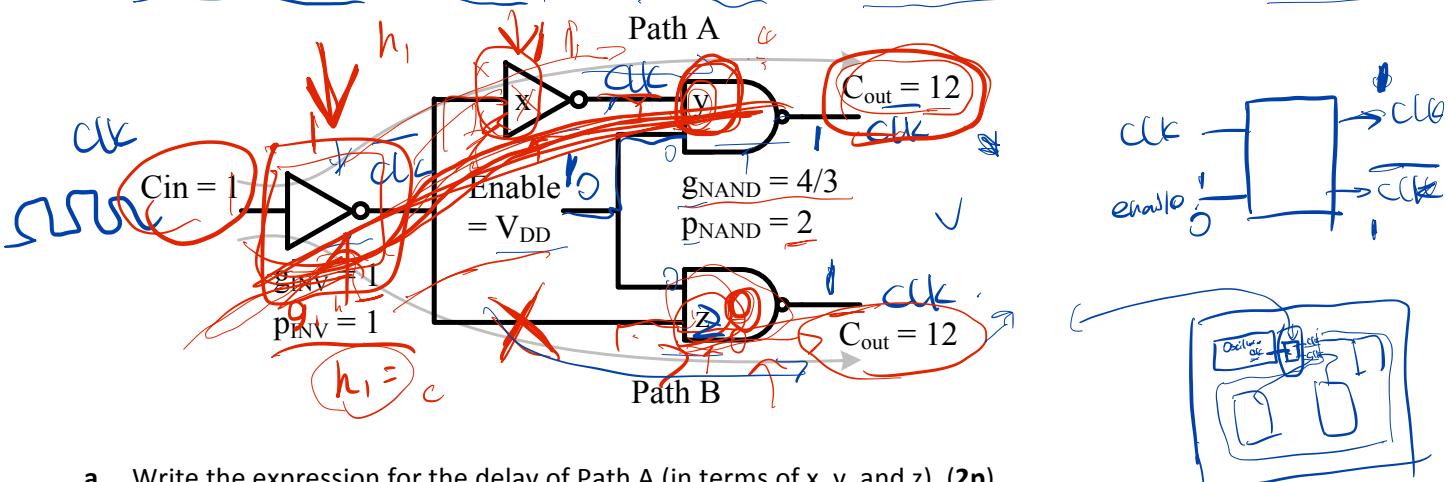
Complex gates should drive smaller load!!!

Minimum path delay

$$D_{min} = \sum (g_i \cdot h_i + p_i) = N \cdot f + P$$

PROBLEM 2: Gate Sizing (10 pts)

The following circuit is commonly used as the root of a clock tree that generates both true and complementary clocks. The circuit also disables the clocks during SLEEP mode. The logical effort and parasitic delay are given. Capacitances are in normalized units (unitless). x , y , and z , are the input capacitances (normalized) of each gate.



- a. Write the expression for the delay of Path A (in terms of x , y , and z). (2p)

$$D_A = \sum_{i=1}^3 g_i h_i + p_i = g_1 h_1 + p_1 + g_2 h_2 + p_2 + g_3 h_3 + p_3 \\ = \frac{4}{3} \cdot x + 1 + \frac{4}{3} \cdot y + 1 + \frac{4}{3} \cdot z + 2 \\ D_{path-A} = 4 + x + 2 + \frac{y}{\frac{3}{4}} + \frac{z}{\frac{3}{4}}$$

- b. Write the expression for the delay of Path B (in terms of x , y , and z). (2p)

$$D_B = g_1 h_1 + p_1 + g_2 h_2 + p_2 \\ = x + 2 + 1 + \frac{4}{3} \cdot \frac{12}{\frac{3}{4}} + 2 \\ D_{path-B} = 3 + x + 2 + \frac{16}{3}$$

- c. Find x and y that minimize the delay of Path A. (2p)

$$D_A(x, y) = 4 + x + \frac{y}{\frac{3}{4}} + \frac{16}{3} + 2$$

$$\text{① } F_A = G \cdot H \cdot B = 1 \cdot 1 \cdot \frac{4}{3} \cdot 12 \cdot 1 = 16$$

$$n=3 \quad f^* = F^{\frac{1}{3}} = 16^{\frac{1}{3}} = g_1 h_1 = g_1 h_2 = g_1 h_3$$

$$x + \frac{y}{\frac{3}{4}} + \frac{16}{3} \geq 3 \cdot \left(x \cdot \frac{y}{\frac{3}{4}} \right)^{\frac{1}{3}} \Rightarrow 3 \cdot 16^{\frac{1}{3}} \text{ when } x = \frac{y}{\frac{3}{4}} = \frac{16}{3}$$

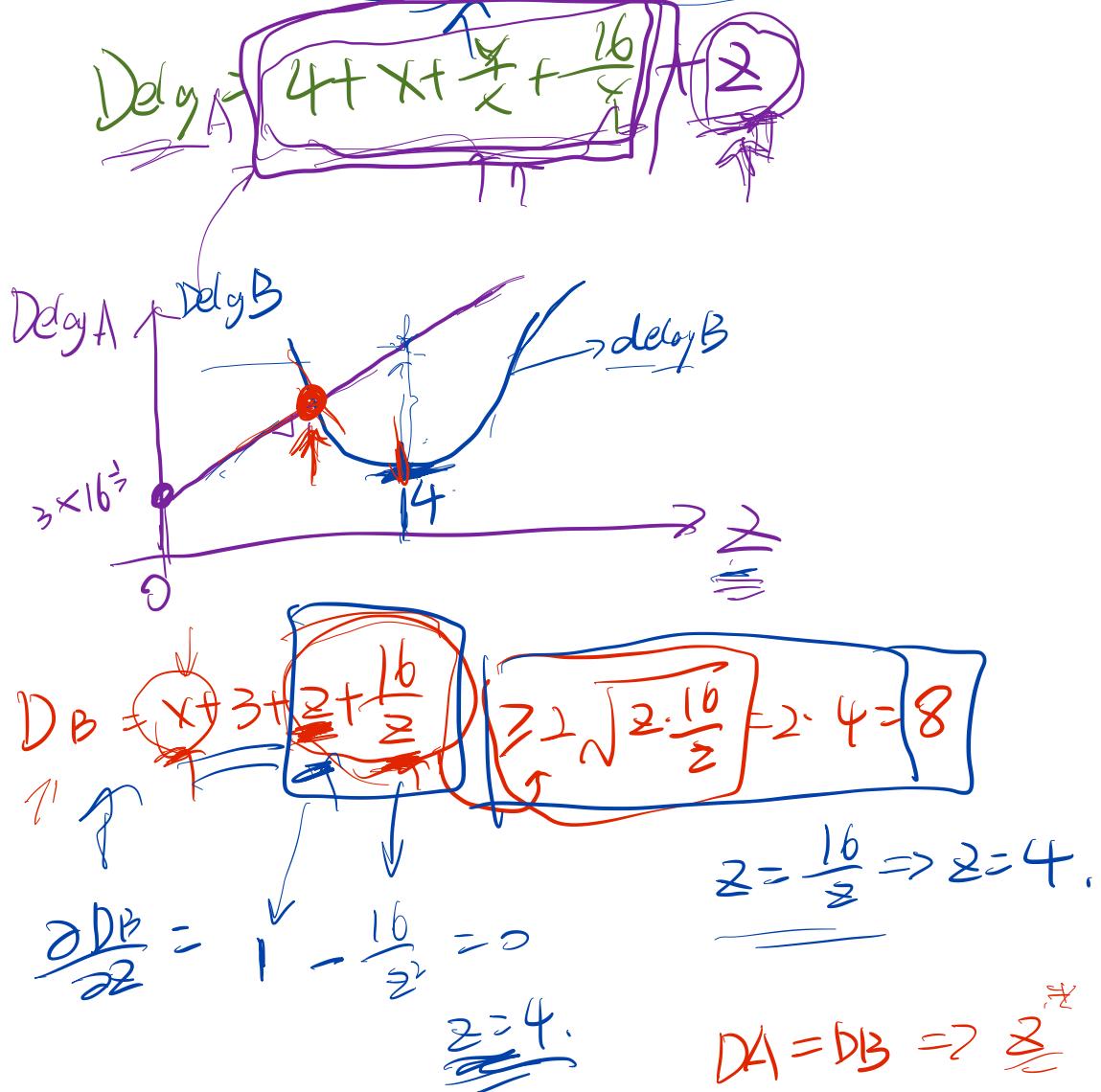
$$x = 16^{\frac{1}{3}}, y = 16^{\frac{1}{3}}$$

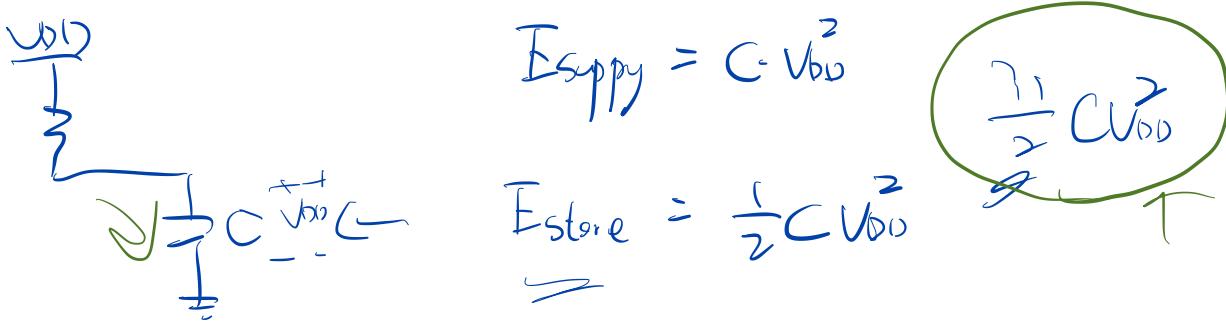
$$\text{② } D_A = f(x, y)$$

$$\checkmark \frac{\partial D_A}{\partial x} = 0 \Rightarrow 0 + 1 - \frac{y}{x^2} + 0 = 0 \Rightarrow 1 - \frac{y}{x^2} = 0 \Rightarrow y = x^2$$

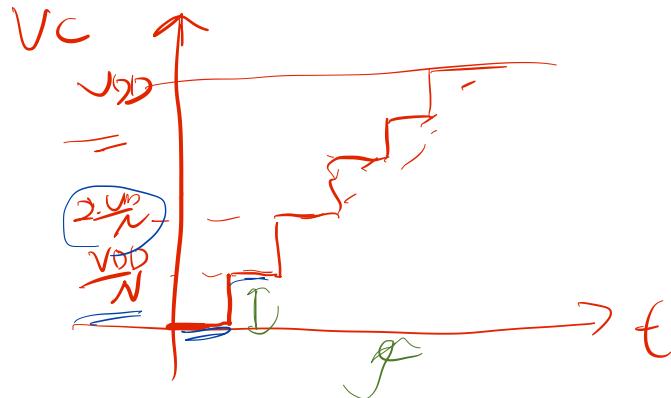
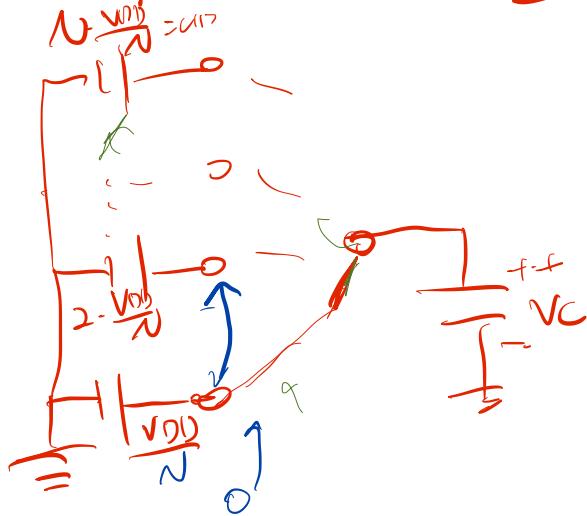
$$\checkmark \frac{\partial D_A}{\partial y} = 0 \Rightarrow 0 + \frac{1}{x} - \frac{16}{y^2} = 0 \Rightarrow \frac{1}{x} = \frac{16}{y^2} \Rightarrow x = \frac{y^2}{16} \Rightarrow x = \frac{x^4}{16} = 16 - x^3$$

d. Determine x , y , and, z for **equal** and **minimum** delay of Path A and Path B.





step wise charging



	$E_{\text{supply}} = C \cdot V_{\text{Supply}} \cdot V_{\text{Supply}}$	$E_{\text{cap}} = \frac{1}{2} C (V_0^2 - V_i^2)$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$
Step 1 $\frac{V_{\text{DD}}}{N}$	$= C \cdot \frac{V_{\text{DD}}}{N} \cdot \frac{V_{\text{DD}}}{N} = C (\frac{V_{\text{DD}}}{N})^2$	$= \frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$
Step $\frac{2V_{\text{DD}}}{N}$	$= C \cdot \frac{2V_{\text{DD}}}{N} \cdot \frac{V_{\text{DD}}}{N} = 2C (\frac{V_{\text{DD}}}{N})^2$	$= \frac{1}{2} C ((\frac{2V_{\text{DD}}}{N})^2 - (\frac{V_{\text{DD}}}{N})^2)$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$
		$= \frac{1}{2} C (4(\frac{V_{\text{DD}}}{N})^2 - (\frac{V_{\text{DD}}}{N})^2)$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$
		$= \frac{3}{2} C (\frac{V_{\text{DD}}}{N})^2$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$

Step K $\frac{(K-1)V_{\text{DD}}}{N}$	$= C \cdot \frac{K \cdot V_{\text{DD}}}{N} \cdot \frac{V_{\text{DD}}}{N} = C K (\frac{V_{\text{DD}}}{N})^2$	$\frac{1}{2} C [(\frac{K \cdot V_{\text{DD}}}{N})^2 - (\frac{(K-1) \cdot V_{\text{DD}}}{N})^2]$	$\frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2$
		$= \frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2 [K^2 - (K-1)^2]$	
		$= \frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2 (K+K-1)(K-K+1)$	
		$= \frac{2K-1}{2} C (\frac{V_{\text{DD}}}{N})^2$	
		$= (K-\frac{1}{2}) C (\frac{V_{\text{DD}}}{N})^2$	
$E_{\text{total, disp}} = N \cdot \frac{1}{2} C (\frac{V_{\text{DD}}}{N})^2 = \frac{1}{2} C V_{\text{DD}}^2$			