A[53.76] FO4(1V),[183.02] Eu(1V)
4-bit Absolute Value Detector

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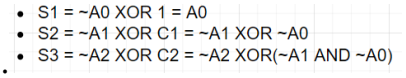
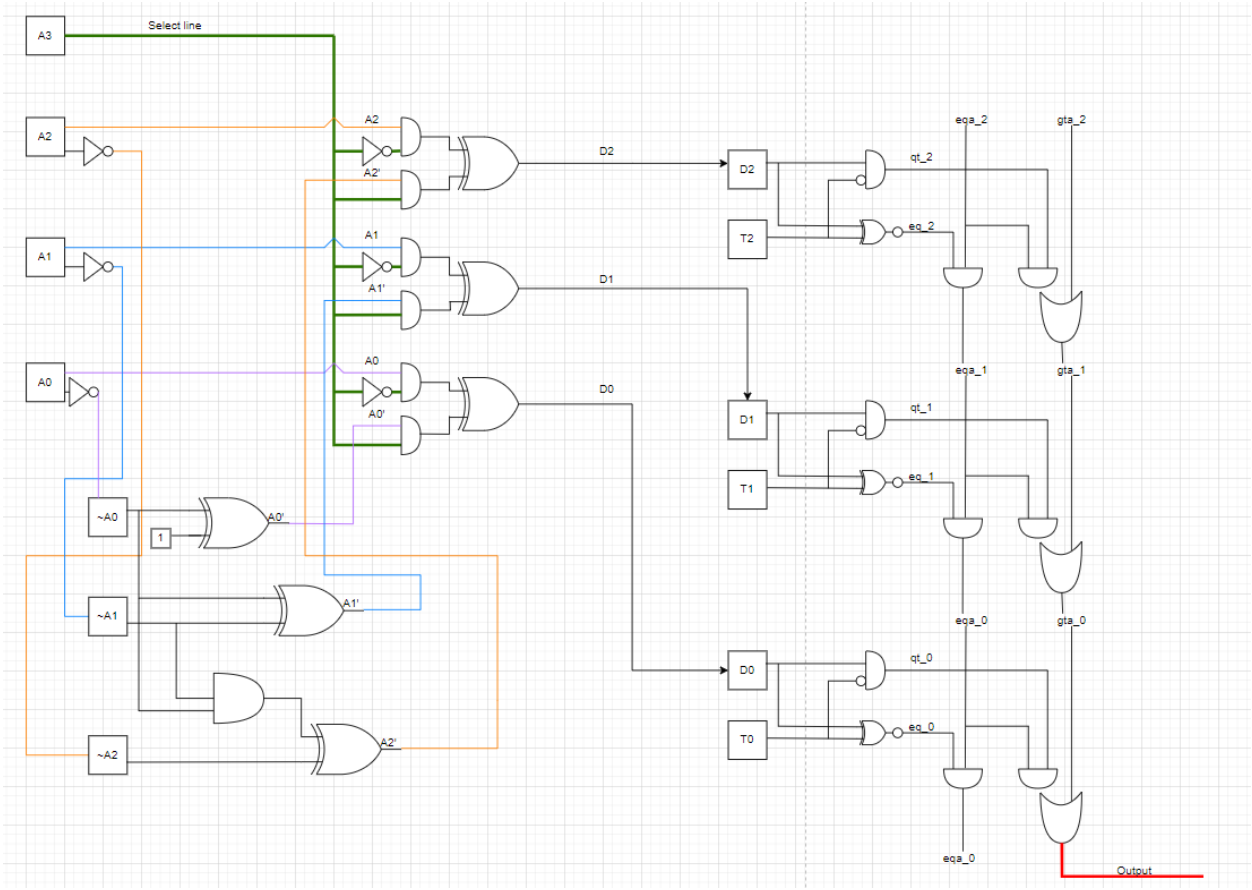
1. Key Design Techniques
   - static CMOS, XOR, AND, and OR gate
   - 2-to-1 mux used to determine whether the sign bit is positive, and it will output corresponding digit.
   - A simplified 2's complement circuit, which used to convert the input digits into 2's complement form. Circuit design is based on the formulas showing below
   - 

   - A 3 bits Comparator which used to compared between the magnitude value of input and threshold value
2. Results
   - E_tot without any optimization = 183.02
   - Sizing + Vdd optimization / Sizing impact (E = 132.54)
   - - Delay increase: [50] % out of 50%
   - - Energy reduction: [27.58] % out of 50%
   - Sizing + Vdd optimization / V_DD impact (E = 109.63)
   - - Delay increase: [50] % out of 50%
   - - Energy reduction: [40] % out of 50%
   - Sizing + Vdd optimization / $combination$ impact (E = 79.61)
   - - Delay increase: [50] % out of 50%
   - - Energy reduction: [56.5] %
3. Finding
   - In this project, we find that Vdd minimization reduces more energy consumption than the sizing impact, which scales down energy consumption of whole design. However, there may exist some disadvantages by doing so. For example, there are not enough energy, or power to drive transistor to send strong signal, i.e., weak HIGH signal.

   - Beyond that, there are still some improvements we could do if there are more time and background information provided. For example, we could minimize energy consumption by reducing total transistors usage, reducing number of stages in the design and using other circuit method, like PTL.

Appendix:


A3
Select line
A2
A1
A0
A2
A2'
A1
A1'
A0
A0'
D2
D1
D0
~A0
1
A0'
~A1
A1'
~A2
A2'
D2
T2
D1
T1
D0
T0
eqa_2
gta_2
qt_2
eq_2
eqa_1
gta_1
qt_1
eq_1
eqa_0
gta_0
qt_0
eq_0
eqa_0
Output