Digital Integrated Circuits
Homework #4

$P(B+C=1) = P(B=0)\cdot P(C=1) = \frac{3}{4}\cdot\frac{1}{3} = \frac{1}{4}$
$+ P(B=1)\cdot P(C=0) = \frac{1}{4}\cdot\frac{2}{3} = \frac{1}{6}$
$+ P(B=1)\cdot P(C=1) = \frac{1}{4}\cdot\frac{1}{3} = \frac{1}{12}$
$= \frac{1}{2}$

Due 2 hours before the next lecture

Problem 1: Finding α

Figure 1 shows the logical symbol (and functional picture) of an "And-Or-Invert" gate that implements $F = (A(B + C))'$.

Estimate the activity factor, $\alpha_{F_{0\to1}}$, for the output f, if $p(A = 1) = 1/2$, $p(B = 1) = 1/4$, and $p(C = 1) = 1/3$.

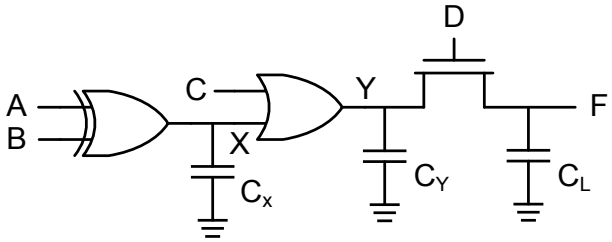
$P(A\cdot(B+C)=1) = P(A=1)\cdot P(B+C=1) = \frac{1}{2}\cdot\frac{1}{2} = \frac{1}{4}$

$P(F=1) = P(A\cdot(B+C)=0) = \frac{3}{4}$

$\alpha_{F_{0\to1}} : P(F=0)\cdot P(F=1) = \frac{1}{4}\cdot\frac{3}{4} = \frac{3}{16}$

Problem 2: Power and Energy

Consider the following circuit, with XOR, AND gates and one NMOS transistor.



$P_{sw} = P_{sw,X} + P_{sw,Y} + P_{sw,F} = 4.9\cdot10^{-7} + 2.3616\cdot10^{-7} = 7.2616\cdot10^{-7}\,W$

(a) What logic function is implemented by this circuit (inputs: A, B, C, and D)?

$F = [(A \oplus B) + C]\cdot D$

(b) Assume the probably of logic 1 for inputs: p(A = 1) = 0.5, p(B = 1) = 0.5, p(C = 1) = 0.2, p(D = 1) = 0.3, capacitance: $C_X = C_Y = 10$ fF, $C_L = 20$ fF, frequency f = 100 MHz, $V_{DD} = 1$V, threshold voltage $V_{TN} = 0.2$ V, $V_{TP} = -0.3$ V. Calculate the average switching power P_{sw} of the circuit (logic gates and input D are powered from V_{DD}).

XOR:

A	B	X
0	0	0
1	0	1
0	1	1
1	1	0

$P(X=1) = P(A=1)\cdot P(B=0) + P(A=0)\cdot P(B=1) = \frac{1}{2}\cdot\frac{1}{2} + \frac{1}{2}\cdot\frac{1}{2} = \frac{1}{2}$

$\alpha_{X:0\to1} = P(X=0)\cdot P(X=1) = \frac{1}{2}\cdot\frac{1}{2} = \frac{1}{4}$
$= P(X=0)\cdot(1 - P(X=0))$

p(X = 1) = 1/2

$\alpha_{X:0\to1}$ = 1/4

C=0: 0.8 C=1: 0.2

OR:

X	C	Y
0	0	0
1	0	1
0	1	1
1	1	1

$P(Y=1) = P(X=1)\cdot P(C=0) + P(X=0)\cdot P(C=1) + P(X=1)\cdot P(C=1) = \frac{1}{2}\cdot0.8 + \frac{1}{2}\cdot0.2 + \frac{1}{2}\cdot0.2 = 0.6$

$\alpha_{Y:0\to1} = P(Y=0)\cdot P(Y=1) = 0.4\cdot0.6$

p(Y = 1) = 0.6

$\alpha_{Y:0\to1}$ = 0.24

$P_{sw,X} + P_{sw,Y} = (\alpha_X\cdot C_X + \alpha_Y\cdot C_Y)\cdot V_{DD}^2\cdot f$
$= \left(\frac{1}{4}\cdot10\cdot10^{-15} + 0.24\cdot10\cdot10^{-15}\right)\cdot1^2\cdot100M = 4.9\cdot10^{-7}\,W$

$P_{sw,X} + P_{sw,Y}$ = $4.9\cdot10^{-7}$ W

AND:

Y	D	F
0	0	0
1	0	0
0	1	0
1	1	1

$P(F=1) = P(Y=1)\cdot P(D=1) = 0.6\cdot0.3 = 0.18$

$\alpha_{F:0\to1} = P(F=1)\cdot P(F=0) = 0.1476$

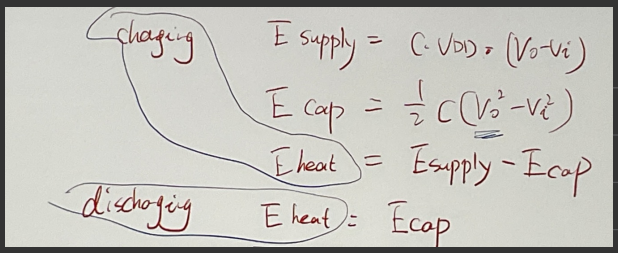
$P_{sw,F} = 0.1476\cdot20f\cdot1\cdot(1-0.2)\cdot100M$

P(F = 1) = 0.18

$\alpha_{F:0\to1}$ = 0.1476

$P_{sw,F}$ = $2.3616\cdot10^{-7}$ W

$\alpha\cdot C\cdot V_{DD}\cdot(V_{DD} - V_{th})\cdot f$



@ Node X

charging $E_{supply} = 10f \cdot 1 \cdot (1-0) = 10fJ$

$E_{cap} = \frac{1}{2} \cdot 10f \cdot (1^2 - 0^2) = 5fJ$

$E_{heat} = 10fJ - 5fJ = 5fJ$

Discharging $E_{heat} = 5fJ$

@ Node Y

charging $E_{supply} = 10f \cdot 1 \cdot (1-0) = 10fJ$

$E_{cap} = \frac{1}{2} \cdot 10f \cdot (1^2 - 0^2) = 5fJ$

$E_{heat} = 10fJ - 5fJ = 5fJ$

Discharging $E_{heat} = 5fJ$

@ Node L

charging $E_{supply} = 20f \cdot 1 \cdot (1.02-0) = 16fJ$

$E_{cap} = \frac{1}{2} \cdot 20f \cdot (0.8^2 - 0^2) = 6.4fJ$

$E_{heat} = 16fJ - 6.4fJ = 9.6fJ$

Discharging $E_{heat} = 6.4fJ$

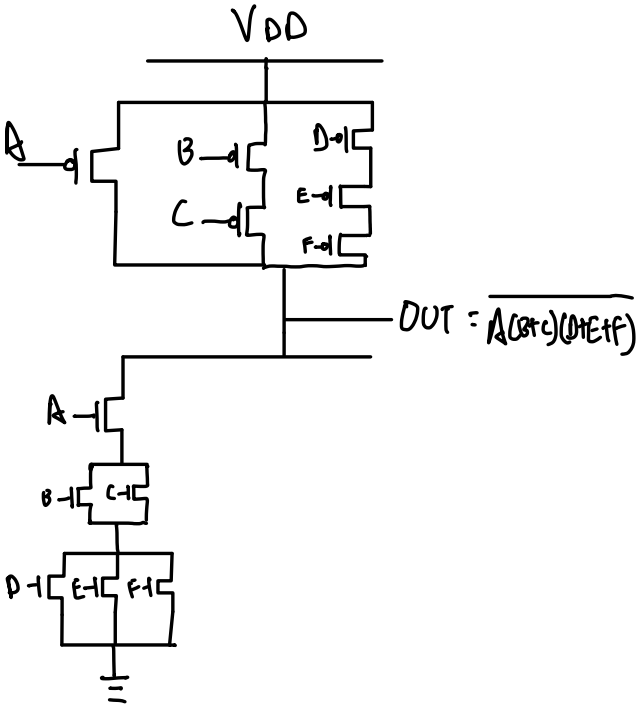
(c) Calculate the heat energy dissipation for charging and discharging C_X, C_Y, and C_L.

Heat Energy	Charging	Discharging
Node X (C_X)	5f J	5f J
Node Y (C_Y)	5f J	5f J
Node F (C_L)	9.6fJ	6.4fJ
Total E_{heat}	19.6fJ	16.4fj

<u>Problem 3:</u> CMOS Logic and Delay

(a) Implement the following function using static CMOS logic.
$F = \overline{A(B+C)(D+E+F)}$

(b) Assume output load capacitance C_L = 50 fF, and that transistors are sized such that the on-resistance of NMOS R_N = 12 kΩ, on-resistance of PMOS R_P = 24 kΩ. Calculate the **worst-case** low-to-high propagation delay t_{pLH} and the **best-case** high-to-low delay t_{pHL}. Assume ideal step-input switching.



Worst t_{pLH} = $8.28 \cdot 10^{-10}$s

Best t_{pHL} =

$t_{pLH} = 0.69 \cdot 3R_P \cdot C_L = 0.69 \cdot 24k \cdot 50f = 2.48 \cdot 10^{-9}$s

when there three PMOS A = 0, B or C = 0 and D or E or F = 0

$t_{pHL} = 0.69 \cdot 3R_N \cdot C_L = 0.69 \cdot 12k \cdot 50f$

$= 1.242 \cdot 10^{-9}$s

we need A = 1
B or C = 1
D or E or F = 1
to go low