A [your delay] $FO4_{(1V)}$, [your energy] $E_{u(1V)}$ 4-bit Absolute-Value Detector

Names

Definitions:

Unit delay = $FO4_{(1V)}$ -- inverter delay at Vdd = 1V

Unit energy = $E_{u(1V)}$ -- energy associated with 1x inverter Cgate at Vdd = 1V

If you scale Vdd, include the effect on delay and energy

Design Summary

Week 5

Week 7

- **1a) Circuit topology, 1b) Circuit Style**
  (e.g. Ripple –carry Adder + Comparator, static CMOS)
  - 1c) justify your selection of (A) and (b)
    (e.g. moderate Area, fast, regular design)
- **Sizing + Vdd optimization / Sizing impact [see slide 13]:**
  - Delay increase: [] % (out of 50%) | Energy reduction: [] %
- **Sizing + Vdd optimization / V_{DD} impact [see slide 13]:**
  - Delay increase: [] % (out of 50%) | Energy reduction: [] %

V_{DD}	Critical path delay	Total energy
1 V	$t_{p\_IN\rightarrow OUT}$ = [] $FO4_{(1V)}$	E = [] $E_{u(1V)}$
[] V	$t_{p\_IN\rightarrow OUT}$ = [] $FO4_{(1V)}$	E = [] $E_{u(1V)}$

Identify which IN and OUT pin gives worst-case delay

Circuit Topology and Circuit Style [2 slide

Week 5

Week 7

- **Provide schematic of your circuit**

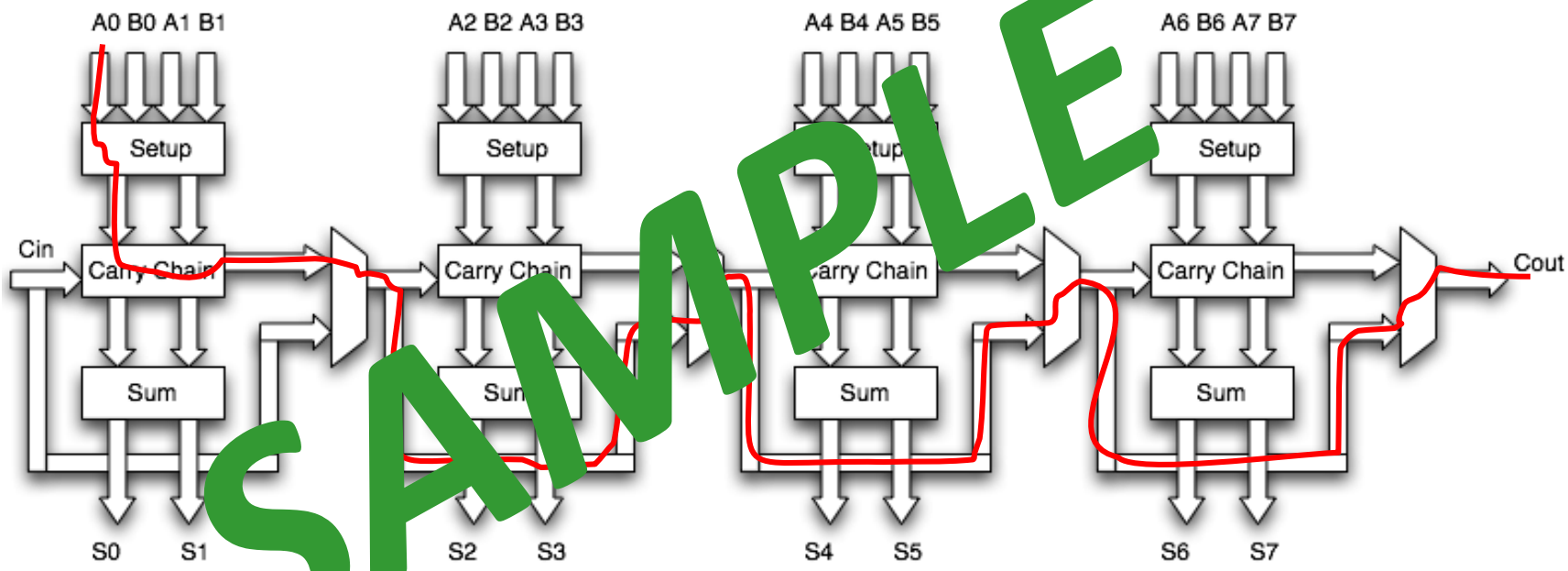
- **Give detailed reasoning about selection of your circuit topology and circuit style**
  - What is unique about your selection of topology and style
  - What other options did you consider and why you discarded them
  - Etc.

Critical Path Analysis [1 slide]

Week 5

Week 7

- **Highlight critical path (w/ input and output bit position)**
  - block diagram of design / crit-path delay equation



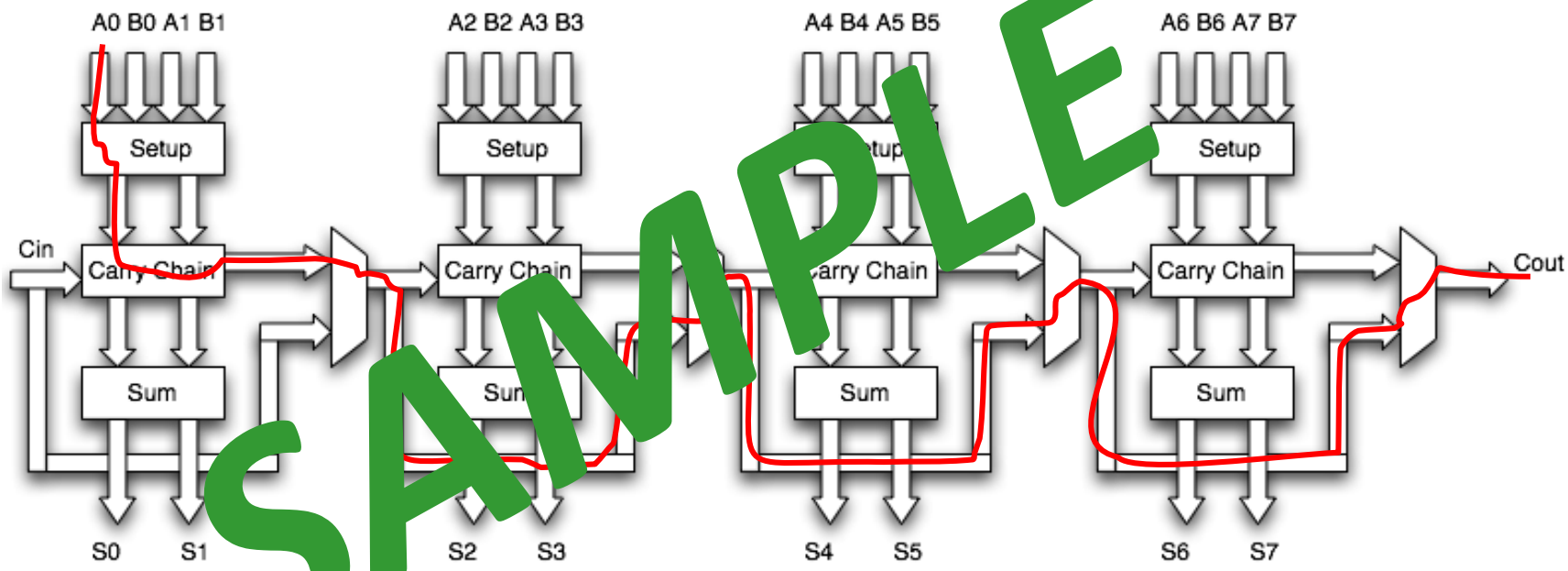
$$t_{critical} = t_{setup} + 2t_{carry} + 4t_{mux}$$

Critical Path Analysis – Delay Model [1 sli

Week 5

Week 7

- **Formulas that you used to model critical-path delay**
  - Write down equation for the full critical path



$$t_{critical} = t_{setup} + 2t_{carry} + 4t_{mux}$$

Sizing vs. V_{DD} Optimization? [1 slide]

Week 6

Week 7

- **How did you decide about relative contribution of sizing and V_{DD} in your overall delay increase?**
  - Explain your decision making process
  - Persuade that your selection is the best available

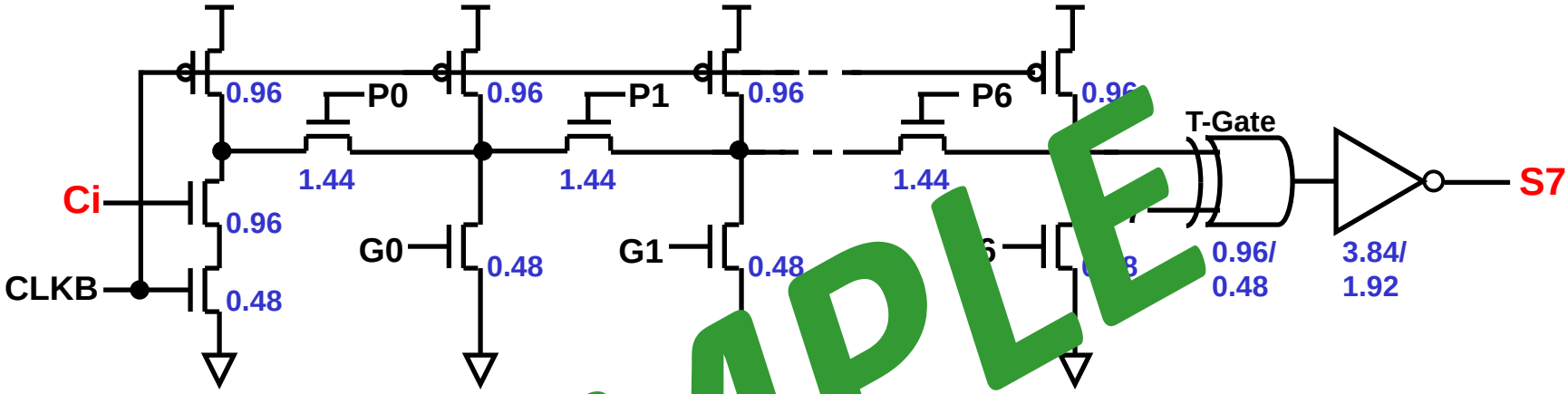
Move on to sizing and V_{DD} optimizations in subsequent slides

Critical Path Gate Sizing Approach [1 slid

Week 6

Week 7

- **Show sizing optimization of the critical path**
  - Indicate sizing on the schematic



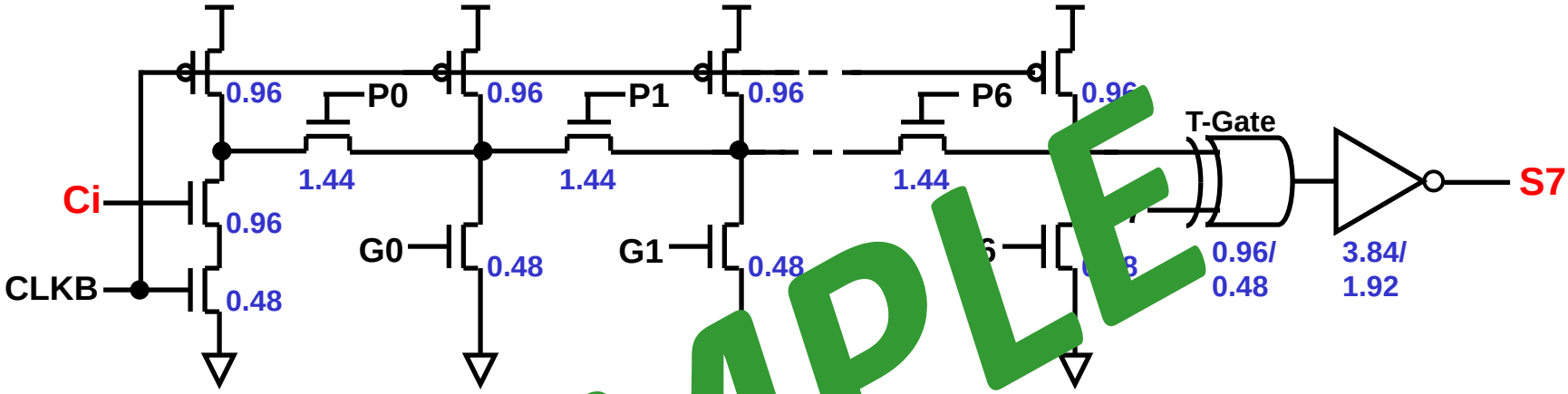
- Propagate $\overline{Carry}$ instead of Carry to reduce transistor count along Manchester chain
- NMOS only pass gates and $\overline{Carry}$ nodes are pre-charged to V_{DD} at CLK=0
- Dynamic logic in Ci inverter and G0:7 AND gates → footless Domino in Manchester chain
- Generate CO and $\overline{CO}$ to incorporate the 4X buffer in signal chain.

Full Sizing Energy Minimization [1-3 slides]

Week 6

Week 7

- Discuss sizing of non-critical paths to minimize energy (add slides as necessary)



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Design Optimization: Supply Voltage [1 sl

Week 6

Week 7

- Show your derivation for V_{DD}^{opt}
- Calculate energy at V_{DD}^{opt}

Any Alternatives You Would Like to Discuss?

Week 7

- If you made significant effort in some alternative design, provide 1-slide summary of your findings

Discussion

Week 7

- **Three most important features of your design**
  - (e.g. Minimum delay through transistors sizing)
  - (e.g. Logic optimization strategy for reduced area)

- **Given another chance, 3 things you would do different**
  - (e.g. Change topology, because…)
  - (e.g. Optimize only last few stages to save design time)
  - (e.g. Nothing, I nailed it down! ;))

11-12 slides + discussion
Each team member to present 3-4 slides

Project Guidance / What to Turn In?

- **Extended Project Abstract: 1 full page**
  - 80% to 100% of full page, 12-pt font, 1.2-line spacing
  - One submission per group
  - Include your project title and your names
  - Document key design techniques, results, and findings
- **Individual Course Reflection: 1 full page**
  - Also 80% to 100% of full page, 12-pt font, 1.2-line spacing
  - Individual submission for each student
  - Reflect on key learning points from the workshop
- **Presentation Slides: each team member has to present**
  - See slides 1-11 of this guide
  - One submission per group

Optimization of Sizing and Vdd Clarified

- **Aim to optimize Sizing and Vdd jointly**
  - Sizing only or Vdd only is suboptimal
- **Useful software tools**
  - MATLAB: fmincon function; Excel: Solver Add-on