Digital Integrated Circuits
Homework #1

Due 2 hours before the next lecture

Problem 1: MOS Transistor – Regions of Operation / Device Parameters

Below is a table showing a set of measurements performed on a newly fabricated MOS transistor. You are convinced that these measurements are correct and a few assumptions will get you the information that you need.

Measurement Number	V_{GS}	V_{DS}	V_{SB}	I_D	Operation Region
1	–0.4 V	–0.8 V	0	–12.05 µA	
2	0.4 V	–0.8 V	0	0.0	
3	–0.8 V	–0.8 V	0	–88.98 µA	
4	–0.5 V	–0.8 V	0	–26.42 µA	
5	–0.4 V	–0.8 V	–0.5V	–7.17 µA	
6	–0.8 V	–0.5 V	0	–76.45 µA	
7	–0.8 V	–0.2 V	0	–53.21 µA	

You may assume that $|V_{DSAT}| = 0.4V$ and $|2\Phi_F| = 0.6V$.

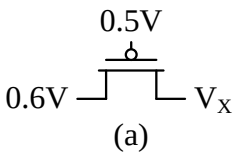
1A Is the measured transistor a PMOS or an NMOS device? Explain your answer.

1B From measurements above, determine the following parameters: V_{T0}, γ, λ.

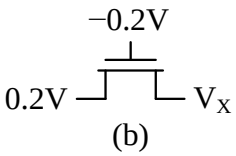
1C Complete the missing column in the table above using the values you obtained in 2B. Fill in either "LINEAR", "CUTOFF", "SATURATION", or "VEL. SATURATION."

Problem 2: MOS Transistor – Regions of Operation

Determine the region of operation for devices (a) and (b) for the V_X values listed in the tables below. If you find that a device is on the boundary of two regions, write both regions in the table. For example, for a device on the boundary of linear and saturation region write (linear/saturation). If a region of operation is not possible, mark the case with DNE (does not exist).



(a)



(b)

Device parameters:
$V_{TN} = 0.2V$, $V_{TP} = -0.2V$
$E_{CN} = 3V/\mu m$, $E_{CP} = 4V/\mu m$
$L_{eff,N} = L_{eff,P} = 70nm$

(continued on next page)

Device (a)

V_X = 0 V	V_X = 0.7 V	V_X = 0.8 V	V_X = 1 V

Device (b)

V_X = 0.5 V	V_X = −0.5 V	V_X = −0.61 V	V_X = −0.7 V

Problem 3: VTC and Inverter Analysis

Figure 3a shows a standard CMOS inverter. However, during the process of manufacturing, the circuit was contaminated with a particle and the gate of the PMOS transistor got shorted to GND instead of being connected to the input. The contaminated inverter circuit could be modeled as shown in Figure 3b.

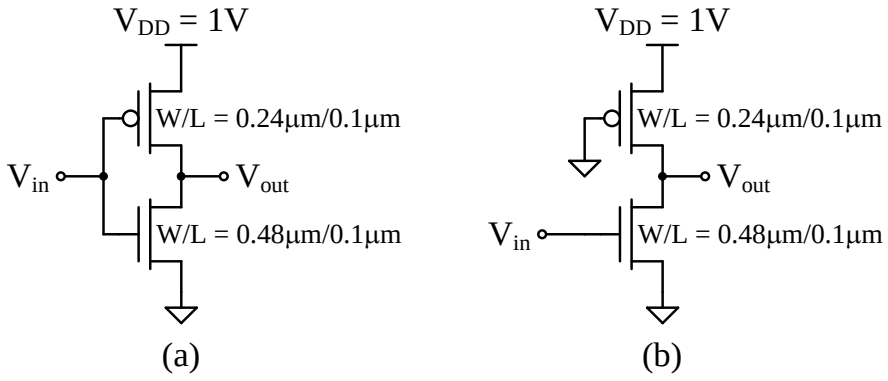


Figure 3: CMOS Inverter.

(*Note:* L indicates drawn channel length, assume x_d = 15nm).

Find $\mathbf{V_{OH}}$, $\mathbf{V_{OL}}$, and $\mathbf{V_M}$ for the inverters in Figures 3a and 3b.
(Don't simply conclude that V_M is $V_{DD}/2$, do some hand calculation)

Use following parameters for hand calculations:

V_{DD} = 1.0V, V_{DSAT} = 0.3V for NMOS, and V_{DSAT} = −0.4V for PMOS
NMOS: V_{T0} = 0.17V, k_n' = 130μA/V^2, γ = 0.1V$^{1/2}$, λ = 0.75V^{-1}, $2\Phi_F$ = 0.6V
PMOS: V_{T0} = −0.20V, k_p'= −100μA/V^2, γ= −0.16V$^{1/2}$, λ= −0.62V^{-1}, $2\Phi_F$ = −0.6V