

Digital Integrated Circuits Workshop

Week 1:
Course Introduction,
History of Digital ICs, and MOS IV Model



Prof. Dejan Markovic
UCLA

Week 1 Agenda

- ◆ Course Introduction
- ◆ History of Digital ICs
- ◆ MOS IV Model

Introductions: Prof. Dejan Markovic



Dejan Marković is a Professor of Electrical and Computer Engineering at the University of California, Los Angeles, and a co-director of Center for NeuroTechnology (CENT). He completed the Ph.D. degree in 2006 at the University of California, Berkeley, for which he was awarded 2007 David J. Sakrison Memorial Prize.

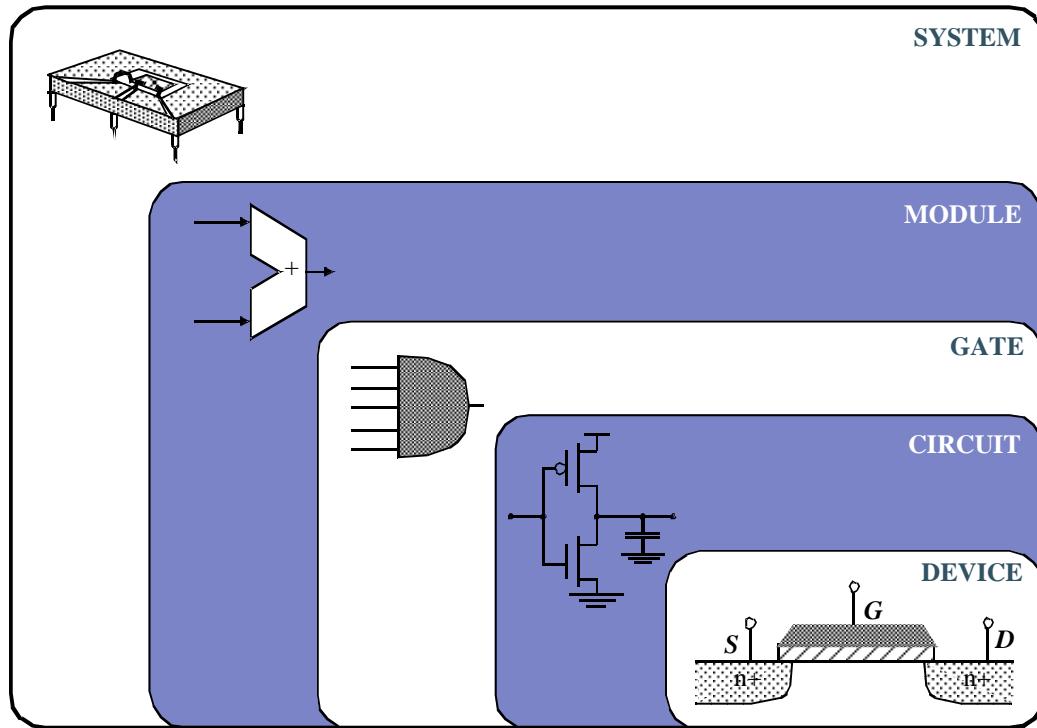
His research includes implantable neuromodulation systems, domain-specific computing, and design methodologies. Dr. Marković co-founded Flex Logix Technologies, a semiconductor IP startup, in 2014, and is involved in several medical device startups.

Prof. Marković received an NSF CAREER Award in 2009. In 2010, he was a co-recipient of ISSCC Jack Raper Award for Outstanding Technology Directions. In 2014, he received ISSCC Lewis Winner Award for Outstanding Paper.

Introductions: Students

- ◆ Please introduce yourself
- ◆ Educational background
- ◆ Motivation to take this course
- ◆ Learning objective for this course
- ◆ Next steps and career plans

Digital Design: Abstraction Levels



This course is about circuit and gate-level design, with device models needed for circuits & gates

Schedule and Syllabus

Weeks 1-7: IC Design	
1	Intro and MOS IV Model
2	Inverter VTC and MOS RC Model
3	Delay and Power Models, CMOS Scaling
4	CMOS and PTL Logic, Gate Sizing
5	Logical Effort Theory
6	Review, Project Status
7	Project Presentations



- ◆ **This is a level-1 course** (undergrad)
- ◆ **Level-2 course: VLSI Design** (advanced undergrad, lower grad)
- ◆ **Level-3 course: Design Optimization** (advanced-1 grad)
- ◆ **Level-4 course: VLSI Signal Processing** (advanced-2 grad)

Grading Policy & Organization

30% ♦ Homework (4)

20% ♦ Project slides

20% ♦ Oral presentation

20% ♦ Project abstract

10% ♦ Participation

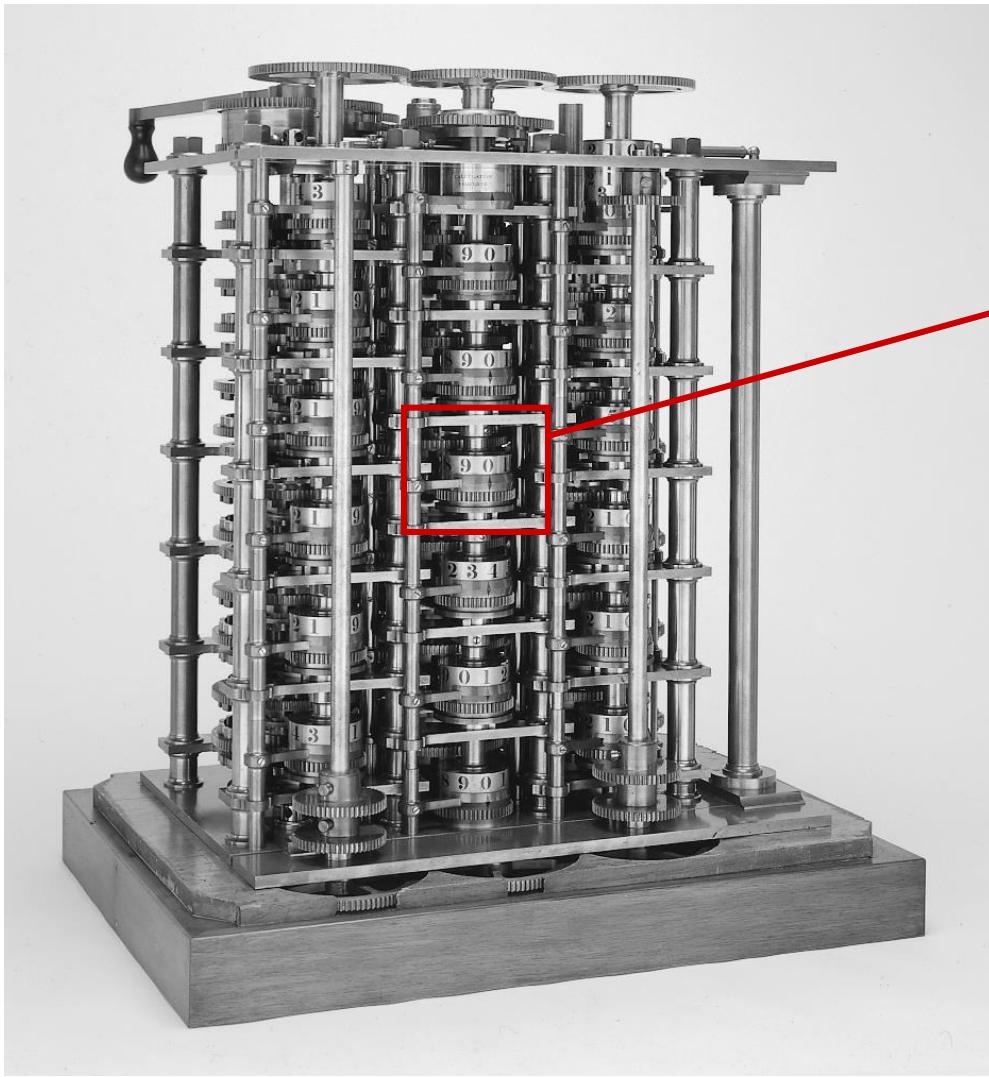
Schedule of Assignments

Week	1	2	3	4	5	6	7
Hw #1							
Hw #2							
Hw #3							
Hw #4							
Hw #5							
Project							

Week 1 Agenda

- ◆ Course Introduction
- ◆ History of Digital ICs
- ◆ MOS IV Model

A Bit of History... The First Computer (1832)

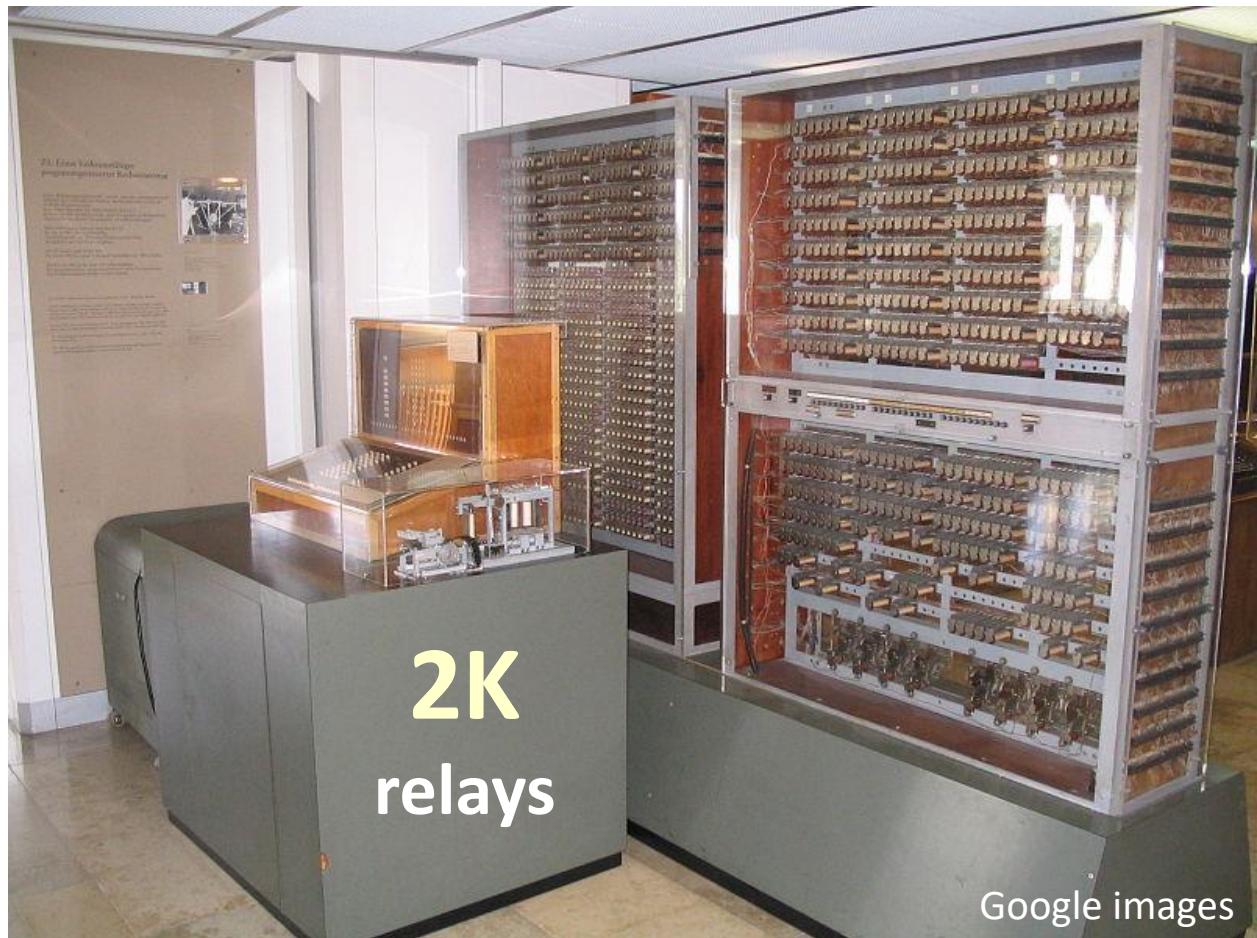


- ◆ **The Babbage Difference Engine**
 - 25,000 parts
 - cost: £17,470

The First Digital Electronic Computer

Zuse Z3
(1941)

Binary
5 – 10 Hz
22b words

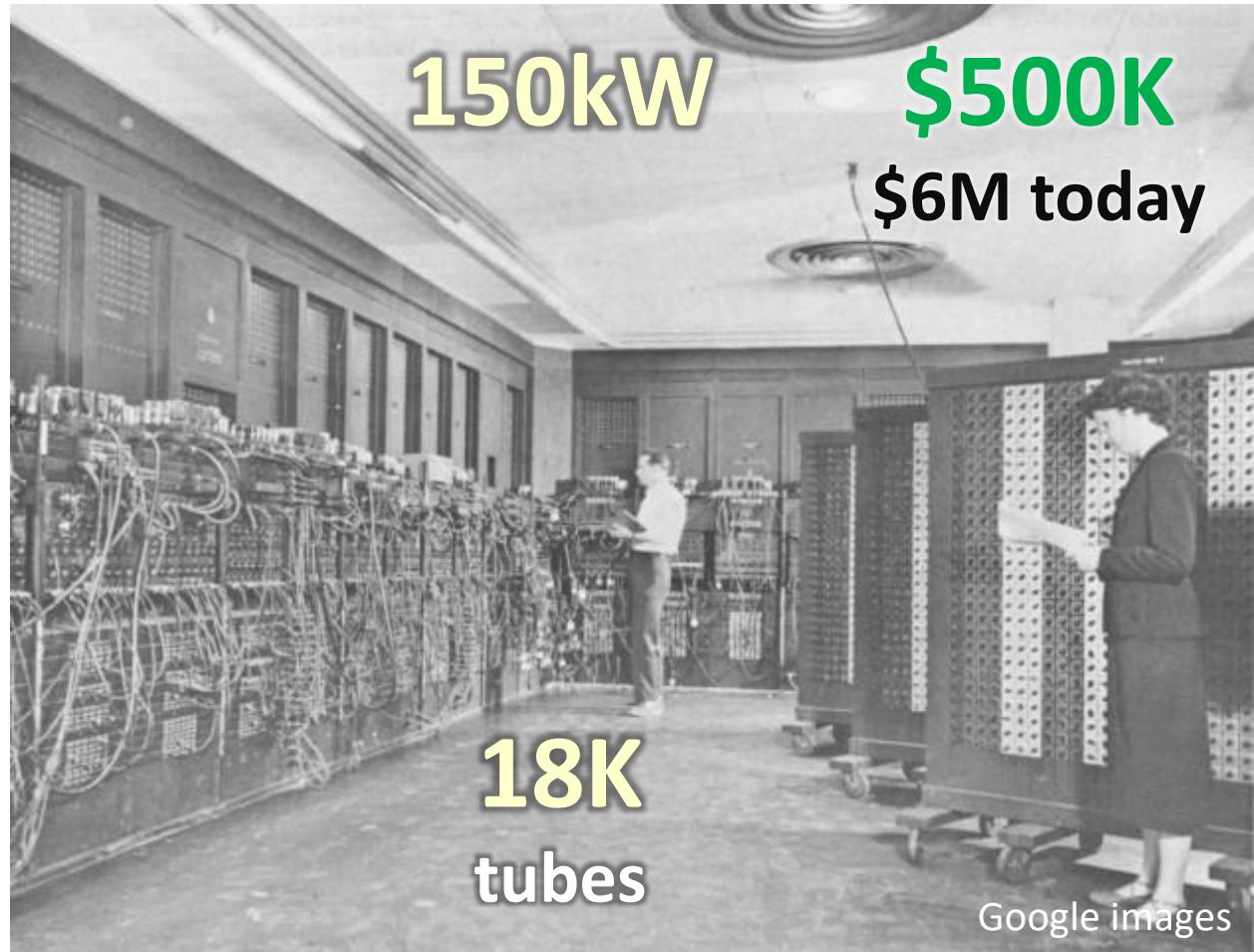


Device: Electromechanical relay

Five Years Later

ENIAC
(1946)

Decimal
5M joints
hand-soldered



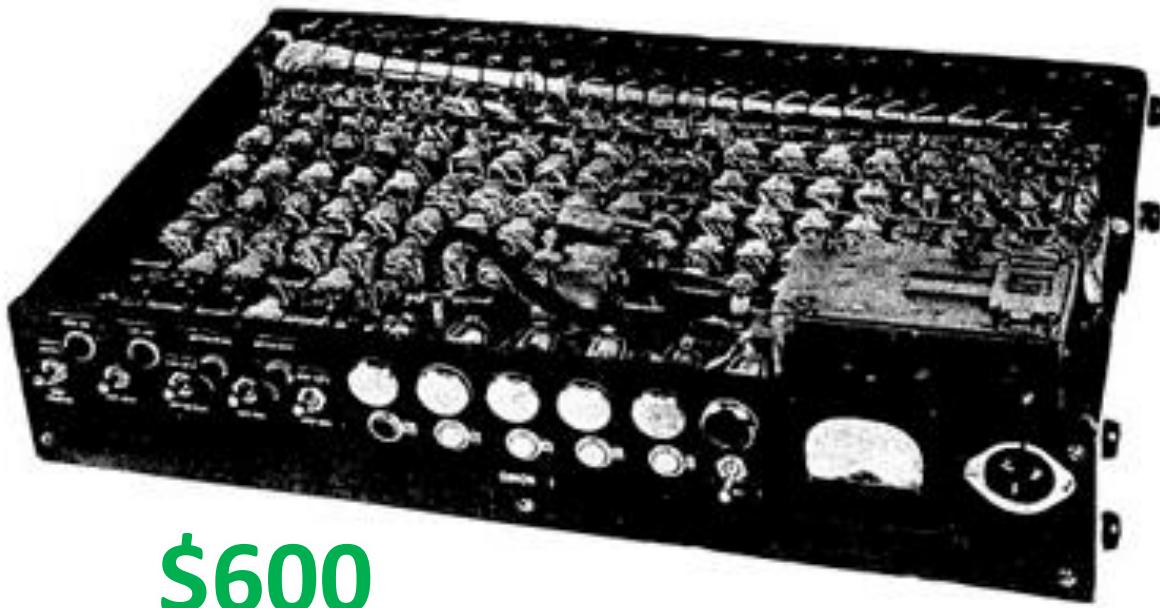
Device: **Vacuum tube**

The First PC

Simon
(1950)

4 ops:
 $+$, $-x$, $>$, S
2b Reg/ALU

\$600



Google images

Device: Electromechanical relay

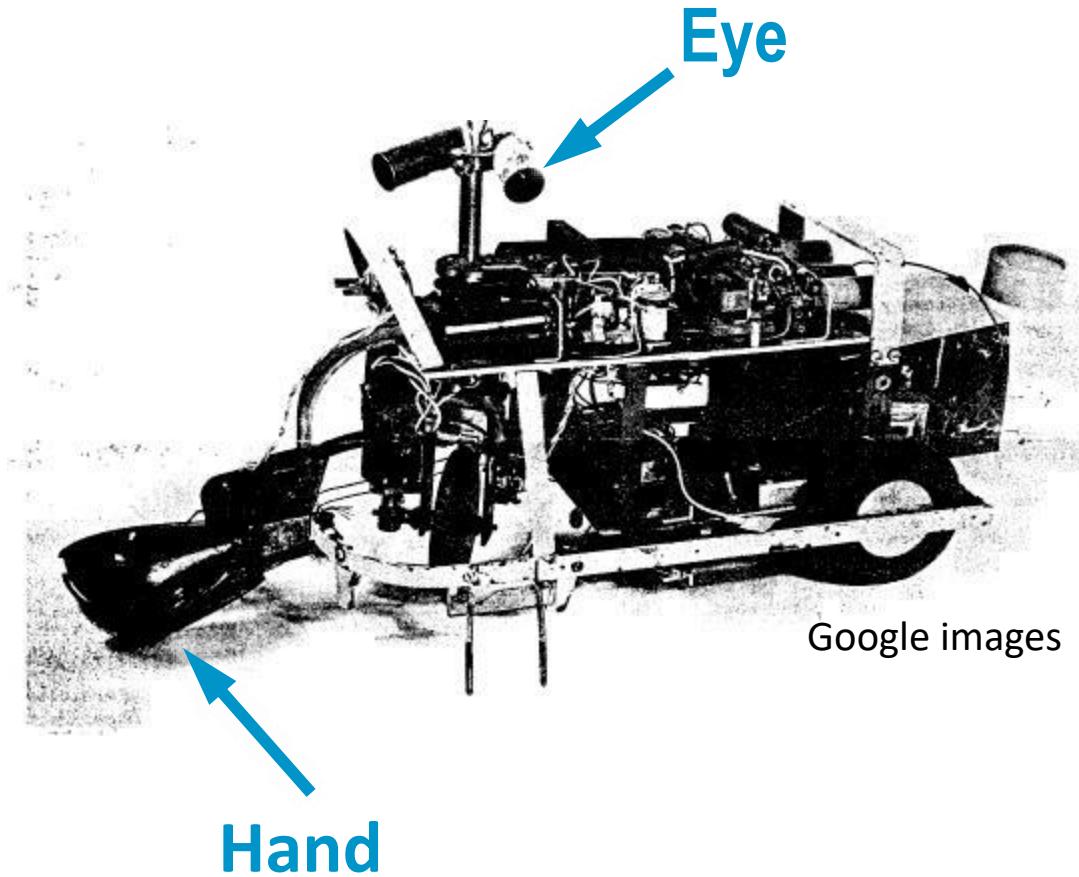
What is the Machine's Future?

Mr. Berkeley's answer:

"Simon has *two futures*. In first place Simon can *grow*. With another chassis and some wiring and engineering, the machine will be able to compute decimaly. Perhaps in six months more, we may be able to have it working on real problems. In the second place, Simon may start a fad of building *baby mechanical brains*, similar to the hobby of building crystal radio sets that swept the country in the 1920's."

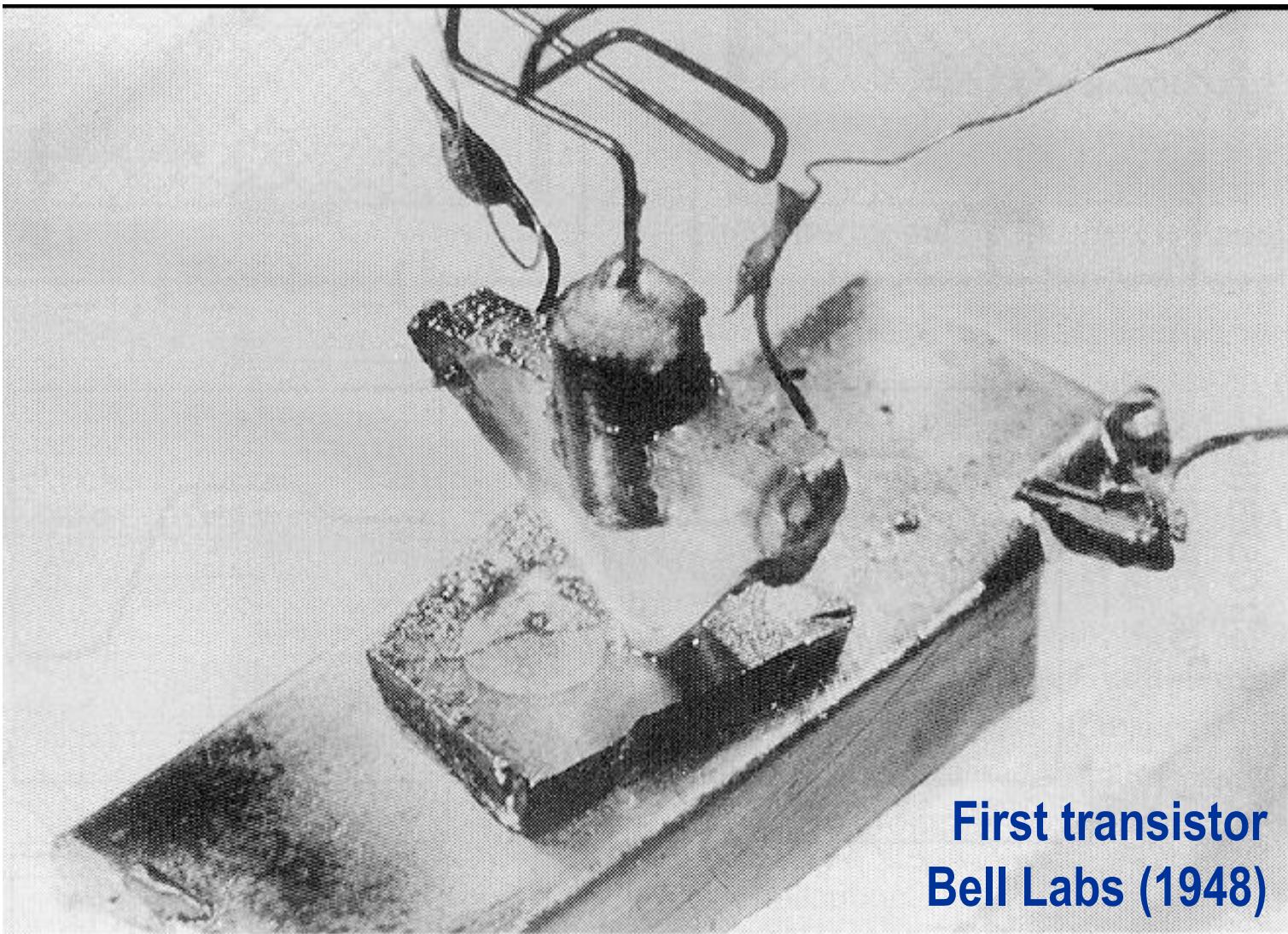
[1956 Berkeley Enterprises Report]

Squee (The Electronic Robot Squirrel)



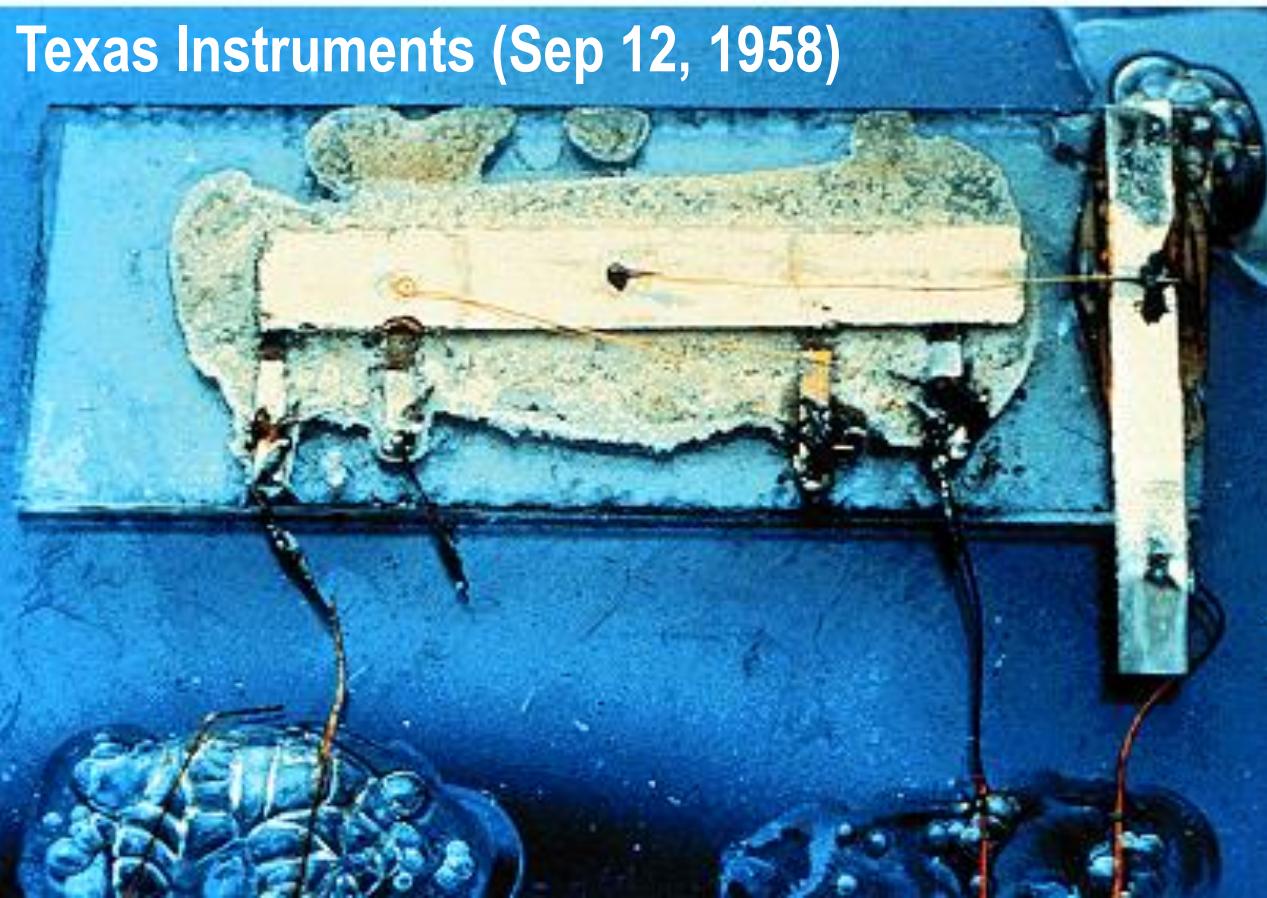
[1956 Berkeley Enterprises Report]

The Transistor Revolution (1948)



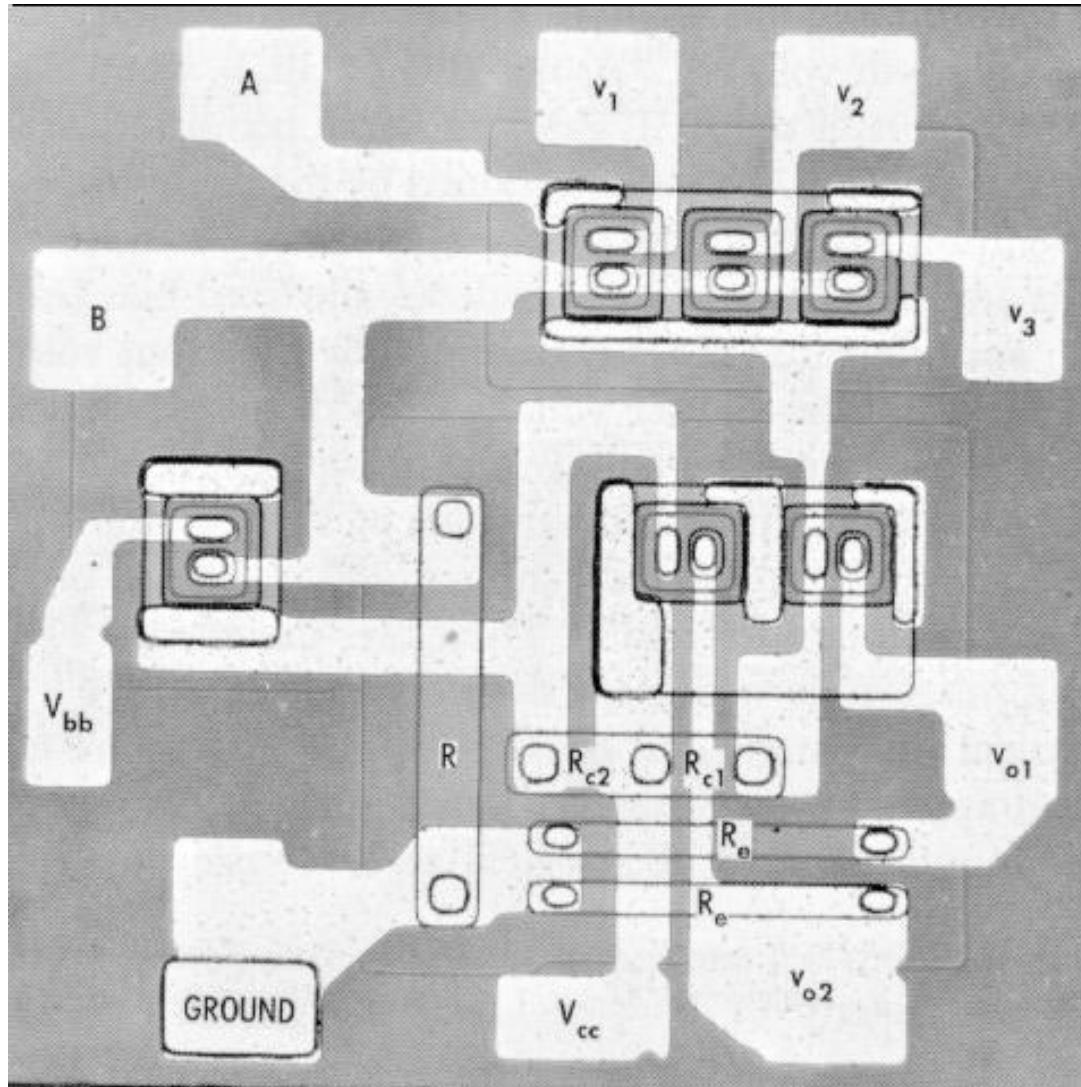
First transistor
Bell Labs (1948)

The First Integrated Circuit (1958)



7/16" wide and containing two transistors, mounted on a bar of germanium
(Image courtesy of Texas Instruments, Inc.)

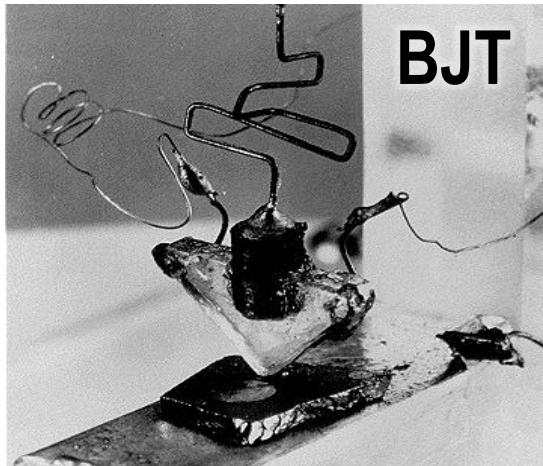
The First Integrated Circuits (1960's)



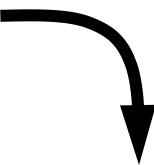
Bipolar logic
(1960's)

ECL 3-input Gate
Motorola (1966)

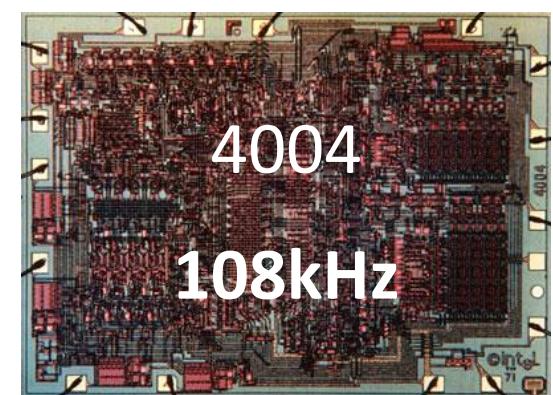
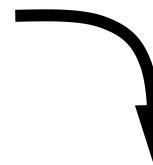
Integrated Electronics



1948 (Bell Labs)

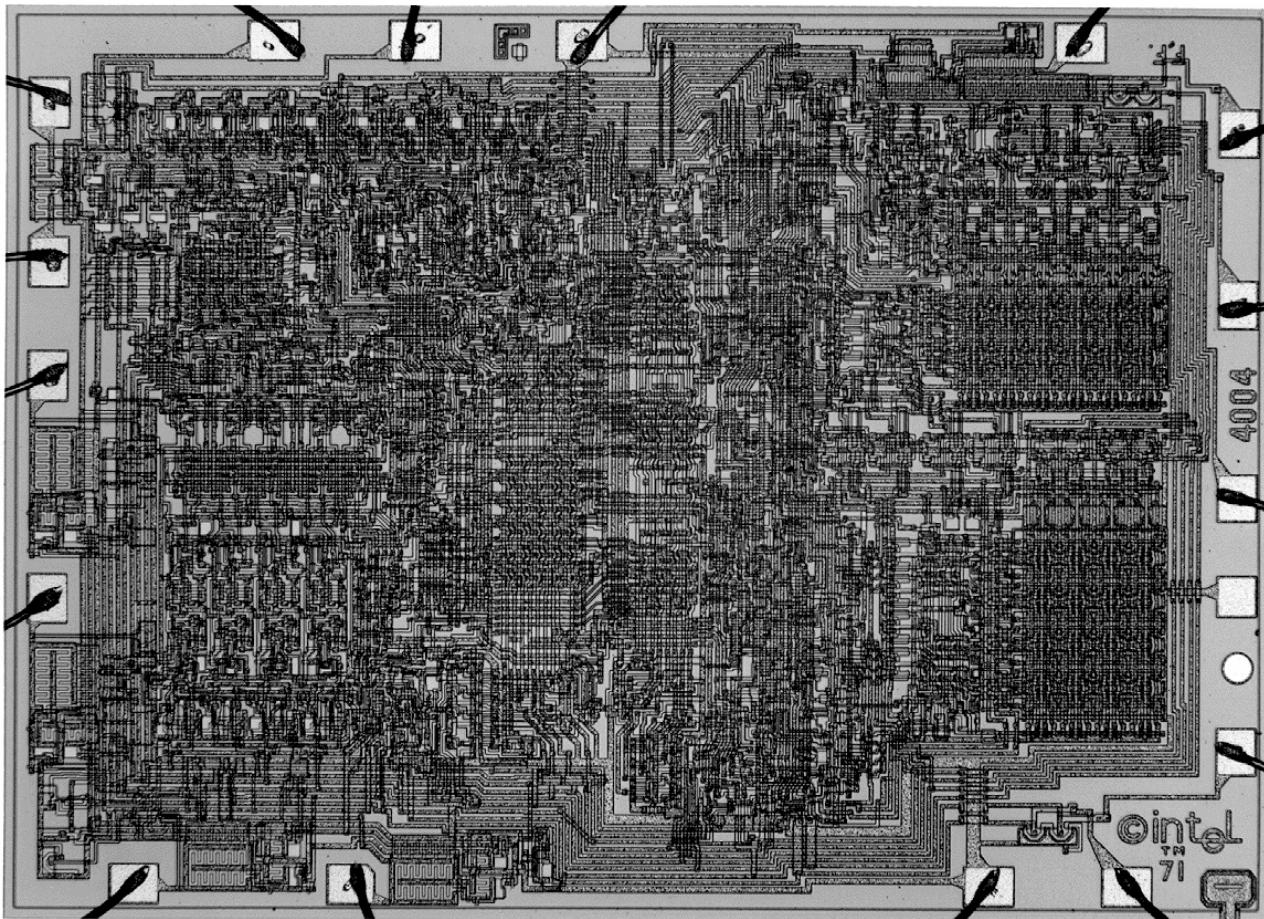


1958 (TI)



1971 (Intel)

Intel 4004 Microprocessor (1971)

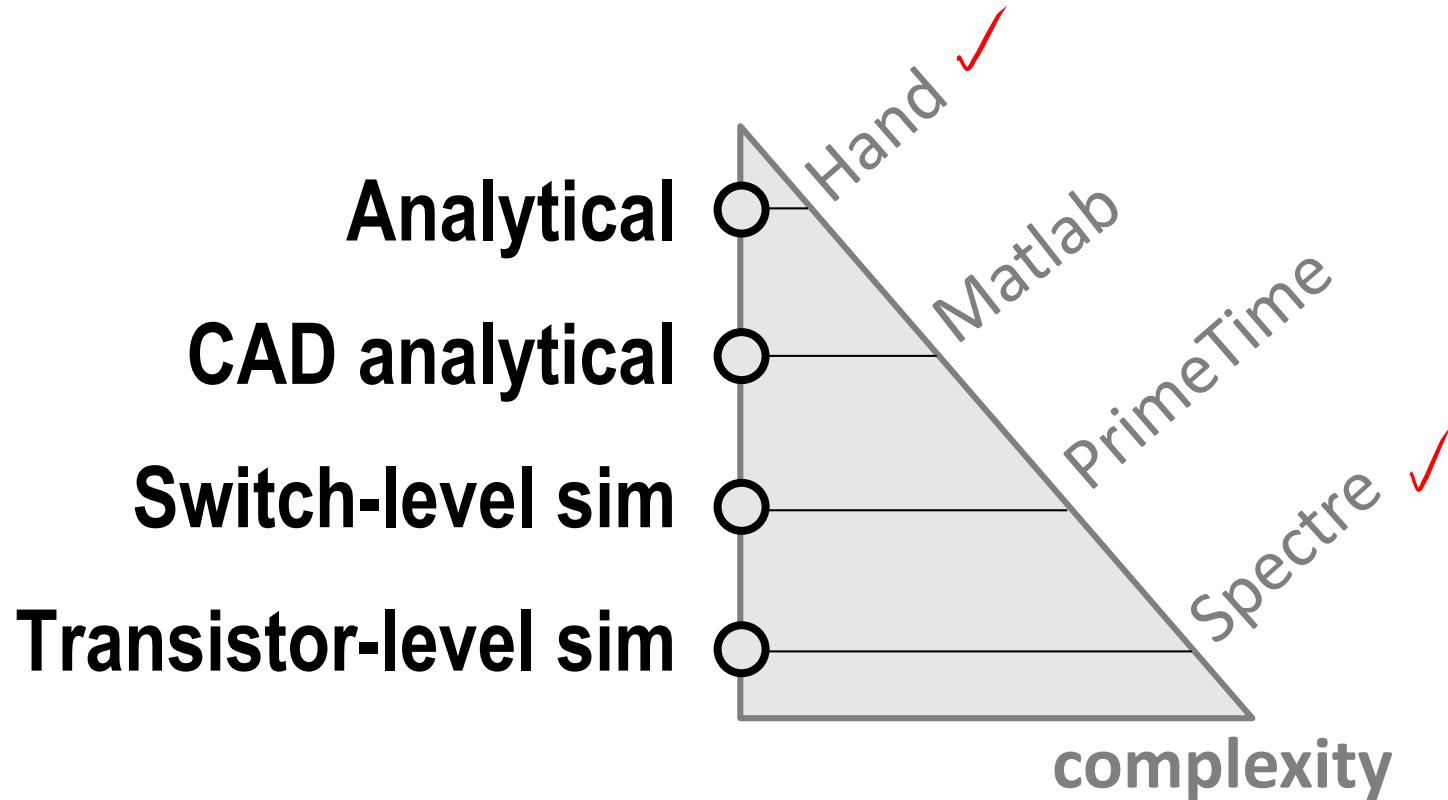


**2,300 transistors (12mm²)
108 KHz operation (10μm)**

Week 1 Agenda

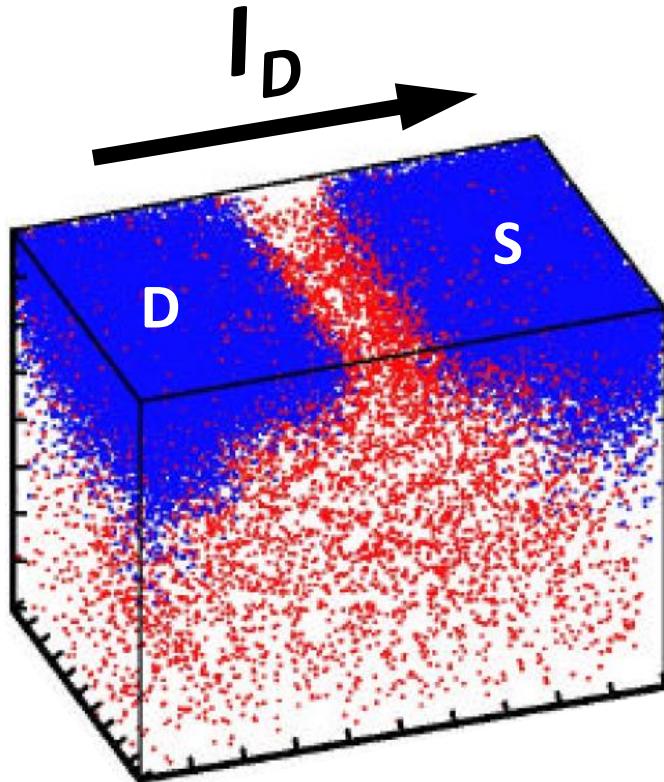
- ◆ Course Introduction
- ◆ History of Digital ICs
- ◆ MOS IV Model

Levels of Modeling



Different **complexity, accuracy, speed of convergence...**

MOS Transistor Modeling

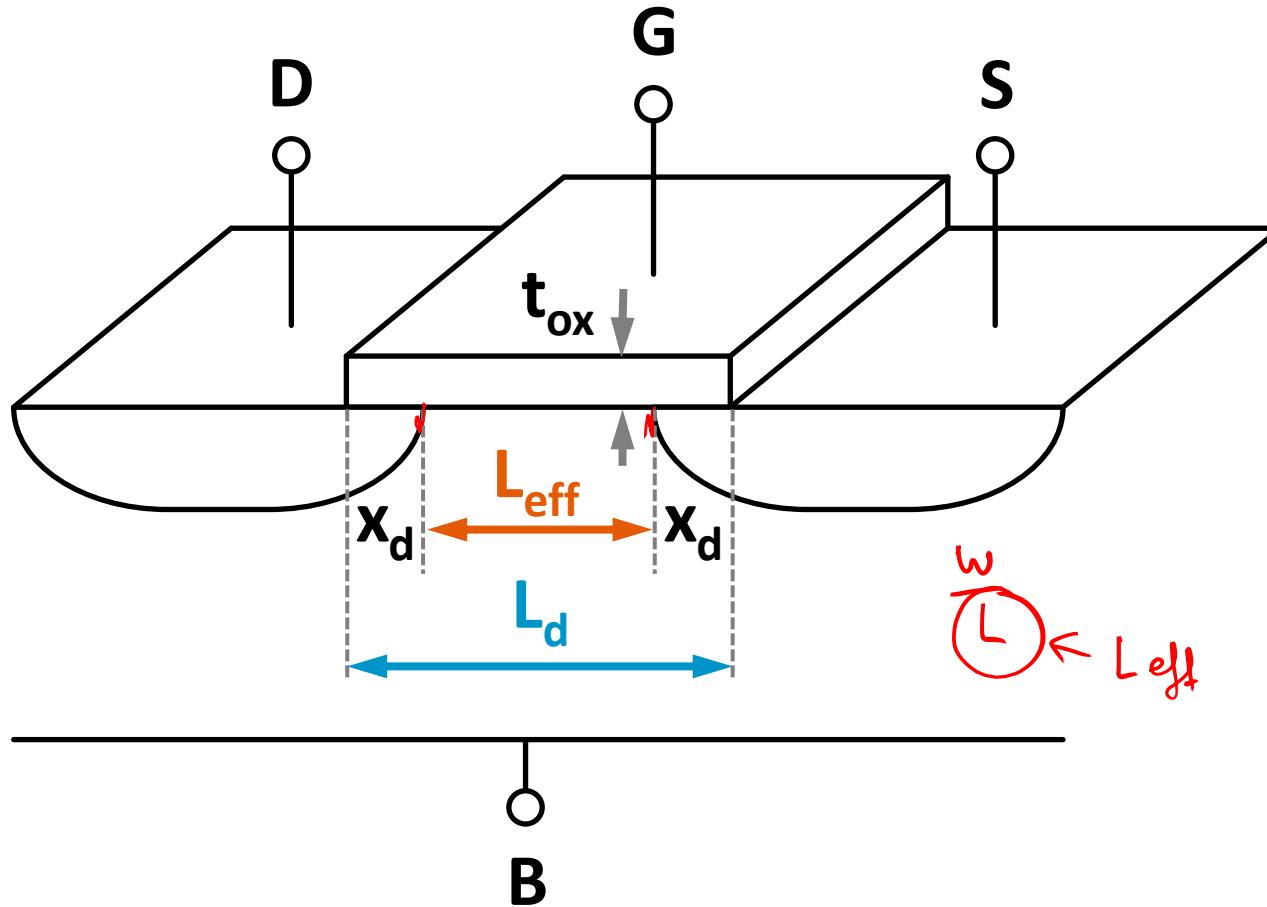


**Our goal is to model
delay and energy**

not current

**But have to start
with current**

MOSFET, Notations



Hand-analysis I-V formulas:

$$L = L_{eff}$$

Important Concepts to Understand

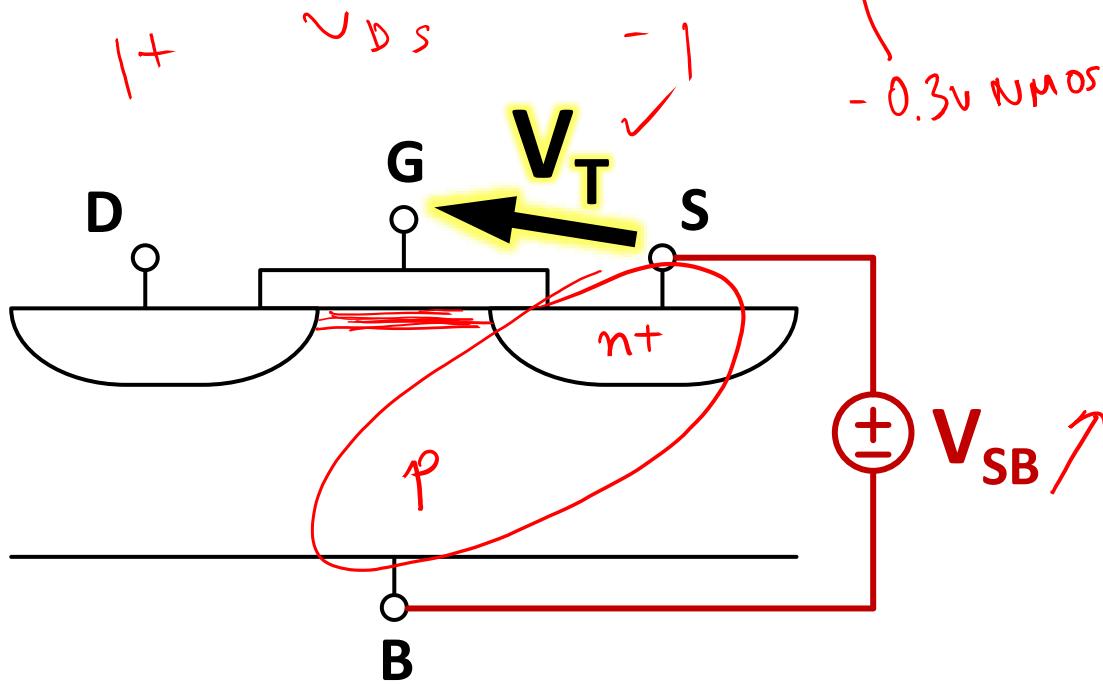
- ◆ Threshold voltage (V_T)
- ◆ Velocity saturation
- ◆ Channel length modulation (channel pinch-off)

Threshold Voltage, V_T

$$V_{SB} = 0$$

V_{T0} is approx 0.2V for our process

$$V_T = V_{T0} + \gamma \cdot (\sqrt{| - 2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$$



NMOS:

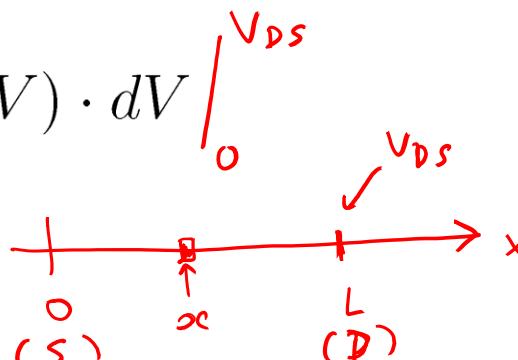
- ◆ $V_{SB} > 0$ (RBB)
- ◆ $V_{SB} < 0$ (FBB)

PMOS:

- ◆ $V_{SB} > 0$ (FBB)
- ◆ $V_{SB} < 0$ (RBB)

The Drain Current in Linear Regime

- Combining velocity and charge:

$$I_D \cdot dx = \mu_n \cdot C_{ox} \cdot W \cdot (V_{GS} - V_T - V) \cdot dV$$


A hand-drawn diagram of a MOSFET channel. A horizontal line represents the channel, with a vertical tick mark at its center labeled 'x'. The left end is labeled '(S)' and the right end is labeled '(D)'. Above the channel, a red arrow labeled 'V_{DS}' points from left to right, indicating the drain-to-source voltage. The total length of the channel is labeled 'L'.

- Integrating over the channel:

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$k'_n \quad k_n$$

Transconductance: $k'_n = \mu_n \cdot C_{ox}$

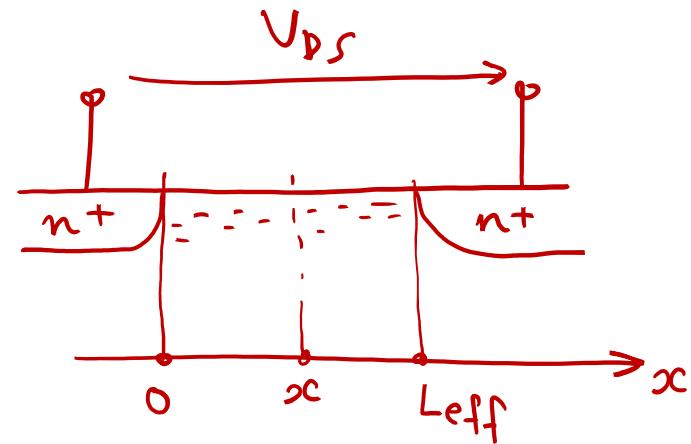
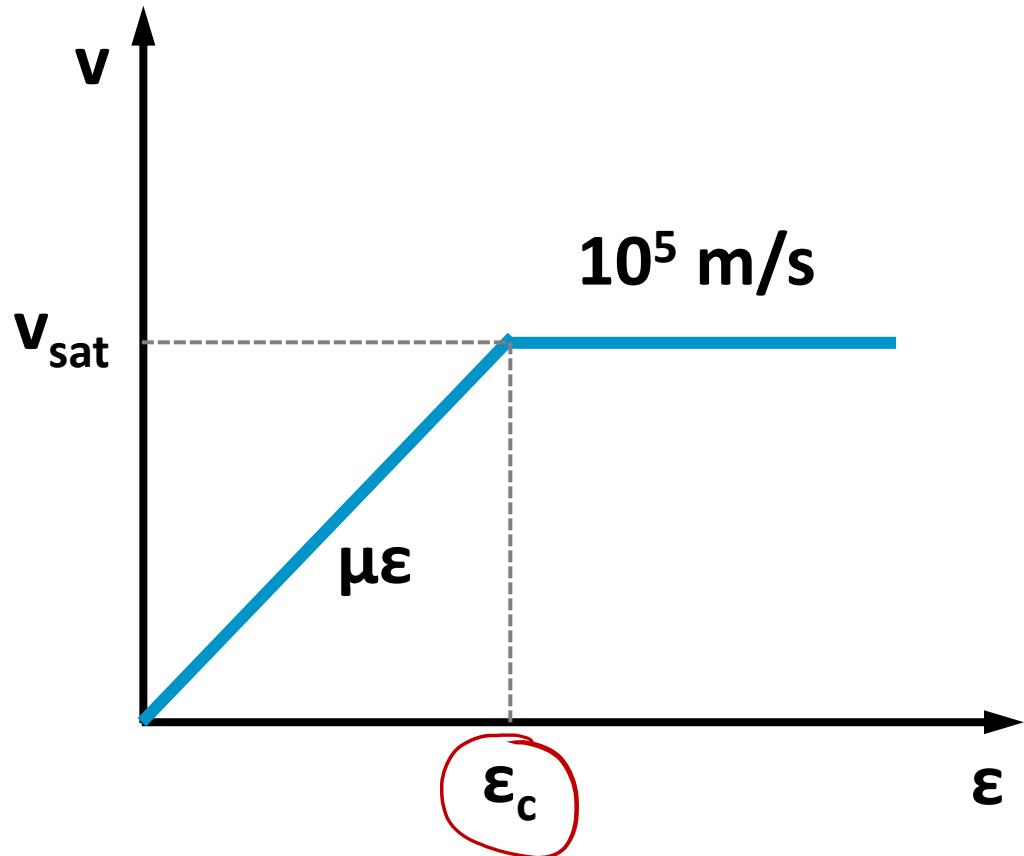
Gain factor: $k_n = k'_n \cdot \frac{W}{L}$

Small $V_{DS} \rightarrow$ ignore quadratic term \rightarrow linear V_{DS} dependence

L = effective L = $L_d - 2x_d$

Velocity Saturation

- Carrier velocity saturates when critical field is reached

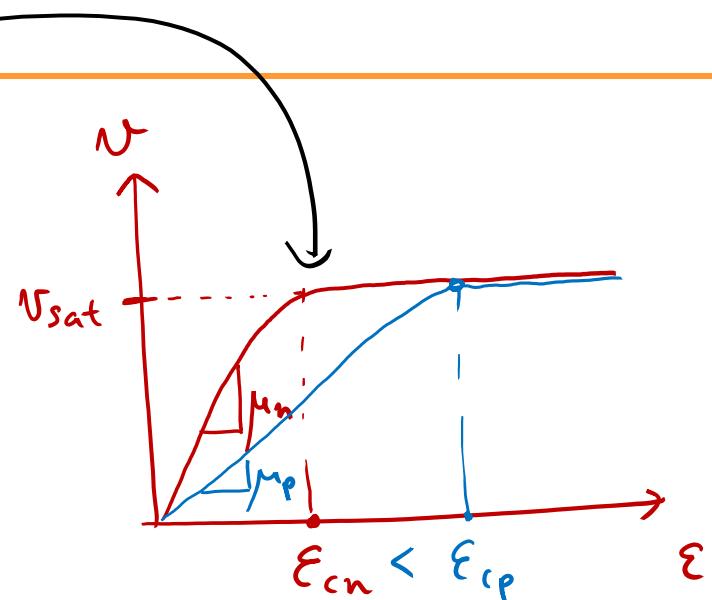


$$\epsilon = \frac{V_{DS}}{L_{eff}}$$

Simple Model

$$V_n = \frac{\mu \varepsilon}{1 + \varepsilon/\varepsilon_c}, \quad \varepsilon \leq \varepsilon_c$$

$$V_n = V_{sat}, \quad \varepsilon \geq \varepsilon_c$$



Continuity @ $\varepsilon = \varepsilon_c$

$$\Rightarrow V_{sat} = \frac{\mu_n \cdot \varepsilon_c}{2}$$

$$V_n^{sat} = V_p^{sat}$$
$$\varepsilon_{cn} < \varepsilon_{cp}$$

A More General Model

- ◆ Approximate velocity:

$$v_n = \frac{\mu_n \cdot \xi}{1 + \xi/\xi_c}$$
 for $\xi \leq \xi_c$
 $v_n = v_{sat}$ for $\xi \geq \xi_c$

- ◆ And integrate current again:

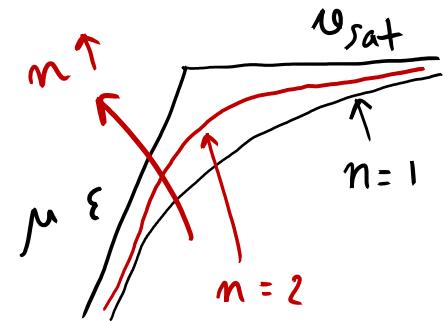
$$I_D = \frac{\mu_n \cdot C_{ox}}{1 + \frac{V_{DS}}{\xi_c \cdot L}} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$\epsilon = \frac{V_{DS}}{L} \frac{\mu n}{1 + \epsilon/\epsilon_c}$

A more general model:

$$v_n = \frac{\mu_n \cdot \xi}{(1 + (\xi/\xi_c)^n)^{1/n}}$$

we use $n = 1$



In **deep submicron**, there are four regions of operation:

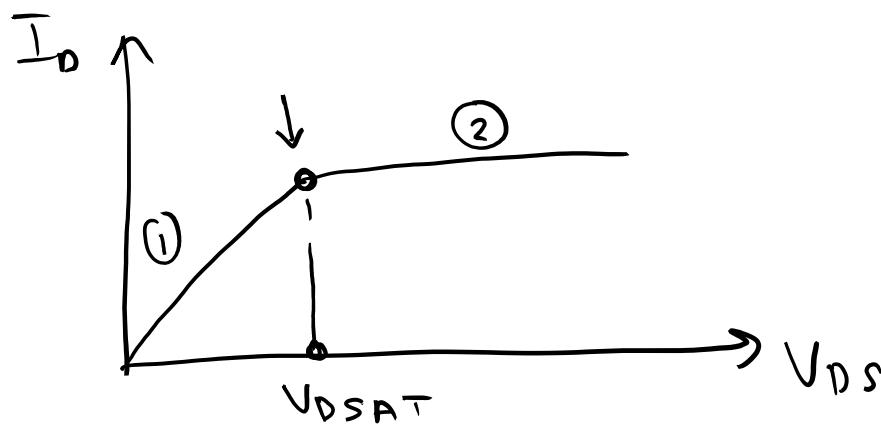
(1) cutoff, (2) resistive, (3) saturation and (4) **velocity saturation**

linear

Including Velocity Saturation in the I_D Formula

① $I_D = \frac{Mn \cdot Cox}{1 + \frac{V_{DS}}{\epsilon_c \cdot L}} \frac{W}{L} \left[\underbrace{(V_{GS} - V_T) \cdot V_{DS}}_{V_{GT}} - \frac{V_{DS}^2}{2} \right] = I_{DSAT}$ @ $V_{DS} = V_{DSAT}$

② $I_{DSAT} = V_{sat} \cdot Cox \cdot W [V_{GS} - V_T - V_{DSAT}]$
 ↑ $\frac{Mn \epsilon_c}{2}$ (continuity of $V(\epsilon)$ model)



Calculating Velocity Saturation, V_{DSAT}

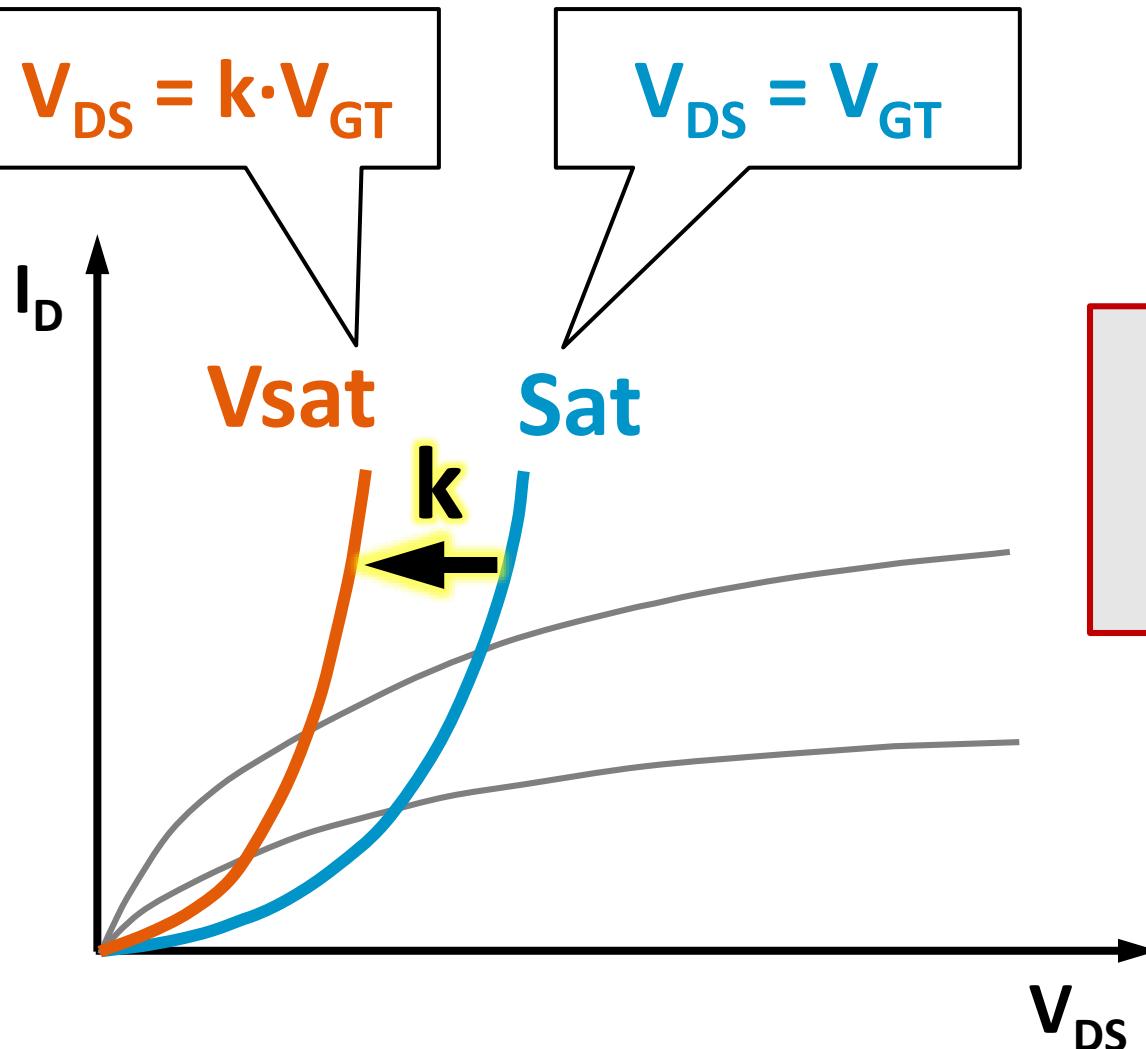
$$\textcircled{1} = \textcircled{2} \Rightarrow \cancel{\frac{\mu_n \epsilon_c}{2} C_{ox} \cdot W \cdot (V_{GT} - V_{DSAT})} = \cancel{\frac{\mu_n C_{ox}}{L}} \cancel{W} \left[V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2} \right]$$
$$1 + \frac{V_{DSAT}}{\epsilon_c \cdot L}$$

$$\left(\frac{\epsilon_c \cdot L}{2} + \frac{V_{DSAT}}{2} \right) (V_{GT} - V_{DSAT}) = V_{GT} \cdot V_{DSAT} - \frac{V_{DSAT}^2}{2}$$

$$\frac{\epsilon_c \cdot L}{2} V_{GT} - \frac{\epsilon_c \cdot L}{2} V_{DSAT} - \frac{V_{GT} \cdot V_{DSAT}}{2} = 0$$

$$K(V_{GT}) = \frac{1}{1 + \frac{V_{GT}}{\epsilon_c \cdot L}} < 1$$
$$V_{DSAT} = \frac{V_{GT}}{1 + \frac{V_{GT}}{\epsilon_c \cdot L}} = \underbrace{K(V_{GT}) \cdot V_{GT}}_{< 1} < V_{GT} - V_T$$

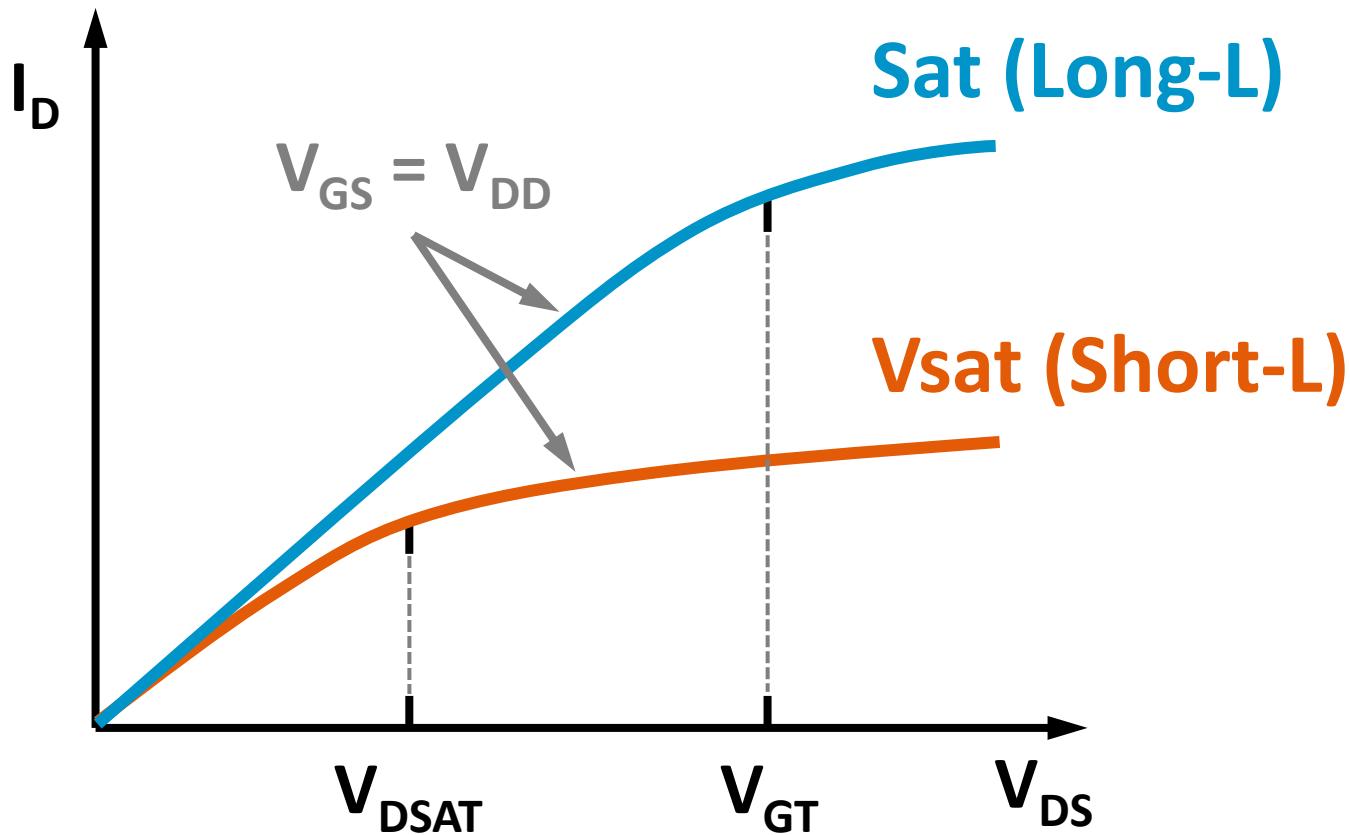
V_{sat} Occurs at LOWER V_{DS} than Sat



$$k = \frac{1}{1 + \frac{V_{GT}}{\epsilon_c \cdot L}}$$

$$k = k(V_{GT})$$

V_{sat} : Less Current for Same V_{GS}

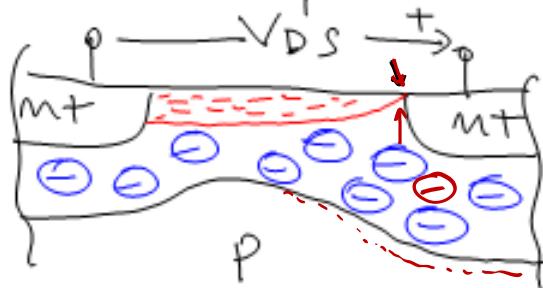


Channel Length Modulation (CLM)

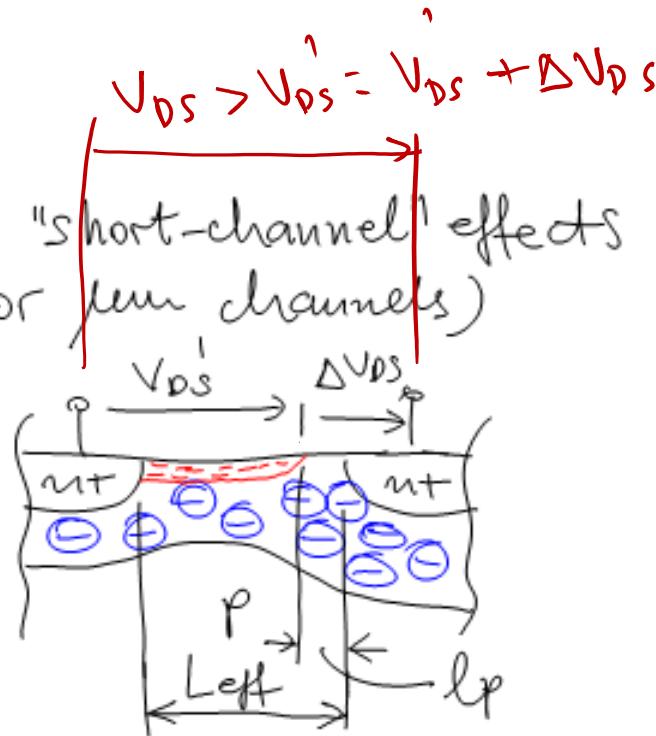
◆ Channel pinch-off

CLM

one of the first "short-channel" effects
(also noticeable for long channels)

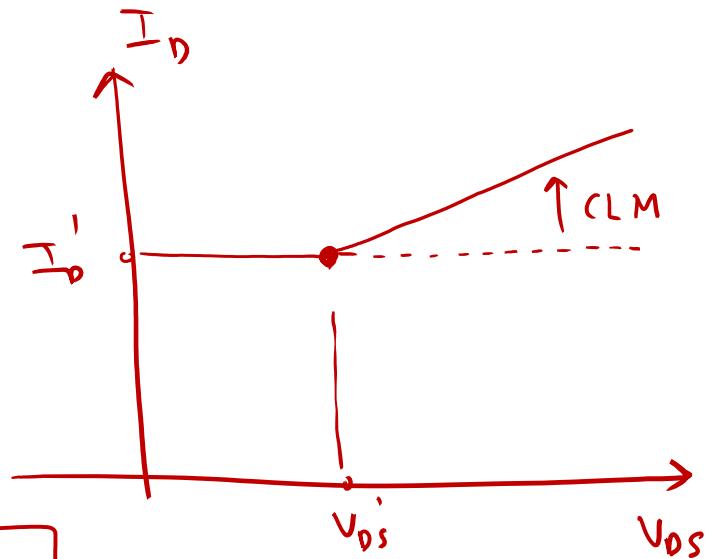
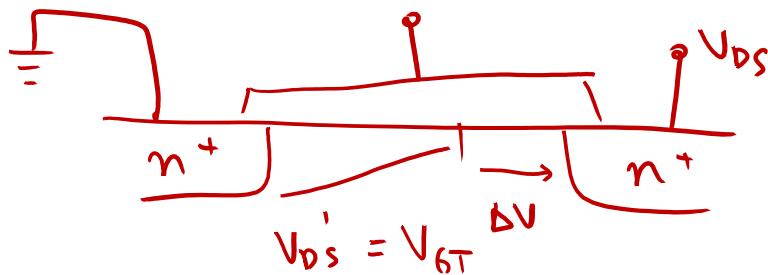


$$V_{DS}' = V_{DS} - V_T$$



MOS in Saturation with CLM

- ◆ Another model: ΔV instead of L_p

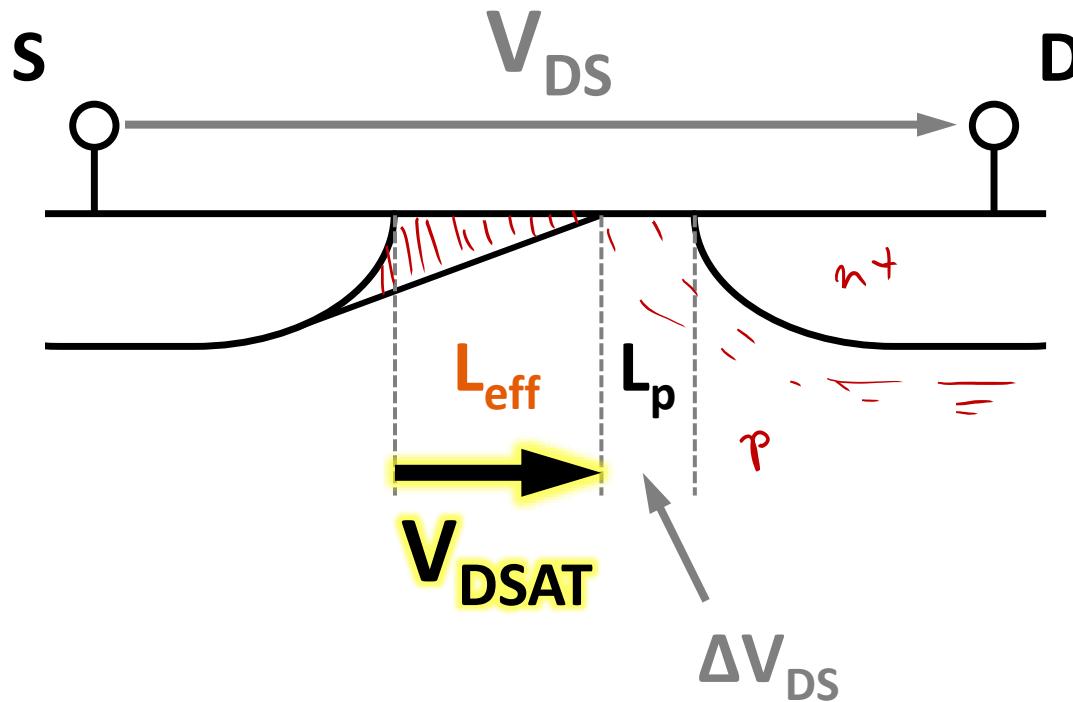


$$I_D = I_D' \cdot (1 + \lambda \cdot V_{DS})$$

CLM parameter

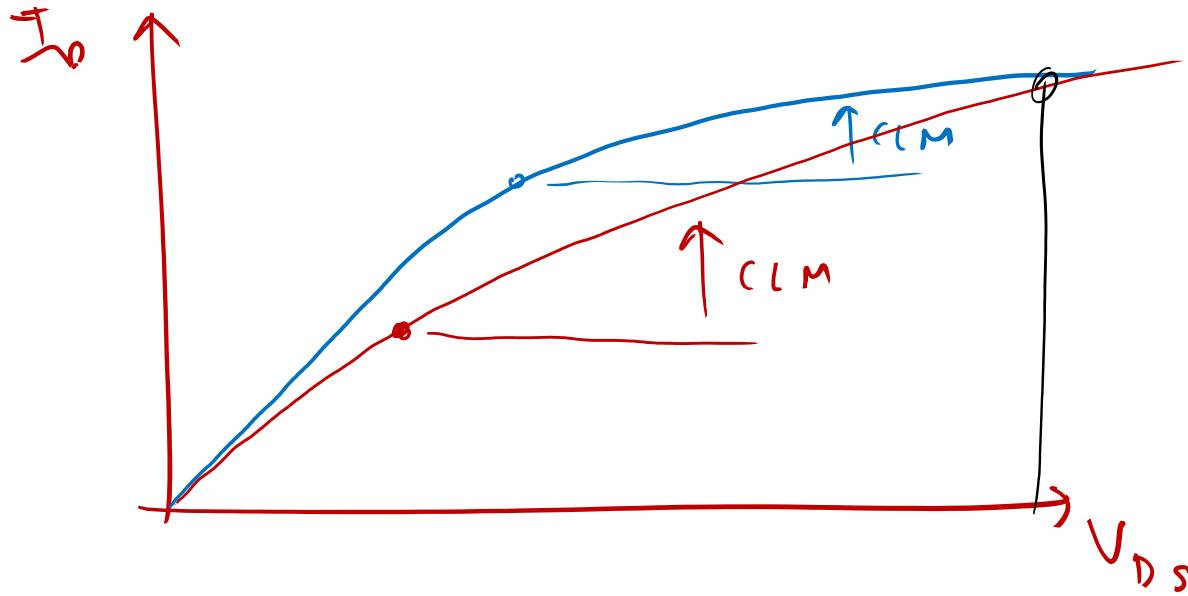
CLM Holds in Vsat

$$V_{DS} > V_{DSAT}$$



Saturation vs. Velocity Saturation

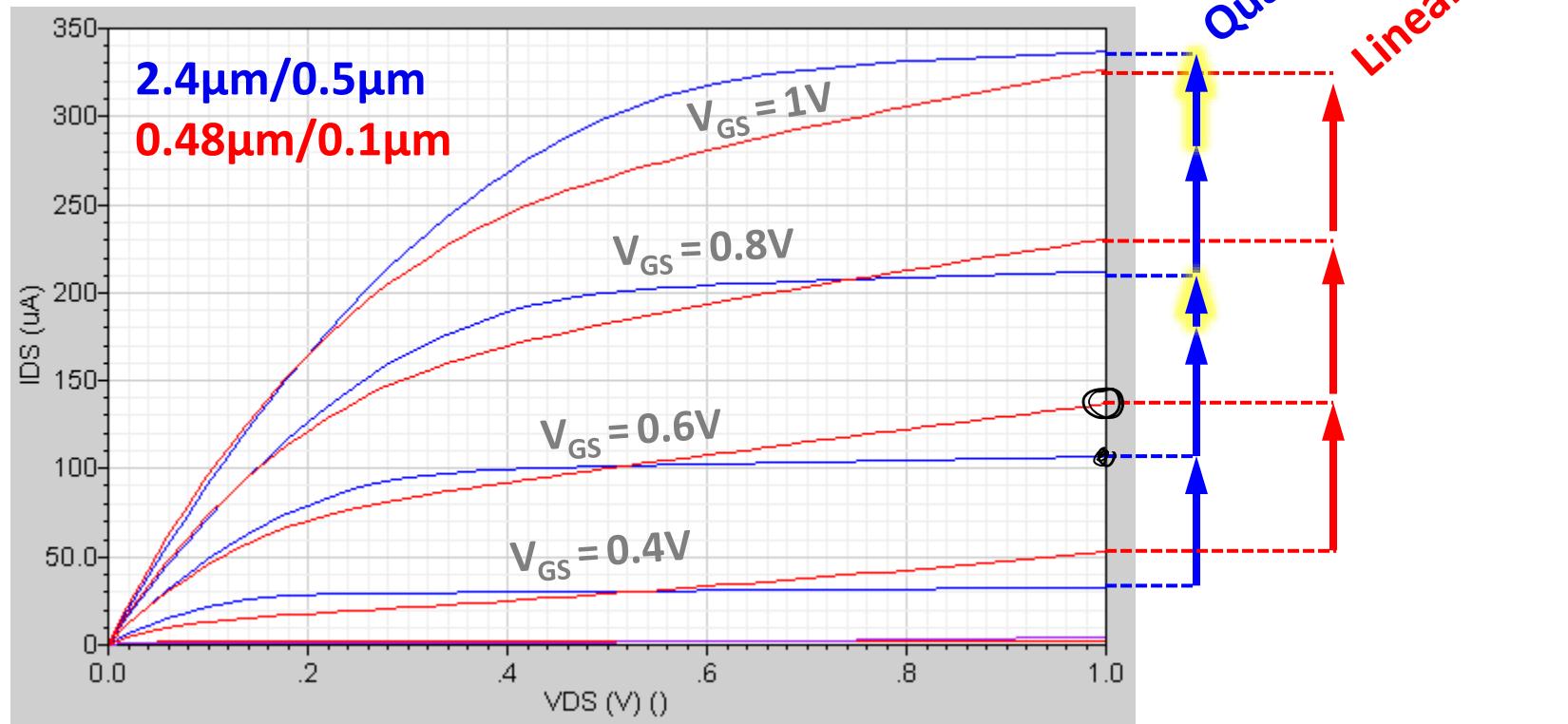
- ◆ V-Sat occurs for lower V_{DS} than Sat



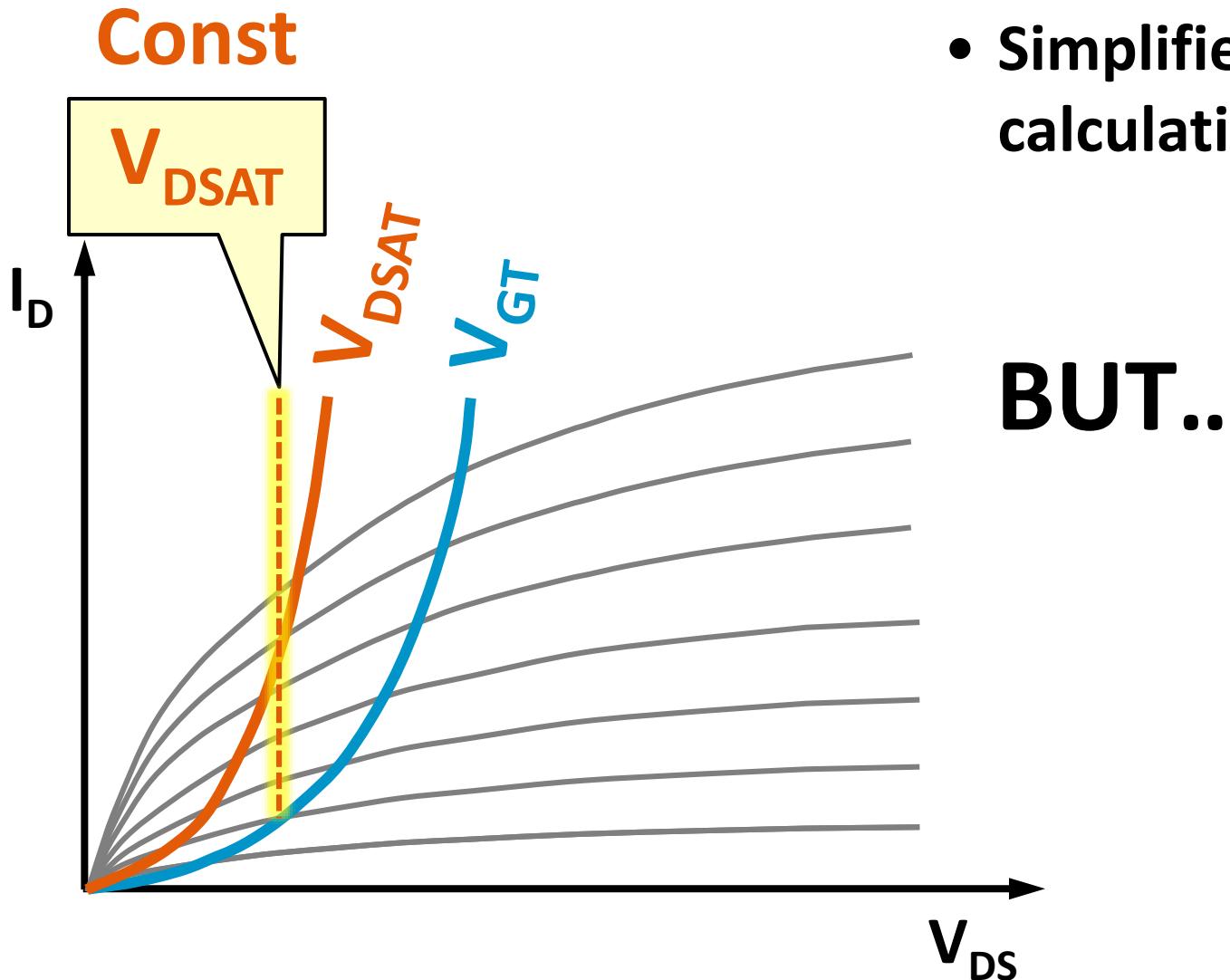
Simulation: Long vs. Short Channel (90nm)

const w/L

- ◆ $I_D^{VSat}(V_{GS})$ linear, $I_D^{Sat}(V_{GS})$ quadratic
- ◆ Stronger CLM in short-L than long-L
- ◆ $I_D^{Vsat} < I_D^{Sat}$ only for large V_{GS}

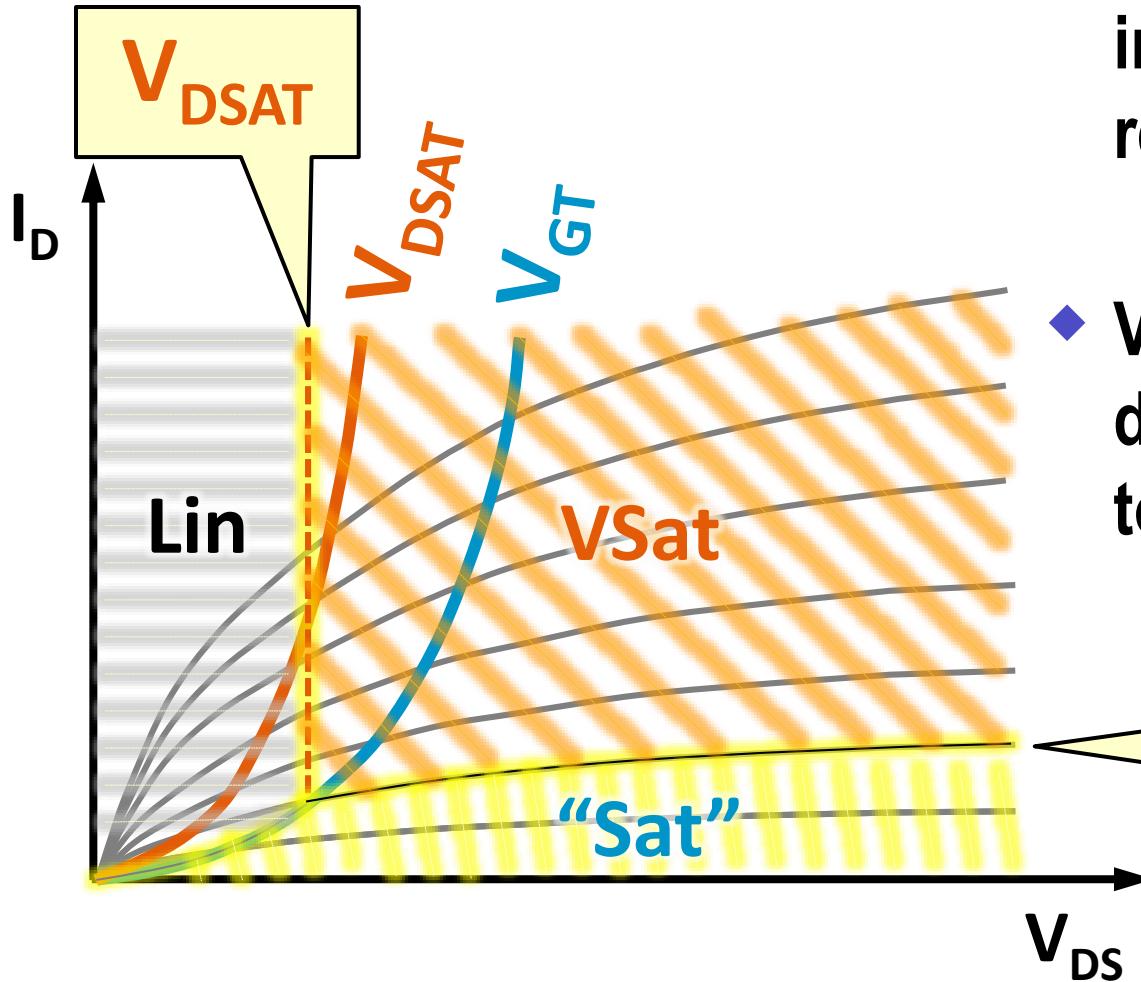


Simplification: $V_{DSAT} = \text{Constant}$



Regions of Operation

Const

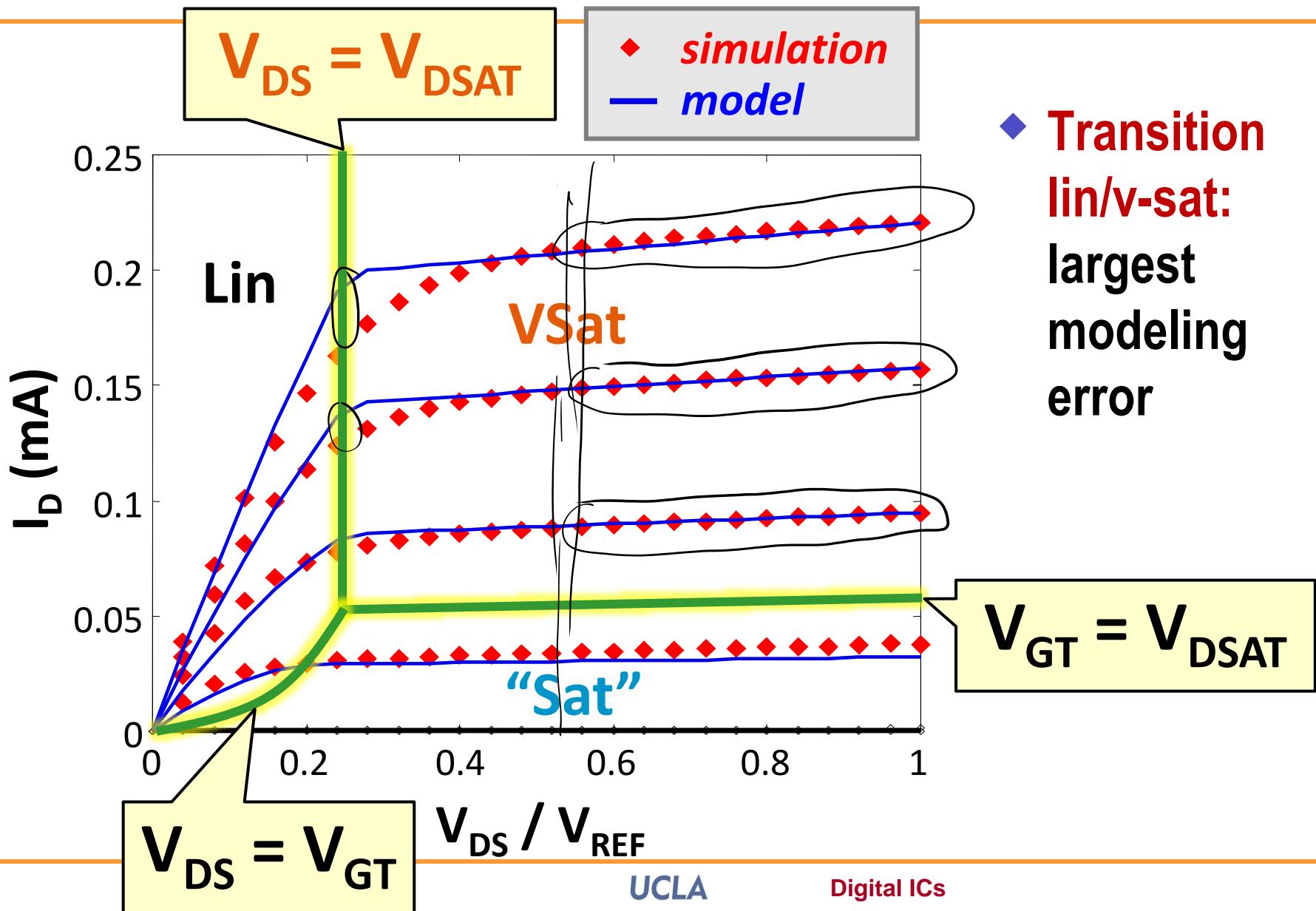


- ◆ Simplification introduces “Sat” region for low V_{GS}

- ◆ $V_{GT} < V_{DSAT}$, the device appears to be in “Sat”

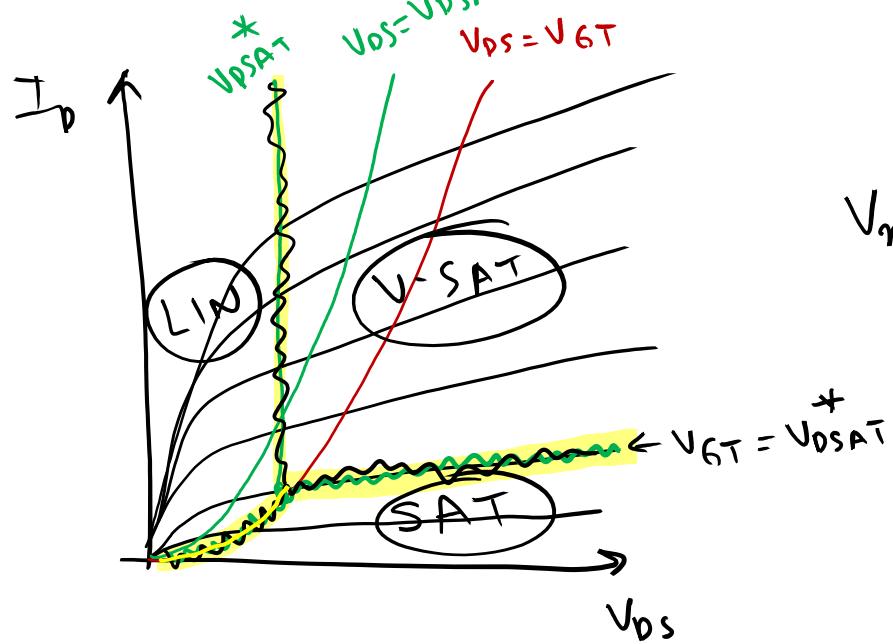
$$V_{GT} = V_{DSAT}$$

Unified Model vs. SPICE Simulation



MOS Regions of Operation

- ◆ Nano-scale MOS devices operate in velocity saturation
 - Saturation still possible for low V_{GS} values (up to V_{DSAT})



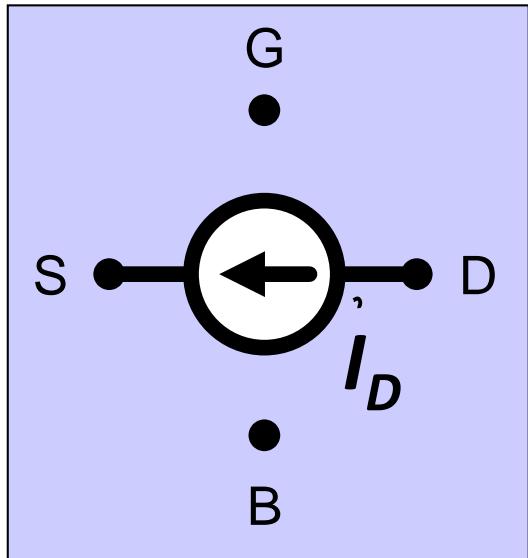
$$V_{min} = \min \left\{ V_{GT}, V_{DS}, V_{DSAT} \right\}$$

Annotations below the equation:

- "SAT" points to the V_{SAT} region.
- "LIN" points to the LIN region.
- "V-SAT" points to the V_{SAT} region.

MOS I-V Model: Active Region

$$V_{GT} = V_{GS} - V_T$$



Active region ($V_{GT} \geq 0$) Lin, Sat, V-Sat

$$I_D = k' \cdot \frac{W}{L} \cdot (V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2}) \cdot (1 + \lambda \cdot V_{DS})$$

$$V_{min} = \min(V_{DS}, V_{GT}, V_{DSAT})$$

↑
Lin Sat V-Sat

Neglect CLM in linear region

Model Parameters: Active Region

- V_{TO} : Threshold voltage
- ? γ : Body effect
- ? V_{DSAT} : Velocity saturation
- k' : Transconductance ($k' = \mu \cdot C_{ox}$)
- ? λ : Channel-length modulation (CLM)

- CLM term $(1 + \lambda V_{DS})$ also included for linear region
 - Empirical, no physical justification

Typical Values for 90nm

- ◆ $\epsilon_{ox} \cdot \epsilon_0 = 3.5 \cdot 10^{-11} \text{ F/m}$ ($\epsilon_{ox} = 3.9$)
 - ◆ $t_{ox} = 2.3 \text{ nm}$
 - ◆ $C_{ox} = \epsilon_{ox} / t_{ox} = 15.2 \text{ fF}/\mu\text{m}^2$
-
- ◆ For W/L = 430nm/120nm
 - ◆ $C_g = 0.65 \text{ fF}$
- $x_d = 15 \text{ nm}$
-
- ◆ $L_{eff} = 70\text{nm}$
 - ◆ $\epsilon_c = 4\text{V}/\mu\text{m}$
 - ◆ $V_{dsat} = \underline{\underline{\epsilon_c L}} = 0.3\text{V}$

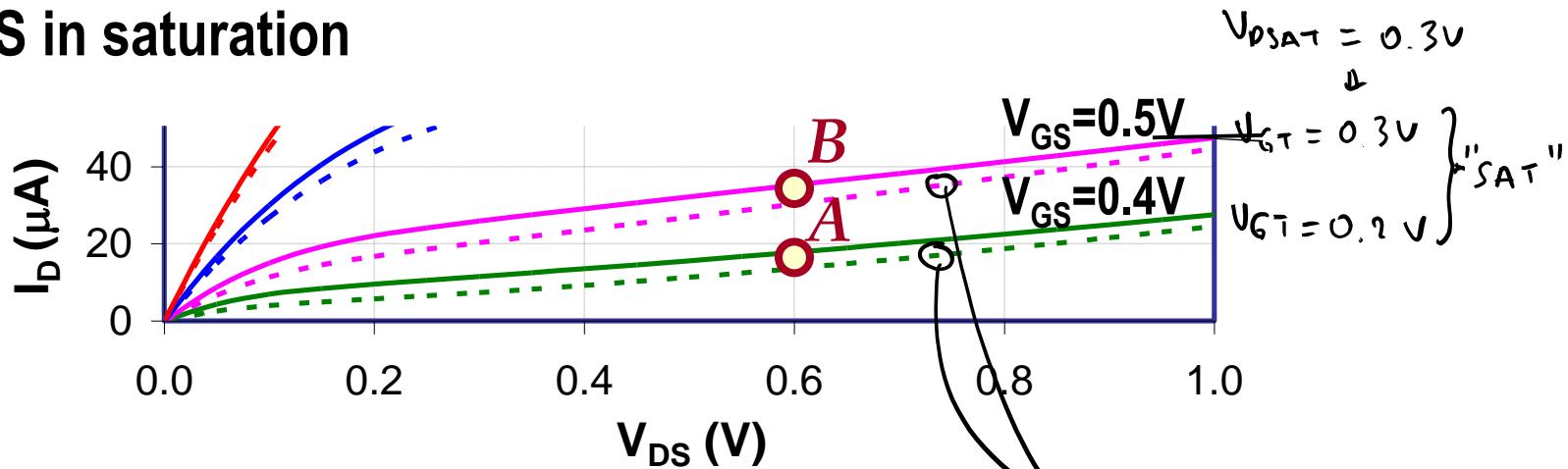
Unified Model: Observations

- ◆ CLM term ($1 + \lambda V_{DS}$) also included for linear region
 - Empirical, not grounded in physical considerations
- ◆ Five parameters: $V_{T0}, \gamma, V_{DSAT}, k', \lambda$
 - Can determine from physics
 - Or choose values that best match simulation/measured data
(match the best in regions that matter the most)
 - Use different model for $L \gg L_{min}$
(in EE115C we assume $L = L_{min}$ unless otherwise specified)

Let's see how do we extract these parameters from the I-V curves

The Meaning of Model Parameters: V_{TO}

- MOS in saturation



\star SAT

$$\frac{I_A}{I_B} = \frac{(V_{GS_A} - V_{TO})^2}{(V_{GS_B} - V_{TO})^2} \Rightarrow \text{solve } V_{TO}$$

✓ with body bias ($V_{SB} > 0$)

The Meaning of Model Parameters: γ

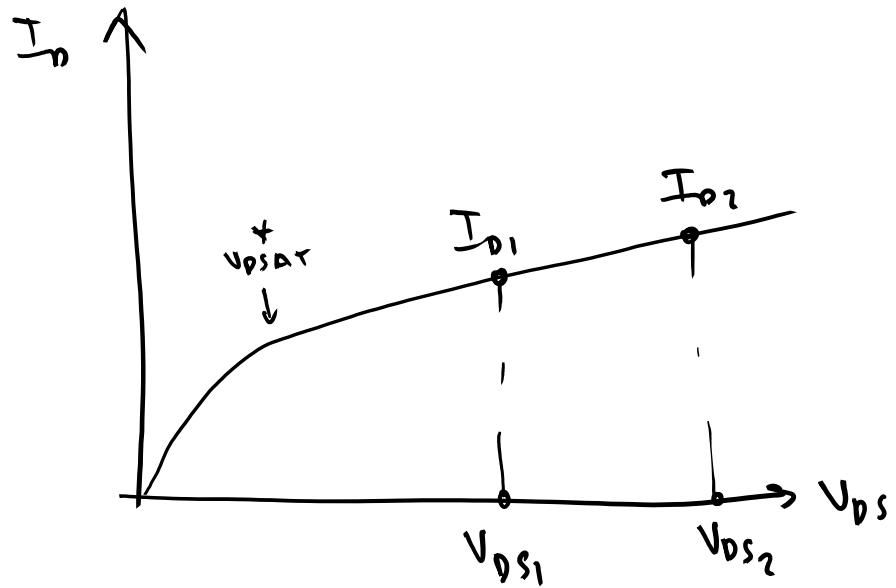
→ V_{TO} (see prev. slide)

→ V_T for known V_{SB}

$$V_T = V_{TO} + \gamma (\sqrt{-2\phi_F + V_{SB}} - \sqrt{12\phi_F})$$

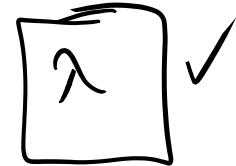
↳ calc / estimate $\boxed{\gamma}$ ✓

The Meaning of Model Parameters: λ



$$\frac{I_{D1}}{I_{D2}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}}$$

=> calc



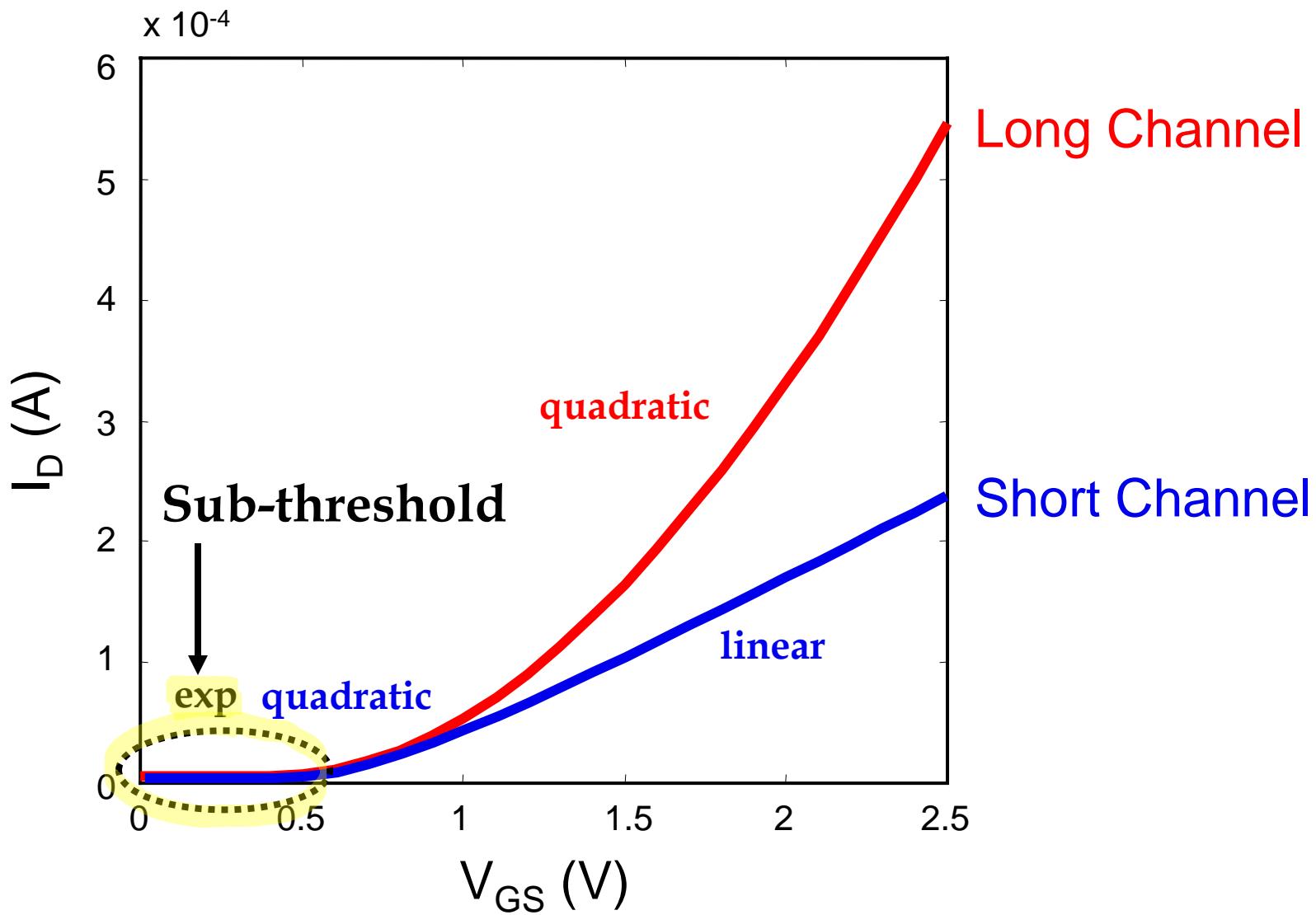
The Meaning of Model Parameters: k'

- assume V_{TO}, λ are known (from previous slides)

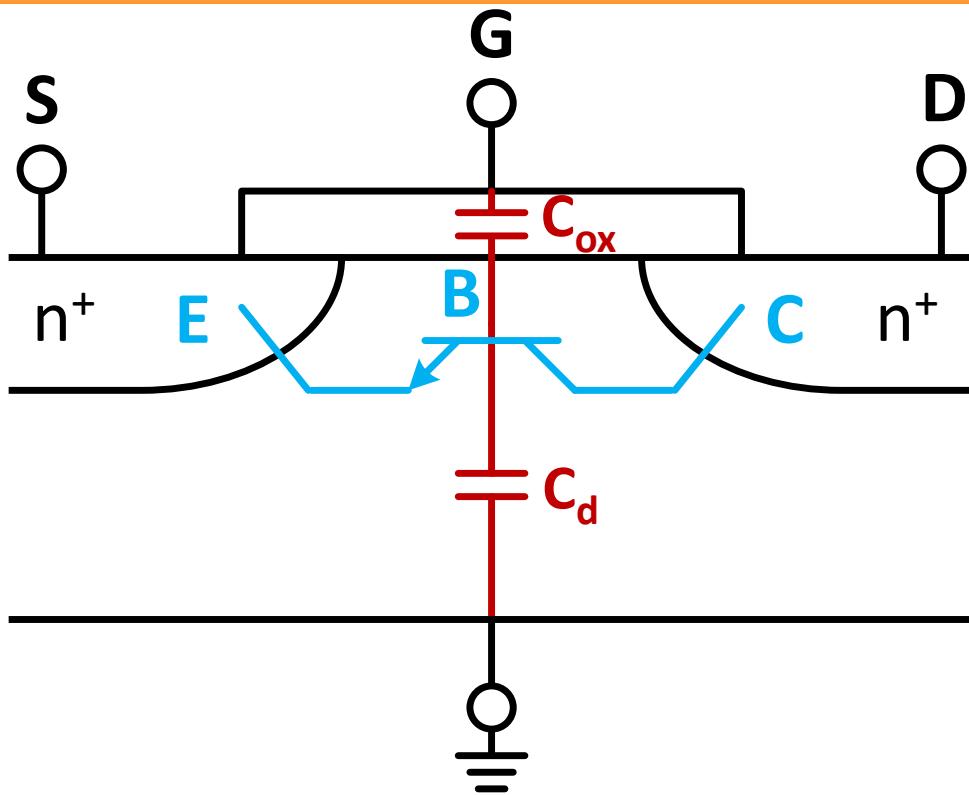
$$I_D = k' \frac{w}{l} V_{GS}^2 (1 + \lambda V_{DS})$$

$$\Rightarrow \boxed{k'} \quad \checkmark$$

Sub-threshold I_D versus V_{GS} is Exponential



Modeling the Sub-threshold Behavior



Parasitic BJT

$$I_C = I_0 e^{\frac{V_{BE}}{\Phi_t}}$$

$$V_{BE} = \frac{V_{GS}}{1 + \frac{C_d}{C_{ox}}}$$

$$n = 1 + \frac{C_d}{C_{ox}}$$

$$\Phi_t = \frac{kT}{q}$$

$$I_D = I_0 \cdot e^{\frac{V_{GS}}{n\Phi_t}} \cdot (1 - e^{-\frac{V_{DS}}{\Phi_t}})$$

Sub-threshold I_D vs. V_{GS}

*Physical
model*

$$I_D = I_0 \cdot e^{\frac{V_{GS}}{n\Phi_t}} \cdot (1 - e^{-\frac{V_{DS}}{\Phi_t}})$$

$$I_0 = \mu \frac{W}{L} \Phi_t^2 e^{-\frac{V_T}{n\Phi_t}}$$

*Empirical
model*

$$I_D = I_0 \cdot \frac{W}{W_0} \cdot 10^{\frac{V_{GS} - V_T + \gamma_D V_{DS}}{S}}$$

DIBL

$$S = n\Phi_t \ln(10) \quad [\text{mV/dec}]$$

The Sub-threshold Slope Parameter

$$S = n\Phi_t \ln(10) \quad [\text{mV/dec}]$$

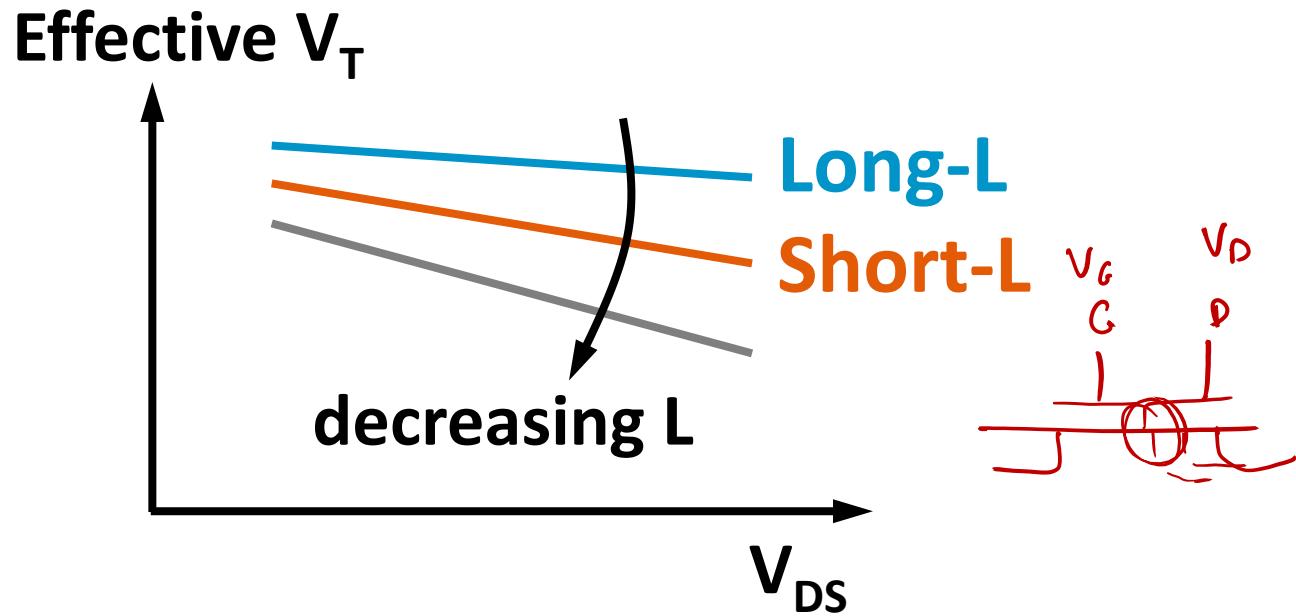
Change in V_{GS} that gives **10x change in I_{DS}**

- ◆ $n = 1 \quad 60 \text{ mV/dec} \quad (\text{ideal})$
- ◆ $n = 1.5 \quad 90 \text{ mV/dec} \quad (\text{typical})$

- S : increases with temperature (Φ_t)
- n : intrinsic to device topology / structure

$$\frac{kT}{q}$$

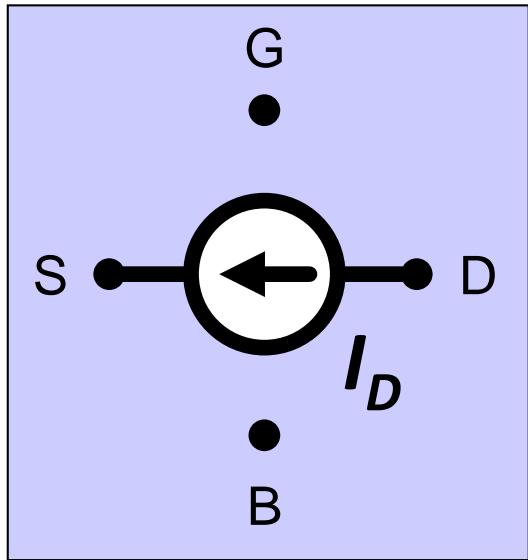
Drain Induced Barrier Lowering (DIBL)



- ◆ Field lines from the drain affect charge in the channel
- ◆ Typically derived for small V_{DS} , holds for large V_{DS}
 - Even if we neglect CLM, I_{DS} will increase b/c of V_T drop
 - Device turned off by V_{GS} (below V_T) may turn on by V_{DS}

MOS I-V Model: Subthreshold

$$V_{GT} = V_{GS} - V_T$$



Subthreshold region ($V_{GT} \leq 0$)

$$I_D = I_0 \cdot \frac{W}{W_0} \cdot 10^{\frac{V_{GS} - V_T + \gamma_D \cdot V_{DS}}{S}}$$

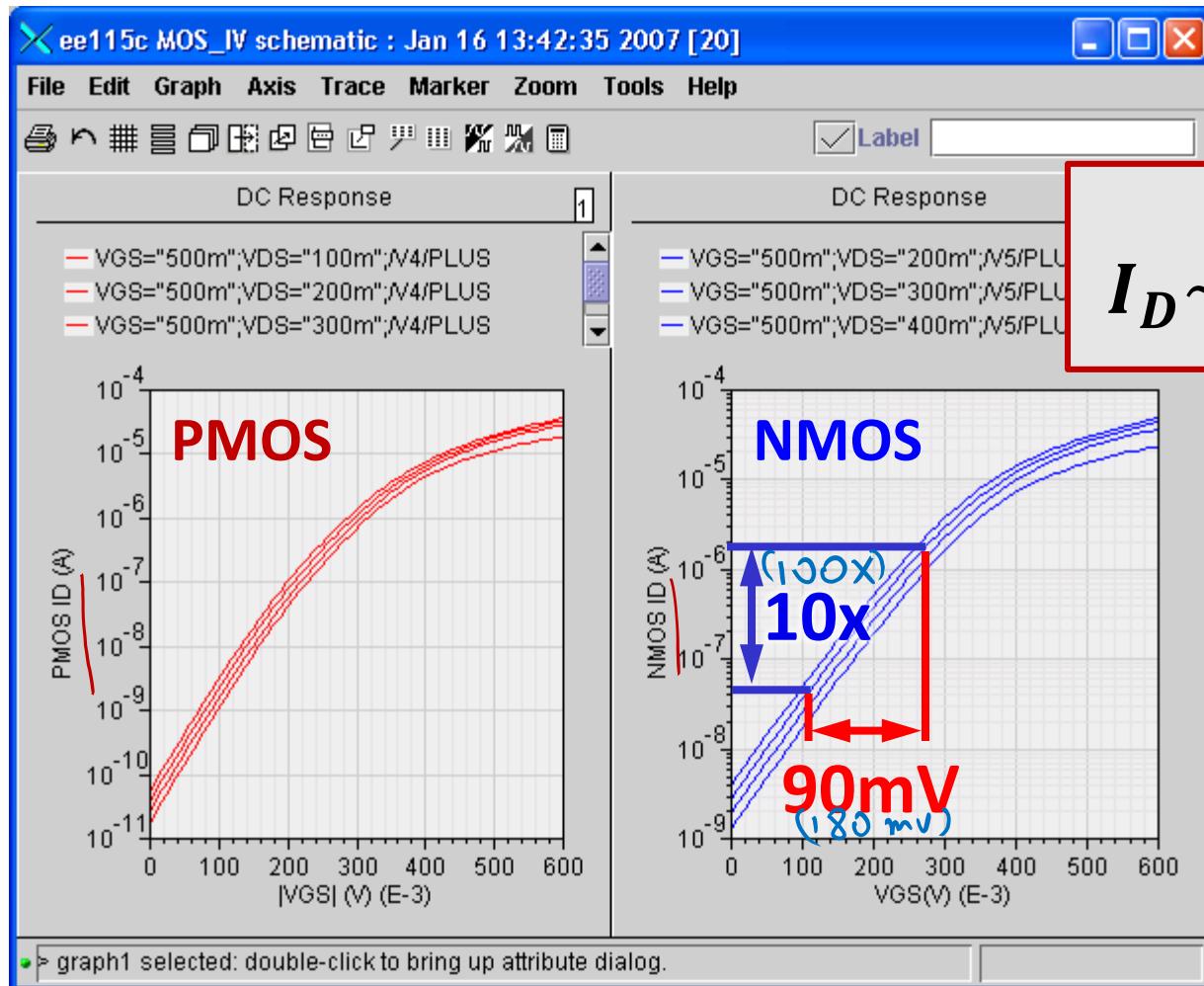
Model parameters

I_0 : Nominal leakage current

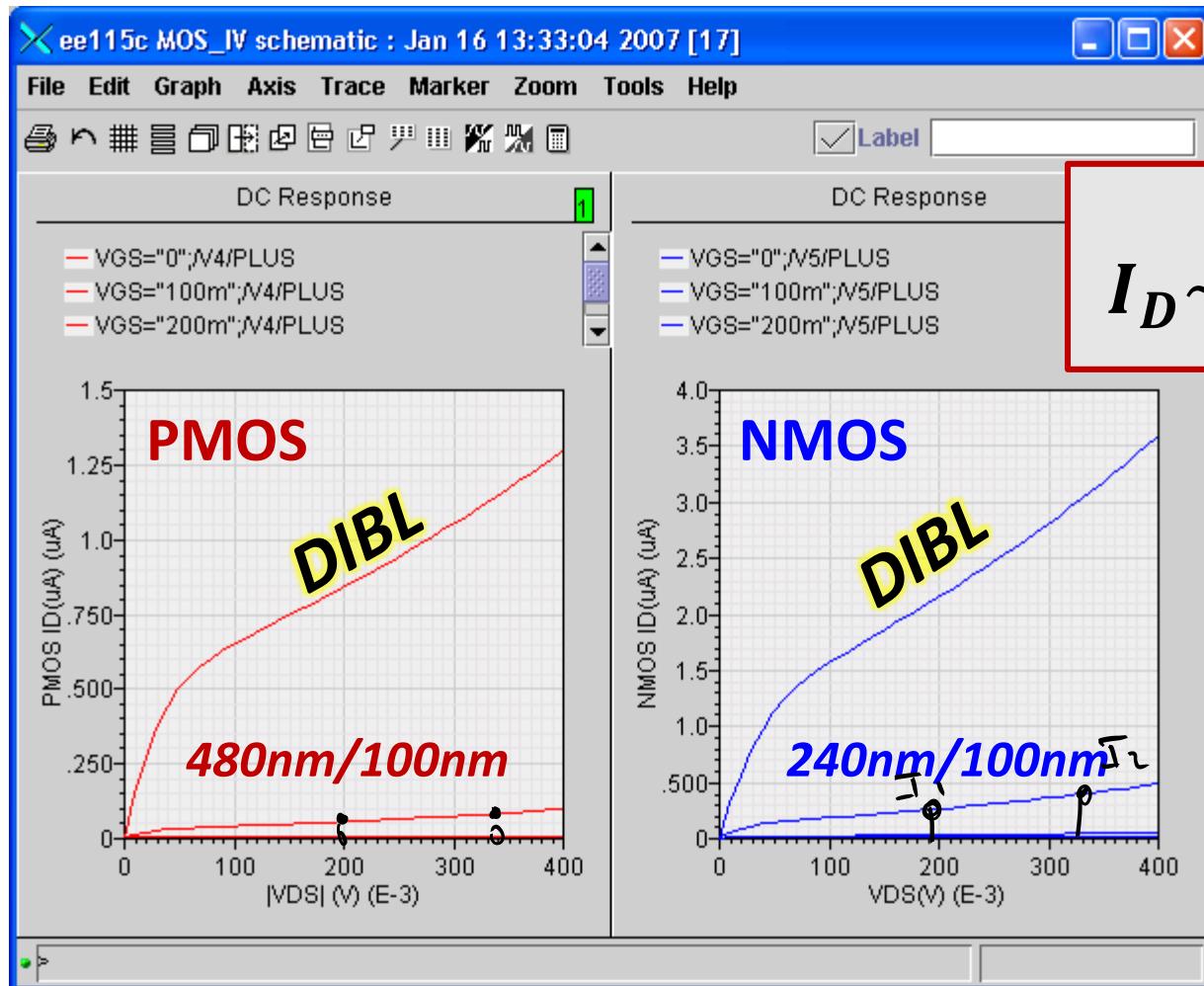
S : Subthreshold slope

$\sqrt{\gamma_D}$: DIBL factor

90nm Simulation: Sub-threshold I_D vs. V_{GS}

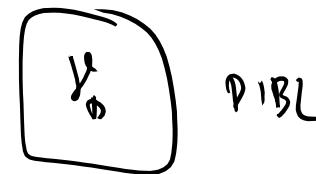


90nm Simulation: Sub-threshold I_D vs. V_{DS}



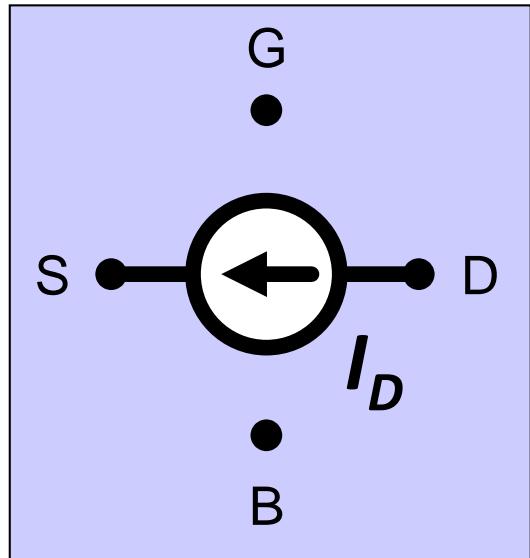
$$I_D \sim 10^{\frac{V_{GS}-V_T+\gamma D V_{DS}}{S}}$$

V_{GS} : 0 to 0.3V



MOS I-V Model: Summary

$$V_{GT} = V_{GS} - V_T$$



Subthreshold region ($V_{GT} \leq 0$)

$$I_D = I_0 \cdot \frac{W}{W_0} \cdot 10^{\frac{V_{GS} - V_T + \gamma_D \cdot V_{DS}}{S_V}}$$

Active region ($V_{GT} \geq 0$) Lin, Sat, V-Sat

$$I_D = k' \cdot \frac{W}{L} \cdot (V_{GT} \cdot V_{min} - \frac{V_{min}^2}{2}) \cdot (1 + \lambda \cdot V_{DS})$$

$$V_{min} = \min(V_{DS}, V_{GT}, V_{DSAT})$$

Lin "Sat" V-Sat

.MODEL Parameters MOS1 (Basic Parameters)

◆ .MODEL Modname NMOS/PMOS <VT0=VT0...>

Name	Parameter	Units	Default	Example	Scale Factor
VTO	Threshold voltage	V	0	1.0	—
KP	Transconductance parameter	AV^{-2}	2.0×10^{-5}	1.0E-3	—
GAMMA	Bulk threshold parameter	$\text{V}^{1/2}$	0	0.5	—
PHI	Surface potential	V	0.6	0.7	—
LAMBDA	Channel length modulation parameter	V^{-1}	0	1.0E-4	—
RD	Drain ohmic resistance	Ω	0	10	—
RS	Source ohmic resistance	Ω	0	10	—
RSH	D and S diffusion sheet resistance	Ω/sq	0	10	NRD NRS
CBD	Zero-bias BD junction capacitance	F	0	5P	—
CBS	Zero-bias BS junction capacitance	F	0	1P	—
CJ	Zero-bias bulk junction bottom capacitance	Fm^{-2}	0	2.0E-4	AD AS
MJ	Bulk junction grading coefficient	—	0.5	0.5	
CJSW	Zero-bias bulk junction sidewall capacitance	Fm^{-1}	0	1.0E- 9	PD PS
MJSW	Bulk junction grading coefficient	—	0.33	0.25	
PB	Bulk junction potential	V	1	0.6	
IS	Bulk junction saturation current	A	10^{-14}	1.0E-16	
CGDO	GD overlap capacitance per unit channel width	Fm^{-1}	0	4.0E-11	W
CGSO	GS overlap capacitance per unit channel width	Fm^{-1}	0	4.0E-11	W
CGBO	GB overlap capacitance per unit channel length	Fm^{-1}	0	2.0E-10	L
TOX	Thin-oxide thickness	m	∞	0.1U	
LD	Lateral diffusion	m	0	0.2U	

In Reality: GPKD090 Model (gpdk090_mos.scs)

```
section TT_s1v
parameters
+ s1v_rs_ne = 0.000000e+000  s1v_vsat_ne = 1.120000e+005  s1v_pldd_surf = 6.000000e+019
+ s1v_uc1_ne = 3.700000e-010  s1v_u0_ne = 2.000000e-002  s1v_nch_ne = 5.200000e+017
+ s1v_rsc_ne = 4.082483e-014  s1v_cgbo_ne = 1.482000e-011  s1v_prt_ne = 1.000000e+001
+ s1v_rdc_ne = 4.082483e-014  s1v_vth0_ne = 1.692662e-001  s1v_k2_ne = 0.000000e+000
+ s1v_cgdo_ne = 2.667600e-010  s1v_ckappa_ne = 4.605336e+000  s1v_wint_ne = 6.000000e-009
+ s1v_k1_ne = 2.825346e-001  s1v_cgsl_ne = 1.111500e-010  s1v_nldd_surf = 3.000000e+019
+ s1v_js_ne = 3.366667e-006  s1v_hdif_ne = 1.400000e-007  s1v_rdsw_ne = 3.900000e-006
+ s1v_jsw_ne = 3.366667e-010  s1v_tox_ne = 2.330000e-009  s1v_cj_ne = 7.983537e-004
+ s1v_cjsw_ne = 4.790122e-011  s1v_ldif_ne = 1.000000e-008  s1v_xj_ne = 2.500000e-008
+ s1v_rd_ne = 0.000000e+000  s1v_pb_ne = 9.918524e-001  s1v_cf_ne = 4.594612e-011
+ s1v_lint_ne = 1.500000e-008  s1v_cjswg_ne = 1.995884e-011  s1v_rsh_ne = 1.000000e+001
+ s1v_u0_pe = 1.200000e-002  s1v_nch_pe = 4.000000e+017  s1v_rsc_pe = 2.886751e-014
+ s1v_cgbo_pe = 1.392363e-011  s1v_rdc_pe = 2.886751e-014  s1v_vth0_pe = -1.359511e-001
+ s1v_k2_pe = 0.000000e+000  s1v_cgdo_pe = 2.506253e-010  s1v_ckappa_pe = 1.043477e+001
+ s1v_wint_pe = 5.000000e-009  s1v_k1_pe = 2.637520e-001  s1v_cgsl_pe = 1.044272e-010
+ s1v_js_pe = 3.350000e-006  s1v_hdif_pe = 1.400000e-007  s1v_rdsw_pe = 7.800000e-006
+ s1v_jsw_pe = 3.350000e-010  s1v_tox_pe = 2.480000e-009  s1v_cj_pe = 7.912252e-004
+ s1v_cjsw_pe = 4.747351e-011  s1v_ldif_pe = 1.000000e-008  s1v_xj_pe = 2.500000e-008
+ s1v_rd_pe = 0.000000e+000  s1v_pb_pe = 1.009805e+000  s1v_cf_pe = 4.527118e-011
+ s1v_lint_pe = 1.500000e-008  s1v_cjswg_pe = 1.978063e-011  s1v_rsh_pe = 2.000000e+001
+ s1v_rs_pe = 0.000000e+000  s1v_vsat_pe = 1.000000e+005
include "gpdk090_mos.scs" section - s1v_mos
endsection TT_s1v
```

This model continues on the next slide

GPDK090 Model (section s1v_mos)

```
section s1v_mos
model gpdk090_nmos1v bsim3v3 type = n
+ lmin = 0.0          lmax = 1.0          wmin = 0.0
+ wmax = 1.0          tnom = 25.0         version = 3.2
+ tox = s1v_tox_ne    toxm = s1v_tox_ne   xj = s1v_xj_ne
+ nch = s1v_nch_ne   lln = 1.0000000    lwn = 1.0000000
+ wln = 1.0000000    wnn = -1.0000000   lint = s1v_lint_ne
+ ll = 0.00           lw = 0.00          lwl = 0.00
+ wint = s1v_wint_ne wl = 0.00          ww = 0.00
+ wwl = 0.00          mobmod = 1        binunit = 2
+ xl = 0              xw = 0             dwg = 0.00
+ dwb = 0.00           acm = 12          ldif = s1v_ldif_ne
+ hdif = s1v_hdif_ne  rsh = s1v_rsh_ne   rd = s1v_rd_ne
+ rs = s1v_rs_ne      rsc = s1v_rsc_ne   rdc = s1v_rdc_ne
+ vth0 = s1v_vth0_ne  k1 = s1v_k1_ne    k2 = s1v_k2_ne
+ k3 = -2.3000000     dvt0 = 3.86366    dvt1 = 1.2
+ dvt2 = 5.0299990E-02 dvt0w = 0.00      dvt1w = 0.00
+ dvt2w = 0.00         nlx = 1.2517999E-07 w0 = -7.1353000E-09
+ k3b = 0.5576769     ngate = 4.0E20      vsat = s1v_vsat_ne
+ ua = -6.1879500E-10 ub = 1.8806652E-18 uc = 1.3823546E-10
+ rdsw = s1v_rdsw_ne  prwb = 0.00        prwg = 0.00
+ wr = 1.0000000      u0 = s1v_u0_ne    a0 = 2.3750000
+ keta = -3.1429991E-02 a1 = 0.00        a2 = 0.9900000
+ ags = 0.8900000     b0 = 0.00        b1 = 0.00
```

And many more parameters... (compare to our 5-parameter model)

Spectre Netlist (NMOS, PMOS)

```
section s1v_mac
subckt s1v_ckt_nch (n11 n2 n33 n4)
parameters l=0.1u w=10u multi=1 factor=1 nrd=s1v_hdif_ne/factor/w nrs=s1v_hdif_ne/factor/w
+ Tox_ratio = 3.0e-9 / (s1v_tox_ne*s1v_tox_ne*s1v_tox_ne)
MAIN (n1 n2 n3 n4) [gdk090_nmos1v] w=w l=l nrd=nrd nrs=nrs multi=multi
GDF1 (n2 n1) bsource i = w*0.6*s1v_xj_ne*4.97232*Tox_ratio*v(n2,n1)*v(n2,n3)*exp(-4.85669e11*s1v_tox_ne*...
GDF2 (n2 n3) bsource i = w*0.6*s1v_xj_ne*4.97232*Tox_ratio*v(n2,n3)*sqrt( (v(n2,n3) - 0.026*log(4.0e20 ...
20 / s1v_nldd_surf)) + 1.0e-4 )*exp(-4.85669e11*s1v_tox_ne*(0.43-0.054*sqrt( (v(n2,n3) - 0.026*log(4.0e20 ...
.0e20 / s1v_nldd_surf)) + ... - 0.026*log(4.0e20 / s1v_nldd_surf))*(v(n2,n3) ...s1v_nldd_surf)) + 1.0e-4 ))
rdn (n1 n11) resistor r= 6.8 *nrd/multi
rsn (n3 n33) resistor r= 6.8 *nrs/multi
ends s1v_ckt_nch

subckt s1v_ckt_pch (p11 p2 p33 p4)
parameters l=0.1u w=10u multi=1 factor=1 nrd=s1v_hdif_pe/factor/w nrs=s1v_hdif_pe/factor/w
+ Tox_ratio = 3.0e-9/(s1v_tox_pe*s1v_tox_pe*s1v_tox_pe)
MAIN (p1 p2 p3 p4) [gdk090_pmos1v] w=w l=l nrd=nrd nrs=nrs multi=multi
GDF1 (p2 p1) bsource i = w*0.6*s1v_xj_pe*3.42537*Tox_ratio*v(p2, p1)*sqrt( (v(p2, p1)-
0.026*log(9.32E19/s1v_pldd_surf))*(v(p2, p1)-0.026*log(9.32E1
9/s1v_pldd_surf)) + 1.0e-4 )*exp(-7.0645e11*s1v_tox_pe*(0.31-0.024*sqrt( (v(p2, p1)-
0.026*log(9.32E19/s1v_pldd_surf))*(v(p2, p1)-0.026*log(9.32E19... s1v_pldd_surf)) + 1.0e-4 ))*(1.0+0.03*sqrt( (v(p2, p1)-
0.026*log(9.32E19/s1v_pldd_surf))*(v(p2, p1)-0.026*log(9.32E19/s1v_pldd_surf)) + 1.0e-4 )))
GDF2 (p2 p3) bsource i = w*0.6*s1v_xj_pe*3.42537*Tox_ratio*...sqrt( (v(p2, p3)-...0.026*log(9.32E19/...)) + 1.0e-4 ))
rdp (p1 p11) resistor r = 7.1 * nrd / multi
rsp (p3 p33) resistor r = 7.1 * nrs / multi
ends s1v_ckt_pch
endsection s1v_mac
```