Q1

1. **Plain Old NMOS [10 pts]**
Consider an NMOS transistor with V_{t0} = 300 mV and k_n' = 100 μA/V². Carry forward values from previous parts.
a) Determine the *W/L* needed to achieve a drain current of 200 μA with V_{OV} = 400 mV for a transistor operating in saturation. Assume that $V_S = V_B$ = 0 V.
b) What is the maximum resistance *R* that can be used as the load on the drain and keep the transistor in saturation with a 2 V supply? *Briefly* explain what happens if this resistance is larger.
c) Assuming saturation, what is the maximum small-signal gain that can be achieved with a resistive load and a supply voltage of 2 V? (Do not consider large-signal swing limitations.)

$V_{OV} = V_{GS} - V_{t0}$

$400mV = V_{GS} - 300mV$

a) Saturation:

$i_{DS} = \frac{1}{2} k_n' \cdot \frac{W}{L} (V_{GS} - V_t)^2$

$i_{DS} = 200\,uA \qquad V_{OV} = V_{GS} - V_t = 400\,mV \qquad k_n' = 100 \frac{uA}{V^2}$

$200\,uA = \frac{1}{2} \cdot 100 \frac{uA}{V^2} \cdot \frac{W}{L} \cdot (0.4)^2 V^2$

$200\,uA = 8\,uA \cdot \frac{W}{L}$

$\boxed{\frac{W}{L} = 25}$

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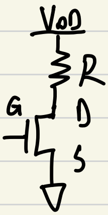
b) Saturation $\quad V_{DS} \geq V_{OV} \qquad V_{DD} = 2V$

V_{DS} at least need to be V_{OV}, So $V_{DS} = 0.4\,V$



① $V_{DS} = V_{DD} - I_{DS}R$

② $I_{DS} = \frac{1}{2} \cdot 100 \cdot 25 \cdot 0.4^2$ Find minimum current to be in Sat

$= 200\,uA$

③ $V_{DS} = 2 - 200 \cdot 10^{-6} \cdot R$

$0.4 = 2 - 200 \cdot 10^{-6} \cdot R$

$1.6 = 200 \cdot 10^{-6} \cdot R$

$R = 8000\,\Omega = \boxed{8k\,\Omega}$

b) Based on the equation ①, and assuming the current is the same.

$V_{DS} = 2 - 200uA \cdot R \Rightarrow R \uparrow \Rightarrow V_{DS} \downarrow$

Then transistor will no longer in the saturation region because $V_{DS} \leq V_{OV}$. The transistor will be in triode region

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c)

$$A_v = \frac{V_{out}}{V_{in}} = -\frac{2 I_D}{V_{OV}} \cdot R_D$$

$$= -\frac{2 \cdot 200u}{0.4} \cdot 8000$$

$$= \boxed{-8}$$

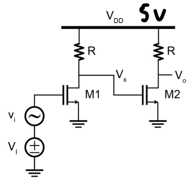
Q2

2. NMOS Cascade Amplifier [10 pts]

Consider the circuit shown below. Use $V_{t0} = 500$ mV, $V_{DD} = 5$ V, and $k_n' = 50\ \mu A/V^2$ for all calculations.

a) For what range of V_I will both M_1 and M_2 be in saturation? Assume $W/L = 30$ and $R = 6\ k\Omega$.

b) Given that $V_I = V_X = V_{DD}/2$ (*i.e.*, the scaling of devices and choice of R values made this happen), find a generalized expression for the per-stage small-signal gain. (Note: This is a special case for identical W/L for both devices).



$k_n' = 50 \frac{uA}{V^2}$ $\quad \frac{W}{L} = 30$

$V_{DD} = 5V$ $\quad R = 6k\Omega$

$V_{t0} = 500mV$

a) In saturation, $i_{DS} = \frac{1}{2} k_n' \cdot \frac{W}{L} \cdot (V_{GS} - V_t)^2$, $V_{DS} \geq V_{OV}$

$V_{GS1} = V_I$ $\qquad V_{GS2} = V_X = V_{DD} - i_{DS1} \cdot R$
$= 5 - i_{DS1} \cdot 6000$

M_1: $V_{DS_1} = V_{GS} - V_t = V_I - 0.5 = V_X = V_{OV_1}$

M_2: $V_{DS_2} = V_X - 0.5 = V_I - 1 = V_{OV_2} = V_O$

$i_{DS_1} = \frac{1}{2} \cdot 50 \cdot 30 \cdot (V_I - 0.5)^2 = 750 (V_I - 0.5)^2 \cdot 10^{-6}$

$i_{DS2} = \frac{1}{2} \cdot 50 \cdot 30 \cdot (V_I - 1)^2 = 750 (V_I - 1)^2 \cdot 10^{-6}$

① $i_{DS1} = \frac{5 - V_X}{6000} = \frac{5 - (V_I - 0.5)}{6000} = 750 (V_I - 0.5)^2 \cdot 10^{-6}$

② $i_{DS2} = \frac{5 - V_O}{6000} = \frac{5 - (V_I - 1)}{6000} = 750 (V_I - 1)^2 \cdot 10^{-6}$

① i_{DS1}: solved by symbolab $\Rightarrow$ $V_I = 1.448$ v or -0.67 v

② i_{DS2}: solved by symbolab $\Rightarrow$ $V_I = 1.948$ v or -0.17 v

so $\boxed{1.448V \leq V_I \leq 1.948V}$

b) $V_I = V_x = V_{DD}/2 = 2.5$ $\qquad V_{DS} = 2.5 > V_1 - 0.5$

For M_1 : $V_x = V_{out}$, $V_I = V_{in}$

$$A_{v_1} = \frac{dV_{out}}{dV_{in}} = \frac{d}{dV_{in}}\left(V_{DD} - \frac{1}{2} k_n' \cdot \frac{W}{L} \cdot (V_{in} - V_{to})^2 \cdot R\right)$$

$$= -k_n' \cdot \frac{W}{L} \cdot (V_I - V_{to}) \cdot R$$

$$A_{v_1} = -k_n' \cdot \frac{W}{L} \cdot (V_I - V_{to}) \cdot R$$

For M_2 : $V_x = V_{in}$ $\quad V_o = V_{out}$

$$A_{v_2} = \frac{dV_{out}}{dV_{in}} = \frac{d}{dV_{in}}\left(V_{DD} - \frac{1}{2} k_n' \cdot \frac{W}{L} (V_{in} - V_{to})^2 \cdot R\right)$$

$$= -k_n' \cdot \frac{W}{L} \cdot (V_x - V_{to}) \cdot R$$

$$A_{v_2} = -k_n' \cdot \frac{W}{L} \cdot (V_x - V_{to}) \cdot R$$

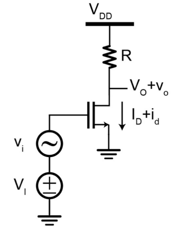
Q3

3. Linearity [15 pts]

Consider the amplifier shown below. Assume a supply voltage of 2.5 V, a bias current of 100 μA, a load resistance of 10 kΩ, V_{t0} = 500 mV, and k_n' = 50 μA/V².

a) What is the maximum possible small-signal gain? Find the corresponding W/L, V_I and DC operating point (*i.e.*, all node voltages and branch currents) if $V_{OV(min)}$ = 150 mV and $W/L_{(max)}$ = 32. (Note: The W/L ratio is restricted to be an integer.)

b) The second- and higher-order terms in the gain expression are known as distortion. (Obviously, you cannot neglect this in this problem…) Redesign the circuit such that for v_i = 50 mV, the distortion term is less than 3.5%. (Hint: Take the ratio of the second-order and linear terms.) Your circuit must still meet the constraints imposed in part (a). Recalculate the W/L, V_I, DC operating point, and small-signal gain.



$V_{DD} = 2.5$

$I_D = 100u$

$R = 10k$

$V_{t_0} = 500m$

$k_n' = 50u \frac{A}{V^2}$

a) $A_v = \frac{-2I_D}{V_{OV}} \cdot R$ Maximum small-signal gain can be get when V_{OV} is at minimum

Then,

$A_v = \frac{-2 \cdot 100u}{150m} \cdot 10k = -\frac{40}{3} = \boxed{-13.\overline{3}}$

Assuming $V_{OV} = 150mV$

$100u = \frac{1}{2} \cdot 50u \cdot \frac{W}{L} \cdot (V_I - 500mV)$

$100 = 25 \frac{W}{L} \cdot 150mV$

$\frac{W}{L} = 26.\overline{6} = \frac{80}{3}$

Assuming $\frac{W}{L} = 32$

$100u = \frac{1}{2} \cdot 50u \cdot 32 \cdot (V_I - 500mV)$

$100 = 800 V_I - 400$

$V_I = \frac{5}{8} = 0.625 \Rightarrow V_{OV} = 0.125mV$ Doesn't satisfy

So @ $V_{OV} = 150mV$, Maximum small-signal gain is $\frac{-40}{3}$

$\boxed{\frac{W}{L} = \frac{80}{3}}$

$V_D = V_{DD} - I_D R = 2.5V - 100u \cdot 10k$
$= 1.5V$

$V_{OV} = V_I - V_t$

$150m = V_I - 500m$

$\boxed{V_I = 650mV}$

$\boxed{V_D = 1.5V}$ $\boxed{I_D = 100u}$

b)

Vout

$$V_O + v_o = V_{DD} - \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{OV} + v_i)^2 \cdot R$$

$$= V_{DD} - \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_I - V_{to} + V_i)^2 \cdot R$$

$$V_o = -\frac{2I_D}{V_{OV}} \cdot R \cdot v_i\left[1 + \frac{v_i}{2V_{OV}}\right]$$ ← 2nd order distortion term

$$= \frac{-2I_D}{V_{OV}} \cdot R \cdot V_i - \frac{I_D \cdot R \cdot V_i^2}{V_{OV}^2}$$

$$\text{Ratio} = \frac{-\frac{I_D \cdot R \cdot V_i^2}{V_{OV}}}{-\frac{2I_D \cdot R \cdot V_i}{V_{OV}^2}} = \frac{-I_D \cdot R \cdot V_i^2}{V_{OV}} \cdot \frac{V_{OV}^2}{-2I_D \cdot R \cdot V_i} = \frac{V_{OV} \cdot V_i}{2} < 3.5\%$$

$$V_{OV} = (2 \cdot 0.035)/V_i = 1.4V$$

@ $V_{OV} = 1.4V$

$$100u = \frac{1}{2} \cdot 50u \cdot \frac{W}{L} \cdot 1.4^2$$

$$\boxed{\frac{W}{L} = \frac{100}{49}}$$

$$V_I = V_{OV} + V_t = 1.4 + 500m = \boxed{1.9}$$

$$A_v = \frac{-2I_D}{V_{OV}} \cdot R = \frac{-200u}{1.4} \cdot 10k = \boxed{-\frac{10}{7}}$$

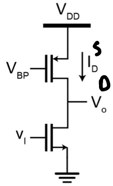
$$V_{DS} = V_{DD} - I_D \cdot R = 2.5 - 100u \cdot 10k$$

$$= \boxed{1.5V}$$

4. PMOS Load [20 pts]

Consider the circuit shown below where the resistor in the previous circuit has been replaced with a PMOS. Assume $k_n' = 80\ \mu A/V^2$, $k_p' = 40\ \mu A/V^2$, $|V_{t0}| = 400$ mV, $V_{DD} = 5.5$ V, $W/L = 1/4$, and $\lambda = 0.1$ 1/V. (Note: The last three parameters are the same for both NMOS and PMOS devices.)

a) For $V_{BP} = 4.5$ V and $V_O = \{0, 1.0, 2.0, 3.0, 4.0, 4.5, 4.8, 4.9, 5.1, 5.2, 5.35 \text{ and } 5.5\}$ V, compute I_D.
b) Sketch I_D vs. V_O from part (a).
c) Repeat parts (a) and (b) for $V_{BP} = 3.5$ V.
d) For a bias point of $V_O = 3.5$ V, use the two adjacent values computed in (a) to construct an equivalent circuit model with a current source (I_{EQ}) and load resistor (R_{EQ}) for the PMOS transistor. One node of the resistor is connected to V_O and the other a bias voltage, V_B chosen such that no current flows through the resistor.



$$i_D = k_p' \frac{W}{L}\left(V_{OV} v_{SD} - \frac{1}{2} v_{SD}^2\right)$$

$$i_D = \frac{1}{2} k_p' \frac{W}{L} V_{OV}^2 (1 + \lambda v_{SD})$$

$V_{SG} = V_S - V_G = 5.5 - 4.5$
$= 1V$

PMOS:

a) $V_{BP} = V_{SG} = 4.5V$ $\quad V_{OV} = V_{SG} - |V_{T0}| = 1 - 0.4 = 0.6$

$V_O = 0V$ $\quad V_{SD} = V_S - V_D = 5.5 - V_O = 5.5V$

$I_D = \frac{1}{2} \cdot 40u \cdot \frac{1}{4} \cdot 0.6^2 \cdot (1 + 0.1 \cdot 5.5) = 2.79uA$

Sat region:

$V_O = 1V$ $\quad V_{SD} = 4.5V$, $I_D = 2.61\ uA$

$V_O = 2V$ $\quad V_{SD} = 3.5V$, $I_D = 2.43\ uA$

$V_O = 3V$ $\quad V_{SD} = 2.5V$ $\quad I_D = 2.25\ uA$

$V_O = 4V$ $\quad V_{SD} = 1.5V$ $\quad I_D = 2.07\ uA$

$V_O = 4.5V$ $\quad V_{SD} = 1V$ $\quad I_D = 1.98\ uA$

$V_O = 4.8V$ $\quad V_{SD} = 0.7V$ $\quad I_D = 1.93\ uA$

$V_O = 4.9V$ $\quad V_{SD} = 0.6V$ $\quad I_D = 1.91\ uA$

$V_{SD} < V_{OV}$, linear region:

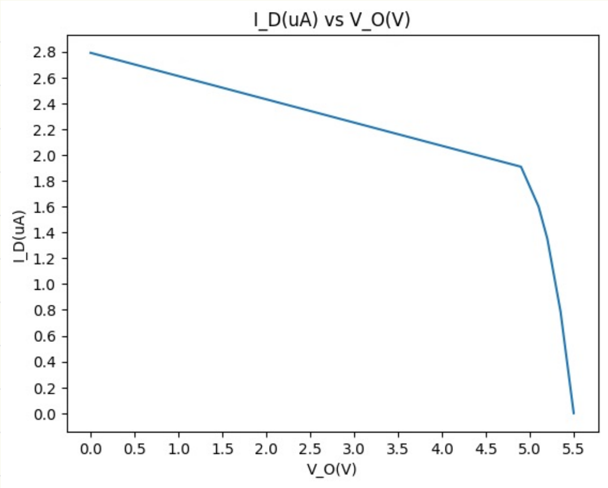
$V_O = 5.1V$ $\quad V_{SD} = 0.4V$ $\quad I_D = 1.6\ uA$

$V_O = 5.2V$ $\quad V_{SD} = 0.3V$ $\quad I_D = 1.35\ uA$

$V_O = 5.35V$ $\quad V_{SD} = 0.15V$ $\quad I_D = 0.79\ uA$

$V_O = 5.5V$ $\quad V_{SD} = 0V$ $\quad I_D = 0\ uA$

b)


I_D(uA) vs V_O(V)
2.8
2.6
2.4
2.2
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
I_D(uA)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
V_O(V)

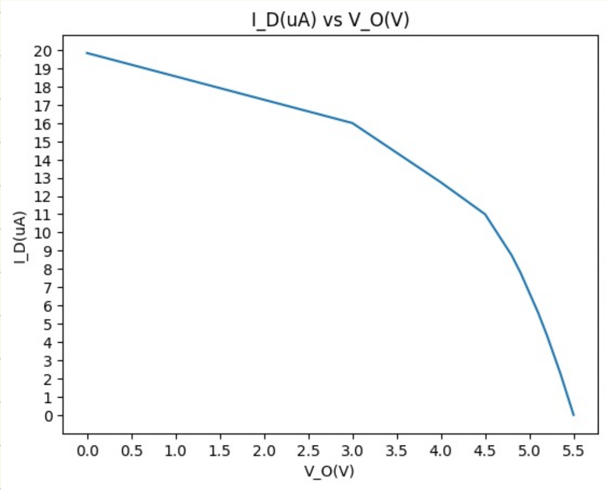
c) $V_{BP} = 3.5V$

$V_{SG} = V_S - V_G = 5.5 - 3.5 = 2V$

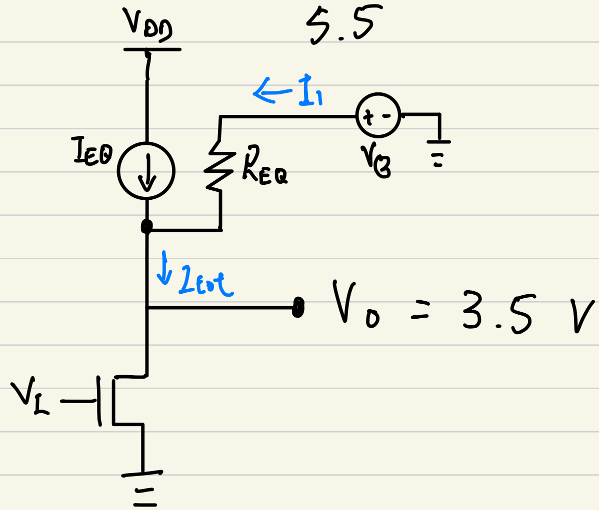
$V_{ov,p} = V_{SG} - |V_{to}| = 2 - 0.4 = 1.6$

	V_O (v)	V_{SD} (v)	I_D (uA)
saturation	0	5.5	19.84
	1	4.5	18.56
	2	3.5	17.28
	3	2.5	16
$V_{SD} < V_{ov}$ Triode region	4	1.5	12.75
	4.5	1	11
	4.8	0.7	8.75
	4.9	0.6	7.8
	5.1	0.4	5.6
	5.2	0.3	4.35
	5.35	0.15	2.29
	5.5	0	0

Plot:



d)



For $V_o = 3.5V$. $I_D = \frac{2.25u + 2.07u}{2} = 2.16uA$

So $\boxed{I_{EQ} = 2.16uA}$

Since no current flows through the resistor, $V_B = V_o = 3.5V$

$I_{tot} = I_1 + I_{Eq} = 0 + 2.16u = 2.16uA$

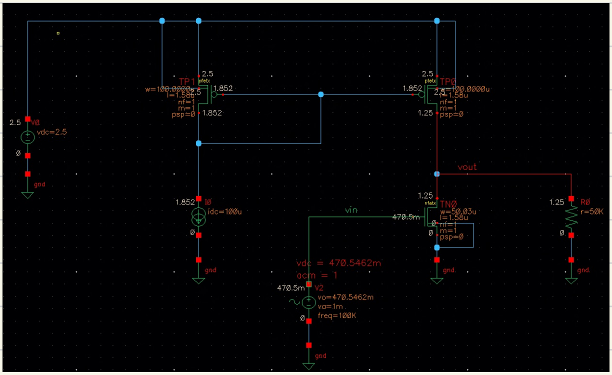
Based on Part A

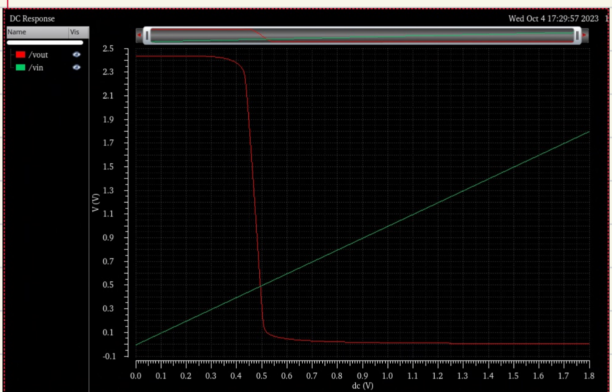
$$R_{Eq} = \frac{\Delta(V_{DD} - V_o)}{\Delta I_D} = \frac{(5.5-4)-(5.5-3)}{2.07u - 2.25u}$$

$$= \boxed{5.\bar{5}\ M\Omega}$$

Q5

Schematic



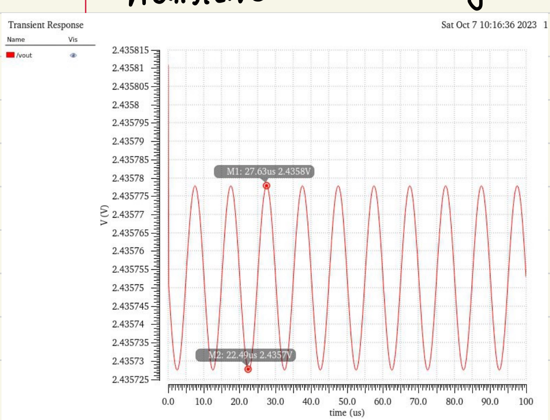


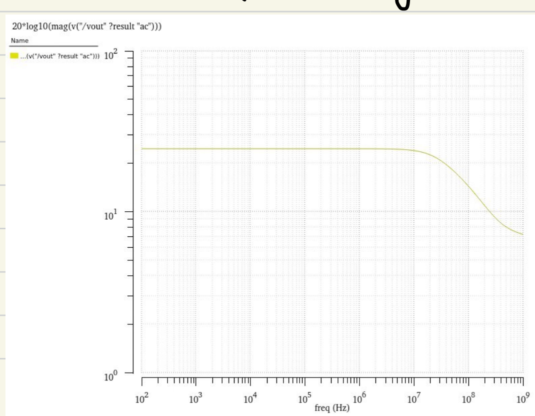
DC Sweep

Transient

$dy = 50uV$ $\quad gain = \frac{50u}{2m} = 0.025$

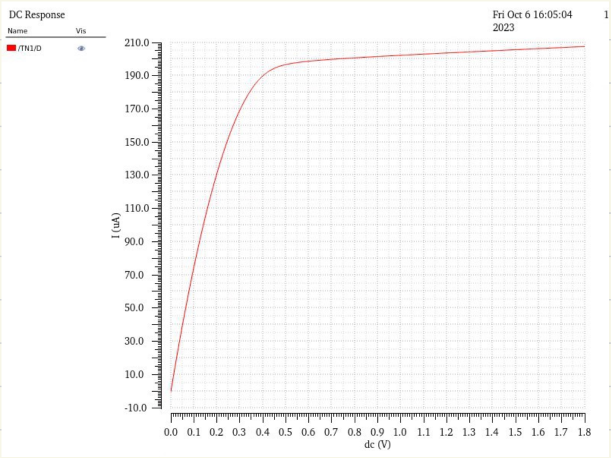
AC Analyses



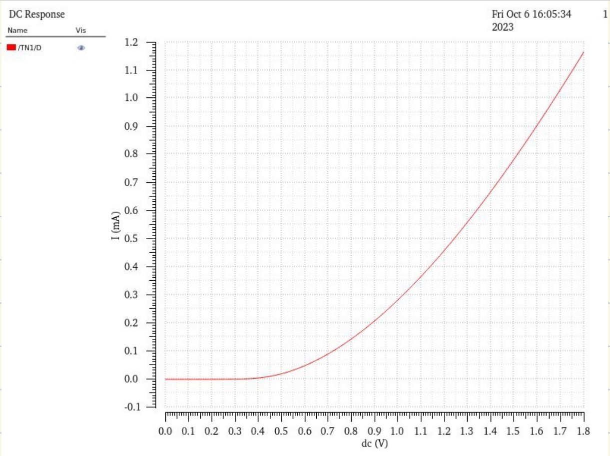


Qb

a)

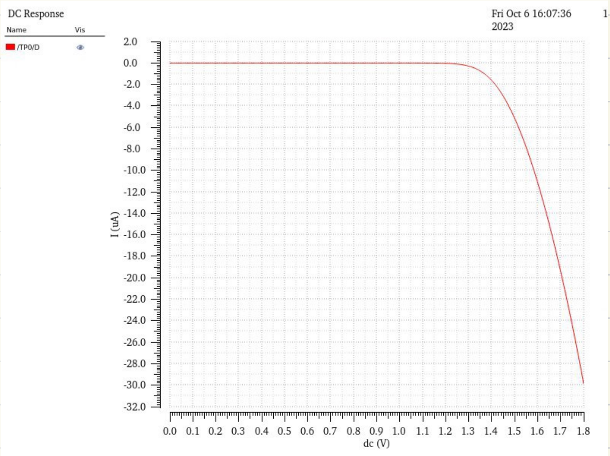


I_D vs. V_{DS}

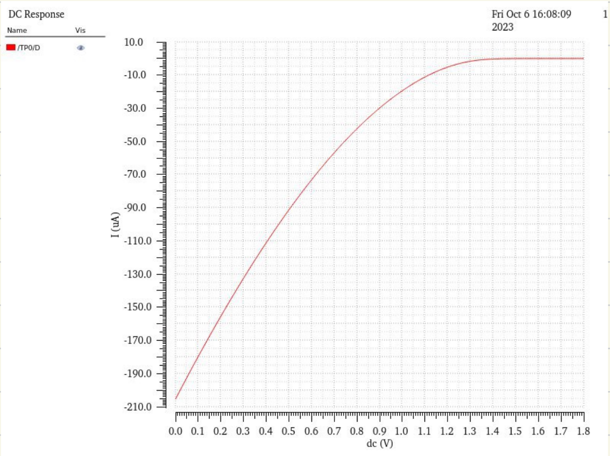


I_D vs. V_{GS}

b)

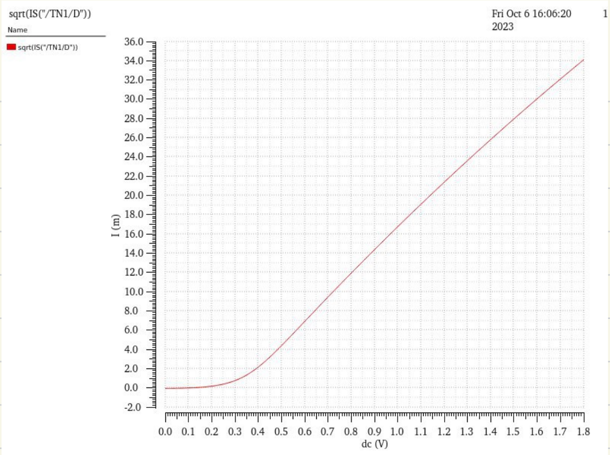


I_D vs. V_{SD}



I_D vs. V_{SG}

c)



NMOS

y: I_D

x: V_{GS}

$$\underbrace{\sqrt{I_D}}_{y} = \underbrace{\sqrt{\frac{1}{2} k_n' \cdot \frac{W}{L} (1+\lambda V_{DS})}}_{k} \cdot \underbrace{(V_{GS} - V_t)}_{x}$$

$$\Downarrow$$

$$y = kx - kV_t$$

$x = 896.4m$ $x = 770.4m$

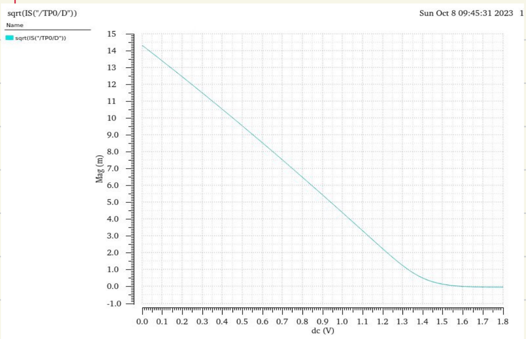
$y = 14.321m$ $y = 11.24m$

$$k = \frac{14.321m - 11.24m}{896.4m - 770.4m} = \frac{1027}{42000}$$

$$14.321m = \frac{1027}{42000} \cdot 896.4m - \frac{1027}{42000} V_t$$

$$\boxed{V_t = 310.7m\ V}$$

c) PMOS



$V_{SG} = V_S - V_G$

$$\underbrace{\sqrt{I_D}}_{y} = \underbrace{\sqrt{\tfrac{1}{2} k_p' \cdot \tfrac{W}{L} (1+\lambda V_{DS})}}_{k} \cdot (\underbrace{V_{SG}}_{x} - V_t)$$

$\Downarrow$

$y = kx - kV_t$

$y = k(x - V_t)$

$-1.354 = x - V_t$

$x = 835.2m \quad x = 669.6\ m$

$y = 6.1352 \quad y = 7.84\ m$

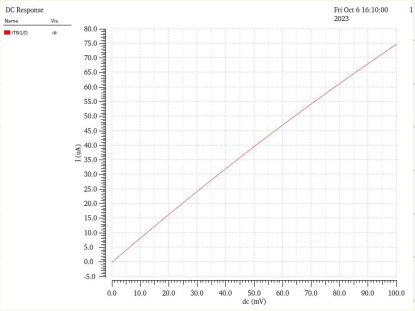
$$k = \frac{7.84 - 6.1352m}{669.6 - 835.2m} = -0.010$$

$6.1352m = -0.010 \cdot 835.2m + 0.010\,V_t$

$$\boxed{V_{t,p} = 1.448\ V}$$

d) From the question, $V_{DS} << 1$. So I plot V_{DS} sweeping from 0 to 100 mV

NMOS



And, the MOS will be in triode region

$x = 14.2\,m$ $\quad$ $x = 47\,m$

$y = 11.73\,u$ $\quad$ $y = 37.402\,u$

$$I_D = \underbrace{k_n' \frac{W}{L} (V_{OV}}_{} \underbrace{V_{DS}}_{x} - \frac{1}{2} V_{DS}^2) \Rightarrow R = \frac{37.402u - 11.73u}{47m - 14.2m}$$

$$I_D = kx - \frac{1}{2}x^2 \qquad = 7.827 \cdot 10^{-4}$$

Since $V_{DS} << 1 \Rightarrow$ the 2^{nd} term $(-\frac{1}{2}x^2)$ can be ignored

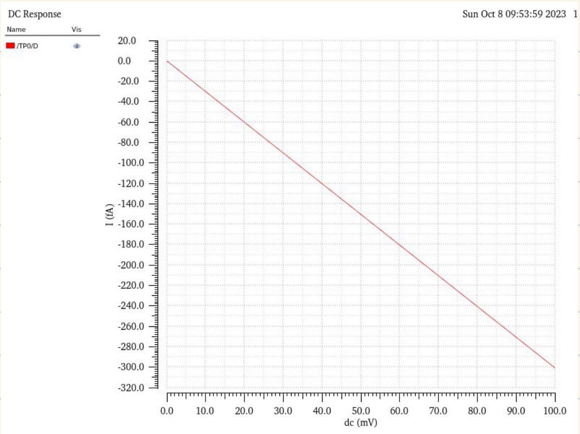
$$k = k_n' \cdot \frac{W}{L} (V_{GS} - V_t)$$

$$7.827 \cdot 10^{-4} = k_n' \cdot 5 \cdot (0.9 - 310.7m)$$

$$k_n' = 2.656 \cdot 10^{-4}\ A/V^2 = \boxed{265.64 \frac{uA}{V^2}}$$

6d) Assumption is the same as PMOS

PMOS $\qquad V_{SD} << |V$



$x = 39.4m \qquad x = 47.6m$

$y = -118.203f \qquad y = -142.803f$

$$I_D = \underbrace{k_n' \frac{W}{L} (V_{ov}}_{k} \underbrace{V_{DS}}_{x} - \frac{1}{2} V_{DS}^2) \Rightarrow R = \frac{-142.803f - (-118.203f)}{47.6m - 39.4m}$$

$$I_D = kx - \frac{1}{2}x^2 \qquad = -3 \cdot 10^{-12}$$

Since $V_{DS} << 1 \rightarrow$ the 2^{nd} term $(-\frac{1}{2}x^2)$ can be ignored

$$k = k_n' \cdot \frac{W}{L} (V_{GS} - V_t)$$

$$-3 \cdot 10^{-12} = k_n' \cdot 5 \cdot (0.9 - 1.448)$$

$$\boxed{k'_{n,p} = 1.09 \cdot 10^{-12} \ A/V^2}$$

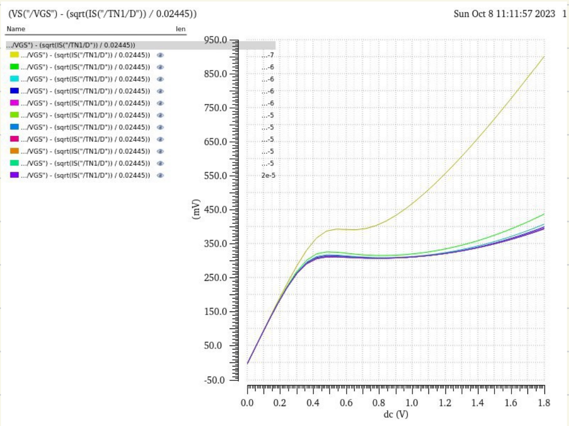
e)

NMOS $$\sqrt{I_D} = \sqrt{\overbrace{\frac{1}{2} k_n' \cdot \frac{W}{L} (1+\lambda V_{DS})}^{k}} \cdot (V_{GS} - V_t)$$

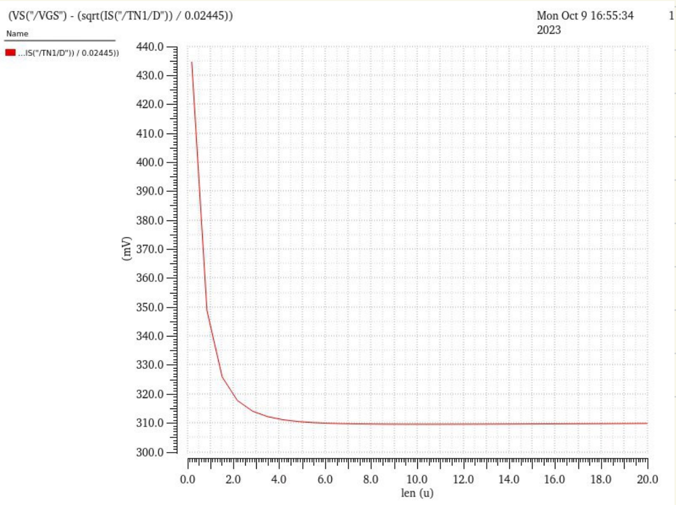
I_D vs. V_{GS} $$y = k(x - V_t)$$

$$V_t = x - \frac{y}{k}$$

$$\boxed{V_{t,n} = V_{GS} - \frac{\sqrt{I_D}}{0.02445}} \longrightarrow \text{from Part C}$$



I_D vs. V_{GS}



$V_{t,n}$ (mV) vs. len (u)

NMOS

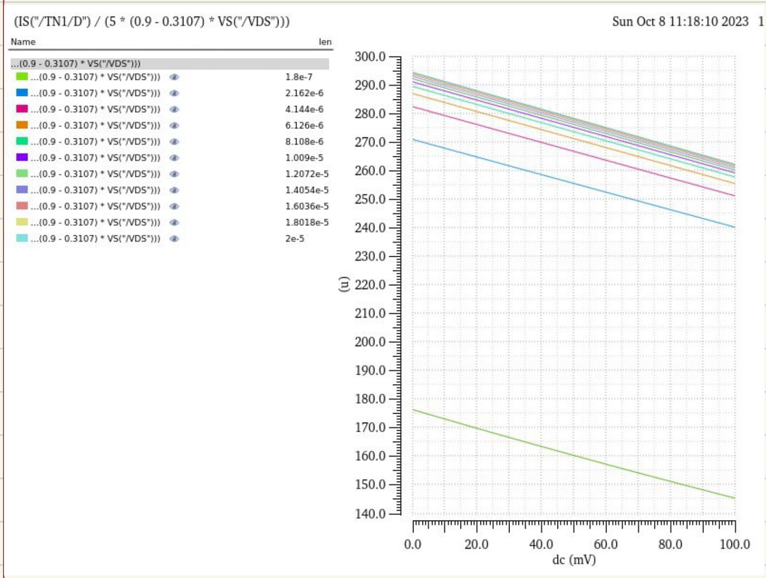
$I_D = \underbrace{k_n' \frac{W}{L} (V_{ov}} \underbrace{V_{ds}}_{x} - \frac{1}{2} V_{DS}^2)$

Assuming $V_{DS} << 1V$

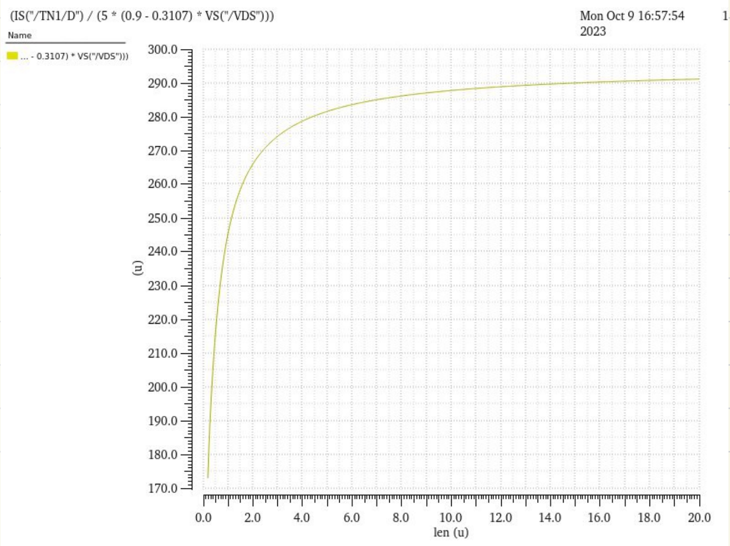
$I_D = kx - \frac{1}{2}x^2$

Ignore the 2^{nd} term

$$\boxed{k_n' = \frac{I_D}{\frac{W}{L} \cdot (V_{GS} - V_t) \cdot V_{DS}} = \frac{I_D}{5 \cdot (0.9 - 0.3107) \cdot V_{DS}}}$$



k_n' vs. V_{DS}



k_n' vs. len

u u

V_{DS} @ 10mV

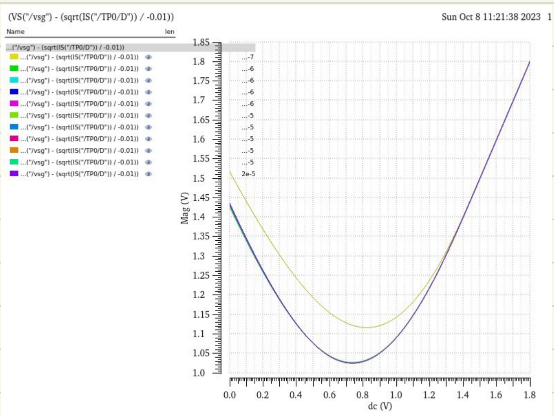
6e) PMOS

$$\sqrt{I_D} = \sqrt{\overbrace{\tfrac{1}{2} k_n' \cdot \frac{W}{L}(1+\lambda V_{DS})}^{k}} \cdot (V_{GS}-V_t)$$

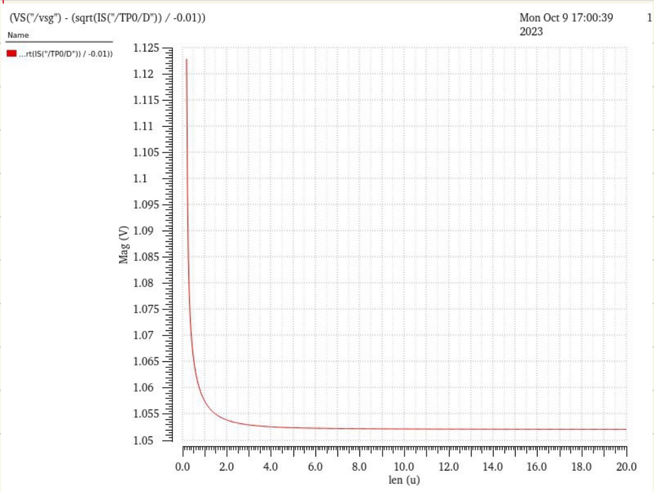
$$y = k(x - V_t)$$

$$V_t = x - \frac{y}{k}$$

$$\boxed{V_{t,p} = V_{SG} - \frac{\sqrt{I_D}}{-0.01}} \rightarrow \text{from Part C}$$



$V_{t,p}$ vs. V_{SG}



$V_{t,p}$ vs. len (u)

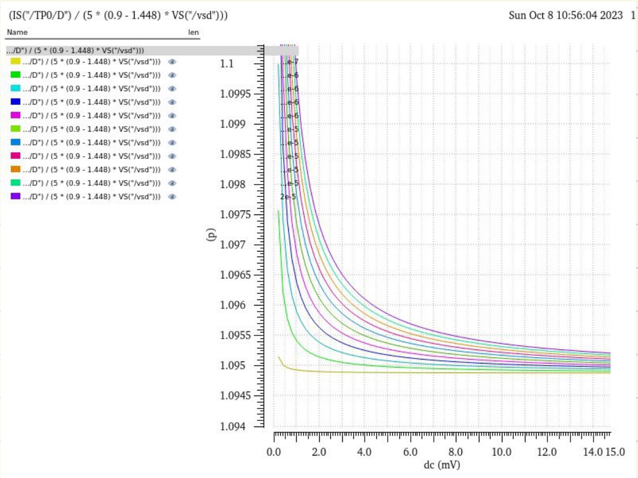
PMOS

k_p'

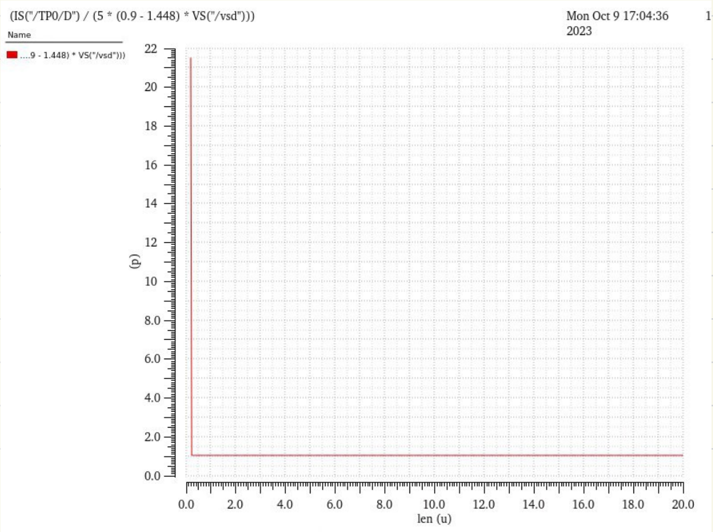
$I_D = \underbrace{k_n' \frac{W}{L} \left(V_{ov}\right.}\underbrace{V_{sd}}_{x} \left. - \frac{1}{2} V_{sd}^2 \right)$ Assuming $V_{DS} << 1V$

$I_D = kx - \frac{1}{2}x^2$ Ignore the 2nd term

$$\boxed{k_p' = \frac{I_D}{\frac{W}{L}\cdot(V_{GS}-V_t)\cdot V_{SD}} = \frac{I_D}{5\cdot(0.9-1.448)\cdot V_{SD}}}$$



k_p' VS. V_{SD}



k_p' vs. len

$\frac{A}{V^2}$ (p) (um)

V_{SD} @ 10mV

6e Conclusion

Beyond 1um, we can tell from all the plots above, we can get a more consisent behavior of $k'_{n,p}$ and $V_{th\,n,p}$.

For both NMOS and PMOS, Vth is higher at 0.18um which cause the device hard to turn on, hard to conduct at lower Vt. And this decrease how much current we can get from the MOS

$k'_{n,p}$ is the lowest at 0.18 um. This affects how much current we can get as well.

In conclusion, at 0.18 um, the current we can get is lower than the MOS which has channel length > 1um.