University of California San Diego
ECE164 - Analog IC Design
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Final Project Report.

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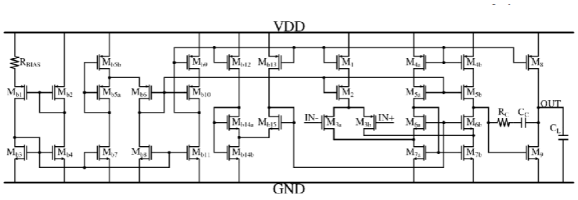

Figure 1: Project Circuit

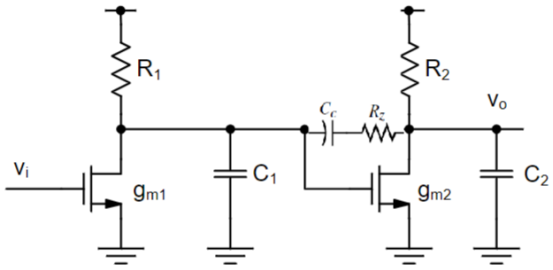

Figure 2: Equivalent Circuit of Two Amplifier Stage

Design Outline

We start our design by reverse engineering from the specs given in the project document. And a few formulas are provided in lecture 10, slide 43. They are listed as follows:

1. $A_{dc} = Av1Av2 \ = \ gm_1R_1gm_2R_2$
2. $w_{p1} \ = -\frac{1}{C_cgm_2R_2R_1}$
3. $w_{p2} \ = -\frac{gm_2}{C_2}$
4. $wc = GBW \ = \ w_{p1}A_v = \ \frac{gm_1}{C_c}$
5. $PM \ = \ 90° - atan\left(\frac{w_c}{w_{p2}}\right)$

And our design approach is as follows:

1. **Frequency Planning:** There are roughly about 4-5 poles in the circuit. There are poles at the output stage of Common Source(CS), at M4, at M6, and at Compensation.
   Our goal is to put the dominant pole at Compensation and the non-dominant pole at the output stage of CS. However, the compensation capacitor C_c will create a Right-half plane zero, which has +20db/dec, and -90 phase/dec. We solve it by using the nulling resistor R_c to move this zero to the $+\infty$. And we can solve gm1 and gm2 from formulas 3-5
2. **Gain Partitioning:** We plan to put more gain in the Folded Cascode(FC) stage 50dB, and CS stage 20dB
3. **Sizing:** Since the gm is known from the step 1 and step2, we use the "Constant Overdrive Voltage(V_{ov})" to find the required I_d for each stage.($I_D = \ \frac{gm \cdot V_{ov}}{2}$), and also the size $\frac{W}{L}$ of each transistor.
4. **Simulation:** After getting the current of each branch and size of transistors, the simulation will be conducted based on values from the hand-analysis

5. **Bias sizing:** In order to keep transistors in the saturation, the bias sizing also needed to be modified accordingly.

6. **Constant gm sizing + Current Mirror:** The magic battery will be known from previous steps. So, we can size the current mirror stage accordingly to get the voltage we need.

7. **Simulation+Final Tweaks:** There would be some discrepancies. So, we need final tweaks to ensure the required specs are satisfied.

Schematic of Final Design

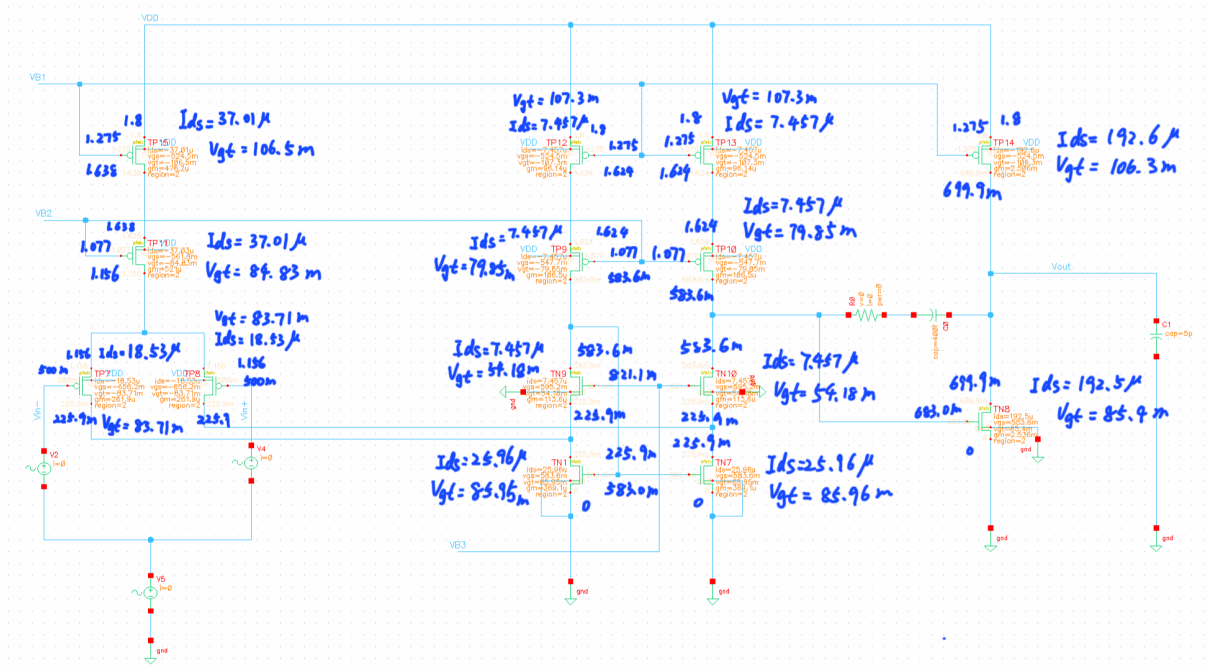

Figure 3: Folded Cascode and Common Source Op

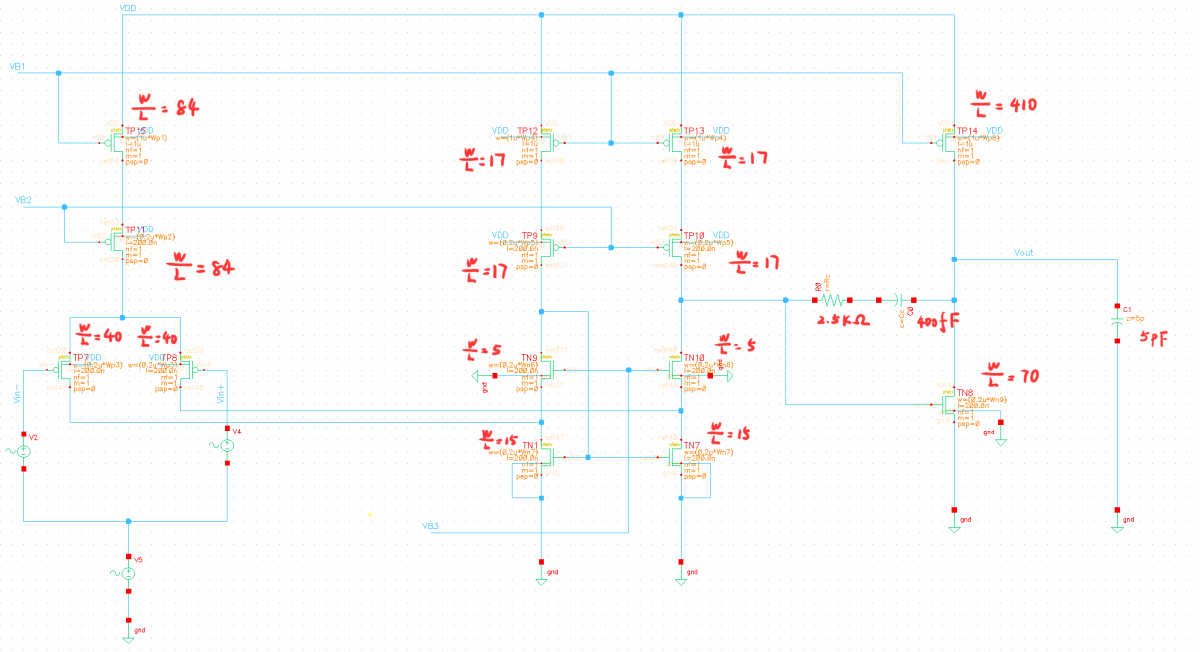

Figure 4: Folded Cascode and Common Source Specs

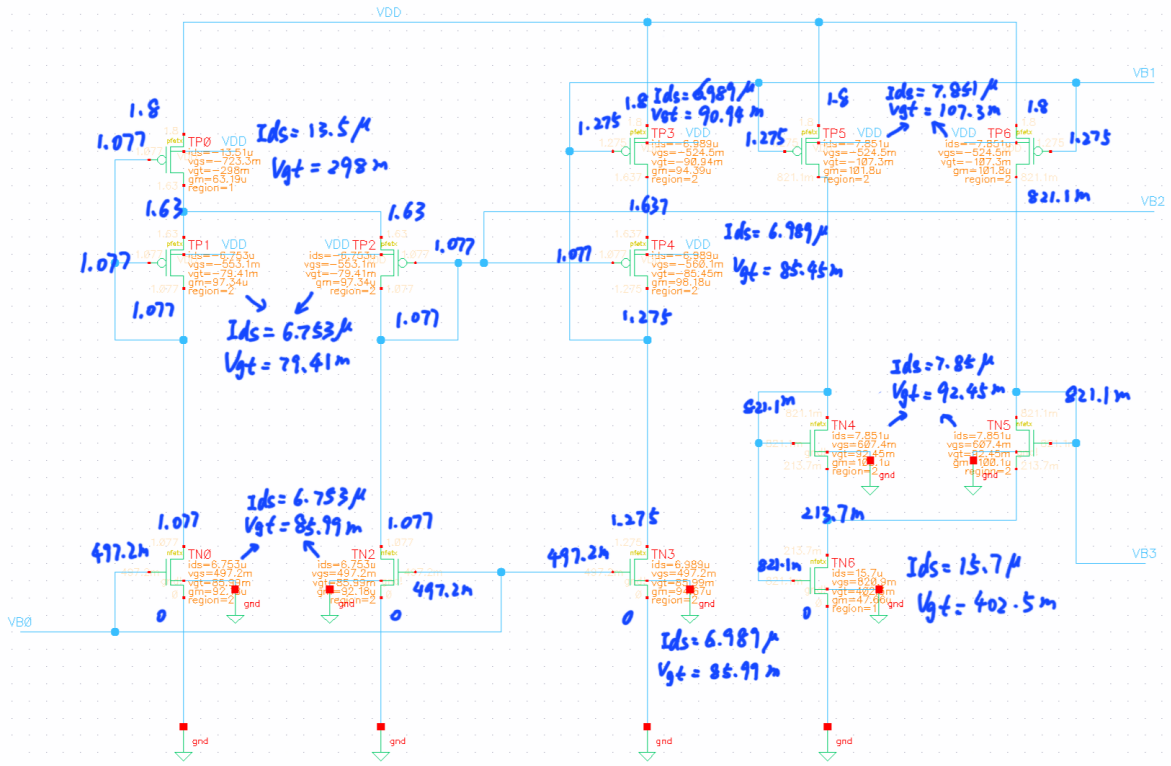

Figure 5: Current Mirror Op

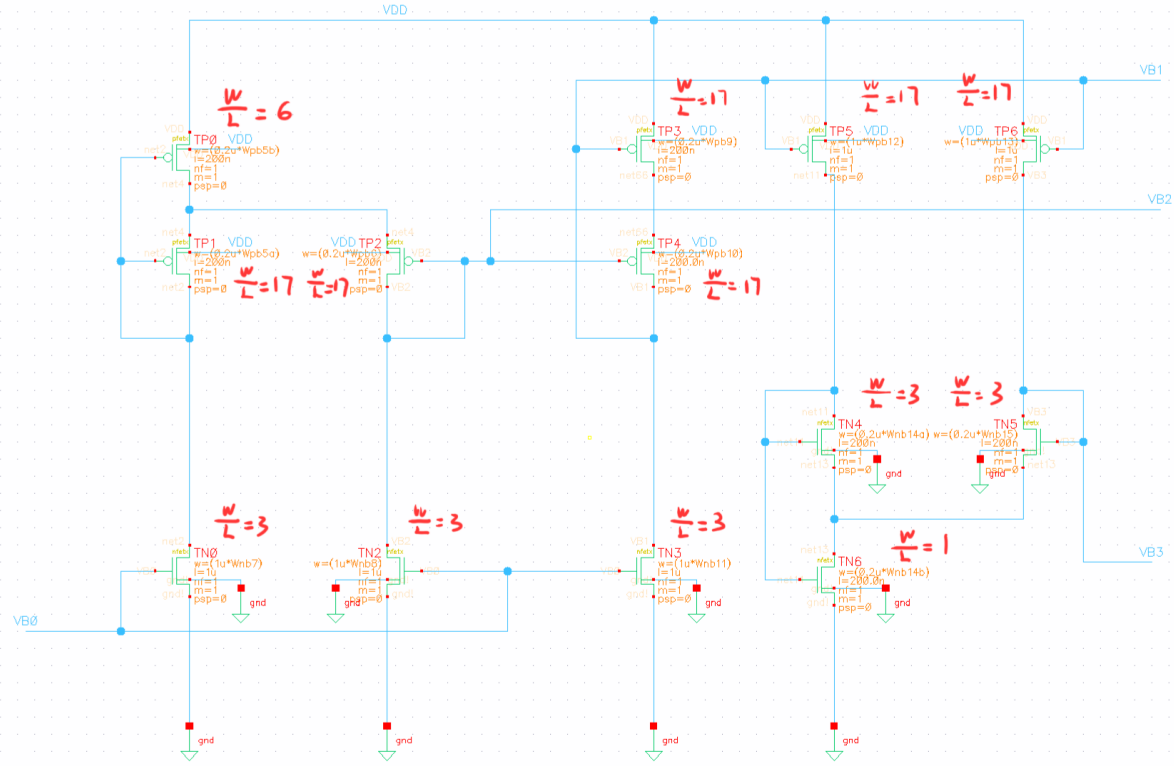

Figure 6: Current Mirror Spec

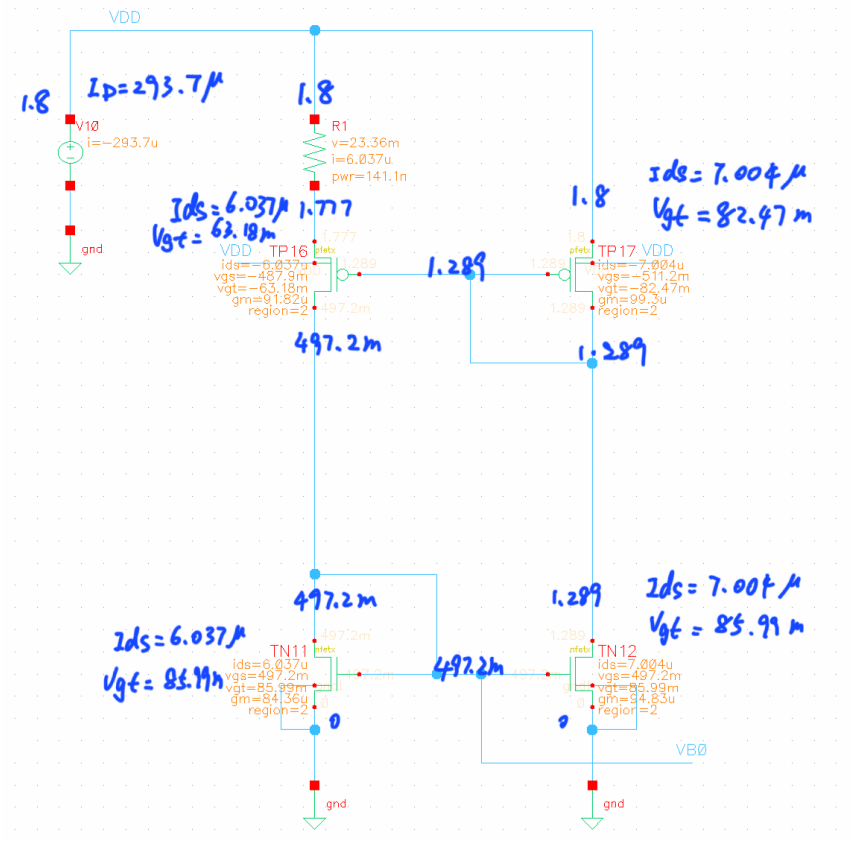

Figure 7: Current gm Op

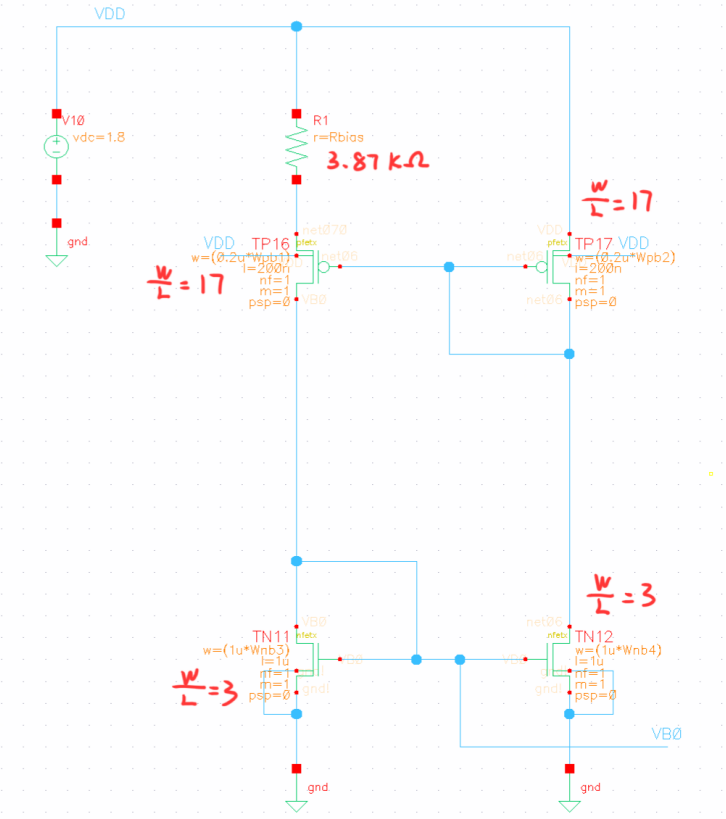

Figure 8: Current gm Spec

Calculate key design parameters

CS + FC Stage gm, I_D, ratio

1. Calculate w_{p2}: $PM = 90° - atan\left(\frac{w_c}{w_{p2}}\right)$. In this formula, w_c = 60MHz, PM = $65°$. The result of w_{p2} is 0.808GHz, and f_{p2} is 0.129GHz
2. Calculate gm_2: $w_{p2} = -\frac{gm_2}{C_2}$. w_{p2} is known from step 2). And C_2 is given as 5pF. The result of gm2 ($gm_2 = C_2 \cdot w_{p2}$) is 4ms
3. Calculate the I_D flow through CS(M_8, M_9) stage: Assuming V_{ov} is 0.2V, the result of $I_{D_{89}}$ = $\frac{gm_2 \cdot Vov}{2}$ = 400uA
4. Calculate gm_1: $w_c = GBW = w_{p1}A_v = \frac{gm_1}{C_c}$. Assuming C_c is 1pF, w_c is known from the specs. The result of gm1 is 377us.
5. Calculate the I_D flow through (M_3) and (M_1, M_2)stage: Assuming V_{ov} is 0.2V, the result of I_{D_3} = $\frac{gm_1 \cdot Vov}{2}$ = 37.6uA. And I_{tail} = $I_3 \cdot 2$ = 75.4uA.
6. Calculate the I_D flowing through (M_4 - M_6) stage: we set the slew rate to be 5. So the current flows into (M_4 - M_6) is 0.2 · I_3 = 7uA
7. Calculate sizing of CS Stage $\left(\frac{W}{L}\right)_{89}$: by square law $I_D = \frac{1}{2} \cdot Knp \cdot \frac{W}{L} \cdot V_{ov}^2$
8. Calculate sizing of FC Stage $\left(\frac{W}{L}\right)_{4-6}$: by square law $I_D = \frac{1}{2} \cdot Knp \cdot \frac{W}{L} \cdot V_{ov}^2$
9. Size of M_7: The current flows into M_7 is the sum of $I_3 + I_6$, and by square law, we can find the ratio from there. After simulation, we found the ratio of M_7 also determined the operating region of M_8 and M_9. So, Little tweaks are needed to bring M_8 and M_9 into saturation region.
10. Calculate Rc: $\frac{1}{gm_2}$ = 250 ohm

Current Mirror Current, gm, R and Ratio

1. Current flow into each branch: we used the current flowing into FC stage as the reference current(I_D) for the current mirror stage. So every transistor in the saturation should have $I_{D3} = 7uA$
2. Current Exception and Operating Region Exception: Transistor M_{b5b} and M_{b14b} takes 2 times current of I_{D3}. They are both part of the magic battery. And these two transistors work in the triode region. So, $I_D = K_{np} \cdot \frac{W}{L} \cdot \left(V_{ov} \cdot V_{DS} - \frac{1}{2}V_{DS}^2\right)$ will be used to calculate the $\frac{W}{L}$
3. Essentially, these current mirror works as a magic battery to bias the FC and CS stages. After simulation, we may need some little tweaks to adjust the V_B out of this Current mirror Stage

Constant gm, Ratio

1. Calculate gm_{b1}: $gm_1 = \frac{2I_D}{V_{ov}}$. From this formula, the I_D is known, which is I_{D4}. V_{ov} is 0.2. We get from our MatLab script is 70uS.

2. Calculate R_{bias}: $gm_1 = \frac{2 \cdot \left(1 - \frac{1}{\sqrt{m}}\right)}{R_{bias}}$. gm_1 is known from step 1), and we set the "m factor" to be 4. So the result of R_{bias} is 14k

3. Calculate $\frac{W}{L}$: The Ratio of M_{b3} and M_{b4} are the same as M_{b7} and M_{b8}, since M_{b7} and M_{b8} need to duplicate the current generated by the constant gm circuit.
   The ratio of M_{b2} is calculated by square law.
   So the ratio of M_{b1} is $m \cdot \frac{W}{L}_2$

Power Consumption

1. I_{D4} = 7uA

2. Current in each stage:
   Constant gm: $2I_{D4}$
   Current mirror: $2I_{D4}$ + I_{D4} +I_{D4} +I_{D4} = $5I_{D4}$
   Folded Cascode: 2 I_{D4} + $10I_{D4}$ = $12I_{D4}$
   Common Source: $25I_{D4}$
   Total I_{D4} = $49I_{D4}$

3. Power Consumption: $V_{DD} \cdot I_{tot}$ = 1.8 · 34 · 7uA = 617.4uW.

Hand Calculation vs.Final Spice values

Variables	Hand Calculation	Simulation
Power dissipation	491.4uW	617.4uW
$gm_1(gm_3)$	377uS	261uS
$gm_2(gm_9)$	4mS	2.536mS
I_{D1-2}	75.4uA	37uA
I_{D3}	37.6uA	18.53uA
I_{D4-6}	7uA	7.457uA
I_{D7}	44.6uA	25.96uA
I_{D8}	400uA	192.5uA
I_{D9}	400uA	192.5uA
R_c	250 ohm	2.5k ohm
C_c	1pF	400fF
R_{bias}	14k	3.87k
gm_{b1}	150mS	99.3uS
m	4	4

Table 1: Hand Calculation vs.Final Spice values

Discrepancies

As seen in the table above, we can see the current doesn't really match the Hand-calculation results. This is probably because we are using the ideal model to find the current, i.e., the square law model. And most of the length of the transistors(except current mirror transistors) we use is 200nm. This put the entire circuit far away from the ideal model.

Before changing to 200nm, we used 1um for all the transistors, which introduces lots of parasitic effects into the Folded Cascode stage. These parasitic effects constrain the phase margin in our first-pass design and further increase the output resistance of each amplifier stage.

Because of the lower I_D, the discrepancies of gm in all devices are reasonable. Based on the formula gm: $gm = \frac{2I_D}{V_{ov}}$, I_D is increased more than the amount of V_{ov} decreasing. So, the discrepancies of gm are not that significant compared to the I_D

Another discrepancy is the V_{ov} of most of the transistors. Our hand calculations used 0.2V as V_{ov}. But 0.11-0.12 V are seen in our simulation. This is because the transistor is trying to maintain the same current flowing into the devices, and the ratio remains unchanged as well. The only way for this device to remain in saturation is to decrease the V_{ov}. And it turns out what we've seen in the circuit.

Lastly, the discrepancies in power dissipation are also predictable. The hand analysis of power consumption is based on the ideal current assumption. However, in the real simulation, each branch gets a lower current than what we estimated in the hand analysis due to second-order and non-ideal effects in each device.

Bode Plot Simulation Results

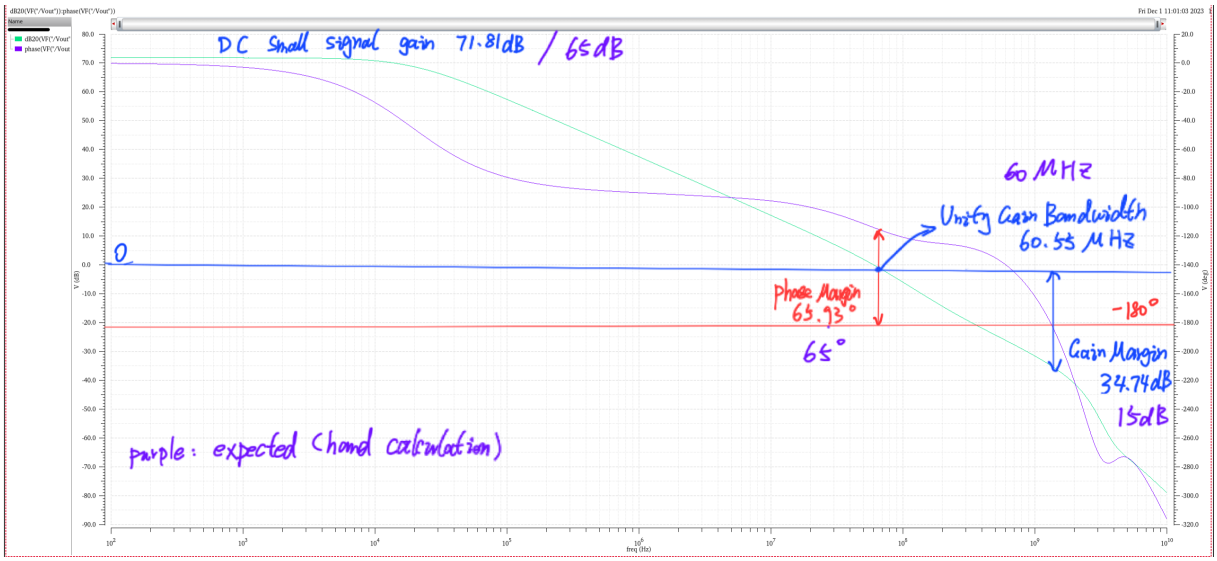

Figure 9: Current Mirror Op

Transient simulation

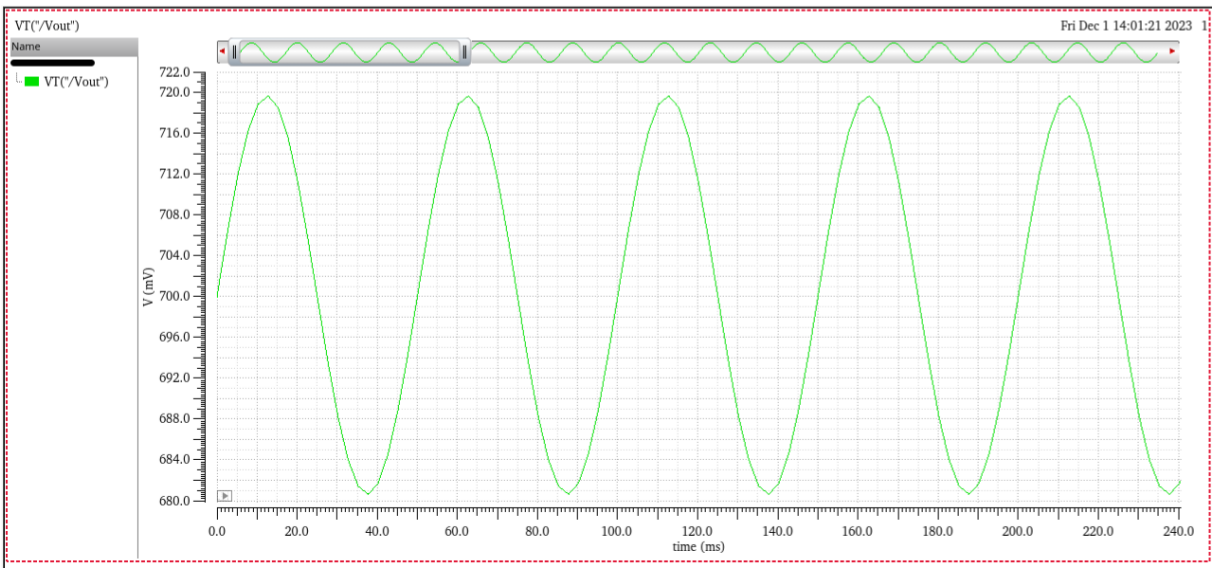

Figure 10: Transient simulation for u 10u V_{pp} sinusoid at 20 Hz

Comments and conclusions

In conclusion, we finished the design by splitting whole circuits into five parts: constant gm, current mirror bias, folded cascode, frequency compensator, and common source. We do the design by working reversely from a common source and folded cascode. After we meet all requirements in these two stages, we use the three bias voltages to design the current mirror bias and finally constant gm. During the hand calculations, we didn't include the parasitic capacitors of the transistors, which led to the discrepancy in the final simulation. The simulated CC is larger than our calculation. Another discrepancy is the current; many terms are ignored because we use the simplified I_D(sat) to calculate our size ratio. As a result, when we use the calculated size ratio in simulation, the current is lower than our calculation.
This project taught us how to adjust the phase margin by knobing the compensation capacitor and nulling the resistor. When we increase the CC, w_{p2} will increase, then the phase margin will also increase. By setting $R_c = \frac{1}{gm_9}$, we move the additional zero caused by CC to $+\infty$, thus mitigating the impact of the zero. However, we didn't learn how to mitigate the zero impact with pole-zero cancellation. We also learned how to improve the power consumption by adjusting the current through the current mirror bias. We set the $Iref = I_{4a}$, which is the lowest current branch in the folded cascode circuit.