ECE260A Lab2

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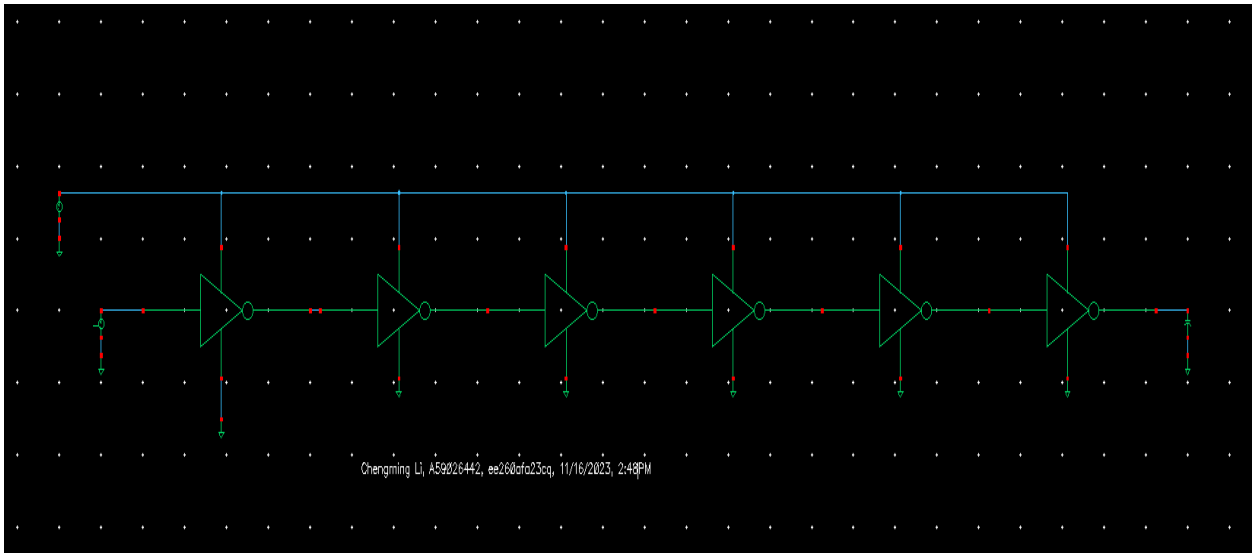
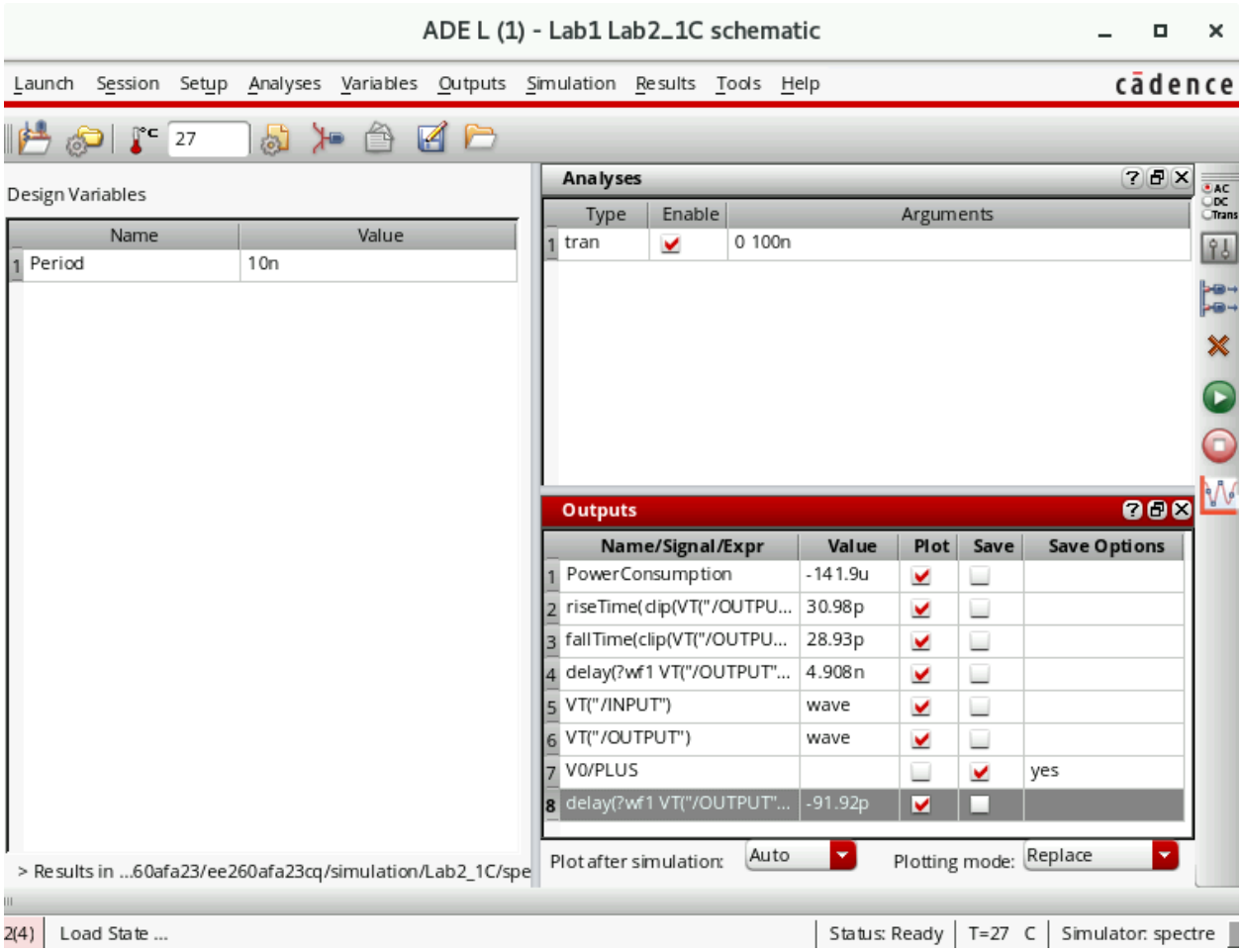
1. Optimal Delay
   a. F = GBH, H = Cout/Cin = 500f/1f*(0.09+0.135) = 2222.2
   Given fastest path when effort delays are about 4
   Best # of stages = log_4(2222.2) ~= 6
   b. It should offer the same equal rise and fall propagation delays, because we are using unit inverter, which gives us the same equal rise and fall time.
   c.

N	f	tpdf(s)	tpdr(s)	tpd(s)	Power(W)	PDP(W*s)	EDP(J*s)
1	2222.2	6.482n	6.382n	6.40n	19.9u	1.27e-13	8.15e-22
2	47.14	174.6	183.5p	208.3p	54.6u	1.137e-14	2.37e-24
3	13.05	52p	54.17p	105.7p	63.81u	6.74f	7.13e-25
4	6.866	30.88p	33.12p	86.45p	77.86u	6.96f	6.02e-25
5	4.67	26.17p	29.66p	85.9p	101.6u	8.73f	7.5*e-25
6	3.612	28.93p	30.98p	91.92p	141.9u	1.3e-14	1.2*e-24

N = 5 will be the one I use, because it gives the lowest delay as shown in the table. This is not the same as my answer in

part a). Because the answer from part a) is an ideal model, which didn't take into account the effects of a nonideal case.





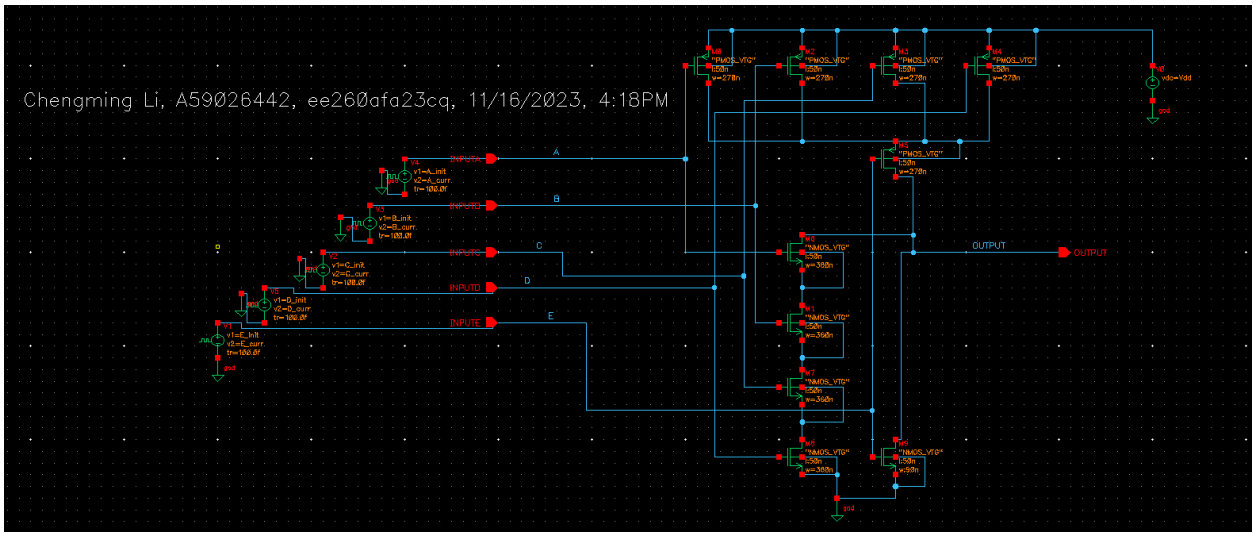
2. A Complex gate
    a. Yes, ~((ABCD)+E)
    b. Yes, since both circuits have the same transistors' size
    c. ABCDE = 1, Req = 7.5k
    d. input patterns (A–E) give the lowest output resistance when the output is high : ABCDE = 0; Req = 9.375k; worst-case output resistance when the output is high: 15k
    e. Best case: plh = 1.125ns, phl = 0.9ns
       Worst case: 1.8ns
    f. Circuit B is better
       Because Input E will be the last input to arrive, In the pull up case, all the other inputs get a chance to charge and wait for E to come in. Comparing to Circuit A, all the other inputs can' charge until arrival of E

       Body effects will increase the Vt. In the circuit A, ABCD's body connect to the Drain of PMOS E, and because of the body effect, it slows down the conduction of 4 Transistors compared to the conduction of 1 Transistor in Circuit B
    g. Slowest tplh happens when
       Previous Input ABCDE = 11110
       Current Input ABCDE = 11100
       As A and D are the two farthest nodes from VDD, the longer distance also contributes to the increase of parasitic Capacitance. And the slowest path occurs when the farthest node switches last.

       Slowest tphl happens when
       Previous Input ABCDE = 11100
       Current Input ABCDE = 11110

Longest Path happens when outer transistor switches last. And the other transistor can't discharge until the outer transistor is connected to the GND

h. It matches what I got from part g)



ADE L (3) - Lab1 Lab2_2h schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help cadence

Design Variables

	Name	Value
1	A_curr	1
2	A_init	0
3	B_curr	1
4	B_init	1
5	C_curr	1
6	C_init	1
7	D_curr	1
8	D_init	1
9	E_curr	0
10	E_init	0
11	Vdd	1

> Results in ...60afa23/ee260afa23cq/simulation/Lab2_2h/

Analyses

	Type	Enable	Arguments
1	tran	✓	0 10n

Outputs

	Name/Signal/Expr	Value	Plot
3	delay(?wf1 VT("/OUTPUT") ?value1 0.5 ?edge1 "risi...		✓
4	delay(?wf1 VT("/OUTPUT") ?value1 0.5 ?edge1 "falli...		✓
5	delay(?wf1 VT("/OUTPUT") ?value1 0.5 ?edge1 "falli...		✓
6	delay(?wf1 VT("/OUTPUT") ?value1 0.5 ?edge1 "falli...	-7.366p	✓
7	delay(?wf1 VT("/OUTPUT") ?value1 0.5 ?edge1 "falli...		✓

Plot after simulation: Auto Plotting mode: Replace

5(20) Edit Variables ... Status: Ready T=27 C Simulator: spectre

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	ee260afa23cq	ChengmingLi	11/16/2023	4:34 PM											
2															
3			Init Condition						Curr Condition				Pull Up		Pulldown
4	Pull Up														
5	A	B	C	D	E		A	B	C	D	E				
6	1	1	1	1	0		0	1	1	1	0		10.11ps		
7	1	1	1	1	0		1	1	1	0	0		16.52ps	← slowest	
8	1	1	1	0	1		1	1	1	0	0		10.8ps		
9	0	1	1	1	1		0	1	1	1	0		4.647ps		
10															
11															
12	Pull Down														
13	1	1	1	0	0		1	1	1	1	0		slowest		11.45ps
14	1	1	1	0	0		1	1	1	0	1				7.841ps
15	0	1	1	1	0		1	1	1	1	0				7.366p
16															
17															
18															
19															
20															

Hand Analysis

Q2 Q3 Q4

Q2

a) Yes. $\boxed{\overline{(ABCD)+E}}$

b) Yes, since both circuits have the same transistors' size

c) sizeing $\frac{P}{N} = \frac{3}{1}$.

The Worst Pulldown is

$ABCD = 0 \quad E = 1 \quad \frac{R}{1} = 15k$

Worst PULLUp is

$ABCD = 0111 \quad E = 0 \quad \frac{3R}{6} + \frac{3R}{6} = R = 15k$

Give the lowest output resistance when output is Low

$\boxed{ABCDE = 1}$

$Req = R \parallel R = \frac{1}{2}R = \boxed{7.5k}$

d) Worst PULLUp is

$ABCD = 0111 \quad E = 0 \quad \frac{3R}{6} + \frac{3R}{6} = \boxed{R = 15k}$

Give the lowest output resistan when output is High

$\boxed{ABCDE = 0}$

$Req = \frac{3R}{6} \parallel \frac{3R}{6} \parallel \frac{3R}{6} \parallel \frac{3R}{6} + \frac{3R}{6} = \frac{R}{8} + \frac{3R}{6} = \frac{5}{8}R$

$= \boxed{9.375k}$

e)

Best case

$P_{LH} = R_{out} \cdot C_L = 9.375k \cdot 120f = \boxed{1.125ns}$

$P_{HL} = 7.5k \cdot 120f = \boxed{0.9ns}$

Worst Case

$P_{LH} = P_{HL} = 15k \cdot 120f = \boxed{1.8ns}$

f) Circuit B is better

Because Input E will be the last input to arrive,
In the pull up case, all the other inputs get chance to charge and waiting for E to come in
Compored to Circuit A, all the other inputs can't charge before arrivia of E

Body Effects will increase the V_T (threshold voltage)
In the circuit A, ABCD's body connect to the Drain of PMOS E. and because of the body effect, it slows down the conduction of 4 Transistors compored to 1 transistor in Circuit B

g)

Slowest t_{plh} (pull up) happens when

previous Input					Current Input				
A	B	C	D	E	A	B	C	D	E
1	1	1	1	0	1	1	1	0	0

As A or D are the two forthest node from V_{DD}, the longer distance also contribute to the increase of parasitic Capacitance

And the slowest path occurs when the forthese node switches last.

Slowest t_{phl} (Pull down)

Previous Input					Current Input				
A	B	C	D	E	A	B	C	D	E
1	1	1	0	0	1	1	1	1	0

Longest Path happens when outer transistor switches last.

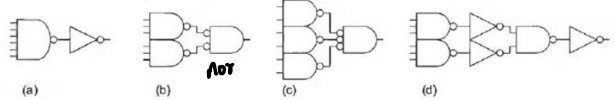
And the other transistor can't discharge until outer transistor is connected to GND

Q3

Problem 3. Hand Analysis

Consider three designs of a 6-input AND gate shows in the following figure. Derive an expression for the delay of each path if the path electrical effort is H. What design is fastest for H=1? H=10? H=25?

$\overline{A}\cdot\overline{B} = \overline{A+B}$ $\overline{A}\cdot\overline{B}\cdot\overline{C}$



Assuming 2:1 size

a) $F = G\cdot B\cdot H$ $\quad B=1 \quad H=1$

$G = \frac{6+2}{3}\cdot 1$

$F : \frac{8}{3}\cdot H$ $\quad D = \hat{N} F^{\frac{1}{N}} + P = \boxed{2\cdot\sqrt{\frac{8}{3}H} + (6+1)}$

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b) $G = \frac{3+2}{3}\cdot\frac{2+2}{3} = \frac{5}{3}\cdot\frac{4+1}{3} = \frac{25}{9}$

$F = \frac{25}{3}H$

$D = 2\cdot\sqrt{\frac{25}{9}H} + 3+2 = \boxed{2\sqrt{\frac{25}{9}H} + 5}$

---

c) $G = \frac{4}{3}\cdot\frac{7}{3}$ $\quad B=1 \quad H$

$F = \sqrt{\frac{28}{9}H}$

$D = \boxed{2\cdot\sqrt{\frac{28}{9}H} + 5}$

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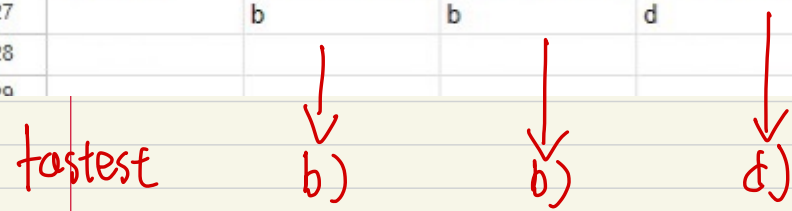
d) $G = \frac{5}{3}\cdot 1\cdot\frac{4}{3}\cdot 1$ $\quad B=1$

$F = \left(\frac{20}{9}H\right)^{\frac{1}{4}}$

$D = 4\cdot\left(\frac{20}{9}H\right)^{\frac{1}{4}} + (3+1+2+1) = \boxed{4\cdot\left(\frac{20}{9}H\right)^{\frac{1}{4}} + 7}$

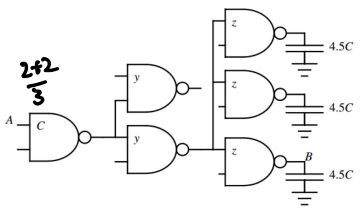
19			H	
20		1	10	25
21	a	10.26598632	17.32795559	23.32993162
22	b	8.333333333	15.54092553	21.66666667
23	c	8.527668415	16.15546702	22.63834207
24	d	11.88378867	15.68474083	17.92048345
25				
26	MinDelay	8.333333333	15.54092553	17.92048345
27		b	b	d
28				
29				



Q4

Problem 4.Hand Analysis

Optimize the circuit in the figure below to obtain the least delay along the path from A to B when the electrical effort of the path is 4.5.



$H = 4.5$

$\frac{y+y}{y} = 2$ $\frac{z+z+z}{z} = 3$

$F = GBH$

$= \left(\frac{4}{3} \cdot \frac{4}{3} \cdot \frac{4}{3}\right) \cdot (2 \cdot 3) \cdot 4.5$

$= \frac{64}{27} \cdot 6 \cdot 4.5 = 64$

Best stage effort $\hat{f} = (64)^{\frac{1}{3}} = 4$

Stage 3

$$z = \frac{4.5C \cdot \frac{4}{3}}{4} = 1.5C$$

Stage 2

$$y = \frac{1.5C(x3) \cdot \frac{4}{3}}{4} = 1.5C$$

Stage 1

$$C = \frac{1.5C(x2) \cdot \frac{4}{3}}{4} = \frac{4C}{4} = C$$

$y = 1.5C \quad z = 1.5C$