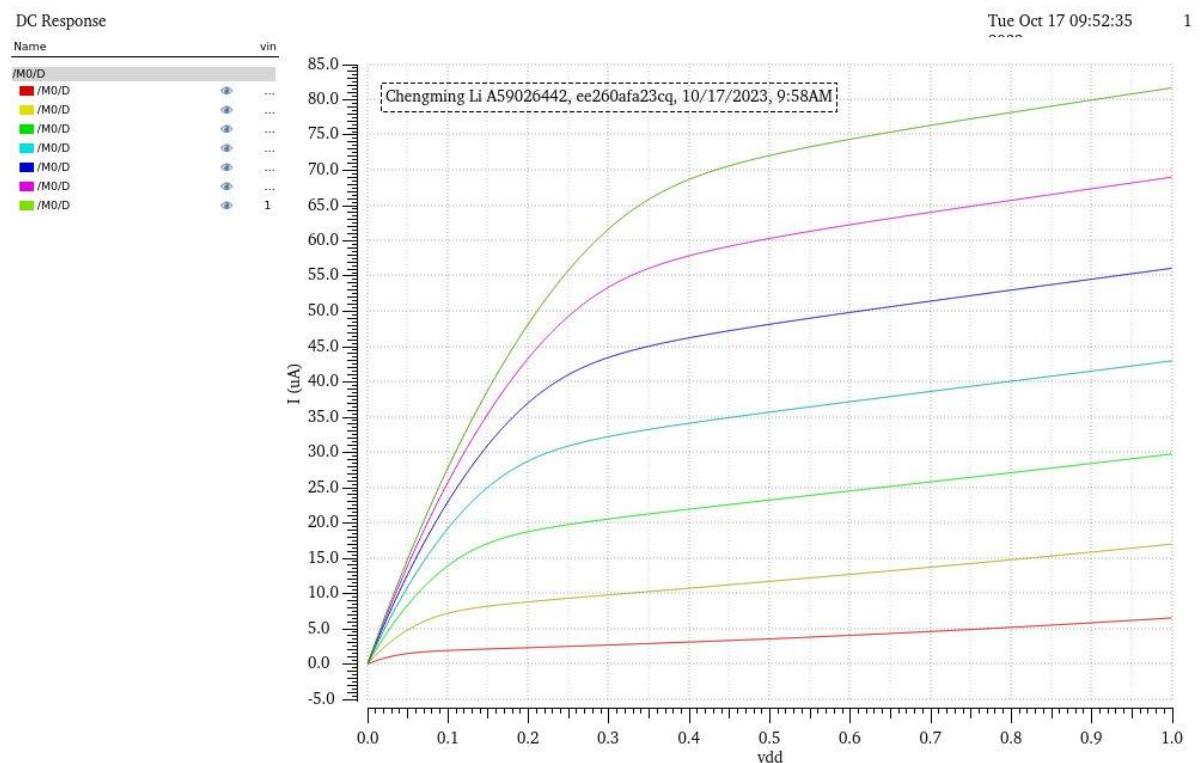


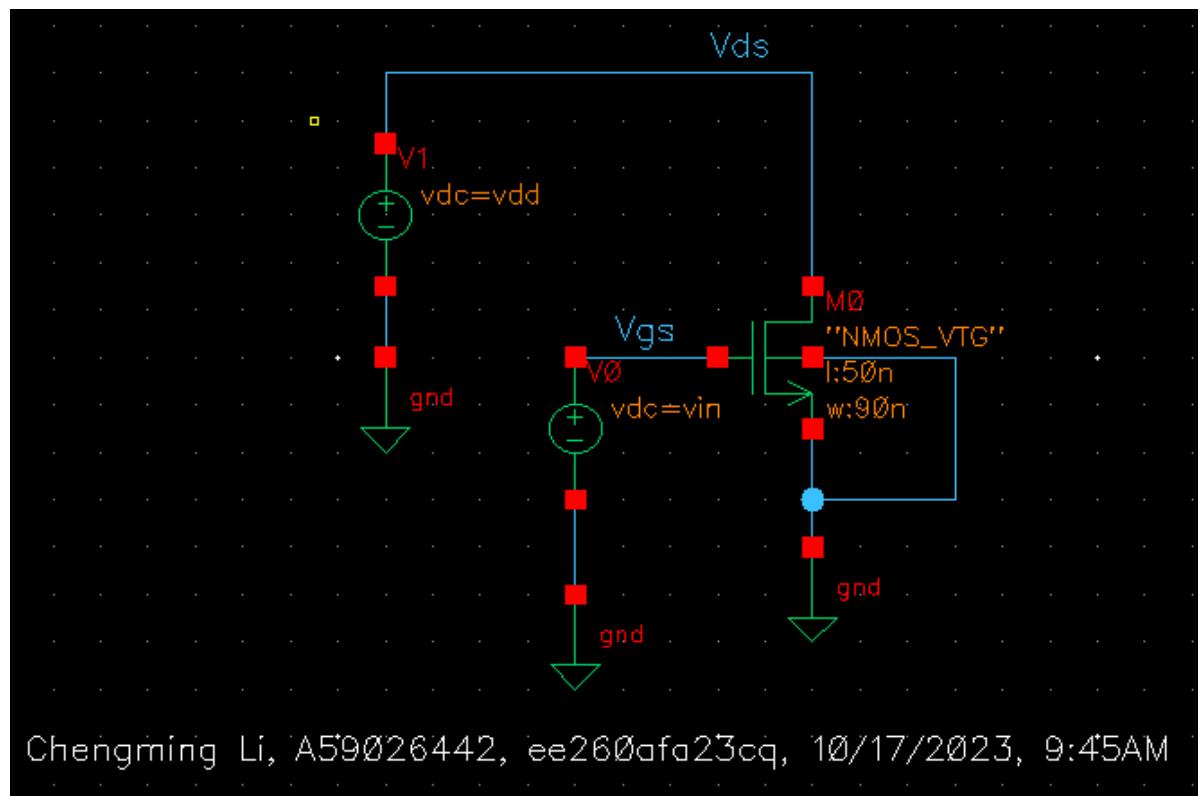
ECE260A VLSI Lab1
Chengming Li A59026442 ee260afa23cq 10/27/2023 1:43PM

1. Problem 1

[a]

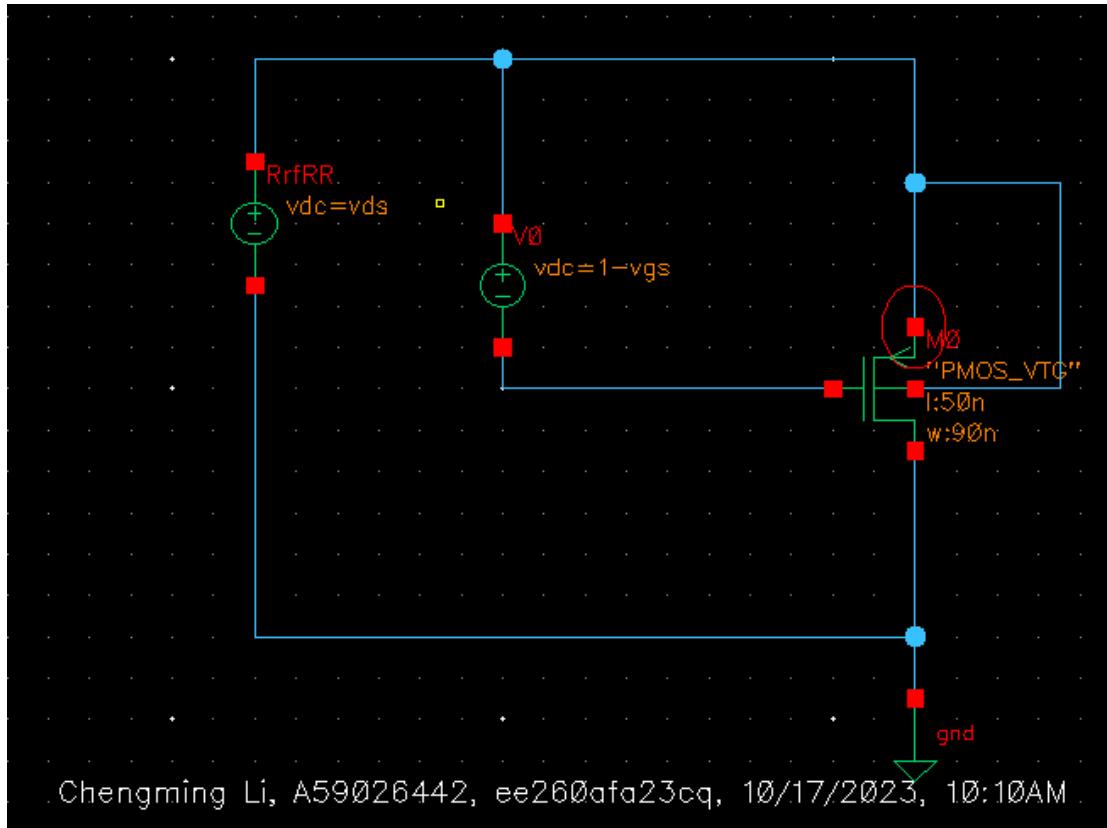


a.

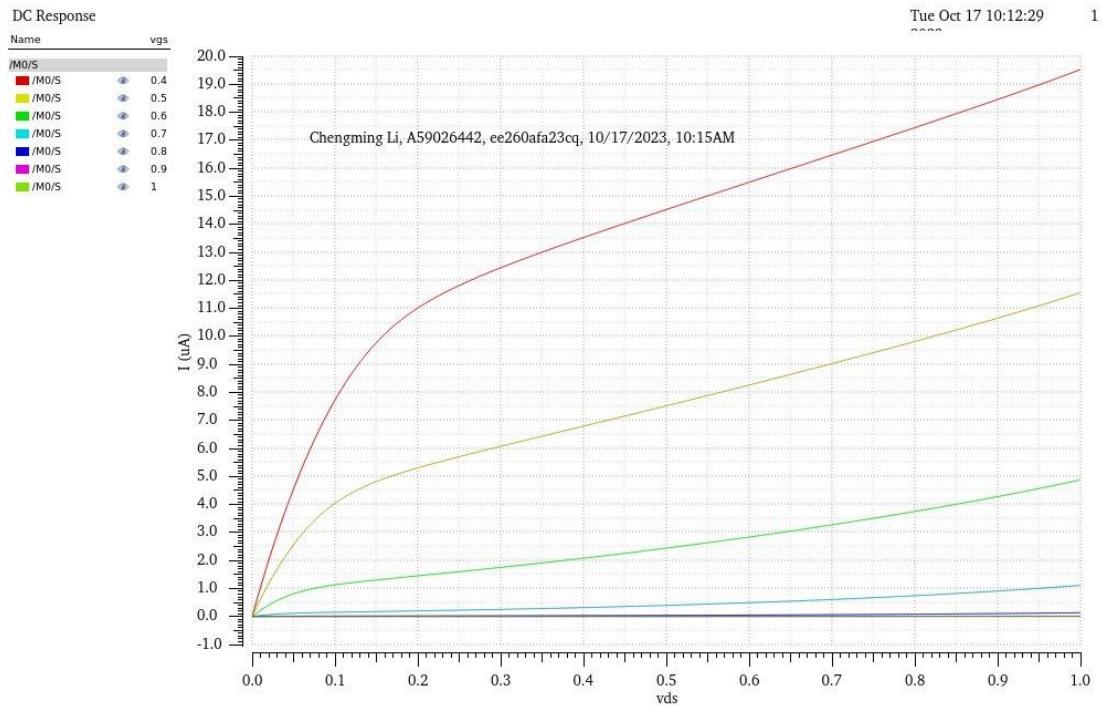


16

- b. Maximum IDS: $81.676\mu\text{A}$ when $\text{vin} = 1\text{V}$,
 Maximum current density = $81.676\mu/90\text{nm} = 907.51\text{A/m}$

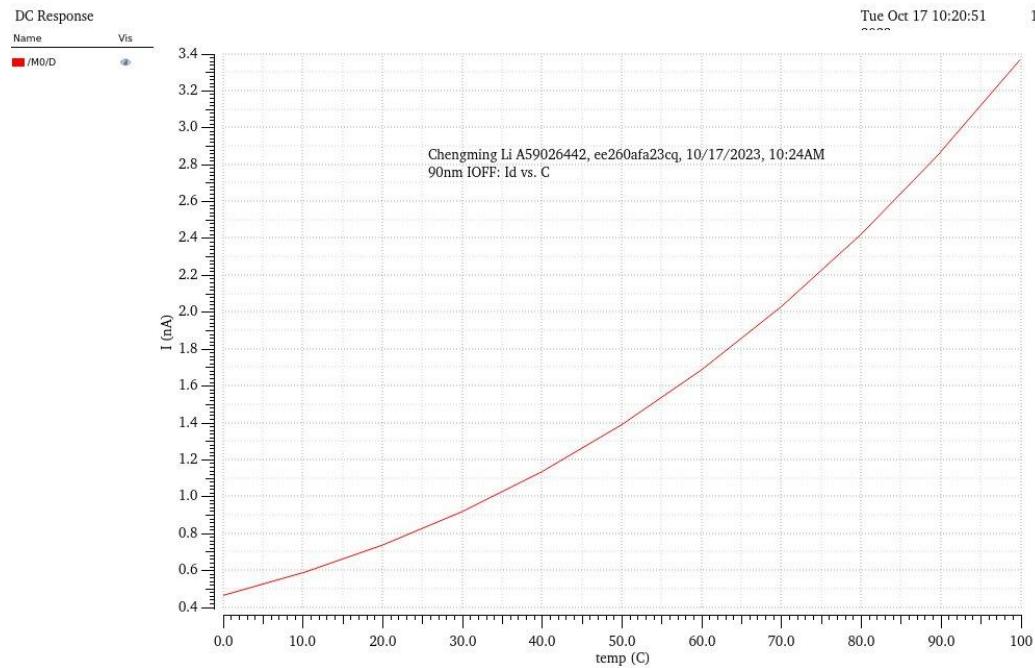


16

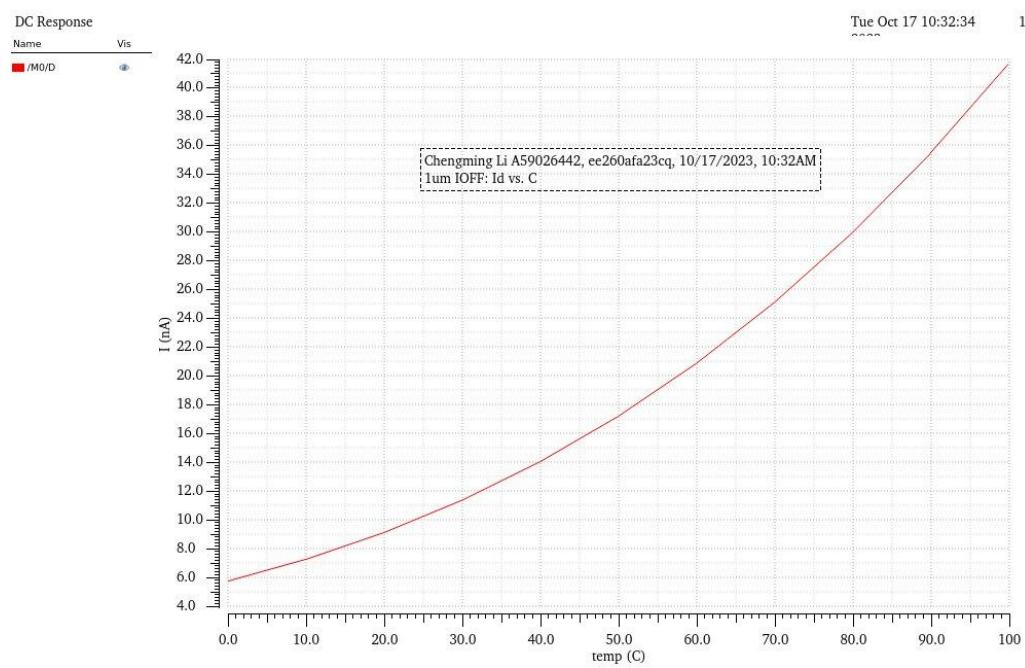


{ d

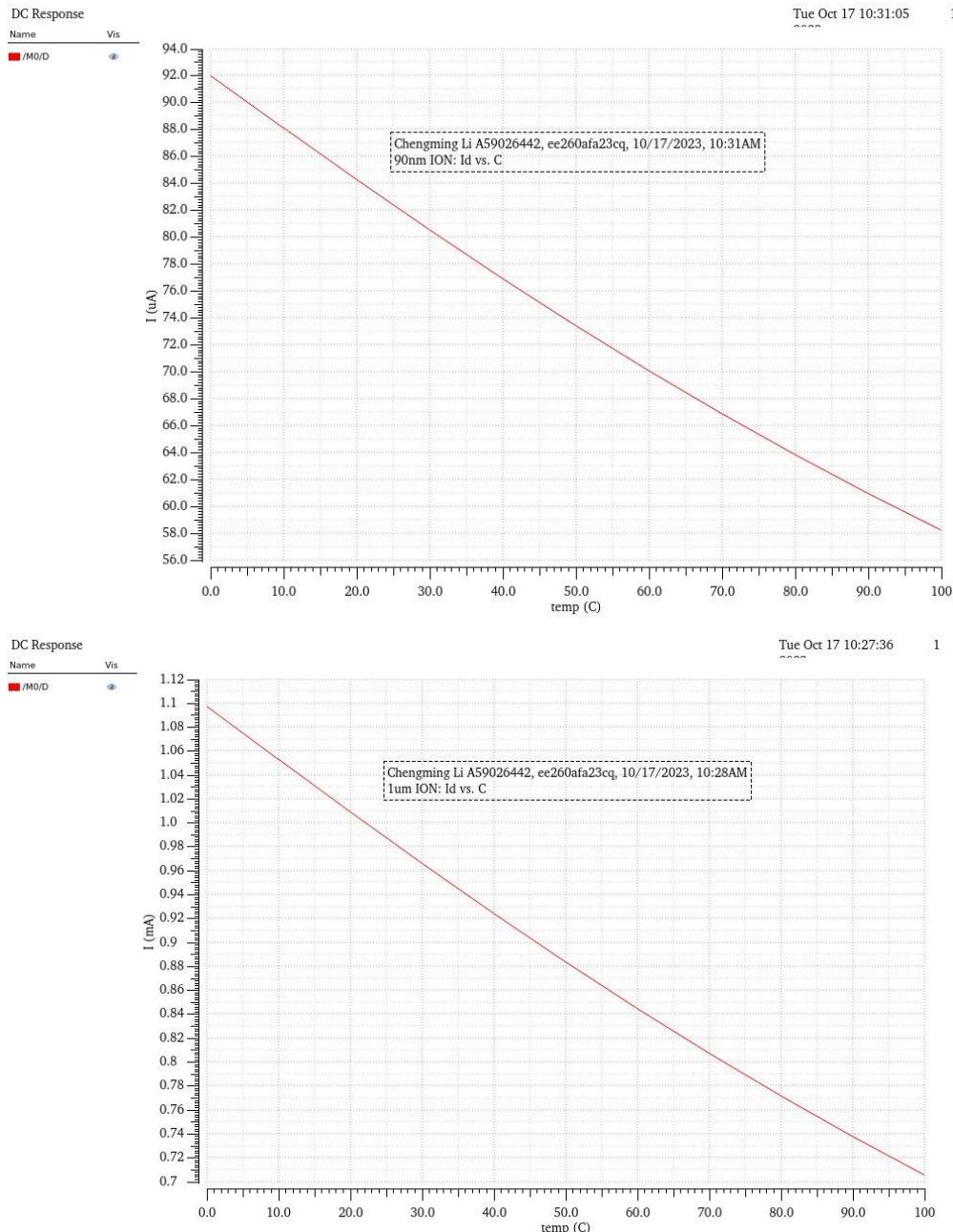
- d. Maximum IDS: 19.513uA when vgs = 0.4V, vin = 0.6V
Maximum current density = 19.513u/90nm = 216.81A/m



e.

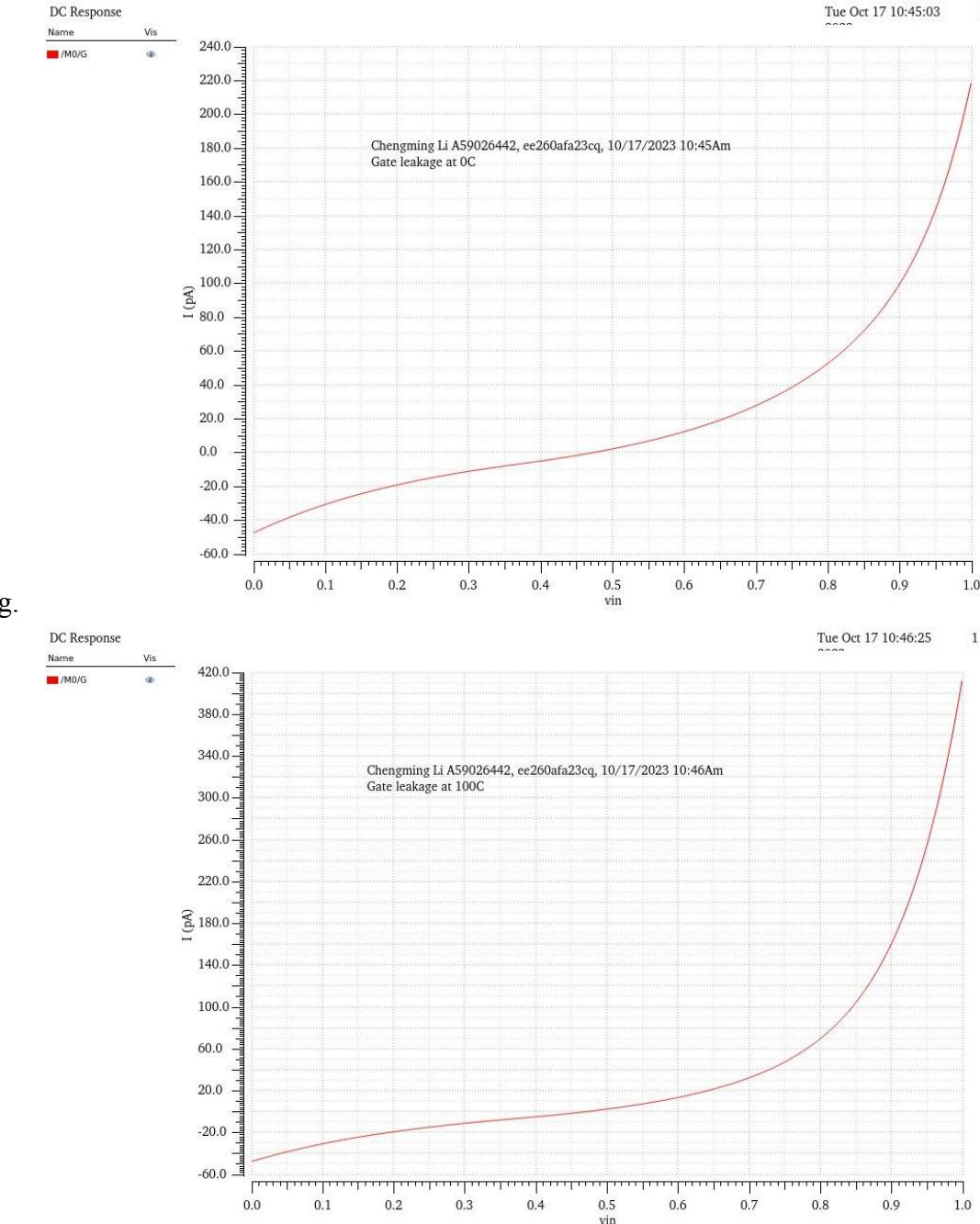


[e



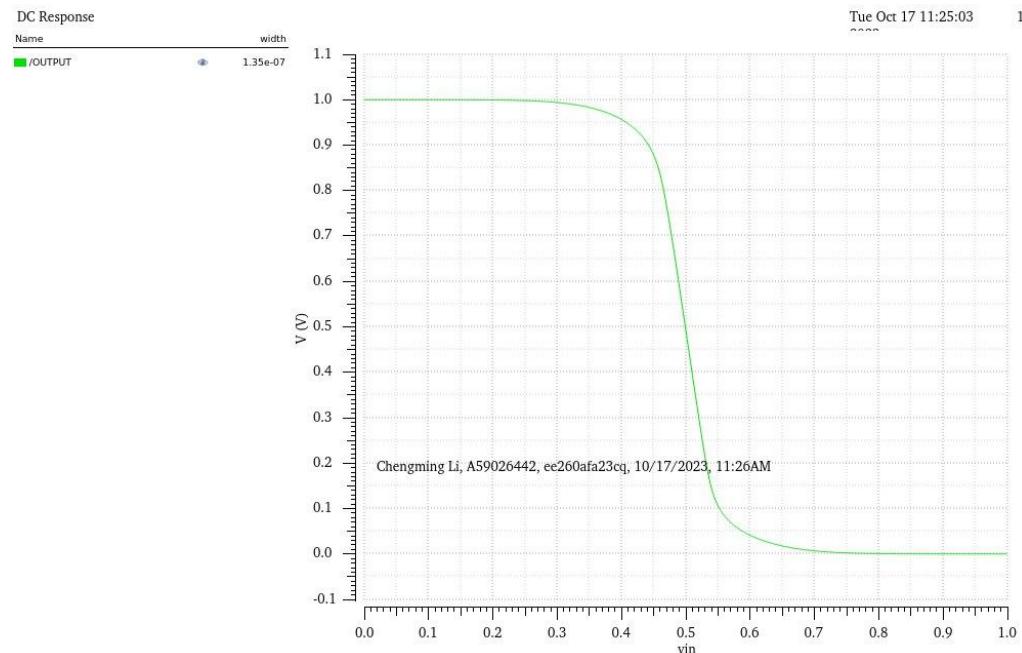
f. Ratio = PMOS(100C,IOFF)/NMOS(100C,IOFF) = 2.962n/3.36559n = 0.88

1 +



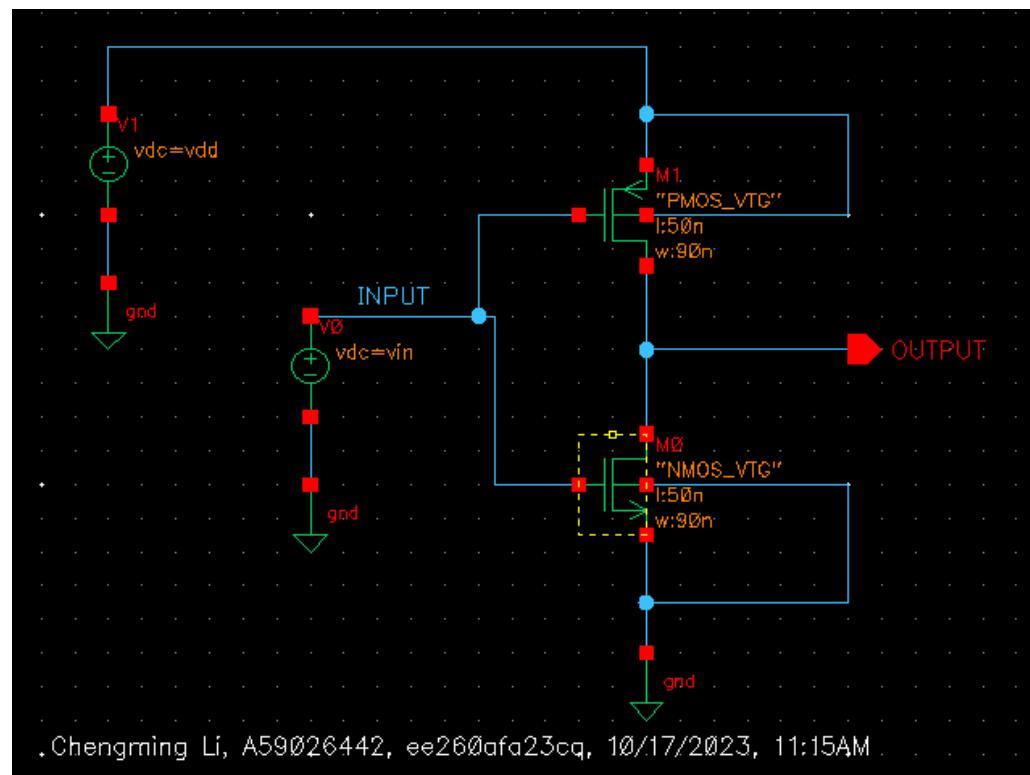
Fraction: 100C,VGS =1: Gate leakage/Drain leakage = $411.497\text{p}/58.255\text{u} = 7.06\text{u}$
 0C,VGS =1: Gate leakage/Drain leakage = $218.1553\text{p}/92.045\text{u} = 2.37\text{u}$

2. Problem 2

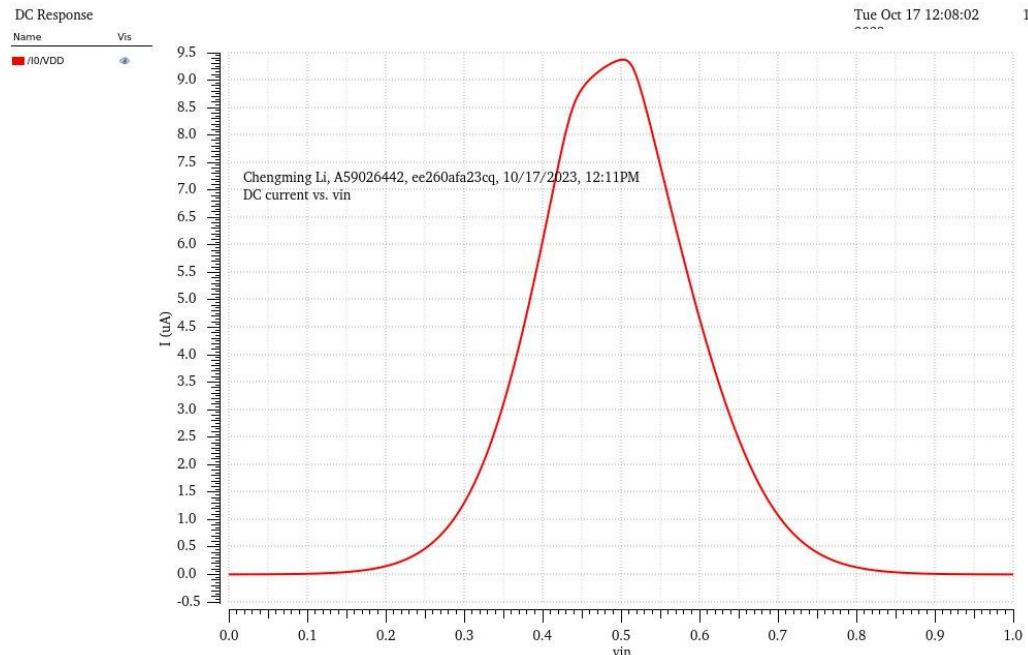


2a

a.



PMOS_Width = 135nm



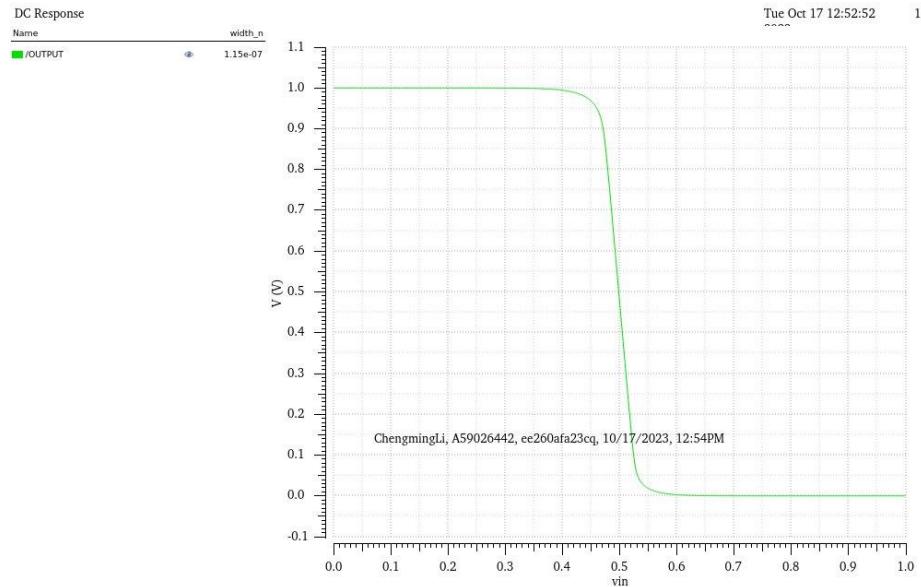
2b

b.

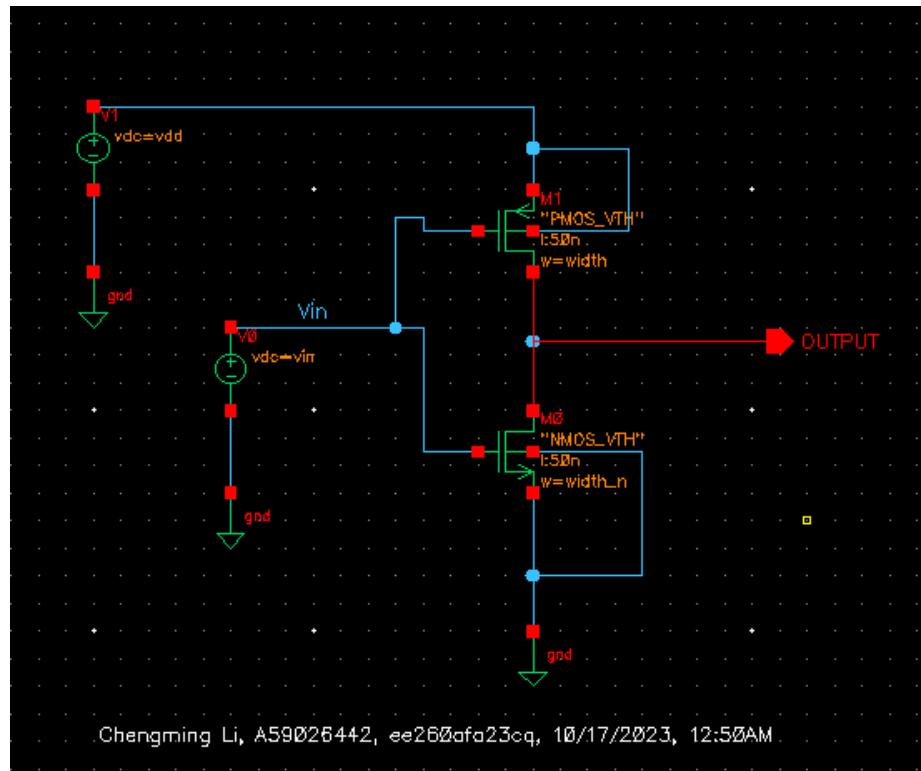
$$\text{Slope} = (dI/dV_{GS})^{-1} = nV_{T}\ln 10$$

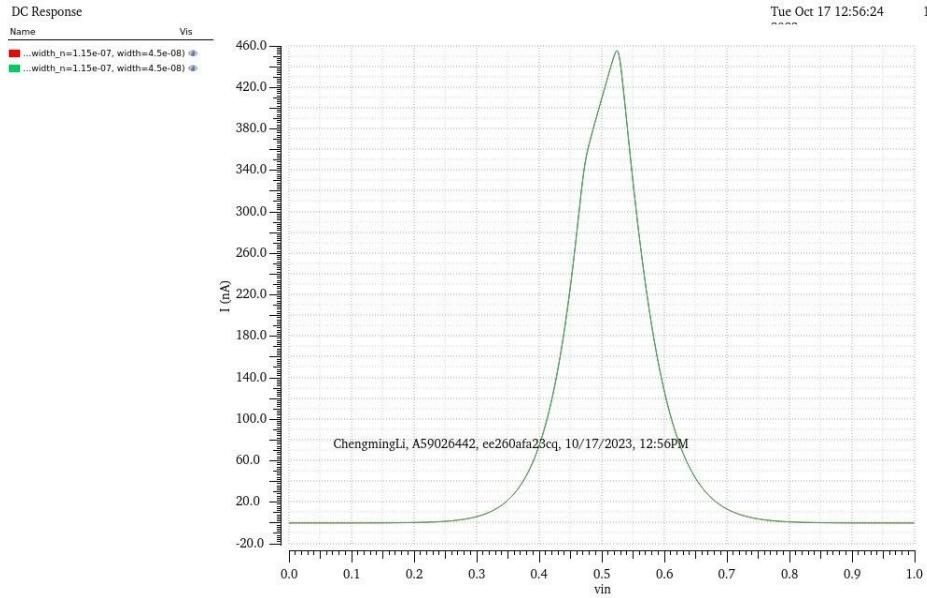
$$\text{PMOS Slope} = 0.106\text{V/decade}, n = 0.115$$

$$\text{NMOS Slope} = 0.11\text{V/decade}, n = 0.119$$



C.





Width: NMOS = 115nm, PMOS = 45nm

PMOS Slope: 0.091V/decade, n = 0.087

NMOS Slope: 0.0986V/decade, n = 0.095

- d. From part a, the width ratio of PMOS/NMOS = $135n/90n = 1.5$
 From part c, the width ratio of PMOS/NMOS = $45n/115n = 0.4$
 Then, in order to gain Low V_{th}, the width of PMOS would be wider/greater, and the width of NMOS would be narrower. And the width ratio of PMOS/NMOS will be greater than VTG
 The Subthreshold slope (and n) for both PMOS and NMOS would be greater than the slope using VTG transistor

2d

3. Problem3

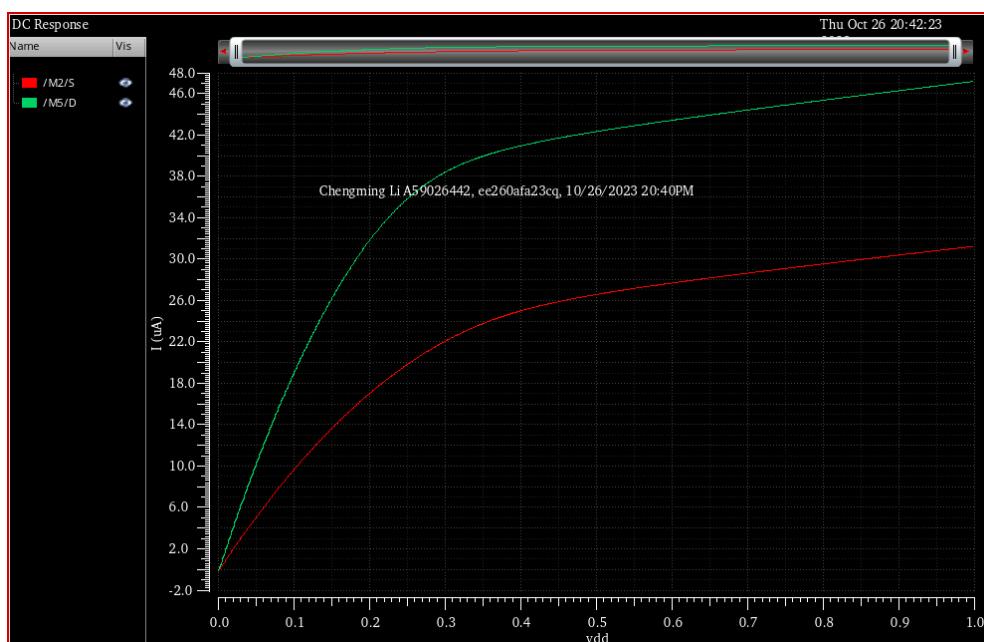
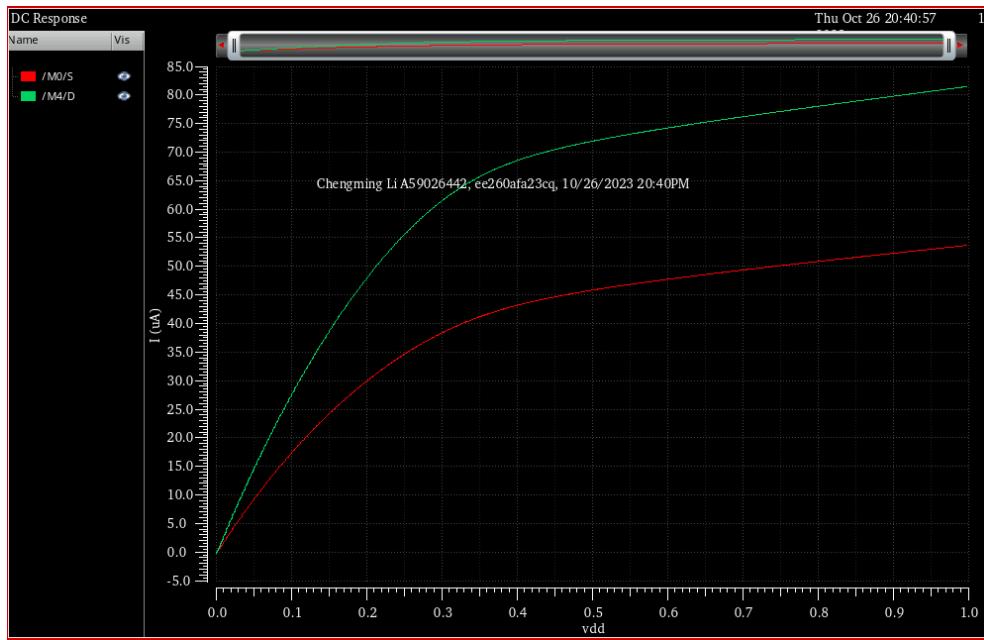
a.

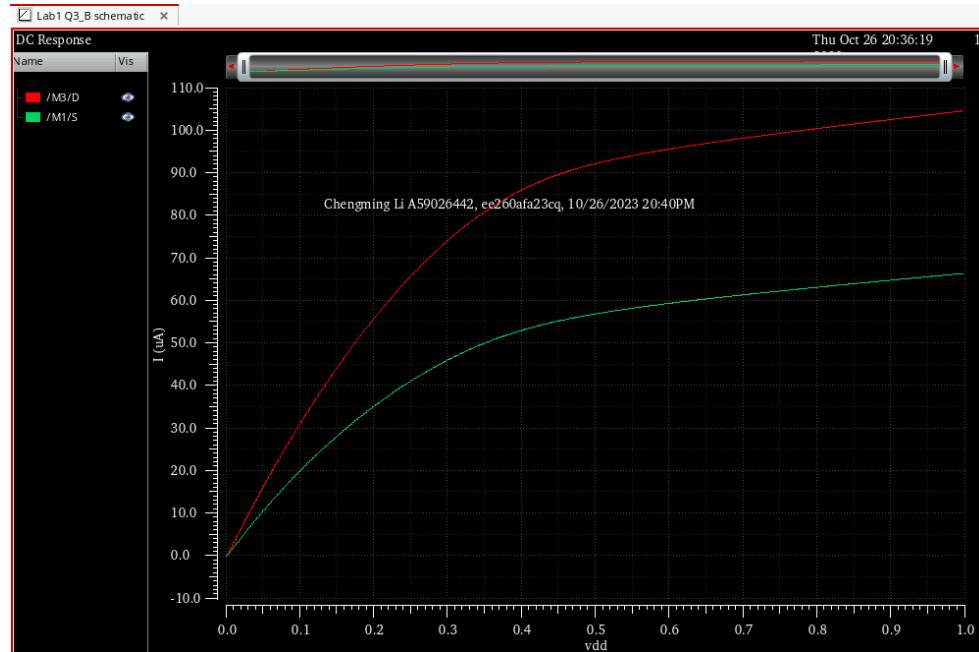
3a

	Gate Capacitance C_g (nF/m)	Capacitance C_{para} (nF/m)	C_{sb} (nF/m)	C_{db} (nF/m)
NMOS_VTL	1.73	3.78	2.02	1.76
NMOS_VTG	1.73	3.78	2.02	1.76
NMOS_VTH	1.28	3.78	2.02	1.76
PMOS_VTL	1.59	4.96	2.02	2.95
PMOS_VTG	1.59	4.96	2.02	2.95
PMOS_VTH	1.3	4.96	2.02	2.95

3b

b.





Figures(Ids vs. Vds for both NMOS and PMOS) in sequence are for VTL, VTG, and VTH. Values got from minimum isze of NMOS and PMOS(90n/50n)

For VTL:

$$\text{NMOS: } R = 1/104.76\mu = 9545.63 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 106 \text{ ohm/nm}$$

$$\text{PMOS: } R = 1/66.549\mu = 15026 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 166.96 \text{ ohm}$$

For VTG:

$$\text{NMOS: } R = 1/81.624\mu = 12251.3 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 136 \text{ ohm/nm}$$

$$\text{PMOS: } R = 1/53.877\mu = 18560.8 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 206 \text{ ohm}$$

For VTH:

$$\text{NMOS: } R = 1/47.274\mu = 21153 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 235 \text{ ohm/nm}$$

$$\text{PMOS: } R = 1/31.327\mu = 31921.34 \text{ ohm,}$$

$$R_{\text{unitWidth}} = 354.68 \text{ ohm}$$

3c

c.

Delay Calculation:

All values are based on W/L = 90n/50n

VTL:

$$C = 90n * (3.78n/m + 4.96n/m) + 4 * 90n(1.73nF/m + 1.59nF/m) = 1.98f$$

PMOS Delay: $RC = 15026 * 1.98f = 29.6ps$

NMOS Delay: $RC = 9545.63 * 1.98f = 18.9s$

VTG:

$$C = 90n * (3.78n/m + 4.96n/m) + 4 * 90n(1.73nF/m + 1.59nF/m) = 1.98f$$

PMOS Delay: $RC = 18560 * 1.98f = 36.8p$

NMOS Delay: $RC = 12251.3 * 1.98f = 24.2ps$

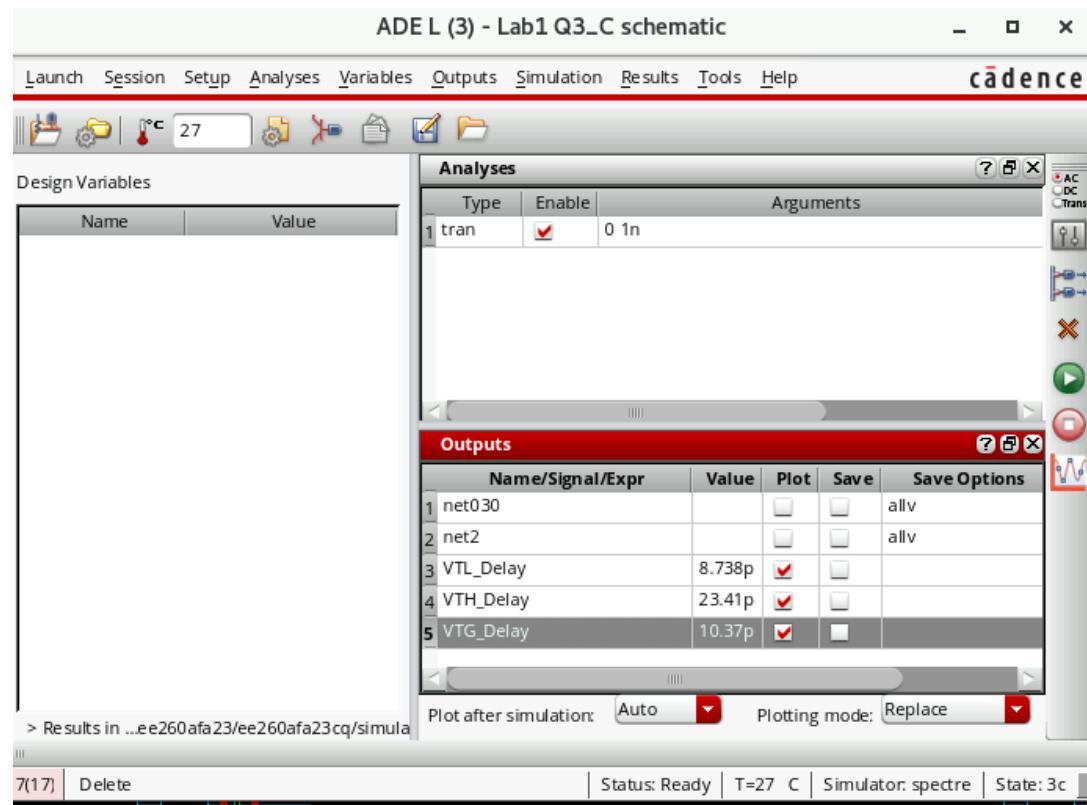
VTH:

$$C = 90n * (3.78n/m + 4.96n/m) + 4 * 90n(1.28nF/m + 1.3nF/m) = 1.715f$$

PMOS Delay: $RC = 31921.34 * 1.715f = 54.7ps$

NMOS Delay: $RC = 21153 * 1.715f = 36.2ps$

Delay Simulation:



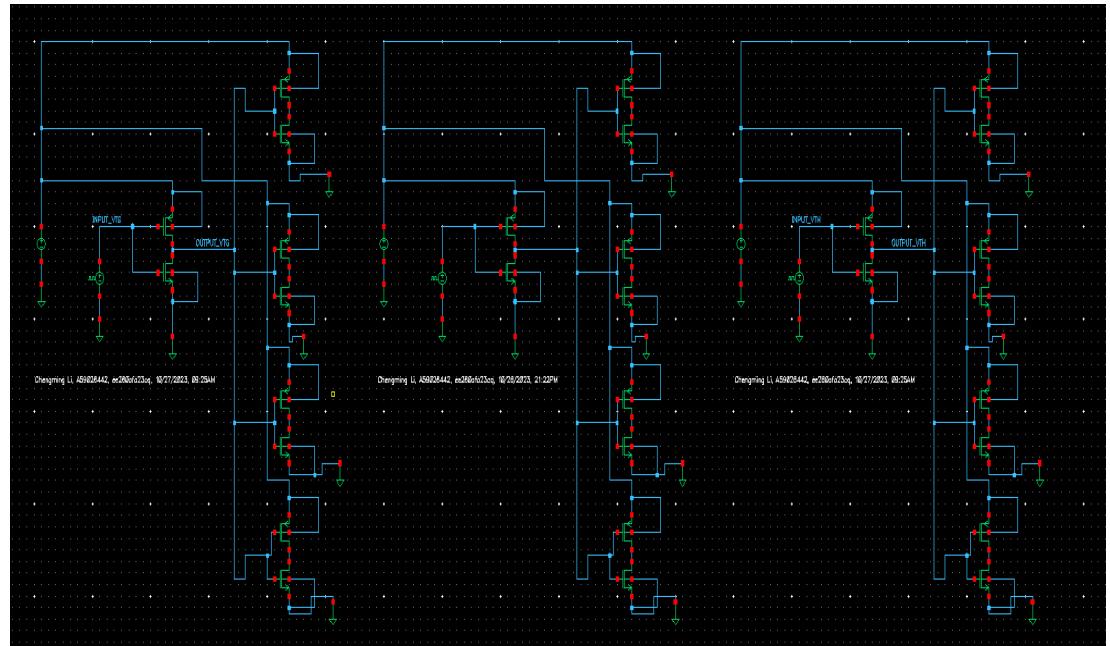
Size of PMOS and NMOS, got it from Q2, are used in the simulation

VTL: 8.738ps

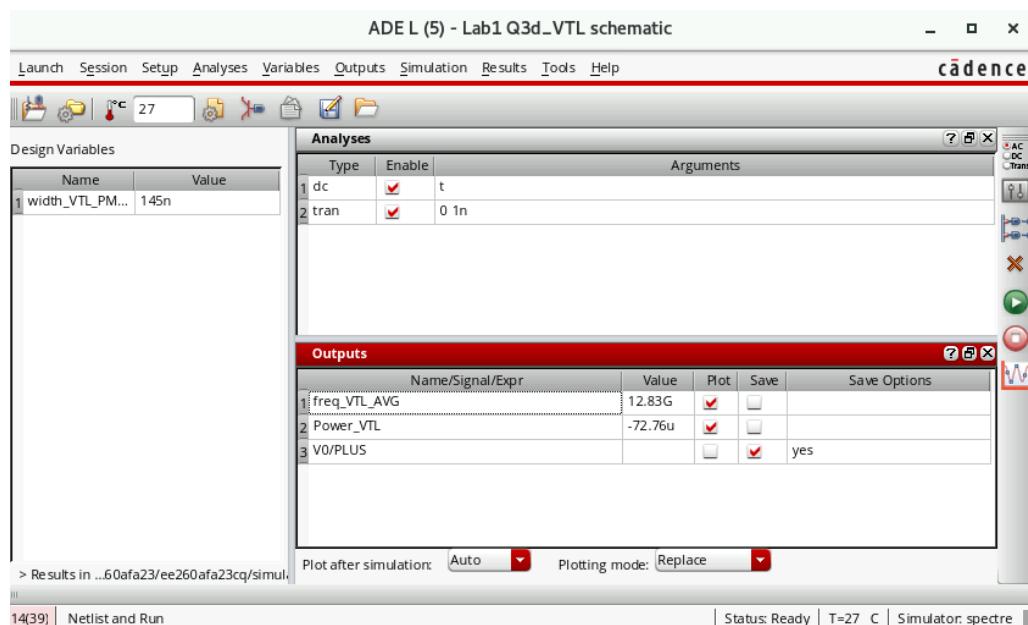
VTG: 10.37ps

VTH: 23.41ps

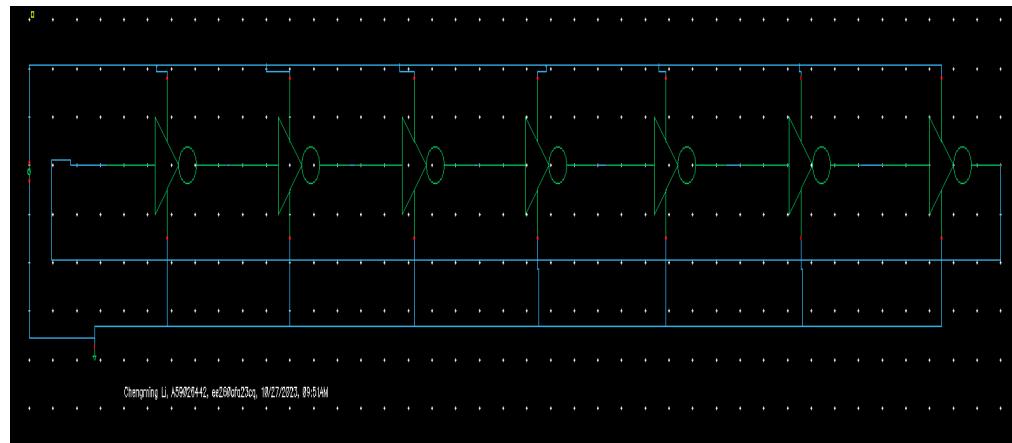
3c schematic



d.



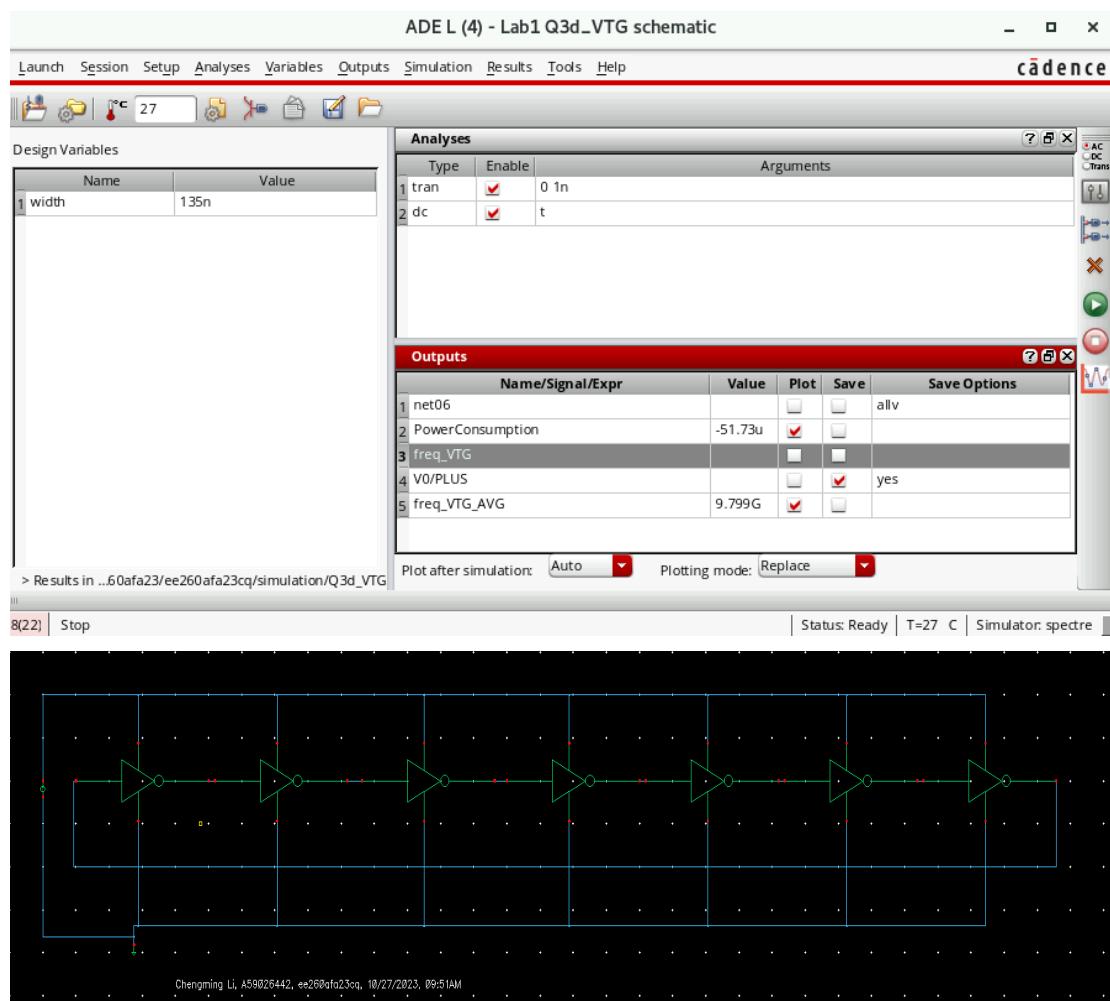
3d



VTL Simulation and Schematic:

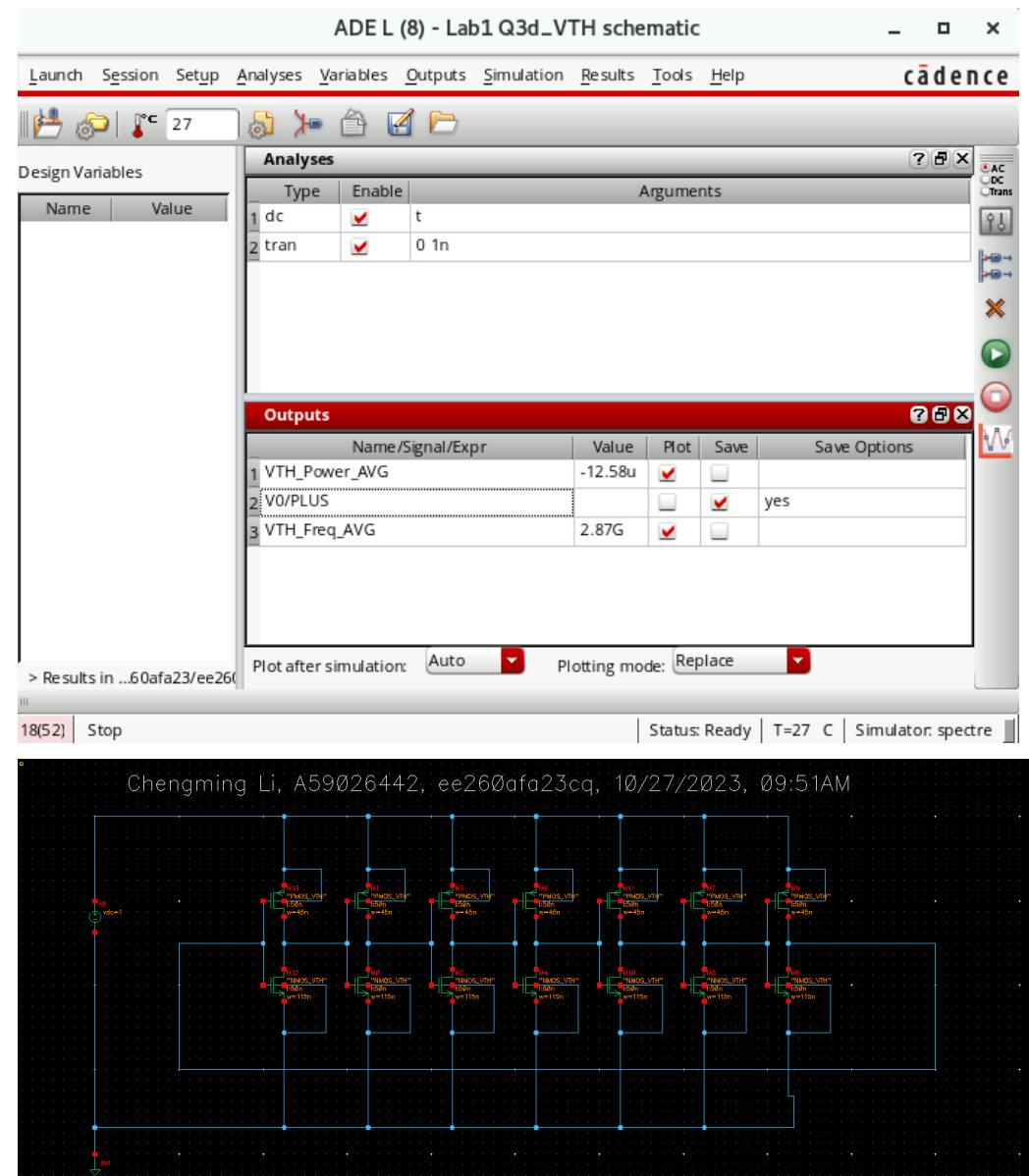
Freq: 12.83G

Power: 72.6uW



VTG Simulation and Schematic:

Freq: 9.799G
Power: 51.73uW



VTH Simulation and Schematic:

Freq: 2.87G
Power: 12.58uW

Hand Calculation

3d

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_{delay}}$$

$$P = \frac{1}{2} C V^2 f$$

V_TL :

$$\text{PMOS : } t_{delay} = R_L = 15026 \cdot 1.08 f$$

$$= 16.22 \text{ ps}$$

$$\text{NMOS } t_{delay} = 9545.63 \cdot 1.08 f$$

$$= 10.3 \text{ ps}$$

$$f_{osc} = \frac{1}{2 \cdot 7 \cdot \left(\frac{16.22 \text{ ps} + 10.3 \text{ ps}}{2} \right)}$$

$$= 5.386 \text{ GHz}$$

$$C \cdot q_{on} \cdot (3.78n + 4.96n \\ + 1.73n + 1.59n)$$

$$= 1.08 f F$$

$$P = 2.9 \mu W$$

V_TG :

$$\text{PMOS : } t_{delay} = R_L = 18560 \cdot 1.08 f$$

$$= 20 \text{ ps}$$

$$\text{NMOS } t_{delay} = 12251.3 \cdot 1.08 f$$

$$= 13.2 \text{ ps}$$

$$C \cdot q_{on} \cdot (3.78n + 4.96n \\ + 1.73n + 1.59n)$$

$$= 1.08 f F$$

$$P = 2.32 \mu W$$

V_TH :

$$\text{PMOS : } t_{delay} = R_L = 3194 \cdot 1.02 f$$

$$= 32.5 \text{ ps}$$

$$\text{NMOS } t_{delay} = 21153 \cdot 1.02 f$$

$$= 21.6 \text{ ps}$$

$$C \cdot q_{on} \cdot (3.78n + 4.96n \\ + 1.28n + 1.3n)$$

$$= 1.02 f F$$

$$f_{osc} = \frac{1}{2 \cdot 7 \cdot \left(\frac{32.5 \text{ ps} + 21.6 \text{ ps}}{2} \right)}$$

$$= 3.13 \text{ GHz}$$

$$P = 1.6 \mu W$$

3e

e.

Power Consumption: VTH > VTG > VTL

Frequency: VTL > VTG > VTH

Delay(FO4): VTH > VTG > VTL

f.

3f

Vdd	Freq(Hz)	Avg.delay(s)	Avg.power(W)	Power-delay product(Ws)	Energy-delay product(Js)
1	9.80E+09	7.26E-12	5.17E-05	3.75E-16	3.83E-26
0.8	7.27E+09	9.80E-12	2.42E-05	2.37E-16	3.26E-26
0.6	3.91E+09	1.85E-11	7.26E-06	1.34E-16	3.43E-26
0.4	6.26E+08	1.17E-10	5.09E-07	5.94E-17	9.49E-26
0.2	1.25E+07	5.77E-09	2.53E-09	1.46E-17	1.16E-24
0	1.48E+06	4.63E-08	1.38E-10	6.40E-18	4.33E-24

Minimum VDD achievable will be < 0.1 V if we give enough time to run.

Because during the simulation, I kept increasing the testbench pulse width to get the frequency. So the Ring oscillator would work as long as given enough time.

Q4

This problem involves some transistor hand analysis. Assume $V_{DD} = 1V$, $W \cdot L_{min} = 90\text{nm}$, $L_{min} = 50\text{nm}$, $T=25^\circ\text{C}$. Use the following parameters for all calculations, representative of a 45nm CMOS technology:

	t_{ox} (nm)	V_{t0} (V)	μ (cm ² /Vs)	v_{SAT} (cm/s)	γ ($\sqrt{\text{V}}$)	n
NMOS	1.14	0.41	450	12.3×10^6	0.4	1.46
PMOS	1.26	-0.38	-200	6.2×10^6	0.4	1.52

- a) What is the on-current of a minimum sized NMOS with $V_{GS} = V_{DS} = 1.0\text{V}$? In this problem, assume the long-channel MOS transistor model, but ignore channel-length modulation (CLM) and DIBL.

a) $V_{GS} = V_{DS} = 1 \rightarrow \text{Saturation}$

$$I_{on} = \frac{1}{2} \beta (V_{GS} - V_t)^2 \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\beta = \mu C_{ox} \frac{W}{L} = 450 \cdot \frac{3.9 \times 8.85 \cdot 10^{-14} \text{ F}}{1.14 \cdot 10^{-7} \text{ cm}} \cdot \frac{90}{50}$$

$$= 2.45 \cdot 10^{-3} \frac{\text{A}}{\text{V}^2}$$

$$I_{on} = \frac{1}{2} \cdot 2.45 \cdot 10^{-3} \cdot (1 - 0.41)^2 = 4.26 \cdot 10^{-4} \text{ A}$$

b) Now, let's use this minimum-sized NMOS device together with a PMOS device with minimum length to design an inverter. What value should you size the PMOS width to be, given that you would like an inverter threshold of $V_{DD}/2$? Again, assume a long channel model, ignoring CLM and DIBL. What is the $(W/L)_p/(W/L)_n$ ratio between the PMOS and NMOS devices? Are the equations you used sufficient to get an exact inverter threshold of $V_{DD}/2$?

$$\text{In order to get } V_{th} = \frac{V_{DD}}{2} , \frac{\beta_p}{\beta_n} = 1$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

$$\beta_p = -200 \cdot \frac{\epsilon_{ox}}{1.26 \cdot 10^{-7}} \cdot \frac{W}{50n}$$

$$\beta_n = 450 \cdot \frac{\epsilon_{ox}}{1.14 \cdot 10^{-7}} \cdot \frac{90n}{50n}$$

$$\beta_p = \beta_n \Rightarrow W_p \approx 223.8 \text{ nm}$$

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\frac{223.8n}{50n}}{\frac{90n}{50n}} = \frac{373}{150} \approx 2.486$$

No, We can't get the exact inverter threshold of $\frac{V_{DD}}{2}$

Redefining $r = W_p v_{sat-p} / W_n v_{sat-n}$, we can again find the inverter threshold

$$V_{inv} = \frac{V_{DD} + V_{tp} + V_{tn} \frac{1}{r}}{1 + \frac{1}{r}}$$

if $V_{tn} = -V_{tp}$ and $r = 1$, $V_{inv} = V_{DD}/2$ as expected.

In our case

$$V_{tn} \neq -V_{tp}$$

$$\gamma = \frac{W_p v_{sat-p}}{W_n v_{sat-n}}$$

$$= 1.25 \neq 1$$

c) Given an input of $V_{in}=1V$, what is the static power consumption of this inverter? Keep on ignoring CLM and DIBL.

$$P_{stat} = I_{stat} \cdot V_{DD}$$

$V_{in}=1V$, NMOS is ON

$$I_{d,n} = I_{on} = \frac{1}{2} \cdot 2.45 \cdot 10^{-3} \cdot (1 - 0.41)^2 = 4.26 \cdot 10^{-4} A$$

\uparrow
From part a

$$P_{stat} = 4.26 \cdot 10^{-4} \cdot 1 = 4.26 \cdot 10^{-4} W$$

d) Is the assumption of using a long channel model in the previous parts a good one? Explain why. In your answer, compute V_{DSAT} .

No, because long channel model neglect the lateral E-field effects, and it assumes OA through an off transistor. So that it overestimates the current through transistor.

$$V_{dsat} = \frac{V_{GT}V_c}{V_{GT} + V_c}$$

$$NMOS \Rightarrow V_{GT} = V_{GS} - V_{t,n} = 1 - 0.41 \\ = 0.59$$

$$\mu_{eff,n} = \frac{540 \frac{cm^2}{V \cdot s}}{1 + \left(\frac{V_{gs} + V_t}{0.54 \frac{V}{nm} t_{ox}} \right)^{1.85}}$$

$$\mu_{eff,p} = \frac{185 \frac{cm^2}{V \cdot s}}{1 + \left(\frac{|V_{gs} + 1.5V_t|}{0.338 \frac{V}{nm} t_{ox}} \right)^{1.85}}$$

$$\mu_{eff,n} = 95.87 \frac{cm^2}{V}$$

$$V_{c,n} = 1.28 V$$

$$V_C = E_C \cdot L$$

$$E_C = \frac{2V_{sat}}{\mu_{eff}}$$

$$V_{dsat,n} = \frac{0.59 \cdot 1.28}{0.59 + 1.28} \\ = 0.4 V$$

e) Now, assume the short-channel model (with velocity saturation). Repeat part a), continuing to ignore CML and DIBL. If your current changed, explain why it changed in the direction it did.

$$I_{ds} = \begin{cases} \frac{\mu_{eff}}{V_c} C_{ox} \frac{W}{L} (V_{GT} - V_{ds}/2) V_{ds} & V_{ds} < V_{dsat} \\ 1 + \frac{V_{ds}}{V_c} \\ C_{ox} W (V_{GT} - V_{dsat}) v_{sat} & V_{ds} > V_{dsat} \end{cases} \quad \begin{matrix} \text{Linear} \\ \text{Saturation} \end{matrix}$$

$$I_{ds} = \frac{3.9 \cdot 8.85 \cdot 10^{14}}{1.14 \cdot 10^7} \cdot 90 \cdot 10^{-7} \cdot (0.59 - 0.4) \cdot 12.3 \cdot 10^6$$

$$= 63.68 \mu A$$

The current decrease due to velocity saturation and mobility degradation

At High V_{os} , the carriers move slower and collide more often, which reduce the amount of current through transistor.

The saturation current increase less than quadratically increasing with V_{gs}

f) Repeat part b) using the velocity saturation equations (and ignore, well, you get it now...). Is the velocity saturation regime the correct assumption here?

$$I_{dsat} = WC_{ox} v_{sat} \frac{V_{GT}^2}{V_{GT} + V_c} \quad V_{ds} > V_{dsat}$$

$$\begin{aligned} V_{GT} &= V_{gs} - V_{t,p} \\ &= 1 - 1.038 \\ &= 0.62 \end{aligned}$$

$$n_{eff,p} = \frac{185}{1 + \frac{|V_{gs} + 1.5V_t|}{0.338 \cdot t_{ox}}} = 92.05 \text{ cm}^2/\text{V}$$

$$V_c, p = \frac{2 \cdot v_{sat}}{n_{eff,p}} = \frac{2 \cdot 6.2 \cdot 10^6}{92.05} \cdot 50n = 0.67 \text{ V}$$

$$V_{osat,p} = \frac{0.62 \cdot 0.67}{0.62 + 0.67} = 0.322 \text{ V}$$

$$I_{d,n} = I_{d,p} = C_{ox} W_p (V_{GT} - V_{osat}) v_{sat}$$

$$63.68 \mu A = \frac{3.9 \cdot 8.85 \cdot 10^{-14}}{1.26 \cdot 10^7} \cdot W_p (0.62 - 0.322) \cdot 6.2 \cdot 10^6$$

$$W_p = 12.6 \mu \text{m}$$

$$\frac{\left(\frac{w}{l}\right)_p}{\left(\frac{w}{l}\right)_n} = \frac{12.6 \mu}{10 \mu} = 140$$

Velocity saturation regime is not the correct assumption here

$$\text{As } r = \frac{W_p \cdot V_{satp}}{W_n \cdot V_{satn}} \approx 70.6 \neq 1$$

$$V_{in} \neq \frac{1}{2} V_{DD}$$

g)

g) What is the static power consumption of the inverter now? If it is different than your answer in part c), explain why.

$$P_{stat} = I_{stat} \cdot V_{DD} , V_{in} = 1 \text{ NMOS is ON}$$
$$= 63.68 \mu A \cdot 1 = 63.68 W$$

Since I_{stat} changed due to the effects of velocity saturation and mobility Degradation

We get less I_{stat} through nmos when V_{DS} is high at 1V.

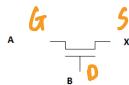
The lateral E-field is strong and affects the velocity of carrier.

In part a. The effects of lateral E-field is assumed to be relatively small. Thus, we neglect the effects of velocity saturation and mobility Degradation

Q5

Suppose $B=1.4V$ and $V_t=0.4V$. Determine X for the following values of A . (Neglect Body Effect)

- a) $A=0V$
- b) $A=0.6V$
- c) $A=1.1V$
- d) $A=1.4V$



Assume $X=0$, $V_{GS} > V_t$, transistor is ON

If X rises to $V_{DD}-V_t$ $V_{GS}=V_t$, transistor cut off

Therefore NMOS would never pull source above

$$V_{DD}-V_t = 1V$$

a) $X = A = \boxed{0V}$

b) $A = 0.6V \quad V_{DD}-V_t = 1V$

$$X = A = \boxed{0.6V}$$

c) $A = 1.1V > V_{DD}-V_t = 1$

$$X = V_{DD}-V_t = \boxed{1V}$$

d) $A = 1.4V > V_{DD}-V_t = 1$

$$X = V_{DD}-V_t = \boxed{1V}$$