
Chengming(Steven) Li

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Summary

Portfolio: <https://stevenlcm16.wixsite.com/chengmingli-steven>

GitHub: <https://github.com/stevenli518>

Detail-oriented team player seeking an internship starting from 03/2025. Or a full-time role, starting from 06-07/2025, in Electrical engineering-related positions to apply and expand technical skills

- **Fast Learner**
Managed to use the internet and online references to study Cadence Virtuoso in less than 2 weeks.
- **Hardware Skills**
Component Selection, PCB design, FPGA, Oscilloscope, Function Generator, Digital Multimeter, Spectrum Analyzer, Surface Mount Soldering
- **Programming Languages**
Python, C/C++, C#, Verilog/System Verilog, MATLAB, Tcl, HTML&CSS, SQL
- **Software Skills**
Altium, LTspice, Cadence Virtuoso, Allegro, ADS, Quartus, ModelSim, Simplicity Studio, VSCode, Visual Studio, MS Office, GitHub, Confluence, Lattice, Slack

Relevant Coursework: Communication Circuit Design, Power Amplifier Design, Analog IC Design, PMIC, VLSI, Universal Verification Methodology (UVM), Modern Communication Networks, Embedded System, Computer Architecture, RTOS,

Work/Research Experience

Renesas Electronics America Inc

San Jose, CA

Hardware Engineer Intern

June 2024 - Sep 2024

- Analyzed induction cooktop circuits, focusing on component selection, datasheets, power consumption, and circuit protection
- Simulated induction cooktop(IH) in LTspice, Flux, and Altium and tested LC tank, gate driver, and OVP using Oscilloscope
- Compared 8-layer Allegro Gerber files with Altium designs and summarized differences in electrical and non-electrical layers

Eridan Communications

Sunnyvale, CA

RF Test Engineer Intern

June 2023 - Aug 2023

- Built a MATLAB and C# DLL-to-Python conversion framework on GitHub for 7+ instruments and PCB testing
- Developed and executed batch scripts to semi-auto the installation process (under 5 minutes) of VScode, Python, and Rclone

University of Colorado at Boulder (Dr. Taylor Barton's RF Power and Analog Lab)

Boulder, CO

Research Assistant

Aug 2022 - May 2023

- Implemented multi-digital filters using Vivado FPGA (Red Pitaya) to reduce the distortion in the Class-AB Power Amplifier
- Automated the test with RF Generator, Spectrum Analyzer, and Power Supply to collect the IMD3, Pout, and Current data
- Processed the IMD3 data using Python and characterized the optimal transfer function using the network analyzer

Project Experience (for more info and pics: <https://stevenlcm16.wixsite.com/chengmingli-steven/projects>)

3-level Buck (1.8V – 0.8V) Converter PMIC Design in Cadence Virtuoso

San Diego, CA

Member of Group 3

Sep 2024 - Dec 2024

- Modeled and optimized in MATLAB the size of transistors, inductor, and capacitor to achieve low power loss and small area
- Designed the schematic and simulation testbench of non-overlapping and deadtime generator, level shifter, and error amplifier
- Performed voltage and temperature variations simulation and achieved 87% nominal efficiency and $0.24 W * mm^2$

2-Stage Class J HBT Power Amplifier Design in ADS

San Diego, CA

Individual

Oct 2024 - Nov 2024

- Developed the schematic and matching network of 2-stage ClassJ PA in ADS, using the loadpull technique to favor efficiency
- Tuned the output matching to achieve -0.5 dB matching loss and low input return loss using Smith-chart and S-parameter
- Achieved 32dB flat gain, 2.609° phase distortion at $P_{L,1} = 35.55 dBm$ at $f_c = 2.535G Hz$ and wideband interstage matching

9-bit 65nm TSMC process SAR ADC Tape out, PCB Design and Test Automation

San Diego, CA

Member of Group 2

April 2024 - Dec 2024

- Laid out comparator, non-overlapping clock generator, and digital logic and optimized CDAC ratios using Cadence Virtuoso
- Used Common centroid and Dummy device to minimize input offset (90 uV) and propagation delay(323.6 ps) of comparator
- Designed the schematic and layout of the PCB board for testing in Altium, considering the drive and debug configurability
- Built Keysight instrument control and data collecting code in Python and processed INL, DNL, SNR, and SFDR in MATLAB

Scalable Electrosurgical Unit for Controlling and Powering the Ligasure Dissection Device

Boulder, CO

Software Lead (Sponsor: Medtronic)

Aug 2022 - May 2023

- Created ADC, PWM, SCI, and CLA modules in C on the TI TMS320F28004C board in response to firmware development
- Reduced the RMS values calculation from 25% to 1.7% errors by using the bitwise mask to optimize the instruction cycles

Education

University of California San Diego

San Diego, CA

Master of Science in Electrical and Computer Engineering Cumulative GPA: 3.67/4.00

Graduation Time: July 2025

University of Colorado at Boulder (BS in ECE) Cumulative GPA: 3.81/4.00

Boulder, CO