Chengming(Steven) Li

stevenlcm16@gmail.com | 650-304-9670

Summary **Portfolio:** https://stevenlcm16.wixsite.com/chengmingli-steven **GitHub:** https://github.com/stevenli518

Detail-oriented team player seeking a full-time role, starting from 04/2025, in Integrated Circuit-related positions to apply and expand technical skills

- **Hardware Skills**
  PCB Design (Altium), Component selection, Analog-Digital circuit design, Microcontroller programming, Communication Protocols (I2C, SPI, UART)
- **Programming Languages**
  Python, C/C++, C#, Verilog/System Verilog, MATLAB, Tcl, Shell scripting
- **Lab Equipment & Skills**
  Oscilloscope, Signal Generator, Digital Multi-meter, Logic Analyzer, Spectrum Analyzer, Temperature Chamber, Surface Mount Soldering, Command Expert
- **Software Skills**
  Altium, LTspice, Cadence Virtuoso, Allegro, ADS, Quartus, ModelSim, Simplicity Studio, VSCode, Visual Studio, MS Office, GitHub, Confluence, Lattice, Slack

Relevant Coursework: RFIC Design, High-Speed Wireline IC Design, Analog IC Design, Power Management IC

Work/Research Experience

Renesas Electronics America Inc San Jose, CA
Hardware Engineer Intern June 2024 - Sep 2024

- Analyzed induction cooktop circuits, focusing on component selection, datasheets, power consumption, and circuit protection
- Simulated induction cooktop(IH) in LTspice, Flux, and Altium and tested LC tank, gate driver, and OVP using Oscilloscope
- Compared 8-layer Allegro Gerber files with Altium designs and summarized differences in electrical and non-electrical layers

Eridan Communications Sunnyvale, CA
RF Test Engineer Intern June 2023 - Aug 2023

- Built a MATLAB and C# DLL-to-Python conversion framework on GitHub for 7+ instruments and PCB testing
- Developed and executed batch scripts to semi-auto the installation process (under 5 minutes) of VScode, Python, and Rclone

University of Colorado at Boulder (Dr. Taylor Barton's RF Power and Analog Lab) Boulder, CO
Research Assistant Aug 2022 - May 2023

- Implemented multi-digital filters using Vivado FPGA (Red Pitaya) to reduce the distortion in the Class-AB Power Amplifier
- Automated the test with RF Generator, Spectrum Analyzer, and Power Supply to collect the IMD3, Pout, and Current data
- Processed the IMD3 data using Python and characterized the optimal transfer function using the network analyzer

Project Experience (for more info and pics: https://stevenlcm16.wixsite.com/chengmingli-steven/projects)

9-bit 65nm TSMC process SAR ADC Tape out, PCB Design and Test Automation San Diego, CA
PCB Designer and Test Script Developer April 2024 - Dec 2024

- Laid out comparator, non-overlapping clock generator, and digital logic and optimized CDAC ratios using Cadence Virtuoso
- Used Common centroid and Dummy device to minimize input offset (90 uV) and propagation delay(323.6 ps) of comparator
- Designed the schematic and layout of the PCB board for testing in Altium, considering the drive and debug configurability
- Built Keysight instrument control and data collecting code in Python and processed INL, DNL, SNR, and SFDR in MATLAB

3-level Buck (1.8V – 0.8V) Converter PMIC Design in Cadence Virtuoso San Diego, CA
Mixed Signal Circuit Designer Sep 2024 - Dec 2024

- Modeled and optimized in MATLAB the size of transistors, inductor, and capacitor to achieve low power loss and small area
- Designed the schematic and simulation testbench of non-overlapping and deadtime generator, level shifter, and error amplifier
- Performed voltage and temperature variations simulation and achieved 87% nominal efficiency and 0.24 $W * mm^2$

2-Stage Class J HBT Power Amplifier Design in ADS San Diego, CA
RF PA Designer Oct 2024 - Nov 2024

- Developed the schematic and matching network of 2-stage ClassJ PA in ADS, using the loadpull technique to favor efficiency
- Tuned the output matching to achieve -0.5 dB matching loss and low input return loss using Smith-chart and S-parameter
- Achieved 32dB flat gain, 48.45% efficiency at PL = 35.55dbm and Fc = 2.535GHz using wideband interstage matching

180nm CMOS 2-Stage Amplifier Design in Cadence Virtuoso San Diego, CA
Analog IC Designer Nov 2023 - Dec 2023

- Designed the transistor size of PMOS Folded Cascode, CS, RC feedback, constant gm, and current mirror using gm-Id
- Achieved 66 dB gain, 62 MHz UGBW, 67° PM in AC, and 491 uW power consumption with wide input and output range

Education

University of California San Diego San Diego, CA
Master of Science in Electrical and Computer Engineering Cumulative GPA: 3.67/4.00 **Graduation Time:** July 2025

University of Colorado at Boulder Boulder, CO
Bachelor of Science in Electrical & Computer Engineering Cumulative GPA: 3.81/4.00 May 2023