

IOCreg.inc

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1  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
2  ;                                                                                      ;
3  ;                                IOCreg.inc                                          ;
4  ;                                IOC Register Constants                             ;
5  ;                                Include File                                       ;
6  ;                                                                                      ;
7  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
8
9  ; This file contains the constants for the IOC control registers for the TI
10 ; CC2652 microcontroller.
11 ;
12 ; References: CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual
13 ;             https://www.ti.com/lit/ug/swcu185g/swcu185g.pdf?ts=1761608306803
14 ;
15 ; Revision History:
16 ;   2/16/22  Glen George      initial revision
17 ;   11/05/23 Glen George      update style and comments
18 ;   10/28/25 Steven Lei       add references to CC2652 Reference manual
19
20
21 ; I/O (DIO) pins are configured through the IOCFGn registers in the MCU IOC
22 ; IOCFGn registers are memory mapped
23 ;   sec 13.3, pg 1070
24
25 ; Base address of the registers
26 ;   table 3-1, pg 319
27 IOC_BASE_ADDR      .equ      0x40081000      ;I/O Controller registers
28
29 ; IOCFGn register offsets in memory map
30 ;   sec 13.10.3, pg 1106
31
32 IOCFG0             .equ      0x0000          ;I/O configuration for DIO0
33 IOCFG1             .equ      0x0004          ;I/O configuration for DIO1
34 IOCFG2             .equ      0x0008          ;I/O configuration for DIO2
35 IOCFG3             .equ      0x000C          ;I/O configuration for DIO3
36 IOCFG4             .equ      0x0010          ;I/O configuration for DIO4
37 IOCFG5             .equ      0x0014          ;I/O configuration for DIO5
38 IOCFG6             .equ      0x0018          ;I/O configuration for DIO6
39 IOCFG7             .equ      0x001C          ;I/O configuration for DIO7
40 IOCFG8             .equ      0x0020          ;I/O configuration for DIO8
41 IOCFG9             .equ      0x0024          ;I/O configuration for DIO9
42 IOCFG10            .equ      0x0028          ;I/O configuration for DIO10
43 IOCFG11            .equ      0x002C          ;I/O configuration for DIO11
44 IOCFG12            .equ      0x0030          ;I/O configuration for DIO12
45 IOCFG13            .equ      0x0034          ;I/O configuration for DIO13
46 IOCFG14            .equ      0x0038          ;I/O configuration for DIO14
47 IOCFG15            .equ      0x003C          ;I/O configuration for DIO15
48 IOCFG16            .equ      0x0040          ;I/O configuration for DIO16
49 IOCFG17            .equ      0x0044          ;I/O configuration for DIO17
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50 IOCFG18      .equ    0x0048      ;I/O configuration for DI018
51 IOCFG19      .equ    0x004C      ;I/O configuration for DI019
52 IOCFG20      .equ    0x0050      ;I/O configuration for DI020
53 IOCFG21      .equ    0x0054      ;I/O configuration for DI021
54 IOCFG22      .equ    0x0058      ;I/O configuration for DI022
55 IOCFG23      .equ    0x005C      ;I/O configuration for DI023
56 IOCFG24      .equ    0x0060      ;I/O configuration for DI024
57 IOCFG25      .equ    0x0064      ;I/O configuration for DI025
58 IOCFG26      .equ    0x0068      ;I/O configuration for DI026
59 IOCFG27      .equ    0x006C      ;I/O configuration for DI027
60 IOCFG28      .equ    0x0070      ;I/O configuration for DI028
61 IOCFG29      .equ    0x0074      ;I/O configuration for DI029
62 IOCFG30      .equ    0x0078      ;I/O configuration for DI030
63 IOCFG31      .equ    0x007C      ;I/O configuration for DI031
64
65
66 ; Port IDs determine the what peripheral function is routed to the pin
67 ; (e.g. GPIO, SSI). Bits 0 to 5 of IOCFGn registers
68 ;   sec 13.8, pg 1074
69
70 IOCFG_GPIO    .equ    0           ;use pin for GPIO
71 IOCFG_AON32   .equ    7           ;use pin for AON 32 KHz clock
72 IOCFG_AUXIO   .equ    8           ;use pin for AUX IO
73 IOCFG_SSI0_RX .equ    9           ;use pin for SSI0 receive
74 IOCFG_SSI0_TX .equ    10          ;use pin for SSI0 transmit
75 IOCFG_SSI0_FSS .equ    11          ;use pin for SSI0 frame signal
76 IOCFG_SSI0_CLK .equ    12          ;use pin for SSI0 clock
77 IOCFG_I2C_MSSDA .equ    13          ;use pin for I2C data
78 IOCFG_I2C_MSSCL .equ    14          ;use pin for I2C clock
79 IOCFG_UART0_RX .equ    15          ;use pin for UART0 receive
80 IOCFG_UART0_TX .equ    16          ;use pin for UART0 transmit
81 IOCFG_UART0_CTS .equ    17          ;use pin for UART0 CTS
82 IOCFG_UART0_RTS .equ    18          ;use pin for UART0 RTS
83 IOCFG_UART1_RX .equ    19          ;use pin for UART1 receive
84 IOCFG_UART1_TX .equ    20          ;use pin for UART1 transmit
85 IOCFG_UART1_CTS .equ    21          ;use pin for UART1 CTS
86 IOCFG_UART1_RTS .equ    22          ;use pin for UART1 RTS
87 IOCFG_PORT_EVENT0 .equ    23          ;use pin for I/O for event 0
88 IOCFG_PORT_EVENT1 .equ    24          ;use pin for I/O for event 1
89 IOCFG_PORT_EVENT2 .equ    25          ;use pin for I/O for event 2
90 IOCFG_PORT_EVENT3 .equ    26          ;use pin for I/O for event 3
91 IOCFG_PORT_EVENT4 .equ    27          ;use pin for I/O for event 4
92 IOCFG_PORT_EVENT5 .equ    28          ;use pin for I/O for event 5
93 IOCFG_PORT_EVENT6 .equ    29          ;use pin for I/O for event 6
94 IOCFG_PORT_EVENT7 .equ    30          ;use pin for I/O for event 7
95 IOCFG_CPU_SWV .equ    32           ;use pin for CPU SWV
96 IOCFG_SSI1_RX .equ    33           ;use pin for SSI1 receive
97 IOCFG_SSI1_TX .equ    34           ;use pin for SSI1 transmit
98 IOCFG_SSI1_FSS .equ    35           ;use pin for SSI1 frame signal
99 IOCFG_SSI1_CLK .equ    36           ;use pin for SSI1 clock
100 IOCFG_I2S_AD0 .equ    37           ;use pin for I2S data 0
101 IOCFG_I2S_AD1 .equ    38           ;use pin for I2S data 1
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102 IOCFG_I2S_WCLK      .equ      39          ;use pin for I2S WCLK
103 IOCFG_I2S_BCLK      .equ      40          ;use pin for I2S BCLK
104 IOCFG_I2S_MCLK      .equ      41          ;use pin for I2S MCLK
105 IOCFG_RFC_TRACE     .equ      46          ;use pin for RF core trace
106 IOCFG_RFC_D00       .equ      47          ;use pin for RF core data out 0
107 IOCFG_RFC_D01       .equ      48          ;use pin for RF core data out 1
108 IOCFG_RFC_D02       .equ      49          ;use pin for RF core data out 2
109 IOCFG_RFC_D03       .equ      50          ;use pin for RF core data out 3
110 IOCFG_RFC_DI0        .equ      51          ;use pin for RF core data in 0
111 IOCFG_RFC_DI1        .equ      52          ;use pin for RF core data in 1
112 IOCFG_RFC_SDO        .equ      53          ;use pin for RF core SMI data link out
113 IOCFG_RFC_SDI        .equ      54          ;use pin for RF core SMI data link in
114 IOCFG_RFC_SCO        .equ      55          ;use pin for RF core SMI command link out
115 IOCFG_RFC_SCI        .equ      56          ;use pin for RF core SMI command link in
116
117
118 ; General IOCFGn configurations (applies to all registers), bits 31:0
119 ;   example for IOCFG0:
120 ;   sec 13.10.3.1, pg 1103
121
122 IOCFG_GEN_DIN        .equ      0x20006000  ;general purpose data input pin
123                      ;0----- reserved
124                      ;-0----- no hysteresis
125                      ;--1----- input
126                      ;--00----- no wakeup
127                      ;--000----- normal mode
128                      ;--000----- no edge detect events
129                      ;--00----- reserved
130                      ;--0----- no edge detect IRQ
131                      ;--00----- no edge detection
132                      ;--0----- reserved
133                      ;--11----- no pull up/down
134                      ;--0----- normal slew
135                      ;--00----- 2mA output
136                      ;--00----- auto drive strength control
137                      ;--0----- no edge detect RTC event
138                      ;--0----- no edge detect wake up event
139                      ;--000000 general purpose I/O
140
141 IOCFG_GEN_DOUT       .equ      0x00006000  ;general purpose data output pin
142                      ;0----- reserved
143                      ;-0----- no hysteresis
144                      ;--0----- output
145                      ;--00----- no wakeup
146                      ;--000----- normal mode
147                      ;--000----- no edge detect events
148                      ;--00----- reserved
149                      ;--0----- no edge detect IRQ
150                      ;--00----- no edge detection
151                      ;--0----- reserved
152                      ;--11----- no pull up/down
153                      ;--0----- normal slew

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```
154 ;-----00----- 2mA output
155 ;-----00----- auto drive strength control
156 ;-----0----- no edge detect RTC event
157 ;-----0----- no edge detect wake up event
158 ;-----000000 general purpose I/O
159
160 IOC_CFG_GEN_DOUT_4MA .equ 0x00006400 ;general data output pin with 4mA drive
161 ;0----- reserved
162 ;-0----- no hysteresis
163 ;--0----- output
164 ;--00----- no wakeup
165 ;---000----- normal mode
166 ;---000----- no edge detect events
167 ;---00----- reserved
168 ;---0----- no edge detect IRQ
169 ;---00----- no edge detection
170 ;---0----- reserved
171 ;---11----- no pull up/down
172 ;---0----- normal slew
173 ;---01----- 4mA output
174 ;---00----- auto drive strength control
175 ;---0----- no edge detect RTC event
176 ;---0----- no edge detect wake up event
177 ;---000000 general purpose I/O
178
```