CPUreg.inc

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;                                                                              ;
;                                  CPUreg.inc                                  ;
;                            CPU Register Constants                            ;
;                                 Include File                                 ;
;                                                                              ;
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; This file contains the constants for the CPU control registers for the TI
; CC2652 microcontroller.
;
; References: CC13×2, CC26×2 SimpleLink™ Wireless MCU Technical Reference Manual
;             https://www.ti.com/lit/ug/swcu185g/swcu185g.pdf?ts=1761608306803
;
; Revision History:
;     2/17/22  Glen George      initial revision
;    11/05/23  Glen George      updated style and comments
;    10/30/25  Steven Lei       add references to manual


; base addresses
;   table 3.1, pg 319
PRCM_BASE_ADDR      .equ    0×40082000   ;power/reset/clock module registers
SCS_BASE_ADDR       .equ    0×E000E000   ;core system control space registers



; register offsets

; SCS - system control space registers

NVIC_ISER0          .equ    0×0100       ;interrupt set enable (irq 0-31)
NVIC_ISER1          .equ    0×0104       ;interrupt set enable (irq 32-63)
VTOR_OFF            .equ    0×0D08       ;vector table offset register
CCR_OFF             .equ    0×0D14       ;configuration control register


; PRCM - power/reset/clock module registers
;   table 7.27, pg 548

PDCTL0_OFF          .equ    0×012C       ;power domain control register 0
PDCTL1_OFF          .equ    0×017C       ;power domain control register 1
PDSTAT0_OFF         .equ    0×0140       ;power domain status register 0
PDSTAT1_OFF         .equ    0×0194       ;power domain status register 1

CLKLOADCTL_OFF      .equ    0×0028       ;load PRCM settings to CLKCTRL domain
GPIOCLKGR_OFF       .equ    0×0048       ;GPIO clock gate settings
```

```
48 GPTCLKGR_OFF       .equ    0×0054       ;GPT clock gate settings
49 GPTCLKDIV_OFF      .equ    0×00CC       ;GPT clock divisor register
50
51
52
53 ; register bit and value definitions
54
55 ; CCR - configuration control register
56
57 STACK_ALIGN_4      .equ    0×00000000   ;keep stack on 4 byte alignment
58 STACK_ALIGN_8      .equ    0×00000100   ;keep stack on 8 byte alignment
59
60
61 ; PDCTL0 - power domain control register 0
62 ;   sec 7.8.2.46, pg 598
63 ;
64 PD_PERIPH_EN       .equ    0×00000004   ;enable power to peripheral domain
65 PD_SERIAL_EN       .equ    0×00000002   ;enable power to serial domain
66 PD_RFC_EN          .equ    0×00000001   ;enable power to RF core domain
67
68
69 ; PDSTAT0       - power domain status register 0
70 ;   sec 7.8.2.50, pg 602
71
72 PD_PERIPH_STAT     .equ    0×00000004   ;status of peripheral power domain
73 PD_SERIAL_STAT     .equ    0×00000002   ;status of serial power domain
74 PD_RFC_STAT        .equ    0×00000001   ;status of RF core power domain
75
76
77 ; CLKLOADCTL - load PRCM settings to CLKCTRL domain
78
79 CLKLOADCTL_LD      .equ    0×00000001   ;load CLKCTL power domain
80 CLKLOADCTL_STAT    .equ    0×00000002   ;status of CLKCLK power domain load
81
82
83 ; GPIOCLKGR - GPIO clock gate settings
84
85 GPIOCLK_EN         .equ    0×00000001   ;enable GPIO clock in run mode
86 GPIOCLK_ON         .equ    0×00000100   ;force GPIO clock on in all modes
87
88
89 ; GPTCLKGR - GPT clock gate settings
90
91 GPTCLK_EN          .equ    0×0000000F   ;enable all GPT clocks in run mode
92 GPT0CLK_EN         .equ    0×00000001   ;enable GPT0 clock in run mode
93 GPT1CLK_EN         .equ    0×00000002   ;enable GPT1 clock in run mode
94 GPT2CLK_EN         .equ    0×00000004   ;enable GPT2 clock in run mode
95 GPT3CLK_EN         .equ    0×00000008   ;enable GPT3 clock in run mode
96 GPTCLK_ON          .equ    0×00000F00   ;force all GPT clocks on in all modes
```

```
GPT0CLK_ON          .equ    0x00000100   ;force GPT0 clock on in all modes
GPT1CLK_ON          .equ    0x00000200   ;force GPT1 clock on in all modes
GPT2CLK_ON          .equ    0x00000400   ;force GPT2 clock on in all modes
GPT3CLK_ON          .equ    0x00000800   ;force GPT3 clock on in all modes


; GPTCLKDIV - GPT clock divisor register

GPTCLKDIV_1         .equ    0x00000000   ;divide GPT incoming clock by 1
GPTCLKDIV_2         .equ    0x00000001   ;divide GPT incoming clock by 2
GPTCLKDIV_4         .equ    0x00000002   ;divide GPT incoming clock by 4
GPTCLKDIV_8         .equ    0x00000003   ;divide GPT incoming clock by 8
GPTCLKDIV_16        .equ    0x00000004   ;divide GPT incoming clock by 16
GPTCLKDIV_32        .equ    0x00000005   ;divide GPT incoming clock by 32
GPTCLKDIV_64        .equ    0x00000006   ;divide GPT incoming clock by 64
GPTCLKDIV_128       .equ    0x00000007   ;divide GPT incoming clock by 128
GPTCLKDIV_256       .equ    0x00000008   ;divide GPT incoming clock by 256
```