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EE 90

Lab 1 Report

Introduction and Design

The goal of this lab is to design and analyze a PID compensation network using ADA4851 op-amps. The circuit is implemented on a PCB and component values for the P, I, and D stages are specced out and then soldered on. The Bode and FFT responses are measured and compared to the expected responses. Noise analysis of the op-amps is also performed to see its effect on the circuit.

According to the lab instructions, the expected Bode response for the PID compensation network should contain circuit poles at e-10,-1000 ± j9.3e-6, and-1e5 rad/sec with the zeros being at t-29.5,-1000, and-4833 rad/sec. The low frequency gain is 23.5 dB, the mid-band gain is 14.06 dB at 188.5 rad/sec, and the high-band gain is 0.314 at 25,132 rad/sec. The schematic for the PID circuit is provided by the lab instructor:

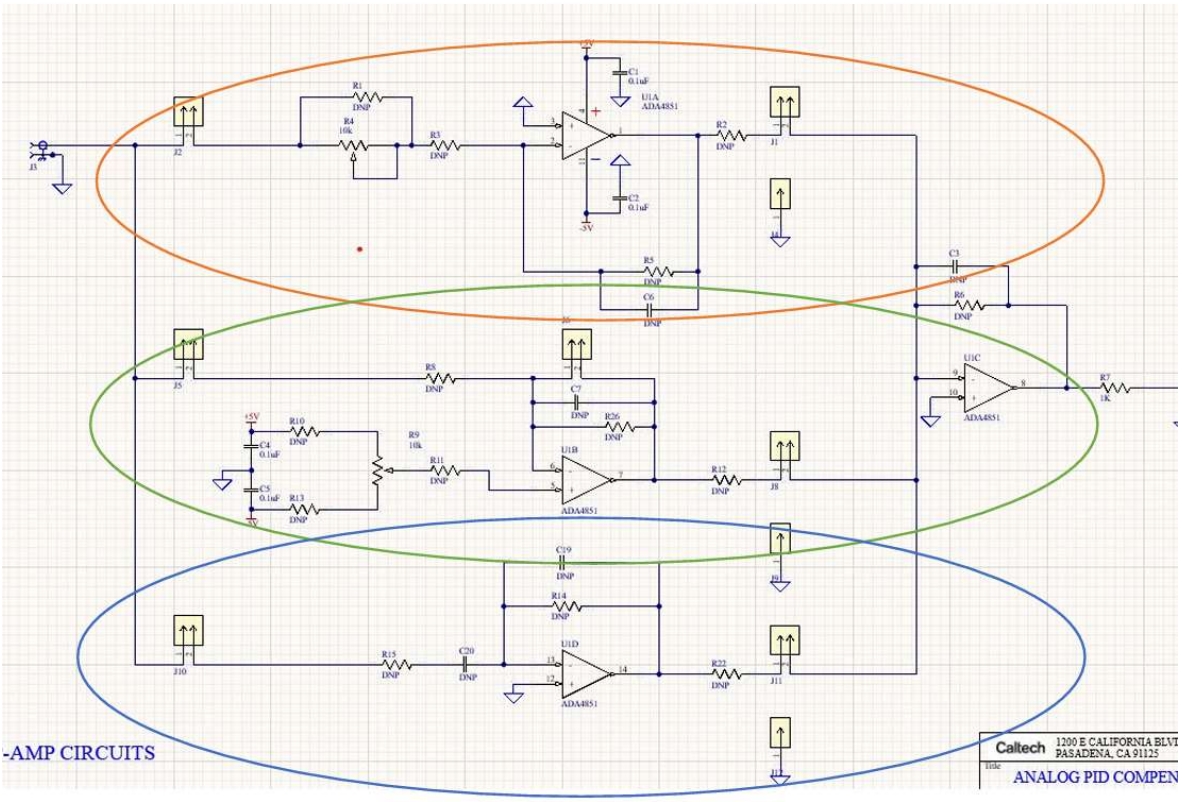

Figure 1: PID circuit. P stage (red), I stage (green), and D stage (blue) are shown.

Through circuit analysis, we derived the following gains ($V_{\{STAGE\}\ OUT}/V_{IN}$) for each stage of the PID controller:

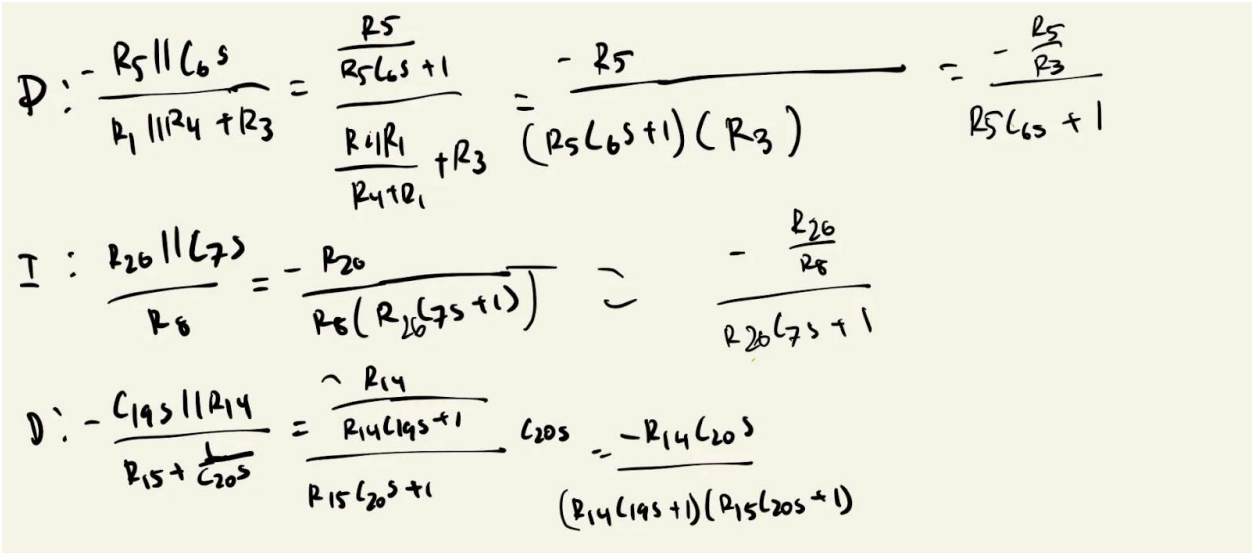

Figure 2: Equation for each controller stage

And the overall summer gain is:

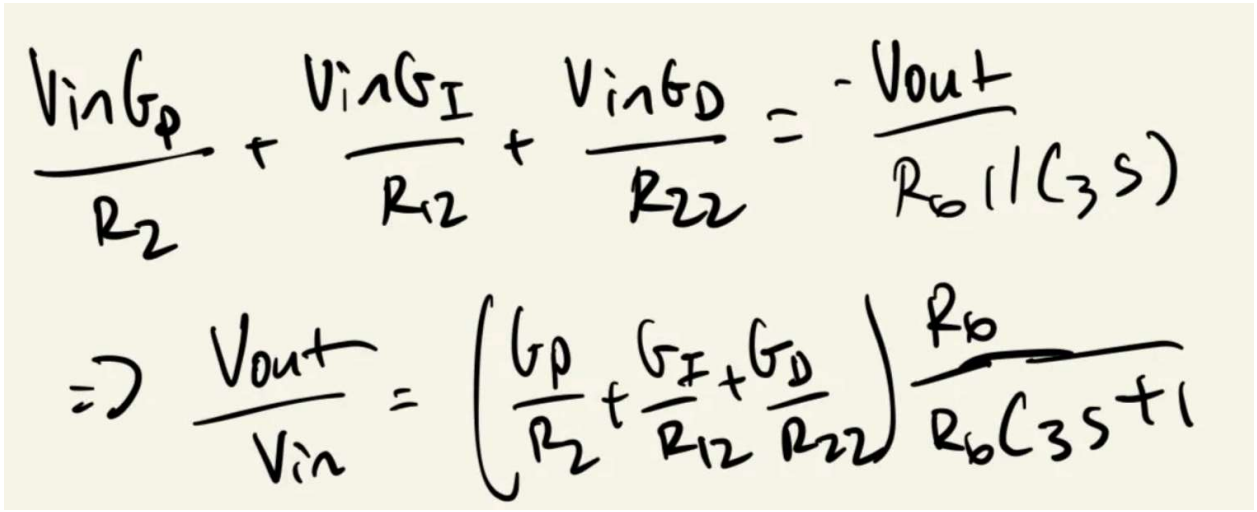

Figure 3: Equation for overall summer gain, where G_P, G_I, G_D are gains at each stage from above

Note that these component numbers reflect the ones used in the attached schematic/provided Altium document.

To determine component values, we first picked out values to satisfy the pole conditions of the circuit. Since we have a low frequency pole at -10 rads/s, that is most likely from the integrator and thus we can set $R_5C_6 = 10^{-1}$ and similarly the midband pole at -1000 rads/s is from

the proportional stage so $R_{26}C_7 = 10^{-3}$. The high frequency pole at -10^5rads/s thus is from the differentiator, and the remaining -1000 rads/s pole must also come from the differentiator since it has a double pole denominator, so $R_{14}C_{19} = 10^{-5}$ and $R_{15}C_{20} = 10^{-3}$. To find constraints of the rest of the component values, we should use the provided zeros and gains given to us. However, doing this analytically for us led to extremely large component values in resistors and capacitors. We tried two different methods analytically without much success. First, we tried solving for the zeros using a system of equations and combining the P, I and D stage equations into one fraction. The other method we tried was substituting frequencies into our gain equations and equating it to known gains. However, given the restriction that all component values should be decade based and that we could plot our PID stage using matplotlib, we found the best component values by computation through python. Through a few iterations of trying to correct each gain plot individually, we arrived at the following values:

P stage: $R_1 = 0\Omega$, $R_3 = 1k\Omega$, $R_2 = 10k\Omega$, $R_5 = 10k\Omega$, $C_6 = 0.1\mu F$

I stage: $R_{11,}R_{10,}R_{13} = 0\Omega$, $R_8 = 10k\Omega$, $R_{26} = 100k\Omega$, $R_{12} = 10k\Omega$, $C_7 = 10\mu F$

D stage: $R_{15} = 1k\Omega$, $R_{14} = 1k\Omega$, $R_{22} = 10k\Omega$, $C_{19} = 10nF$, $C_{20} = 1\mu F$

Summer: $R_6 = 10k\Omega$, $C_6 = 0F$

which produced a graph that was very similar to the expected Bode response:

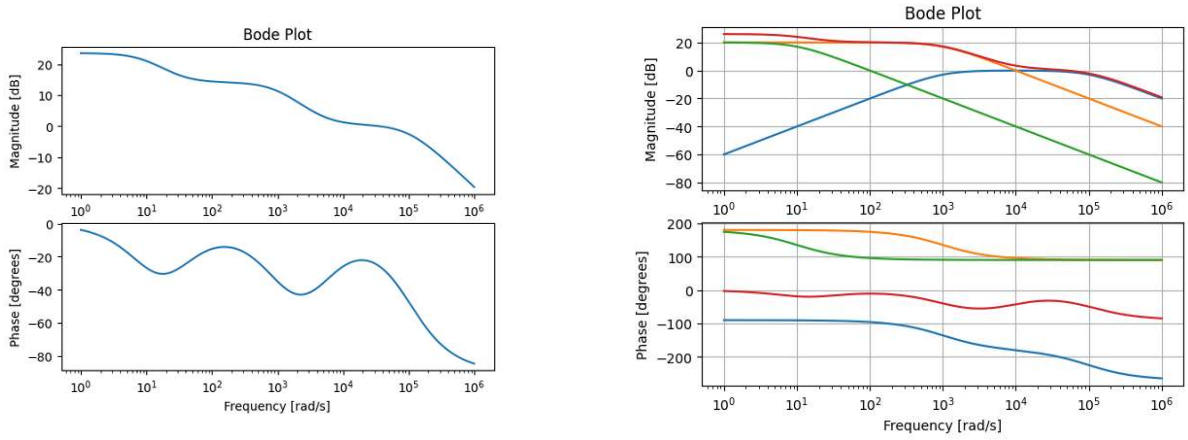

Figure 4: Bode response of expected (left) vs designed (right) circuit (red = total PID response)

We further simulated our circuit in LTSpice to verify the response:

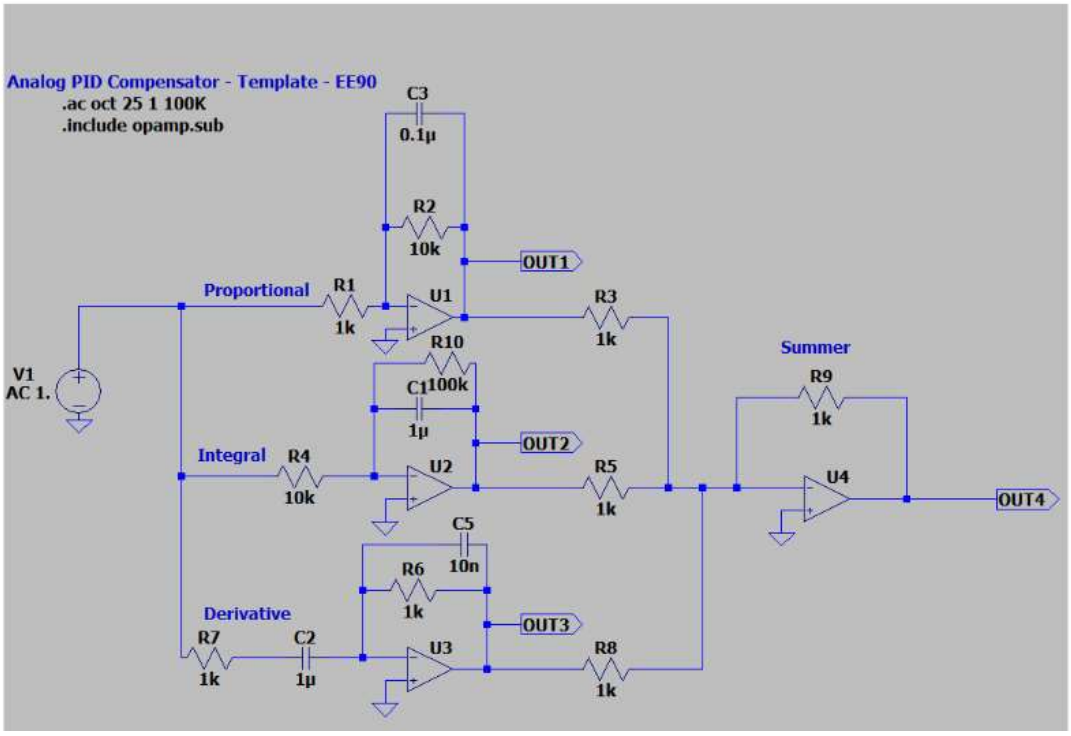

Figure 5: LTSpice model of circuit

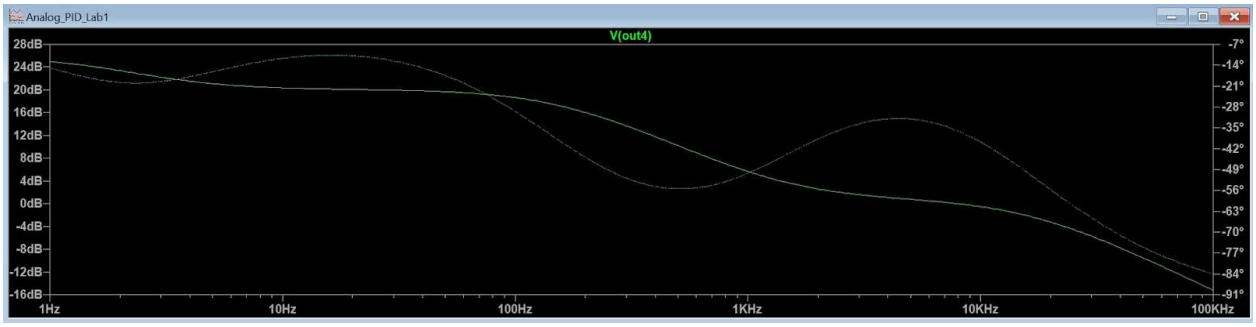

Figure 6: LTspice simulation (note graph is in Hz, not rads/s)

We can see that our designed circuit produces a response very similar to the expected response. For both, the low frequency gains starts out at 24 dB, with two gain plateaus at 20 dB and 0 dB. The high frequency gain at 10^6 rads/s is -20 dB, and the poles/zeros are at the correct spots. The phase also starts and ends at approximately the same angle with a similar shape.

Setup and Experiment

With the component values chosen, we then soldered SMD resistors and capacitors onto our PCB.

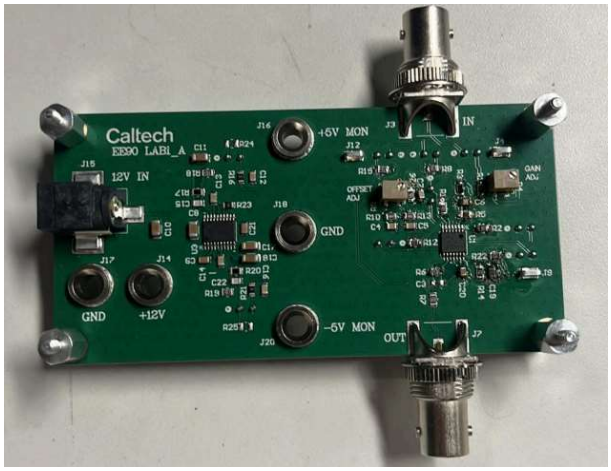

Figure 7: PCB with soldered on components

We then measured the input voltage and regulator output voltages using a voltmeter to ensure the regulator works within < 300mV. Then we checked for shorts in our circuit by measuring output voltages at J13 and J19. Lastly, we tuned our integrator offset using potentiometer R_9 such that the offset was less than +- 10mV.

We measured our circuit's Bode response using the DH0924S oscilloscope. We connected a BNC cable from the AWG output to the input of our circuit and channel 1 of the scope. We then connect the output of the circuit to channel 2 of the scope with a BNC cable. Lastly, we attach the 12V power supply from the wall wart to the PCB. The following settings were used through the Bode menu of the scope:

Sweep Type: Log, **Disp Type**: Wave, **Start Freq**: 10 Hz, **Stop Freq**: 100kHz,

Points: 50, **Amplitude**: 100 mV.

For the P and D stages we were able to get a bode response with little noise using a 100 mV amplitude. However, the I stage was exceptionally noisy, so we used the largest amplitude possible (5V) to minimize the effect of noise. After verifying all stages were correct, we then measured the total output of the PID controller by connecting all jumpers on the PCB. All of the data was recorded into a .csv file and graphed using python.

Lastly, we performed a FFT measurement using the FFT function in the oscilloscope. We disconnected the input of the circuit from the scope and replaced it with a BNC termination. We kept the output connected at channel 2. We used the following settings for the FFT measurement:

Window Type: Hanning, **Center Frequency:** 50 kHz, **Span**: 100 kHz, **Scale**: 35 dbV

and on the channel we used the following acquisition settings:

Averages: 64 (this helps reduce the noise floor).

Data of the FFT measurement was collected by saving the scope screen as an image.

Results

Voltage measurements:

Power supply voltage: 11.92V (target is 12V)

Rail supply voltage: 5V and -4.98V (target is 5V)

Integrator offset: -4mV (target is less than +-10mV)

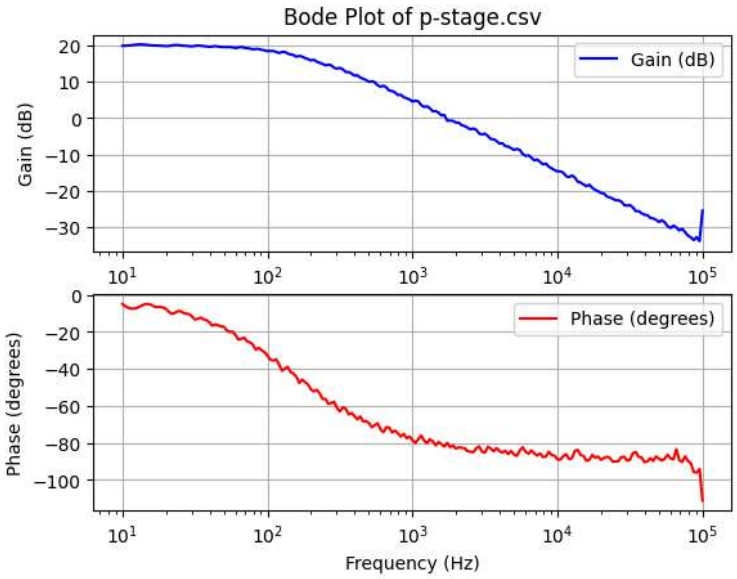

Figure 8: Bode response of P-stage

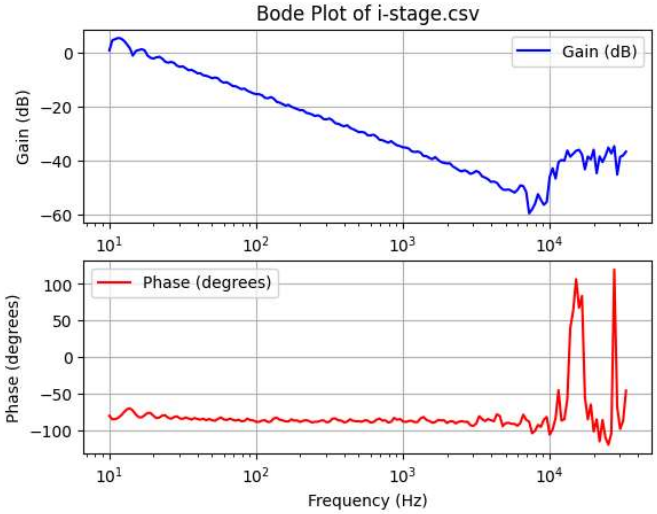

Figure 9: Bode response of i-stage (note the noise at high frequencies)

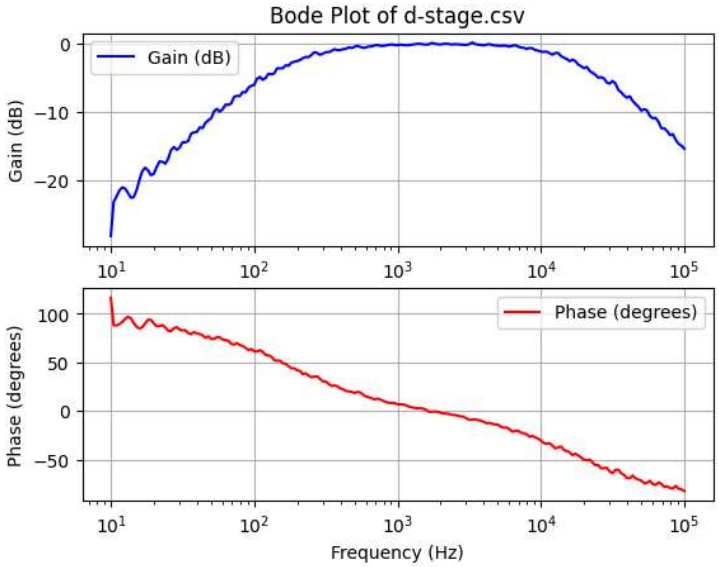

Figure 10: Bode response of the D-stage

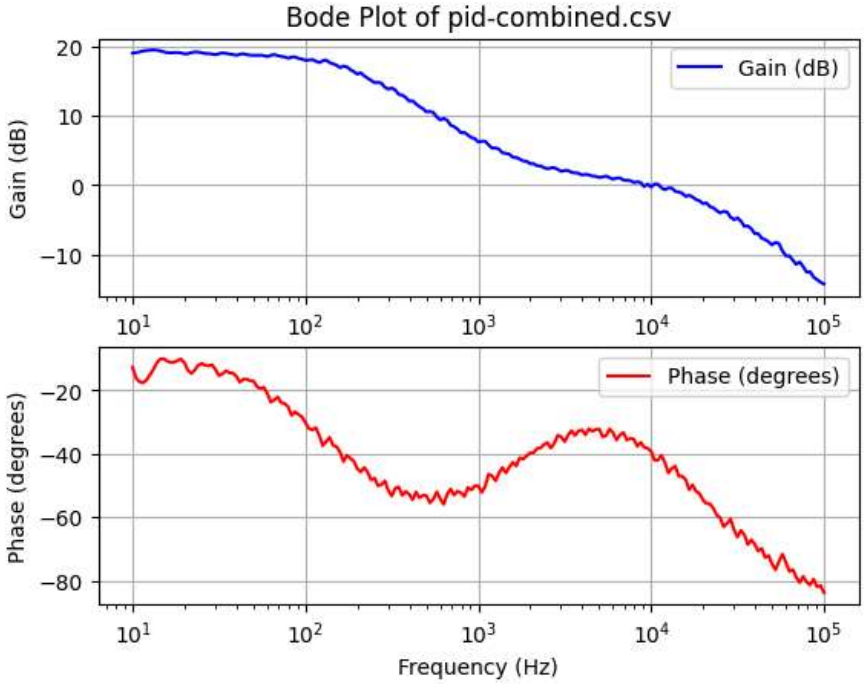

Figure 11: Bode response of total response (PID)

Figure 12: FFT Response

Analysis

Bode Response

From our plots, we can see that our implemented circuit behaves similarly to the simulated version of our designed circuit. There is also an offset in the measured phase response for the P, I, and D graphs relative to the simulated graphs, which could possibly be due to an inconsistency in how the oscilloscope measures phase shifts. However, the overall shape and response of the gain and phase in the measured P, D, and combined graphs are very similar to the respective simulated graphs (with exception to the I stage, due to noise). Using python, I was able to overlay the data of the combined PID stage for measured vs simulated. Note that because the minimal frequency allowed for the oscilloscope bode plot is 10Hz, we do not have data of very low frequencies from 0-10 Hz to compare with:

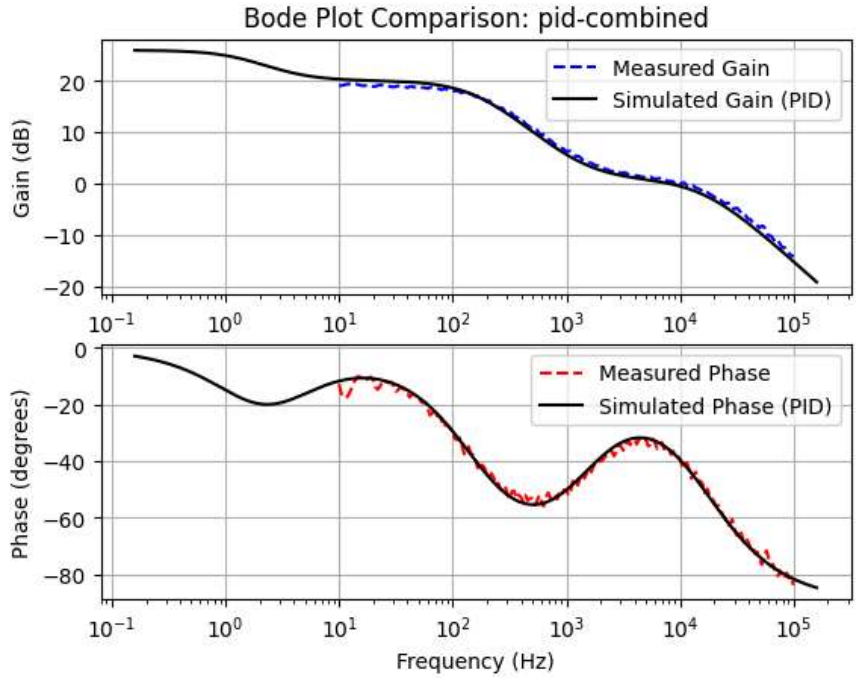

Figure 13: Measured response vs simulated response using designed circuit

We can see that the gain and phase response is very accurate between our measured and simulated circuits. There are some inaccurate points, which can be accounted for by the component tolerances, non-idealities in the op-amp, and potential scope noise/measuring inaccuracy. We can also compare this to the graph of the expected response provided by the instructor. The low frequency gain at ~16Hz (100 rads/s) is about 20dB, midband 1600 Hz (10,000 rads/s) gain is 2 dB, and high frequency gain at 16000 Hz (100,000 rads/s) is about -4

dB for our physical circuit. Based on the instructor provided graph, the gains at these respective frequencies are about 15 dB, 0dB, and -2dB. While these are only 3 test points, judging from the shape and comparison with the simulated graph, we can fairly say that our measured circuit behaves similarly to the expected circuit.

FFT and Noise

We did not see a spike in the noise floor at ~70 kHz in our FFT. However, if we were to see one, it would probably not be a "real" spike because there is probably high frequency noise coming from the RC-network controlling the integrator offset. Since this high frequency cannot be detected by the scope properly, it is probably aliased into the scope and that is the ~70 kHz spike we should see. We used 0 ohm resistors for our integrator offset adjustment, which could possibly be the reason why we don't see the spike.

From our FFT, we can notice that white noise starts appearing after the -66.53 dBV drop. We also use a 100kHz span with 10k sampling points, as shown in the image. This means our frequency bandwidth is 0.1Hz Thus, our noise floor is $10^{-66.53/20}/\sqrt{(0.1)} = 0.05$ V/√Hz.

For calculating the spot noise through the p-stage and summer @1 kHz, we can first note that we can use the same equation for both op-amps since they are configured in the same manner (ignoring feedback capacitances). Using the op-amp noise model, we can represent the stages as:

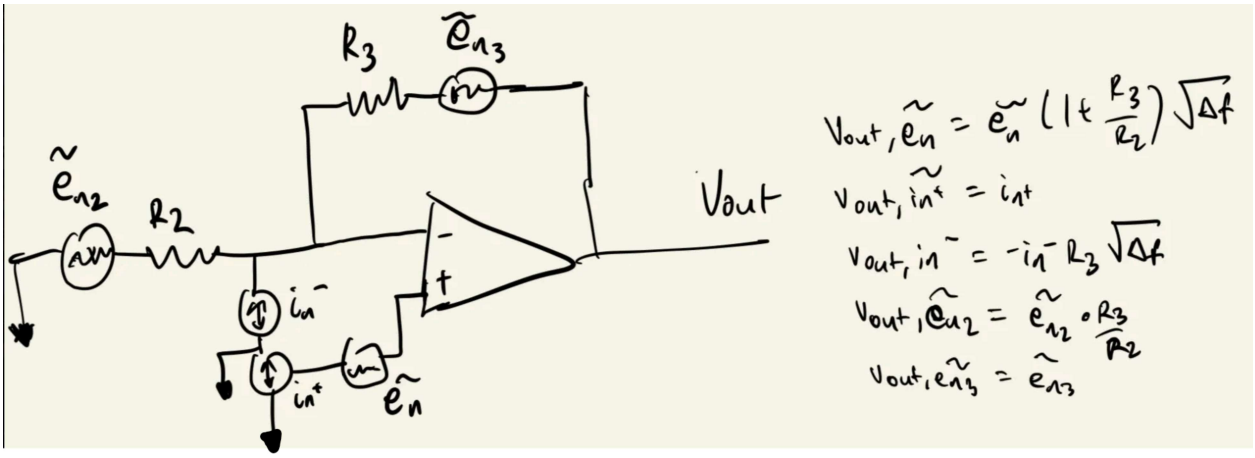

Figure 14 : Op-amp noise model for the P/Summer stage

and we can get the equations by selecting only 1 noise source and nulling the rest. Our V_{TOTAL_RMS} is then

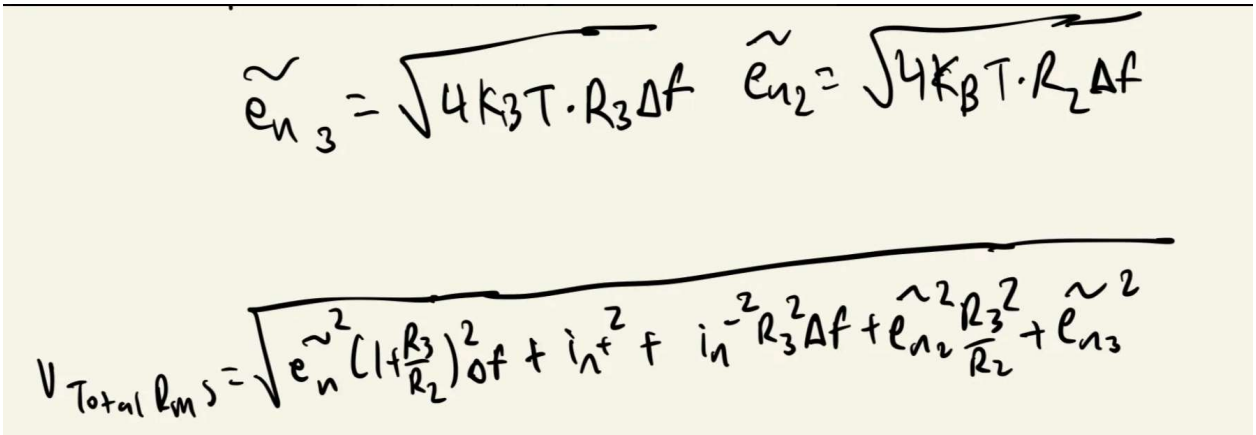

Figure 15: V_{TOTAL_RMS} calculation for spot noise.

Note that e_n = 30 nV/√Hz and i_n = 5.3 pA/√Hz can be found by looking at the voltage noise and current noise vs frequency graphs in the ADA4851 op-amp data sheet. Note that K_B is the Boltzman constant, T = 298.15K (room temperature in Kelvins), and Δf = 1 since we are looking at only 1 frequency point. For the p stage, using R_3 = 10k and R_2 = 1k, we find the V_{TOTAL_RMS} = 0.3 uV√Hz. For the summer stage, R_3 = 1k and R_2 = 1k, so V_{TOTAL_RMS} = 0.06 uV√Hz, meaning that the total spot noise @ 1kHz is 0.36 uV√Hz.

Thus the calculated spot noise of 0.36 uV√Hz. is much lower than the noise floor of 0.05 V√Hz we measured from the FFT. This means that our scope is not able to measure the spot noise through the p-stage and summer because the scope noise floor is too high.

Conclusion and Summary

In this lab, we were able to design, implement, measure, and analyze a PID controller and its response. We were given a desired Bode response of the circuit and the schematic, and using circuit analysis, were able to derive component values to hit the target poles that characterize the Bode response. Using python and matplotlib plotting, we were further able to computationally derive other component values to achieve roughly the desired gain and phase response. We then simulated the designed circuit in LTSpice to confirm our python simulation.

We then populated our PCB with components and tuned settings such as the voltage regulator and integrator offset before taking measurements. We recorded Bode responses using the oscilloscope for each P, I, D stage, and the combined result. Our resulting combined response plot was very similar to our combined response plot in both phase and gain, meaning our circuit was relevantly accurate to the expected response provided by the instructor.

Lastly, we performed an FFT on the circuit with no input to determine the noise floor. We did not find a 70kHz spike in the noise floor. We calculated a spot noise measurement and found it to be much lower than the noise floor, indicating that the scope cannot pick up the spot noise at 1 kHz.

Some further measurements we can do include comparing our measured PID response with the actual expected response (if we had the data points) provided by the instructor. We can further measure the accuracy by calculating the average difference between points at a given frequency. With regards to noise, we can also look at the spot noise through the integrator and differentiator, as well as the combined response and compare that to the noise floor. This would provide further insight on if the scope could truly measure the circuit noise at 1 kHz. We could also repeat this for smaller and target larger frequencies.