ATMega64 Timers

	Timer 0	Timer 1	Timer 2	Timer 3
Bits	8	16	8	16
Modes	Auto Reload Fast PWM ϕ Correct PWM Asynchronous Mode	Auto Reload Fast PWM ϕ Correct PWM ϕ/f Correct PWM Input Capture Frequency Generator Event Counter	Auto Reload Fast PWM ϕ Correct PWM	Auto Reload Fast PWM ϕ Correct PWM ϕ/f Correct PWM Input Capture Frequency Generator Event Counter
Control Registers	TCCR0	TCCR1A TCCR1B TCCR1C	TCCR2	TCCR3A TCCR3B TCCR3C
Count Registers	TCNT0	TCNT1H TCNT1L	TCNT2	TCNT2H TCNT2L
Output Compare Registers	OCR0	OCR1AH OCR1AL OCR1BH OCR1BL OCR1CH OCR1CL	OCR2	OCR3AH OCR3AL OCR3BH OCR3BL OCR3CH OCR3CL
Input Compare Registers		ICR1H ICR1L		ICR3H ICR3L
Asynchronous Status Register	ASSR			
Special Function Register (SFIOR)	TSM (7) PSR0 (1)	TSM (7) PSR321 (0)	TSM (7) PSR321 (0)	TSM (7) PSR321 (0)

Timer Interrupts

	Timer 0	Timer 1	Timer 2	Timer 3
Interrupt Mask TIMSK	OCIE0 (1) TOIE0 (0)	TICIE1 (5) OCIE1A (4) OCIE1B (3) TOIE1 (2)	OCIE2 (7) TOIE2 (6)	
ETIMSK		OCIE1C (0)		TICIE3 (5) OCIE3A (4) OCIE3B (3) OCIE3C (1) TOIE3 (2)
Interrupt Flag TIFR	OCF0 (1) TOV0 (0)	ICF1 (5) OCF1A (4) OCF1B (3) TOV1 (2)	OCF2 (7) TOV2 (6)	
ETIFR		OCF1C (0)		ICF3 (5) OCF3A (4) OCF3B (3) OCF3C (1) TOV3 (2)

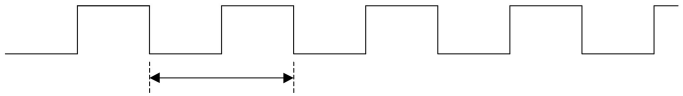
Timer Prescalar

Setting	Frequency (f)	Period (P)
clock / 1	8 MHz	125 ns
clock / 8	1 MHz	1 µs
clock / 32	250 KHz	4 µs
clock / 64	125 KHz	8 µs
clock / 128	62.5 KHz	16 µs
clock / 256	31.25 KHz	32 µs
clock / 1024	7.3125 KHz	128 µs

8-bit Timer Outputs

Auto Reload

Square Wave

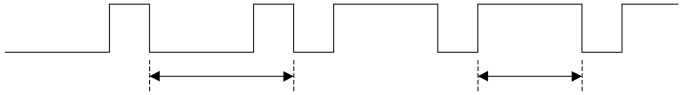


Period = 2 × OCRn × P

Frequency = f / (2 × OCRn)

assumes OCn in toggle mode

Fast PWM



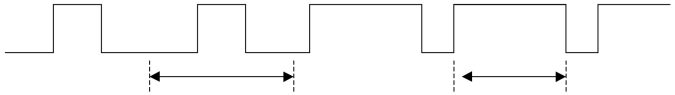
Period = 256 × P

Frequency = f / 256

Width = OCRn × P

assumes OCn in non-inverted mode

Phase Correct PWM



Period = 512 × P

Frequency = f / 512

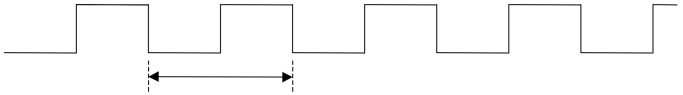
Width = 2 × OCRn × P

assumes OCn in non-inverted mode

16-bit Timer Outputs

Auto Reload

Square Wave

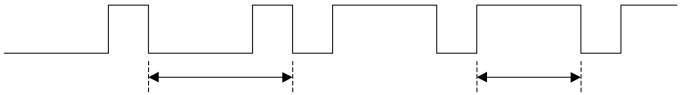


Period = 2 × OCRnx × P

Frequency = f / (2 × OCRnx)

assumes OCnx in toggle mode

Fast PWM



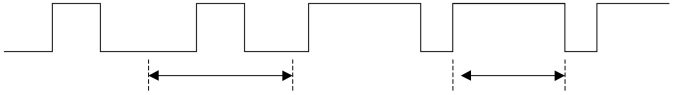
Period = n × P

Frequency = f / n

Width = OCRnx × P

assumes OCnx in non-inverted mode

Phase Correct PWM



Period = 2 × n × P

Frequency = f / (2 × n)

Width = 2 × OCRnx × P

assumes OCnx in non-inverted mode

n is: 256 512 1024 OCRnA ICRn

not allowed in Frequency and Phase Correct PWM