A 20mV Rectifier for Boosting Internet of Natural Things (IoNT)

Cleonilson Protasio de Souza, Andréa Willa Rodrigues Villarim
Department of Electrical Engineering
Federal University of Paraiba
João Pessoa, Brazil
{protasio, andrea.villarim}@cear.ufpb.br

Orlando Baiocchi
Institute of Technology
University of Washignton Tacoma
Tacoma, USA
baiocchi@uw.edu

***Abstract*—Internet of Natural Things (IoNT) is a new paradigm coming from IoT that enable Natural Things, as trees, to be connected to the Internet. However, to embed electronic in natural trees is a challenge since the use of chemical batteries is not a reasonable solution. For this, Energy Harvesting, that is, the conversion of ambient energy present in the environment into usable electrical energy, is a very interesting solution, but the low level of generated energy from the ambient energy causes the necessity to develop low-power and low-voltage circuits. A very frequently circuit need in this context is the rectifier since a lot of energy sources generate alternate voltage. In this paper, a 20mV MOSFET-based rectifier based on Latour detector and on Zero-Threshold transistor is introduced. A discrete prototype of the rectifier has been made and experimental results confirm its low-voltage operation when the input voltage supply is about 20 mV or even lower.**

Keywords*— Internet of Natural Things, Energy Harvesting, Low-power and low-voltage circuit, Latour's detector, Zero-threshold transistor.

I. Introduction

A very significant and crucial issue related to Wireless Sensor Network (WSN) is the power supply for its sensor nodes. Usually, chemical batteries are the main or unique solution for that. However, routinely maintenance is needed since batteries must be regularly replaced or recharged, which in some cases may be very difficult, dangerous or impossible in distant or inaccessible locations [1], [2]. Consequently, this can imply in substantial and additional costs and complexity to change or charge batteries with a given regularity [3]. Furthermore, used-up batteries are potentially detrimental to natural environments and they also need to be stored before been recycled [1].

As a potential solution, if the sensor nodes of a WSN could be powered from some kind of environmental energy surrounding them, then the WSN may operate in an energy autonomous and maintenance-free way, and with theoretically infinite lifetime (taking only the battery capacity in consideration). This context has given rise the concept and development of Energy Harvesting.

Energy harvesting is the conversion of ambient energy present in the environment into usable electrical energy by collecting, conditioning, and storing of the harvested energy [4]–[9] into low-power electronic devices, particularly into portable and wireless ones used in WSN and Internet of Things (IoT). Some examples of ambient energy used in energy harvesting are heat, vibration, sun, and others.

Fig. 1 shows a block diagram of an energy-harvesting based sensor node [4] where the main blocks related to energy harvesting are (I) the energy transducer, (II) the energy conditioning circuit, and, if need, (III) an optional storage devices that can be either a supercapacitor or even a battery. The energy transducer performs the conversion of a primary ambient energy source to electrical energy and the energy management circuit carries out voltage rectification, conversion, regulation, and others.

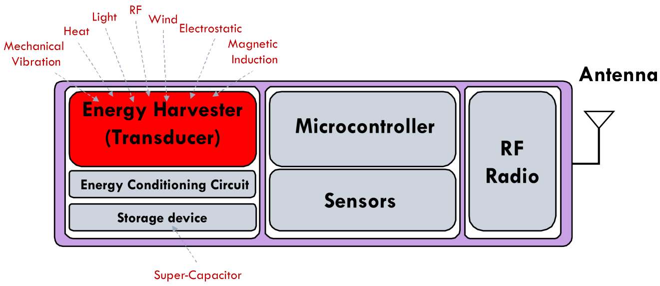

Fig. 1. An architecture of an energy harvesting based sensor node [4].

Among several energy harvesting solutions, *e.g.* solar cells [10], [11], piezoelectricity [12], RF [13], [14], magnetic induction [6], [7], the thermoelectric-based energy harvester [5], [9] is been classified as one of the most promising technologies to convert waste heat into electrical energy [15]. In recent years, the number of thermoelectric energy harvesting applications has increased, for example, Reference [16] has introduced the concept of Internet of Natural Things (IoNT) and has conceived the idea of a Smart Tree, in which a tree can generate its own energy by thermoelectricity to power a low-power embedded sensor node, as shown in Fig. 2. The idea consists in harvesting the thermal gradient between the tree's external temperature and the internal temperature of its trunk. The experiment showed that it is possible to get energy from that gradient. However, they observed that, on day light, the gradient is positive (external temperature greater than internal one) generating (+) positive voltage when a semiconductor thermoelectric generator (TEG, also called Peltier cell) is used, and, at night, generating (−) negative voltage, since a temperature reversion takes place, that is, the external temperature is lesser than the internal one. The TEG is based

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on the Seebeck effect meaning that the generated voltage is proportional to the temperature gradient on its sides [4].

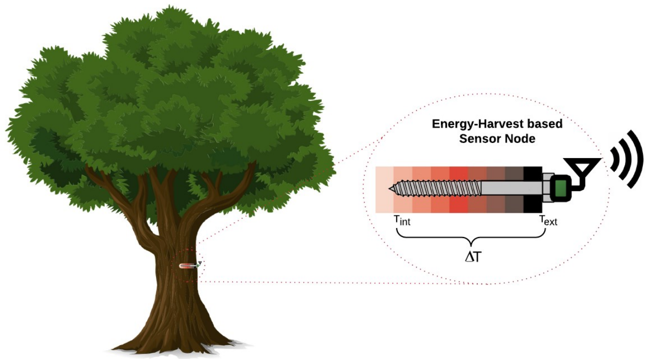


Fig. 2. An instance of an Internet of Natural Things (IoNT): a Smart Tree [16].

The achieved average absolute voltage was about 35 mV [16], which could be applied to, for example, a voltage step-up dc-dc converter integrated circuit like the LTC3108 from Linear Technology that operates from at least 20 mV to achieve 3.3V needed to power a sensor node. Taking in consideration that the LTC3108 works only on positive input voltage level and the TEG output voltage can present either (+) positive or (−) negative voltage level, an ultra-low-voltage rectifier circuit is needed to convert the TEG output voltage into a positive one to be applied to the LTC3108. Fig. 3 shows the TEG, in which its output voltage can vary from + to − voltage level according to the Smart Tree's thermal gradient in the moment, connected to a rectifier (*D*) and to the step-up converter to power a sensor node.

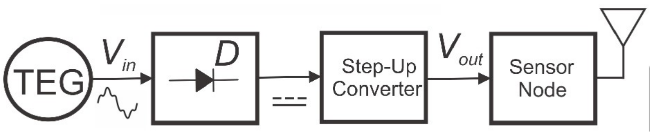


Fig. 3. A general view of a sensor node TEG-based power supply where the TEG is subject to bipolar temperature gradient.

It is well known that a simple diode-based rectifier requires at least about 700 mV to be operational, but this level of voltage is too huge to be considered in the Smart Tree project. Therefore, in this work, a 20mV MOSFET-based rectifier based on a Zero-Threshold transistor is introduced. A discrete prototype of the rectifier has been made and the measurement results confirm its low-voltage operation when the input voltage supply is at least 20 mV.

The rest of the paper is organized as follows. Section 2 presents some low-loss rectifier topologies. Section 3 describes a rectifier topology based on the Latour's detector, the application of zero-threshold transistor and the proposed Latour-based rectifier topology. Section 4 presents the experimental results of the proposed solution. Finally, Section 5 presents the conclusions.

II. LOW-LOSS RECTIFIER TOPOLOGIES

Rectifier circuits convert AC voltage source to a coarse DC level to be applied to the next stage of energy regulation (normally, a filter and a voltage regulator). In general, full-wave rectifier is often preferred to the half-wave counterpart because it results in a smaller output ripple voltage and consequently the filter is optimized. The disadvantage is that the voltage drop of full-wave rectifier is greater at least two times, due to the diode forward voltage drop, resulting in a lower Voltage Conversion Efficiency (VCE) causing considerable loss in AC to DC conversion, except that the diodes are implemented in low-threshold-voltage transistors [17].

High-VCE rectifiers are usually applied to RFID, biomedical instrumentation, and in any electronic device where the energy level is critical, as in energy harvesting system. Some rectifier topologies are based on: (I) Threshold-voltage cancellation techniques [18], [19]; (II) circuits with active-diode using operational amplifiers [20], [21]; (III) bridgeless AC-DC converters [20]; (IV) conventional AC-DC rectifier using transistors instead of diodes [19], [21].

Currently, transistor-based rectifiers have been based on MOSFET transistor and, in general, they are studied to reduce the voltage drop of the constituent transistors and to improve rectifier's power and voltage efficiency [19], [20], [22].

Taking in consideration full-wave rectifiers, the main transistor-based rectifier topologies are the full-wave rectifier using four diode-connected MOS transistors and the full-wave rectifier using cross-coupled MOS transistors, as shown in Fig. 4.

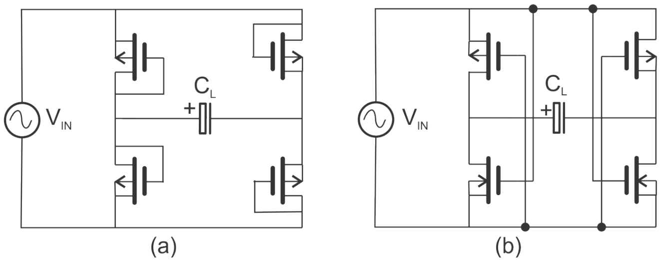


Fig. 4. Full-wave rectifier topologies using: (a) four diode-connected pMOS transistors. (b) two cross-coupled nMOS transistors and two diode-connected pMOS transistors [23].

However, the most is the number of diodes, the greater is the drop voltage and both topologies shown in Fig. 4 includes a path from AC to DC that adds up two voltage drops. In addition, rectifier topologies aiming high VCE include more transistors to achieve their objectives arising the cost and complexity.

The issue concerning how to obtain a high-VCE with less transistor count takes an optimal solution when two factors are taken in account: a one-voltage-drop rectifier topology and the usage of zero-threshold transistor.

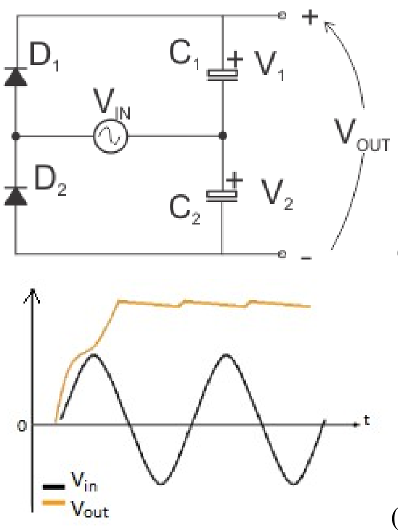
The next section, a solution taking these factors into account is proposed.

III. A Latour-based Rectifier Topology

Taking into consideration the factors to obtain an optimal solution for a high-VCE rectifier, namely, a **one-voltage-drop rectifier topology** and the use of **zero-threshold transistor**, the following two subsections deal with them in separate and, in the third subsection, a rectifier topology is introduced.

A. One-voltage-drop rectifier topology

The one-voltage-drop rectifier topology considers in this work is the voltage-doubler type-Latour-structure diode-based rectifier as described in [24], called here Latour's Rectifier, that is based on the Latour's doubler detector. The Latour's rectifier is composed of two rectifier diodes D_1 and D_2 and two capacitors C_1 and C_2, as shown in Fig. 5(a), and the AC voltage source is given by V_{in}. The operation of the Latour's Rectifier consists in charge the capacitor C_1 through D_1 in series with it, in the positive half wave of V_{in}, generating the voltage V_1. In the negative half wave of V_{in}, the capacitor C_2 is charged through D_2 generating the voltage V_2. The Latour's Rectifier output voltage V_{out} is then equals $V_1 + V_2$, that is, the double of the peak value of V_{in} minus the diode forward drop. Clearly, it is a one-voltage-drop rectifier topology. Fig. 5 (b) shows V_{in} and the resulted V_{out}.



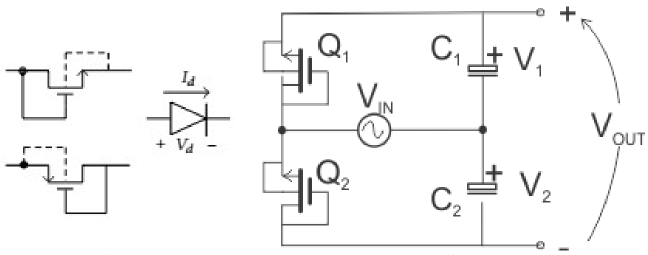
(a)

(b)

Fig. 5. (a) The Latour's Rectifier and (b) the corresponding input and output waveforms. Source: [24].

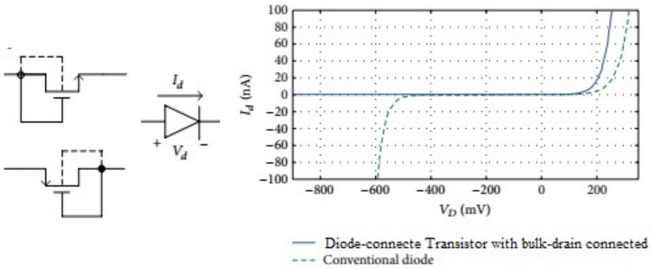
To converter the Latour's Rectifier to a diode-connected MOS transistor, simply it is necessary to exchange D_1 and D_2 for their transistor-base counterpart, as shown in Fig. 6.

Nonetheless, as described in [25], the conventional diode-connected MOS transistor presents some drawback that can be overcome when the transistor's bulk is connected to the drain instead of the source, as shown in Fig. 7(a). The diode-connected MOS transistors with interconnected bulk-drain introduced in [25] reduce the threshold voltage and leakage current of the diode-connected MOS transistors, as shown in Fig. 7(b) and, therefore, it contributes to increment of the rectifier's VCE, output current, and efficiency.



(a) (b)

Fig. 6. (a) Conventional diode-connected MOS transistors [25] and (b) Latour's Rectifier using diode-connected MOS transistors.



(a) (b)

Fig. 7. (a) Diode-connected MOS transistors with bulk-drain interconnected [25] and (b) I-V characteristic comparison of the Diode-connected MOS transistors with bulk-drain interconnected with the conventional Diode-connected MOS transistors. Source: [25].

B. Zero-threshold transistor

Currently, with the huge studies and implementations of low-power and low-voltage applications, zero-threshold MOS transistors have turned out to be more and more attractive for those applications due to the advantages of these devices, though the concept of zero-threshold transistors was introduced in the mid 90's [26]. Zero-threshold transistor's manufactures radically setting the threshold voltage of this device to zero achieves, as a result, the optimum power dissipation, but having as drawback that the device will never completely switch off [26].

One current low-cost zero-threshold transistor is the ALD310700 from Advanced Linear Devices (ALD), that is a member of a patented technology of ALD called EPAD MOSFET, which threshold voltage is fixed to zero, but presents very low leakage characteristics similar to that for a conventional MOSFET [27].

The ALD310700 is an integrated circuit composed of 4 PMOS transistors matching with the threshold voltage set precisely at +0.00V +/-0.02V, featuring a typical offset voltage of only +/-0.001V (1mV), as showing in Fig. 8. It is important to observe that the substrate pin is externally available.

C. The Proposed Latour-based Rectifier Topology

In this work, a Latour-based MOS rectifier topology is proposed. The topology is based on the Latour's Rectifier using diode-connected MOS transistors, as shown in Fig. 6, but the diode-connected MOS transistors in it have their bulk and drain interconnected, according to Fig. 7. As an important result, the proposed rectifier topology shows to be very efficient and work with input voltage extremely small. In addition, it takes the advantages of both the one-voltage-drop rectifier topologies and of using diode-connected MOS transistors with interconnected bulk-drain. Fig. 9 shows the combined circuit.

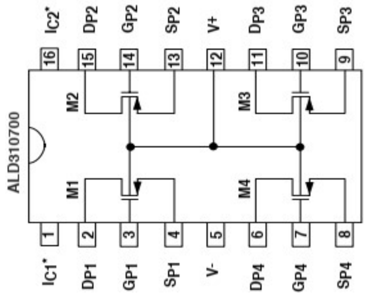


Fig. 8. ALD310700 pin configuration [28].

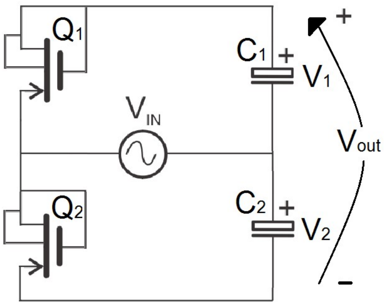


Fig. 9. Latour's Rectifier using diode-connected MOS transistors with interconnected bulk-drain.

IV. Experimental Results

In order to assess the proposed Latour's Rectifier using diode-connected MOS transistors with interconnected bulk-drain with respect to its capabilities to work with extremely low-voltage, the load capacitances were exchanged to load resistor, as shown in Fig. 10, in order to obtain experimental result without capacitive filter influence.

For the experiment, an AFG1022 Arbitrary/Function Generator and a MSO2024B Mixed Signal Oscilloscope of Tektronix have been used to generate the input voltage and to visualize the output voltage, respectively.

Fig. 11 shows the experimental results when a peak input voltage V_{in}, where $0 < V_{in}(V) < 2V$, is applied to the rectifier. $V_{out}(V)$ is the peak output voltage. Fig. 12 shows the experimental results when a peak input voltage V_{in}, where $0 < V_{in}(V) < 500mV$, and Fig. 13 shows the experimental results when a peak input voltage V_{in}, where $0 < V_{in}(V) < 100mV$. The dotted line means a trend average line that show to be very linear.

As Fig. 13 shows, the rectifier works with input voltage as low as 20mV or less, but with a greater loss. In this way, that result enables the proposed rectifier to be used in the application described in Fig. 3 allowing also harvest energy from TEG when very small temperature gradient is present in its faces.

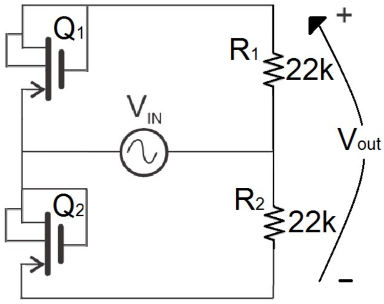


Fig. 10. The Proposed Latour-based Rectifier Topology using diode-connected MOS transistors with interconnected bulk-drain.

V. Conclusions

In this work, a new rectifier topology based on the Latour's detector is introduced. In addition, it was proposed the usage of diode-connected MOS transistors with interconnected bulk-drain to improve the Voltage Conversion efficiency. The experimental results show that the proposed rectifier work with input voltage of about 20mV or lower allowing it to be applied in extremely low-voltage applications.

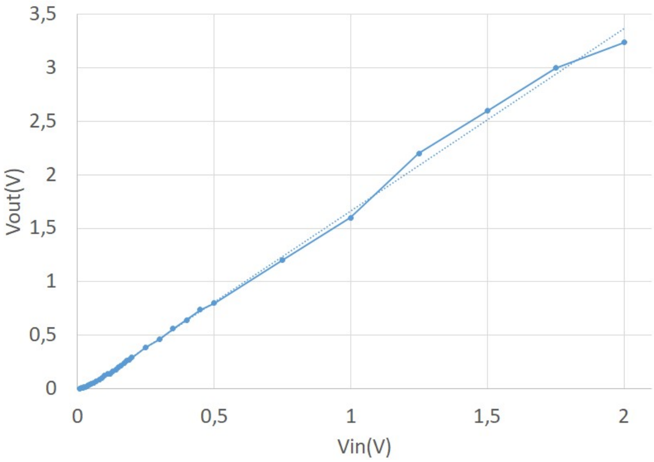


Fig. 11. Experimental results: $V_{out}(V)$ *versus* $V_{in}(V)$: $0 < V_{in}(V) < 2V$.

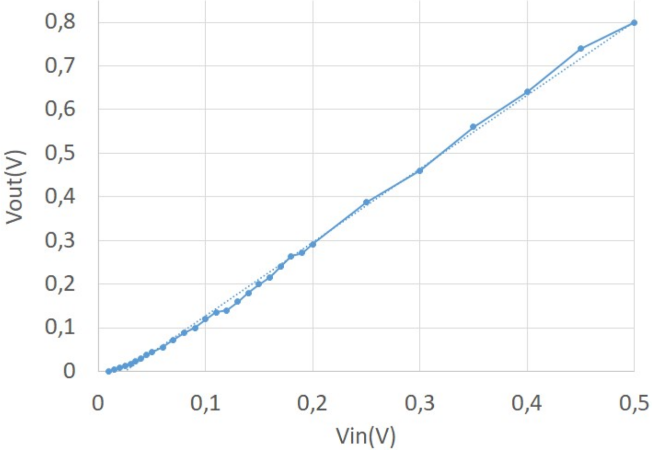


Fig. 12. Experimental results: $V_{out}(V)$ *versus* $V_{in}(V)$: $0 < V_{in}(V) < 500mV$.

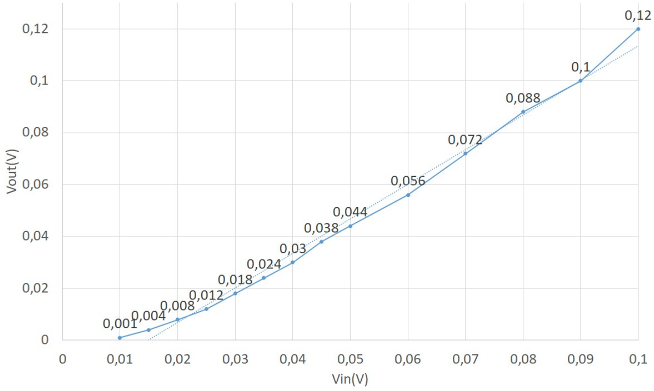


Fig. 13. Experimental results: $V_{out}(V)$ *versus* $V_{in}(V)$: $0 < V_{in}(V) < 100mV$.

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