Curriculum Vitae

STEVO BAILEY

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EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY, Berkeley, CA (UCB) Fall 2012–Present

- Masters of Science in Electrical Engineering and Computer Science, December 2014
- Title: "Modeling Radiation-Induced Soft Errors in Logic and the Overhead of Resiliency Techniques"
- Doctor of Philosophy in Electrical Engineering and Computer Science, in progress
- GPA: 3.95 / 4.00

UNIVERSITY OF VIRGINIA, Charlottesville, VA (UVA) Fall 2008–Spring 2012

- Bachelor of Science in Engineering Science
- Bachelor of Arts in Physics
- Bachelor of Arts in Music
- Minor in Electrical Engineering
- Rodman Scholar, GPA: 3.86 / 4.00

EXPERIENCE AND EMPLOYMENT HISTORY

Graduate Researcher, UCB Fall 2012–Present

- Researching under Professor Bora Nikolic
- Led the tape out of two instances of the Chisel DSP generator methodology, one targeting Radar applications with Northrop Grumman Corporation and Cadence Design Systems, and the other targeting sparse spectrum sensing radio applications, both in May 2017 in TSMC 16nm FinFET
- Designed a DSP coprocessor generator methodology in Chisel, including verification generators, for the DARPA CRAFT project and my final PhD work, available here: https://github.com/ucb-art/craft2-chip
- Assisted in top-level integration and the ASIC design flow perfection of a rapidly-produced RISC-V processor with sparse FFT DSP coprocessor in August 2016 in TSMC 16nm FinFET
- Taped out a new spatial computing architecture with vector unit, thread-level speculation, and dynamic memory allocation for digital signal processing applications in March 2016 in ST 28nm FDSOI
- Led the tape-out of a 10 GHz bandwidth ASIC spectrometer I designed at JPL in Summer 2014, which also included a high-speed 8 lane SerDes, nearly fully digital bang-bang PLL, and new radiation-hardened flip-flop design; taped out December 2015 in ST's 28nm UTB FDSOI process
- Updated and improved Raven 3 with more vector lanes, more test and measurement structures, and a back-bias generator; taped out in November 2014
- Established and perfected the place-and-route flow for Raven 3, a custom RISC-V processor with on-chip DVFS using high-efficiency, unregulated DCDC converters and an adaptive clock generator; taped out in ST's 28nm UTB FDSOI process in August 2013; achieved 26 GFLOPS/W running DGEMM
- Scripted a flow to calculate the energy efficiency and failure rate of numerous soft-error resiliency techniques for arbitrary logic circuits and flip-flop designs; tested on the Raven 3 architecture
- Designed a touch screen capacitance-to-digital converter in a 45nm bulk CMOS PTM
- Designed and synthesized a histogram filter image processor in a 32nm bulk CMOS PTM

- Simulated and characterized the energy efficiency of a manycore processor with dynamic voltage and frequency scaling for each core

Intern, Nvidia Corporation Summer 2015
- Participated in a 13-week research internship in Santa Clara, California
- Joined the Circuits Research Group managed by Tom Gray and mentored by Xi Chen
- Researched the effect of radiation-induced soft errors in integrated circuits

Intern, NASA Jet Propulsion Laboratory Summer 2014
- Participated in the 10-week JPL Summer Internship Program in Pasadena, California
- Designed a 10 GHz bandwidth ASIC spectrometer digital backend, including a polyphase FIR filter bank, FFT, and accumulator, using Chisel, a Berkeley-developed hardware construction language

Graduate Student Instructor, UCB Fall 2013–Spring 2015
- Created weekly homework assignments and exam questions in digital integrated circuits for 40 students
- Prepared and lectured at weekly discussion sections, held weekly office hours for student help, proctored exams, and mentored students in Cadence software for lab assignments and a CORDIC design project
- Mentored eight remote working professionals online for Berkeley's MAS-IC program in two separate classes
- Created and graded weekly assignments for 23 students in advanced digital integrated circuits class
- Gave two lectures, created exam questions, and mentored students on individual projects

Researcher, UVA Summer 2011
- Researched as an undergrad with Professor Mircea Stan and graduate students
- Investigated an integrated circuit modular adder design with error detection and correction
- Continued the work unpaid in my fourth year and published a paper at ISCAS, an IEEE conference

Intern, Virginia Microelectronics Consortium, Newport News, VA Summer 2010
- Researched with Old Dominion University professors at Jefferson Lab for 12 weeks
- Experimented with Atomic Layer Deposition, Scanning Electron Microscopy, solar cells, and phosphors

Factory Assistant, Xymid, LLC, Richmond, VA August 2009
- Prepared and packaged fabric rolls at a textile company managed by previous DuPont employees
- Cleaned textile machines including a loom covered in carbon and a press that had to be food-grade clean
- Organized over 100 boxes of files and moved them to storage

Math Grader, Department of Applied Mathematics, UVA Spring 2009
- Graded weekly differential equations homework for 45 students over 14 weeks
- Collected and organized homework and recorded grades for the professor

Server, Bruster's Real Ice Cream, Midlothian, VA Summer 2008
- Prepared and served ice cream to customers for 4 months
- Thoroughly cleaned and restocked the entire store daily

PUBLICATIONS

Bailey, S., Wright, J., Mehta, N., Hochman, R., Jarnot, R., Milovanović, V., Werthimer, D., and Nikolić, B., "A 28nm FDSOI 8192-Point Digital ASIC Spectrometer from a Chisel Generator," IEEE Custom Integrated Circuits Conference (CICC), April 2018.

Wang, A., Richards, B., Dabbelt, P., Mao, H., Bailey, S., Jaeduk, H., Chang, E., Dunn, J., Alon, E., and Nikolić, B., "A 0.37mm^2 LTE/Wi-Fi compatible, memory-based, runtime-reconfigurable $2^n3^m5^k$ FFT accelerator integrated with a RISC-V core in 16nm FinFET," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 305-308, November 2017.

Keller, B., Cochet, M., Zimmer, B., Kwak, J., Puggelli, A., Lee, Y., Blagojević, M., Bailey, S., Chiu, P.-F., Dabbelt, P., Schmidt, C., Alon, E., Asanović, K., and Nikolić, B. "A RISC-V Processor SoC With Integrated Power Management at Submicrosecond Timescales in 28 nm FD-SOI," IEEE Journal of Solid-State Circuits (JSSC), vol. 52, no. 7, pp. 1863-1875, May 2017.

Keller, B., Cochet, M., Zimmer, B., Lee, Y., Blagojević, M., Kwak, J., Puggelli, A., Bailey, S., Chiu, P.-F., Dabbelt, P., Schmidt, C., Alon, E., Asanović, K., and Nikolić, B. "Sub-microsecond adaptive voltage scaling in a 28nm FD-SOI processor SoC," ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne, pp. 269-272, September 2016.

Zimmer, B., Lee, Y., Puggelli, A., Kwak, J., Jevtić, R., Keller, B., Bailey, S., Blagojević, M., Chiu, P.-F., Le, H.-P., Chen, P.-H., Sutardja, N., Avizienis, R., Waterman, A., Richards, B., Flatresse, P., Alon, E., Asanović, K., and Nikolić, B. "A RISC-V Vector Processor With Simultaneous-Switching Switched-Capacitor DC–DC Converters in 28 nm FDSOI," IEEE Journal of Solid State Circuits (JSSC), vol. 51, no. 4, pp. 930-942, April 2016.

Lee, Y., Waterman, A., Cook, H., Zimmer, B., Keller, B., Puggelli, A., Kwak, J., Jevtić, R., Bailey, A., Blagojević, M., Chiu, P.-F., Avizieni, R., Richards, B., Bachrach, J., Patterson, D., Alon, E., Nikolić, B., and Asanović, K. "An Agile Approach to Building RISC-V Microprocessors," IEEE Micro, pp. 8-20, March 2016.

Lee, Y., Zimmer, B., Waterman, A., Puggelli, A., Kwak, J., Jevtić, R., Keller, B., Bailey, S., Blagojević, M., Chiu, P.-F., Cook, H., Avizienis, R., Richards, B., Alon, E., Nikolić, B., and Asanović, K. "Raven: A 28nm RISC-V vector processor with integrated switched-capacitor DC-DC converters and adaptive clocking," 2015 IEEE Hot Chips 27 Symposium (HCS), Cupertino, CA, 2015, pp. 1-45, August 2015.

Zimmer, B., Lee, Y., Puggelli, A., Kwak, J., Jevtić, R., Keller, B., Bailey, S., Blagojević, M., Chiu, P.-F., Le, H.-P., Chen, P.-H., Sutardja, N., Avizienis, R., Waterman, A., Richards, B., Flatresse, P., Alon, E., Asanović, K., and Nikolić, B., "A RISC-V vector processor with tightly-integrated switched-capacitor DC-DC converters in 28nm FDSOI," 2015 Symposium on VLSI Circuits (VLSI Circuits), pp. C316-C317, June 2015.

Jevtić, R., Le, H.-P., Blagojević, M., Bailey, S., Asanović, K., Alon, E., and Nikolić, B., "Per-core DVFS with switched-capacitor converters for energy efficiency in manycore processors," IEEE Transaction on Very Large Scale Integration Systems (TVLSI), vol. PP, no. 99, May 2014.

Bailey, S. and Stan, M., "A new taxonomy for reconfigurable prefix adders," IEEE International Symposium on Circuits and Systems (ISCAS), May 2012. [Student Best Paper Award finalist]

AWARDS AND HONORS

Best Student Poster, BWRC retreat, UCB — Summer 2017
Electrical Engineering and Computer Sciences Departmental Fellowship, UCB — Fall 2012–Spring 2013
Best Individual Project Presentation at UVA's Spring Engineering Science Symposium — Spring 2012
Dean's List, UVA — Fall 2008–Spring 2012
ASM Eastern Virginia Scholarship — Fall 2008–Spring 2012
McIntire Department of Music's Departmental Recognition for excellent and imaginative work — Fall 2011

Academic Intermediate Honors, UVA Fall 2010

ACTIVITIES AND LEADERSHIP POSITIONS

***Instructor*,** Generator Bootcamps, Berkeley and San Jose, CA Fall 2017

- Designed a suite of instructive tutorials on Chisel and our Craft digital design generator methodology
- Led two bootcamps on this material, one at UC Berkeley and the other at Cadence Design Systems

Webmaster and Media Chair, Engineers Without Borders, UCB Fall 2016–Spring 2017

- Webmaster for EWB at Berkeley
- Kept the website up-to-date
- Designed flyers, announcements, and a t-shirt using Adobe Photoshop

Peru Team Lead, Engineers Without Borders, UCB Spring 2016–Spring 2017

- Attended weekly meetings discussing our rainwater catchment (RWC) projects in Peru, designed to provide clean, arsenic-free sources of water to schools in the Puno region
- Took CPR and First Aid classes to become the travel team's Health and Safety Officer
- Traveled to Peru, conducted monitoring and evaluation on previous RWC implementations, tested extant well water and RWC water for arsenic, took pre-implementation measurements for a new RWC system, and discussed a new agreement with members of Suma Marka (local NGO), the local health system, the local university, and the local community
- Led the documentation team to design and document a new RWC system and implementation trip slated for August 2017

Volunteer, Alta Bates Summit Medical Center, Berkeley, CA Spring 2016–Fall 2016

- Served customers and restocked the gift shops at Ashby and Herrick campuses, totaling 100 hours
- Volunteered for Nursing Unit 8, Cardiology, restocking PPE and visiting patients, totaling 100 hours

Exhibitor, DARPA Demo Day, The Pentagon, Arlington, VA May 2016

- Demonstrated our Raven chip running a neural network classifying CIFAR10 images at sub 1 W power
- Presented a poster detailing our work on PERFECT, reducing the power of computation for UAVs

Student, Synopsys, Inc., Mountain View, CA September 2013

- Attended a two day lecture series on Synopsys PrimeTime Signal Integrity and constraint debugging

Lecturer, IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, South Korea May 2012

- Gave a 20 minute professional lecture on my publication at the conference
- Presented my poster after being selected as a finalist for the Student Best Paper Award

Treasurer, Tau Beta Pi Engineering Honor Society, Virginia Alpha Chapter Fall 2010–Spring 2012

- Managed finances for UVA's Tau Beta Pi honor society, which inducts over 60 new members each year
- Attended a two-day conference at George Washington University to network with 17 other chapters

Volunteer, Ronald McDonald House, Charlottesville, VA Fall 2010–Fall 2011

- Bought and prepared food for the local Charlottesville Ronald McDonald House, a refuge for families with seriously ill children

Volunteer, Hoos for Haiti, Charlottesville, VA Fall 2010

- Washed and folded clothes collected for donation to victims of the Haiti earthquakes

Bassist, Jazz Chamber Ensemble, UVA Fall 2009–Spring 2010

- Played the electric bass for a 6-member jazz chamber ensemble group

Student, Engineering in a Global Context, Stuttgart, Germany Summer 2009

- Attended presentations at 12 different locations including German engineering companies, universities, and museums to hear speakers and ask questions related to research topic
- Researched and wrote a 10 page paper comparing German and American sustainability

Webmaster, American Institute for Aeronautics and Astronautics Club, UVA Fall 2008–Spring 2010

- Completely redesigned and managed the website for the aerospace engineering club at UVA

SKILLS

- Programming: Java, Perl, Python, Bash, Verilog, Chisel, Scala, TCL, MATLAB, LaTeX, HTML, CSS
- Computer Skills: Linux, Cadence CAD tools (Virtuoso, Genus, Innovus), Synopsys CAD tools (Design Compiler, IC Compiler, Milkyway), Mentor CAD tools (Calibre), Git, Microsoft Office, VIM

RELEVANT COURSEWORK

Completed Courses (UVA)

ECE 2066 (Science of Information)	A
ECE 2330 (Digital Logic Design)	A+
ECE 2630 (Introductory Circuit Analysis)	A+
ECE 2660 (Electronics I)	A
ECE 3103 (Solid State Devices)	A
ECE 3209 (Electromagnetic Fields)	A+
ECE 3330 (Computer Architecture)	A+
ECE 3632 (Electronics II)	A
ECE 3663 (Digital Integrated Circuits)	A+
ECE 3750 (Signals and Systems I)	A
ECE 4332 (Introduction to VLSI Design)	A+
ECE 4502 (Mixed-Signal Integrated Circuits)	A
ECE 6502 (ASIC/SOC VLSI Design)	A
MSE 2090 (Introduction to Materials Science)	A

Completed Courses (UCB)

EE 140 (Linear Integrated Circuits)	A
CS 250 (VLSI Systems Design)	A
EE 240 (Advanced Integrated Circuit Design and Analysis)	A-
EE 241 (Advanced Digital Integrated Circuits)	A
EE 244 (Algorithms for System Modeling, Analysis, and Optimization)	A+
PHYS 110A (Electromagnetism and Optics)	A
EE 290C (VLSI Signal Processing)	A
ASTRO 121 (Radio Astronomy Lab)	A
ASTRO C162 (Planetary Astrophysics)	A+
MBA 209F (Fundamentals of Business)	A-