Project UPSET

Understanding and Protecting against Single Event Transients

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Outline

Motivation

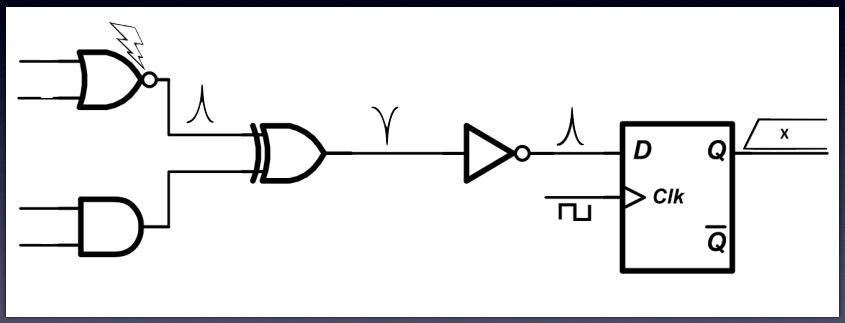
Background

Design & Implementation

Results

Conclusion

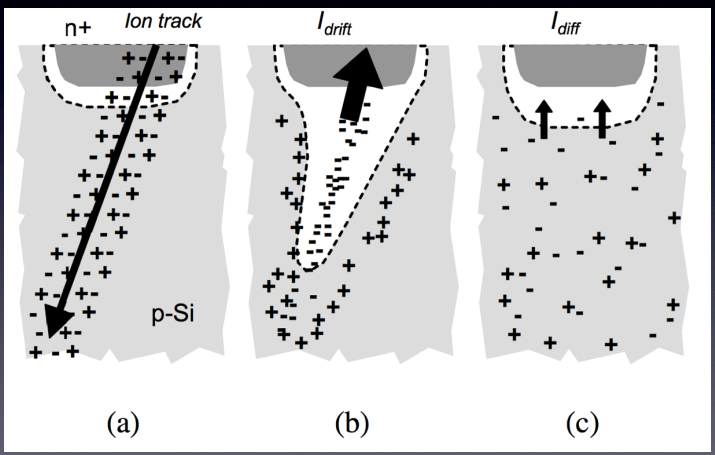
Single Event Transients



Problem Statement

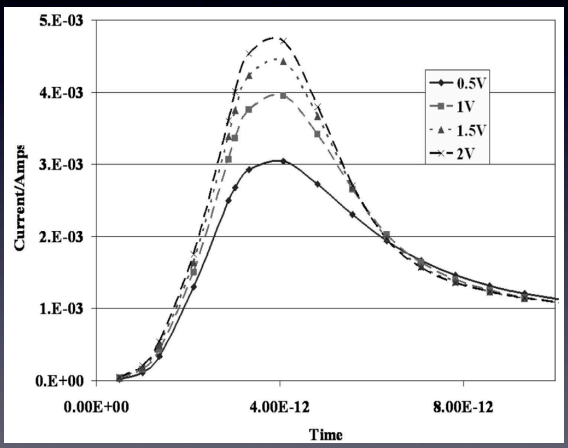
- Are certain circuits more or less vulnerable than others?
- Can this vulnerability be correlated with circuit parameters?

Modeling



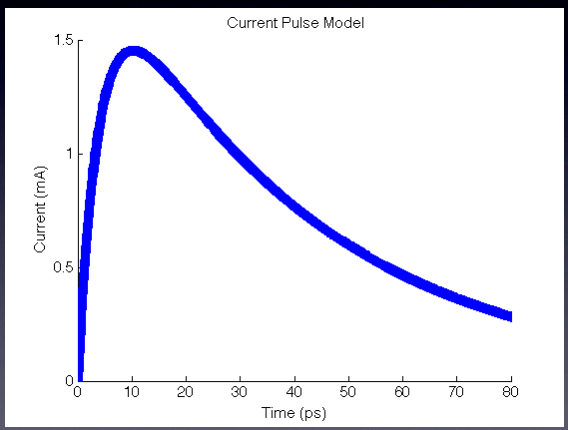
Seifert, FTEDA 2010

Modeling

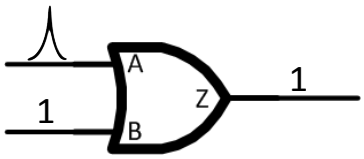


Ramanarayanan, DSC 2009

Modeling

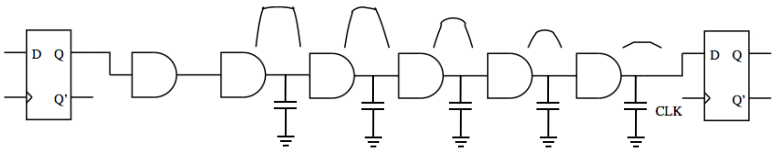


Logical Masking

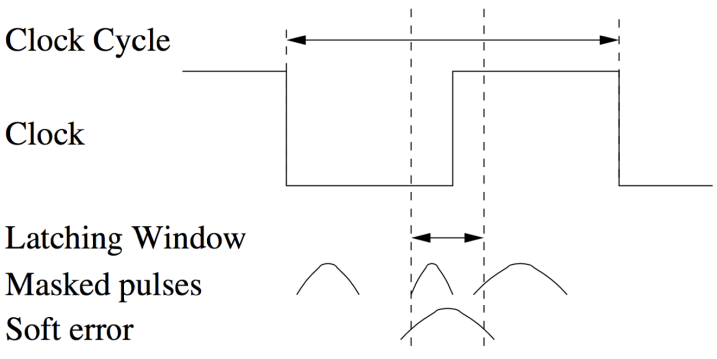


A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

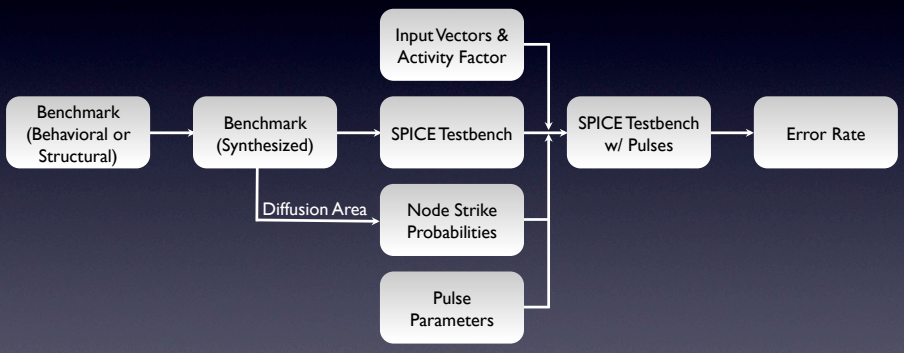
Electrical Masking



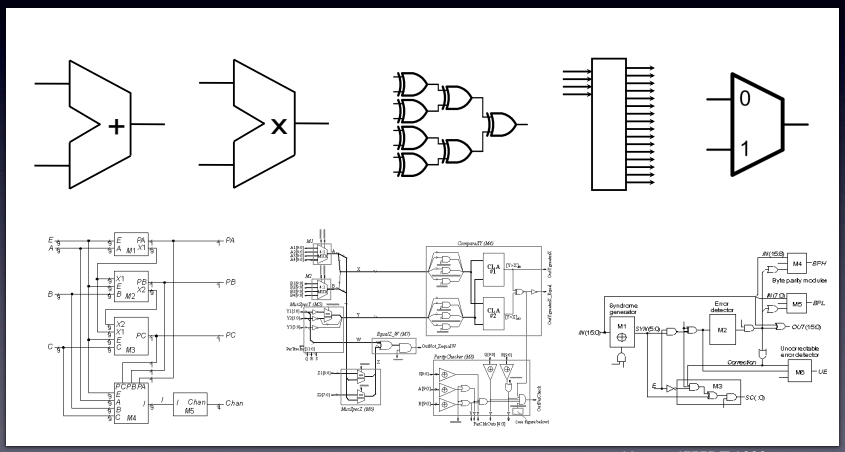
Latching Window Masking



Our Flow: Overview



Our Flow: Benchmarks



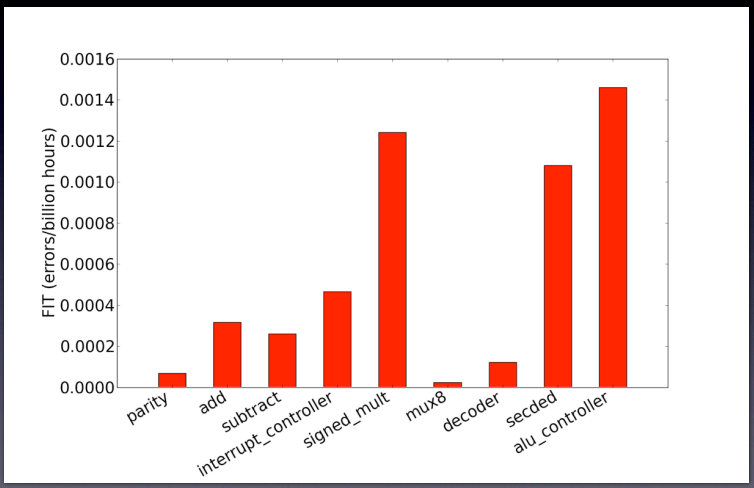
Hansen, IEEEDT 1999

Our Flow: FIT Calculation

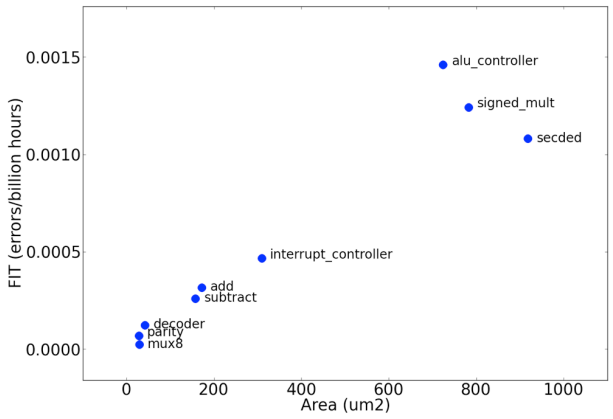
FIT (Failures In Time):
Number of Failures
in 10^9 hours

Flux
× Area
× Diffusion Derating
× Upsets/Strike
FIT

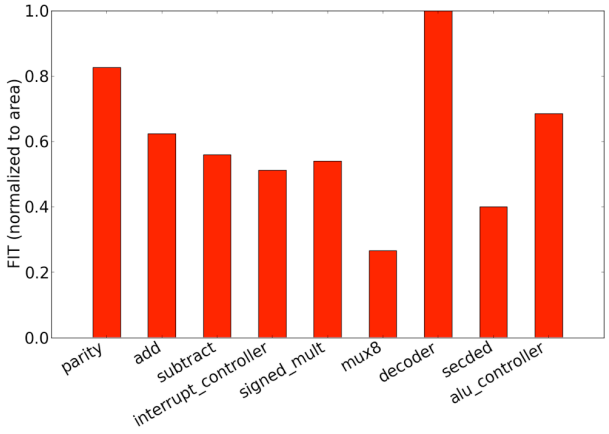
Results



Results



Results



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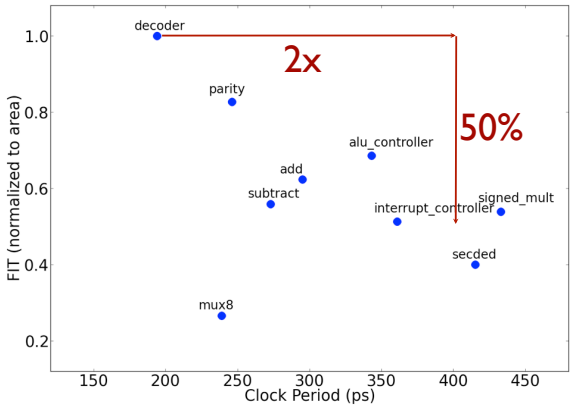
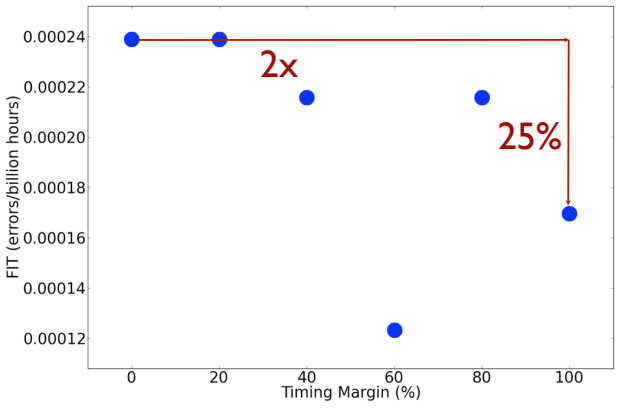
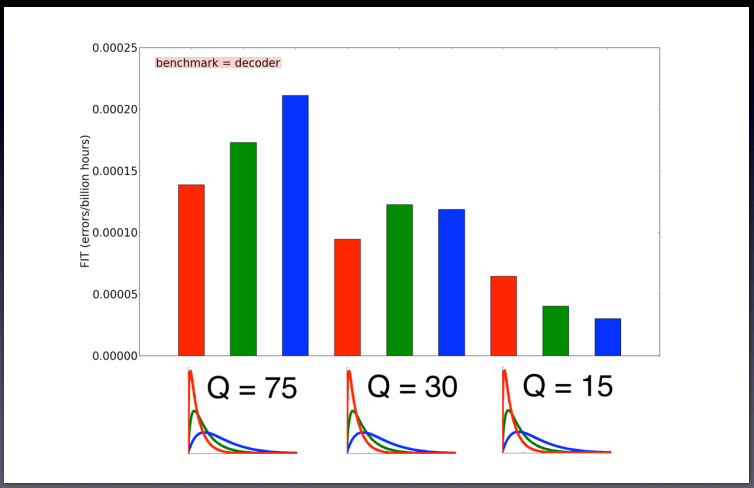


Results



Results



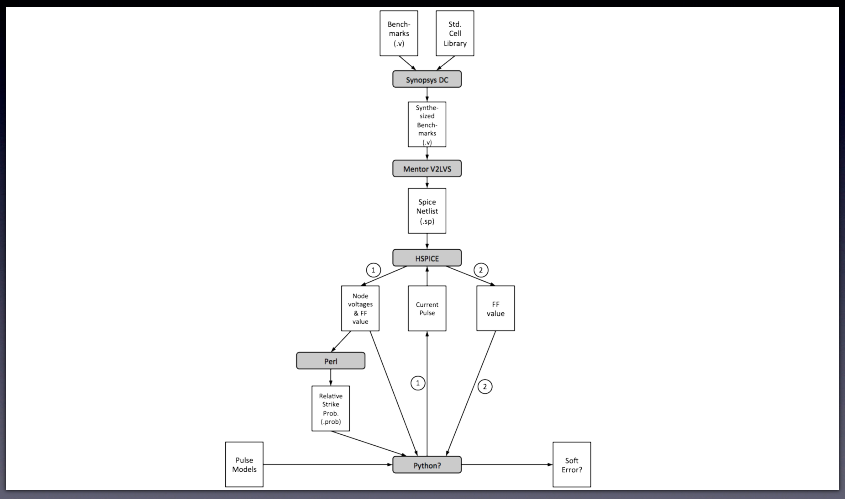
Conclusion

- Datapath FIT rate due to SETs depends on:
  - Area
  - Logical Depth
- Adding logic is more effective than adding margin to reduce FIT rate
- Future work could accurately characterize pulse models at the device level

References

- N. Seifert, “Radiation-induced soft errors: A chip-level modeling perspective,” Foundations and Trends in Electronic Design Automation, vol. 4, no. 2-3, pp. 99–221, 2010.
- R. Ramanarayanan, et al., “Modeling soft errors at the device and logic levels for combinational circuits,” Dependable and Secure Computing, pp. 202–216, 2009.
- P. Shivakumar, et al., “Modeling the effect of technology trends on the soft error rate of combinational logic.” Dependable Systems and Networks, pp. 389–398, 2002.
- M. Hansen, H. Yalcin, and J. P. Hayes, "Unveiling the ISCAS-85 Benchmarks: A Case Study in Reverse Engineering," IEEE Design and Test, vol. 16, no. 3, pp. 72-80. 1999.

Backup



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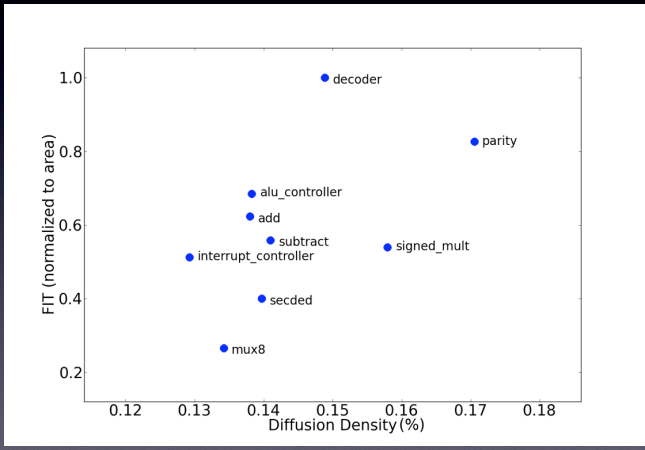

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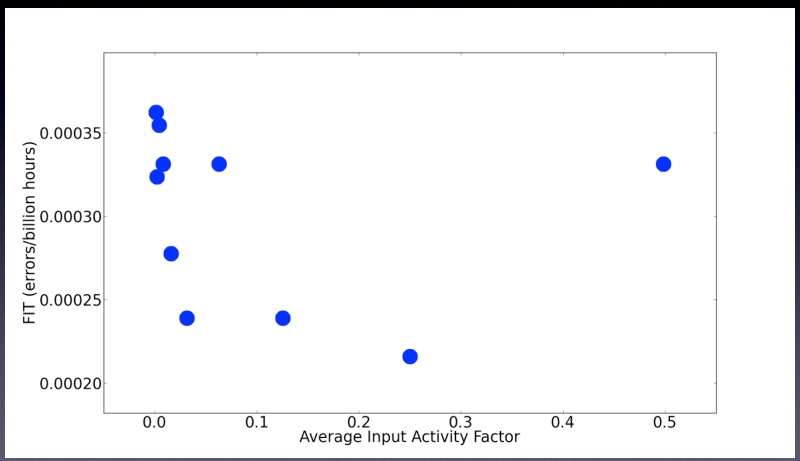

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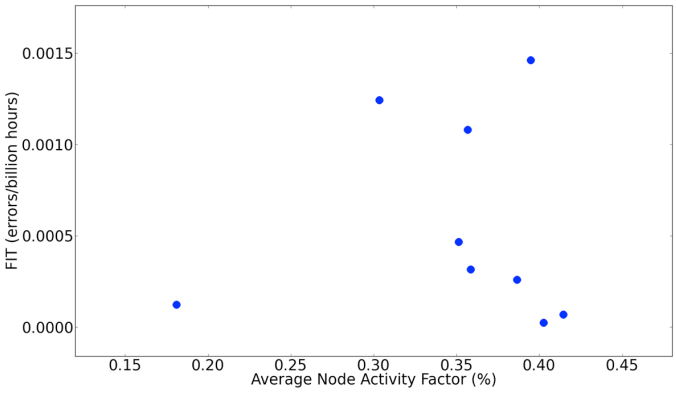

Backup