SLATE: A Combined Architecture for LDPC and Turbo Decoding

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EE290C Final Project

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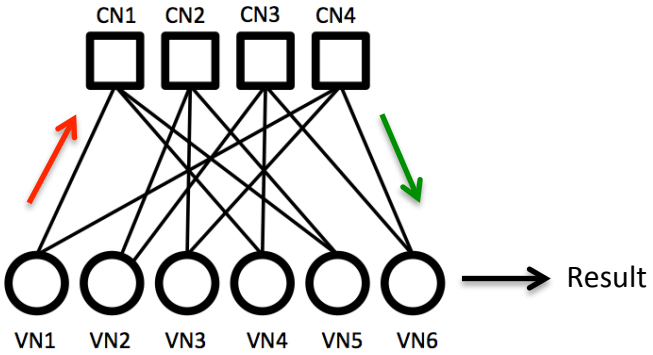
Outline

- LDPC Overview
- Turbo Overview
- Common Elements
- Combined Architecture
- Results
- Conclusions

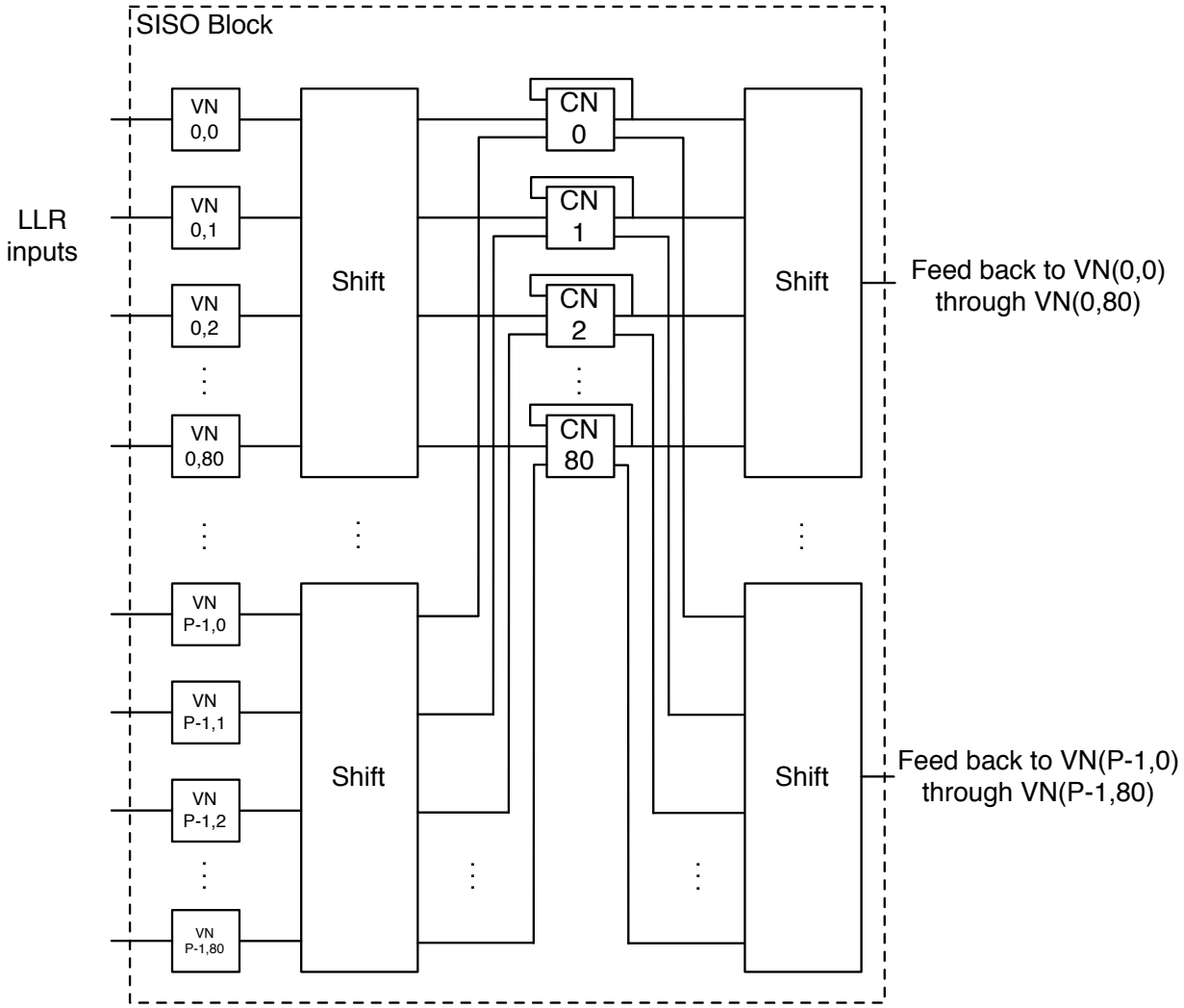
LDPC Decoding

1. Load LLR values into variable nodes, send to check nodes
2. Repeat:
   - Variable nodes marginalize, accumulate
   - Check nodes compute offset-min
   - Compute hard variable node result, use to compute syndrome, loop if desired metric not met

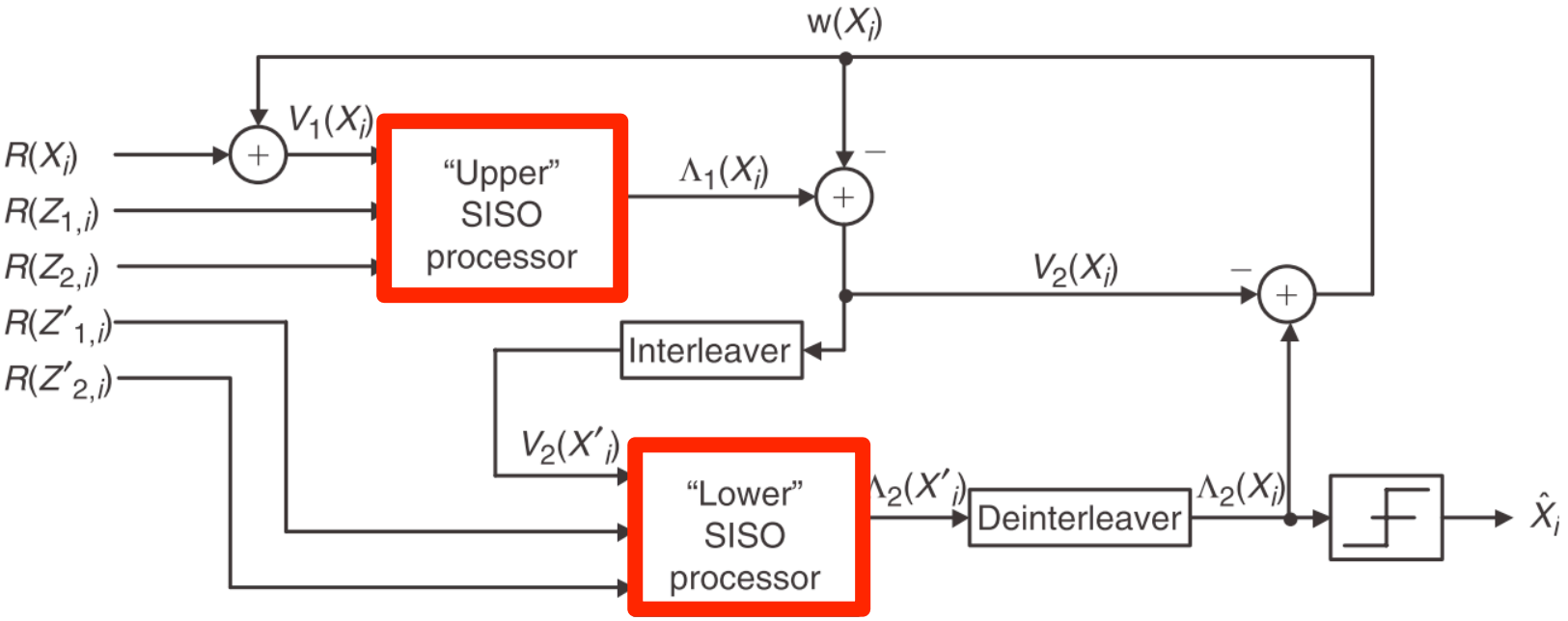


Source: Matt Weiner

LDPC Decoding

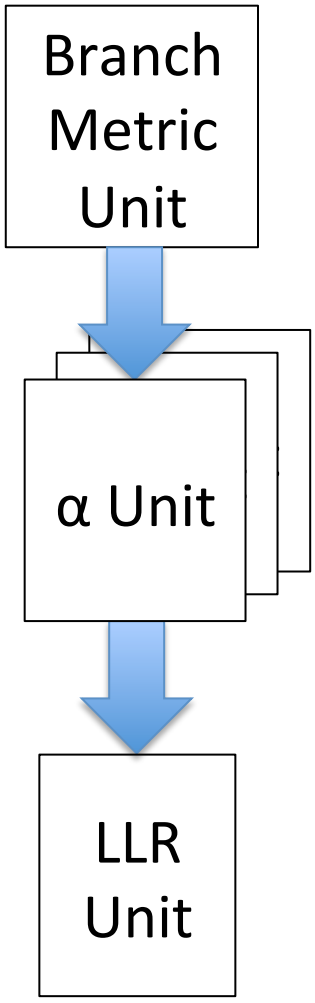


Turbo Decoding



Source: Valenti and Sun, *Handbook of RF and Wireless Technologies*

SISO Block



$$\gamma_1 = y_a$$

$$\gamma_2 = c_c$$

$$\gamma_3 = y_a + c_c$$

$$\alpha_k = \max^*(\alpha_{k-1,0} + \lambda_{k,0}, \alpha_{k-1,1} + \lambda_{k,1})$$

Calculate alphas, betas, and "dummy betas" in parallel for each window.

γ_k = [max* reduction of 1 transitions] –
[max* reduction of 0 transitions]

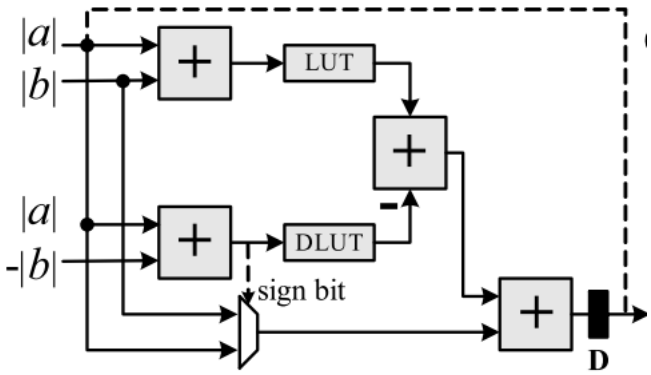
Uncommon Elements

- Routing
  - LDPC: Cyclic shifts of 27, 54, 81
  - Turbo: Permutation depends on block size
- Memories for intermediate results
  - LDPC: many small memories for v2c and c2v marginalization
  - Turbo: a few small memories as scratchpads within each window

Common Elements

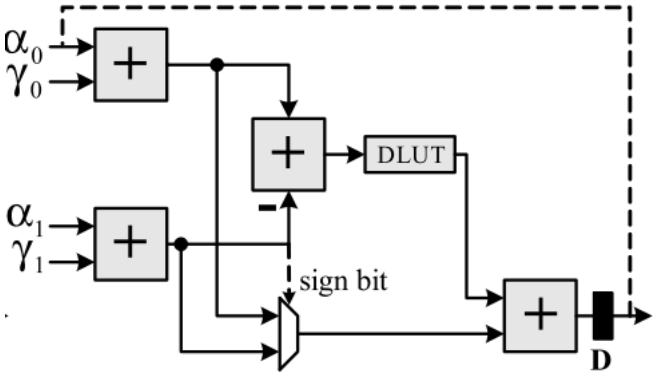
LDPC: Offset-min

[min1,min2] = min(a,b,c) + offset



Turbo: max*

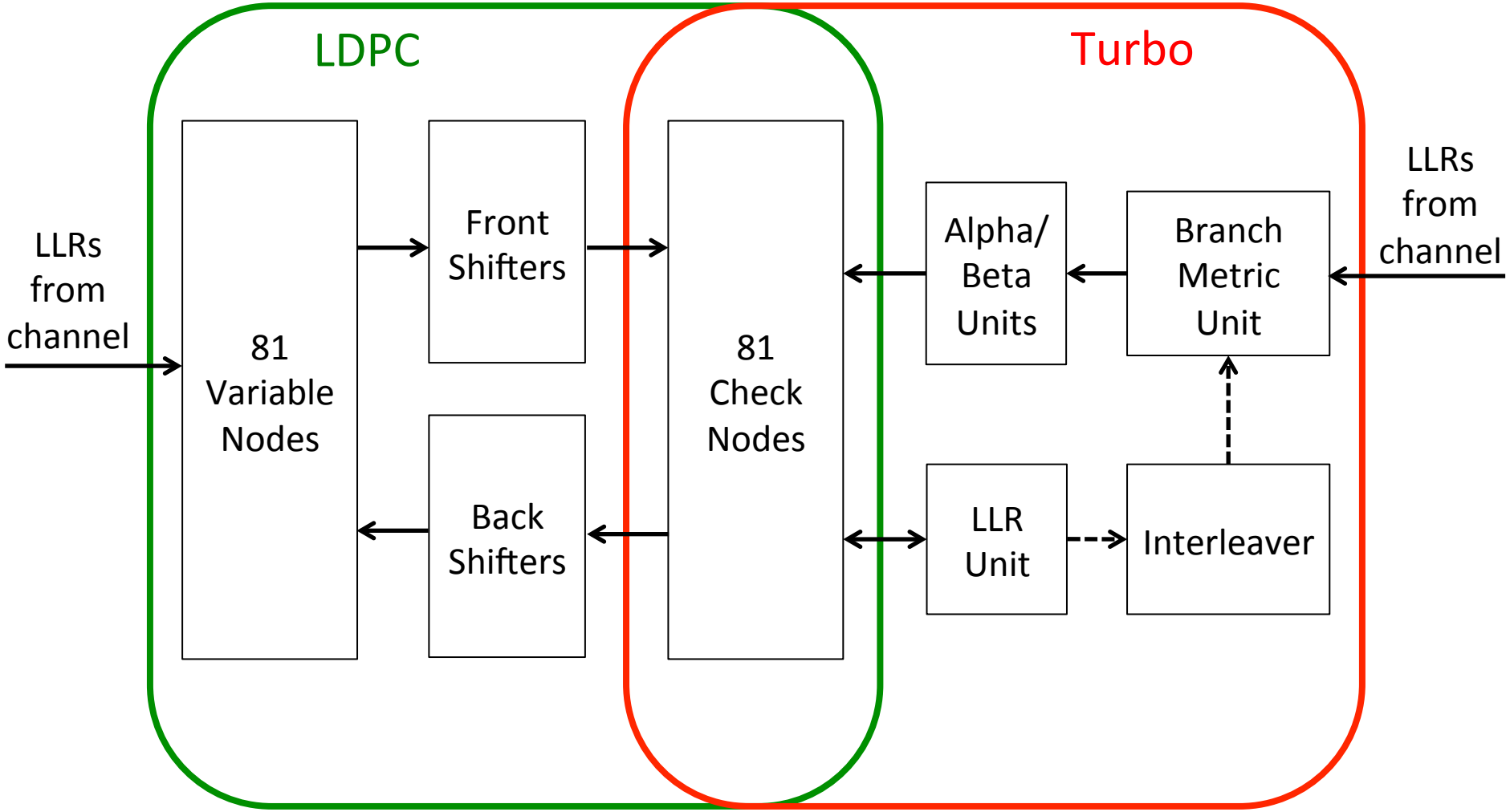
max* = max(a,b) + offset



Combine these and share the check nodes!

Source: Sun and Cavallero, “Unified Decoder Architecture for LDPC and Turbo Codes”

System Block Diagram



Sharing the Check Nodes

- LDPC
  - 81 3-input min-offset blocks
- Turbo
  - 8 2-input max* for alpha/beta calculations (3x)
  - 14 2-input max* per window for LLR calculations
  - Total: 38 2-input max* per window
  - 81 4-input min/max* => 4 parallel windows

Results: Throughput

- Clock period = 1.8ns (unpipelined)
  - Critical path: VN -> shifter -> CN
  - Should be much improved with pipelining
- LDPC throughput: 960 Mb/s
  - Block length: 1944, 10 iterations, 6 bits per LLR
- Turbo throughput (estimated): 384 Mb/s
  - Block length: 6144, 10 iterations, 2Ghz clock

LDPC Results: Area

LDPC Component	Synthesized Area (um^2)
Back Shifters	16,800
Check Nodes	18,800
Front Shifters	18,600
Schedule	9,500
Variable Nodes	570,000
Combinational	228,000
Registers	342,000
	Total: 0.64 mm^2

LDPC Results: Energy

- Clock period = 1.8ns (unpipelined)
- Energy = 0.28 nJ/b post-synthesis
  - Block length: 1944, 10 iterations, 6 bits per LLR

Project Progress

- Completed:
  - Tested MATLAB implementations
  - Built and tested most functional blocks
  - Synthesized full LDPC design
- Still to do:
  - Improve pipelining and variable node design
  - Integrate and test top-level design
  - Place-and-route design for realistic area numbers

Future Work

- Increase throughput
  - More VNGs: do part or all of a row at once
  - More parallel turbo decoding windows
  - Higher radix turbo decoding
- Reduce memory footprint of LDPC
- Fuller LDPC/turbo resource sharing
  - Share variable node arithmetic blocks
  - Share scratch memory

References

- Y. Sun and J. Cavallaro. “Unified Decoder Architecture for LDPC/Turbo Codes.”
- M. Valenti and J. Sun. *Handbook of RF and Wireless Technologies*, Chapter 12.
- Y. Sun, J. Cavallaro, et al. “Configurable and Scalable Turbo Decoder for 4G Wireless Receivers.”
- M. Weiner. “A High-Throughput, Flexible LDPC Decoder for Multi-Gb/s Wireless Personal Area Networks.”

Thanks to Bora, Matt, and Sriram for fruitful discussions.