Soft Errors in Datapaths, or Project UPSET (Understanding and Protecting against Single Event Transients)

Garen Der-Khachadourian, Stevo Bailey, and Ben Keller

Project Summary

Modern power-constrained microprocessors reduce the operating voltage as much as possible to save energy. However, nanoscale devices operating at low voltages are vulnerable to soft errors caused by background radiation. Single event transients result in a voltage pulse at a particular node, which can propagate through logic and, in the worst case, cause an undetectable error in operation. To guard against this possibility, operating voltages are increased by some additional margin. This project will explore appropriate models and circuit techniques to guard against soft errors in logic while reducing or eliminating this margin, allowing for reduced operating power.

We propose three main phases of the project.

Phase 1: Review existing literature on soft errors to adopt or develop an appropriate model of single event transients.

Phase 2: Apply this model to simulated combinational circuits to determine the effects of single event transients on logic.

Phase 3: Design or adopt circuits to guard against single event transients, and determine the design tradeoffs in such circuit techniques (e.g., increased area against reduced margin).

References

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