Project UPSET: Understanding and Protecting Against Single Event Transients

Stevo Bailey
stevo.bailey@eecs.berkeley.edu

Ben Keller
bkeller@eecs.berkeley.edu

Garen Der-Khachadourian
gdd9@berkeley.edu

***Abstract*—A particle strike can result in a single-event transient (SET) at a node in circuit logic, which may cause incorrect operation. While prior work describes and models the nature and effect of SETs, existing approaches address different aspects of the circuit-level failures-in-time (FIT) rate calculation individually. We used comprehensive simulations to identify key determinants of circuit-level soft error rates (SER). Simple circuits were synthesized and simulated using Synopsys Design Compiler, HSPICE, and custom scripts. The results indicate that datapath SER may be a function of simple circuit parameters such as area, logic depth, and diffusion density.**

I. Introduction

Modern digital circuits must demonstrate resiliency in the face of process, voltage, and temperature variations. Radiation strikes pose a particular resiliency challenge, as they do not represent a marginal variation, but rather a transient and unpredictable event. This project characterizes the vulnerability of circuits to soft errors, so that resiliency can be improved while avoiding unnecessary overhead and margin.

A high-energy particle striking a circuit node results in a voltage pulse known as a single-event transient, or SET. An accurate model uses device characteristics to determine the probability that a certain particle will strike a node and the nature of the pulse produced at that node. Circuit-level models characterize the propagation of the voltage pulse through combinational logic and into a latch or flip-flop. Additionally, architectural models can describe the effect of an incorrect flip-flop value on the system. This hierarchical model combines to determine a failure rate for the entire system, often reported as failures in time (FIT), or number of failures per 10^9 hours. Our work builds on prior work in modeling device-level parameters to describe a comprehensive circuit-level model for determining FIT rates of combinational blocks.

II. Background and Prior Work

Radiation striking a chip typically originates from cosmic rays interacting with atmospheric particles or from radioactive isotopes on the chip's packaging [1]. When these neutrons or alpha particles strike a junction, they generate electron-hole pairs. The electron-hole pairs drift and diffuse at the junction, creating a current. However, the generated electron-hole pairs are quickly used up, so the current simply pulses for a short time [2]. This current charges or discharges the struck node, producing a SET which propagates through the logic until it reaches a latch or flip-flop. If the storage element latches the pulse instead of the correct data, the microarchitectural state is corrupted and a single-event upset (SEU) occurs [1]. In this section, we present a brief overview of prior work in device and circuit characterization of SETs.

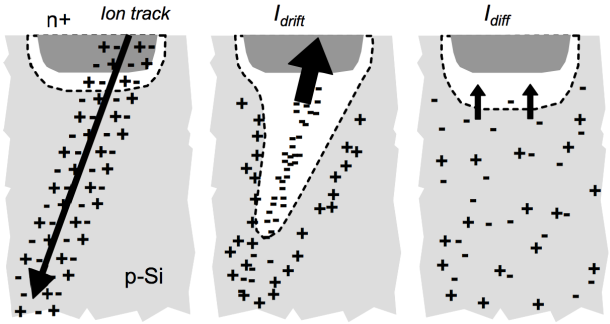


Fig. 1. Charge generation and collection at a junction [1].

A. Device-Level Modeling

Modeling SETs at the device level can be considered in three parts. The first part must describe the frequency of various types of radiation strikes. The next must describe the amount of charge imparted by each strike. The third part should detail the nature of the current pulse resulting from this charge.

When a particle strikes a junction, it produces a funnel of electron-hole pairs, as seen in Figure 1. These electron-hole pairs drift and diffuse, causing a current pulse. Initially, the electric field inherent in reverse-biased junctions separates the charges, spiking the current. Any remaining carriers then diffuse, creating a long tail current in the current pulse.

Many pulse models use a double exponential equation to model the fast spike and slow fall of the current pulse [3]:

$$I(t) = \frac{Q_{coll}}{\tau_a - \tau_b}\left(e^{\frac{-t}{\tau_a}} - e^{\frac{-t}{\tau_b}}\right), \quad (1)$$

where Q_{coll} is the total collected charge, and τ_a and τ_b are time constants. All three of these parameters depend on the technology, voltage, circuit, temperature, and particle energy, so each must be characterized for the particular application and operating condition. Figure 2 shows sample current pulses in a 130nm bulk CMOS process.

Much prior work has modeled current pulses in various technologies [4] [5] [6]. Because we lack process-specific information, we use these models to determine the size and

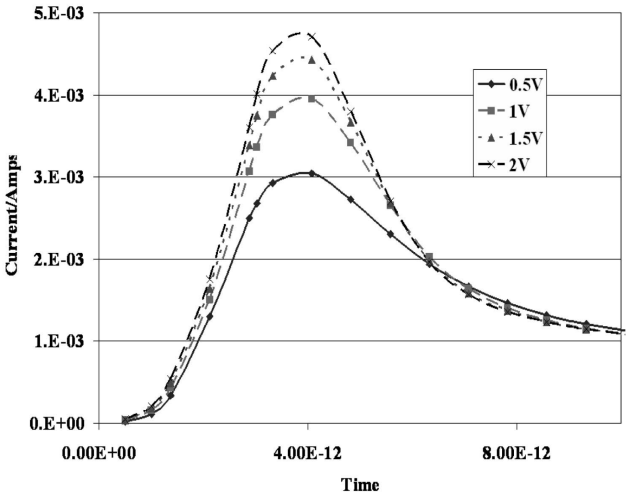


Fig. 2. Measured radiation current pulse waveforms [2]. Note the fast rise time and slow fall time of the current pulse.

duration of representative current pulses for our circuit-level model.

B. Circuit-Level Modeling

After a particle strike generates a current pulse at a node, a transient voltage pulse propagates through the combinational logic paths following that node. The effects of this pulse in logic are mitigated by three distinct masking effects.

1) **Logical Masking:** A pulse is logically masked if it does not affect the output of a gate. For example, a NOR gate with one high input masks any changes on the other input, including SETs.
2) **Electrical Masking:** A gate's intrinsic electrical properties dampen the transient pulse's magnitude as it propagates down a logic path.
3) **Latching Window Masking:** A transient pulse in a combinational block only affects the microarchitectural state if the pulse occurs on an input to a sequential logic cell when it is latching the data. If a pulse reaches a sequential boundary and dissipates before or after the sampling window, the pulse is masked and does not affect the recorded output of the combinational block.

Modeling these effects can be computationally expensive since each effect is data-dependent, and cannot be deduced based on topology alone. Several prior techniques attempted to reduce the amount of computation [4] [7] [8]. These approaches systematically address each masking effect, reducing simulation time at a potential cost to accuracy. A detailed circuit simulation tool such as HSPICE can accurately model all three masking effects but requires a long runtime.

Note that higher levels of abstraction, such as the architectural state, operating system, and software, further mask errors that are realized at the microarchitectural level because not every upset register necessarily translates into incorrect program execution [9] [10]. Such higher-level considerations are beyond the scope of the project.

III. Methodology

Rather than employing simplifying models to describe the circuit-level effects of SETs, we use HSPICE simulations to capture results as accurately as possible. By injecting current pulses in SPICE simulations for several circuit benchmarks and determining the correctness and error rates at the registered outputs, the FIT rate of various combinational circuits can be determined.

A. Overview

Figure 3 illustrates the steps performed to determine FIT rates. Circuit designs described in an HDL are inputs to the flow. These circuits are synthesized into a gate-level netlist using a standard cell library. The synthesized HDL netlist is then translated into a SPICE netlist, which is simulated to determine correct circuit operation. Next, current pulses are injected at random times within a clock period and random locations within the circuit. The probability of a node being struck is found based on the amount of diffusion tied to that node. Finally, a second HSPICE simulation is performed and the results are used to determine if errors have occurred.

B. Benchmark Circuits

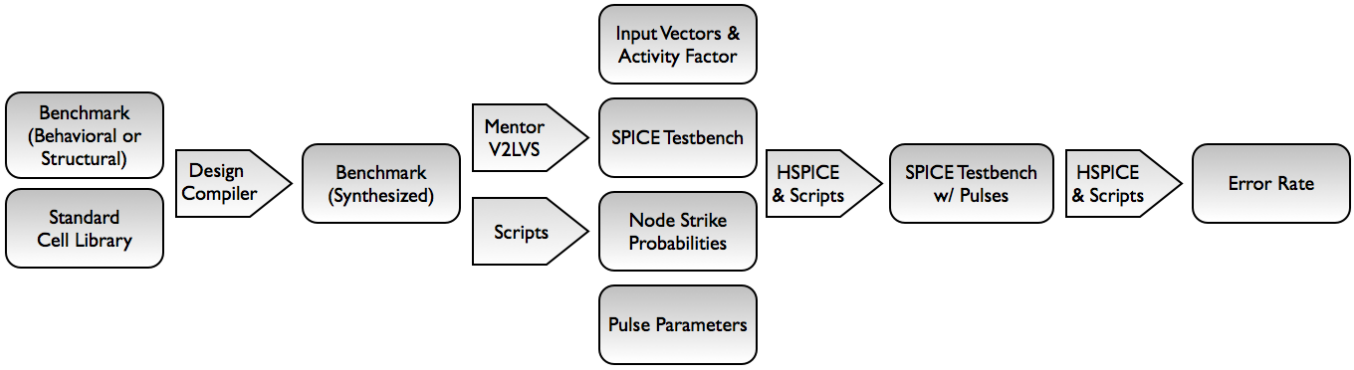
We selected a variety of combinational circuits in an attempt to expose any differences in the response of combinational logic to SETs. Several simple combinational blocks were written in behavioral HDL, including 8-bit arithmetic blocks, an 8:1 multiplexer, and a 16:4 decoder. In addition, several circuits from the ISCAS '85 benchmark set [11] were used to add to the diversity of our benchmark circuits in terms of functionality and logic depth. These types of combinational blocks are commonly found in many designs.

Input and output registers were added to the input and output nodes of each combinational block. In real integrated circuits, an error occurs if a node is struck and the altered datum is latched by a storage element. Thus, the output registers ensure accurate simulation of latching window masking and indicate whether faulty data are stored as a result of a single event transient. The input registers ensure that the input data are realistically shaped as they enter the circuit.

C. Circuit Synthesis

Behavioral Verilog descriptions of benchmark circuits must be converted into SPICE representations of a realistic technology model for simulation. This is done by first synthesizing the Verilog using a commercial synthesis tool, and then by converting the synthesized Verilog netlist into a SPICE netlist that can be simulated directly in HSPICE. All designs in this report were synthesized and simulated using RVT standard cells from the Synopsys 32nm educational library.

Commercial synthesis tools do a reasonable job of choosing ideal standard cells to create a circuit that is well-defined, accurate, and fast enough to meet an imposed timing constraint. The synthesis tools apply a measure of fairness to all behavioral HDL descriptions because they can optimize away inefficiencies in the implementation. We therefore employ



(a)

Fig. 3. System-Level Block Diagram

synthesis tools to ensure a fair comparison between realistic benchmark circuits. The behavioral descriptions are synthesized using Synopsys Design Compiler. Minimal input drive and output loading of 1fF was assigned to all input and output gates to avoid the addition of unnecessary fanout or buffering by the tool. A clock period target of 250ps was used for all designs. Although it is not critical that every design meet this target, this timing constraint ensures that, for most multi-stage combinational paths, the synthesis tool performs some timing optimizations to ensure a reasonably fast circuit block.

The synthesized Verilog netlist was converted to a SPICE deck directly using the Mentor Calibre v2lvs program. The hierarchy was flattened to simplify pulse insertion later in the flow. To limit the SPICE deck file size, flattening was completed using the non-extracted SPICE standard cell library. While excluding parasitics limits the simulation accuracy, a relatively coarse-grained final result (whether or not a state element is upset) is unlikely to be affected by this simplification.

D. SPICE Ground Truth

Before any current pulses are injected to simulate the occurrence of SETs, the SPICE deck is simulated "as is" to provide a ground truth against which later simulations of error events can be compared. To drive the simulation, input vectors are generated randomly according to a defined input activity factor constraint that sets the probability that any input switches from cycle to cycle. For this initial characterization run, the circuit is clocked much more slowly than the synthesis target to ensure correct operation. (The clock period will be shortened based on the results of this initial simulation, as described in the next section.) The number of simulation cycles is constrained by simulation runtime, which increases dramatically for larger combinational blocks. Typically, no more than 200 cycles are simulated for a given netlist. Once this initial simulation is complete, the voltages of the output nodes are used to define correct circuit operation of the simulated circuit for the generated set of input vectors.

E. SPICE with Inserted Pulses

Radiation that strikes at or near a reverse-biased PN junction causes a current pulse. Thus, the probability that a strike occurs at a circuit node depends on the size of all the junctions connected to that node. To simplify this calculation, the SPICE netlist was previously flattened to a transistor granularity. The area of the junctions (source or drain diffusions) connected to a circuit node are summed, and this area is divided by the total combinational circuit area estimated by Design Compiler to obtain the node's strike probability. We make the simplifying assumption that a particle strike only causes a current pulse if it strikes diffusion directly. In reality, a particle striking near diffusion also produces a current pulse, but we neglect this effect for our analysis because the pulse diminishes with increasing distance from the diffusion. We also neglect the possibility that one pulse strikes multiple nodes and produces multiple pulses. Note that the sum of all the probabilities is not one since the total circuit area contains more than just PN junctions. To speed up simulation, the probabilities are weighted to sum to one, and the final FIT rate is derated to account for strikes that would impact the circuit area but miss PN junctions completely.

The minimum clock period for each benchmark is computed to more accurately model behavior, since circuits are generally driven at the minimum allowable clock period. The minimum clock periods are determined by finding the latest-transitioning signal of all signals arriving at the output flip-flops in the SPICE ground truth simulation. These clock periods are measured from SPICE data and so are more accurate than the critical paths reported by Design Compiler, both because of better simulator accuracy and because false paths are not possible. The resultant clock periods are used to simulate the circuit at its fastest possible operation.

Pulse characteristics depend on many factors, and generally an accurate pulse model requires device-level simulation. Such device-level simulation and modeling are beyond the scope of this project, so we used current pulse model parameters derived from literature. We used Equation 1 and approximated the constants Q_{coll}, τ_a, and τ_b from [4], [5], and [6]. In

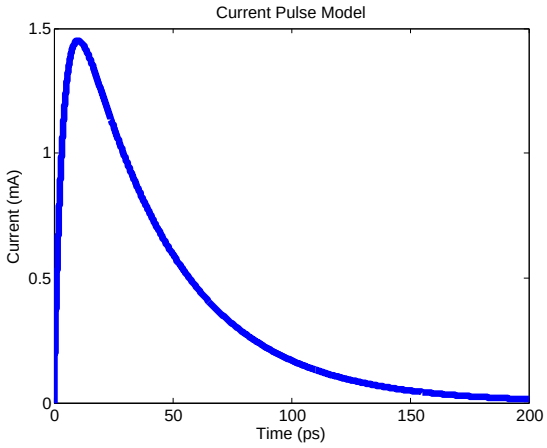


Fig. 4. Pulse model used in our analysis

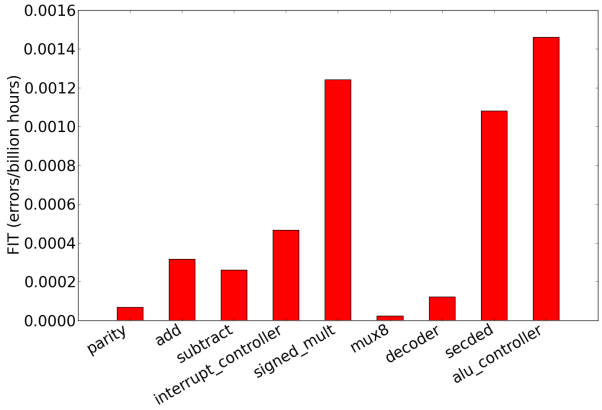


Fig. 5. FIT rates for various benchmark circuits.

particular, Moen characterizes pulse shapes for a 45nm bulk CMOS process, the closest technology to our 32nm library. We chose $Q_{coll} = 75fC$, $\tau_a = 40ps$, and $\tau_b = 4ps$ as default values, which produces the current pulse shown in Figure 4. The current pulse is injected into a random location based on the area-weighted probabilities. Since electron-hole pairs are generated in reverse-biased PN junctions, the struck drain or source of a transistor will always flip the "wrong" way when not connected explicitly to V_{DD} or ground. Thus, high nodes are only injected with negative current, and low nodes are only injected with positive current. These pulses are added to the original SPICE netlist, which is also modified to run at the minimum clock period.

After the pulses are added to the SPICE deck, the SPICE simulation is re-run with the same input vectors as the initial characterization run. Any difference in registered outputs in this second run can then be attributed to an error caused by the injected current pulse.

F. Calculating FIT Rates

Including the area derating mentioned earlier, the total FIT was calculated using the following formula:

$$(\text{flux}) \times (\text{total area}) \times (\text{diffusion derating}) \times (\text{upsets per strike}) \quad (2)$$

Total circuit area was obtained from Design Compiler's report, and matches the sum of all combinational standard cell areas in the block. Since one SET could upset multiple flip-flops, the number of upsets per strike was calculated as the total number of upset bits divided by the number of particle strikes simulated.

IV. Results

All simulations were conducted over 200 cycles, which limited random result variation to a reasonable range while allowing for practical simulation runtimes. The input vectors were randomly generated with an activity factor of 0.5, simulating completely random input activity. Pulse parameters from [6] were used to define an input pulse as shown in Figure 4. Flux was estimated from [1] to be 10^{-9} neutron particles per square micron per second. The simulated FIT rates of a range of combination benchmark circuits are shown in Figure 5. A wide range of FIT rates are measured depending on the circuit. Typical simulated FIT rates range from 10^{-5} to 10^{-3} for the entire circuit. Note that these FIT rates are generally much less than the FIT rate that results from direct particle strikes on the feedback nodes of storage elements, which is typically estimated at 10^{-2} to 10^{-3} per register or SRAM node [12]. Nonetheless, the combinational FIT rate might be more significant for new devices or pulse parameters not modeled here, and is more difficult to correct with error-correcting techniques commonly used in memories.

A. FIT Dependence on Area

One obvious cause of this variation is that larger circuits have more diffusion area and so are more likely to be struck by a random particle. Figure 6 shows a clear correlation between total circuit area and FIT rate. However, this large area dependence masks other important dependencies between circuit parameters and FIT rate. Figure 7 shows FIT rate for various benchmark circuits normalized against the combinational area of each circuit. Even discounting the impact of circuit area, a wide variation in FIT rate remains for different circuits. The impacts of other circuit parameters must therefore be further explored.

B. FIT Dependence on Clock Period

Figure 8 shows the variation in FIT rate against the minimum clock period of each circuit, a measure of the logical depth of the circuit critical path. Note that the FIT rates are again normalized to area, because area and minimum clock period are highly correlated, and the area dependence would otherwise mask the independent contribution of clock period to the FIT rate. A weak negative correlation is observed across the benchmark circuits. This implies that, ignoring circuit area considerations, a more complex circuit with a greater logical depth and longer critical path generally has a lower FIT rate than a simple circuit with a shorter critical path.

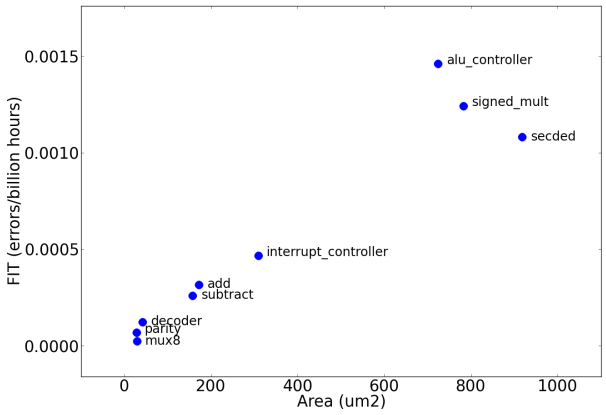


Fig. 6. Circuit FIT rate versus circuit area.

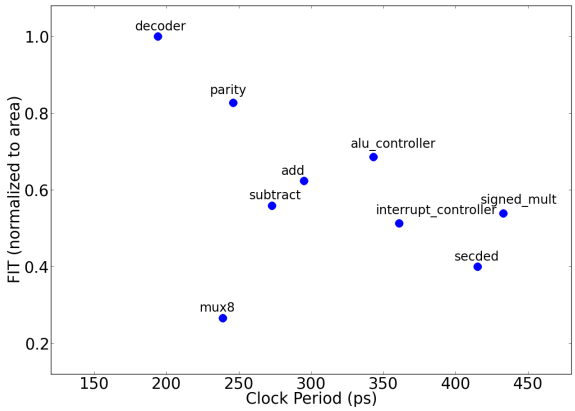


Fig. 8. FIT rates compared to circuit clock period, normalized to area.

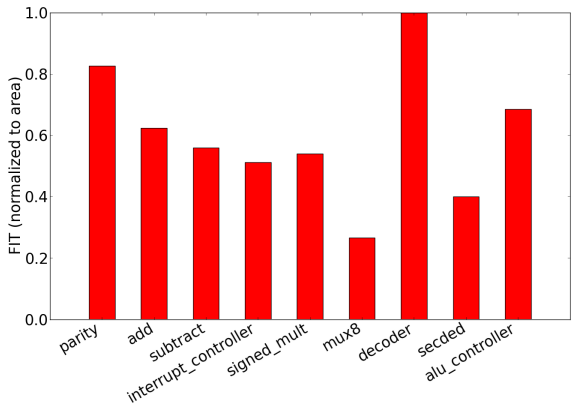


Fig. 7. FIT rates normalized to area.

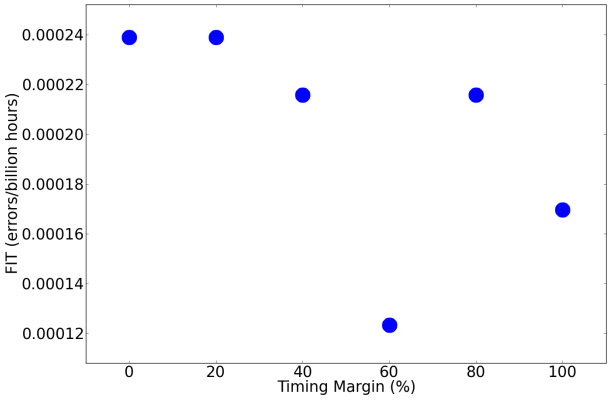


Fig. 9. FIT rates with added timing margin for an 8-bit adder. The data point measured with 60% timing margin is believed to be an outlier due to statistical variation.

This effect reflects the increase in magnitude of all three circuit masking effects for longer combinational paths. More logical and electrical masking occurs over longer paths, and the latching window is a smaller fraction of the overall clock period.

Another way to realize these benefits and decrease FIT rate is to increase the clock period of a circuit by adding additional timing margin. Figure 9 shows the simulated FIT rate for an 8-bit adder with the clock margin increased until the clock period is double the minimum period. Interestingly, even the addition of a large timing margin cannot completely eliminate the effect of SETs because there is always a possibility of a strike occurring at the "wrong" time and being latched into the state element.

Also note that the decrease in FIT is greater for larger circuits with a slower clock period than it is for smaller circuits with an added timing margin. The trend in Figure 8 shows that a circuit with twice the clock period due to more logical depth reduces FIT by about 50%, while a circuit with twice the clock period due to added margin reduces FIT by only 25%. One explanation of this is that adding margin improves only the latching window masking of the circuit, while leaving the logical and electrical masking factors unaffected. Adding additional logic to the path, on the other hand, improves all three masking effects. This suggests that adding excessive margin to each clock cycle is less efficient in reducing FIT for combinational blocks than simply increasing the number of logical stages in each clock period.

C. FIT Dependence on Diffusion Density

In addition to area dependence, some standard cells have a higher diffusion density than others, leading to marginal differences in overall diffusion density of the benchmark circuits. Figure 10 shows the variation in FIT rate against this variation in average diffusion density, normalized to area. As expected, a circuit with a higher percentage of diffusion is more vulnerable to strikes. This effect is small in our circuits because the total combinational area is defined as the sum of the standard cells areas. However, in circuits with area set aside for routing or other purposes, the lower diffusion density would make the circuit less susceptible to SETs.

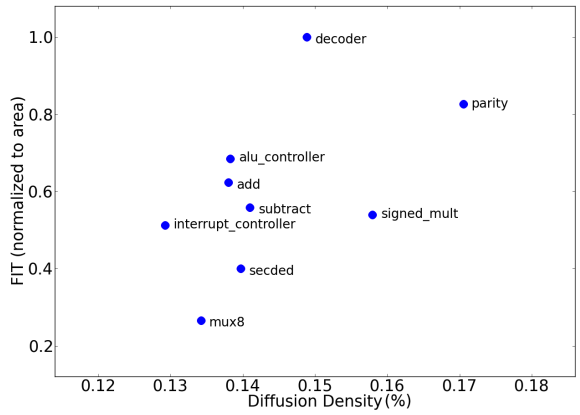


Fig. 10. FIT rates of circuits with various diffusion densities.

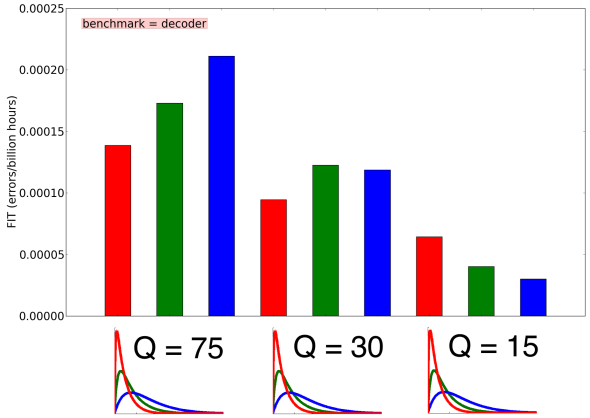


Fig. 11. FIT rates with various pulses injected. Q is charge in fC.

D. FIT Dependence on Pulse Parameters

While the shape of the current pulse used in simulation was estimated from literature, the actual pulse parameters vary with the operating condition, distance from diffusion, strike angle, and particle energy. These dependencies require device-level simulations to accurately characterize the pulse shape. To model this, the collected charge and time constants from Equation 1 were varied. Figure 11 shows how pulse parameters change the FIT rate. When the collected charge Q is large, increasing the pulse duration increases the FIT because a significant voltage transient lasts longer. As the collected charge decreases, electrical masking lowers the FIT rate of longer pulses. The pulse dimensions clearly have a large impact on the overall FIT rate. More accurate pulse measurements or simulations would improve the accuracy of the modeling described in this work.

V. Conclusion

Combinational logic upset rates were found to depend on several circuit parameters, including circuit area, logic depth, and diffusion density. Current methods of calculating datapath FIT rates require complex multi-level approximations and equations, while our work relies on SPICE simulations to fully capture circuit behavior. This work could be extended by applying more accurate models of the current pulse caused by particle strikes. Nonetheless, our results lay the groundwork for a comprehensive measure of circuit vulnerability to radiation-induced soft errors.

References

[1] N. Seifert, "Radiation-induced soft errors: A chip-level modeling perspective," *Foundations and Trends in Electronic Design Automation*, vol. 4, no. 2-3, pp. 99–221, 2010.

[2] R. Ramanarayanan, V. Degalahal, R. Krishnan, J. S. Kim, V. Narayanan, Y. Xie, M. J. Irwin, and K. Unlu, "Modeling soft errors at the device and logic levels for combinational circuits," *Dependable and Secure Computing*, pp. 202–216, 2009.

[3] A. Chavan, E. MacDonald, J. Neff, and E. Bozeman, "Radiation hardened flip-flop design for super and sub threshold voltage operation," *Aerospace Conference*, pp. 1–6, 2011.

[4] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, , and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," *Dependable Systems and Networks*, pp. 389–398, 2002.

[5] G. Hubert, A. Bougerol, F. Miller, N. Buard, L. Anghel, T. Carriere, F. Wrobel, and R. Gaillard, "Prediction of transient induced by neutron/proton in cmos combinational logic cells," *On-Line Testing Symposium*, 2006.

[6] K. Moen, S. Phillips, E. Wilcox, J. Cressler, H. Nayfeh, A. Sutton, J. Warner, S. Buchner, D. McMorrow, G. Vizkelethy, and P. Dodd, "Evaluating the inuence of various body-contacting schemes on single event transients in 45-nm soi cmos," *Transactions on Nuclear Science*, pp. 3366–3372, 2010.

[7] B. Zhang, W. S. Wang, and M. Orshansky, "Faser: Fast analysis of soft error susceptibility for cell-based designs," *7th International Symposium on Quality Electronic Design*, pp. 760–765, 2006.

[8] F. Wang, Y. Xie, R. Rajaraman, , and B. Vaidyanathan, "Soft error rate analysis for combinational logic using an accurate electrical masking model," *VLSI Design*, pp. 165–170, 2007.

[9] S. Mukherjee, C. Weaver, J. Emer, S. Reinhardt, and T. Austin, "A systematic methodology to compute the architectural vulnerability factors for a high-performance microprocessor," in *Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on*, Dec., pp. 29–40.

[10] N. Wang, J. Quek, T. Rafacz, and S. Patel, "Characterizing the effects of transient faults on a high-performance processor pipeline," in *Dependable Systems and Networks, 2004 International Conference on*, June-1 July, pp. 61–70.

[11] M. Hansen, H. Yalcin, and J. P. Hayes, "Unveiling the iscas-85 benchmarks: A case study in reverse engineering," *IEEE Design and Test*, vol. 16, no. 3, pp. 72–80, 1999.

[12] S. Mukherjee, J. Emer, and S. Reinhardt, "The soft error problem: an architectural perspective," in *High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on*, Feb., pp. 243–247.