Logic Energy and Resiliency (LEARN) Project

Goal

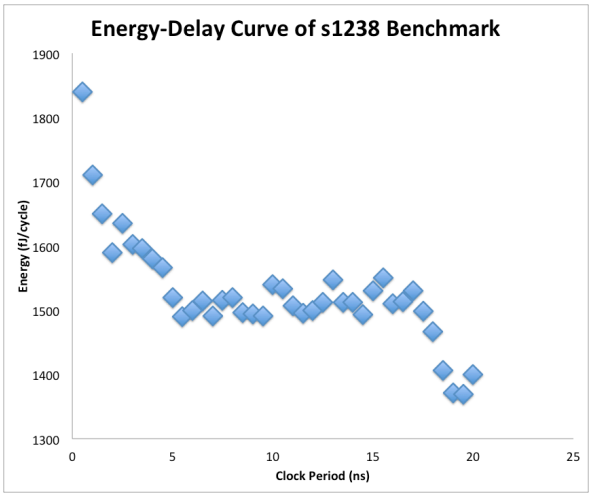
There are two goals of the project. The first goal is to obtain energy vs. resiliency Pareto-optimal curves for various parameters. The second goal is to focus on scaling the computations for large designs (> 100k gates) to reasonable runtimes (~ hours).

Results so far

We have chosen parameters to vary, given below.

- Clock period
- Number of latches hardened
- Number of gates hardened
- Number of flip-flops replaced with BISER flip-flops
- Number of combinational logic (CL) blocks replaced with CL BISER
- Amount of error correcting code (ECC) on pipeline/datapath
- Number of flip-flops replaced with Razor flip-flops
- Number of latches replaced with Bubble Razor latches

We have chosen two benchmarks for now. The first is a small ISCAS benchmark (s1238) with 428 gates. The second is the RISC V processor with Rocket ISA designed by the architecture group here at Berkeley (50k gates, more if vector unit is included). My task has been setting up Synopsys CAD tools to run simulation and provide accurate energy measurements. Our flow currently correctly synthesizes a design, simulates it, and then calculates the energy per cycle of the design. We get the plot shown in Figure 1 when we vary the clock period of the s1238 design. The "noise" in the s1238 energy calculations is likely due to the small size of the benchmark.



Changes in direction

Considering the effort it will take to implement the various parameters, we have decided to make the second goal optional. If we have time, we will work on it.

Schedule

Week	Task	Who?
Nov. 18-22	Implement hardened cells Pre-characterize tech. cells	Stevo Amudhan
Nov. 25-29	Implement BISER parameter	Stevo
Dec. 2-6	Implement Razor/ECC params Edit BFIT to work with Verilog	Stevo Amudhan
Dec. 9-12	Compile presentation	Both
Dec. 16-18	Write report	Both