STEVO BAILEY

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EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY, Berkeley, CA (UCB) Fall 2012–Present

- MS (Fall 2014), Doctor of Philosophy in Electrical Engineering and Computer Science (in progress) (GPA: 3.95/4.00)

UNIVERSITY OF VIRGINIA, Charlottesville, VA (UVA) Fall 2008–Spring 2012

- BS in Engineering Science, Minor in Electrical Engineering, BA in Physics, BA in Music, Rodman Scholar (GPA: 3.9/4.0)

Programming Skills: Java, Perl, Python, Bash, Verilog, Chisel, Scala, TCL, MATLAB, LaTeX, HTML, CSS
Computer Skills: Linux, Cadence CAD tools, Synopsys CAD tools, Mentor CAD tools, Git, Microsoft Office, VIM

EXPERIENCE AND EMPLOYMENT HISTORY

Graduate Researcher, UCB Fall 2012–Present

- Researching under Professor Bora Nikolić
- Led the tape out of two instances of the Chisel DSP generator methodology, one targeting Radar applications with Northrop Grumman Corporation and Cadence Design Systems, and the other targeting sparse spectrum sensing radio applications, both in May 2017 in TSMC 16nm FinFET
- Designed a DSP coprocessor generator methodology in Chisel, including verification generators, for the DARPA CRAFT project and my final PhD work, available here: https://github.com/ucb-art/craft2-chip
- Led the tape-out of the 10 GHz bandwidth ASIC spectrometer I designed at JPL in Summer 2014, which also included a high-speed 8 lane SerDes, nearly fully digital bang-bang PLL, and new radiation-hardened flip-flop design; taped out December 2015 in ST's 28nm UTB FDSOI process

Intern, Nvidia Corporation Summer 2015

- Researched the effect of radiation-induced soft errors in integrated circuits in the Circuits Research Group under Tom Gray

Intern, NASA Jet Propulsion Laboratory Summer 2014

- Designed a 10 GHz bandwidth ASIC spectrometer digital backend using Chisel, a Berkeley hardware construction language

Researcher, UVA Summer 2011

- Investigated an integrated circuit modular adder design with error detection and correction under Professor Mircea Stan

SELECTED PUBLICATIONS

Bailey, S. et al., "A 28nm FDSOI 8192-Point Digital ASIC Spectrometer from a Chisel Generator", CICC, April 2018.
Wang, A., et a., "A 0.37mm2 LTE/Wi-Fi compatible, memory-based, runtime-reconfigurable 2n3m5k FFT accelerator integrated with a RISC-V core in 16nm FinFET", ASSCC, pp. 305-308, November 2017.
Keller, B. et al., "A RISC-V Processor SoC With Integrated Power Management at Submicrosecond Timescales in 28 nm FD-SOI", JSSC, vol. 52, no. 7, pp. 1863-1875, May 2017.
Zimmer, B. et al., "A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI," JSSC, vol. 51, no. 4, pp. 930-942, April 2016.
Lee, Y. et al., "An agile approach to building RISC-V microprocessors," IEEE Micro, pp. 8-20, March 2016.
Bailey, S. and Stan, M. "A new taxonomy for reconfigurable prefix adders," ISCAS, May 2012.

AWARDS AND HONORS

Electrical Engineering and Computer Sciences Departmental Fellowship, UCB Fall 2012–Spring 2013
ASM Eastern Virginia Scholarship Fall 2008–Spring 2012

ACTIVITIES AND LEADERSHIP POSITIONS

Instructor, Generator Bootcamps, Berkeley and San Jose, CA Fall 2017

- Designed a suite of instructive tutorials on Chisel and our Craft digital design generator methodology
- Led two bootcamps on this material, one at UC Berkeley and the other at Cadence Design Systems

Peru Team Lead, Engineers Without Borders, UCB Spring 2016–Spring 2017