STEVO BAILEY

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EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY, Berkeley, CA (UCB) Fall 2012–Present

- MS (Fall 2014), Doctor of Philosophy in Electrical Engineering and Computer Science (in progress) (GPA: 3.95/4.00)

UNIVERSITY OF VIRGINIA, Charlottesville, VA (UVA) Fall 2008–Spring 2012

- BS in Engineering Science, Minor in Electrical Engineering, BA in Physics, BA in Music, Rodman Scholar (GPA: 3.9/4.0)

Programming Skills: Java, Perl, Python, Bash, Verilog, Chisel, TCL, MATLAB, LaTeX, HTML, CSS
Computer Skills: Linux, Cadence CAD tools, Synopsys CAD tools, Git, Microsoft Office, VIM

EMPLOYMENT HISTORY

Graduate Researcher, UCB Fall 2012–Present

- Researching under Professors Bora Nikolić
- Led the tape-out of the 10 GHz bandwidth ASIC spectrometer I designed at JPL in Summer 2014, which also included a high-speed 8 lane SerDes, nearly fully digital bang-bang PLL, and new radiation-hardened flip-flop design; taped out December 2015 in ST's 28nm UTB FDSOI process
- Scripted a flow to calculate the energy efficiency and failure rate of numerous soft-error resiliency techniques for arbitrary logic circuits and flip-flop designs; tested on the Raven 3 architecture
- Established and perfected the place-and-route flow for Raven 3, a custom RISC-V processor with on-chip DVFS using high-efficiency, unregulated DCDC converters and an adaptive clock generator; taped out in ST's 28nm UTB FDSOI process in August 2013; achieved 26 GFLOPS/W running DGEMM

Intern, Nvidia Corporation Summer 2015

- Researched the effect of radiation-induced soft errors in integrated circuits in the Circuits Research Group under Tom Gray

Intern, NASA Jet Propulsion Laboratory Summer 2014

- Designed a 10 GHz bandwidth ASIC spectrometer digital backend using Chisel, a Berkeley hardware construction language

Researcher, UVA Summer 2011

- Investigated an integrated circuit modular adder design with error detection and correction under Professor Mircea Stan

PUBLICATIONS

Zimmer, B. et al., "A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI," JSSC, vol. 51, no. 4, pp. 930-942, April 2016.

Lee, Y. et al., "An agile approach to building RISC-V microprocessors," IEEE Micro, pp. 8-20, March 2016.

Zimmer, B. et al., "A RISC-V vector processor with tightly-integrated switched-capacitor DC-DC converters in 28nm FDSOI," VLSI Circuits, 2015.

Jevtic, R., Hanh-Phuc Le, Blagojevic, M., Bailey, S., Asanovic, K., Alon, E., and Nikolic, B., "Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors," TVLSI, vol. PP, no. 99, 2014.

Bailey, S. and Stan, M. "A new taxonomy for reconfigurable prefix adders," ISCAS, 2012.

AWARDS AND HONORS

Electrical Engineering and Computer Sciences Departmental Fellowship, UCB Fall 2012–Spring 2013
ASM Eastern Virginia Scholarship Fall 2008–Spring 2012

ACTIVITIES AND LEADERSHIP POSITIONS

Webmaster, Engineers Without Borders, UC Berkeley Spring 2016–Present

- Traveled to Peru, conducted monitoring and evaluation on previous RWC implementations, tested extant well water and RWC water for arsenic, took pre-implementation measurements for a new RWC system, and discussed a new agreement with members of Suma Marka (local NGO), the local health system, the local university, and the local community

Volunteer, Alta Bates Summit Medical Center, Berkeley, CA Spring 2016–Present