STEVO BAILEY

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EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY, Berkeley, CA (UCB) Fall 2012–Present

- MS (Fall 2014), Doctor of Philosophy in Electrical Engineering and Computer Science (GPA: 3.97 / 4.00)

UNIVERSITY OF VIRGINIA, Charlottesville, VA (UVA) Fall 2008–Spring 2012

- BS in Engineering Science, Minor in Electrical Engineering, BA in Physics, BA in Music (GPA: 3.86 / 4.00)

Programming Skills: Java, Perl, Python, Bash, Verilog, Chisel, TCL, MATLAB, LaTeX, HTML, CSS
Computer Skills: Linux, Cadence CAD tools, Synopsys CAD tools, Git, Microsoft Office, VIM

EMPLOYMENT HISTORY

Graduate Researcher, UCB Fall 2012–Present

- Researching under Professors Bora Nikolic and Krste Asanovic
- Scripted a flow to calculate the energy efficiency and failure rate of numerous soft-error resiliency techniques for arbitrary logic circuits; tested on the Raven 3 architecture
- Established and perfected the place-and-route flow for Raven 3, a custom RISC-V processor with on-chip DVFS using high-efficiency, unregulated DCDC converters and an adaptive clock generator; taped out in ST's 28nm UTB FDSOI process in August 2013; achieved 26 GFLOPS/W running DGEMM
- Helped update and improve Raven 3 with more vector lanes, more test and measurement structures, and a back-bias generator; taped out in November 2014
- Currently researching a new spatial computing architecture with RISC-V cores, vector units, thread-level speculation, and dynamic memory allocation for digital signal processing applications

Intern, NASA Jet Propulsion Laboratory Summer 2014

- Designed a 10 GHz bandwidth ASIC spectrometer digital backend using Chisel, a Berkeley hardware construction language

Graduate Student Instructor, UCB Fall 2013–Spring 2014

- Created weekly homework assignments and exam questions in digital integrated circuits for 40 students
- Prepared and lectured at weekly discussion sections, held weekly office hours for student help, proctored exams, and mentored students in Cadence software for lab assignments and a CORDIC design project

Researcher, UVA Summer 2011

- Researched as an undergrad with Professor Mircea Stan and graduate students
- Investigated an integrated circuit modular adder design with error detection and correction

PUBLICATIONS

Bailey, S. and Stan, M. "A new taxonomy for reconfigurable prefix adders," ISCAS, 2012.
Jevtic, R., Hanh-Phuc Le, Blagojevic, M., Bailey, S., Asanovic, K., Alon, E., and Nikolic, B., "Per-Core DVFS With Switched-Capacitor Converters for Energy Efficiency in Manycore Processors," TVLSI, vol. PP, no. 99, 2014.

AWARDS AND HONORS

Electrical Engineering and Computer Sciences Departmental Fellowship, UCB Fall 2012-Spring 2013
ASM Eastern Virginia Scholarship Fall 2008-Spring 2012

ACTIVITIES AND LEADERSHIP POSITIONS

Student, Synopsys, Inc., Mountain View, CA September 2013

- Attended a two day lecture series on Synopsys PrimeTime Signal Integrity and constraint debugging

Student, Engineering in a Global Context, Stuttgart, Germany Summer 2009

- Attended presentations at 12 different locations including German engineering companies, universities, and museums to hear speakers and ask questions related to research topic
- Researched and wrote a 10 page paper comparing German and American sustainability