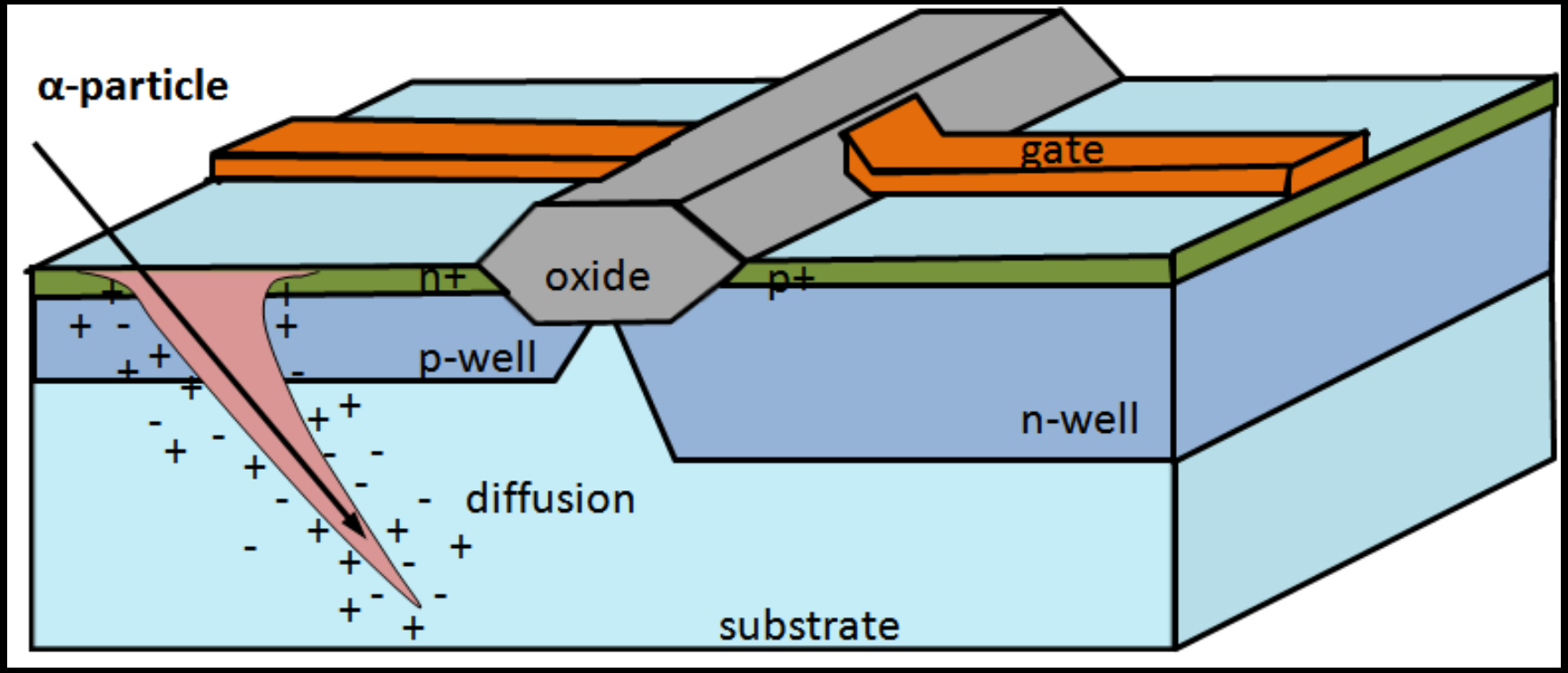
Logic Energy and Resiliency

Radiation-induced Soft Error Hardening Analysis

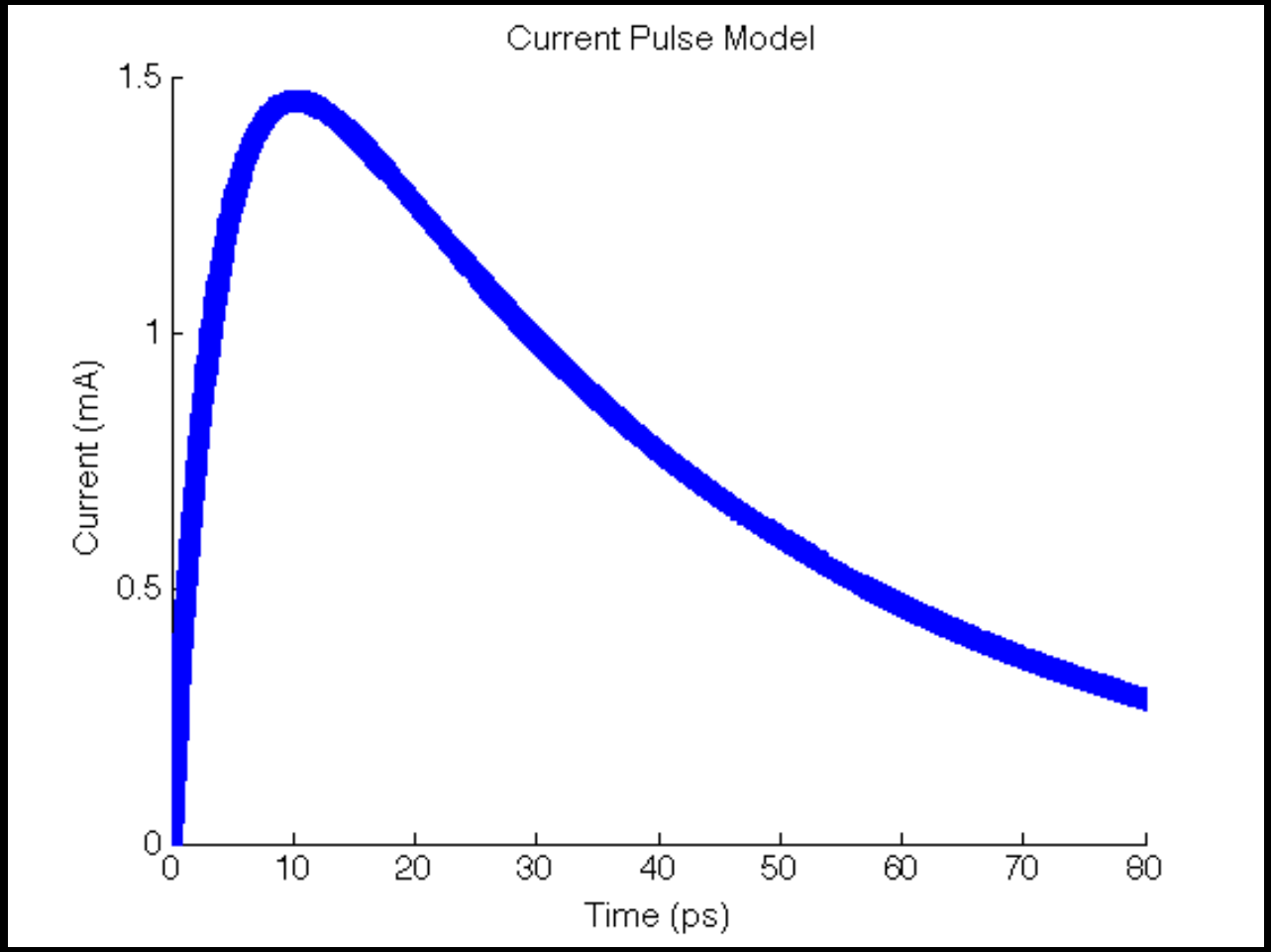
Background



[http://aviral.lab.asu.edu/?page_id=1434]

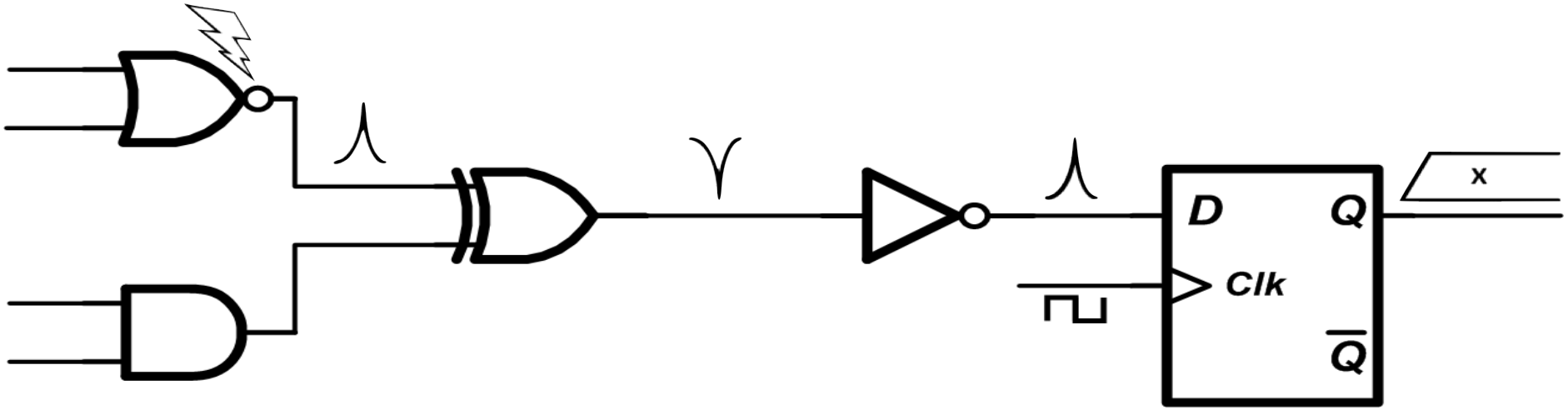
High-energy particle strikes induce current

Background

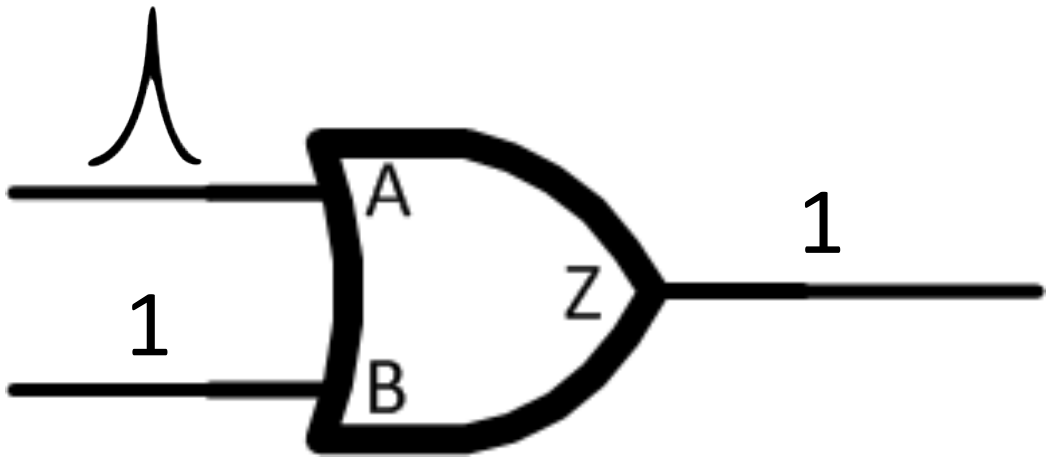


Induced current is double exponential pulse

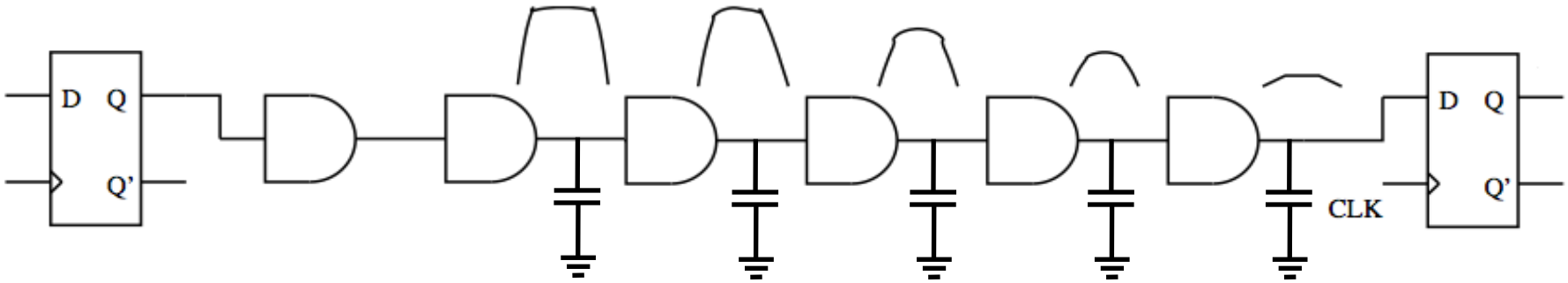
Background



Logical Masking

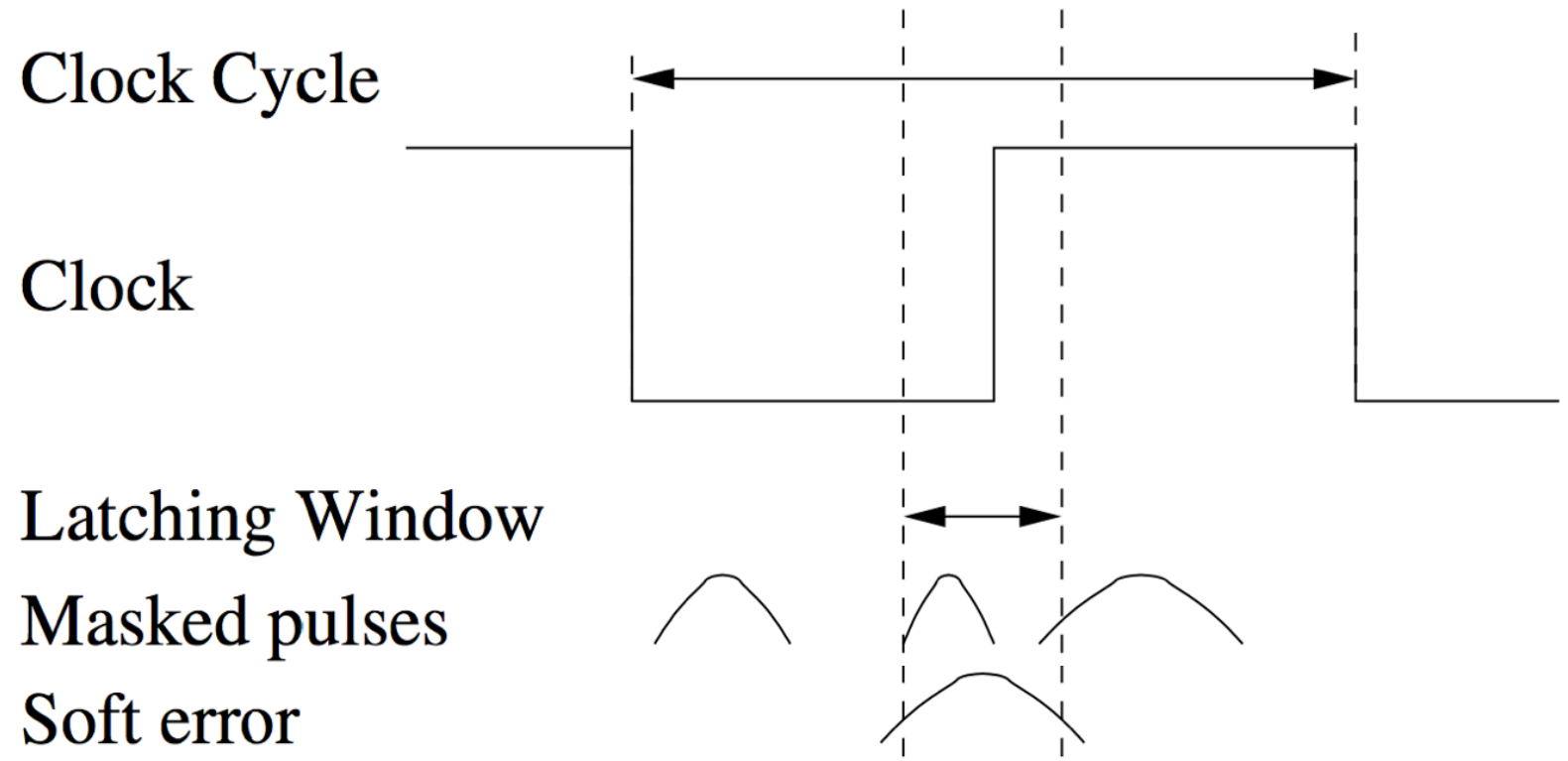


Electrical Masking



Shivakumar, DSN 2002

Latching Window Masking



Shivakumar, DSN 2002

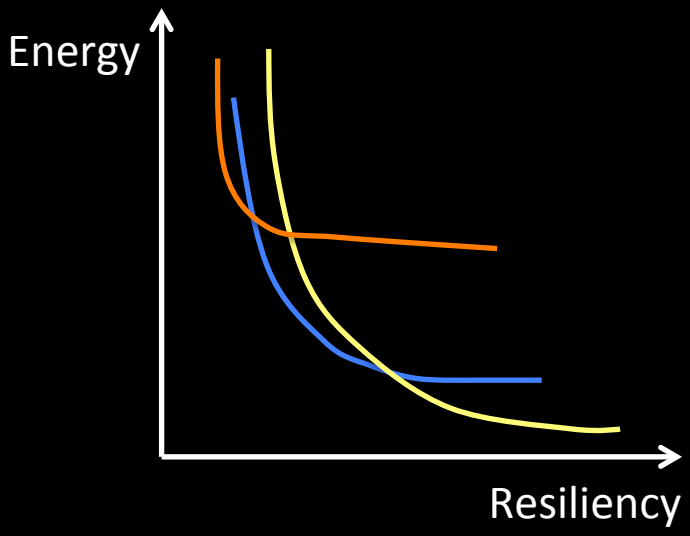
Logic Resiliency Techniques

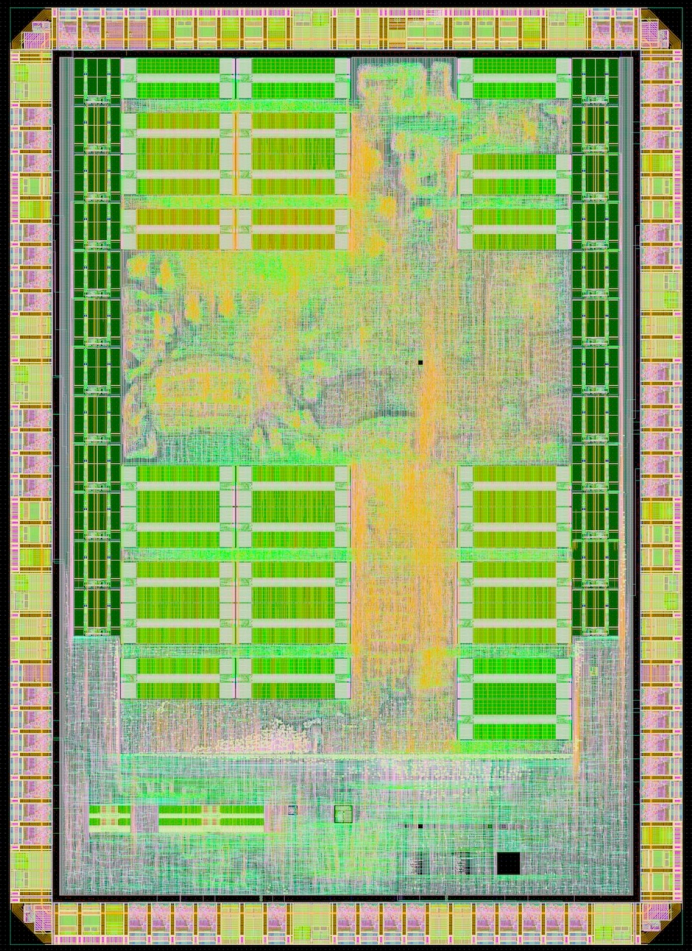
- Bigger devices
- Redundancy
- Error detection/correction
- …

But at what cost??

Project Goals

1) Energy vs. Resiliency curves for various logic resiliency techniques
2) Scalable algorithms for large designs

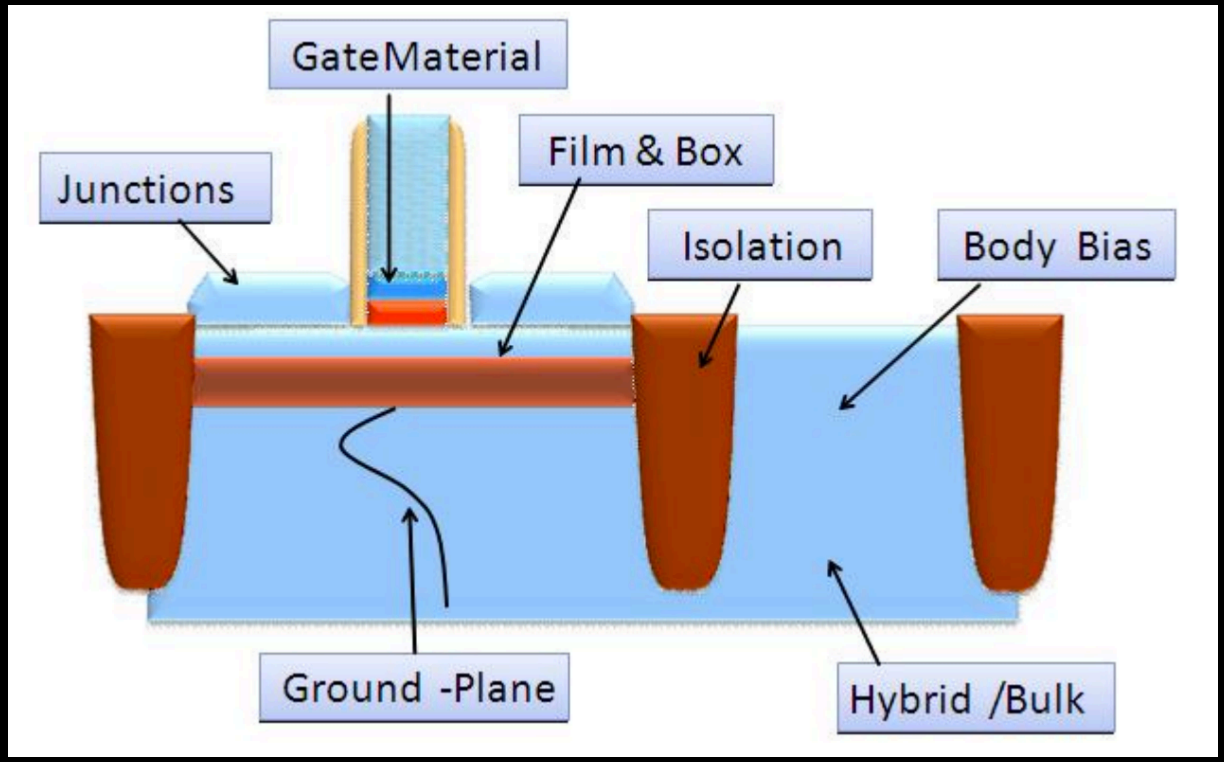




Project Outline

- Resiliency techniques:
  - Manual insertion
- Energy:
  - Synopsys CAD tools
- Resiliency:
  - BFIT (Berkeley logic FIT estimation tool)

Technology

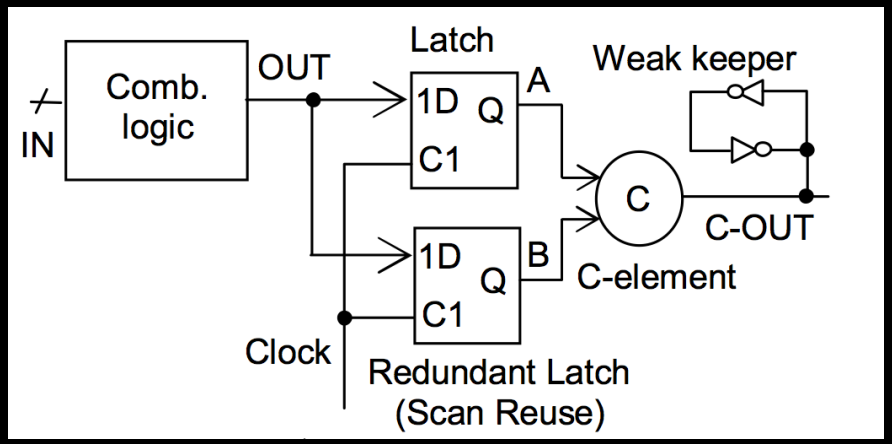


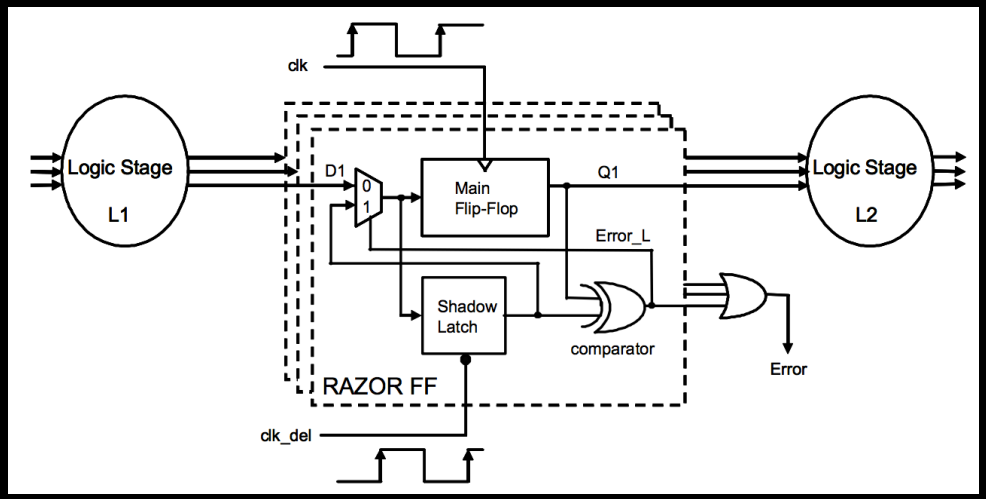
STMicroelectronics 28nm FDSOI

Resiliency Techniques

1. Performance scaling
2. Latch Hardening
3. Gate Hardening
4. BISER
5. Datapath ECC
6. Razor

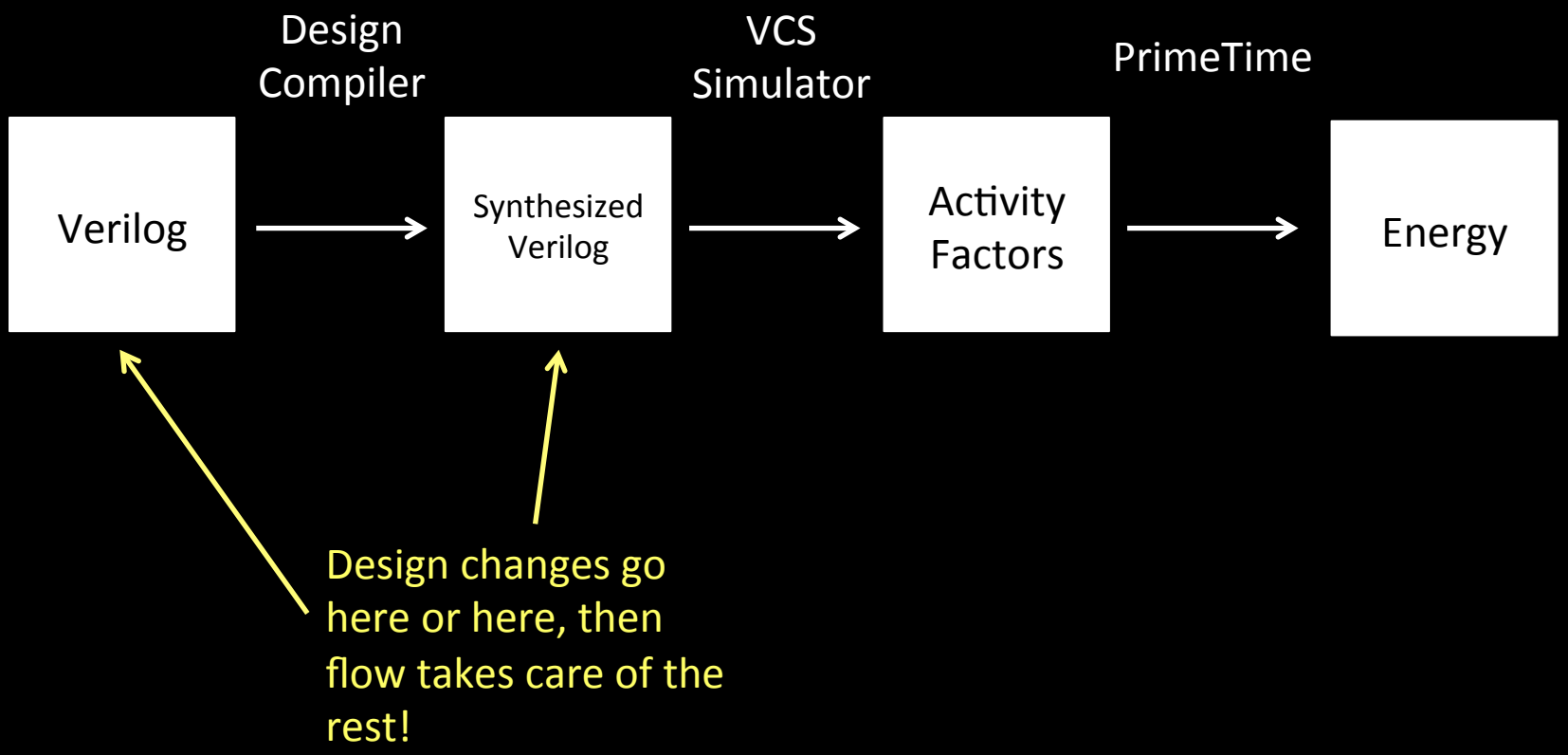
Mitra, ITC 2006





Ernst, Micro 2003

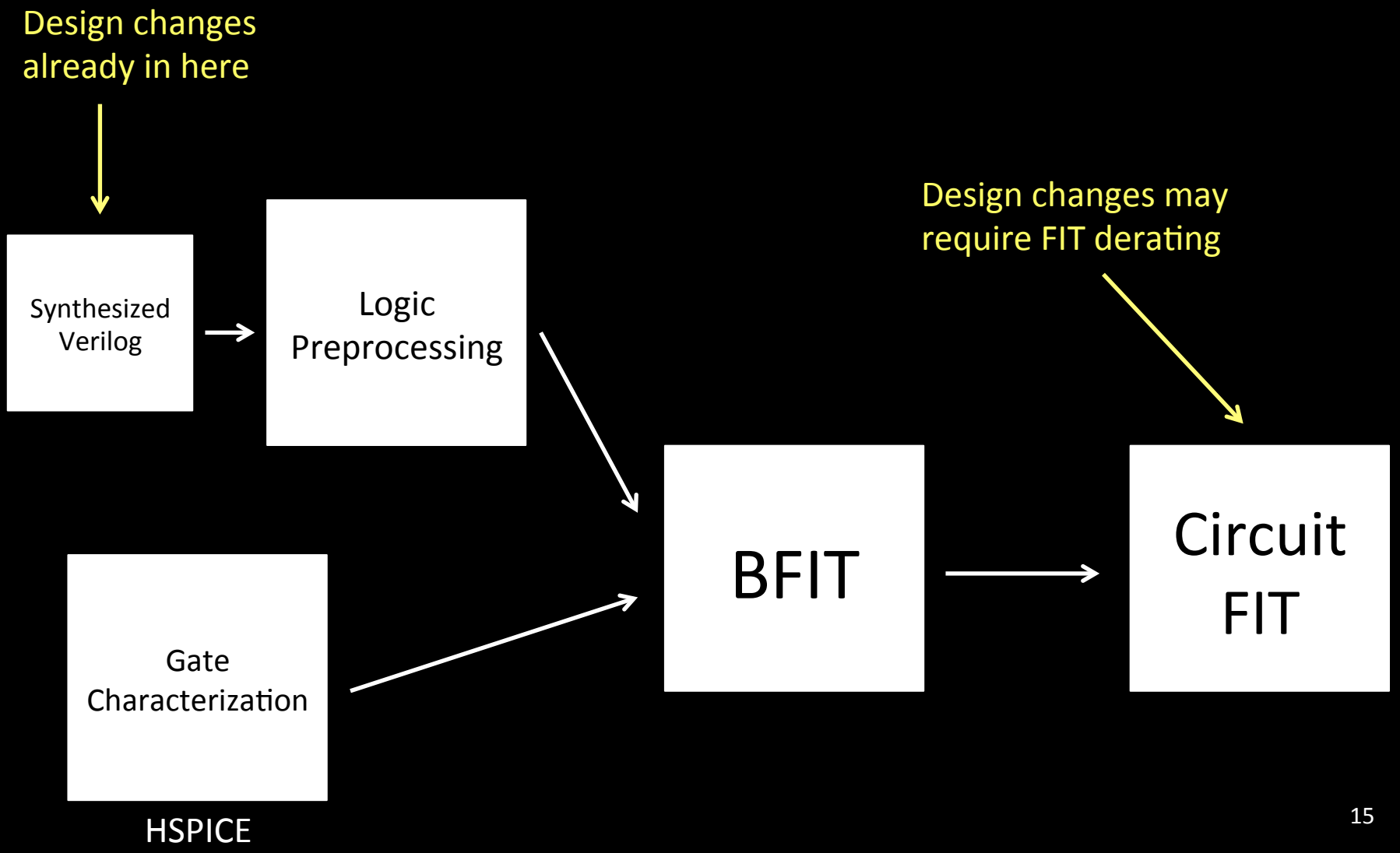
Energy


Design Compiler
VCS Simulator
PrimeTime
Verilog
Synthesized Verilog
Activity Factors
Energy
Design changes go here or here, then flow takes care of the rest!

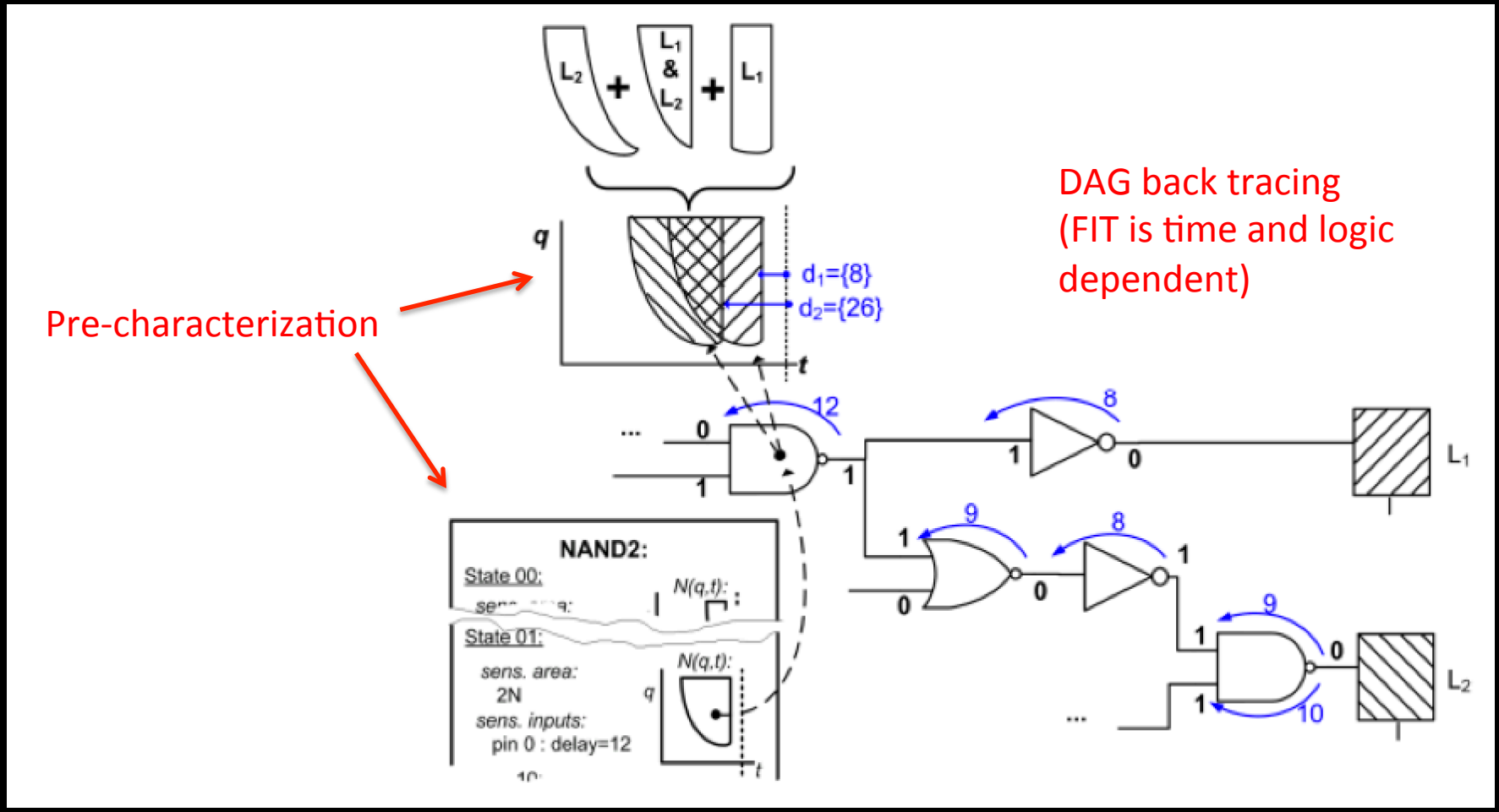
Resiliency

(FIT = Failures in Time,
or failures per billion hours)

Resiliency

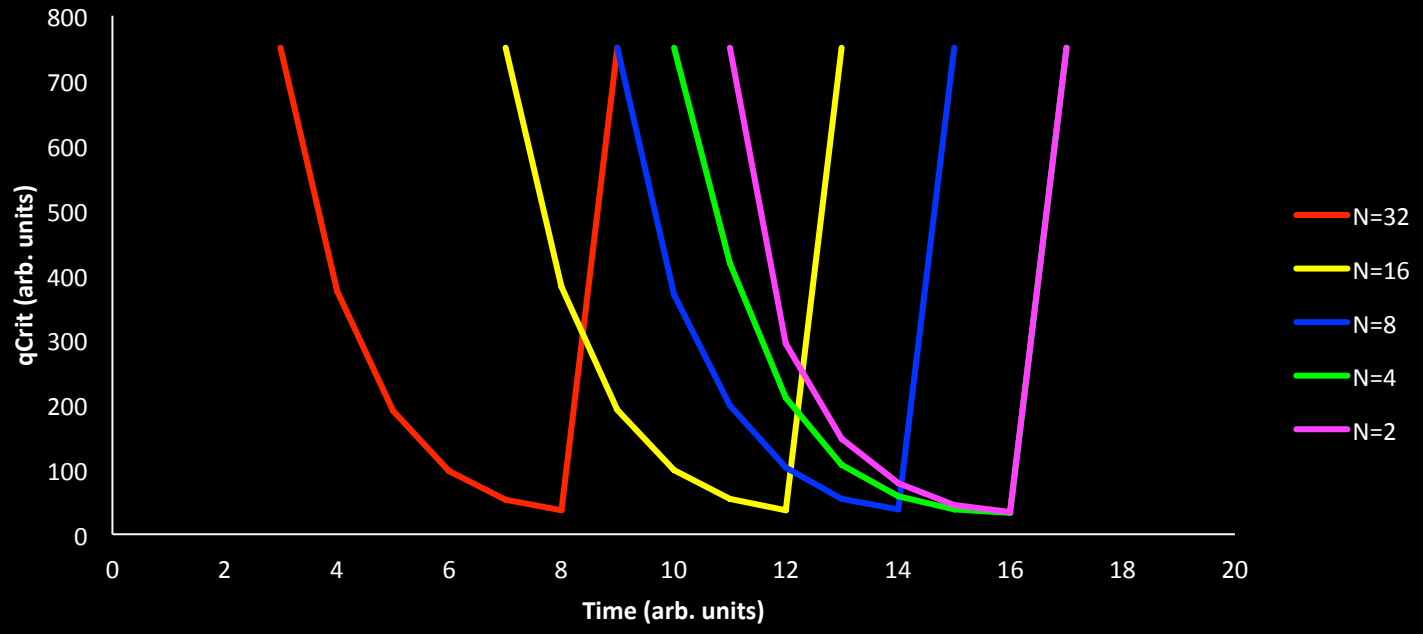

Design changes already in here
Synthesized Verilog
Logic Preprocessing
Design changes may require FIT derating
Gate Characterization
HSPICE
BFIT
Circuit FIT

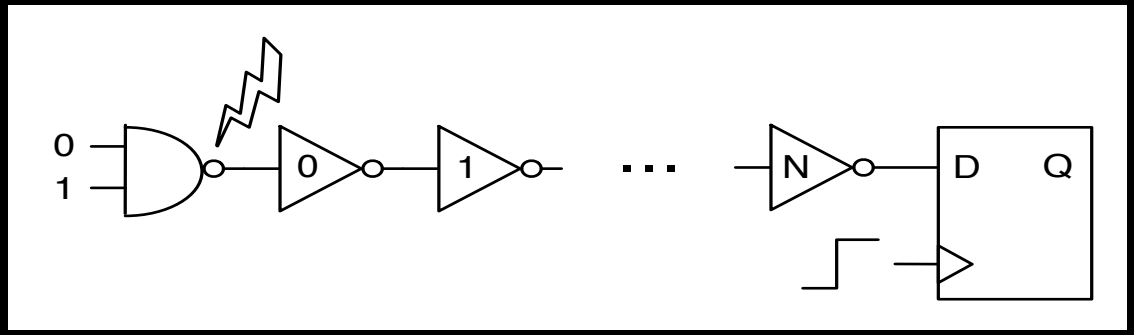
BFIT


Pre-characterization
DAG back tracing
(FIT is time and logic dependent)
L2
L1 & L2
L1
q
t
d1={8}
d2={26}
12
8
9
8
9
10
NAND2:
State 00:
State 01:
sens. area:
2N
sens. inputs:
pin 0 : delay=12
N(q,t):

Electrical Attenuation

No significant electrical attenuation in 28nm FDSOI

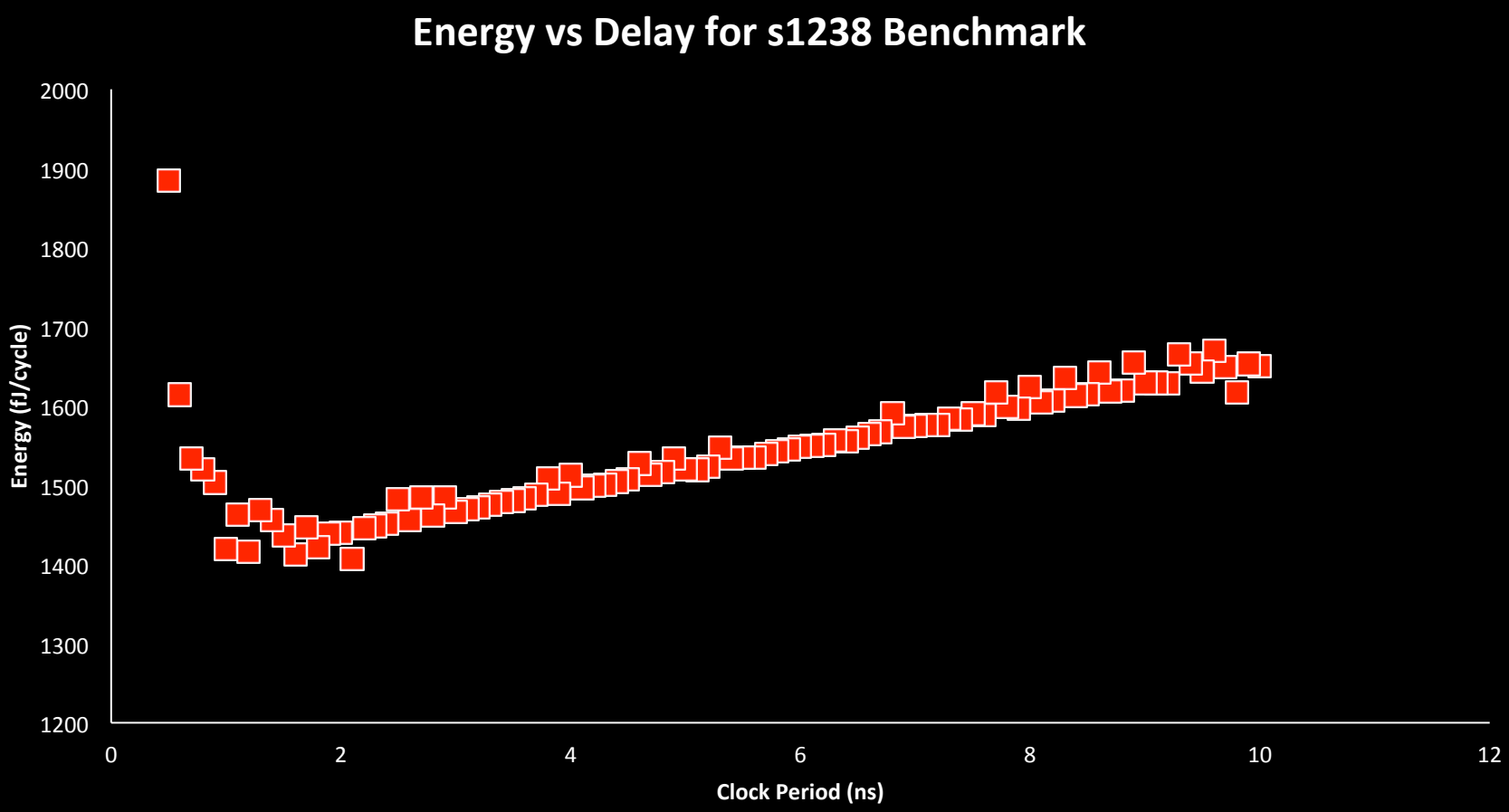




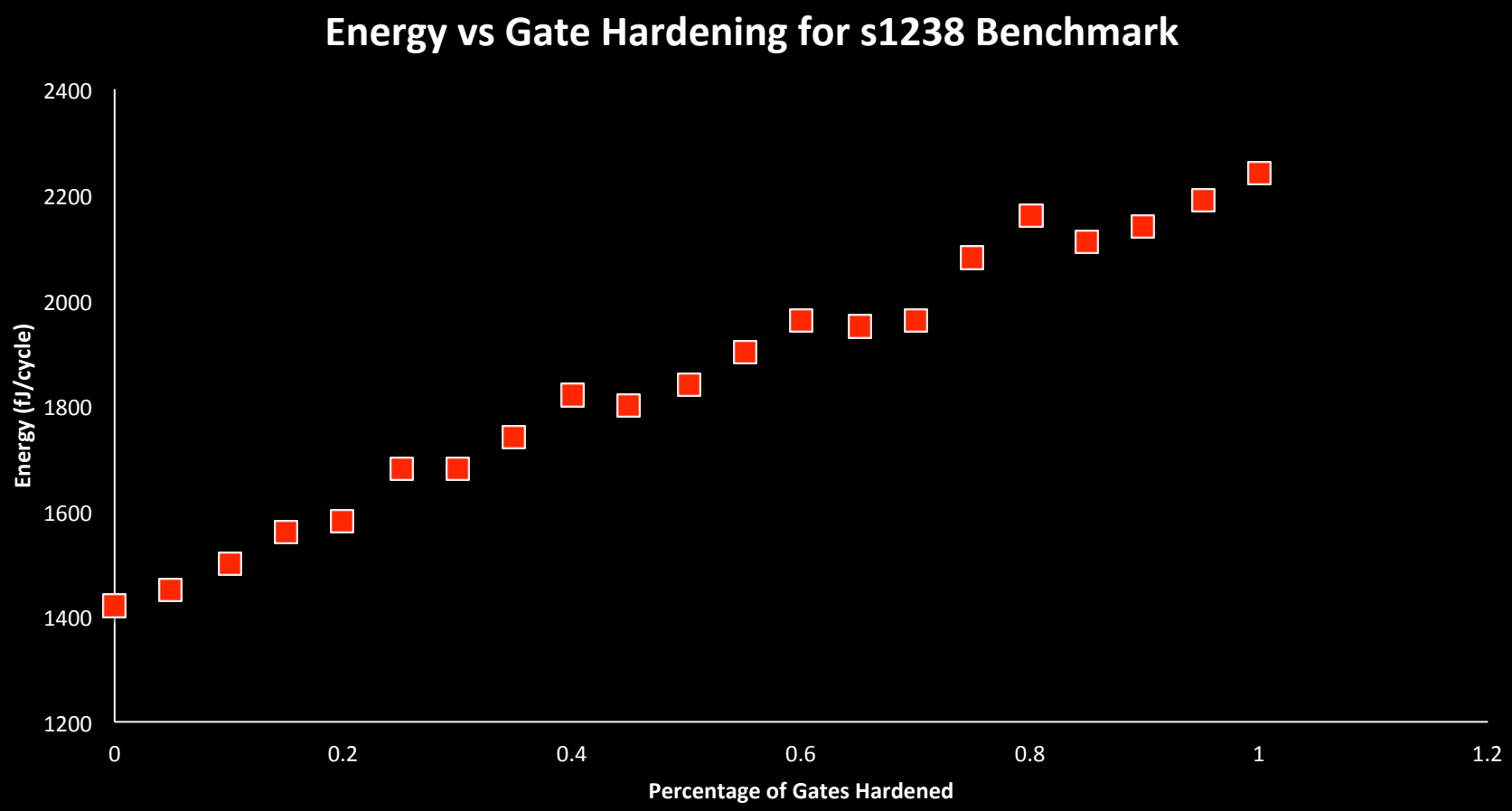
Designs

- S1238 – arbitrary ISCAS benchmark
  - 350 gates
- Rocket core with RISCV ISA
  - Berkeley processor
  - ~300k gates

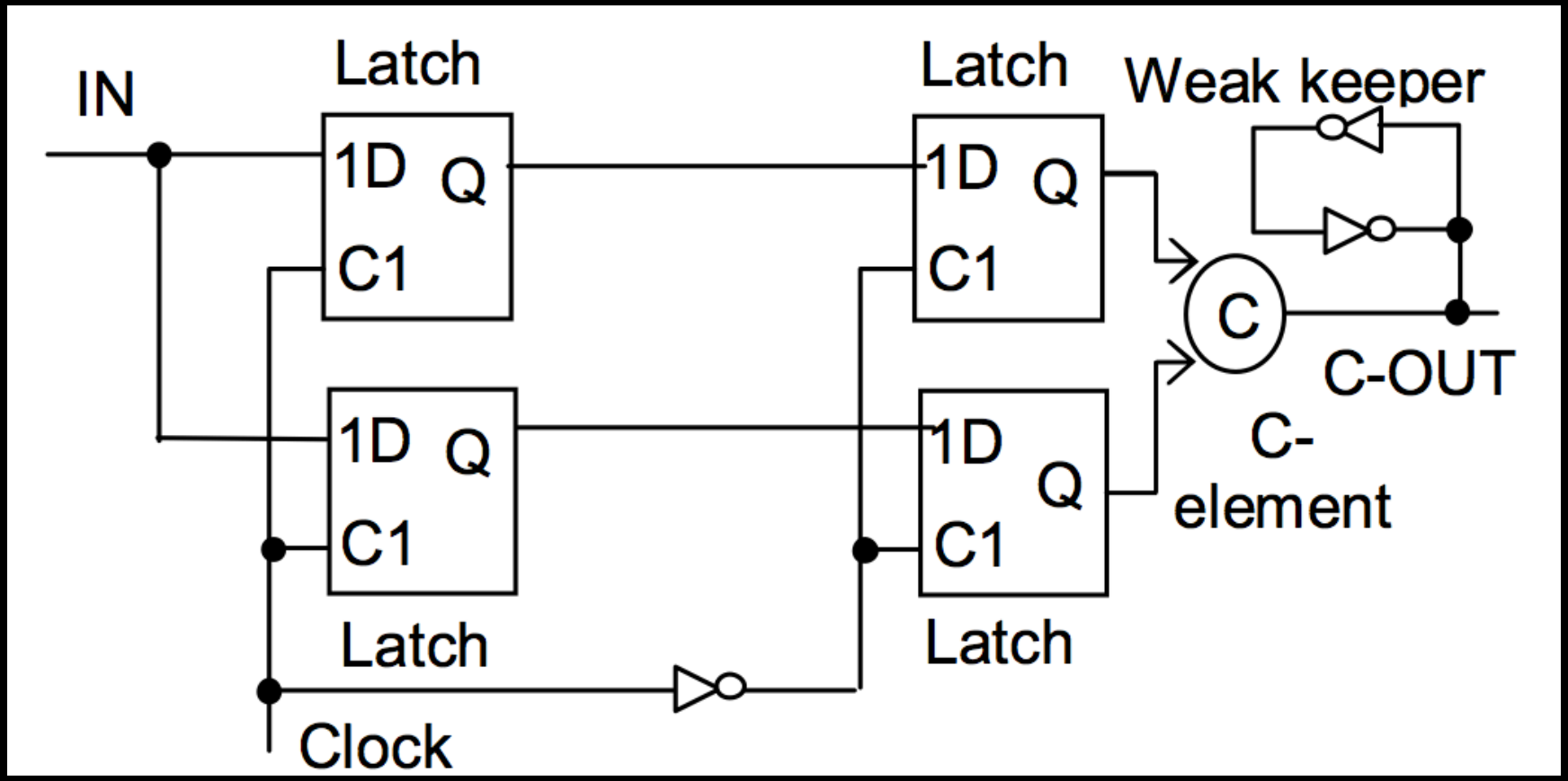
Results


Energy vs Delay for s1238 Benchmark
Energy (fJ/cycle)
2000
1900
1800
1700
1600
1500
1400
1300
1200
0
2
4
6
8
10
12
Clock Period (ns)

Results

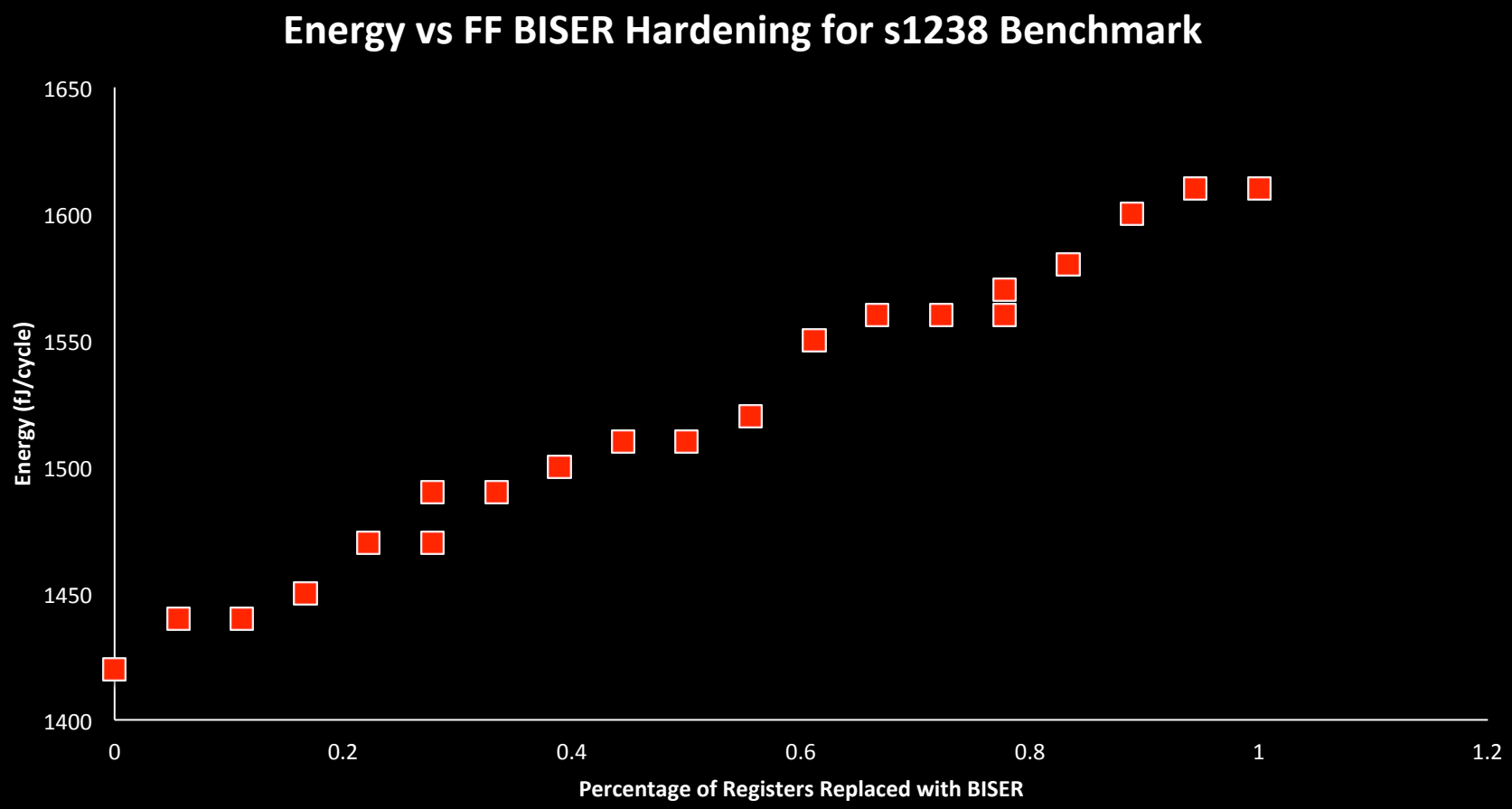

Energy vs Gate Hardening for s1238 Benchmark
Energy (fJ/cycle)
2400
2200
2000
1800
1600
1400
1200
0
0.2
0.4
0.6
0.8
1
1.2
Percentage of Gates Hardened

Results

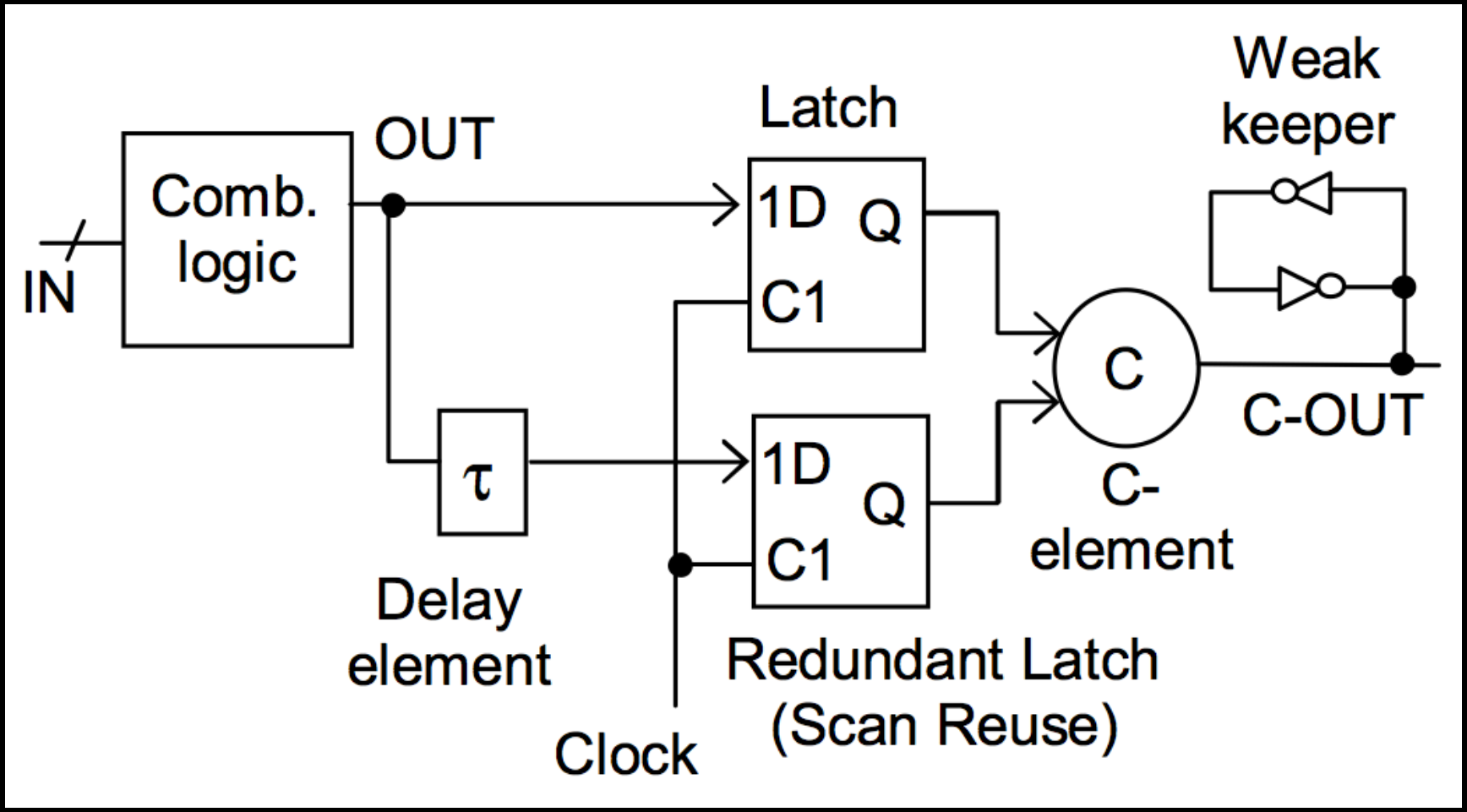


BISER

Results

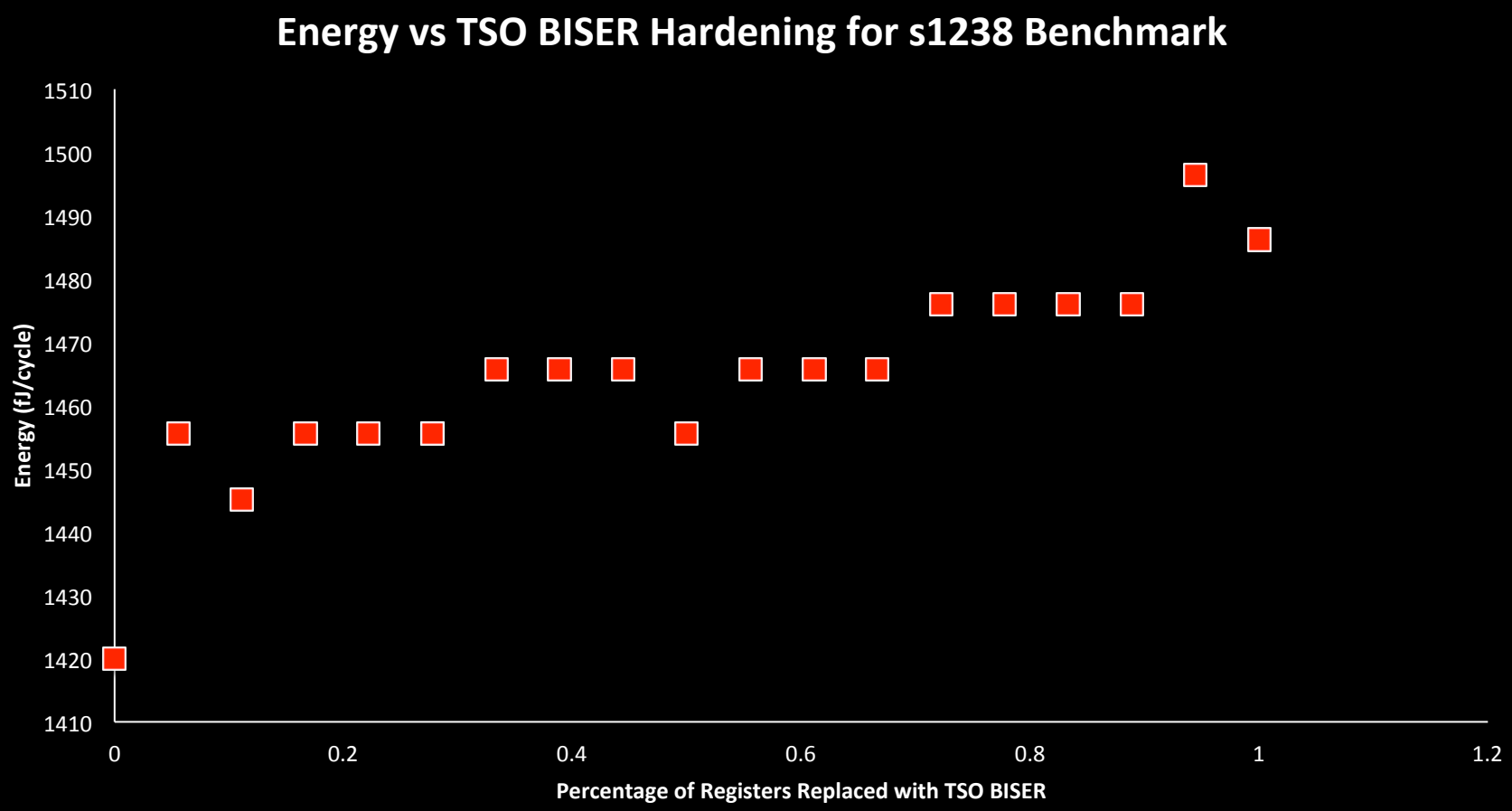

Energy vs FF BISER Hardening for s1238 Benchmark
Energy (fJ/cycle)
1650
1600
1550
1500
1450
1400
0
0.2
0.4
0.6
0.8
1
1.2
Percentage of Registers Replaced with BISER

Results



TSO BISER

Results


Energy vs TSO BISER Hardening for s1238 Benchmark
Energy (fJ/cycle)
1510
1500
1490
1480
1470
1460
1450
1440
1430
1420
1410
0
0.2
0.4
0.6
0.8
1
1.2
Percentage of Registers Replaced with TSO BISER

Retrospection

- Scripting takes a long time
- So does porting code/flows to new technologies
- Learned lots of python
- Learned some basic C++

- Will continue this research next semester
- Future goal: automate design hardening