

Project UPSET: Understanding and Protecting Against Single Event Transients

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Abstract—A particle strike can result in a single-event transient (SET) at a node in circuit logic, which may cause incorrect operation. While much prior work describes and models the nature and effect of SETs, these models largely address errors in bulk technology and are often limited to a single aspect of the circuit hierarchy. We propose to develop and apply models for the effects of SETs in FD-SOI technologies. We will use real technology models for a 28nm process to produce accurate simulation results via HSPICE. By applying the results of our low-level modeling through the design hierarchy, we will be able to accurately estimate chip-level error rates.

I. INTRODUCTION

Reducing the supply voltage of microprocessors also reduces energy, but any circuit requires a minimum operating voltage, V_{min} , to function correctly at a given clock frequency. This V_{min} depends primarily on the critical path delay, but margins are added for noise, temperature, and process variations [1]. In addition, radiation striking a node may induce a glitch, which manifests as a soft error in memory or a voltage pulse in logic [2]. Guaranteeing correct operation requires adding margin for these radiation effects or detecting and correcting them. This project explores appropriate models to simulate soft errors in logic with the goal of reducing or eliminating added margin, allowing for reduced operating power.

Radiation striking a chip typically originates from cosmic rays interacting with atmospheric particles or from radioactive isotopes on the chip's packaging [2]. When these neutrons or alpha particles strike a junction, they generate electron-hole pairs. The electron-hole pairs drift and diffuse at the junction, creating a current. However, the generated electron-hole pairs are quickly used up, so the current simply pulses for a short time [3]. This current charges or discharges the struck node. In memory, if enough charge is moved, the stored bit may flip, producing a single-event upset (SEU). In logic, the current pulse produces a voltage pulse (termed a single-event transient, or SET), which propagates through the logic until it reaches a latch or flip-flop. If the storage element latches the pulse instead of the correct data, the microarchitectural state is corrupted and a datapath SEU occurs [2].

The goal of radiation modeling is to estimate a chip-level soft error rate (SER) for logic or memory. SER is often reported as failures in time (FIT), where 1 FIT means one failure in 10^9 hours. Existing logic SER models can be hierarchically divided into three levels:

- 1) **Device level:** The probability that a certain particle will strike a node and the current/voltage pulse produced at that node.
- 2) **Circuit Level:** The propagation of the voltage pulse through combinational logic and into a latch or flip-flop.
- 3) **Architecture Level:** The effect of an incorrect datapath flip-flop value on the system.

Modeling at each level can be based in simulation or analytical models, or a combination of the two. Simulation-based models are generally more accurate but require a longer runtime than equation-based models. Analytical formulas exist for each of the above levels of hierarchy, and modern CAD tools can simulate each level as well [2][3][4]. Past modeling research has largely focused on bulk CMOS [5]. As the use of FinFET and SOI technologies for arbitrary logic becomes more common, existing models will require modifications to accurately predict logic SER. Predicted SER trends have become obsolete with the advent of multi-core processors in new technologies [6]. These factors have given rise to a need for accurate models of chip-level logic SER in emerging technologies for modern architectures.

In addition to SER models, soft error mitigation, detection, and correction schemes are necessary to ensure correct functionality. In memory, error correcting codes (ECCs) and interleaving protect against SEUs. In logic, SETs and SEUs occur infrequently, but radiation-hardened latches and timing error detection flops can prevent radiation-induced failure. Architectural design decisions may also reduce the impact of SETs.

II. PROBLEM DEFINITION

Despite extensive prior work on SEUs, several fundamental understandings about the impacts of SETs in logic using FD-SOI devices remain unclear. The following are a list of questions that we hope to address with this project:

- How do FD-SOI devices respond to particle strikes? Are they more or less vulnerable to SETs than bulk devices?
- What is the nature of the distribution of current pulses that result from particle strikes? Is this distribution wide or narrow?
- In addition to causing pulses at logic nodes, particle strikes can directly flip storage bits in latches and SRAMs. Some prior research has predicted that the number of soft errors in logic may become comparable to those in memory as scaling decreases device size [6].

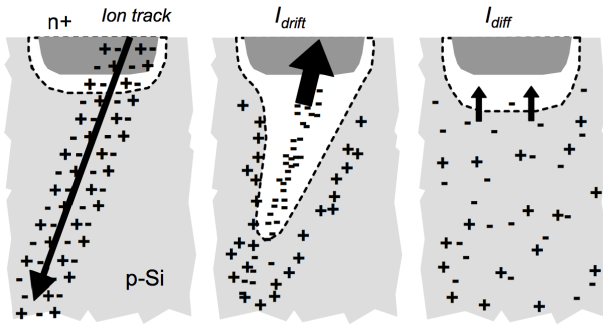


Fig. 1. Charge generation and collection at a junction [2].

What is the relative effect of SEUs caused by SETs in logic as opposed to those caused by direct strikes to memory elements at the 28nm technology node?

- How does the area of a combinational block affect the probability of an SEU at its latched outputs? Are more complex blocks of logic more or less vulnerable to SETs?

Note that we will not address mitigation techniques as they would require a broader project scope than is feasible in the available timeframe.

III. BACKGROUND AND PRIOR WORK

The effects of SETs have been extensively measured and simulated in literature. In this section, we provide an overview of prior work throughout the hierarchy.

A. Device-Level Modeling

Modeling SETs at the device level can be divided into three sub-models. The first model must describe the frequency of various types of radiation strikes. The next must describe the amount of charge imparted by each strike. The third model should detail the nature of the current pulse resulting from this charge.

Several radiation sources are commonly identified as causes of SETs. High-energy neutrons occurring from cascading reactions of cosmic rays and atmospheric particles comprise most soft errors. Additionally, alpha particles generated from lead-based solder in the packaging may affect the SER if such solder is used [2]. However, lead-based solders were phased out to reduce this type of error, so only high-energy neutrons are considered as a SET source. The energies of these neutrons can vary, so the distribution of energies should be considered when calculating the SER. While the neutron fluence (flux integrated over time) depends on location, altitude, and date, average or maximum fluence values may be used instead.

When a particle strikes a junction, it produces a funnel of electron-hole pairs, as seen in Figure 1. These electron-hole pairs drift and diffuse, causing a current pulse. The electric field inherent in reverse-biased junctions separates the charges, spiking the current. Remaining carriers then diffuse, creating a long tail current in the current pulse. These carries may also turn on parasitic BJTs in bulk or PD-SOI devices, amplifying

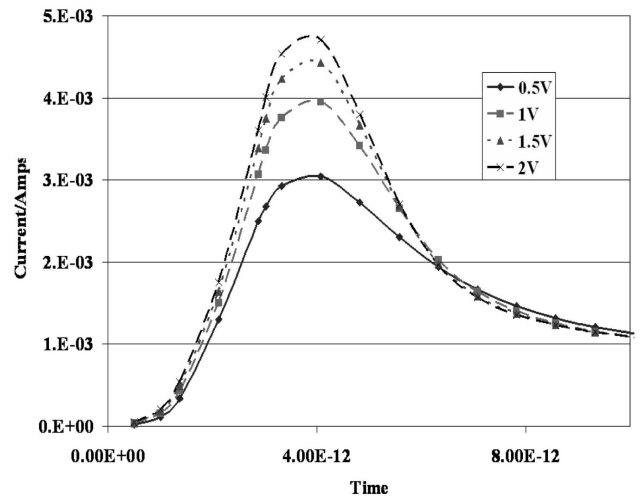


Fig. 2. Measured radiation current pulse waveforms [3]. Note the fast rise and slow fall times of the current pulse.

the collected charge. However, as this is not an issue in FD-SOI devices, we will not consider this effect in our models.

Pulse models use a double exponential to show the fast spike and slow fall of the current pulse [7]:

$$I(t) = \frac{Q_{coll}}{\tau_a - \tau_b} (e^{-\frac{t}{\tau_a}} - e^{-\frac{t}{\tau_b}}), \quad (1)$$

where Q_{coll} contains the total collected charge, and τ_a and τ_b are time constants. All three of these parameters depend on the technology, voltage, circuit, temperature, and particle energy, so each must be characterized for the particular application. Figure 2 exemplifies how a bulk current pulse depends on the node voltage.

General approaches to modeling particle fluence, charge generation, and charge collection rely on simulation using CAD tools. High-energy neutron fluence may be measured directly or calculated through radiation transport codes, such as FLUKA, MCNPx and Geant4 [8][9][10]. Monte Carlo NParticle (MCNP) and nuclear codes have been used to model the interaction of these neutrons with silicon or oxygen [3]. Charge generation and collection typically requires simulation in 3D TCAD tools, such as Synopsys Davinci. Prior work has extensively studied bulk technologies, but models for emerging FD-SOI devices have yet to be addressed thoroughly in the literature.

B. Circuit-Level Modeling

After a particle strike generates a current pulse at a node, a transient voltage pulse propagates through the combinational logic paths following that node. The effects of this pulse in logic are mitigated by three distinct masking effects. A pulse might be logically masked if it does not affect the output of a gate. A simple example of logical masking can be understood by considering a NOR gate with one high input. If the other input pulses temporarily high, the output is not affected and the transient pulse is masked. Electrical masking represents the dampening of a transient pulse due to the electrical properties



Fig. 3. A pulse is electrically masked [6]. The amplitude of the pulse decreases as the signal propagates through subsequent gates.

of the gates along the path (see Figure 3). Latching window masking occurs because a transient pulse in a combinational block only affects the microarchitectural state if the pulse occurs on an input to a sequential logic cell when it is latching the data. As shown in Figure 4, if a pulse reaches a sequential boundary and dissipates before or after the sampling window, the pulse is masked and does not affect the recorded output of the combinational block.

Modeling these effects can be computationally expensive since each effect is data-dependent, and cannot be deduced based on topology alone. Several techniques that improve result turnaround time have been examined. One approach that efficiently models logical masking is the FASER static SER analysis technique proposed in [11]. Fault pulses are encoded and propagated using binary decision diagrams (BDDs), which are part of a data structure that provides an effective way to handle Boolean functions. The tool returns the error rates of the output latches when given a netlist, probability densities of inputs, and collision rates of high-energy particles.

Latching window masking effects are explored in [6]. The proposed model assumes that an error occurs when a faulty pulse is present at the input of a sequential block throughout the entire latching window. The SER is thus determined by the probability that an incident pulse overlaps with a latching window in a given interval of time.

Electrical masking is investigated in [4]. This effect is particularly challenging to verify since oversimplified models fail to incorporate the non-linear gate properties of MOS devices and thus introduce inaccuracies. The approach in [4] analyzes entire blocks of logic rather than particular paths.

The above approaches systematically address each masking effect, reducing simulation time at potential cost to accuracy. A detailed circuit simulation tool such as HSPICE can accurately model all three masking effects.

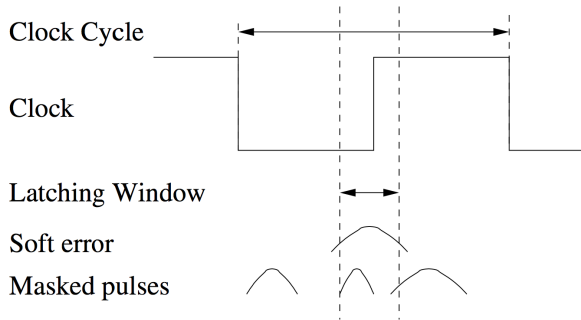


Fig. 4. Latching window masking [6]. Only the center pulse is latched, while the other two pulses are ignored.

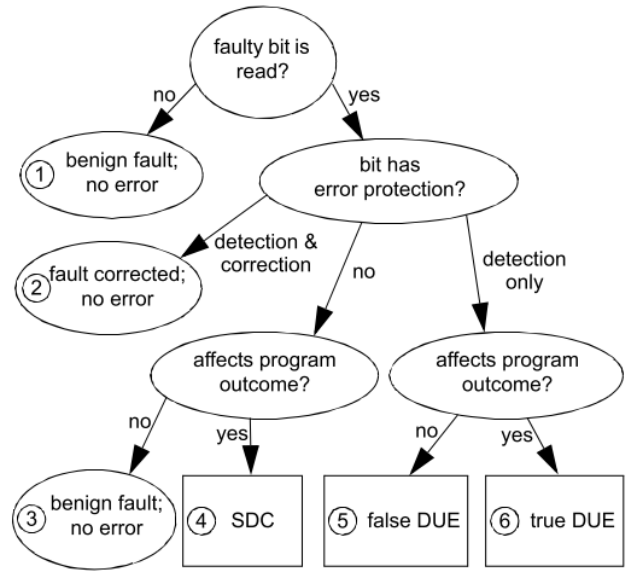


Fig. 5. Possible results of a microarchitectural SEU [12]. Note that only outcomes 4 (Silent Data Corruption) or 6 (true Detected Unrecoverable Errors) result in an error realized at the level of the program outputs.

C. Architectural Modeling

Single-event upsets disturb the microarchitectural state of the system by flipping one or more bits of a register, memory, or other storage element. However, in some cases, an unwanted change in microarchitectural state of a block might not affect the architectural state of the block in a way that is manifested in the output of the hardware. For example, a bit flip in the branch predicting unit of a processor might cause a branch to be taken incorrectly, but this will only cause a minor performance hit as the pipeline is flushed, and will not result in incorrect operation. Figure 5 details possible outcomes of a change in microarchitectural state in a microprocessor, only some of which lead to errors that affect the outcome of the program.

The probability that a change in microarchitectural state of a block will affect the architectural state and hardware outputs is called the *architectural vulnerability factor* (AVF) of the block. The AVF of a block can range from 0 to 1. Blocks such as the program counter, which use nearly all of their microarchitectural state to determine the program output, have very high AVF (near 1), while blocks such as branch predictor units, which generally do not directly contribute to the program output, have very low AVF (near 0). The AVF of each block can be multiplied by the probability of an SEU in each block to determine a chip-level SER. Note that AVF is generally defined for all SEU sources, not just those that result from a SET occurring in logic.

The AVF of each block depends on the microarchitecture of the block, the architecture of the entire system, and the input data to the system, and as such, is difficult to definitively determine. Two broad approaches exist for determining AVF in literature. The first technique is simulation-based, and involves running a performance simulator, randomly injecting faults

into the system, and then comparing the system outputs to a golden model [13]. This technique realistically captures fault propagation, but requires long simulation times and may not capture all possible faults due to its stochastic nature. The second technique tracks the relative importance of all state bits in a block. By determining which bits are required for *architecturally correct execution* (ACE bits), the percentage of bits that are relevant to system execution can be found deterministically [14]. This technique avoids lengthy simulation, but requires detailed knowledge of the function and interaction of all state bits in the block.

Note that even higher levels of abstraction, such as the operating system and software, further mask errors that are realized at the architectural level. Such higher-level considerations are beyond the scope of the project.

IV. PROJECT PROPOSAL

A. Device-Level Modeling

We propose to subsume all charge generation and collection effects into the the current pulse model in (1) and to pre-characterize its parameters for circuit-level use. We will first validate its application in FD-SOI technologies. Then we will characterize its parameters in a 28nm FD-SOI technology for different particle energies, diffusion sizes, temperatures, load capacitances, node voltages, and devices. We will use 3D device simulators to model the effects of these variables. Similar results for bulk devices have been published [3], but the difference in device mechanics and structure between FD-SOI and bulk technologies requires explicit characterization of FD-SOI as well. This database of FD-SOI current pulses will be used in the circuit-level model.

B. Circuit-Level Modeling

Once we have determined the nature and distribution of the current pulses that constitute SETs, we will use HSPICE to simulate the effects of SETs on combinational circuits. Because HSPICE is a full electrical circuit simulator, we expect HSPICE to fully capture the effects of logical masking, electrical masking, and latching window masking, without any of the approximations inherent to algebra-based models. However, the runtime of HSPICE practically limits its use to small combinational blocks, and so other models will be necessary to determine the effect of these results on an entire system.

We will need to determine representative combinational circuits to use in HSPICE. One option is to use "standard" combinational blocks, similar to the technique in [15] of using ISCAS '85 circuits to model SEUs. Another option is to use combinational paths from a synthesized digital block.

C. Architectural Modeling

One weakness of existing methods of determining the impact of SEUs on the system output is that they tend to assume a random distribution of SEUs. While particle strikes are stochastic in nature, we expect to find that different circuits and nodes may be more vulnerable to SEUs than others. We

propose propagating the results of our lower-level model to a fault-injection based simulation of the RTL of a processor element to determine the AVF of the element. By using a fault injection distribution grounded in detailed lower-level modeling, we expect to determine a more realistic AVF than is possible by simple random injection.

V. CONCLUSION

Soft errors in logic represent a major source of uncertainty in modern circuit design, particularly in emerging device technologies such as FD-SOI. Accurate models of SETs at the device, circuit, and architectural level are of critical importance for removing unnecessary margin and reducing operating power. Appropriate models may also facilitate mitigation and correction techniques to reduce the impact of SETs.

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