

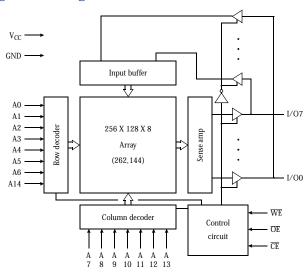
5V/3.3V 32K X 8 CMOS SRAM (Common I/O)

Features

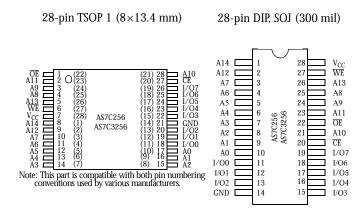
- AS7C256 (5V version)
- AS7C3256 (3.3V version)
- Industrial and commercial temperature
- Organization: $32,768 \text{ words} \times 8 \text{ bits}$
- High speed
 - 12/15/20 ns address access time
 - 6, 7, 8 ns output enable access time
- Very low power consumption: ACTIVE
 - 660mW (AS7C256) / max @ 12 ns
 - 216mW (AS7C3256) / max @ 12 ns

- Very low power consumption: STANDBY
- 22 mW (AS7C256) / max CMOS I/O
- 7.2 mW (AS7C3256) / max CMOS I/O
- Easy memory expansion with \overline{CE} and \overline{OE} inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard packages
- 300 mil PDIP
- 300 mil SOJ
- 8×13.4 mm TSOP 1
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

		-12	-15	-20	Unit
Maximum address access time		12	15	20	ns
Maximum output enable access time		6	7	8	ns
Maximum operating current	AS7C256	120	115	110	mA
Maximum operating current	AS7C3256	60	55	50	mA
Maximum CMOS standby current	AS7C256	4	4	4	mA
Waximum Cwos standby current	AS7C3256	2	2	2	mA



Functional description

The AS7C(3)256 is a 5V/3.3V high-performance CMOS 262,144-bit Static Random-Access Memory (SRAM) device organized as 32,768 words \times 8 bits. It is designed for memory applications requiring fast data access at low voltage, including PentiumTM, PowerPCTM, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters standby mode when CE is high. CMOS standby mode consumes ≤3.6 mW. Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode.

Equal address access and cycle times (t_{AA} , t_{RC} , t_{WC}) of 12/15/20 ns with output enable access times (t_{OE}) of 6, 7, 8 ns are ideal for high-performance applications. The chip enable (\overline{CE}) input permits easy memory expansion with multiple-bank memory organizations.

A write cycle is accomplished by asserting chip enable (\overline{CE}) and write enable (\overline{WE}) LOW. Data on the input pins I/O0-I/O7 is written on the rising edge of \overline{WE} (write cycle 1) or \overline{CE} (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable (\overline{OE}) or write enable (\overline{WE}).

A read cycle is accomplished by asserting chip enable (CE) and output enable (OE) LOW, with write enable (WE) high. The chip drives I/O pins with the data word referenced by the input address. When chip enable or output enable is high, or write enable is low, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible and 5V tolerant. Operation is from a single $3.3\pm0.3V$ supply. The AS7C(3)256A is packaged in high volume industry standard packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V _{CC} relative to GND	AS7C256	V _{t1}	-0.5	+7.0	V
voltage on vec relative to GND	AS7C3256	V _{t1}	-0.5	+5.0	V
Voltage on any pin relative to GND		V _{t2}	-0.5	$V_{CC} + 0.5$	V
Power dissipation		P_{D}		1.0	W
Storage temperature (plastic)		T _{stg}	-65	+150	оС
Ambient temperature with V _{CC} applied		T _{bias}	-55	+125	оС
DC current into outputs (low)		I _{OUT}	-	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

CE	WE	ŌE	Data	Mode
Н	X	X	High Z	Standby (I _{SB} , I _{SB1})
L	Н	Н	High Z	Output disable (I _{CC})
L	Н	L	D _{OUT}	Read (I _{CC})
L	L	X	D _{IN}	Write (I _{CC})

Key: X = Don't care, L = Low, H = High



Recommended operating conditions

Parameter	Device	Symbol	Min	Typical	Max	Unit
Supply voltage	AS7C256	V_{CC}	4.5	5.0	5.5	V
Supply voltage	AS7C3256	V _{CC}	3.0	3.3	3.6	V
	AS7C256	V_{IH}	2.2	_	V _{CC} +0.5	V
Input voltage	AS7C3256	V_{IH}	2.0	_	V _{CC} +0.5	V
	_	${ m V_{IL}}^*$	-0.5*	_	0.8	V
Ambient operating temperature	commercial	T _A	0	_	70	оС
Ambient operating temperature	industrial	T_{A}	-40	-	85	оС

^{*} V_{IL} min = -2.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)¹

				-1	12	-1	15	-2	20	
Parameter	Sym	Test conditions	Device	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	I _{LI}	$V_{CC} = Max,$ $V_{in} = GND \text{ to } V_{CC}$	Both	-	1	-	1	-	1	μA
Output leakage current	I _{LO}	$V_{CC} = Max,$ $V_{OUT} = GND \text{ to } V_{CC}$	Both	-	1	-	1	-	1	μA
Operating	Ţ	$V_{CC} = Max. \overline{CE} \le V_{TI}$	AS7C256	_	120	-	115	1	110	
power supply current	I_{CC}	$\begin{aligned} &V_{CC} = Max, \ \overline{CE} \leq V_{IL} \\ &f = f_{Max}, \ I_{OUT} = 0mA \end{aligned}$	AS7C3256	-	60	_	55	-	50	mA
	I _{SB}	$V_{CC} = Max, \overline{CE} \le V_{IL}$	AS7C256	_	40	_	35	-	30	mA
Standby power	-SB	$f = f_{Max}$, $I_{OUT} = 0mA$	AS7C3256	_	20	_	20	_	20	ША
supply current		$V_{CC} = Max, \overline{CE} \ge V_{CC} - 0.2V$	AS7C256	_	4.0	_	4.0	-	4.0	
	I _{SB1}	$\begin{aligned} V_{IN} &\leq \text{GND} + 0.2 \text{V or} \\ V_{IN} &\geq V_{CC} - 0.2 \text{V, f} = 0 \end{aligned}$	AS7C3256	-	2.0	_	2.0	_	2.0	mA
Output voltage	V_{OL}	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$	Both	_	0.4	_	0.4	1	0.4	V
Output voltage	V_{OH}	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$	Both	2.4	_	2.4	_	2.4	_	V

Capacitance (f = 1MHz, T_a = room temperature, V_{CC} = NOMINAL)²

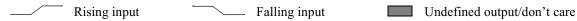
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C _{IN}	A, CE, WE, OE	$V_{in} = 0V$	5	pF
I/O capacitance	C _{I/O}	I/O	$V_{in} = V_{out} = 0V$	7	pF



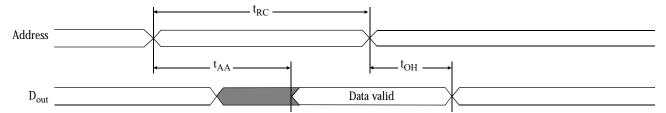
Read cycle (over the operating range)^{3,9}

		-]	12	-]	15	-2	50		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	12	-	15	_	20	_	ns	
Address access time	t _{AA}	-	12	-	15	-	20	ns	3
Chip enable (CE) access time	t _{ACE}	-	12	-	15	-	20	ns	3
Output enable (OE) access time	t _{OE}	_	6	-	7	_	8	ns	
Output hold from address change	t _{OH}	3	_	3	-	3	_	ns	5
CE LOW to output in low Z	t _{CLZ}	3	-	3	-	3	-	ns	4, 5
CE HIGH to output in high Z	t _{CHZ}	_	3	-	4	_	5	ns	4, 5
OE LOW to output in low Z	t _{OLZ}	0	-	0	-	0	-	ns	4, 5
OE HIGH to output in high Z	t _{OHZ}	_	3	-	4	-	5	ns	4, 5
Power up time	t _{PU}	0	-	0	-	0	-	ns	4, 5
Power down time	t _{PD}	-	12	_	15	-	20	ns	4, 5

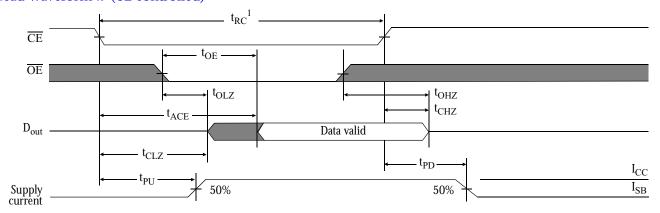
Key to switching waveforms



Read waveform 1 (address controlled)^{3,6,7,9}



Read waveform 2 ($\overline{\text{CE}}$ controlled)^{3,6,8,9}

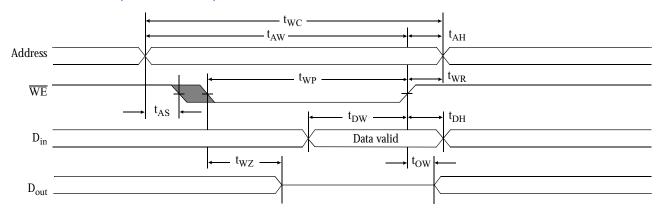




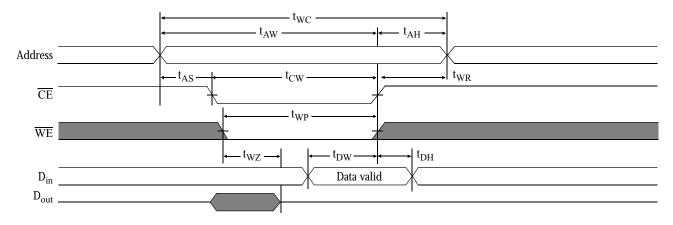
Write cycle (over the operating range) II

		- 1	12	-1	15	-2	20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t _{WC}	12	_	15	-	20	-	ns	
Chip enable to write end	t _{CW}	8	_	10	-	12	-	ns	
Address setup to write end	t _{AW}	8	_	10	-	12	-	ns	
Address setup time	t _{AS}	0	_	0	_	0	_	ns	
Write pulse width	t _{WP}	8	_	9	-	12	-	ns	
Write recovery time	t _{WR}	0	_	0	-	0	-	ns	
Address hold from end of write	t _{AH}	0	-	0	-	0	-	ns	
Data valid to write end	t _{DW}	6	_	8	_	10	_	ns	
Data hold time	t _{DH}	0	_	0	-	0	-	ns	4, 5
Write enable to output in high Z	t _{WZ}	-	5	-	5	_	5	ns	4, 5
Output active from write end	t _{OW}	3	Ī	3	-	3	-	ns	4, 5

Write waveform 1 ($\overline{\text{WE}}$ controlled)^{10,11}



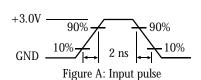
Write waveform 2 ($\overline{\text{CE}}$ controlled)^{10,11}





AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.



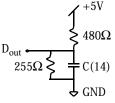


Figure B: Output load

Thevenin equivalent

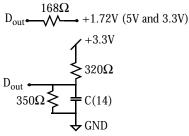
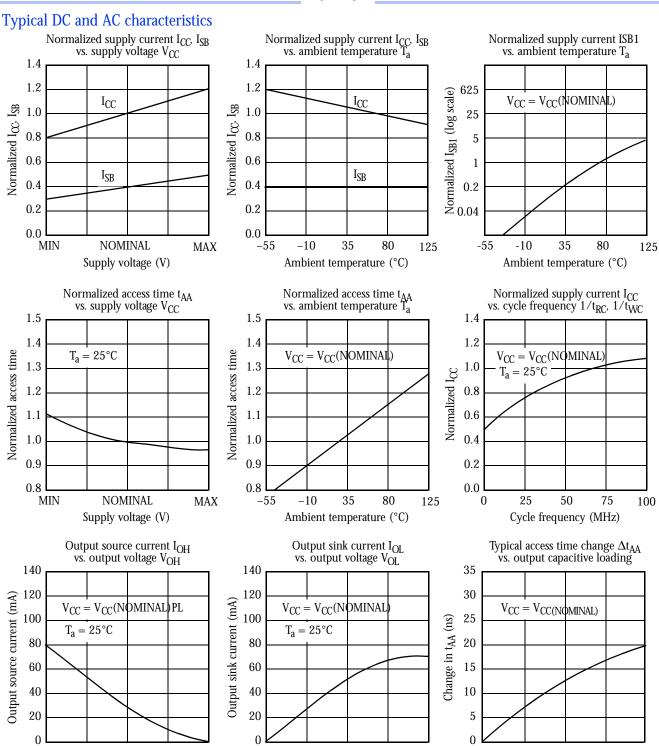


Figure C: Output load

Notes

- 1 During V_{CC} power-up, a pull-up resistor to V_{CC} on \overline{CE} is required to meet I_{SB} specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, C.
- 4 These parameters are specified with CL = 5pF, as in Figures B or C. Transition is measured ±500mV from steady-state voltage.
- 5 This parameter is guaranteed, but not tested.
- 6 WE is High for read cycle.
- 8 Address valid prior to or coincident with $\overline{\text{CE}}$ transition Low.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10 CE or WE must be High during address transitions. Either CE or WE asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12 **CEI** and CE2 have identical timing.
- 13 C=30pF, except on High Z and Low Z parameters, where C=5pF.





Output voltage (V)

 $V_{CC} \\$

250

0

500

Capacitance (pF)

0

Output voltage (V)

 v_{CC}

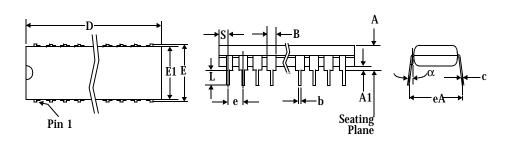
0

750

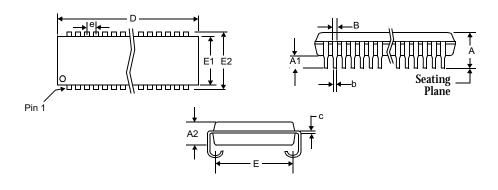
1000

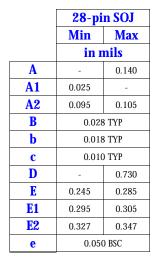


Package diagrams



	28-pin PDIP						
	Min	Max					
	in mils						
A	-	0.175					
A1	0.010	-					
В	0.058	0.064					
b	0.016	0.022					
c	0.008	0.014					
D	-	1.400					
E	0.295	0.320					
E1	0.278	0.298					
e	0.100	O BSC					
eA	0.330	0.370					
L	0.120	0.140					
a	0°	15°					
S	-	0.055					





	c L	$A2^{\uparrow}$ A^{\uparrow} $A1$
D Hd	pin 1(22) pin 8(21) pin 1(7) pin 5(8)	α
<u>'□ </u>	28-pin	
€ ————	Note: This part is compatible with both pin numbering conventions used by various manufacturers.	

	28-pin							
	8×13.4 mm							
	Min Max							
A	-	1.20						
A1	0.10	0.20						
A2	0.95	1.05						
b	0.15	0.25						
c	0.10	0.20						
D	11.60	11.80						
e	0.55 n	ominal						
E	8.0 nc	ominal						
Hd	13.30	13.50						
L	0.50	0.70						
α	0°	5°						



Ordering information

Package / Access time	Volt/Temp	12 ns	15 ns	20 ns
Plastic DIP, 300 mil	5V commercial	AS7C256-12PC	AS7C256-15PC	AS7C256-20PC
Flastic Dir, 300 iiiii	3.3V commercial	AS7C3256-12PC	AS7C3256-15PC	AS7C3256-20PC
	5V commercial	AS7C256-12JC	AS7C256-15JC	AS7C256-20JC
Plastic SOJ, 300 mil	3.3V commercial	AS7C3256-12JC	AS7C3256-15JC	AS7C3256-20JC
Tiastic 303, 300 IIII	5V industrial	AS7C256-12JI	AS7C256-15JI	AS7C256-20JI
	3.3V industrial	AS7C3256-12JI	AS7C3256-15JI	AS7C3256-20JI
	5V commercial	AS7C256-12TC	AS7C256-15TC	AS7C256-20TC
TSOP 8x13.4mm	3.3V commercial	AS7C3256-12TC	AS7C3256-15TC	AS7C3256-20TC
1301 0.13.411111	5V industrial	AS7C256-12TI	AS7C256-15TI	AS7C256-20TI
	3.3V industrial	AS7C3256-12TI	AS7C3256-15TI	AS7C3256-20TI

Part numbering system

AS7C	3	256	-XX	X	C or I
SRAM prefix	Voltage: 3 = 3.3V supply 5 = 5V supply	Device number	Access time	Packages: P = PDIP 300 mil J = SOJ 300 mil T = TSOP 8x13.4mm	Temperature range: C = 0 °C to 70 °C I = -40C to 85C

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