



The  
Programmable  
Logic  
Data Book  
October 1998

Data Book



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# The Programmable Logic Data Book

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United Kingdom Hotline: (44) 1932-820821  
Fax: (44) 1932-828522  
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France Hotline: (33) 1-3463-0100  
Fax: (33) 1-3463-0959  
Email: [frhelp@xilinx.com](mailto:frhelp@xilinx.com)

Germany Hotline: (49) 89-93088-130  
Fax: (49) 89-93088-188  
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Japan Hotline: (81) 3-3297-9163  
Fax: (81) 3-3297-0067  
Email: [jhotline@xilinx.com](mailto:jhotline@xilinx.com)

Korea Hotline: (82) 2-761-4277  
Fax: (82) 2-761-4278  
Email: [korea@xilinx.com](mailto:korea@xilinx.com)

Hong Kong Hotline: (85) 2-2424-5200  
Fax: (85) 2-2424-7159  
Email: [hongkong@xilinx.com](mailto:hongkong@xilinx.com)

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2100 Logic Drive  
San Jose, California 95124  
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On behalf of the employees of Xilinx, our sales representatives, our distributors, and our manufacturing partners, welcome to our 1998 Data Book, and thank you for your interest in Xilinx products and services.

As the inventor of Field Programmable Gate Array technology and the world's leading supplier of programmable logic, we would like to pledge our continuing commitment to providing you, our users, with the best possible integrated circuit components, development systems, and technical and sales support.

Over the past year, we have substantially enhanced our product line with the introduction of the XC4000XL, XC4000XV, and Spartan series of FPGAs, as well as XH3 FpgASIC Hardwire technology. We have continued to enhance our leading-edge products with new speed grades and improved pricing. The Alliance and Foundation series products have set a new standard for functionality and ease-of-use in programmable logic development systems. You can expect this pace of innovation to continue, and even increase, as we maintain our leadership role in bringing leading-edge programmable logic solutions to the market.

We look forward to satisfying all of your programmable logic needs.

Sincerely,

A handwritten signature in black ink that reads "Wim Roelandts".

Wim Roelandts

Chief Executive  
Officer



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November 10, 1997

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## About this Book

This Data Book provides a "snapshot in time" in its listing of IC devices and development system software available from Xilinx as of late 1997. New devices, speed grades, package types and development system products are continually being added to the Xilinx product portfolio. Users are encouraged to contact their local Xilinx sales representative and consult the WebLNX World Wide Web site and the quarterly XCELL newsletter for the latest information regarding new product availability.

This book covers the current XC4000E/EX/XL, XC4000XV, XC4000XLT, Spartan, XC5200, XC3000A/L, XC3100A/L, XC9500, XC1700D/L and XC1701L.

The product specifications for several older Xilinx FPGA families are not included in this Data Book. This does not imply that these products are no longer available. However, for new designs, users are encouraged to use the newer products described in this book, which offer better performance at lower cost than the older technologies. Product specifications for the older products are available at WebLNX, the Xilinx site on the World Wide Web, or through your local Xilinx sales representative.

## Data Sheet Categories

In order to provide the most up-to-date information, some component products included in this book may not have been fully characterized at the time of publication. In these cases, the AC and DC characteristics included in the data sheets will be marked as *Advance* or *Preliminary* information. (Notwithstanding the definitions of such terms, all specifications are subject to change without notice.) These designations have the following meaning:

- **Advance** — Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, but not for final production.
- **Preliminary** — Based on preliminary characterization. Changes are possible, but not expected.
- **Final (unmarked)** — Specifications not identified as either Advance or Preliminary are to be considered final.

## Data Book Contents

**Chapter 1** is a general overview of the Xilinx product line, and is recommended reading for designers who are new to the field of high-density programmable logic.

**Chapter 2** contains a discussion of the overall design methodology when using Xilinx programmable logic and descriptions of Xilinx development system products. This chapter is placed at the beginning of the book since these development tools are needed to design with any of the Xilinx programmable logic devices.

**Chapter 3** contains the product descriptions for the Xilinx Complex Programmable Logic Device (CPLD) products, including the XC9000 series.

**Chapter 4** includes the product descriptions for the Xilinx static-memory-based Field Programmable Gate Array (FPGA) products, including the XC3000, XC4000, XC5000, and Spartan series.

**Chapter 5** holds the product descriptions for the XC1701L and XC1700D families of Serial PROM devices. These Serial PROMs provide a convenient, low-cost means of storing configuration programs for the SRAM-based FPGAs described in Chapter 4.

**Chapter 6** is an overview of Xilinx components appropriate for 3.3 V and mixed-voltage systems. This chapter will refer you back to the appropriate product descriptions in the earlier chapters.

**Chapter 7** contains a brief overview of the HardWire product line. Detailed product specifications are available in separate Xilinx data sheets.

**Chapter 8** is an overview of Xilinx High-Reliability/Military products. Detailed product specifications are available in separate Xilinx data sheets.

**Chapter 9** describes the HW130 device programmer for the XC170X series of Serial PROMs and the XC9500 series of CPLDs.

**Chapter 10** contains a description of all the physical packages for the various IC products, including information about the thermal characteristics of those packages.

**Chapter 11** discusses the testing, quality, and reliability of Xilinx component products.

**Chapter 12** includes a listing of all the technical support facilities provided by Xilinx.

**Chapter 13** contains additional information about Xilinx components that is not provided in the product specifications of the earlier chapters. This includes some additional electrical parameters that are not in the product specifications because they are not part of the manufacturing test program for the particular device, but may be of interest to the user. Also included in this chapter is a discussion of the

JTAG boundary test scan logic found in several Xilinx component families.

The final two sections contain an index to the topics included in this Data Book and a listing of Xilinx sales offices, sales representatives, and distributors.

## About the Company

Xilinx, Inc., offers the industry's broadest selection of programmable logic devices. With 1997 revenues of over \$560 million, Xilinx is the world's largest supplier of programmable logic, and the market leader in Field Programmable Gate Arrays (FPGAs).

Xilinx was founded in 1984, based on the revolutionary idea of combining the logic density and versatility of gate arrays with the time-to-market advantages and convenience of user-programmable standard parts. One year later, Xilinx introduced the world's first Field Programmable Gate Array. Since then, through a combination of architectural and manufacturing process improvements, the company has continually increased device performance, in terms of capacity, speed, and ease-of-use, while lowering costs.

In 1992, Xilinx expanded its product line to include advanced Complex Programmable Logic Devices (CPLDs). For the user, CPLDs are an attractive complement to FPGAs, offering simpler design software and more predictable timing.

As the market leader in one of the fastest growing segments of the semiconductor industry, Xilinx strategy is to focus its resources on creating new ICs and development system software, providing world-class technical support, developing markets, and building a diverse customer base across a broad range of geographic and end-use application segments. The company has avoided the large capital commitment and overhead burden associated with sole ownership and operation of a wafer fabrication facility. Instead, Xilinx has established alliances with several high-volume, state-of-the-art CMOS IC manufacturers. Using standard, high-volume processes assures low manufacturing costs, produces programmable logic devices with well-established reliability, and provides for early access to advances in CMOS processing technology.

Xilinx headquarters are located in San Jose, California. The company markets its products worldwide through a network of direct sales offices, manufacturers' representatives, and distributors (as listed in the back of this book). The company has representatives and distributors in over 38 countries.

## Product Line Overview

Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) can be used in virtually any digital logic system. Over 50 million Xilinx components have been used in a wide variety of end-equipment applications, ranging from supercomputers to hand-held



instruments, from central office switches to centrifuges, and from missile guidance systems to guitar synthesizers.

Xilinx achieved its leading position through a continuing commitment to provide a complete product solution. This encompasses a focus on all three critical areas of the high-density programmable solution "triangle": components (silicon), software, and service (Figure 2).

## Programmable Logic vs. Gate Arrays

Xilinx programmable logic devices provide the benefits of high integration levels without the risks or expenses of semi-custom and custom IC development. Some of the benefits of programmable logic versus mask-programmed gate arrays are briefly discussed below.

### Faster Design and Verification

Xilinx FPGAs and CPLDs can be designed and verified quickly while the same process requires several weeks with gate arrays. There are no non-recurring engineering (NRE) costs, no test vectors to generate, and no delay while waiting for prototypes to be manufactured.

### Design Changes without Penalty

Because the devices are software-configured and user-programmed, modifications are much less risky and can be made anytime - in a manner of minutes or hours, as opposed to the weeks it would take with a gate array. This results in significant cost savings in design and production.

### Shortest Time-to-Market

When designing with Xilinx programmable logic, time-to-market is measured in days or a few weeks, not the months often required when using gate arrays. A study by market research firm McKinsey & Co. concluded that a six-month delay in getting to market can cost a product

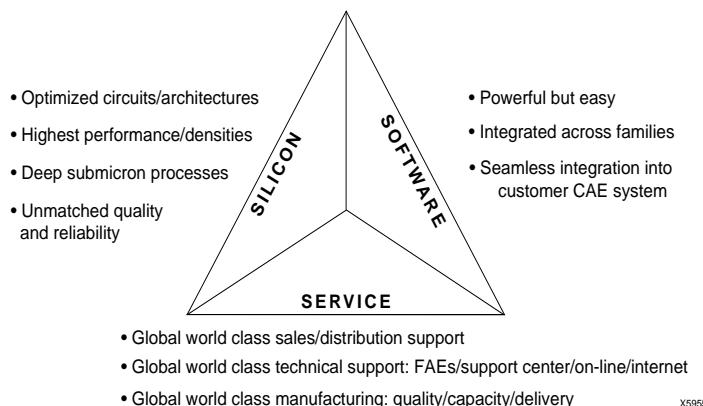
one-third of its lifetime potential profit. With mask-programmed gate arrays, design iterations can easily add that much time, and more, to a product schedule.

Once the decision has been made to use Xilinx programmable logic, a choice must be made from a number of product families, device options, and product types. The information in the product selection matrices that follow can help guide that selection; detailed product specifications are available in subsequent chapters of this book. Since many component products are available in common packages with common footprints, designs often can be migrated to higher or lower density devices, or even across some product families, without any printed circuit board changes. Design ideas, represented in text or schematic format, are converted into a configuration data file for an FPGA or CPLD device using the Xilinx XACTstep development software running on a PC or workstation.

## Component Products

Xilinx offers the broadest line of programmable logic devices available today, with hundreds of products featuring various combinations of architectures, logic densities, package types, and speed grades in commercial, industrial, and military grades. This breadth of product offerings allows the selection of the programmable logic device that is best suited for the target application.

Xilinx programmable logic offerings include several families of reprogrammable FPGAs and FLASH-memory-based CPLDs (Figure 3). HardWire devices are mask-programmed versions of the reprogrammable FPGAs, and provide a transparent, no-risk migration path to lower-cost devices for high-volume, stable designs. Additionally, a family of Serial PROM devices is available to store configuration programs for the reprogrammable FPGA devices. Many devices are available in military temperature range



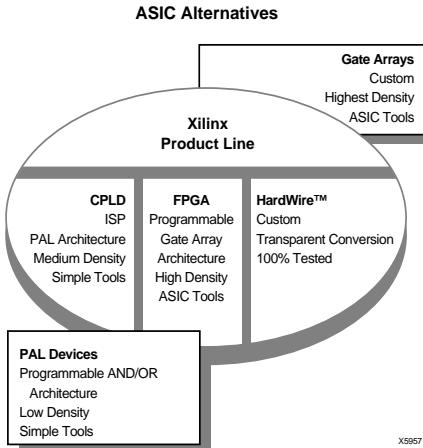
**Figure 2: The Xilinx Programmable Solution Triangle**

and/or MIL-STD-883B versions, for high-reliability and military applications.

### Field Programmable Gate Arrays (FPGAs)

FPGA devices feature a gate-array-like architecture, with a matrix of logic cells surrounded by a periphery of I/O cells, as diagrammed in [Figure 4](#). Segments of metal interconnect can be linked in an arbitrary manner by programmable switches to form the desired signal nets between the cells.

FPGAs combine an abundance of logic gates, registers, and I/Os with fast system speed. Xilinx offers several families of reprogrammable, static-memory-based (SRAM-based) FPGAs, including the XC3000, XC4000, XC5000, and XC6000 series.



**Figure 3:** Application-Specific IC Products

### Complex Programmable Logic Devices (CPLDs)

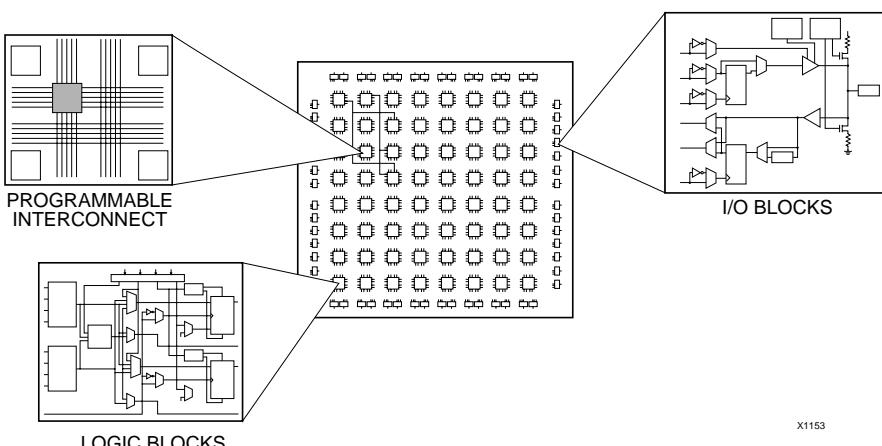
Designers more comfortable with the speed, design simplicity, and predictability of PALs may prefer CPLD devices. Conceptually, CPLDs consist of multiple PAL-like function blocks that can be interconnected through a switch matrix ([Figure 5](#)). The XC9000 CPLD series features 5V in-system programmable FLASH technology, and, like most of the FPGA families, includes built-in JTAG boundary scan test logic.

### HardWire devices

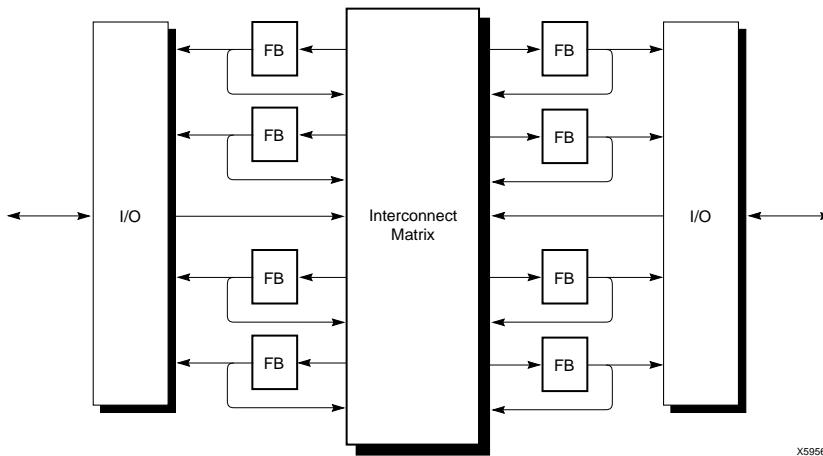
HardWire devices are masked-programmed versions of the SRAM-based FPGAs. The HardWire products provide an easy, transparent migration path to a cost-reduced device without the engineering burden associated with conventional gate array re-design. The HardWire gate array is architecturally identical to its FPGA counterpart, but the programmable elements in the FPGA are replaced with fixed metal connections. The resulting die is considerably smaller, with a correspondingly lower cost. Using proprietary automatic test vector generation software and patented test logic, Xilinx guarantees over 95% fault coverage, while eliminating the need for user-generated test vectors. The mask and test programs are generated automatically by Xilinx from the user's existing FPGA design file.

### Serial PROMs

The XC1700 family features one-time programmable serial PROMs ranging in density from about 18,000 bits to over 260,000 bits. These serial PROMs are an easy-to-use, cost-effective method for storing configuration data for the SRAM-based FPGAs.



**Figure 4:** FPGA Architecture



X5956

**Figure 5: CPLD Architecture**

### High-Reliability Devices

Xilinx was the first company to offer high-reliability FPGAs by introducing MIL-STD-883B qualified XC2000 and XC3000 series devices in 1989. MIL-STD-883B members of the XC4000 FPGA series are currently available, and qualified versions of additional Xilinx families are in development. The product line also includes Standard Microcircuit Drawing (SMD) versions of several families. Some Xilinx devices are available in tested die form through arrangements with manufacturing partners.

### Development System Products

Xilinx offers a complete software environment for the implementation of logic designs in Xilinx programmable logic devices. This environment combines powerful technology with a flexible, easy-to-use graphical interface to help users achieve the best possible designs, regardless of experience level. The user has a wide range of choices between a fully-automatic implementation and detailed involvement in the layout process. The development system provides all the implementation tools required to design with Xilinx logic devices, including the following:

- libraries and interfaces for popular schematic editors, logic synthesis tools, and simulators
- design manager/flow engine
- module generator
- map, place, and route compilation software
- static timing analyzer
- hardware debugger

Xilinx is committed to an "open system" approach to front-end design creation, synthesis, and verification. Xilinx devices are supported by the broadest number of EDA vendors and synthesis vendors in the industry. Supported plat-

forms include the ubiquitous PC and several popular workstations.

### Technical Support and Service

Providing global, world-class manufacturing, technical support, and sales/distribution support is an essential foundation of the Xilinx product strategy. Xilinx manufacturing facilities have earned ISO9002 certification, and Xilinx quality and reliability achievements are among the world's best - not just for programmable logic suppliers, but among all semiconductor companies. Comprehensive technical support facilities include training courses, extensive product documentation and application notes, a quarterly technical newsletter, the WebLINX World Wide Web site, technical support hotlines, and a cadre of Field Application Engineers. Sales support is provided by a worldwide network of representatives and distributors.

**XC3000 Series Product Selection Matrix**

		XC3000 Series													
FEATURES DENSITY	KEY FEATURES	Low Cost/ Low Power					High Performance					Low Voltage (3.3 V) High Performance			
		Max Logic Gates (K)	1.5	2	3	4.5	6	1.5	2	3	4.5	6	7.5	3	6
		Max RAM Bits	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
		Typical Gate Range (K)	1.1-5	1.5-2	2-3	3.5-4.5	5-6	1.1-5	1.5-2	2-3	3.5-4.5	5-6	6.5-7.5	2-3	5-6
		CLBs	64	100	144	224	320	64	100	144	224	320	484	144	320
		Flip-Flops	256	360	480	688	928	256	360	480	688	928	1320	480	928
		Output Drive (mA)	4	4	4	4	4	8	8	8	8	8	8	4	4
		JTAG (IEEE 1149.1)	N	N	N	N	N	N	N	N	N	N	N	N	N
		Dedicated Arithmetic	N	N	N	N	N	N	N	N	N	N	N	N	N
		Quiescent Current (mA)	0.5/0.02	0.5/0.02	0.5/0.02	0.5/0.02	0.5/0.02	8	8	8	8	8	1.5	1.5	1.5
		Fastest Speed Grade	-6/-8	-6/-8	-6/-8	-6/-8	-6/-8	-09	-09	-09	-09	-09	-09	-2	-2

**XC4000 Series Product Selection Matrix**

		XC4000 Series														
FEATURES DENSITY	KEY FEATURES	High Density High Performance Select-RAM™ Memory														
		System Gate Range* (Logic and RAM) (K)	2-5	3-9	4-12	6-15	7-20	10-30	13-40	15-45	18-50	22-65	27-80	33-100	40-130	55-180
		Logic Cells	238	466	608	770	950	1368	1862	2432	2432	3078	3800	4598	5472	7448
		Max Logic Gates, (no RAM) (K)	3	5	6	8	10	13	20	25	28	36	44	52	62	85
		Max RAM Bits (no Logic)	3200	6272	8192	10368	12800	18432	25088	32768	32768	41472	51200	61952	73728	100352
		CLBs	100	196	256	324	400	576	784	1024	1024	1296	1600	1936	2304	3136
		Flip-Flops	360	616	768	936	1120	1536	2016	2560	2560	3168	3840	4576	5376	7168
		Output Drive (mA)	12	12	12	12	12	12	12	12	12	12	12	12	12	12
		JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Dedicated Arithmetic	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Quiescent Current (mA)	10	10	10	10	10	10	10	10	10	10	10	10	10	10
		Fastest Speed Grade	-1	-09	-1	-1	-09	-09	-09	-1	-09	-09	-09	-09	-09	-09

\*Maximum System gates assume 20% of CLBs used as RAM

## Spartan Series Product Selection Matrix

KEY FEATURES	Spartan Series	XCS05 XCS05-XL	XCS10 XCS10-XL	XCS20 XCS20-XL	XCS30 XCS30-XL	XCS40 XCS40-XL
KEY FEATURES		High Density High Performance Select-RAM™ Memory Low Cost				
DENSITY	System Gate Range* (Logic and RAM) (K)	2-5	3-10	7-20	10-30	13-40
	Logic Cells	238	466	950	1368	1862
	Max Logic Gates, (no RAM) (K)	3	5	10	13	20
	Max RAM Bits (no Logic)	3200	6272	12800	18432	25088
	CLBs	100	196	400	576	784
	Flip-Flops	360	616	1120	1536	2016
FEATURES	Output Drive (mA)	12	12	12	12	12
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y
	Dedicated Arithmetic	Y	Y	Y	Y	Y
	Quiescent Current (mA)	3	3	3	3	3
	Fastest Speed Grade	-4	-4	-4	-4	-4

\*Maximum System gates assume 20% of CLBs used as RAM

## XC5200 Series Product Selection Matrix

KEY FEATURES	XC5200 Series	XC5202	XC5204	XC5206	XC5210	XC5215
KEY FEATURES		High Density Low Cost				
DENSITY	Max Logic Gates (K)	3	6	10	16	23
	Max RAM Bits	N/A	N/A	N/A	N/A	N/A
	Typical Gate Range (K)	2-3	4-6	6-10	10-16	15-23
	CLBs/Logic Cells	64	120	196	324	484
	Flip-Flops	256	480	784	1296	1936
	Output Drive (mA)	8	8	8	8	8
FEATURES	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y
	Dedicated Arithmetic	Y	Y	Y	Y	Y
	Quiescent Current (mA)	15	15	15	15	15
	Fastest Speed Grade	-3	-3	-3	-3	-3

**XC9500 Series Product Selection Matrix**

KEY FEATURES / DEVICES	CPLD Families	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
KEY FEATURES		JTAG 5 V ISP 3 V or 5 V I/O					
DENSITY FEATURES	Gates (K)	0.8	1.6	2.4	3.2	4.8	6.4
	Macrocells	36	72	108	144	216	288
	Flip-Flops	36	72	108	144	216	288
	Output Drive (mA)	24	24	24	24	24	24
	JTAG (IEEE 1149.1)	Y	Y	Y	Y	Y	Y
	Dedicated Arithmetic	N	N	N	N	N	N
	Quiescent Current (mA)	—	—	140	—	—	—
	Fastest Speed Grade	-5	-7	-7	-7	-10	-10



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March 24, 1998 (Version 2.0)

### Product Overview

## Introduction

Leading-edge silicon products, state-of-the art software solutions and world-class technical support make up the total solution delivered by Xilinx. The software component of this solution is critical to the success of every design project. Xilinx Software Solutions provide powerful tools which make designing with programmable logic simple. Push button design flows, integrated on-line help, multimedia tutorials, plus high performance automatic and auto-interactive tools, help designers achieve optimum results. And the industry's broadest array of programmable logic technology and EDA integration options deliver unparalleled design flexibility.

## Product Overview

Xilinx Software Solutions are available in two different product series making it easy for designers to choose the right system for their needs. These two series support the industry's broadest array of programmable logic IC families. This allows users to standardize their design tools for all programmable logic applications and use these tools to realize the benefits of the industry's highest performance and density FPGAs and CPLDs. It also makes it easy to migrate designs to new technologies and re-use existing designs in new applications.

The **Xilinx Foundation Series** provides designers with a complete, ready-to-use solution for programmable logic design.

The **Xilinx Alliance Series** provides designers powerful integration of Xilinx design tools with their existing EDA environment.

## Flexible Configurations

Xilinx Software Solutions are available in two device configurations giving designers a cost-effective way to match their tools to the design methodologies they require. These configurations are available for both the Foundation and Alliance Series.

- Base configurations provide push button design flows and support a broad array of FPGA and CPLD devices targeted for low density and high volume applications.
- Standard configurations combine push button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation. Standard configurations include support for

all Xilinx programmable logic devices, featuring the industry's largest FPGA devices.

## Foundation Series

The Xilinx Foundation Series provides everything required to design a programmable logic device in an easy-to-use environment. This fully integrated tool set allows users to access design entry, synthesis, implementation and simulation tools in a ready-to-use package. Every step in the design process is accomplished using graphical tool bars, icons and pop-up menus supported by interactive tutorials and comprehensive on-line help.

The Xilinx Foundation Series features support for standards based HDL design. All configurations support the popular ABEL language, with integrated compilers optimized for each target architecture. HDL configurations include integrated VHDL/Verilog synthesis from Synopsys with tutorials and graphical HDL design entry tools to turn new users into experts quickly and easily.

## HDL Configurations

HDL configurations of the Foundation Series contain integrated VHDL/Verilog synthesis and graphical interactive HDL entry tools with the following features:

- On-line tutorial teaches the art of VHDL design.
- Xilinx HDL Editor provides color coding, syntax checking and single click error navigation making it easy to create and debug VHDL, Verilog and ABEL designs.
- Graphical State Machine editor makes the design of simple or complex state machines simple and intuitive.
- HDL Language Assistant provides libraries of common functions with optimized VHDL, Verilog and ABEL code.
- FPGA and CPLD specific synthesis and optimization from Synopsys tools produce high-utilization, high-performance results

## Alliance Series

The Alliance Series provides powerful and integrated design tools for users who require a quality solution for their chosen EDA design solution. With the Alliance Series, users can choose from a wide range of design techniques including schematic capture, module-based design and HDL design solutions. With standard based design interfaces including EDIF, VITAL, VHDL, Verilog and SDF, this series provides maximum flexibility, portability, mixed vendor support, and design reuse.

Quality integration with leading EDA vendors such as ALDEC, Exemplar, Cadence, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest and VIEWlogic provide tightly-coupled environments that make it easy to move through the design process and through a mixed EDA vendor flow. The EDA vendors are supported through the Xilinx Alliance Program, insuring high quality tools and accuracy of results. Information on Xilinx Alliance Program vendors can be found on the Xilinx WEB page [www.xilinx.com](http://www.xilinx.com).

The Alliance Series includes an enhanced set of easy-to-use features including, design manager, flow engine, installation, on-line documentation, and answer database. In addition, the Alliance Series includes a powerful and complete implementation toolset, LogiBLOX (next generation module generation), fully integrated EDA vendor support, and a powerful gate-level optimizer. Also included are new advanced place and route software that has incremental design capabilities and SMARTspecs (a robust timing constraint language). Users can achieve up to 25% performance improvements with no additional elapse time through the use of the Alliance Series Turns Engine. The Turns Engine uses networked workstations to run multiple place and route passes for a single design. This feature is included with the Alliance Series BASE and Standard workstation development systems. The libraries and interface provide Xilinx Unified Library schematic symbols, HDL synthesis libraries, VITAL(VHDL) and Verilog simulation models with timing information and translators through a standard netlist format. All of these tools provide a complete spectrum of high density design methodologies from fully-automatic to hand-crafted and close integration with Xilinx LogiCores and AllianceCore partners.

## **Alliance Series Options**

VIEWlogic Workview Office Development System options as part of the Alliance Series are intended for users who want the integration of a complete solution with the power to access board and system level design tools. These products include VIEWlogic Workview Office schematic capture and simulation tools.

## **Xilinx M1 Software Technology**

M1 technology represents Xilinx's next generation software technology. This advanced technology developed as a result of the Xilinx merger with NeoCAD Inc., enables digital system designers to increase design performance, leverage standards-based, high-level design methodologies and quickly receive new software features and device support through Xilinx Foundation Series and Alliance Series software solutions.

## **Increased Design Performance**

The M1 technology provides dramatically improved design performance through advanced place-and-route software

which delivers push-button design flows and incremental design capabilities. These Xilinx-exclusive capabilities leverage results from previous design iterations to reduce runtimes and shorter design iterations to less than ten minutes. As engineers design complex circuits incrementally, this technology allows them to work in their preferred methodology.

M1 Technology also delivers advanced timing driven place-and route capabilities to deliver maximum design performance through push-button flows.

## **M1 Technical Benefits**

### **Maximum Design Performance**

M1 technology enables the user to achieve maximum design performance by providing a unique combination of advanced algorithms and interactive tools. Designer productivity is greatly enhanced through use of simple, push-button flows and optional auto-interactive tools. Customer testing has shown that M1 technology used with XC4000XL/XV devices results in 70 percent shorter run times, up to a 25 percent performance improvement, and the ability to place and route devices with up to 100 percent utilization with a push-button flow.

### **Modular Software System**

The modular architecture of the Xilinx M1 technology allows rapid delivery of incremental technologies, new features, device support, and versions of its leading software product families. New feature sets can now be released independently resulting in users' ability to quickly complete designs without having to re-learn new tools as enhancements are made. The investment Xilinx has made in the M1 technology ensures that the continuous delivery of innovative device architectures and improved software solutions can be done more rapidly, and predictably than previous software versions.

### **Methodology Flexibility**

High-level design methodologies are becoming the methodology choice for the design of complex programmable logic. M1 technology delivers programmable logic specific high-level flows. The flows provide high-quality, high performance optimized results, and afford fast, flexible design changes and iterations to match the way engineers design. Designers employ a mixture of graphical and language-based design entry methods while providing an easy-to-learn environment for Hardware Description Language (HDL) based design. Xilinx recognizes that design environments are variant and, therefore, has created a flexible system enabling the customer to choose the best methodology for their environment or design challenge.



## Development Systems: Product Descriptions

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November 25, 1997 (Version 2.0)

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### Development Systems Descriptions

It's simple to order a Xilinx Development System. Just choose a Foundation or Alliance Series and a few options. Give your local Xilinx Sales Office a call for information about our evaluation kits.

#### Foundation Series

- Foundation Base System (PC)
- Foundation Base-Express System (PC)
- Foundation Standard System (PC)
- Foundation Express System (PC)

#### Alliance Series

- Alliance Base (PC or Workstation)
- Alliance Standard (PC or Workstation)

#### Alliance Series Options

- VIEWlogic Workview Office Standard Development System Options (PC)

## Foundation Series: Foundation Base System (PC)

### Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Base System provides design entry (schematic and Abel HDL), simulation, and device implementation tools for a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

### System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for the Abel 6 HDL
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

### Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

### Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements: 32 MB RAM, 32-64 MB Virtual Memory
- CD-ROM drive

### Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	✓	✓	✓	✓
FPGA Devices	✓ <sup>1</sup>	✓	✓ <sup>1</sup>	✓
Libraries and Interface	✓	✓	✓	✓
Schematic Editor	✓	✓	✓	✓
HDL Editor	✓	✓	✓	✓
Graphical State Editor	✓	✓	✓	✓
ABEL 6 Entry / Synthesis	✓	✓	✓	✓
VHDL Entry / Synthesis			✓	✓
Verilog Entry / Synthesis			✓	✓
Schematic-centric Synthesis	✓	✓	✓	✓
HDL-centric Synthesis				✓
Simulator	✓	✓	✓	✓
Device Implementation	✓	✓	✓	✓
Maintenance <sup>2</sup>	✓	✓	✓	✓

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Notes: 1. Spartan, XC3x00A/X, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.  
 2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

## Foundation Series: Foundation Base-Express System with VHDL/Verilog Synthesis (PC)

### Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Express System incorporates advanced synthesis technology from Synopsys, and provides design entry (schematic and HDL), VHDL and Verilog synthesis, simulation, and device implementation tools for a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

### System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for VHDL, Verilog, and Abel 6 HDL
- VHDL and Verilog synthesis, including compilation and optimization
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

### Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

### Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements: 32 MB RAM, 32-64 MB Virtual Memory
- CD-ROM drive

### Package Features - Foundation Base-Express System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	√	√	√	√
FPGA Devices	√ <sup>1</sup>	√	√ <sup>1</sup>	√
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
HDL Editor	√	√	√	√
Graphical State Editor	√	√	√	√
ABEL 6 Entry / Synthesis	√	√	√	√
VHDL Entry / Synthesis			√	√
Verilog Entry / Synthesis			√	√
Schematic-centric Synthesis	√	√	√	√
HDL-centric Synthesis				√
Simulator	√	√	√	√
Device Implementation	√	√	√	√
Maintenance <sup>2</sup>	√	√	√	√

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Notes:

1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

## Foundation Series: Foundation Standard System (PC)

### Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Standard System provides design entry (schematic and Abel HDL), simulation, and device implementation tools for all Xilinx CPLDs and Xilinx FPGAs.

### System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for the Abel 6 HDL
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

### Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

### Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements
  - Small Devices (< 10K gates): 32 MB RAM, 32-64 MB Virtual Memory
  - Medium Devices (10K to 30K gates): 64 MB RAM, 64-128 MB Virtual Memory
  - Large Devices (> 30K gates): 128 MB RAM, 128-256 MB Virtual Memory
- CD-ROM drive

### Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	✓	✓	✓	✓
FPGA Devices	✓ <sup>1</sup>	✓	✓ <sup>1</sup>	✓
Libraries and Interface	✓	✓	✓	✓
Schematic Editor	✓	✓	✓	✓
HDL Editor	✓	✓	✓	✓
Graphical State Editor	✓	✓	✓	✓
ABEL 6 Entry / Synthesis	✓	✓	✓	✓
VHDL Entry / Synthesis			✓	✓
Verilog Entry / Synthesis			✓	✓
Schematic-centric Synthesis	✓	✓	✓	✓
HDL-centric Synthesis				✓
Simulator	✓	✓	✓	✓
Device Implementation	✓	✓	✓	✓
Maintenance <sup>2</sup>	✓	✓	✓	✓

11/12/97

Notes: 1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.  
 2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

## Foundation Series: Foundation Express System (PC)

### Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Express System incorporates advanced synthesis technology from Synopsys, and provides design entry (schematic and HDL), VHDL and Verilog synthesis, simulation, and device implementation tools for all Xilinx CPLDs and Xilinx FPGAs.

### System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for VHDL, Verilog, and Abel 6 HDL
- VHDL and Verilog synthesis, including compilation and optimization
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

### Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

### Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements
  - Small Devices (< 10K gates): 32 MB RAM, 32-64 MB Virtual Memory
  - Medium Devices (10K to 30K gates): 64 MB RAM, 64-128 MB Virtual Memory
  - Large Devices (> 30K gates): 128 MB RAM, 128-256 MB Virtual Memory
- CD-ROM drive

### Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	✓	✓	✓	✓
FPGA Devices	✓ <sup>1</sup>	✓	✓ <sup>1</sup>	✓
Libraries and Interface	✓	✓	✓	✓
Schematic Editor	✓	✓	✓	✓
HDL Editor	✓	✓	✓	✓
Graphical State Editor	✓	✓	✓	✓
ABEL 6 Entry / Synthesis	✓	✓	✓	✓
VHDL Entry / Synthesis			✓	✓
Verilog Entry / Synthesis			✓	✓
Schematic-centric Synthesis	✓	✓	✓	✓
HDL-centric Synthesis				✓
Simulator	✓	✓	✓	✓
Device Implementation	✓	✓	✓	✓
Maintenance <sup>2</sup>	✓	✓	✓	✓

11/12/97

Notes:

1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

## Alliance Series: Alliance Base (PC or Workstation)

### Overview

Next generation FPGA/CPLD design solutions leveraging "Open Systems" integration with premier EDA partners for devices up to 10,000 gates.

### Base System Features:

- EDA Libraries & Interfaces
- Design Manager and Flow Engine
- LogiBLOX Module Generator
- Gate Optimizer
- Complete HDL design methodology support
- Incremental design capabilities
- Place and route utilizing SMARTspecs
- Re-entrant router
- Multi-pass PAR
- Timing Analyzer
- Standard netlist and backannotation (EDIF, SDF, VITAL VHDL and Verilog)
- Xchecker Hardware Debugger (workstation only)

### Package Includes:

- Alliance Quick Start Guide
- Alliance Release Document
- Answer Database
- Core Technology CD
- CAE Libraries CD
- On-line Documentation CD with DynaText browser
- Hardware Cable
- Demoboard

### Device Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

### Libraries and Interfaces

#### Cadence

- Concept schematic libraries and Verilog-XL simulation models

#### Mentor

- Falcon Framework schematic capture library and ModelSim simulation models
- Leonardo synthesis libraries and interfaces are available from Mentor or Exemplar Logic

#### Synopsys

- HDL Design Solutions (VHDL and Verilog)
- Design Compiler, FPGA Compiler II, FPGA Express, VSS
- Vital Simulation models
- DesignWare arithmetic modules
- \* No libraries required to support FPGA Express

#### VIEWlogic

- Workview Office schematic capture library and functional and timing simulation interface

#### Exemplar

- Leonardo and Galileo synthesis libraries and interfaces are available from Exemplar Logic

#### Symplicity

- Synplify synthesis libraries and interfaces are available from Symplicity

#### Model Technology

- ModelSim, V-System HDL simulation libraries and interface

Contact your local EDA sales office to purchase these EDA tools.

### Support and Updates Include:

- Answers Database - <http://www.xilinx.com> or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes
- Software Updates (for in-maintenance customers)
  - A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information

## Required Hardware Environment (PC)

- Fully IBM compatible PC486/Pentium
  - NEC98 supported
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 300 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- 32 MB RAM (Use additional RAM to increase performance)
- 32 MB - 64 MB Virtual Memory

## Required Hardware Environment (Workstation)

- Ultra Sparc (or equivalent)
  - Sun OS 4.1.3 and 4.1.4
  - Solaris 2.5
- HP715 (or equivalent)
  - HP-UX 10.2
- RS6000
  - AIX 4.1.5 (no GUIs)
- 64 MB RAM (Use additional to increase performance)
- 64MB min Swap Space
- Color Monitor

## Alliance Series: Alliance Standard (PC or Workstation)

### Overview

Next generation FPGA/CPLD design solutions leveraging "Open Systems" integration with premier EDA partners for unlimited gate capacity.

### Base System Features:

- EDA Libraries & Interfaces
- Design Manager and Flow Engine
- LogiBLOX Module Generator
- Gate Optimizer
- Full HDL design methodology support
- Incremental design capabilities
- Place and route utilizing SMARTspecs
- Re-entrant router
- Multi-pass PAR
- Timing Analyzer
- Standard netlist and backannotation (EDIF, SDF, VITAL VHDL and Verilog)
- Xchecker Hardware Debugger (workstation only)

### Package Includes:

- Alliance Quick Start Guide
- Alliance Release Document
- Answer Database
- Core Technology CD
- CAE Libraries CD
- On-line Documentation CD with DynaText browser
- Hardware Cable
- Demoboard

### Device Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

### Libraries and Interfaces

#### **Cadence**

- Concept schematic libraries and Verilog-XL simulation models

#### **Mentor**

- Falcon Framework schematic capture library and ModelSim simulation models
- Leonardo synthesis libraries and interfaces are available from Mentor or Exemplar Logic

#### **Synopsys**

- HDL Design Solutions (VHDL and Verilog)
- Design Compiler, FPGA Compiler II, FPGA Express, VSS
- Vital Simulation models
- DesignWare arithmetic modules
- \* No libraries required to support FPGA Express

#### **VIEWlogic**

- Workview Office schematic capture library and functional and timing simulation interface

#### **Exemplar**

- Leonardo and Galileo synthesis libraries and interfaces are available from Exemplar Logic

#### **Symplicity**

- Synplify synthesis libraries and interfaces are available from Symplicity

#### **Model Technology**

- ModelSim, V-System HDL simulation libraries and interface

Contact your local EDA sales office to purchase these EDA tools.

### Support and Updates Include:

- Answers Database - <http://www.xilinx.com> or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes
- Software Updates (for in-maintenance customers)
  - A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information

## Required Hardware Environment (PC)

- Fully IBM compatible PC486/Pentium
  - NEC98 supported
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 300 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- Small Devices: (8K or <) XC9536 - XC95108; XC4003E - XC4008E; XC4005XL - XC4008XL
  - 32 MB RAM (Use additional RAM to increase performance)
  - 32 -64 MB Virtual Memory
- Medium Devices: (10K- 28K) XC95144 - XC95216; XC4010E - XC4025E; XC4028EX - XC4036EX; XC4010XL - XC4028XL
  - 64 MB RAM (Use additional RAM to increase performance)
  - 64-128 MB Virtual Memory
- Large Devices: (36K or >) XC4036XL - XC4062XL
  - 128K RAM (Use additional RAM to increase performance)
  - 128 - 256 MB Virtual Memory

## Required Hardware Environment (Workstation)

- Ultra Sparc (or equivalent)
  - Sun OS 4.1.3 and 4.1.4
  - Solaris 2.5
- HP715 (or equivalent)
  - HP-UX 10.2
- RS6000
  - AIX 4.1.5 (no GUIs)
- Small Devices: (28K or <) XC4000E; XC4028EX - XC4036EX; XC4005XL - XC4028XL
  - 64 MB RAM (Use additional RAM to increase performance)
  - 64MB min Swap Space
- Large Devices (36K or >) XC4036XL - XC4062XL
  - 128 MB RAM (Use additional RAM to increase performance)
  - 128 MB min Swap Space
- Color Monitor

## Alliance Series Options (PC)

### Overview

VIEWlogic Workview Office schematic capture and gate simulator development system with libraries and interfaces for Xilinx FPGAs and CPLDs.

### Workview Office Standard Features:

- Workview Office schematic editor
- Workview Office gate simulator
- Libraries and interfaces
- Hotline support
- Software maintenance for 90-days

### Libraries Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

### Support and Updates Include:

- Answers Database - <http://www.xilinx.com> or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Software Updates (for in-maintenance customers)
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

### Required Hardware Environment:

- Fully IBM compatible PC486/Pentium
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 500 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- 64 Mbytes RAM recommended (increase to improve performance)

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September 5, 1997 (Version 1.0)

## Product Overview

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## Background

The ASIC core industry has been developing for over a decade. Today there exists a wealth of intellectual property (IP) that is readily available from numerous sources. During this time, however, programmable logic did not have the density or the performance needed to accommodate large IP cores.

Today, things have changed considerably. Xilinx is shipping FPGAs like the XL family that have usable densities up to 125,000 gates. Now, not only is the use of pre-defined logic functions in programmable logic a possibility, it is becoming a requirement to meet ever-shrinking product development cycles.

As a result, many ASIC core vendors and system designers are beginning to look at using cores for their programmable logic designs. It is for this reason that Xilinx created the CORE Solutions portfolio of products.

## CORE Solutions Products

CORE Solutions products support four application areas. The application areas are as follows:

- **Standard Bus Interfaces** - such as PCI, PCMCIA, USB and Plug-and-Play ISA.
- **DSP Functions** - These range from small building blocks such adders, registers and multipliers, to larger system-level functions such as FIR filters and Reed-Solomon coders.
- **Telecom and Networking** - building blocks for popular communications standards.
- **Base-Level Functions** - a broad category of functions used across many application segments. These include the every small parameterizable LogiBLOX macros up through larger functions such as UARTs and DMA controllers.

## CORE Solutions Data Book

The goal of the CORE Solutions portfolio of products is to provide cores with the shortest time-to-market and best possible device utilization the programmable logic industry has to offer. Xilinx has published a brand new data book focused entirely on programmable logic cores and related products. Now there is one definitive sourcebook with detailed descriptions of all Xilinx CORE Solutions.

When you receive your copy of the CORE Solutions Data Book, become familiar with the *Product Listing by Application Segment Table*, (reproduced at the end of this over-

view) which lists all of the functions available today. This table will be your best guide to locating a specific product. If you don't see what you need, check the *AllianceCORE Partner Profiles*, Areas of Expertise section, for each of our AllianceCORE partners. Our partners will be more than willing to discuss the possibility of producing a core specifically for your needs.

## Data Book Contents

The contents of the data book are as follows:

- Introduction
  - Program Overview
  - Product Listing by Application Segment
- LogiCORE Products, sold and supported by Xilinx
  - Product Overview
  - PCI
  - DSP
  - CORE Generator products
- AllianceCORE Products, sold and supported by Xilinx' Partners
  - Program Overview
  - Products
  - AllianceCORE Partner Profiles
- LogiBLOX, GUI-based small function generator
- Reference Designs
- Sales Offices, Representatives and Distributors

## Ordering Information

To order a copy, request the CORE Solutions Data Book from the Xilinx Literature Department. In the US call 1-800-231-3386. For international locations call 1-408-879-5017 or you can send an E-mail request to:

literature@xilinx.com.

An electronic version of the CORE Solutions Data Book (1.2M Adobe Acrobat .pdf format) can also be downloaded from:

[www.xilinx.com/products/logicore/core\\_sol.pdf](http://www.xilinx.com/products/logicore/core_sol.pdf)

## LogiCORE Products

LogiCORE products are sold, licensed and supported by Xilinx. They are developed internally by Xilinx or jointly with a partner.

The cores that Xilinx provides as LogiCORE products typically fall into one of two categories. The first are high-performance interface cores that require a thorough understanding and control of the FPGA technology and

implementation software in order to achieve the desired performance and complexity. An example of a core in this category is the LogiCORE PCI interface.

The second category are cores that benefit from a very specialized implementation in the FPGA. An example is the LogiCORE DSP modules that are implemented using a unique algorithm, Distributed Arithmetic. This algorithm fits the lookup-table-based architecture of the FPGA. The result is outstanding performance and device utilization, often more than 10 times better than generic HDL descriptions.

### Xilinx CORE Generator

In addition to actual cores, Xilinx is committed to develop enabling design tools and methodologies to facilitate usage of cores with FPGAs. The first products available in this category are the web-based CORE Generator for PCI and the CORE Generator for DSP (available on CD). This innovative methodology for acquiring and using cores combines the benefits of

- a firm core with predictable performance, and
- the flexibility of system level design, facilitated by behavioral languages such as VHDL and Verilog.

In addition, because Xilinx is using the web as a distribution mechanism, you always have access to the latest versions and enhancements of the cores at:

[www.xilinx.com/products/logicore/logicore.htm](http://www.xilinx.com/products/logicore/logicore.htm)

The LogiCORE products are customized to fit your specific application using an intuitive graphical user interface. Based on your inputs, the tool then generates a proven core with highly predictable timing that can be integrated using any VHDL-, Verilog- or schematic-based design flow. As a result, you can integrate several individually proven cores with given performance into one system on a single FPGA. Because each core is already verified, the time-to-market benefits are maintained for high-complexity FPGAs.

### Xilinx PCI Solutions

Xilinx' PCI solution includes devices, tools and cores needed to build a cost-effective single-chip PCI system in record time.

- LogiCORE PCI - the only proven PCI core with predictable timing
- XC4000E/XL - the industry's fastest FPGAs that allow you to integrate the PCI interface plus 5 to 60 thousand gates of user designed logic
- HardWire - an automatic migration path to a low-cost chip for volume production
- CORE Generator - for easy configuration and integration of the LogiCORE PCI module
- 3<sup>rd</sup> party Design Centers - with PCI expertise available for special applications and customization of the core

PCI is an extremely high-performance and complex specification that is challenging to meet in any technology. To meet the stringent PCI specification the core is carefully hand-tuned for the targeted architecture. Placement and routing for the critical parts of the core is locked down to ensure that timing can be met every time the core is used.

To achieve our goals, the LogiCORE development team is working closely with both the IC and Software teams. As an example of this teamwork, new methodologies for characterizing and modeling our FPGAs have been developed. The result is access to state of the art technology and expertise, that allows you to complete your PCI application in record time.

Xilinx has sold over 250 licenses of the LogiCORE PCI interface and has built up solid knowledge about PCI. We are committed, and will continuously develop our PCI products to remain state of the art.

### Xilinx DSP Solutions

Using an FPGA to implement high performance DSP functions often allows a radical performance advantage over fixed processors while maintaining maximum flexibility and the shortest time-to-market. Until now, tools to automate the design process have been lacking and most designs have been completed manually by experienced FPGA designers.

With the introduction of Xilinx' CORE Generator for DSP, complex parameterized DSP building blocks can be implemented automatically with performance and density equal to or better than a hand-tuned implementation. LogiCORE DSP modules can be used with VHDL-, Verilog- or schematic based design methodologies.

Higher level DSP cores are available from our AllianceCORE partners.

### Acquiring LogiCORE Products

LogiCORE products are available from your local Xilinx sales representative similar to other Xilinx software products. Xilinx and your local sales representative will also be your primary source for support of the core, the devices and the design tools.

You can also send email questions to:

[logicore@xilinx.com](mailto:logicore@xilinx.com).

### AllianceCORE Overview

The AllianceCORE program is a cooperative effort between Xilinx and independent third-party core developers. It is designed to produce a broad selection of industry-standard solutions dedicated for use in Xilinx programmable logic.

Xilinx takes an active role with its partners in the process of productizing AllianceCOREs. This is unique to the AllianceCORE program. Because the process is so involved,

we work closely with our partners to select the right cores first. This naturally limits the number of partners we can work with at any one time and subsequently the number of available cores. At the same time it raises the quality and usability of the cores that are offered.

## AllianceCORE Criteria

A core must meet a minimum set of criteria before it can receive the AllianceCORE label.

### Core Selection

The AllianceCORE program looks at cores from a practical point of view. A programmable logic version of a core must have value over an ASIC or standard product version of the same function. It must be cost effective and make sense for use in a programmable device in a production system. If a candidate core does not pass these simple tests, then it does not make sense to invest the effort to convert it to an AllianceCORE module.

### Core Qualification

Generic, synthesizable cores offer maximum flexibility for users with unique requirements. This is typically the format for cores provided to the ASIC market. With programmable logic, however, this flexibility can come at the expense of efficiency and performance. It can take a considerable amount of effort to get a specific core to synthesize in a way that meets density and timing requirements. Time spent trying to accomplish this can quickly reduce the time-to-market advantage of using programmable logic and cores in the first place.

Xilinx is not interested in promoting generic, synthesizable functions as AllianceCOREs. Instead, AllianceCOREs are generally provided as parameterizable black-boxes that allow customization in critical areas. This guarantees that the implementation is optimized for density while still meeting performance, preserving the time-to-market value of programmable logic. Flexibility is provided by allowing you to quickly implement your unique logic on the same device. Source code versions of the cores are also available from the partners at additional cost for those who need ultimate flexibility.

Announced AllianceCOREs have been implemented and verified in a Xilinx device. They are available immediately for purchase in a Xilinx-specific format. Timing-critical cores designed to adhere to an industry standard also come with appropriate constraints files in order to guaran-

tee functionality and compliance. AllianceCOREs originated from either schematic or HDL entry tools.

### Core Integration

AllianceCOREs are not just cores, they are complete solutions for system designs. While cores by themselves have value, in many cases it is often not enough to just supply a generic core. You may need additional tools such as system software and prototyping equipment to help you rapidly integrate the core into your design, perform system debug in a real-world environment, and then quickly convert the prototype to a production unit. This is particularly true of complex functions.

Many AllianceCORE functions are supported by Xilinx-based demonstration or prototyping boards. Some also have system simulation models or debug software. All of this allows you to evaluate and work with the function before you have to layout your board. These tools are provided by the AllianceCORE partner, usually at additional cost. Descriptions of the support tools available for each core are included in the CORE Solutions Data Book.

Complete solutions like these help preserve the value of using programmable logic while minimizing the support burden for the core provider.

### Acquiring AllianceCORE Products

AllianceCORE products are sold and serviced directly by the AllianceCORE partners since they are the experts for their particular products. They are responsible for pricing, licensing terms, delivery and technical support. Contact information for each partner is included in the AllianceCORE Partner Profiles section of the CORE Solutions Data Book.

If you want additional information about the AllianceCORE program or are interested in becoming a partner, contact Xilinx directly.

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
Attn: Mark Bowlby, AllianceCORE Product Manager  
Phone: +1 408-879-5381  
Fax: +1 408-879-4780  
E-mail: [alliancecore@xilinx.com](mailto:alliancecore@xilinx.com)  
URL: [www.xilinx.com/products/logicore/alliance/tblpart.htm](http://www.xilinx.com/products/logicore/alliance/tblpart.htm)

**Table 1: Product Listing by Application Segment**Check [www.xilinx.com/products/logicore/tbls\\_cores.htm](http://www.xilinx.com/products/logicore/tbls_cores.htm) for the latest listing of available Cores

Function	CORE Solution
<b>Standard Bus Interfaces</b>	
IIC Two-Wire Serial Interface	AllianceCORE
ISA Plug and Play Interface	Reference Design
ISA Interface for JPEG Motion Codec	Reference Design
PCI Master/Slave Interfaces 1.2.0	LogiCORE
PCI Master/Slave Interfaces 2.0.0	LogiCORE
PCMCIA Fax/Modem	AllianceCORE
PCMCIA Library	AllianceCORE
USB - Low-Speed Function Controller	AllianceCORE
USB - Full-Speed Function Controller	AllianceCORE
USB - 3-Port Hub Controller	AllianceCORE
<b>DSP Functions</b>	
1's Complement	LogiCORE
Accumulator, Scaled by 1/2	LogiCORE
Adder, Registered	LogiCORE
Adder, Registered Loadable	LogiCORE
Adder, Registered Scaled	LogiCORE
Adder, Registered Serial	LogiCORE
Adders, Subtractors, Accumulators	Reference Design
Comb Filter	LogiCORE
Correlator, 1-D RAM Based	LogiCORE
Correlator, 1-D ROM Based	LogiCORE
Delay Element	LogiCORE
FIR Filter, 16-Tap, 8-Bit	Reference Design
FIR Filter - Serial Distributed Arithmetic	LogiCORE
FIR Filter - Dual Channel Serial Distributor Arithmetic	LogiCORE
Integrator	LogiCORE
Memory - 16-Word Deep Register Look-up Table	LogiCORE
Memory - 32-Word Deep Register Look-up Table	LogiCORE
Memory - 16-Word Deep Registered RAM	LogiCORE
Memory - 32-Word Deep Registered RAM	LogiCORE
Memory - Registered Synchronous RAM	LogiCORE
Memory - Registered ROM	LogiCORE
Multiplier, Constant Coefficient	LogiCORE
Multiplier, Constant Coefficient (pipelined)	LogiCORE
Multipliers, Parallel - Area Optimized	LogiCORE
Multipliers, Parallel - Performance Optimized	LogiCORE
Parallel to Serial Converter	LogiCORE
Reed-Solomon Decoder	AllianceCORE
Reed-Solomon Encoder	AllianceCORE
SDA FIR Control Logic	LogiCORE
Sine/Cosine	LogiCORE
Square Root	LogiCORE
Subtracter, Registered	LogiCORE
Subtracter, Registered Loadable	LogiCORE

**Table 1: Product Listing by Application Segment (Continued)**

**Check [www.xilinx.com/products/logicore/tbls\\_cores.htm](http://www.xilinx.com/products/logicore/tbls_cores.htm) for the latest listing of available Cores**

Function	CORE Solution
Time Skew Buffer - Non-Symmetric 16-Deep	LogiCORE
Time Skew Buffer - Non-Symmetric 32-Deep	LogiCORE
Time Skew Buffer - Symmetric 16-Deep	LogiCORE
Transform, DFT	LogiCORE
Transform, FFT	LogiCORE
<b>Base-Level Functions</b>	
16450 UART	AllianceCORE
16550A UART with RAM	AllianceCORE
8250 Asynchronous Communications	AllianceCORE
8254 Programmable Timer	AllianceCORE
M8255 Programmable Peripheral Interface	AllianceCORE
XF8255 Programmable Peripheral Interface	AllianceCORE
Accumulator	LogiBLOX
Adder/Subtractor	LogiBLOX
Clock Divider	LogiBLOX
Comparator	LogiBLOX
Constant	LogiCORE
Constant	LogiBLOX
Counter	LogiBLOX
Counter, Loadable Binary	Reference Design
Counter, Ultra-Fast Synchronous	Reference Design
Counter, Accelerating Loadable	Reference Design
Data Register	LogiBLOX
Decoder	LogiBLOX
FIFOs in XC4000 RAM	Reference Design
FIFO, High-Performance RAM-Based	Reference Design
FIFO, Register-Based	Reference Design
Frequency/Phase Comparator for PLL	Reference Design
Gates, Simple	LogiBLOX
Harmonic Frequency Synthesizer and FSK Modulator	Reference Design
Input/Output	LogiBLOX
Microcontroller, Dynamic	Reference Design
Memory (ROM, RAM, Synch-RAM, Dual Port RAM)	LogiBLOX
Multiplexer	LogiBLOX
Multiplexers, Barrel Shifters	Reference Design
Multiplexer, Two Input	LogiCORE
Multiplexer, Three Input	LogiCORE
Multiplexer, Four Input	LogiCORE
Pad	LogiBLOX
Pulse-Width Modulation	Reference Design
Register	LogiCORE
Serial Code Conversion between BCD and Binary	Reference Design
Shift Register	LogiBLOX
Tristate	LogiBLOX





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**2 Development System Products and CORE Solutions Products**

**3 CPLD Products**

**4 FPGA Products**

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**7 HardWire FpgASIC Products**

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**13 Product Technical Information**



## CPLD Products Table of Contents

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### CPLD Products

**XC9500XL 3.3V In-System Programmable CPLD Family**

**XC9500 5V In-System Programmable CPLD Family**





# FastFLASH™ XC9500XL High-Performance CPLD Family

October 2, 1998 (Version 1.1)

Preliminary Product Information

## Features

- Optimized for high-performance 3.3V systems
  - 4 ns pin-to-pin logic delays, with internal system frequency up to 200 MHz
  - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
  - Lower power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 10,000 program/erase cycles endurance rating
  - 20 year data retention
- Pin-compatible with 5V core XC9500 family in common package footprints

## Family Overview

The FastFLASH XC9500XL family is a 3.3V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XL device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XL family is

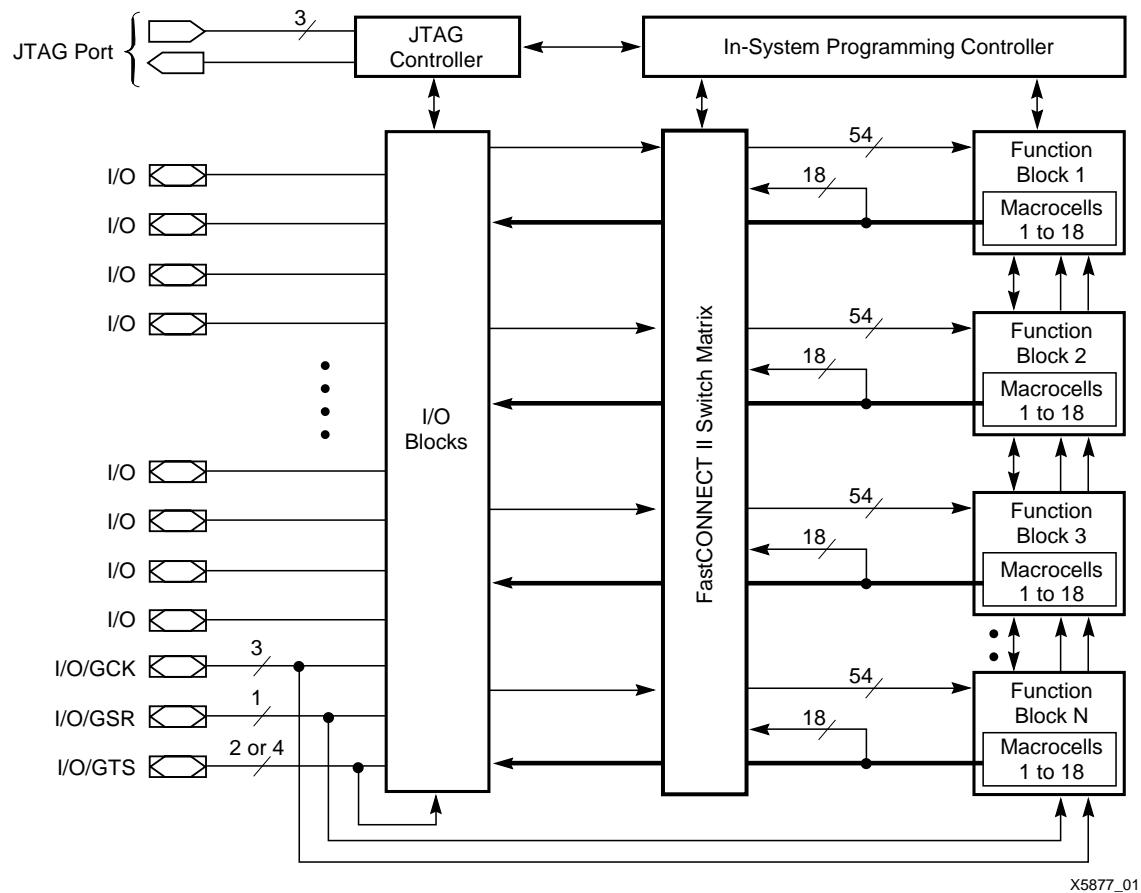
designed to work closely with the Xilinx Spartan-XL and XC4000XL FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in Table 1, logic density of the XC9500XL devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500XL family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XL architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 5V, 3.3V, and 2.5V inputs, and the outputs may be configured for 3.3V or 2.5V operation. The XC9500XL device exhibits symmetric full 3.3V output voltage swing to allow balanced rise and fall times.

## Architecture Description

Each XC9500XL device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54 inputs and 18 outputs. The FastCONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

**Figure 1: XC9500XL Architecture**

Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

**Table 1: XC9500XL Device Family**

	<b>XC9536XL</b>	<b>XC9572XL</b>	<b>XC95144XL</b>	<b>XC95288XL</b>
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
$t_{PD}$ (ns)	4	5	5	6
$t_{SU}$ (ns)	3	3.7	3.7	4.1
$t_{CO}$ (ns)	3	3.5	3.5	4.3
$f_{SYSTEM}$ (MHz)	200	178	178	151

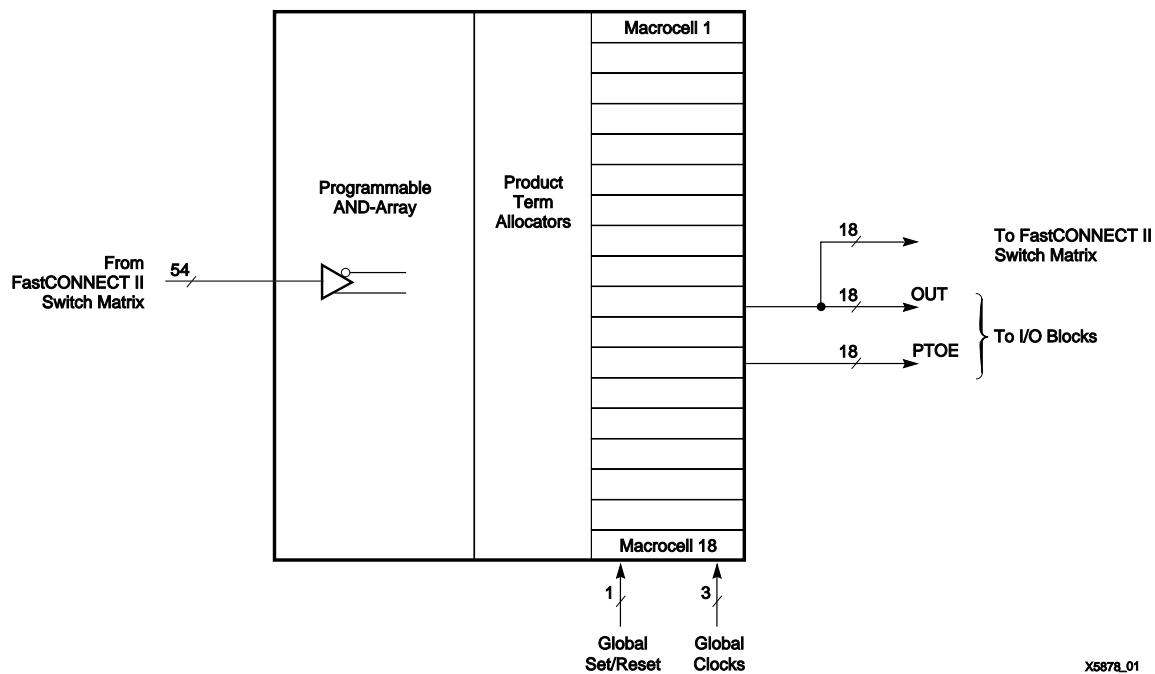
**Table 2: XC9500XL Packages and User I/O Pins (not including 4 dedicated JTAG pins)**

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
44-Pin PLCC	34	34		
64-Pin VQFP	36	52		
100-Pin TQFP		72	81	
144-Pin TQFP			117	117
208-Pin PQFP				168
48-Pin CSP	36	38		
144-Pin CSP			117	
352-Pin BGA				192

## Function Block

Each Function Block, as shown in Figure 2 is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Fifty-four inputs provide 108 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.



**Figure 2: XC9500XL Function Block**

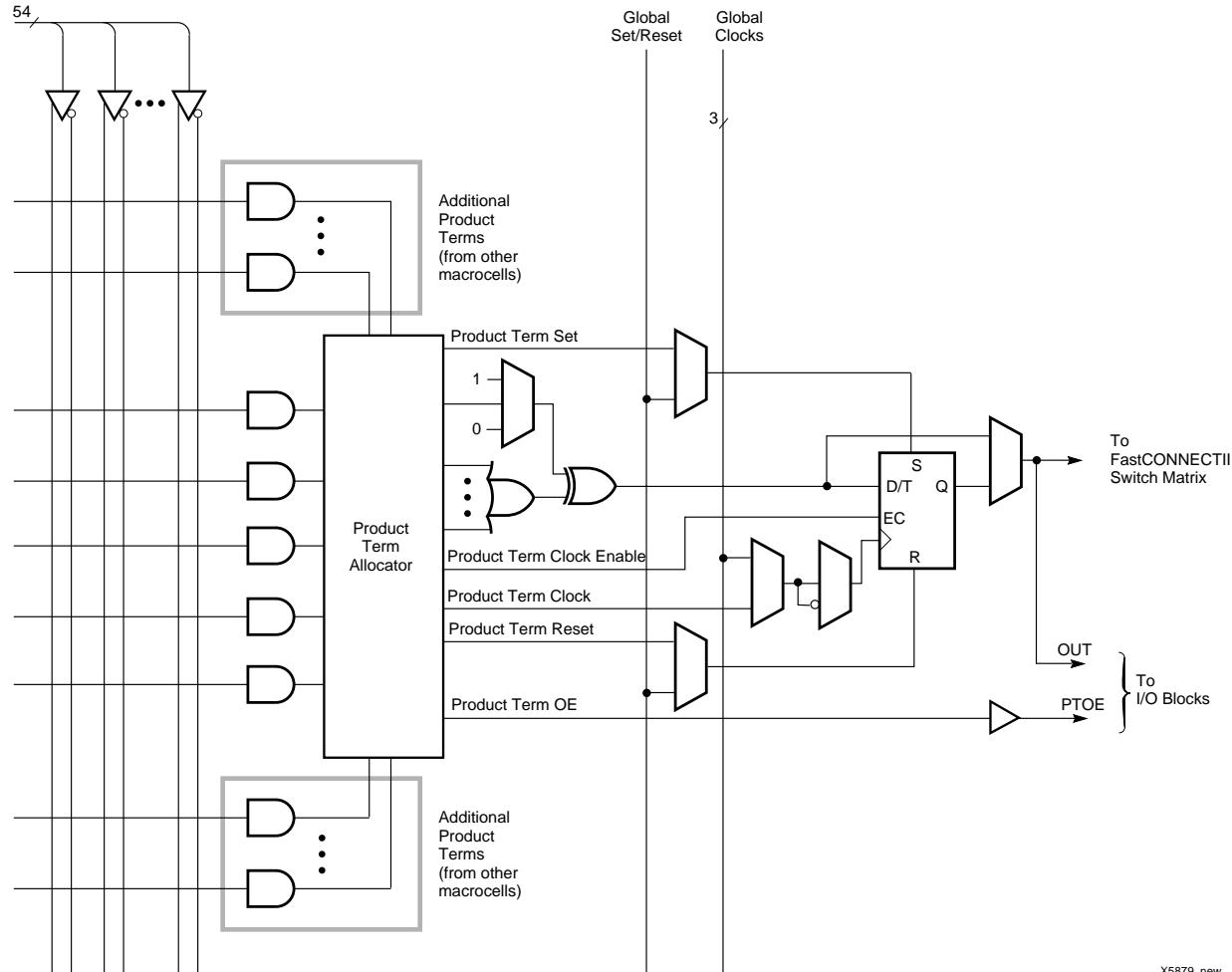
## Macrocell

Each XC9500XL macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, clock enable, set/reset, and output enable.

The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

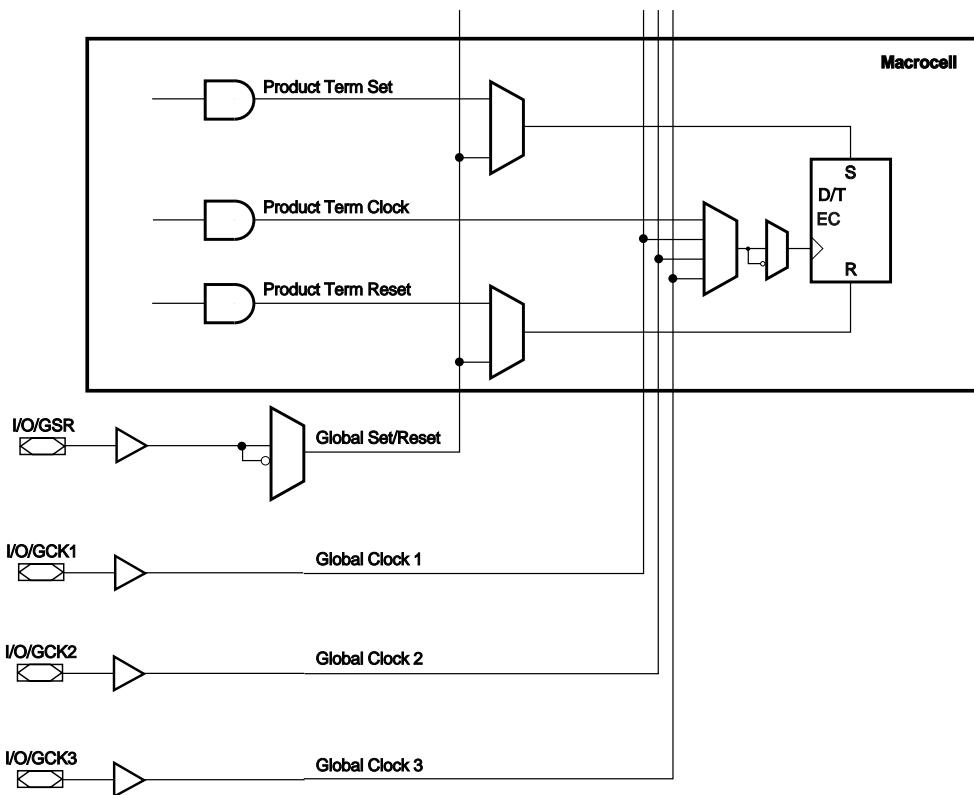


X5879\_new

**Figure 3: XC9500XL Macrocell Within Function Block**

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product

term clock. Both true and complement polarities of the selected clock source can be used within each macrocell. A GSR input is also provided to allow user registers to be set to a user-defined state.

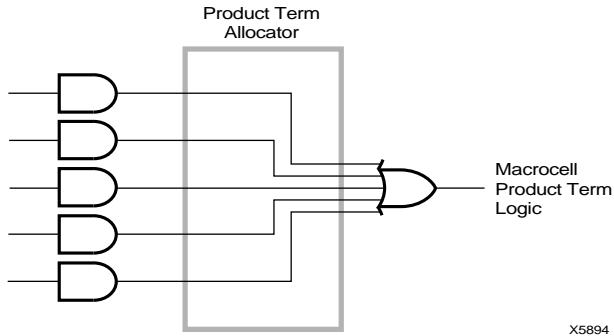


X5880\_01

**Figure 4: Macrocell Clock and Set/Reset Capability**

## Product Term Allocator

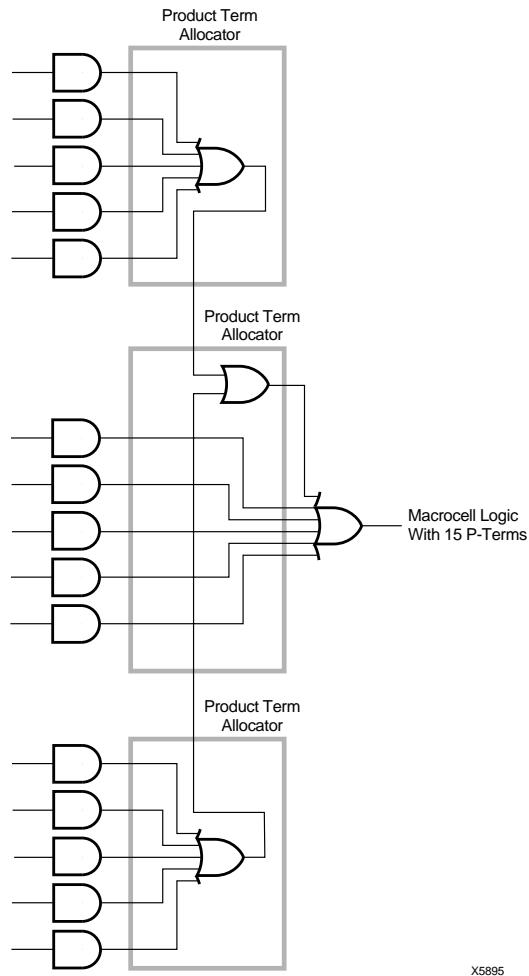
The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.



**Figure 5: Macrocell Logic Using Direct Product Term**

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of t<sub>PTA</sub>, as shown in Figure 6.

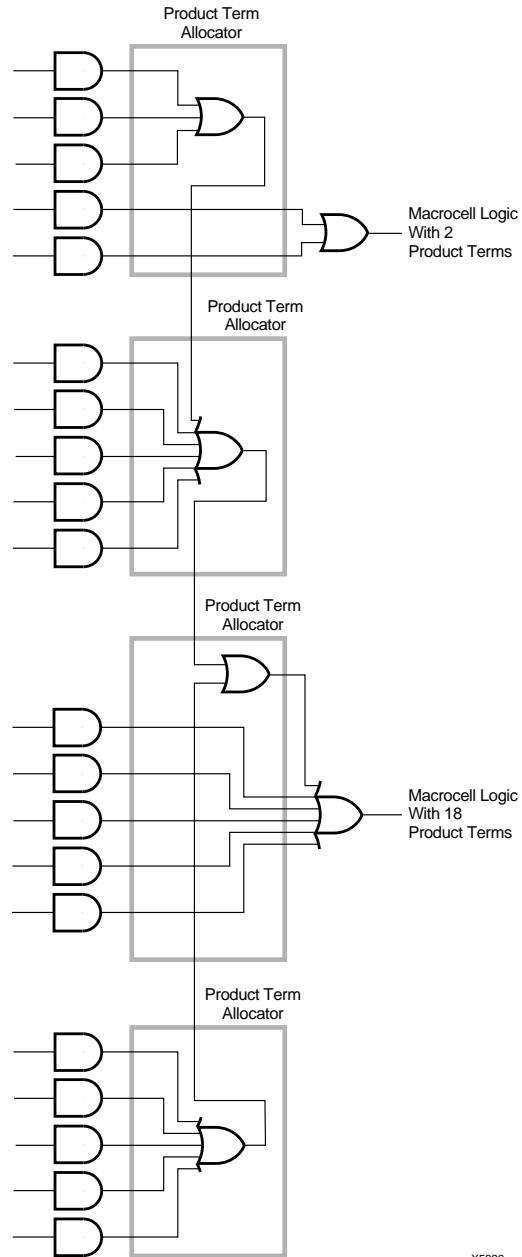
Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed.



**Figure 6: Product Term Allocation With 15 Product Terms**

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7.

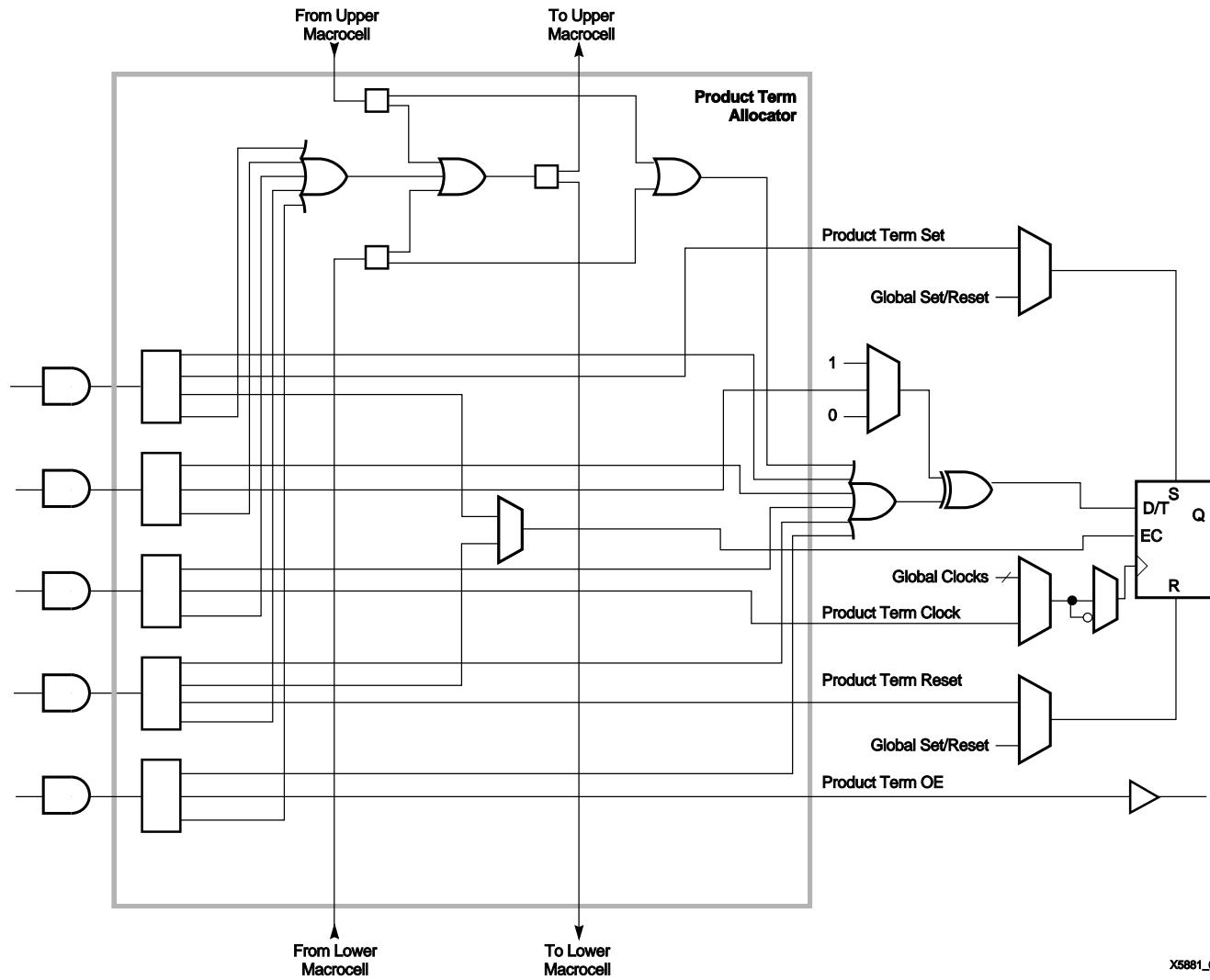
In this example, the incremental delay is only  $2 \cdot t_{PTA}$ . All 90 product terms are available to any macrocell, with a maximum incremental delay of  $8 \cdot t_{PTA}$ .



X5896

**Figure 7: Product Term Allocation Over Several Macrocells**

The internal logic of the product term allocator is shown in Figure 8.

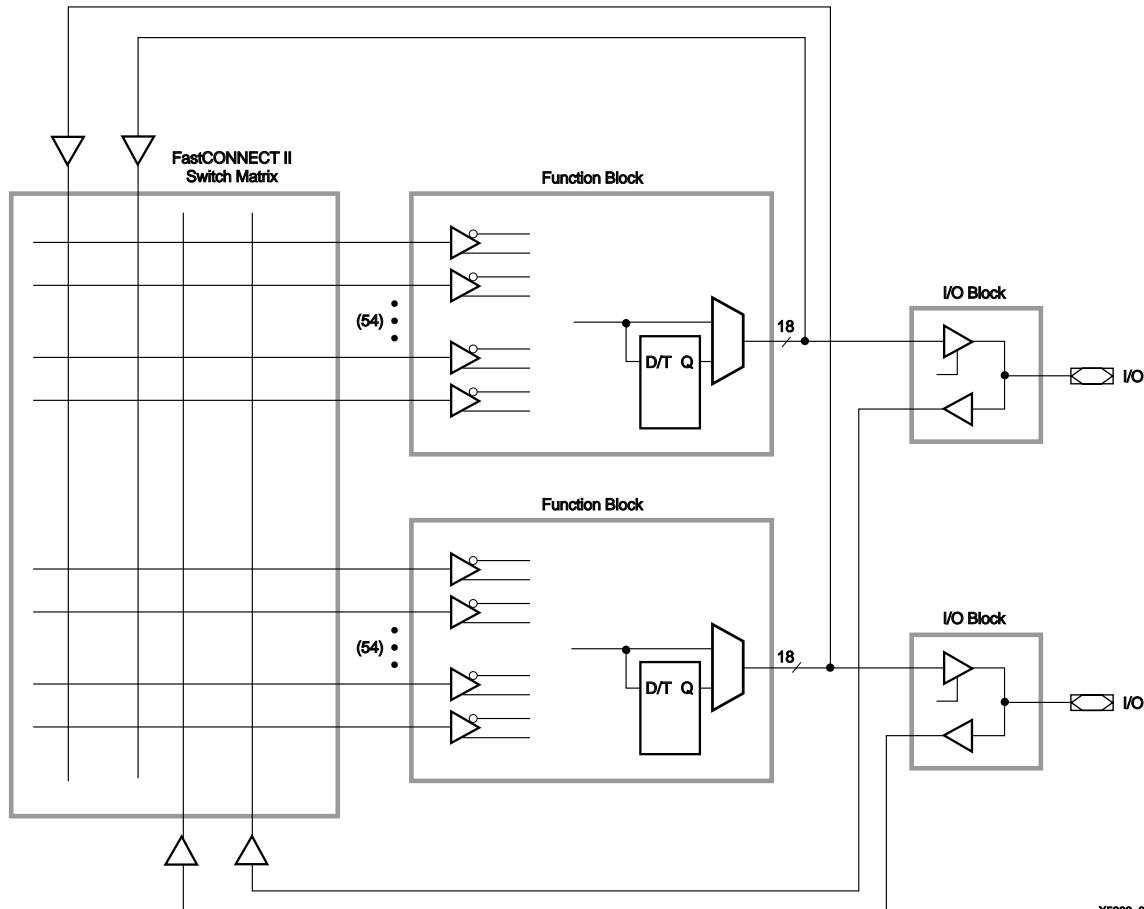


**Figure 8: Product Term Allocator Logic**

## FastCONNECT II Switch Matrix

The FastCONNECT II Switch Matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the

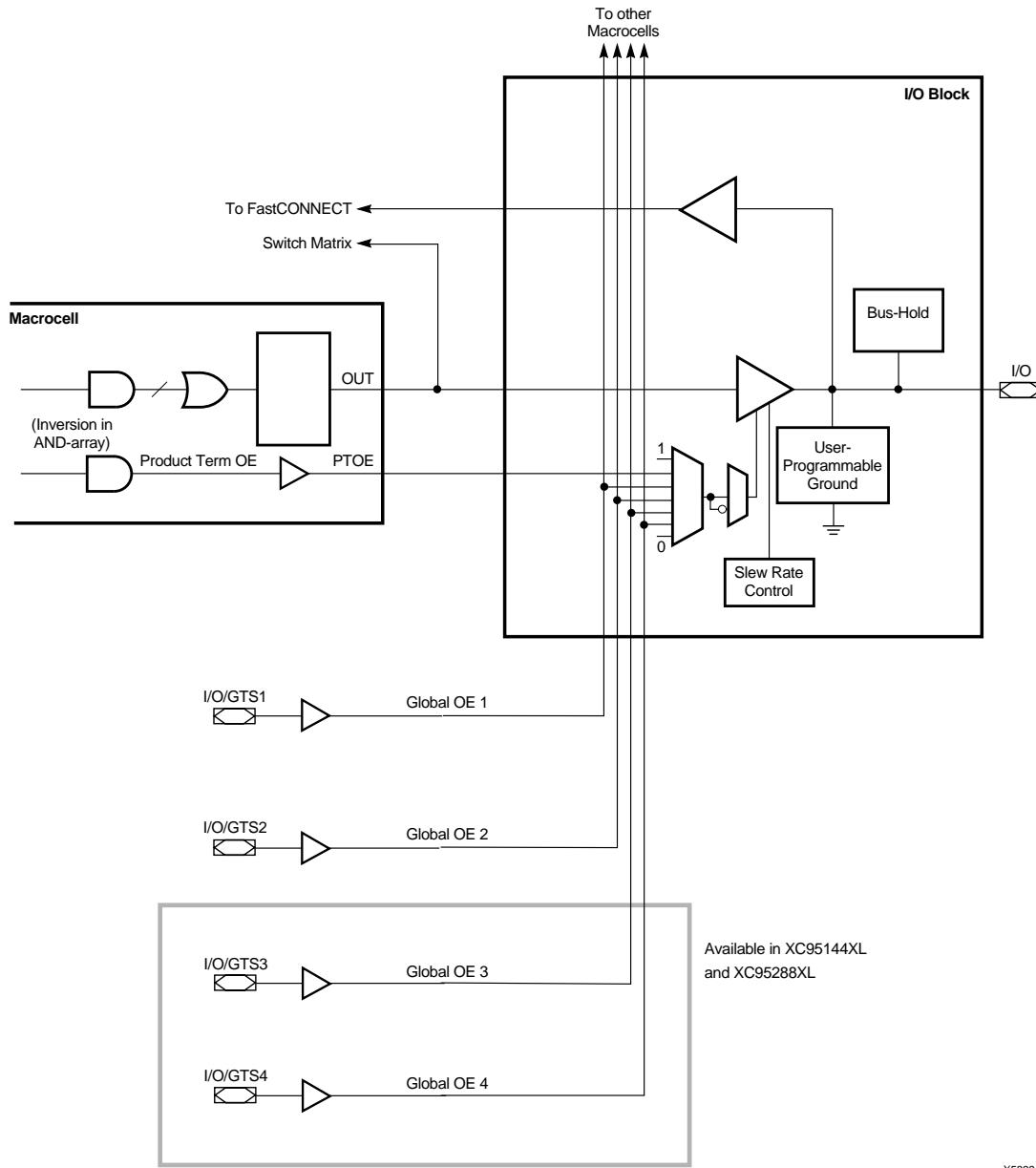
FastCONNECT II matrix. Any of these (up to a fan-in limit of 54) may be selected to drive each FB with a uniform delay.



**Figure 9: FastCONNECT II Switch Matrix**

## I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.



**Figure 10: I/O Block and Output Enable Capability**

The input buffer is compatible with 5V CMOS, 5V TTL, 3.3V CMOS, and 2.5V CMOS signals. The input buffer uses the internal 3.3V voltage supply ( $V_{CCINT}$ ) to ensure that the input thresholds are constant and do not vary with the  $V_{CCIO}$  voltage. Each input buffer provides input hysteresis

(50 mV typical) to help reduce system noise for input signals with slow rise or fall edges.

Each output driver is designed to provide fast switching with minimal power noise. All output drivers in the device may be configured for driving either 3.3V CMOS levels (which are compatible with 5V TTL levels as well) or 2.5V CMOS levels

by connecting the device output voltage supply ( $V_{CCIO}$ ) to a 3.3V or 2.5V voltage supply. Figure 11 shows how the XC9500XL device can be used in 3.3V only systems and mixed voltage systems with any combination of 5V, 3.3V and 2.5V power supplies.

Each output driver can also be configured for slew-rate limited operation. Output edge rates may be slowed down to reduce system noise (with an additional time delay of  $t_{SLEW}$ ) under user control. See Figure 12.

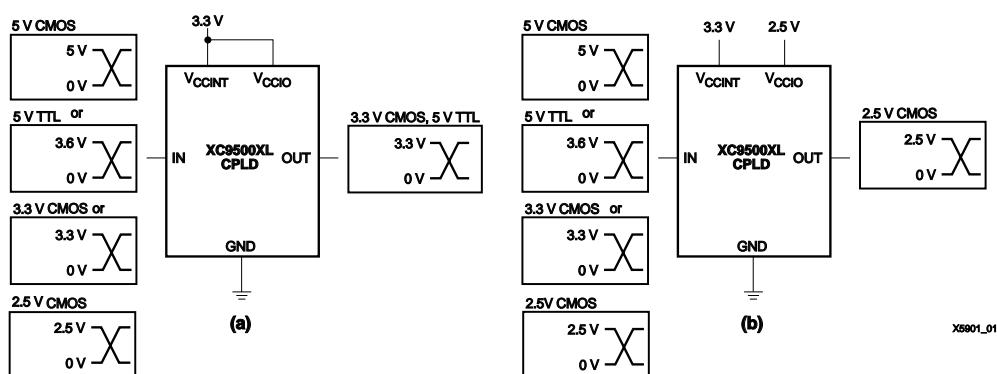
The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global output enable signals (GTS), always "1," or always "0." There are two global output enables for devices with 72 or fewer macrocells, and four global output enables for devices with 144 or more macrocells. Any selected output enable signal may be inverted locally at each pin output to provide maximal design flexibility.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins in order to force otherwise unused pins to a low voltage state, as well as provide for additional device grounding capability. This grounding of the pin is

achieved by internal logic that forces a logic low output regardless of the internal macrocell signal, so the internal macrocell logic is unaffected by the programmable ground pin capability.

Each IOB also provides for bus-hold circuitry that is active during valid user operation. The bus-hold feature eliminates the need to tie unused pins either high or low by holding the last known state of the input until the next input signal is present. The bus-hold circuit drives back the same state via a nominal resistance ( $R_{BH}$ ) of 50k ohms. See Figure 13. Note the bus-hold output will drive no higher than  $V_{CCIO}$  to prevent overdriving signals when interfacing to 2.5V components.

When the device is not in valid user operation, the bus-hold circuit defaults to an equivalent 50k ohm pull-up resistor in order to provide a known repeatable device state. This occurs when the device is in the erased state, in programming mode, in JTAG INTEST mode, or during initial power-up. A pull-down resistor (1k ohm) may be externally added to any pin to override the default  $R_{BH}$  resistance to force a low state during power-up or any of these other modes.



**Figure 11: XC9500XL Devices in (a) 3.3V only and (b) Mixed 5V/3.3V/2.5V Systems**

## 5V Tolerant I/Os

The I/Os on each XC9500XL device are fully 5V tolerant even though the core power supply is 3.3 volts. This allows 5V CMOS signals to connect directly to the XC9500XL inputs without damage. In addition, the 3.3V  $V_{CCINT}$  power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply ( $V_{CCINT}$ ), and the output power supply ( $V_{CCIO}$ ) may have power applied in any order. This makes the XC9500XL devices immune to power supply sequencing problems.

## Pin-Locking Capability

The capability to lock the user defined pin assignments during design iteration depends on the ability of the architecture to adapt to unexpected changes. The XC9500XL devices incorporate architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500XL architecture provides for superior pin-locking characteristics with a combination of large number of routing switches in the FastCONNECT II switch matrix, a 54-wide input Function Block, and flexible, bi-directional product term allocation within each macrocell. These features address design changes that require adding or

changing internal routing, including additional signals into existing equations, or increasing equation complexity, respectively.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new

design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.

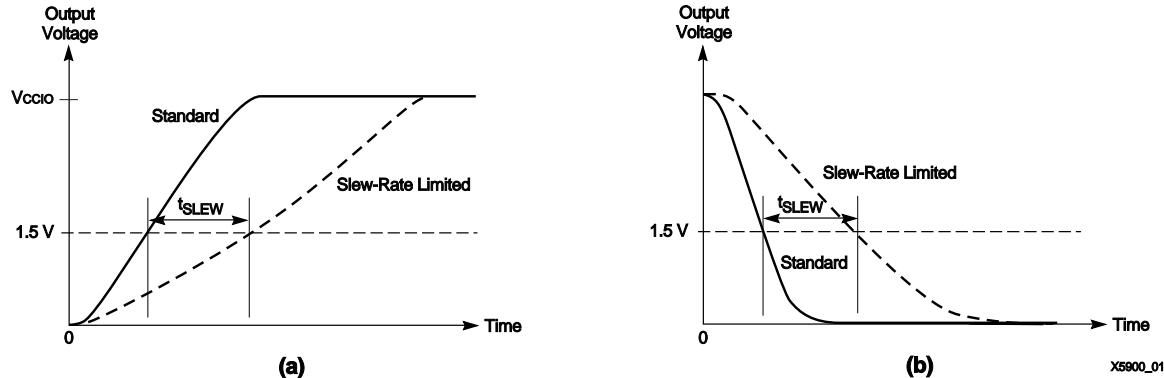


Figure 12: Output Slew-Rate Control For (a) Rising and (b) Falling Outputs

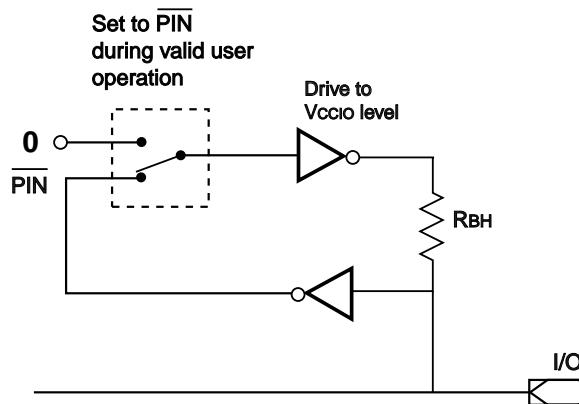


Figure 13: Bus-Hold Logic

## In-System Programming

One or more XC9500XL devices can be daisy chained together and programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 14. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are 3-stated and pulled high by the bus-hold circuitry during in-system programming. If a particular signal

must remain low during this time, then a pulldown resistor may be added to the pin.

## External Programming

XC9500XL devices can also be programmed by the Xilinx HW-130 device programmer as well as third-party programmers. This provides the added flexibility of using pre-programmed devices during manufacturing, with an in-system programmable option for future enhancements and design changes.

## Reliability and Endurance

All XC9500XL CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles and a minimum

data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

## IEEE 1149.1 Boundary-Scan (JTAG)

XC9500XL devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, HIGHZ and CLAMP instructions are supported in each device. Additional instructions are included for in-system programming operations.

## Design Security

XC9500XL devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

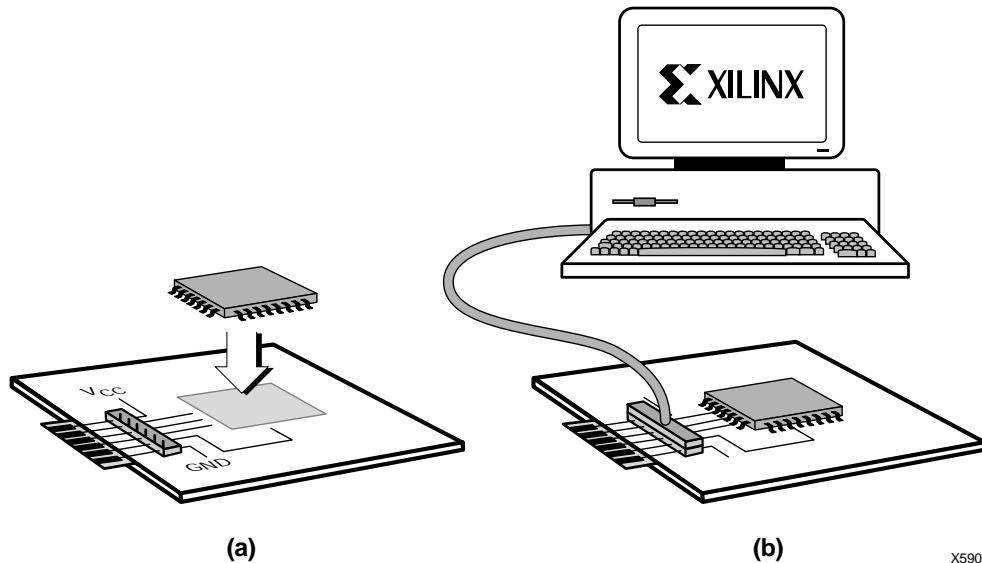
The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. When set, they also inhibit further program operations but

allow device erase. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern with a specific sequence of JTAG instructions.

**Table 3: Data Security Options**

		Read Security	
		Default	Set
Write Security	Default	Read Allowed Program/Erase Allowed	Read Inhibited Program Inhibit Erase Allowed
	Set	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Inhibited



X5902

**Figure 14: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

## Low Power Mode

All XC9500XL devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur addi-

tional delay ( $t_{LP}$ ) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

## Timing Model

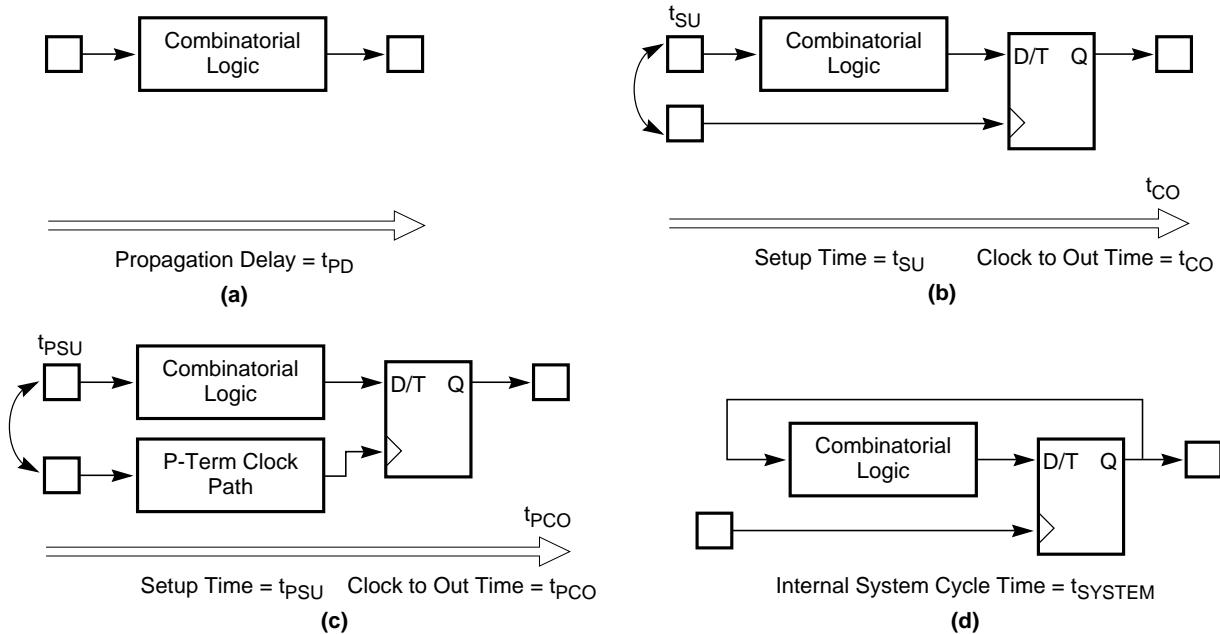
The uniformity of the XC9500XL architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 15, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how

each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

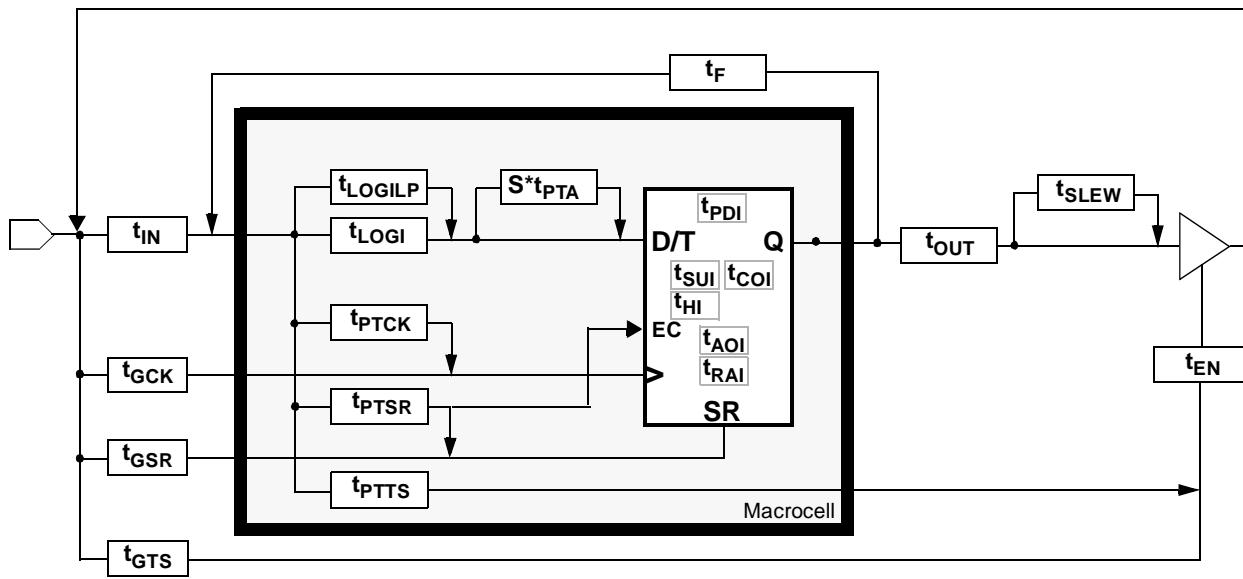
The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The example in Figure 6 shows that up to 15

product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

Detailed timing information may be derived from the full timing model shown in Figure 16. The values and explanations for each parameter are given in the individual device data sheets.



**Figure 15: Basic Timing Model**



**Figure 16:** Detailed Timing Model

## Power-Up Characteristics

The XC9500XL devices are well behaved under all operating conditions. During power-up each XC9500XL device employs internal circuitry which keeps the device in the quiescent state until the  $V_{CCINT}$  supply voltage is at a safe level (approximately 2.5 V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the pins weakly pulled high, as shown in Table 5. When the supply voltage reaches a safe level, all user registers become initialized (typically within 200  $\mu$ s), and the device is immediately available for operation, as shown in Figure 17.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

## Development System Support

The XC9500XL family and associated in-system programming capabilities are fully supported in either software solutions available from Xilinx.

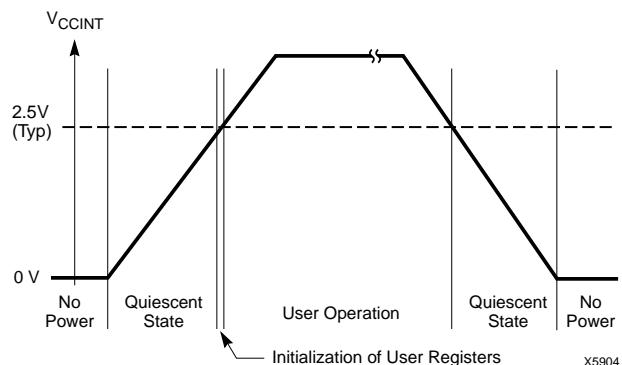
The Foundation Series is an all-in-one development system containing schematic entry, HDL (VHDL, Verilog, and

ABEL), and simulation capabilities. It supports the XC9500XL family as well as other CPLD and FPGA families.

The Alliance Series includes CPLD and FPGA implementation technology as well as all necessary libraries and interfaces for Alliance partner EDA solutions.

## FastFLASH Technology

An advanced 0.35 micron feature size CMOS Flash process is used to fabricate all XC9500XL devices. The FastFLASH process provides high performance logic capability, fast programming times, and superior reliability and endurance ratings.



**Figure 17:** Device Behavior During Power-up

**Table 4: Timing Model Parameters**

Description	Parameter	Product Term Allocator <sup>1</sup>	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	$t_{PD}$	$+ t_{PTA} * S$	$+ t_{LP}$	$+ t_{SLEW}$
Global Clock Setup Time	$t_{SU}$	$+ t_{PTA} * S$	$+ t_{LP}$	—
Global Clock-to-output	$t_{CO}$	—	—	$+ t_{SLEW}$
Product Term Clock Setup Time	$t_{PSU}$	$+ t_{PTA} * S$	$+ t_{LP}$	—
Product Term Clock-to-output	$t_{PCO}$	—	—	$+ t_{SLEW}$
Internal System Cycle Period	$t_{SYSTEM}$	$+ t_{PTA} * S$	$+ t_{LP}$	—

**Note:** 1. S = the logic span of the function, as defined in the text.

**Table 5: XC9500XL Device Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold	Pull-up	Pull-up	Bus-Hold
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

## Features

- 4 ns pin-to-pin logic delays
- System frequency up to 200 MHz
- 36 macrocells with 800 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 48-pin CSP (36 user I/O pins)
  - 64-pin VQFP (36 user I/O pins)
- Optimized for high-performance 3.3 V systems
  - Low power operation
  - 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
  - 3.3 V or 2.5 V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000 V
- Pin-compatible with 5 V-core XC9536 device in the 44-pin PLCC package and the 48-pin CSP package

## Description

The XC9536XL is a 3.3 V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 4 ns. See Figure 2 for architecture overview.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of  $I_{CC}$ , the following equation may be used:

$$I_{CC} (\text{mA}) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance (default) mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual  $I_{CC}$  value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

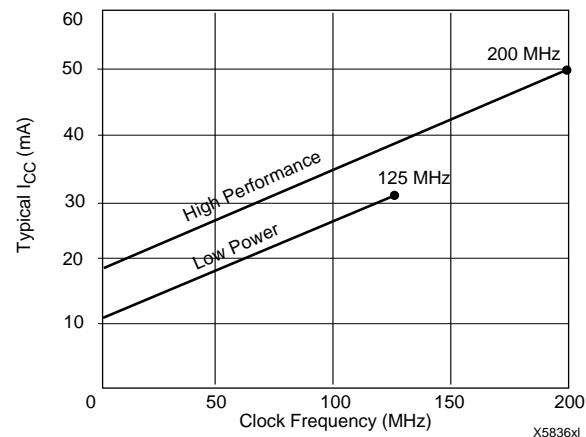
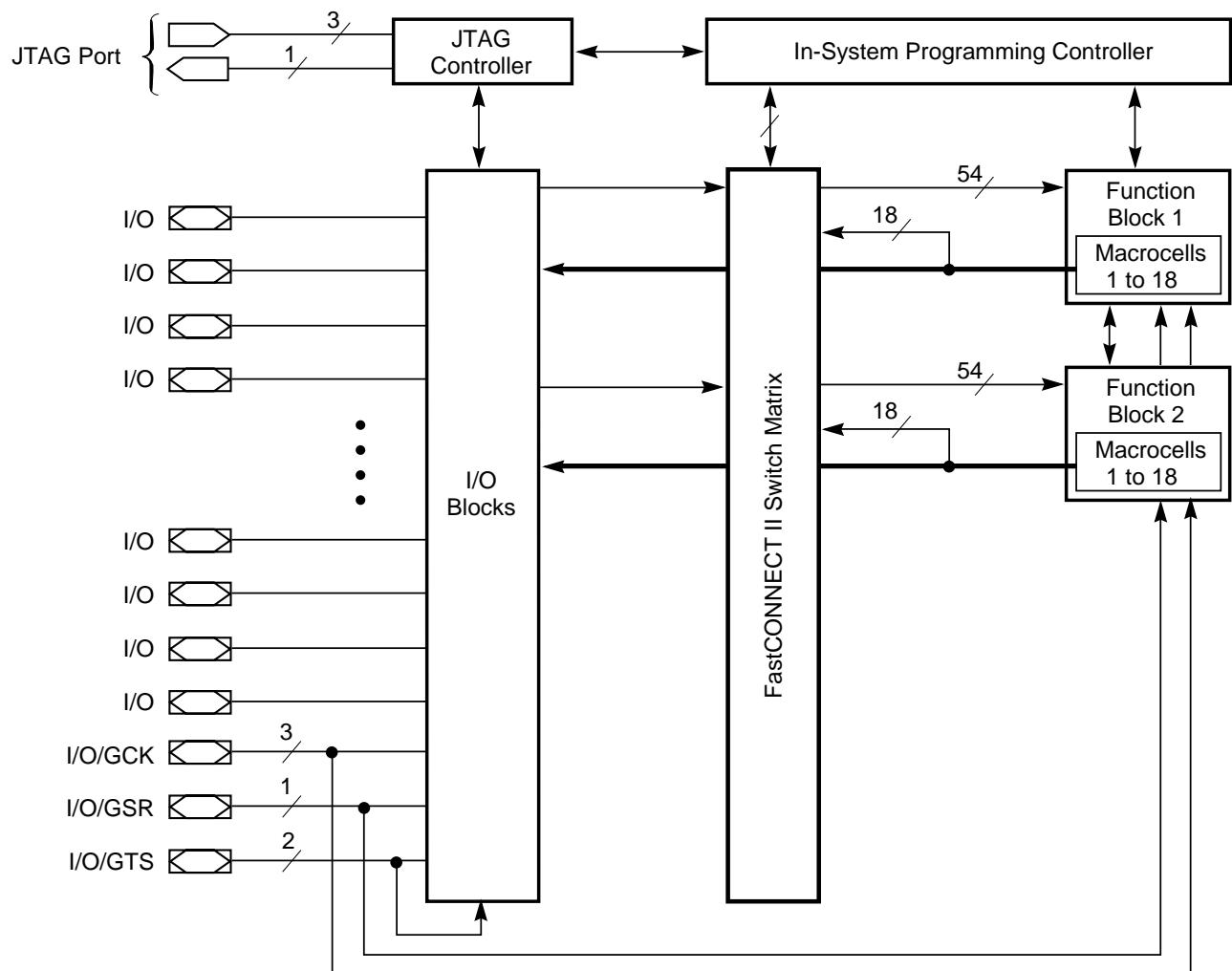


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC9536XL



X5922C\_1

**Figure 2: XC9536XL Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

Note 1: Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	3.0	3.6	V
		Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers for 3.3 V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5 V operation		2.3	2.7	V
$V_{IL}$	Low-level input voltage		0	0.80	V
$V_{IH}$	High-level input voltage		2.0	5.5	V
$V_O$	Output voltage		0	$V_{CCIO}$	V

## Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles (Endurance)	10,000	-	Cycles
$V_{ESD}$	Electrostatic Discharge (ESD)	2,000	-	Volts

## DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 3.3 V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4		V
	Output high voltage for 2.5 V outputs	$I_{OH} = -500 \mu\text{A}$	90% $V_{CCIO}$		V
$V_{OL}$	Output low voltage for 3.3 V outputs	$I_{OL} = 8.0 \text{ mA}$		0.4	V
	Output low voltage for 2.5 V outputs	$I_{OL} = 500 \mu\text{A}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{cc}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	10(Typ)		mA

## AC Characteristics

Symbol	Parameter	XC9536XL-4		XC9536XL-5		XC9536XL-7		XC9536XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	Min	Max	
t <sub>PD</sub>	I/O to output valid		4.0		5.0		7.5		10.0	ns
t <sub>SU</sub>	I/O setup time before GCK	3.0		3.7		4.8		6.5		ns
t <sub>H</sub>	I/O hold time after GCK	0.0		0.0		0.0		0.0		ns
t <sub>CO</sub>	GCK to output valid		3.0		3.5		4.5		5.8	ns
f <sub>SYSTEM</sub>	Multiple FB internal operating frequency		200.0		178.6		125.0		100.0	MHz
t <sub>PSU</sub>	I/O setup time before p-term clock input	1.2		1.7		1.6		2.1		ns
t <sub>PH</sub>	I/O hold time after p-term clock input	1.8		2.0		3.2		4.4		ns
t <sub>PCO</sub>	P-term clock output valid		4.8		5.5		7.7		10.2	ns
t <sub>OE</sub>	GTS to output valid		3.5		4.0		5.0		7.0	ns
t <sub>OD</sub>	GTS to output disable				4.0		5.0		7.0	ns
t <sub>POE</sub>	Product term OE to output enabled		6.5		7.0		9.5		11.0	ns
t <sub>POD</sub>	Product term OE to output disabled				7.0		9.5		11.0	ns
t <sub>AO</sub>	GSR to output valid		7.6		10.0		12.0		14.5	ns
t <sub>PAO</sub>	P-term S/R to output valid		8.4		10.5		12.6		15.3	ns
t <sub>WLH</sub>	GCK pulse width (High or Low)	2.5		2.8		4.0		4.5		ns
t <sub>PLH</sub>	P-term clock pulse width (High or Low)	5.0		5.0		6.5		7.0		ns
		Advance		Preliminary						

Note 1:Please contact Xilinx for up-to-date information on advance specifications.

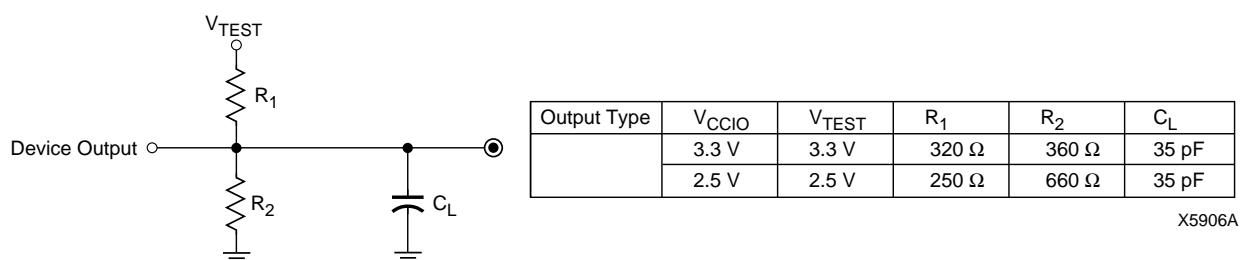


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC9536XL-4		XC9536XL-5		XC9536XL-7		XC9536XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>										
t <sub>IN</sub>	Input buffer delay		1.2		1.5		2.3		3.5	ns
t <sub>GCK</sub>	GCK buffer delay		1.0		1.1		1.5		1.8	ns
t <sub>GSR</sub>	GSR buffer delay		1.2		2.0		3.1		4.5	ns
t <sub>GTS</sub>	GTS buffer delay		3.5		4.0		5.0		7.0	ns
t <sub>OUT</sub>	Output buffer delay		1.6		2.0		2.5		3.0	ns
t <sub>EN</sub>	Output buffer enable/disable delay		0.0		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>										
t <sub>PTCK</sub>	Product term clock delay		1.6		1.6		2.4		2.7	ns
t <sub>PTSR</sub>	Product term set/reset delay		0.8		1.0		1.4		1.8	ns
t <sub>PTTS</sub>	Product term 3-state delay		5.3		5.5		7.2		7.5	ns
<b>Internal Register and Combinatorial Delays</b>										
t <sub>PDI</sub>	Combinatorial logic propagation delay		0.4		0.5		1.3		1.7	ns
t <sub>SUI</sub>	Register setup time	2.0		2.3		2.6		3.0		ns
t <sub>HI</sub>	Register hold time	1.0		1.4		2.2		3.5		ns
t <sub>ECSU</sub>	Register clock enable setup time	2.0		2.3		2.6		3.0		ns
t <sub>ECHO</sub>	Register clock enable hold time	1.0		1.4		2.2		3.5		ns
t <sub>COI</sub>	Register clock to output valid time		0.4		0.4		0.5		1.0	ns
t <sub>AOI</sub>	Register async. S/R to output delay		4.8		6.0		6.4		7.0	ns
t <sub>RAI</sub>	Register async. S/R recover before clock			5.0		7.5		10.0		ns
t <sub>LOGI</sub>	Internal logic delay		0.8		1.0		1.4		1.8	ns
t <sub>LOGILP</sub>	Internal low power logic delay		3.8		5.0		6.4		7.3	ns
<b>Feedback Delays</b>										
t <sub>F</sub>	FastCONNECT II™ feedback delay		1.8		1.9		3.5		4.2	ns
<b>Time Adders</b>										
t <sub>PTA</sub>	Incremental product term allocator delay		0.6		0.7		0.8		1.0	ns
t <sub>SLEW</sub>	Slew-rate limited delay		2.5		3.0		4.0		4.5	ns
Advance					Preliminary					

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

## XC9536XL I/O Pins

Function Block	Macrocell	PC44	CS48	VQ64	BScan Order	Notes
1	1	2	D6	9	105	
1	2	3	C7	10	102	
1	3	5	B7	15	99	[1]
1	4	4	C6	11	96	
1	5	6	B6	16	93	[1]
1	6	8	A6	19	90	
1	7	7	A7	17	87	[1]
1	8	9	C5	20	84	
1	9	11	B5	22	81	
1	10	12	A4	24	78	
1	11	13	B4	25	75	
1	12	14	A3	27	72	
1	13	18	B2	33	69	
1	14	19	B1	35	66	
1	15	20	C2	36	63	
1	16	22	C3	38	60	
1	17	24	D2	42	57	
1	18	-	D3	39	54	

Function Block	Macrocell	PC44	CS48	VQ64	BScan Order	Notes
2	1	1	D7	8	51	
2	2	44	E5	7	48	
2	3	42	E6	5	45	[1]
2	4	43	E7	6	42	
2	5	40	F6	2	39	[1]
2	6	39	G7	64	36	[1]
2	7	38	G6	63	33	
2	8	37	F5	62	30	
2	9	36	G5	61	27	
2	10	35	F4	60	24	
2	11	34	G4	57	21	
2	12	33	E3	56	18	
2	13	29	F2	50	15	
2	14	28	G1	48	12	
2	15	27	F1	45	9	
2	16	26	E2	44	6	
2	17	25	E1	43	3	
2	18	-	E4	49	0	

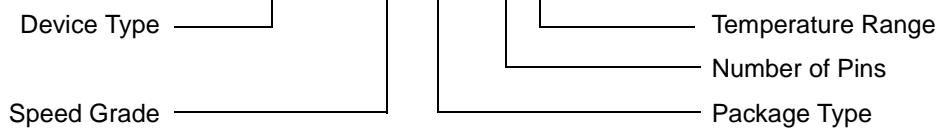
Note 1: Global control pin.

## XC9536XL Global, JTAG and Power Pins

Pin Type	PC44	CS48	VQ64
I/O/GCK1	5	B7	15
I/O/GCK2	6	B6	16
I/O/GCK3	7	A7	17
I/O/GTS1	42	E6	5
I/O/GTS2	40	F6	2
I/O/GSR	39	G7	64
TCK	17	A1	30
TDI	15	B3	28
TDO	30	G2	53
TMS	16	A2	29
$V_{CCINT}$ 3.3 V	21, 41	C1, F7	3, 37
$V_{CCIO}$ 2.5 V/3.3 V	32	G3	55
GND	10, 23, 31	A5, D1, F3	21, 41, 54
No Connects	-	-	1, 4, 12, 13, 14, 18, 23, 26, 31, 32, 34, 40, 46, 47, 51, 52, 58, 59

## Ordering Information

**Example: XC9536XL -5 PC 44 C**



### Speed Options

- 10 10 ns pin-to-pin delay
- 7 7.5 ns pin-to-pin delay
- 5 5 ns pin-to-pin delay
- 4 4 ns pin-to-pin delay

### Packaging Options

- PC44 44-Pin Plastic Lead Chip Carrier (PLCC)
- CS48 48-Pin Chip Scale Package
- VQ64 64-Pin Quad Flat Pack (VQFP)

### Temperature Options

C = Commercial  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$   
 I = Industrial  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

## Component Availability

Pins		44	48	64
Type		Plastic PLCC	Plastic CSP	Plastic VQFP
Code		PC44	CS48	VQ64
XC9536XL	-10	C, I	-	C, I
	-7	C	C	C
	-5	C	C	C
	-4	(C)	-	(C)

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ) I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

( ) Parenthesis indicate future planned products. Please contact Xilinx for up-to-date information.

## Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 48-pin CSP (38 user I/O pins)
  - 64-pin VQFP (52 user I/O pins)
  - 100-Pin TQFP (72 user I/O pins)
- Optimized for high-performance 3.3 V systems
  - Low power operation
  - 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
  - 3.3 V or 2.5 V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000 V
- Pin-compatible with 5 V-core XC9572 device in the 44-pin PLCC package and the 100-pin TQFP package

## Description

The XC9572XL is a 3.3 V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 4 ns. See Figure 2 for architecture overview.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of  $I_{CC}$ , the following equation may be used:

$$I_{CC} (\text{mA}) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance (default) mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual  $I_{CC}$  value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

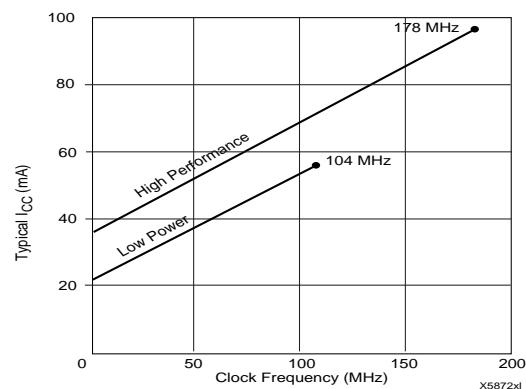
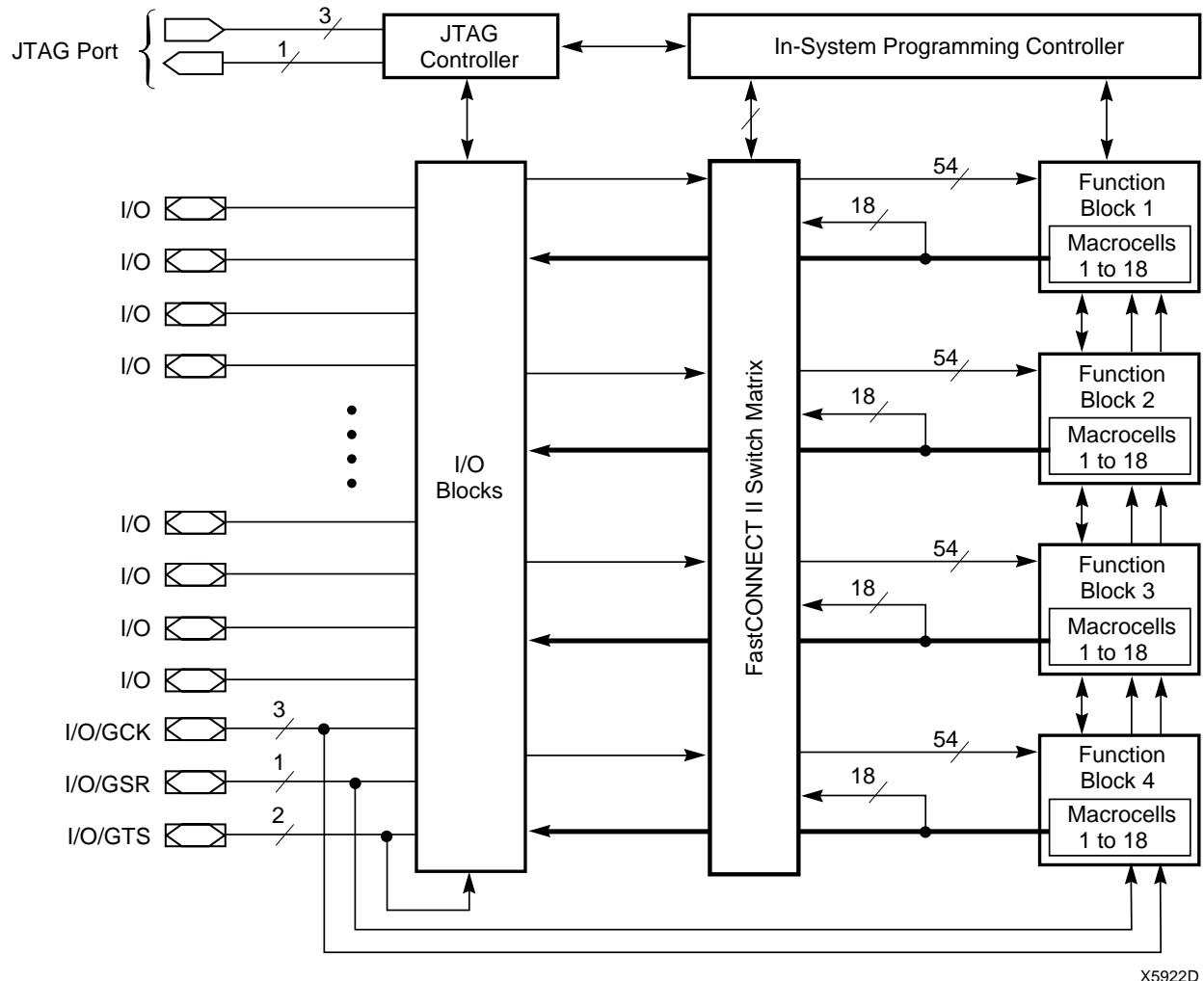


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC9572XL



X5922D\_1

**Figure 2: XC9572XL Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

Note 1: Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	3.0	3.6	V
		Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers for 3.3 V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5 V operation		2.3	2.7	V
$V_{IL}$	Low-level input voltage		0	0.80	V
$V_{IH}$	High-level input voltage		2.0	5.5	V
$V_O$	Output voltage		0	$V_{CCIO}$	V

## Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles (Endurance)	10,000	-	Cycles
$V_{ESD}$	Electrostatic Discharge (ESD)	2,000	-	Volts

## DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 3.3 V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4		V
	Output high voltage for 2.5 V outputs	$I_{OH} = -500 \mu\text{A}$	90% $V_{CCIO}$		V
$V_{OL}$	Output low voltage for 3.3 V outputs	$I_{OL} = 8.0 \text{ mA}$		0.4	V
	Output low voltage for 2.5 V outputs	$I_{OL} = 500 \mu\text{A}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	20 (Typ)		mA

## AC Characteristics

Symbol	Parameter	XC9572XL-5		XC9572XL-7		XC9572XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	
t <sub>PD</sub>	I/O to output valid		5.0		7.5		10.0	ns
t <sub>SU</sub>	I/O setup time before GCK	3.7		4.8		6.5		ns
t <sub>H</sub>	I/O hold time after GCK	0.0		0.0		0.0		ns
t <sub>CO</sub>	GCK to output valid		3.5		4.5		5.8	ns
f <sub>SYSTEM</sub>	Multiple FB internal operating frequency		178.6		125.0		100.0	MHz
t <sub>PSU</sub>	I/O setup time before p-term clock input	1.7		1.6		2.1		ns
t <sub>PH</sub>	I/O hold time after p-term clock input	2.0		3.2		4.4		ns
t <sub>PCO</sub>	P-term clock output valid		5.5		7.7		10.2	ns
t <sub>OE</sub>	GTS to output valid		4.0		5.0		7.0	ns
t <sub>OD</sub>	GTS to output disable		4.0		5.0		7.0	ns
t <sub>POE</sub>	Product term OE to output enabled		7.0		9.5		11.0	ns
t <sub>POD</sub>	Product term OE to output disabled		7.0		9.5		11.0	ns
t <sub>AO</sub>	GSR to output valid		10.0		12.0		14.5	ns
t <sub>PAO</sub>	P-term S/R to output valid		10.5		12.6		15.3	ns
t <sub>WLH</sub>	GCK pulse width (High or Low)	2.8		4.0		4.5		ns
t <sub>PLH</sub>	P-term clock pulse width (High or Low)	5.0		6.5		7.0		ns
		Advance		Preliminary				

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

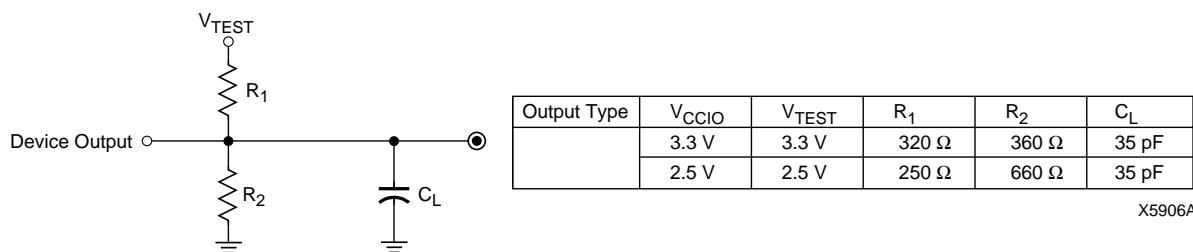


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC9572XL-5		XC9572XL-7		XC9572XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	
<b>Buffer Delays</b>								
$t_{IN}$	Input buffer delay		1.5		2.3		3.5	ns
$t_{GCK}$	GCK buffer delay		1.1		1.5		1.8	ns
$t_{GSR}$	GSR buffer delay		2.0		3.1		4.5	ns
$t_{GTS}$	GTS buffer delay		4.0		5.0		7.0	ns
$t_{OUT}$	Output buffer delay		2.0		2.5		3.0	ns
$t_{EN}$	Output buffer enable/disable delay		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>								
$t_{PTCK}$	Product term clock delay		1.6		2.4		2.7	ns
$t_{PTSR}$	Product term set/reset delay		1.0		1.4		1.8	ns
$t_{PTTS}$	Product term 3-state delay		5.5		7.2		7.5	ns
<b>Internal Register and Combinatorial Delays</b>								
$t_{PDI}$	Combinatorial logic propagation delay		0.5		1.3		1.7	ns
$t_{SUI}$	Register setup time	2.3		2.6		3.0		ns
$t_{HI}$	Register hold time	1.4		2.2		3.5		ns
$t_{ECSU}$	Register clock enable setup time	2.3		2.6		3.0		ns
$t_{ECHO}$	Register clock enable hold time	1.4		2.2		3.5		ns
$t_{COI}$	Register clock to output valid time		0.4		0.5		1.0	ns
$t_{AOI}$	Register async. S/R to output delay		6.0		6.4		7.0	ns
$t_{RAI}$	Register async. S/R recover before clock	5.0		7.5		10.0		ns
$t_{LOGI}$	Internal logic delay		1.0		1.4		1.8	ns
$t_{LOGILP}$	Internal low power logic delay		5.0		6.4		7.3	ns
<b>Feedback Delays</b>								
$t_F$	FastCONNECT II™ feedback delay		1.9		3.5		4.2	ns
<b>Time Adders</b>								
$t_{PTA}$	Incremental product term allocator delay		0.7		0.8		1.0	ns
$t_{SLEW}$	Slew-rate limited delay		3.0		4.0		4.5	ns
<b>Advance</b>				<b>Preliminary</b>				

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

## XC9572XL I/O Pins

Function Block	Macro-cell	PC44	CS48	VQ64	TQ100	BScan Order	Notes
1	1	-	-	-	16	213	
1	2	1	D7	8	13	210	
1	3	-	D4	12	18	207	
1	4	-	-	13	20	204	
1	5	2	D6	9	14	201	
1	6	3	C7	10	15	198	
1	7	-	-	-	25	195	
1	8	4	C6	11	17	192	
1	9	5	B7	15	22	189	[1]
1	10	-	-	18	28	186	
1	11	6	B6	16	23	183	[1]
1	12	-	-	23	33	180	
1	13	-	-	-	36	177	
1	14	7	A7	17	27	174	[1]
1	15	8	A6	19	29	171	
1	16	-	-	-	39	168	
1	17	9	C5	20	30	165	
1	18	-	-	-	40	162	
2	1	-	-	-	87	159	
2	2	35	F4	60	94	156	
2	3	-	-	58	91	153	
2	4	-	-	59	93	150	
2	5	36	G5	61	95	147	
2	6	37	F5	62	96	144	
2	7	-	-	-	3	141	[2]
2	8	38	G6	63	97	138	
2	9	39	G7	64	99	135	[1]
2	10	-	-	1	1	132	
2	11	40	F6	2	4	129	[1]
2	12	-	-	4	6	126	
2	13	-	-	-	8	123	
2	14	42	E6	5	9	120	[3]
2	15	43	E7	6	11	117	
2	16	-	-	-	10	114	
2	17	44	E5	7	12	111	
2	18	-	-	-	92	108	

Note 1: Global control pin.

Note 2: GTS1 for TQ100

Note 3: GTS1 for PC44, CS48, VQ64

Function Block	Macro-cell	PC44	CS48	VQ64	TQ100	BScan Order	Notes
3	1	-	-	-	41	105	
3	2	11	B5	22	32	102	
3	3	-	C4	31	49	99	
3	4	-	-	32	50	96	
3	5	12	A4	24	35	93	
3	6	-	-	34	53	90	
3	7	-	-	-	54	87	
3	8	13	B4	25	37	84	
3	9	14	A3	27	42	81	
3	10	-	D3	39	60	78	
3	11	18	B2	33	52	75	
3	12	-	-	40	61	72	
3	13	-	-	-	63	69	
3	14	19	B1	35	55	66	
3	15	20	C2	36	56	63	
3	16	24	D2	42	64	60	
3	17	22	C3	38	58	57	
3	18	-	-	-	59	54	
4	1	-	-	-	65	51	
4	2	25	E1	43	67	48	
4	3	-	-	46	71	45	
4	4	-	-	47	72	42	
4	5	26	E2	44	68	39	
4	6	-	E4	49	76	36	
4	7	-	-	-	77	33	
4	8	27	F1	45	70	30	
4	9	-	-	-	66	27	
4	10	-	-	51	81	24	
4	11	28	G1	48	74	21	
4	12	-	-	52	82	18	
4	13	-	-	-	85	15	
4	14	29	F2	50	78	12	
4	15	33	E3	56	89	9	
4	16	-	-	-	86	6	
4	17	34	G4	57	90	3	
4	18	-	-	-	79	0	

## XC9572XL Global, JTAG and Power Pins

Pin Type	PC44	CS48	VQ64	TQ100
I/O/GCK1	5	B7	15	22
I/O/GCK2	6	B6	16	23
I/O/GCK3	7	A7	17	27
I/O/GTS1	42	E6	5	3
I/O/GTS2	40	F6	2	4
I/O/GSR	39	G7	64	99
TCK	17	A1	30	48
TDI	15	B3	28	45
TDO	30	G2	53	83
TMS	16	A2	29	47
V <sub>CCINT</sub> 3.3 V	21, 41	C1, F7	3, 37	5, 57, 98
V <sub>CCIO</sub> 2.5 V/3.3 V	32	G3	26, 55	26, 38, 51, 88
GND	10, 23, 31	A5, D1, F3	14, 21, 41, 54	21, 31, 44, 62, 69, 75, 84, 100
No Connects	-	-	-	2, 7, 19, 24, 34, 43, 46, 73, 80



## Ordering Information

**Example:** XC9572XL -7 TQ 100 C

Device Type \_\_\_\_\_

#### - Temperature Range

### Speed Grade

#### – Number of Pins

## **Speed Options**

- 10 10 ns pin-to-pin delay
  - 7 7.5 ns pin-to-pin delay
  - 5 5 ns pin-to-pin delay

#### Packaging Options

PC44 44-Pin Plastic Lead Chip Carrier (PLCC)

CS48 48-Pin Chip Scale Package (CSP)

## VQ64 64-Pin Very Thin Quad Flat Pack (VQFP)

## TQ100 100-Pin Thin Quad Flat Pack (TQFP)

## Temperature Options

C = Commercial T<sub>A</sub> = 0°C to +70°C

I = Industrial       $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

## Component Availability

Pins	44	48	64	100
Type	Plastic PLCC	Plastic CSP	Plastic VQFP	Plastic TQFP
Code	PC44	CS48	VQ64	TQ100
XC9572XL	-10	C, I	-	C, I
	-7	C	C	C
	-5	(C)	-	(C)

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ) I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

( ) Parenthesis indicate future planned products. Please contact Xilinx for up-to-date availability information.

## Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-pin CSP (117 user I/O pins)
- Optimized for high-performance 3.3 V systems
  - Low power operation
  - 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
  - 3.3 V or 2.5 V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000 V
- Pin-compatible with 5 V-core XC95144 device in the 100-pin TQFP package

## Description

The XC95144XL is a 3.3 V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 5 ns. See Figure 2 for architecture overview.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application, and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of  $I_{CC}$ , the following equation may be used:

$$I_{CC} (\text{mA}) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance (default) mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual  $I_{CC}$  value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in graphical form.

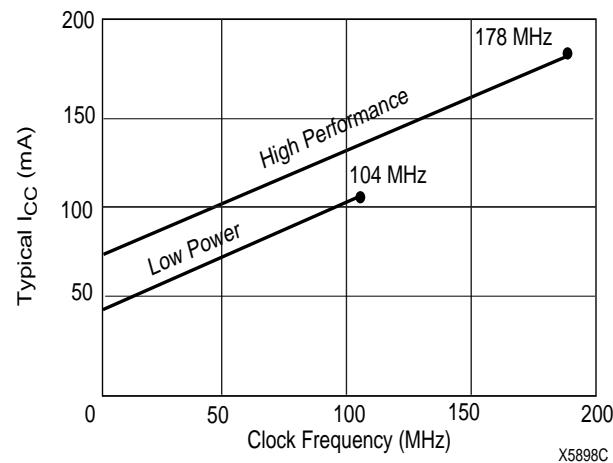
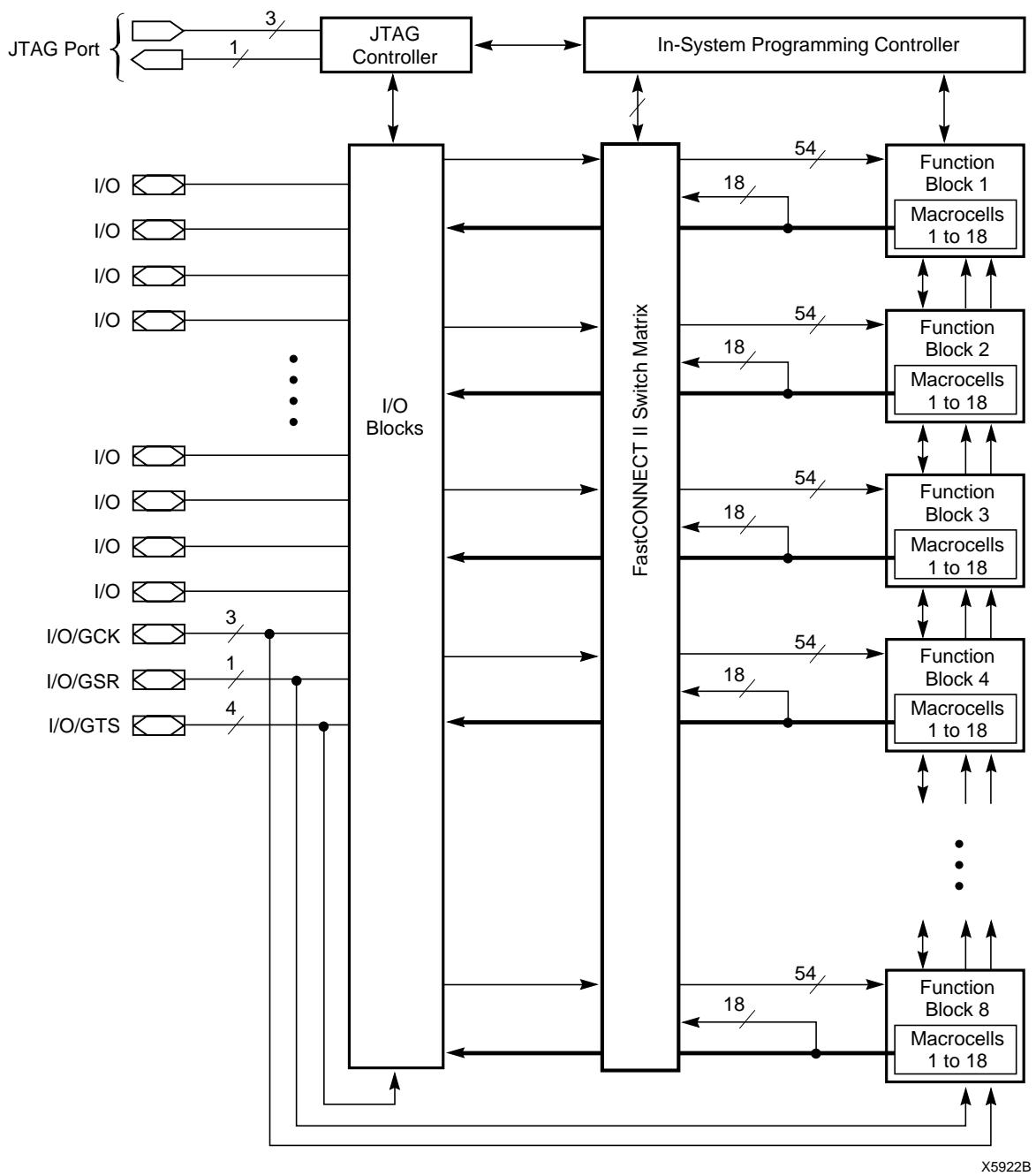


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC95144XL

**Figure 2: XC95144XL Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

Note 1: Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	3.0	3.6	V
		Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers for 3.3 V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5 V operation		2.3	2.7	V
$V_{IL}$	Low-level input voltage		0	0.80	V
$V_{IH}$	High-level input voltage		2.0	5.5	V
$V_O$	Output voltage		0	$V_{CCIO}$	V

## Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles (Endurance)	10,000	-	Cycles
$V_{ESD}$	Electrostatic Discharge (ESD)	2,000	-	Volts

## DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 3.3 V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4		V
	Output high voltage for 2.5 V outputs	$I_{OH} = -500 \mu\text{A}$	90% $V_{CCIO}$		V
$V_{OL}$	Output low voltage for 3.3 V outputs	$I_{OH} = 8.0 \text{ mA}$		0.4	V
	Output low voltage for 2.5 V outputs	$I_{OL} = 500 \mu\text{A}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	45		ma

## AC Characteristics

Symbol	Parameter	XC95144XL-5		XC95144XL-7		XC95144XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	
t <sub>PD</sub>	I/O to output valid		5.0		7.5		10.0	ns
t <sub>SU</sub>	I/O setup time before GCK	3.7		4.8		6.5		ns
t <sub>H</sub>	I/O hold time after GCK	0.0		0.0		0.0		ns
t <sub>CO</sub>	GCK to output valid		3.5		4.5		5.8	ns
f <sub>SYSTEM</sub>	Multiple FB internal operating frequency		178.6		125.0		100.0	MHz
t <sub>PSU</sub>	I/O setup time before p-term clock input	1.7		1.6		2.1		ns
t <sub>PH</sub>	I/O hold time after p-term clock input	2.0		3.2		4.4		ns
t <sub>PCO</sub>	P-term clock output valid		5.5		7.7		10.2	ns
t <sub>OE</sub>	GTS to output valid		4.0		5.0		7.0	ns
t <sub>OD</sub>	GTS to output disable		4.0		5.0		7.0	ns
t <sub>POE</sub>	Product term OE to output enabled		7.0		9.5		11.0	ns
t <sub>POD</sub>	Product term OE to output disabled		7.0		9.5		11.0	ns
t <sub>AO</sub>	GSR to output valid		10.0		12.0		14.5	ns
t <sub>PAO</sub>	P-term S/R to output valid		10.5		12.6		15.3	ns
t <sub>WLH</sub>	GCK pulse width (High or Low)	2.8		4.0		4.5		ns
t <sub>PLH</sub>	P-term clock pulse width (High or Low)	5.0		6.5		7.0		ns
		Advance		Preliminary				

Note 1:Please contact Xilinx for up-to-date information on advance specifications.

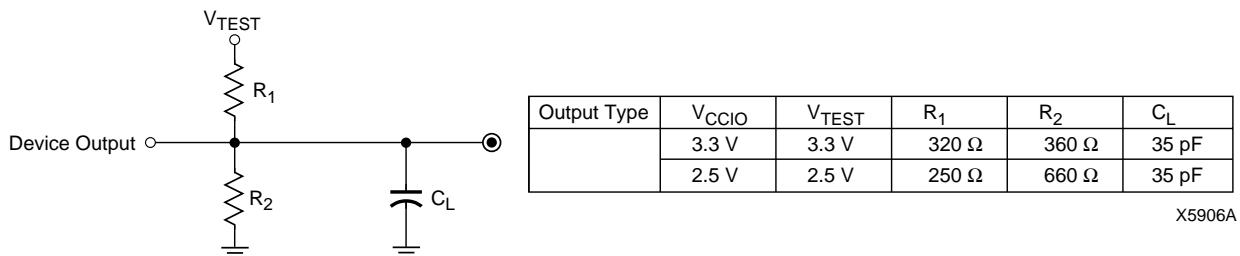


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95144XL-5		XC95144XL-7		XC95144XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min	Max	Min	Max	
<b>Buffer Delays</b>								
$t_{IN}$	Input buffer delay		1.5		2.3		3.5	ns
$t_{GCK}$	GCK buffer delay		1.1		1.5		1.8	ns
$t_{GSR}$	GSR buffer delay		2.0		3.1		4.5	ns
$t_{GTS}$	GTS buffer delay		4.0		5.0		7.0	ns
$t_{OUT}$	Output buffer delay		2.0		2.5		3.0	ns
$t_{EN}$	Output buffer enable/disable delay		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>								
$t_{PTCK}$	Product term clock delay		1.6		2.4		2.7	ns
$t_{PTSR}$	Product term set/reset delay		1.0		1.4		1.8	ns
$t_{PTTS}$	Product term 3-state delay		5.5		7.2		7.5	ns
<b>Internal Register and Combinatorial Delays</b>								
$t_{PDI}$	Combinatorial logic propagation delay		0.5		1.3		1.7	ns
$t_{SUI}$	Register setup time	2.3		2.6		3.0		ns
$t_{HI}$	Register hold time	1.4		2.2		3.5		ns
$t_{ECSU}$	Register clock enable setup time	2.3		2.6		3.0		ns
$t_{ECHO}$	Register clock enable hold time	1.4		2.2		3.5		ns
$t_{COI}$	Register clock to output valid time		0.4		0.5		1.0	ns
$t_{AOI}$	Register async. S/R to output delay		6.0		6.4		7.0	ns
$t_{RAI}$	Register async. S/R recover before clock	5.0		7.5		10.0		ns
$t_{LOGI}$	Internal logic delay		1.0		1.4		1.8	ns
$t_{LOGILP}$	Internal low power logic delay		5.0		6.4		7.3	ns
<b>Feedback Delays</b>								
$t_F$	FastCONNECT II™ feedback delay		1.9		3.5		4.2	ns
<b>Time Adders</b>								
$t_{PTA}$	Incremental product term allocator delay		0.7		0.8		1.0	ns
$t_{SLEW}$	Slew-rate limited delay		3.0		4.0		4.5	ns
<b>Advance</b>				<b>Preliminary</b>				

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

## XC95144XL I/O Pins

Function Block	Macrocell	TQ100	TQ144	CS144	BScan Order	Notes
1	1	-	23	H3	429	
1	2	11	16	F1	426	
1	3	12	17	G2	423	
1	4	-	25	J1	420	
1	5	13	19	G3	417	
1	6	14	20	G4	414	
1	7	-	-	-	411	
1	8	15	21	H1	408	
1	9	16	22	H2	405	
1	10	-	31	K3	402	
1	11	17	24	H4	399	
1	12	18	26	J2	396	
1	13	-	-	-	393	
1	14	19	27	J3	390	
1	15	20	28	J4	387	
1	16	-	35	M1	384	
1	17	22	30	K2	381	[1]
1	18	-	-	-	378	
2	1	-	142	C3	375	
2	2	99	143	A2	372	[1]
2	3	-	-	-	369	
2	4	-	4	C1	366	
2	5	1	2	B1	363	[1]
2	6	2	3	C2	360	[1]
2	7	-	-	-	357	
2	8	3	5	D4	354	[1]
2	9	4	6	D3	351	[1]
2	10	-	7	D2	348	
2	11	6	9	E4	345	
2	12	7	10	E3	342	
2	13	-	12	E1	339	
2	14	8	11	E2	336	
2	15	9	13	F4	333	
2	16	-	14	F3	330	
2	17	10	15	F2	327	
2	18	-	-	-	324	

Note 1: Global control pin.

Function Block	Macrocell	TQ100	TQ144	CS144	BScan Order	Notes
3	1	-	39	M3	321	
3	2	23	32	L1	318	[1]
3	3	-	41	K4	315	
3	4	-	44	N4	312	
3	5	24	33	L2	309	
3	6	25	34	L3	306	
3	7	-	46	L5	303	
3	8	27	38	N2	300	[1]
3	9	28	40	N3	297	
3	10	-	48	N5	294	
3	11	29	43	M4	291	
3	12	30	45	K5	288	
3	13	-	-	-	285	
3	14	32	49	K6	282	
3	15	33	50	L6	279	
3	16	-	-	-	276	
3	17	34	51	M6	273	
3	18	-	-	-	270	
4	1	-	118	C9	267	
4	2	87	126	A7	264	
4	3	-	133	A5	261	
4	4	-	-	-	258	
4	5	89	128	D7	255	
4	6	90	129	A9	252	
4	7	-	-	-	249	
4	8	91	130	B6	246	
4	9	92	131	C6	243	
4	10	-	135	C5	240	
4	11	93	132	D6	237	
4	12	94	134	B5	234	
4	13	-	137	A4	231	
4	14	95	136	D5	228	
4	15	96	138	B4	225	
4	16	-	139	C4	222	
4	17	97	140	A3	219	
4	18	-	-	-	216	

## XC95144XL (Continued)

Function Block	Macrocell	TQ100	TQ144	CS144	BScan Order	Notes
5	1	-	-	-	213	
5	2	35	52	NG	210	
5	3	-	59	L8	207	
5	4	-	-	-	204	
5	5	36	53	M7	201	
5	6	37	54	N7	198	
5	7	-	66	M10	195	
5	8	39	56	K7	192	
5	9	40	57	N8	189	
5	10	-	68	N11	186	
5	11	41	58	M8	183	
5	12	42	60	K8	180	
5	13	-	70	L11	177	
5	14	43	61	N9	174	
5	15	46	64	K9	171	
5	16	-	-	-	168	
5	17	49	69	M11	165	
5	18	-	-	-	162	
6	1	-	-	-	159	
6	2	74	106	C11	156	
6	3	-	-	-	153	
6	4	-	111	B11	150	
6	5	76	110	A12	147	
6	6	77	112	A11	144	
6	7	-	-	-	141	
6	8	78	113	D10	138	
6	9	79	116	A10	135	
6	10	-	115	B10	132	
6	11	80	119	B9	129	
6	12	81	120	A9	126	
6	13	-	-	-	123	
6	14	82	121	D8	120	
6	15	85	124	A8	117	
6	16	-	117	D9	114	
6	17	86	125	B7	111	
6	18	-	-	-	108	

Function Block	Macrocell	TQ100	TQ144	CS144	BScan Order	Notes
7	1	-	-	-	105	
7	2	50	71	N12	102	
7	3	-	75	L12	99	
7	4	-	-	-	96	
7	5	52	74	M13	93	
7	6	53	76	L13	90	
7	7	-	77	K10	87	
7	8	54	78	K11	84	
7	9	55	80	K13	81	
7	10	-	79	K12	78	
7	11	56	82	J11	75	
7	12	58	85	H10	72	
7	13	-	81	J10	69	
7	14	59	86	H11	66	
7	15	60	87	H12	63	
7	16	-	83	J12	60	
7	17	61	88	H13	57	
7	18	-	-	-	54	
8	1	-	-	-	51	
8	2	63	91	G11	48	
8	3	-	95	F11	45	
8	4	-	97	E13	42	
8	5	64	92	G10	39	
8	6	65	93	F13	36	
8	7	-	-	-	33	
8	8	66	94	F12	30	
8	9	67	96	F10	27	
8	10	-	101	D13	24	
8	11	68	98	E12	21	
8	12	70	100	E10	18	
8	13	-	103	D11	15	
8	14	71	102	D12	12	
8	15	72	104	C13	9	
8	16	-	107	B13	6	
8	17	73	105	C12	3	
8	18	-	-	-	0	

## XC95144XL Global, JTAG and Power Pins

Pin Type	TQ100	TQ144	CS144
I/O/GCK1	22	30	K2
I/O/GCK2	23	32	L1
I/O/GCK3	27	38	N2
I/O/GTS1	3	5	D4
I/O/GTS2	4	6	D3
I/O/GTS3	1	2	B1
I/O/GTS4	2	3	C2
I/O/GSR	99	143	A2
TCK	48	67	L10
TDI	45	63	L9
TDO	83	122	C8
TMS	47	65	N10
V <sub>CCINT</sub> 3.3 V	5, 57, 98	8, 42, 84, 141	B3, D1, J13, L4
V <sub>CCIO</sub> 2.5 V/3.3 V	26, 38, 51, 88	1, 37, 55, 73, 109, 127	A1, A13, C7, L7, N1, N13
GND	21, 31, 44, 62, 69, 75, 84, 100	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	B8, B12, C10, E11, G1, G12, G13, K1, M2, M5, M9, M12
No Connects	-	-	-

## Ordering Information

**Example:** XC95144XL -7 TQ 100 C

Device Type \_\_\_\_\_

#### - Temperature Range

### Speed Grade

#### – Number of Pins

### Speed Grade

#### – Package Type

## Speed Options

- 10 10 ns pin-to-pin delay  
-7 7.5 ns pin-to-pin delay  
-5 5 ns pin-to-pin delay

### Packaging Options

- TQ100 100-Pin Thin Quad Flat Pack (TQFP)  
TQ144 144-Pin Thin Quad Flat Pack (TQFP)  
CS144 144-Pin Chip Scale Package (CSP)

## Temperature Options

C= Commercial  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$   
I= Industrial  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

## Component Availability

Pins	100	144	144
Type	Plastic TQFP	Plastic TQFP	Chip Scale Package CSP
Code	TQ100	TQ144	CS144
XC95144XL	-10	C, I	C, I
	-7	C	C
	-5	(C)	(C)

C = Commercial ( $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ) I = Industrial ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

( ) Parenthesis indicate future planned products. Please contact Xilinx for up-to-date availability information.

## Features

- 6 ns pin-to-pin logic delays
- System frequency up to 151 MHz
- 288 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (117 user I/O pins)
  - 208-pin PQFP (168 user I/O pins)
  - 352-pin BGA (192 user I/O pins)
- Optimized for high-performance 3.3 V systems
  - Low power operation
  - 5 V tolerant I/O pins accept 5 V, 3.3 V, and 2.5 V signals
  - 3.3 V or 2.5 V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with 3 global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000 V
- Pin-compatible with 5 V-core XC95288 device in the 208-pin HQFP package

## Description

The XC95288XL is a 3.3 V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of sixteen 54V18 Function Blocks, providing 6,400 usable gates with propagation delays of 6 ns. See Figure 2 for architecture overview.

## Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of  $I_{CC}$ , the following equation may be used:

$$I_{CC} (\text{mA}) = MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance (default) mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual  $I_{CC}$  value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

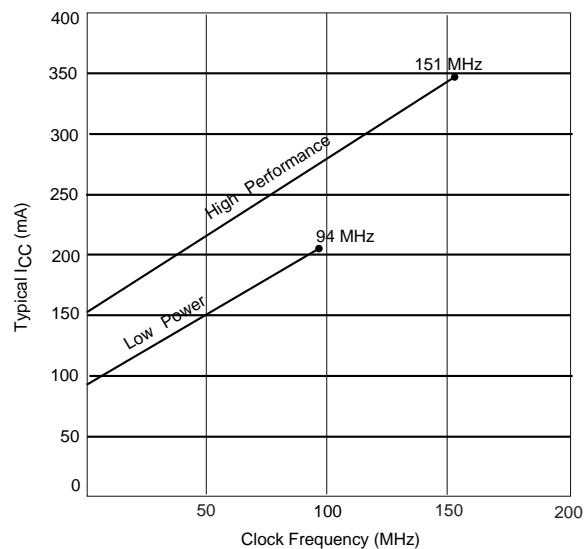
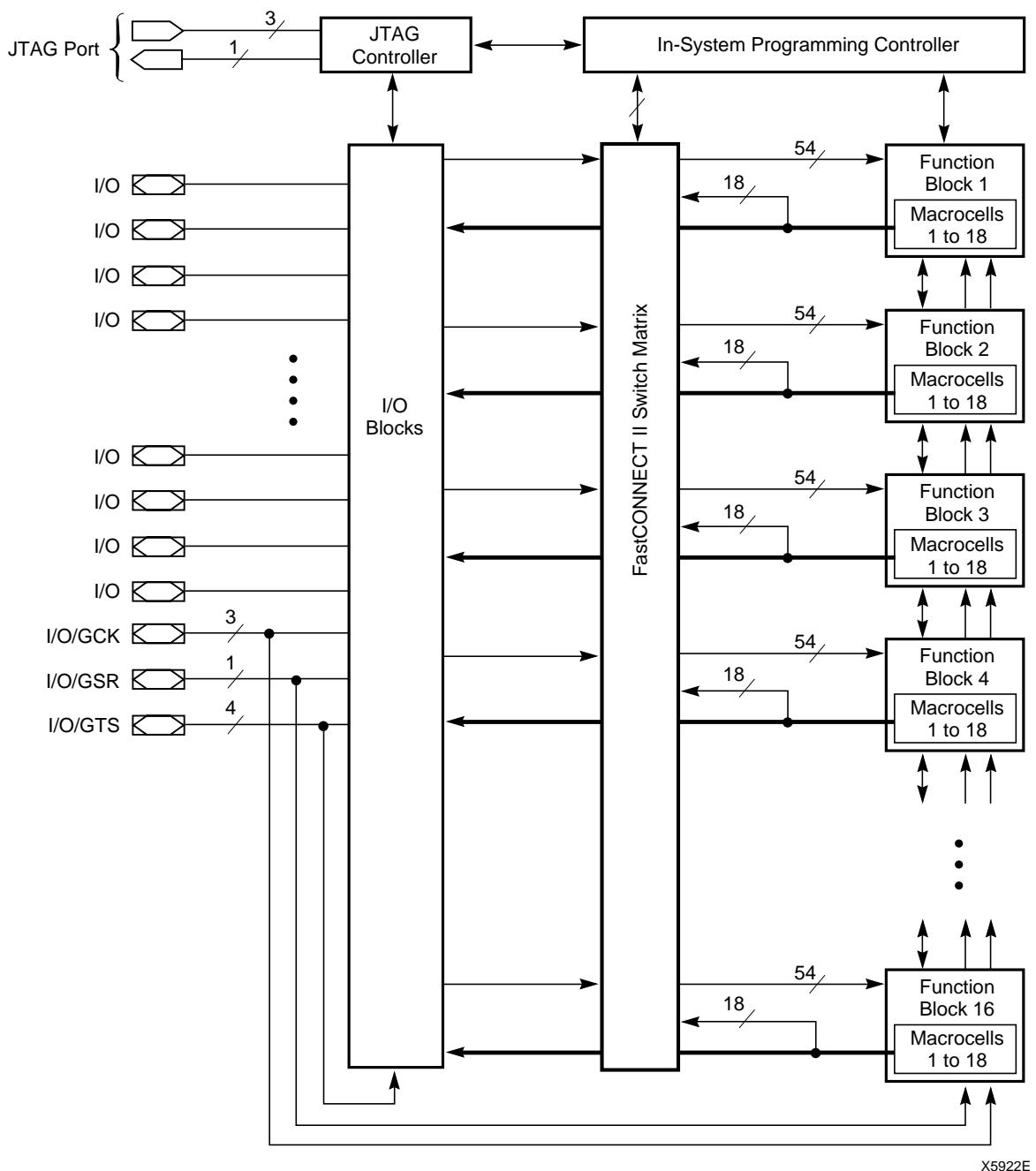


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC95288XL

**Figure 2: XC95288XL Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

Note 1: Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to +7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic	Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	3.0	3.6	V
	and input buffers	Industrial $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	3.0	3.6	V
$V_{CCIO}$	Supply voltage for output drivers for 3.3 V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5 V operation		2.3	2.7	V
$V_{IL}$	Low-level input voltage		0	0.80	V
$V_{IH}$	High-level input voltage		2.0	5.5	V
$V_O$	Output voltage		0	$V_{CCIO}$	V

## Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles (Endurance)	10,000	-	Cycles
$V_{ESD}$	Electrostatic Discharge (ESD)	2,000	-	Volts

## DC Characteristic Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 3.3 V outputs	$I_{OH} = -4.0 \text{ mA}$	2.4		V
	Output high voltage for 2.5 V outputs	$I_{OH} = -500 \mu\text{A}$	90% $V_{CCIO}$		V
$V_{OL}$	Output low voltage for 3.3 V outputs	$I_{OL} = 8.0 \text{ mA}$		0.4	V
	Output low voltage for 2.5 V outputs	$I_{OL} = 500 \mu\text{A}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{cc}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	85(Typ)		mA

## AC Characteristics

Symbol	Parameter	XC95288XL-6		XC95288XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min <sup>1</sup>	Max <sup>1</sup>	
t <sub>PD</sub>	I/O to output valid		6.0		10.0	ns
t <sub>SU</sub>	I/O setup time before GCK	4.1		6.5		ns
t <sub>H</sub>	I/O hold time after GCK	0.0		0.0		ns
t <sub>CO</sub>	GCK to output valid		4.3		5.8	ns
f <sub>SYSTEM</sub>	Multiple FB internal operating frequency		151.5		100.0	MHz
t <sub>PSU</sub>	I/O setup time before p-term clock input	2.1		2.1		ns
t <sub>PH</sub>	I/O hold time after p-term clock input	2.0		4.4		ns
t <sub>PCO</sub>	P-term clock output valid		6.3		10.2	ns
t <sub>OE</sub>	GTS to output valid		4.5		7.0	ns
t <sub>OD</sub>	GTS to output disable				7.0	ns
t <sub>POE</sub>	Product term OE to output enabled		8.0		11.0	ns
t <sub>POD</sub>	Product term OE to output disabled				11.0	ns
t <sub>AO</sub>	GSR to output valid		10.8		14.5	ns
t <sub>PAO</sub>	P-term S/R to output valid		11.6		15.3	ns
t <sub>WLH</sub>	GCK pulse width (High or Low)	3.3		4.5		ns
t <sub>PLH</sub>	P-term clock pulse width (High or Low)	6.0		7.0		ns
<b>Advance</b>						

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

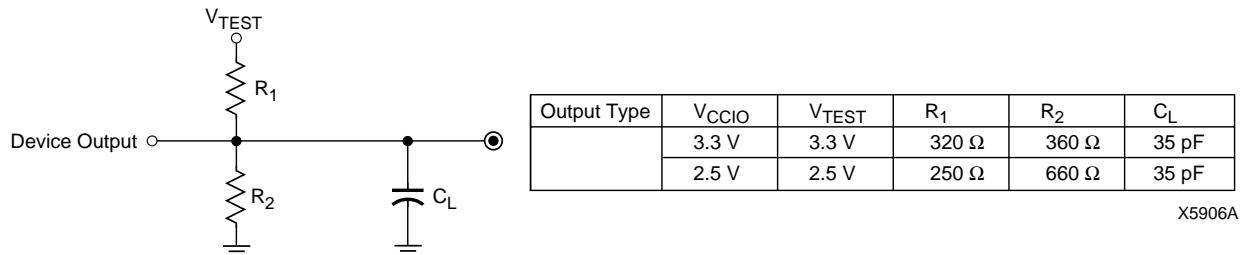


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95288XL-6		XC95288XL-10		Units
		Min <sup>1</sup>	Max <sup>1</sup>	Min <sup>1</sup>	Max <sup>1</sup>	
<b>Buffer Delays</b>						
t <sub>IN</sub>	Input buffer delay		1.8		3.5	ns
t <sub>GCK</sub>	GCK buffer delay		1.4		1.8	ns
t <sub>GSR</sub>	GSR buffer delay		2.2		4.5	ns
t <sub>GTS</sub>	GTS buffer delay		4.5		7.0	ns
t <sub>OUT</sub>	Output buffer delay		2.4		3.0	ns
t <sub>EN</sub>	Output buffer enable/disable delay		0.0		0.0	ns
<b>Product Term Control Delays</b>						
t <sub>PTCK</sub>	Product term clock delay		1.6		2.7	ns
t <sub>PTSR</sub>	Product term set/reset delay		1.2		1.8	ns
t <sub>PTTS</sub>	Product term 3-state delay		6.2		7.5	ns
<b>Internal Register and Combinatorial Delays</b>						
t <sub>PDI</sub>	Combinatorial logic propagation delay		0.6		1.7	ns
t <sub>SUI</sub>	Register setup time	2.5		3.0		ns
t <sub>HI</sub>	Register hold time	1.6		3.5		ns
t <sub>ECSU</sub>	Register clock enable setup time	2.5		3.0		ns
t <sub>ECHO</sub>	Register clock enable hold time	1.6		3.5		ns
t <sub>COI</sub>	Register clock to output valid time		0.5		1.0	ns
t <sub>AOI</sub>	Register async. S/R to output delay		6.2		7.0	ns
t <sub>RAI</sub>	Register async. S/R recover before clock			10.0		ns
t <sub>LOGI</sub>	Internal logic delay		1.2		1.8	ns
t <sub>LOGILP</sub>	Internal low power logic delay		5.2		7.3	ns
<b>Feedback Delays</b>						
t <sub>F</sub>	FastCONNECT II™ feedback delay		2.4		4.2	ns
<b>Time Adders</b>						
t <sub>PTA</sub>	Incremental product term allocator delay		0.8		1.0	ns
t <sub>SLEW</sub>	Slew-rate limited delay		3.5		4.5	ns
<b>Advance</b>						

Note 1: Please contact Xilinx for up-to-date information on advance specifications.

**XC95288XL I/O Pins**

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes	Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
1	1	—	—	—	861		3	1	—	—	—	753	
1	2	—	28	N26	858		3	2	28	38	U24	750	
1	3	—	29	P25	855		3	3	—	39	U23	747	
1	4	—	—	—	852		3	4	—	—	—	744	
1	5	20	30	P23	849		3	5	—	40	Y26	741	
1	6	21	31	P24	846		3	6	—	41	W25	738	
1	7	—	—	—	843		3	7	—	—	—	735	
1	8	22	32	R26	840		3	8	—	43	AA26	732	
1	9	—	—	R25	837		3	9	—	—	Y25	729	
1	10	23	33	R24	834		3	10	30	44	Y24	726	[1]
1	11	—	—	R23	831		3	11	—	—	AA25	723	
1	12	24	34	T26	828		3	12	31	45	AB25	720	
1	13	—	—	—	825		3	13	—	—	—	717	
1	14	25	35	T25	822		3	14	32	46	AA24	714	[1]
1	15	26	36	T23	819		3	15	33	47	Y23	711	
1	16	—	—	—	816		3	16	—	—	—	708	
1	17	27	37	V26	813		3	17	—	48	AC26	705	
1	18	—	—	—	810		3	18	—	—	—	702	
2	1	—	—	—	807		4	1	—	—	—	699	
2	2	9	15	K23	804		4	2	2	3	E23	696	[1]
2	3	10	16	K24	801		4	3	—	4	C26	693	
2	4	—	—	—	798		4	4	—	—	—	690	
2	5	11	17	J25	795		4	5	3	5	E24	687	[1]
2	6	12	18	L24	792		4	6	4	6	F24	684	
2	7	—	—	—	789		4	7	—	—	—	681	
2	8	13	19	K25	786		4	8	5	7	E25	678	[1]
2	9	—	—	L25	783		4	9	—	—	D26	675	
2	10	14	20	L26	780		4	10	—	8	G24	672	
2	11	—	—	M23	777		4	11	—	—	F25	669	
2	12	15	21	M24	774		4	12	6	9	F26	666	[1]
2	13	—	—	—	771		4	13	—	—	—	663	
2	14	16	22	M25	768		4	14	7	10	H23	660	
2	15	17	23	M26	765		4	15	—	12	G26	657	
2	16	—	—	—	762		4	16	—	—	—	654	
2	17	19	25	N25	759		4	17	—	14	H25	651	
2	18	—	—	—	756		4	18	—	—	—	648	

**Notes:** [1] Global control pin

## XC95288XL I/O Pins (continued)

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes	Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
5	1	—	—	—	645		7	1	—	—	—	537	
5	2	34	49	AA23	642		7	2	—	62	AC19	534	
5	3	—	50	AB24	639		7	3	45	63	AD19	531	
5	4	—	—	—	636		7	4	—	—	—	528	
5	5	35	51	AD25	633		7	5	46	64	AE20	525	
5	6	—	54	AE24	630		7	6	—	66	AC18	522	
5	7	—	—	—	627		7	7	—	—	—	519	
5	8	38	55	AD23	624	[1]	7	8	—	67	AD18	516	
5	9	—	—	AC22	621		7	9	—	—	AE19	513	
5	10	39	56	AF24	618		7	10	—	69	AD17	510	
5	11	—	—	AD22	615		7	11	—	—	AE18	507	
5	12	40	57	AE23	612		7	12	48	70	AF18	504	
5	13	—	—	—	609		7	13	—	—	—	501	
5	14	41	58	AE22	606		7	14	—	71	AE17	498	
5	15	43	60	AE21	603		7	15	49	72	AE16	495	
5	16	—	—	—	600		7	16	—	—	—	492	
5	17	44	61	AF21	597		7	17	—	73	AF16	489	
5	18	—	—	—	594		7	18	—	—	—	486	
6	1	—	—	—	591		8	1	—	—	—	483	
6	2	135	197	C19	588		8	2	130	186	A15	480	
6	3	136	198	D18	585		8	3	131	187	B15	477	
6	4	—	—	—	582		8	4	—	—	—	474	
6	5	137	199	A21	579		8	5	132	188	C15	471	
6	6	138	200	B20	576		8	6	—	189	D15	468	
6	7	—	—	—	573		8	7	—	—	—	465	
6	8	139	201	C20	570		8	8	133	191	A16	462	
6	9	—	—	B21	567		8	9	—	—	B16	459	
6	10	140	202	B22	564		8	10	134	192	C16	456	
6	11	—	—	C21	561		8	11	—	—	B17	453	
6	12	—	203	D20	558		8	12	—	193	C17	450	
6	13	—	—	—	555		8	13	—	—	—	447	
6	14	142	205	B24	552		8	14	—	194	B18	444	
6	15	143	206	C23	549	[1]	8	15	—	195	A20	441	
6	16	—	—	—	546		8	16	—	—	—	438	
6	17	—	208	D22	543		8	17	—	196	B19	435	
6	18	—	—	—	540		8	18	—	—	—	432	

Note: [1] Global control pin

**XC95288XL I/O Pins (continued)**

Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes	Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
9	1	—	—	—	429		11	1	—	—	—	321	
9	2	50	74	AE14	426		11	2	—	87	AD9	318	
9	3	51	75	AF14	423		11	3	60	88	AC10	315	
9	4	—	—	—	420		11	4	—	—	—	312	
9	5	52	76	AE13	417		11	5	61	89	AF7	309	
9	6	53	77	AC13	414		11	6	—	90	AE8	306	
9	7	—	—	—	411		11	7	—	—	—	303	
9	8	54	78	AD13	408		11	8	—	91	AD8	300	
9	9	—	—	AF12	405		11	9	—	—	AE7	297	
9	10	—	80	AE12	402		11	10	64	95	AD7	294	
9	11	56	82	AD12	399		11	11	66	97	AE5	291	
9	12	57	83	AC12	396		11	12	68	99	AC7	288	
9	13	—	—	—	393		11	13	—	—	—	285	
9	14	58	84	AF11	390		11	14	69	100	AE3	282	
9	15	—	85	AE11	387		11	15	—	101	AD4	279	
9	16	—	—	—	384		11	16	—	—	—	276	
9	17	59	86	AE9	381		11	17	70	102	AC5	273	
9	18	—	—	—	378		11	18	—	—	—	270	
10	1	—	—	—	375		12	1	—	—	—	267	
10	2	117	170	C10	372		12	2	110	158	B3	264	
10	3	118	171	B9	369		12	3	111	159	A3	261	
10	4	—	—	—	366		12	4	—	—	—	258	
10	5	119	173	A9	363		12	5	112	160	D6	255	
10	6	120	174	D11	360		12	6	—	161	C6	252	
10	7	—	—	—	357		12	7	—	—	—	249	
10	8	121	175	B11	354		12	8	113	162	B5	246	
10	9	—	—	A11	351		12	9	—	—	A4	243	
10	10	124	178	C12	348		12	10	115	164	B6	240	
10	11	125	179	B12	345		12	11	—	165	A6	237	
10	12	126	180	A12	342		12	12	116	166	D8	234	
10	13	—	—	—	339		12	13	—	—	—	231	
10	14	128	182	A13	336		12	14	—	167	B7	228	
10	15	—	183	B14	333		12	15	—	168	A7	225	
10	16	—	—	—	330		12	16	—	—	—	222	
10	17	129	185	C14	327		12	17	—	169	D9	219	
10	18	—	—	—	324		12	18	—	—	—	216	

## XC95288XL I/O Pins (continued)

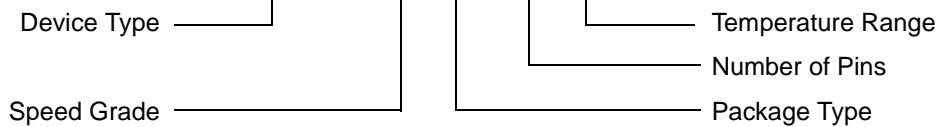
Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes	Function Block	Macrocell	TQ144	PQ208	BG352	BScan Order	Notes
13	1	—	—	—	213		15	1	—	—	—	105	
13	2	71	103	AD3	210		15	2	79	117	V3	102	
13	3	—	106	AD2	207		15	3	80	118	W2	99	
13	4	—	—	—	204		15	4	—	—	—	96	
13	5	—	107	AC3	201		15	5	—	119	U4	93	
13	6	—	109	AD1	198		15	6	—	120	U3	90	
13	7	—	—	—	195		15	7	—	—	—	87	
13	8	74	110	AA4	192		15	8	81	121	V2	84	
13	9	—	—	AA3	189		15	9	—	—	V1	81	
13	10	—	111	AB2	186		15	10	82	122	U2	78	
13	11	75	112	AC1	183		15	11	83	123	T2	75	
13	12	—	113	AA2	180		15	12	85	125	R4	72	
13	13	—	—	—	177		15	13	—	—	—	69	
13	14	76	114	AA1	174		15	14	86	126	R3	66	
13	15	77	115	Y1	171		15	15	87	127	R2	63	
13	16	—	—	—	168		15	16	—	—	—	60	
13	17	78	116	V4	165		15	17	88	128	R1	57	
13	18	—	—	—	162		15	18	—	—	—	54	
14	1	—	—	—	159		16	1	—	—	—	51	
14	2	—	144	K3	156		16	2	91	131	P1	48	
14	3	100	145	G1	153		16	3	92	133	N2	45	
14	4	—	—	—	150		16	4	—	—	—	42	
14	5	101	146	H2	147		16	5	93	134	N4	39	
14	6	102	147	H3	144		16	6	94	135	N3	36	
14	7	—	—	—	141		16	7	—	—	—	33	
14	8	103	148	J4	138		16	8	95	136	M1	30	
14	9	—	—	F1	135		16	9	—	—	M2	27	
14	10	104	149	G2	132		16	10	96	137	M3	24	
14	11	105	150	G3	129		16	11	97	138	M4	21	
14	12	—	151	F2	126		16	12	98	139	L1	18	
14	13	—	—	—	123		16	13	—	—	—	15	
14	14	106	152	E2	120		16	14	—	140	L2	12	
14	15	107	154	D2	117		16	15	—	142	L3	9	
14	16	—	—	—	114		16	16	—	—	—	6	
14	17	—	155	F4	111		16	17	—	143	J1	3	
14	18	—	—	—	108		16	18	—	—	—	0	

## XC95288XL Global, JTAG and Power Pins

Pin Type	TQ144	PQ208	BG352
I/O/GCK1	30	44	Y24
I/O/GCK2	32	46	AA24
I/O/GCK3	38	55	AD23
I/O/GTS1	5	7	E25
I/O/GTS2	6	9	F26
I/O/GTS3	2	3	E23
I/O/GTS4	3	5	E24
I/O/GSR	143	206	C23
TCK	67	98	AD6
TDI	63	94	AF6
TDO	122	176	D12
TMS	65	96	AE6
V <sub>CCINT</sub> 3.3V	8, 42, 84, 141	11, 59, 124, 153, 204	J23, V24, AF23, AC15, AF15, AD11, AD5, Y3, T1, J3, G4, D5, D10, B13, D17, C22, H24
V <sub>CCIO</sub> 2.5V/3.3 V	1, 37, 55, 73, 109, 127	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184	A10, A17, B2, B25, D7, D13, D19, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC8, AC14, AC20, AE25, AF10, AF17
GND	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	2, 13, 24, 27, 42, 52, 68, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, C7, C9, C13, C18, D24, E1, E26, H1, H26, K4, N1, N24, P3, P26, V23, W1, W4, W26, AB1, AB4, AB26, AC9, AD10, AD14, AD15, AD20, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26
No Connects	—	—	A18, A23, A24, B4, B8, B10, B23, C1, C2, C3, C4, C5, C8, C11, C24, C25, D1, D3, D4, D14, D16, D21, D23, D25, E3, E4, F3, F23, G25, J2, J24, J26, K2, L4, L23, P2, T3, T4, T24, U25, V25, W3, W24, Y2, AB3, AB23, AC2, AC4, AC6, AC11, AC16, AC17, AC21, AC23, AC24, AC25, AD16, AD21, AD24, AD26, AE2, AE4, AE10, AE15, AF3, AF4, AF9, AF20

## Ordering Information

**Example: XC95288XL -6 TQ 144 C**



### Speed Options

- 10 10 ns pin-to-pin delay
- 6 6 ns pin-to-pin delay

### Packaging Options

- TQ144 144-Pin Thin Quad Flat Pack (TQFP)
- PQ208 208-Pin Plastic Quad Flat Pack (PQFP)
- BG352 352-Pin Plastic Ball Grid Array (BGA)

### Temperature Options

- C = Commercial  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$
- I = Industrial  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

## Component Availability

Pins	144	208	352
Type	Plastic TQFP	Plastic PQFP	Plastic BGA
Code	<b>TQ144</b>	<b>PQ208</b>	<b>BG352</b>
XC95288XL	-10	C, I	C, I
	-6	(C)	(C)

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ) I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

( ) Parenthesis indicate future product plans. Please contact Xilinx for up-to-date availability information.

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January 16, 1998 (Version 2.1)

Product Information

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## Features

- High-performance
  - 5 ns pin-to-pin logic delays on all pins
  - $f_{CPLD}$  to 125 MHz
- Large density range
  - 36 to 288 macrocells with 800 to 6,400 usable gates
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-5, -7, -10 speed grades)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of multiple XC9500 devices

## Family Overview

The XC9500 CPLD family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration. All devices are in-system programmable for a minimum of 10,000 program/erase cycles. Extensive IEEE 1149.1 (JTAG) boundary-scan support is also included on all family members.

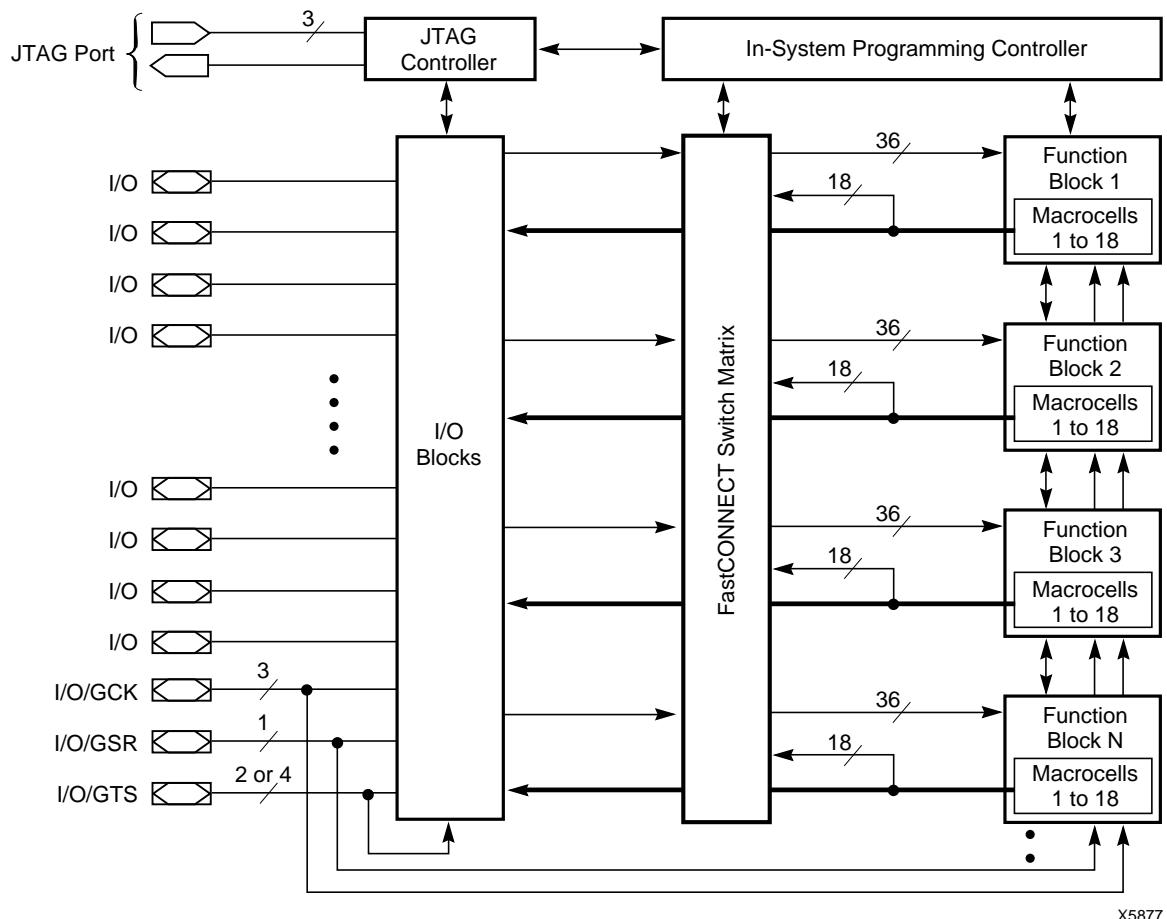
As shown in Table 1, logic density of the XC9500 devices ranges from 800 to over 6,400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500 family is fully pin-compatible allowing easy design migration across multiple density options in a given package footprint.

The XC9500 architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. An expanded JTAG instruction set allows version control of programming patterns and in-system debugging. In-system programming throughout the full device operating range and a minimum of 10,000 program/erase cycles provide worry-free reconfigurations and system field upgrades.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. I/Os may be configured for 3.3 V or 5 V operation. All outputs provide 24 mA drive.

## Architecture Description

Each XC9500 device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with 36 inputs and 18 outputs. The FastCONNECT switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, 12 to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.



X5877

**Figure 1: XC9500 Architecture**

**Note:** Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

**Table 1: XC9500 Device Family**

	<b>XC9536</b>	<b>XC9572</b>	<b>XC95108</b>	<b>XC95144</b>	<b>XC95216</b>	<b>XC95288</b>
Macrocells	36	72	108	144	216	288
Usable Gates	800	1,600	2,400	3,200	4,800	6,400
Registers	36	72	108	144	216	288
$t_{PD}$ (ns)	5	7.5	7.5	7.5	10	15
$t_{SU}$ (ns)	4.5	5.5	5.5	5.5	6.5	8.0
$t_{CO}$ (ns)	4.5	5.5	5.5	5.5	6.5	8.0
$f_{CNT}$ (MHz)	100	125	125	125	111	95
$f_{SYSTEM}$ (MHz)	100	83	83	83	67	56

**Note:**  $f_{CNT}$  = Operating frequency for 16-bit counters

$f_{SYSTEM}$  = Internal operating frequency for general purpose system designs spanning multiple FBs.

**Table 2: Available Packages and Device I/O Pins (not including dedicated JTAG pins)**

	<b>XC9536</b>	<b>XC9572</b>	<b>XC95108</b>	<b>XC95144</b>	<b>XC95216</b>	<b>XC95288</b>
44-Pin VQFP	34					
44-Pin PLCC	34	34				
84-Pin PLCC		69	69			
100-Pin TQFP		72	81	81		
100-Pin PQFP		72	81	81		
160-Pin PQFP			108	133	133	
208-Pin HQFP					166	168
352-Pin BGA					166	192

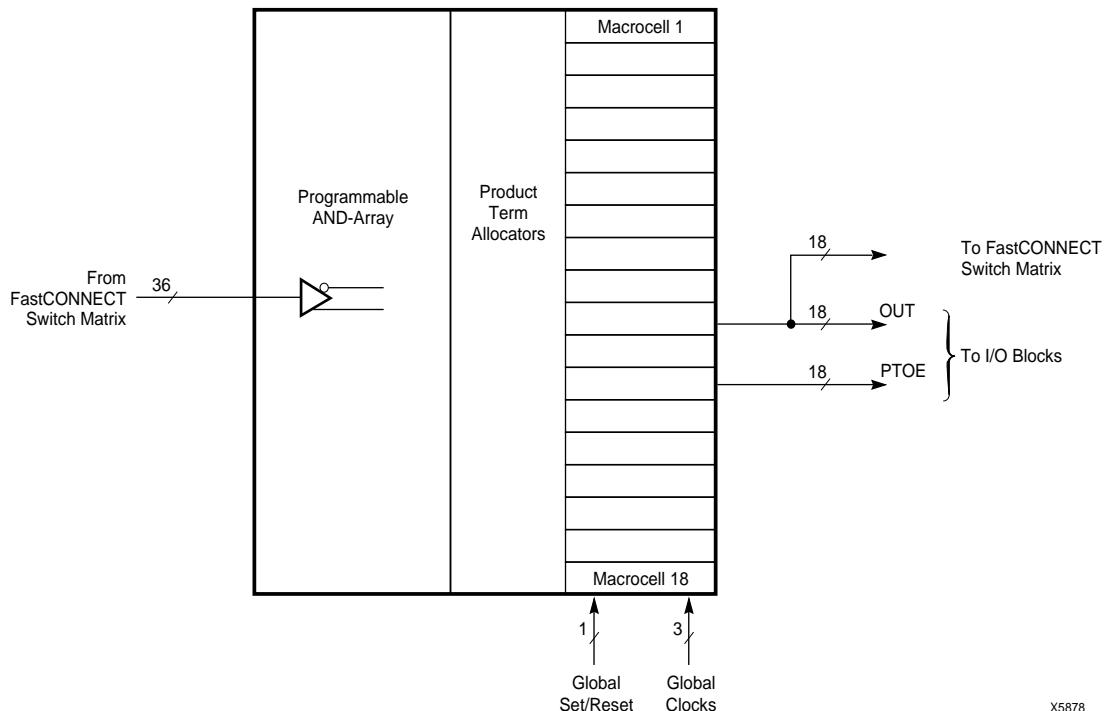
## Function Block

Each Function Block, as shown in Figure 2, is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Thirty-six inputs provide 72 true and complement signals into the programmable AND-array to

form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

Each FB (except for the XC9536) supports local feedback paths that allow any number of FB outputs to drive into its own programmable AND-array without going outside the FB. These paths are used for creating very fast counters and state machines where all state registers are within the same FB.



**Figure 2: XC9500 Function Block**

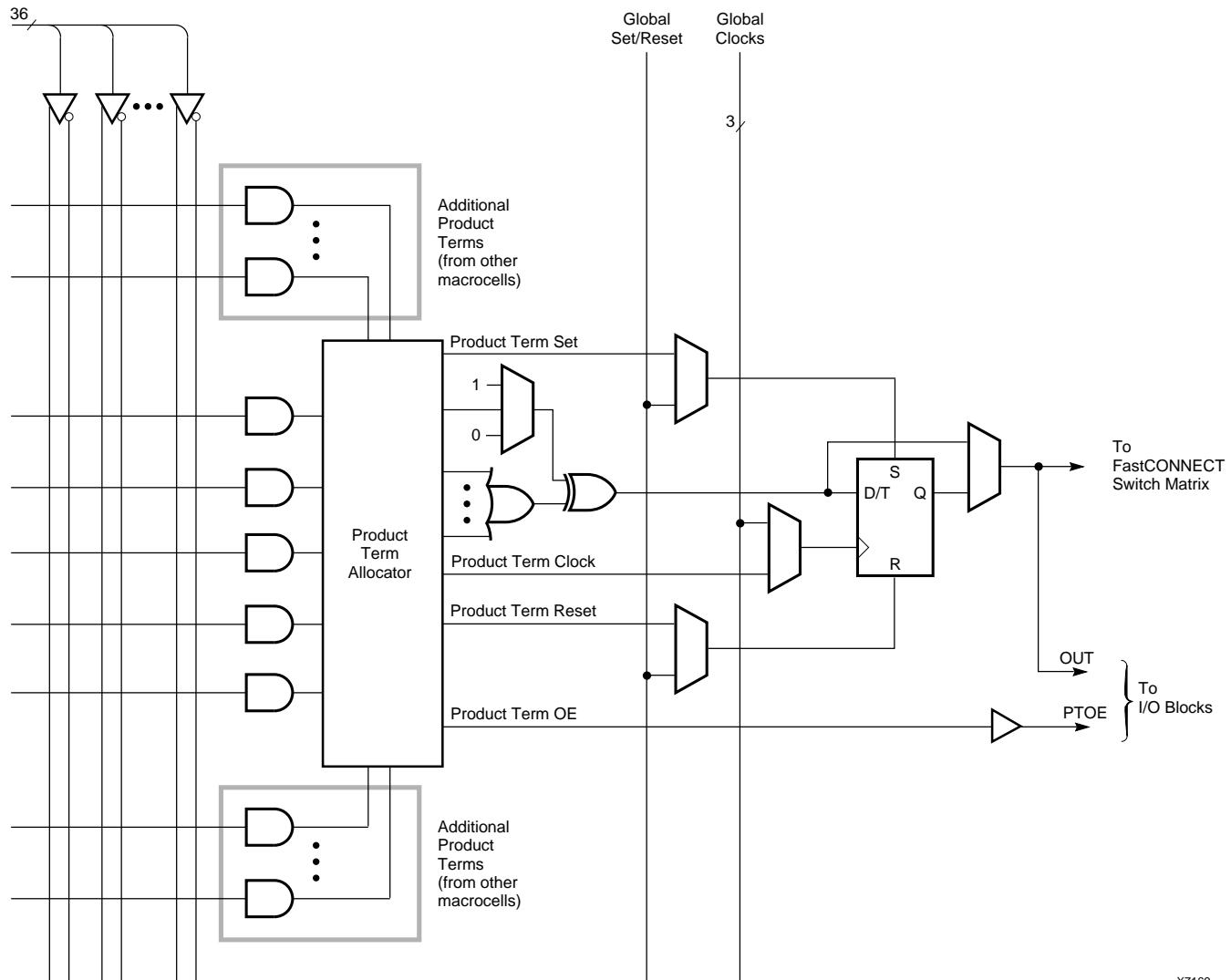
## Macrocell

Each XC9500 macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, set/reset, and output enable. The product

term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

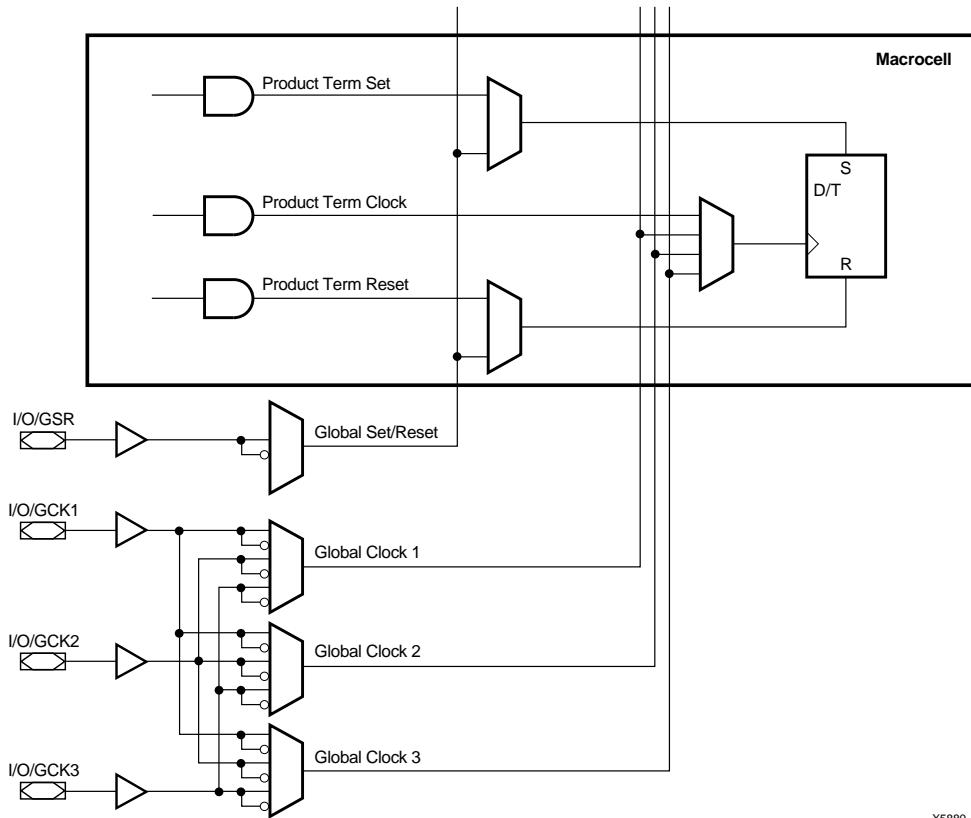


**Figure 3: XC9500 Macrocell Within Function Block**

X7169

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product

term clock. Both true and complement polarities of a GCK pin can be used within the device. A GSR input is also provided to allow user registers to be set to a user-defined state.

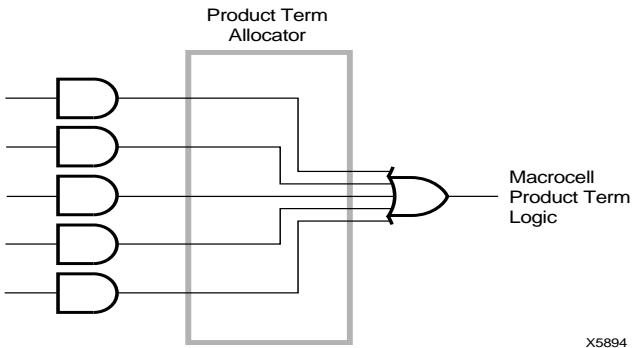


X5680

**Figure 4: Macrocell Clock and Set/Reset Capability**

## Product Term Allocator

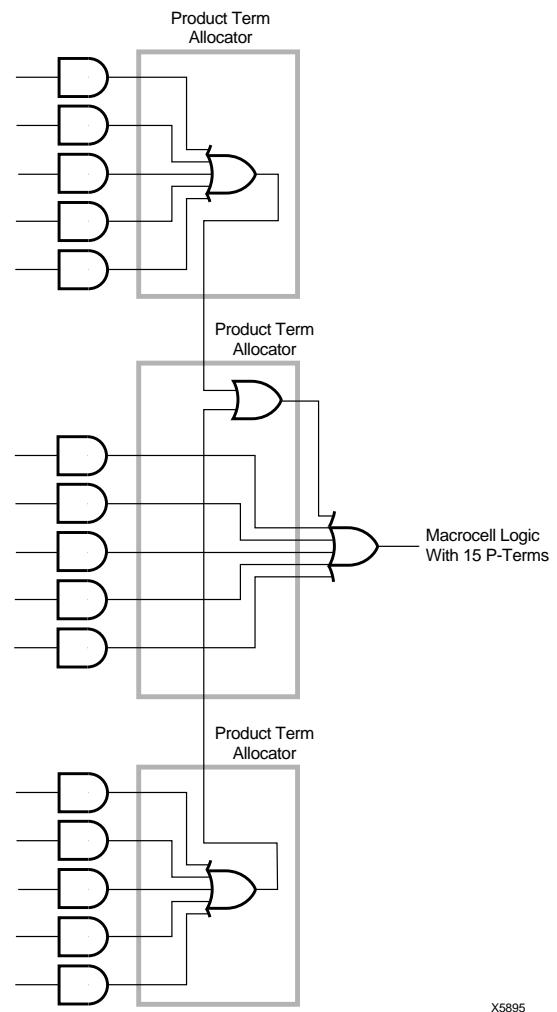
The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.



**Figure 5: Macrocell Logic Using Direct Product Term**

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of  $t_{PTA}$ , as shown in Figure 6.

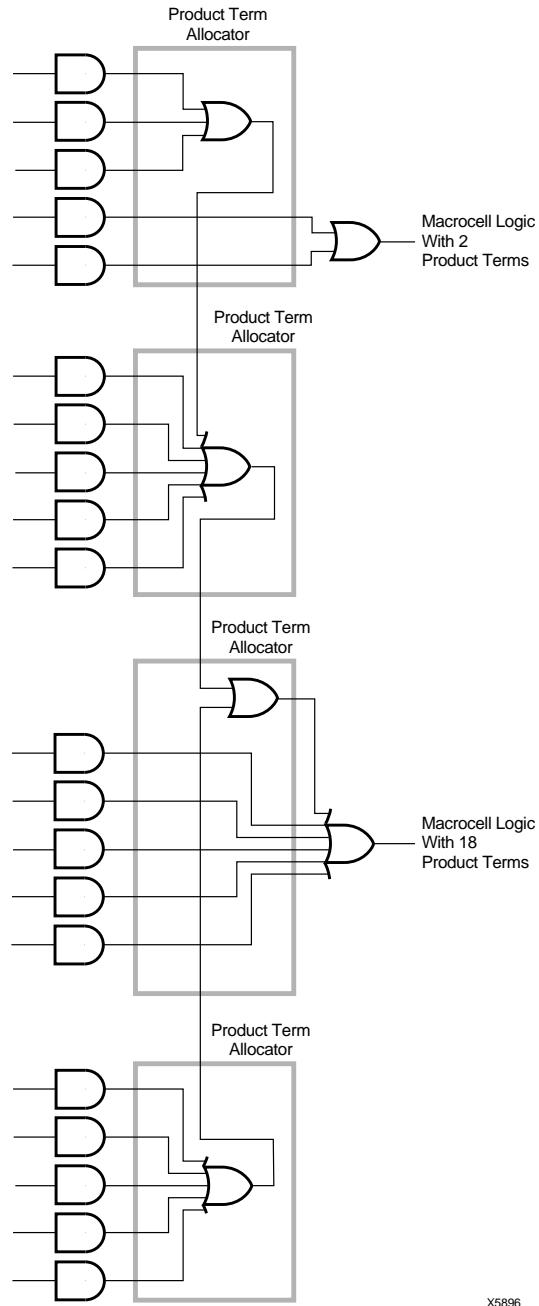
Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed.



**Figure 6: Product Term Allocation With 15 Product Terms**

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7.

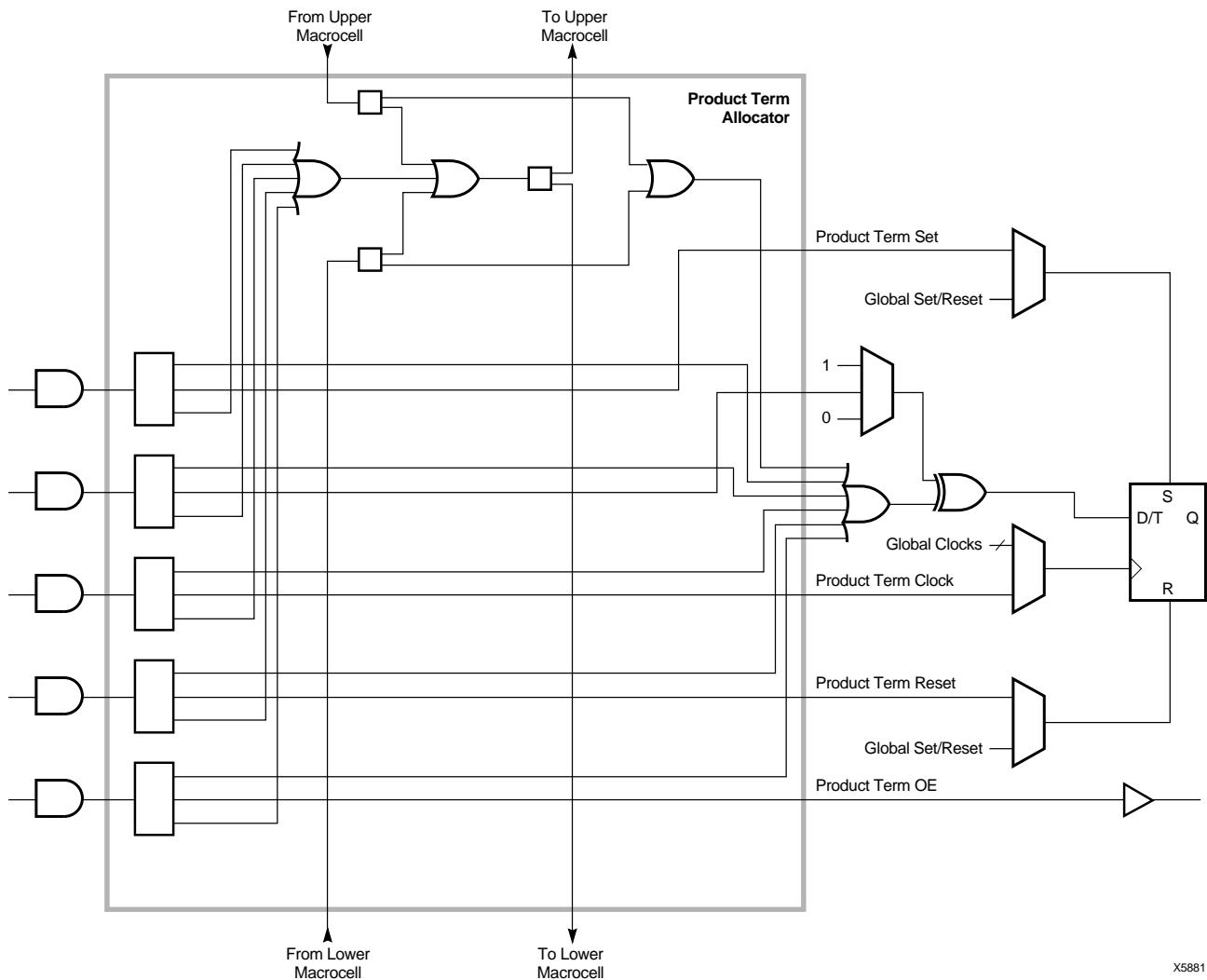
In this example, the incremental delay is only  $2 \cdot t_{PTA}$ . All 90 product terms are available to any macrocell, with a maximum incremental delay of  $8 \cdot t_{PTA}$ .



X5896

**Figure 7: Product Term Allocation Over Several Macrocells**

The internal logic of the product term allocator is shown in Figure 8.



**Figure 8: Product Term Allocator Logic**

## FastCONNECT Switch Matrix

The FastCONNECT switch matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT matrix. Any of these (up to a FB fan-in limit of 36) may be selected, through user programming, to drive each FB with a uniform delay.

The FastCONNECT switch matrix is capable of combining multiple internal connections into a single wired-AND output before driving the destination FB. This provides additional logic capability and increases the effective logic fan-in of the destination FB without any additional timing delay. This capability is available for internal connections originating from FB outputs only. It is automatically invoked by the development software where applicable.

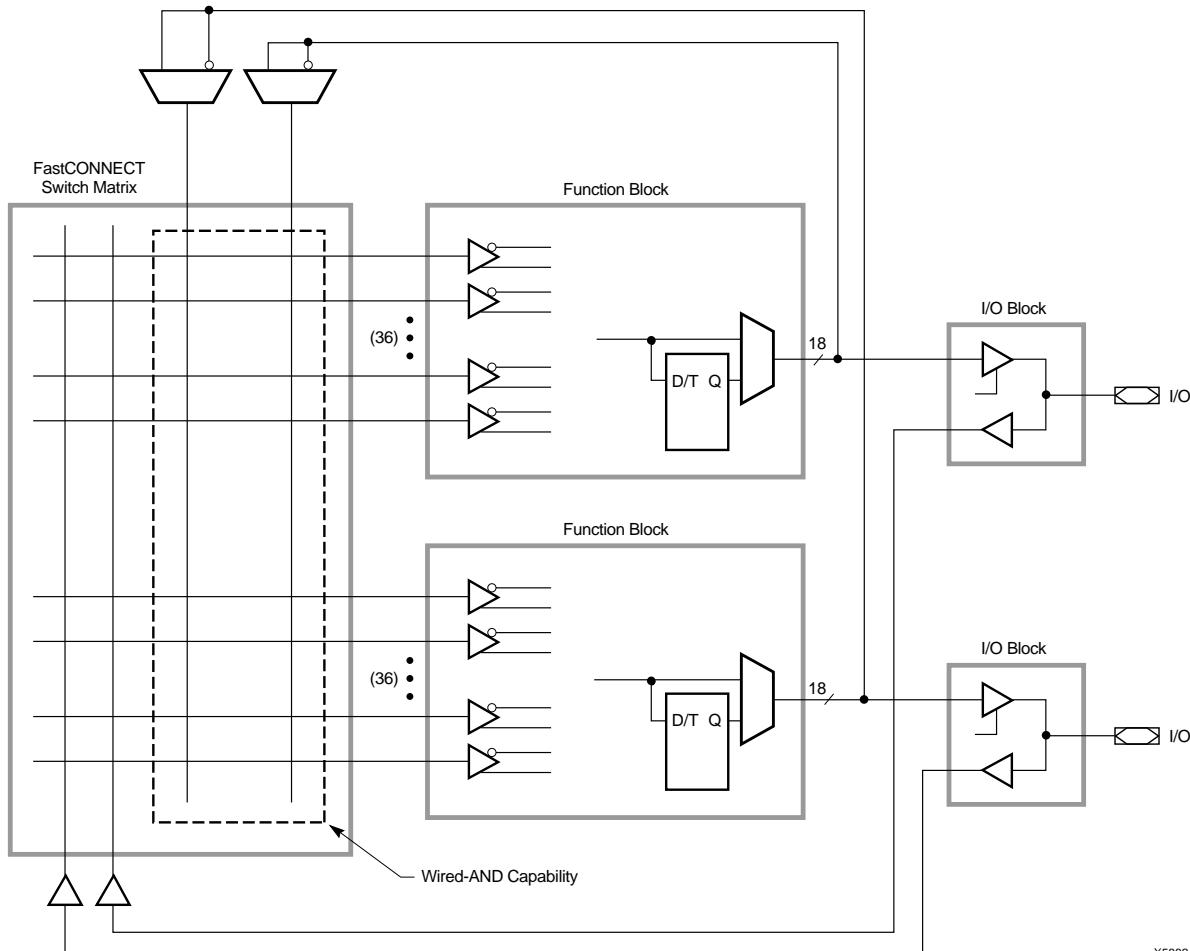


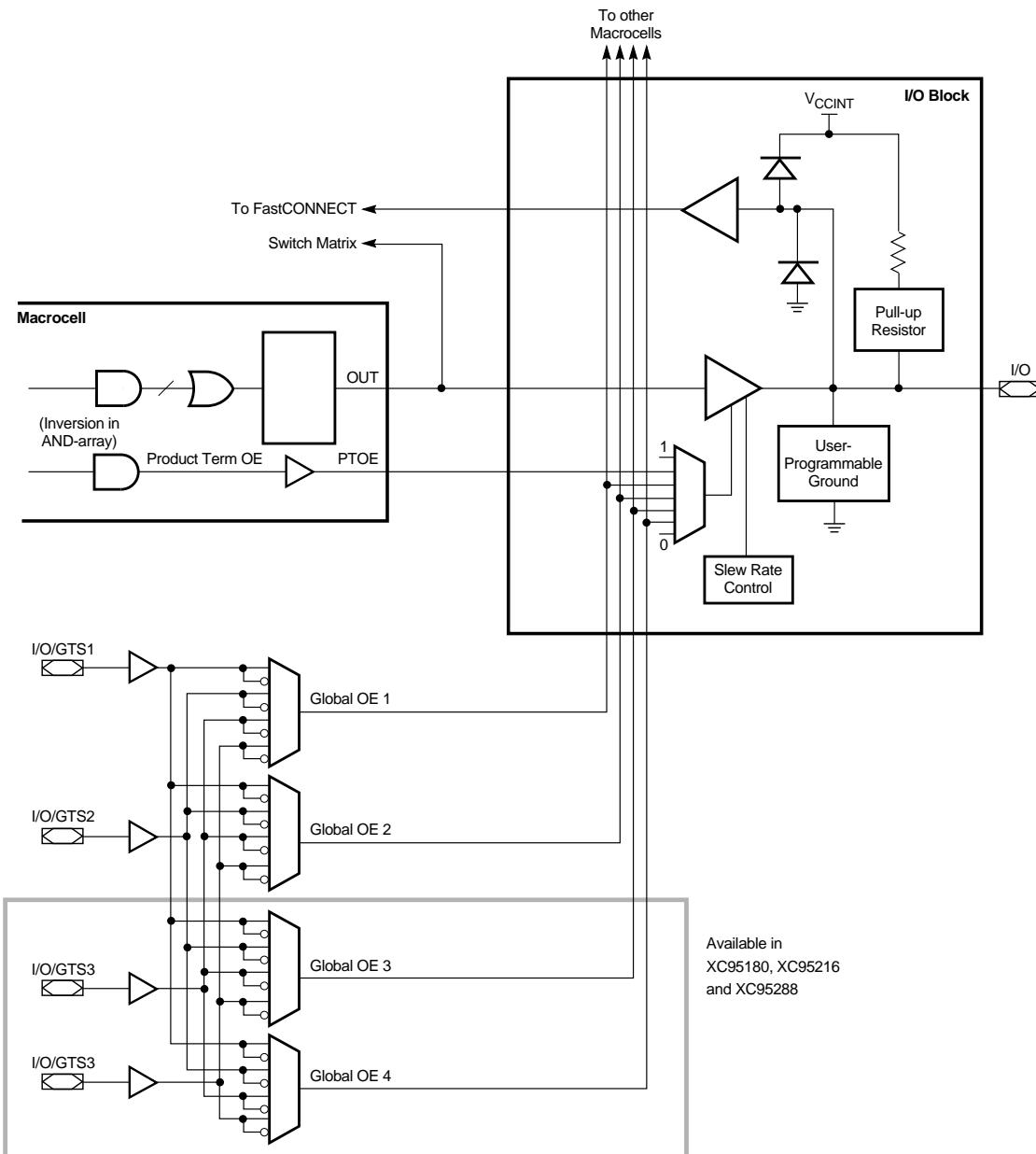
Figure 9: FastCONNECT Switch Matrix

## I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

The input buffer is compatible with standard 5 V CMOS, 5 V TTL and 3.3 V signal levels. The input buffer uses the internal 5 V voltage supply ( $V_{CCINT}$ ) to ensure that the input thresholds are constant and do not vary with the  $V_{CCIO}$  voltage.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global OE signals, always “1”, or always “0”. There are two global output enables for devices with up to 144 macrocells, and four global output enables for devices with 180 or more macrocells. Both polarities of any of the global 3-state control (GTS) pins may be used within the device.



**Figure 10: I/O Block and Output Enable Capability**

Each output has independent slew rate control. Output edge rates may be slowed down to reduce system noise (with an additional time delay of  $t_{SLEW}$ ) through programming. See Figure 11.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins. By tying strategically located programmable ground pins to the external ground connection, system noise generated from large numbers of simultaneous switching outputs may be reduced.

A control pull-up resistor (typically 10K ohms) is attached to each device I/O pin to prevent them from floating when the device is not in normal user operation. This resistor is active during device programming mode and system power-up. It is also activated for an erased device. The resistor is deactivated during normal operation.

The output driver is capable of supplying 24 mA output drive. All output drivers in the device may be configured for either 5 V TTL levels or 3.3 V levels by connecting the device output voltage supply ( $V_{CCIO}$ ) to a 5 V or 3.3 V

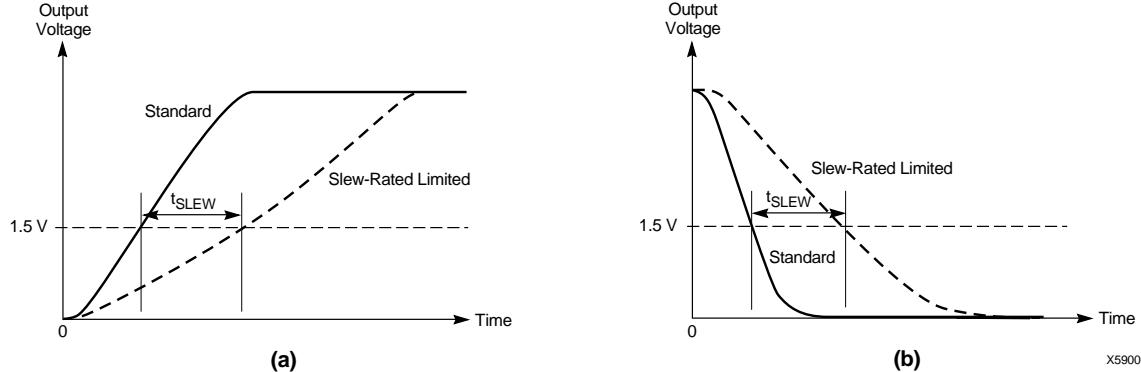
voltage supply. Figure 12 shows how the XC9500 device can be used in 5 V only and mixed 3.3 V/5 V systems.

## Pin-Locking Capability

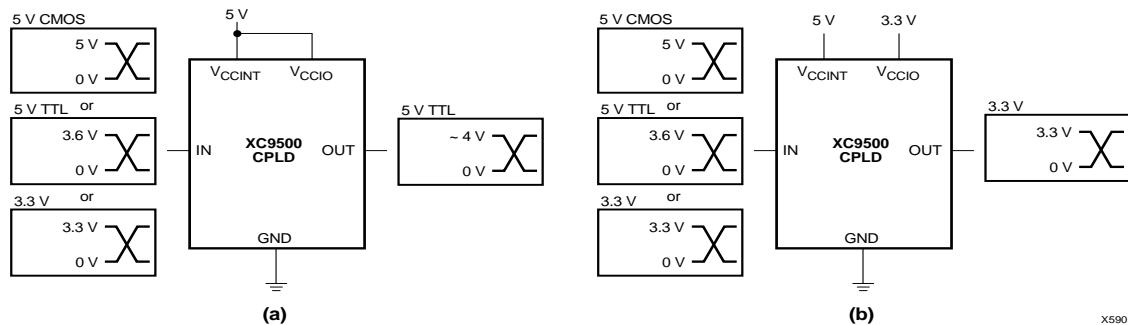
The capability to lock the user defined pin assignments during design changes depends on the ability of the architecture to adapt to unexpected changes. The XC9500 devices have architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500 architecture provides maximum routing within the FastCONNECT switch matrix, and incorporates a flexible Function Block that allows block-wide allocation of available product terms. This provides a high level of confidence of maintaining both input and output pin assignments for unexpected design changes.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.



**Figure 11: Output Slew-Rate Control For (a) Rising and (b) Falling Outputs**



**Figure 12: XC9500 Devices in (a) 5 V Systems and (b) Mixed 3.3 V/5 V Systems**

## In-System Programming

XC9500 devices are programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 13. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are 3-stated and pulled high by the IOB resistors during in-system programming. If a particular signal must remain low during this time, then a pulldown resistor may be added to the pin.

## External Programming

XC9500 devices can also be programmed by the Xilinx HW130 device programmer as well as third-party programmers. This provides the added flexibility of using pre-programmed devices during manufacturing, with an in-system programmable option for future enhancements.

## Endurance

All XC9500 CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles. Each device meets all functional, performance, and data retention specifications within this endurance limit.

## IEEE 1149.1 Boundary-Scan (JTAG)

XC9500 devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USER-CODE, INTEST, IDCODE, and HIGHZ instructions are supported in each device. For ISP operations, five additional instructions are added; the ISPEN, FERASE, FPGM, FVFY, and ISPEX instructions are fully compliant extensions of the 1149.1 instruction set.

The TMS and TCK pins have dedicated pull-up resistors as specified by the IEEE 1149.1 standard.

Boundary Scan Description Language (BSDL) files for the XC9500 are included in the development system and are available on the Xilinx FTP site.

## Design Security

XC9500 devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

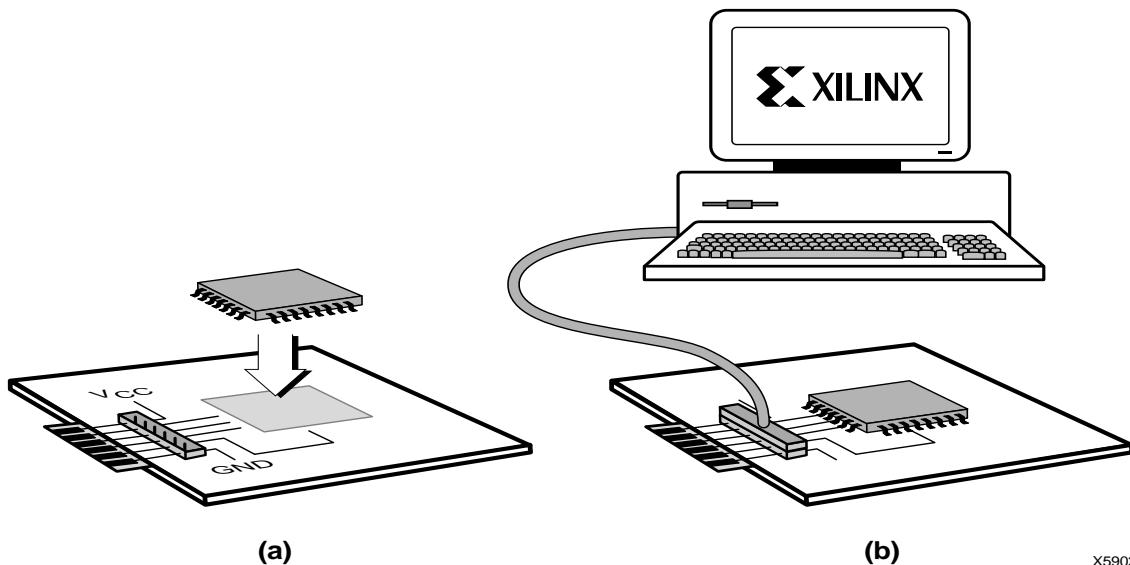
The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern.

**Table 3: Data Security Options**

		Read Security	
		Default	Set
Write Security	Default	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Allowed
	Set	Read Allowed Program/Erase Inhibited	Read Inhibited Program/Erase Inhibited

X5905



**Figure 13: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

## Low Power Mode

All XC9500 devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay ( $t_{LP}$ ) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

# Timing Model

The uniformity of the XC9500 architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 14, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The example in Figure 6 shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

Detailed timing information may be derived from the full timing model shown in Figure 15. The values and explanations for each parameter are given in the individual device data sheets.

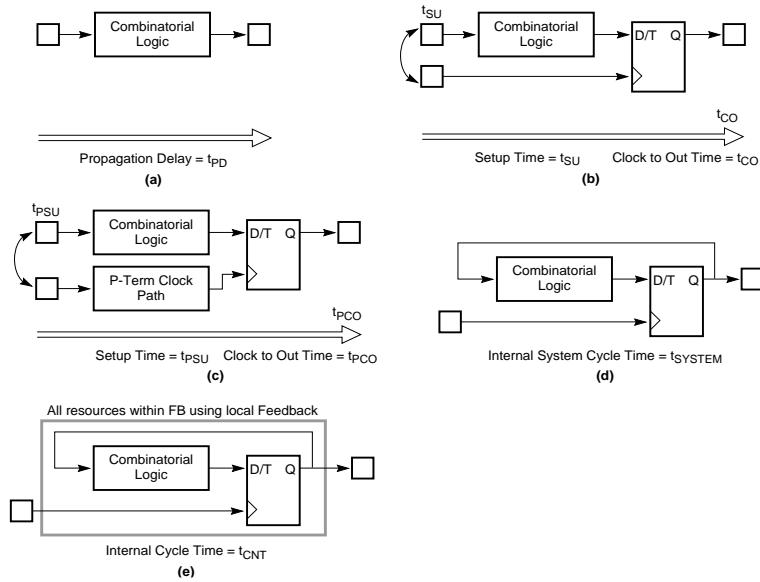


Figure 14: Basic Timing Model

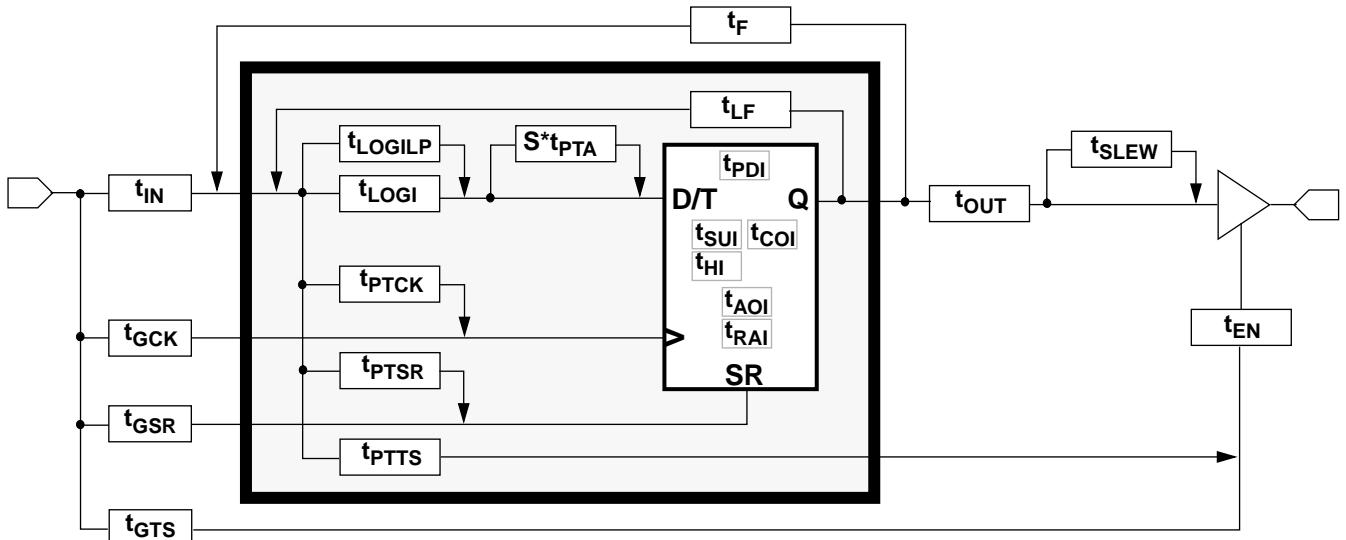


Figure 15: Detailed Timing Model

## Power-Up Characteristics

The XC9500 devices are well behaved under all operating conditions. During power-up each XC9500 device employs internal circuitry which keeps the device in the quiescent state until the  $V_{CCINT}$  supply voltage is at a safe level (approximately 3.8 V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the IOB pull-up resistors ( $\sim 10K$  ohms) enabled, as shown in Table 5. When the supply voltage reaches a safe

level, all user registers become initialized (typically within 100  $\mu$ s for 9536 - 95144, 200  $\mu$ s for 95216 and 300  $\mu$ s for 95288), and the device is immediately available for operation, as shown in Figure 16.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with the IOB pull-up resistors enabled. The JTAG pins are enabled to allow the device to be programmed at any time.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

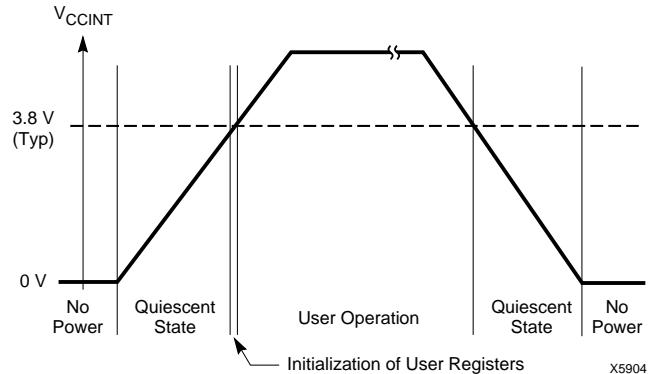
## Development System Support

The XC9500 CPLD family is fully supported by the development systems available from Xilinx and the Xilinx Alliance Program vendors.

The designer can create the design using ABEL, schematics, equations, VHDL, or Verilog in a variety of software front-end tools. The development system can be used to implement the design and generate a JEDEC bitmap which can be used to program the XC9500 device. Each development system includes JTAG download software that can be used to program the devices via the standard JTAG interface and a download cable.

## FastFLASH Technology

An advanced CMOS Flash process is used to fabricate all XC9500 devices. Specifically developed for Xilinx in-system programmable CPLDs, the FastFLASH process provides high performance logic capability, fast programming times, and endurance of 10,000 program/erase cycles.



**Figure 16: Device Behavior During Power-up**

**Table 4: Timing Model Parameters**

Description	Parameter	Product Term Allocator <sup>1</sup>	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	$t_{PD}$	$+ t_{PTA} * S$	$+ t_{LP}$	$+ t_{SLEW}$
Global Clock Setup Time	$t_{SU}$	$+ t_{PTA} * S$	$+ t_{LP}$	—
Global Clock-to-output	$t_{CO}$	—	—	$+ t_{SLEW}$
Product Term Clock Setup Time	$t_{PSU}$	$+ t_{PTA} * S$	$+ t_{LP}$	—
Product Term Clock-to-output	$t_{PCO}$	—	—	$+ t_{SLEW}$
Internal System Cycle Period	$t_{SYSTEM}$	$+ t_{PTA} * S$	$+ t_{LP}$	—

**Note:** 1. S = the logic span of the function, as defined in the text.

**Table 5: XC9500 Device Characteristics**

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Pull-up Resistors	Enabled	Enabled	Disabled
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled



June 3, 1998 (Version 3.0)

Product Specification

## Features

- 5 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 100 MHz
- 36 macrocells with 800 usable gates
- Up to 34 user I/O pins
- 5 V in-system programmable (ISP)
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-5, -6, -7, -10 speed grades)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC, 44-pin VQFP, and 48-pin CSP packages

## Description

The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of two 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC9536 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9536 device.

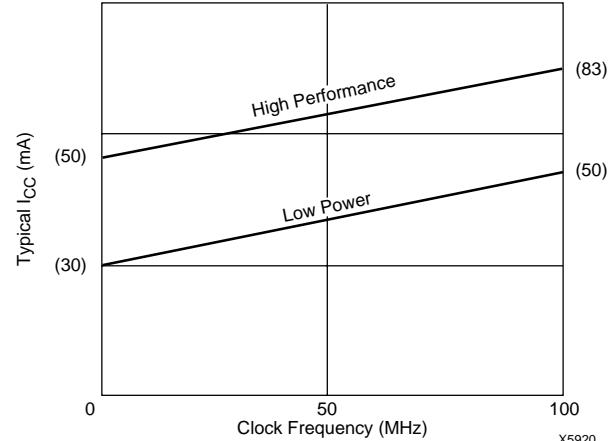
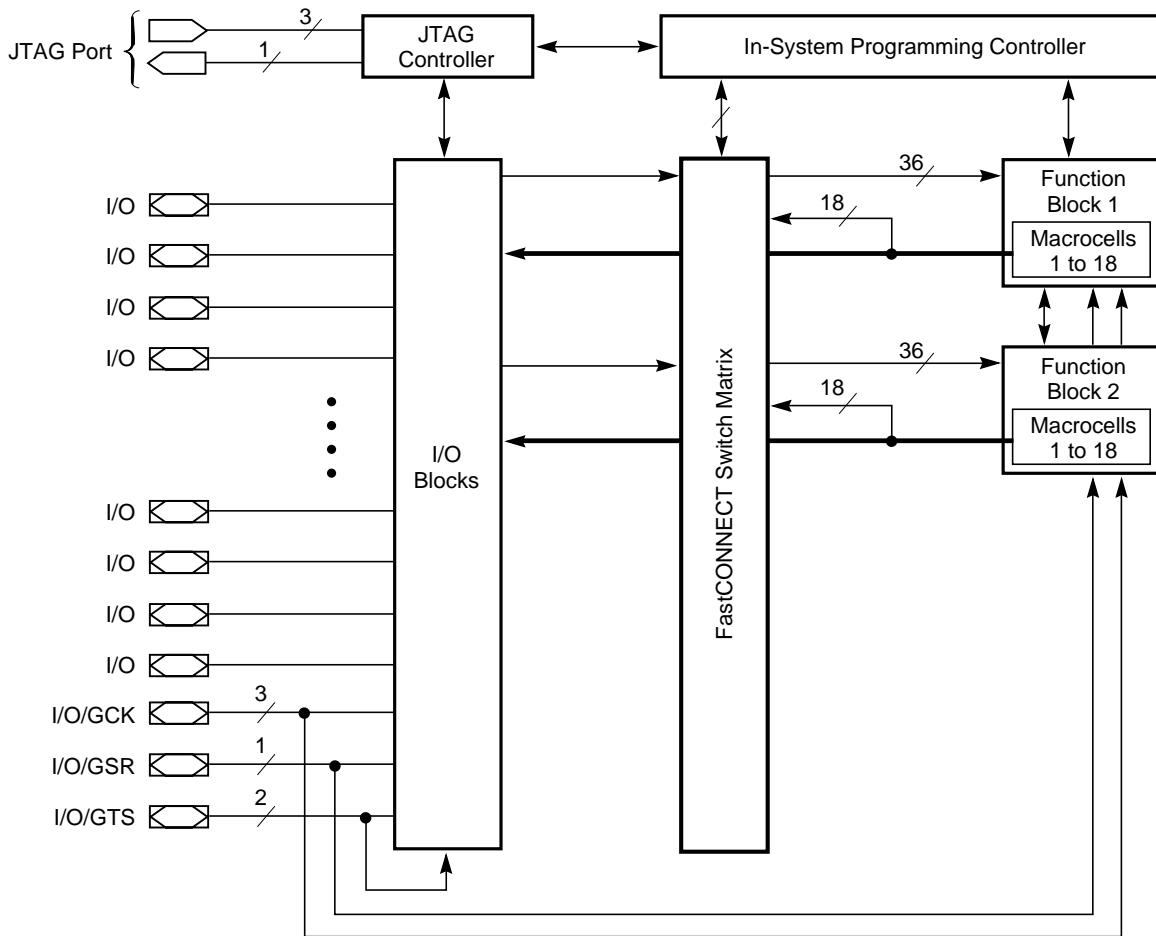


Figure 1: Typical  $I_{CC}$  vs. Frequency For XC9536



X5919

**Figure 2: XC9536 Architecture**

**Note:** Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

Note 1. Numbers in parenthesis are for industrial-temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	30 (Typ)		mA

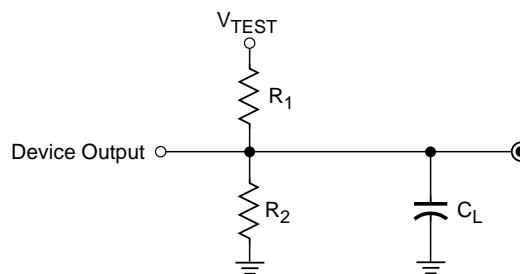
## AC Characteristics

Symbol	Parameter	XC9536-5		XC9536-6		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		5.0		6.0		7.5		10.0		15.0	ns
$t_{SU}$	I/O setup time before GCK	4.5		4.5		5.5		6.5		8.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		0.0		0.0		0.0		ns
$t_{CO}$	GCK to output valid		4.5		4.5		5.5		6.5		8.0	ns
$f_{CNT}^1$	16-bit counter frequency	100		100		83		67		56		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	100		100		83		67		56		MHz
$t_{PSU}$	I/O setup time before p-term clock input	0.5		0.5		1.5		2.5		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		4.0		4.0		4.0		4.0		ns
$t_{PCO}$	P-term clock to output valid		8.5		8.5		9.5		10.5		12.0	ns
$t_{OE}$	GTS to output valid		6.0		6.0		7.0		10.0		15.0	ns
$t_{OD}$	GTS to output disable		6.0		6.0		7.0		10.0		15.0	ns
$t_{POE}$	Product term OE to output enabled		10.5		10.5		13.0		15.5		18.0	ns
$t_{POD}$	Product term OE to output disabled		10.5		10.5		13.0		15.5		18.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		4.0		4.0		4.0		4.5		5.5	ns

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	$V_{CCIO}$	$V_{TEST}$	$R_1$	$R_2$	$C_L$
	5.0 V	5.0 V	160 $\Omega$	120 $\Omega$	35 pF
	3.3 V	3.3 V	260 $\Omega$	360 $\Omega$	35 pF

X5906

Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC9536-5		XC9536-6		XC9536-7		XC9536-10		XC9536-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>												
$t_{IN}$	Input buffer delay		1.5		1.5		2.5		3.5		4.5	ns
$t_{GCK}$	GCK buffer delay		2.0		2.0		2.5		3.0		3.0	ns
$t_{GSR}$	GSR buffer delay		4.0		4.0		4.5		6.0		7.5	ns
$t_{GTS}$	GTS buffer delay		6.0		6.0		7.0		10.0		15.0	ns
$t_{OUT}$	Output buffer delay		2.0		2.0		2.5		3.0		4.5	ns
$t_{EN}$	Output buffer enable/disable delay		0.0		0.0		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>												
$t_{PTCK}$	Product term clock delay		4.5		4.5		4.0		3.5		2.5	ns
$t_{PTSR}$	Product term set/reset delay		1.0		1.0		2.0		2.5		3.0	ns
$t_{PTTS}$	Product term 3-state delay		9.0		9.0		10.5		12.0		13.5	ns
<b>Internal Register and Combinatorial delays</b>												
$t_{PDI}$	Combinatorial logic propagation delay		0.5		1.5		0.5		1.0		3.0	ns
$t_{SUI}$	Register setup time	4.0		4.0		3.5		3.5		3.5		ns
$t_{HI}$	Register hold time	0.5		0.5		2.0		3.0		4.5		ns
$t_{COI}$	Register clock to output valid time		0.5		0.5		0.5		0.5		0.5	ns
$t_{AOI}$	Register async. S/R to output delay		6.0		6.0		6.5		7.0		8.0	ns
$t_{RAI}$	Register async. S/R recovery before clock	5.0		5.0		7.5		10.0		15.0		ns
$t_{LOGI}$	Internal logic delay		1.0		1.0		2.0		2.5		3.0	ns
$t_{LOGILP}$	Internal low power logic delay		9.0		9.0		10.0		11.0		11.5	ns
<b>Feedback Delays</b>												
$t_F$	FastCONNECT matrix feedback delay		4.5		4.5		6.0		8.5		11.0	ns
$t_{LF}$	Function Block local feedback delay		4.5		4.5		6.0		8.5		11.0	ns
<b>Time Adders</b>												
$t_{PTA}^3$	Incremental Product Term Allocator delay		1.0		1.0		1.0		1.0		1.5	ns
$t_{SLEW}$	Slew-rate limited delay		3.5		3.5		4.0		4.5		5.0	ns

**Note:** 3.  $t_{PTA}$  is multiplied by the span of the function as defined in the family data sheet.

**XC9536 I/O Pins**

Function Block	Macrocell	PC44	VQ44	CS48	BScan Order	Notes
1	1	2	40	D6	105	
1	2	3	41	C7	102	
1	3	5	43	B7	99	[1]
1	4	4	42	C6	96	
1	5	6	44	B6	93	[1]
1	6	8	2	A6	90	
1	7	7	1	A7	87	[1]
1	8	9	3	C5	84	
1	9	11	5	B5	81	
1	10	12	6	A4	78	
1	11	13	7	B4	75	
1	12	14	8	A3	72	
1	13	18	12	B2	69	
1	14	19	13	B1	66	
1	15	20	14	C2	63	
1	16	22	16	C3	60	
1	17	24	18	D2	57	
1	18	—	—	-	54	

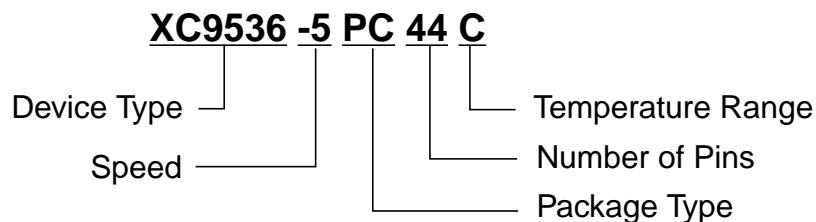
**Note:** [1] Global control pin

Function Block	Macrocell	PC44	VQ44	CS48	BScan Order	Notes
2	1	1	39	D7	51	
2	2	44	38	E5	48	
2	3	42	36	E6	45	[1]
2	4	43	37	E7	42	
2	5	40	34	F6	39	[1]
2	6	39	33	G7	36	[1]
2	7	38	32	G6	33	
2	8	37	31	F5	30	
2	9	36	30	G5	27	
2	10	35	29	F4	24	
2	11	34	28	G4	21	
2	12	33	27	E3	18	
2	13	29	23	F2	15	
2	14	28	22	G1	12	
2	15	27	21	F1	9	
2	16	26	20	E2	6	
2	17	25	19	E1	3	
2	18	-	-	-	0	

**Note:** [1] Global control pin**XC9536 Global, JTAG and Power Pins**

Pin Type	PC44	VQ44	CS48
I/O/GCK1	5	43	B7
I/O/GCK2	6	44	B6
I/O/GCK3	7	1	A7
I/O/GTS1	42	36	E6
I/O/GTS2	40	34	F6
I/O/GSR	39	33	G7
TCK	17	11	A1
TDI	15	9	B3
TDO	30	24	G2
TMS	16	10	A2
$V_{CCINT}$ 5 V	21,41	15,35	C1,F7
$V_{CCIO}$ 3.3 V/5 V	32	26	G3
GND	23,10,31	17,4,25	A5, D1, F3
No Connects	—	—	C4, D3, D4, E4

## Ordering Information



### Speed Options

-15	15 ns	pin-to-pin delay
-10	10 ns	pin-to-pin delay
-7	7.5 ns	pin-to-pin delay
-6	6 ns	pin-to-pin delay
-5	5 ns	pin-to-pin delay

### Packaging Options

PC44	44-Pin Plastic Leaded Chip Carrier (PLCC)
VQ44	44-Pin Thin Quad Pack (VQFP)
CS48	48-Pin Chip Scale Package (CSP)

### Temperature Options

C = Commercial (0°C to +70°C)  
 I = Industrial (-40°C to +85°C)

## Component Availability

Pins		44		48
Type		Plastic PLCC	Plastic VQFP	Plastic CSP
Code		PC44	VQ44	CS48
XC9536	-15	C,I	C,I	
	-10	C,I	C,I	C
	-7	C,I	C,I	C
	-6	C	C	
	-5	C <sup>1</sup>	C	

C = Commercial (0°C to +70°C), I = Industrial (-40°C to +85°C)

Note 1: Contact factory for availability.

### Revision Control

Date	Reason
6/3/98	Revise datasheet to reflect new CSP package pinouts & ordering code.



October 28, 1997 (Version 2.0)

Product Specification

## Features

- 7.5 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable (ISP)
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC, 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages

## Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

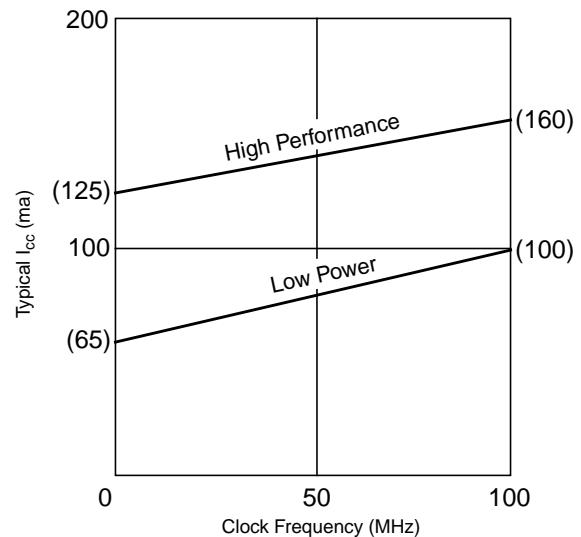
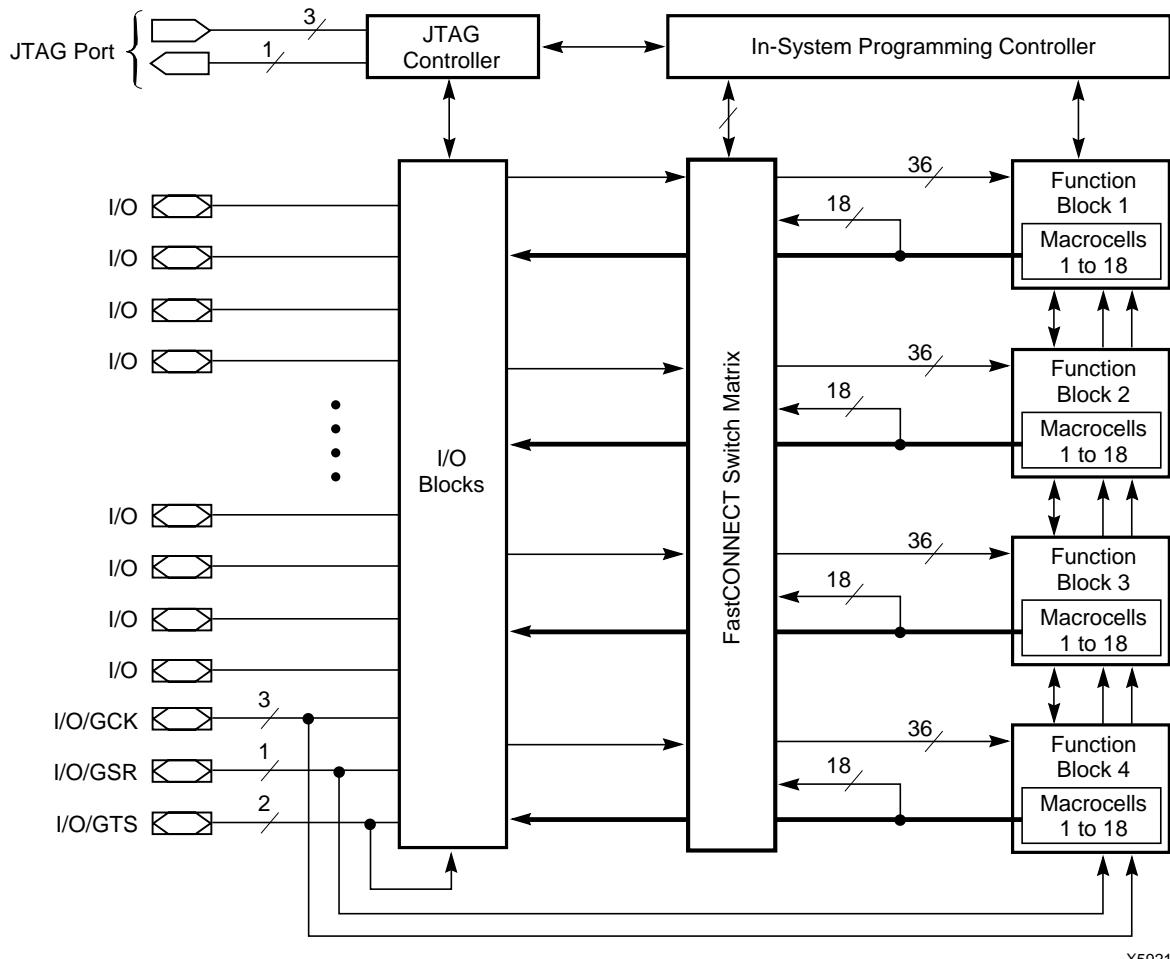


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC9572



X5921

**Figure 2: XC9572 Architecture**

**Note:** Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

**Note:** 1. Numbers in parenthesis are for industrial temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	65 (Typ)		ma

## AC Characteristics

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		7.5		10.0		15.0	ns
$t_{SU}$	I/O setup time before GCK	5.5		6.5		8.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		0.0		ns
$t_{CO}$	GCK to output valid		5.5		6.5		8.0	ns
$f_{CNT}^1$	16-bit counter frequency	125		111		95		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	83		67		56		MHz
$t_{PSU}$	I/O setup time before p-term clock input	1.5		2.5		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		4.0		4.0		ns
$t_{PCO}$	P-term clock to output valid		9.5		10.5		12.0	ns
$t_{OE}$	GTS to output valid		7.0		10.0		15.0	ns
$t_{OD}$	GTS to output disable		7.0		10.0		15.0	ns
$t_{POE}$	Product term OE to output enabled		13.0		15.5		18.0	ns
$t_{POD}$	Product term OE to output disabled		13.0		15.5		18.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		4.0		4.5		5.5	ns

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available, using the local feedback when applicable.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.

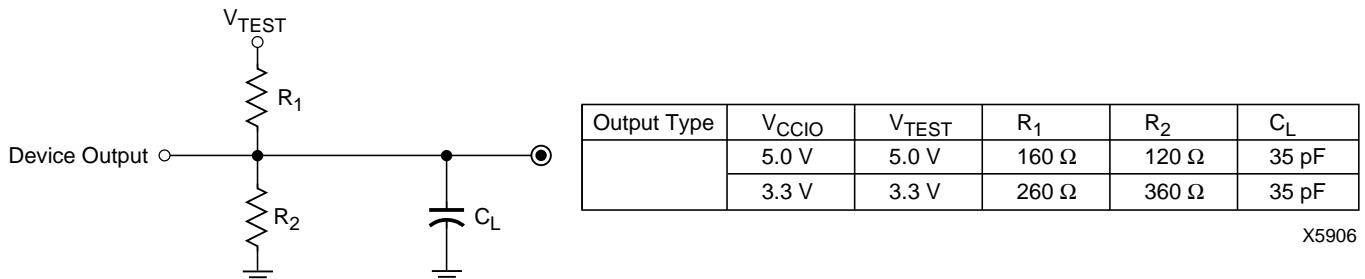


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>								
$t_{IN}$	Input buffer delay			2.5		3.5		4.5 ns
$t_{GCK}$	GCK buffer delay			2.5		3.0		3.0 ns
$t_{GSR}$	GSR buffer delay			4.5		6.0		7.5 ns
$t_{GTS}$	GTS buffer delay			7.0		10.0		15.0 ns
$t_{OUT}$	Output buffer delay			2.5		3.0		4.5 ns
$t_{EN}$	Output buffer enable/disable delay			0.0		0.0		0.0 ns
<b>Product Term Control Delays</b>								
$t_{PTCK}$	Product term clock delay			4.0		3.5		2.5 ns
$t_{PTSR}$	Product term set/reset delay			2.0		2.5		3.0 ns
$t_{PTTS}$	Product term 3-state delay			10.5		12.0		13.5 ns
<b>Internal Register and Combinatorial delays</b>								
$t_{PDI}$	Combinatorial logic propagation delay			0.5		1.0		3.0 ns
$t_{SUI}$	Register setup time		3.5		3.5		3.5	
$t_{HI}$	Register hold time		2.0		3.0		4.5	
$t_{COI}$	Register clock to output valid time			0.5		0.5		0.5 ns
$t_{AOI}$	Register async. S/R to output delay			6.5		7.0		8.0 ns
$t_{RAI}$	Register async. S/R recovery before clock	7.5		10.0		15.0		
$t_{LOGI}$	Internal logic delay			2.0		2.5		3.0 ns
$t_{LOGILP}$	Internal low power logic delay			10.0		11.0		11.5 ns
<b>Feedback Delays</b>								
$t_F$	FastCONNECT matrix feedback delay			6.0		8.5		11.0 ns
$t_{LF}$	Function Block local feedback delay			2.0		2.5		3.5 ns
<b>Time Adders</b>								
$t_{PTA}^3$	Incremental Product Term Allocator delay			1.0		1.0		1.5 ns
$t_{SLEW}$	Slew-rate limited delay			4.0		4.5		5.0 ns

**Note:** 3.  $t_{PTA}$  is multiplied by the span of the function as defined in the family data sheet.

**XC9572 I/O Pins**

Function Block	Macrocell	PC 44	PC 84	PQ 100	TQ 100	BScan Order	Notes
1	1	—	4	18	16	213	
1	2	1	1	15	13	210	
1	3	—	6	20	18	207	
1	4	—	7	22	20	204	
1	5	2	2	16	14	201	
1	6	3	3	17	15	198	
1	7	—	11	27	25	195	
1	8	4	5	19	17	192	
1	9	5	9	24	22	189	[1]
1	10	—	13	30	28	186	
1	11	6	10	25	23	183	[1]
1	12	—	18	35	33	180	
1	13	—	20	38	36	177	
1	14	7	12	29	27	174	[1]
1	15	8	14	31	29	171	
1	16	—	23	41	39	168	
1	17	9	15	32	30	165	
1	18	—	24	42	40	162	
2	1	—	63	89	87	159	
2	2	35	69	96	94	156	
2	3	—	67	93	91	153	
2	4	—	68	95	93	150	
2	5	36	70	97	95	147	
2	6	37	71	98	96	144	
2	7	—	76	5	3	141	[2]
2	8	38	72	99	97	138	
2	9	39	74	1	99	135	[1]
2	10	—	75	3	1	132	
2	11	40	77	6	4	129	[1]
2	12	—	79	8	6	126	
2	13	—	80	10	8	123	
2	14	42	81	11	9	120	[3]
2	15	43	83	13	11	117	
2	16	—	82	12	10	114	
2	17	44	84	14	12	111	
2	18	—	—	94	92	108	

**Notes:** [1] Global control pin

[2] Global control pin GTS1 for PC84, PQ100, and TQ100

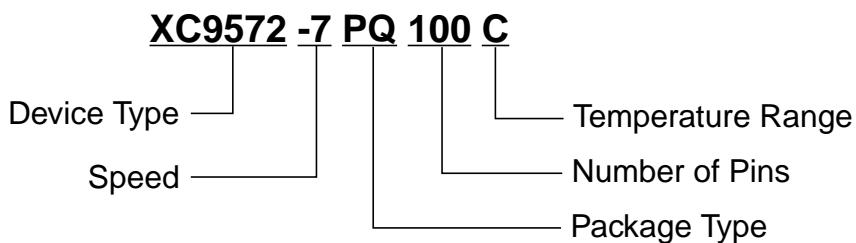
[3] Global control pin GTS1 for PC44

Function Block	Macrocell	PC 44	PC 84	PQ 100	TQ 100	BScan Order	Notes
3	1	—	25	43	41	105	
3	2	11	17	34	32	102	
3	3	—	31	51	49	99	
3	4	—	32	52	50	96	
3	5	12	19	37	35	93	
3	6	—	34	55	53	90	
3	7	—	35	56	54	87	
3	8	13	21	39	37	84	
3	9	14	26	44	42	81	
3	10	—	40	62	60	78	
3	11	18	33	54	52	75	
3	12	—	41	63	61	72	
3	13	—	43	65	63	69	
3	14	19	36	57	55	66	
3	15	20	37	58	56	63	
3	16	—	45	67	65	60	
3	17	22	39	60	58	57	
3	18	—	—	61	59	54	
4	1	—	46	68	66	51	
4	2	24	44	66	64	48	
4	3	—	51	73	71	45	
4	4	—	52	74	72	42	
4	5	25	47	69	67	39	
4	6	—	54	78	76	36	
4	7	—	55	79	77	33	
4	8	26	48	70	68	30	
4	9	27	50	72	70	27	
4	10	—	57	83	81	24	
4	11	28	53	76	74	21	
4	12	—	58	84	82	18	
4	13	—	61	87	85	15	
4	14	29	56	80	78	12	
4	15	33	65	91	89	9	
4	16	—	62	88	86	6	
4	17	34	66	92	90	3	
4	18	—	—	81	79	0	

## XC9572 Global, JTAG and Power Pins

Pin Type	PC44	PC84	PQ100	TQ100
I/O/GCK1	5	9	24	22
I/O/GCK2	6	10	25	23
I/O/GCK3	7	12	29	27
I/O/GTS1	42	76	5	3
I/O/GTS2	40	77	6	4
I/O/GSR	39	74	1	99
TCK	17	30	50	48
TDI	15	28	47	45
TDO	30	59	85	83
TMS	16	29	49	47
V <sub>CCINT</sub> 5 V	21,41	38,73,78	7,59,100	5,57,98
V <sub>CCIO</sub> 3.3 V/5 V	32	22,64	28,40,53,90	26,38,51,88
GND	10,23,31	8,16,27,42, 49,60	2,23,33,46,64,71, 77,86	100,21,31,44,62,69, 75, 84
No Connects	—	—	4,9,21,26,36,45,48, 75, 82	2,7,19,24,34,43,46, 73, 80

## Ordering Information



### Speed Options

- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay
- 7 7.5 ns pin-to-pin delay

### Packaging Options

- PC44 44-Pin Plastic Leaded Chip Carrier (PLCC)
- PC84 84-Pin Plastic Leaded Chip Carrier (PLCC)
- PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
- TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)

### Temperature Options

- |   |            |               |
|---|------------|---------------|
| C | Commercial | 0°C to 70°C   |
| I | Industrial | -40°C to 85°C |

## Component Availability

Pins		44	84	100	
Type		Plastic PLCC	Plastic PLCC	Plastic PQFP	Plastic TQFP
Code		PC44	PC84	PQ100	TQ100
XC9572	-15	C,I	C,I	C,I	C,I
	-10	C,I	C,I	C,I	C,I
	-7	C	C	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C

October 28, 1997 (Version 2.0)

Product Specification

## Features

- 7.5 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 125 MHz
- 108 macrocells with 2400 usable gates
- Up to 108 user I/O pins
- 5 V in-system programmable (ISP)
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-7, -10 speed grades)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 84-pin PLCC, 100-pin PQFP, 100-pin TQFP and 160-pin PQFP packages

## Description

The XC95108 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of six 36V18 Function Blocks, providing 2,400 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC95108 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95108 device.

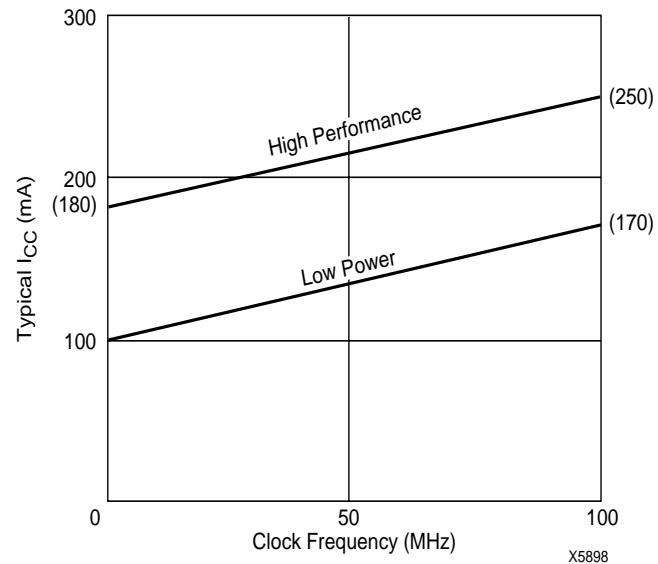
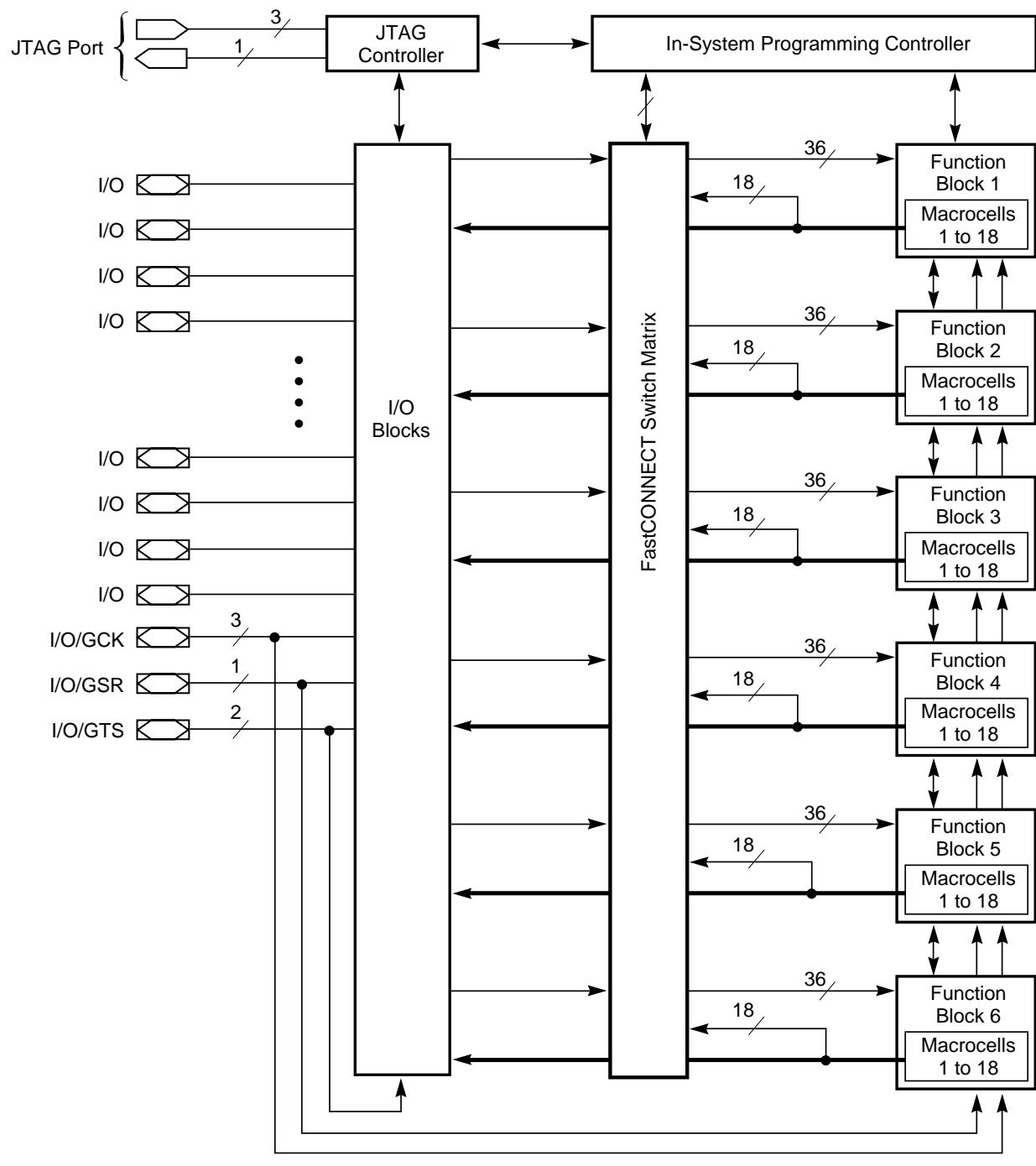


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC95108



X5897

**Figure 2: XC95108 Architecture**

**Note:** Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

**Note:** 1. Numbers in parenthesis are for industrial-temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	100 (Typ)		ma

## AC Characteristics

Symbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		7.5		10.0		15.0		20.0	ns
$t_{SU}$	I/O setup time before GCK	5.5		6.5		8.0		10.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		0.0		0.0		ns
$t_{CO}$	GCK to output valid		5.5		6.5		8.0		10.0	ns
$f_{CNT}^1$	16-bit counter frequency	125		111		95		83		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	83		67		56		50		MHz
$t_{PSU}$	I/O setup time before p-term clock input	1.5		2.5		4.0		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		4.0		4.0		6.0		ns
$t_{PCO}$	P-term clock to output valid		9.5		10.5		12.0		16.0	ns
$t_{OE}$	GTS to output valid		7.0		10.0		15.0		20.0	ns
$t_{OD}$	GTS to output disable		7.0		10.0		15.0		20.0	ns
$t_{POE}$	Product term OE to output enabled		13.0		15.5		18.0		22.0	ns
$t_{POD}$	Product term OE to output disabled		13.0		15.5		18.0		22.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		4.0		4.5		5.5		5.5	ns

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available, using the local feedback when applicable.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.

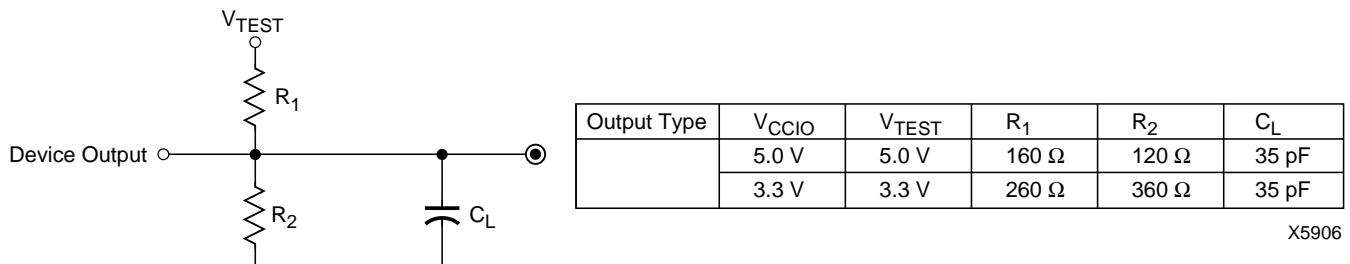


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95108-7		XC95108-10		XC95108-15		XC95108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>										
$t_{IN}$	Input buffer delay			2.5		3.5		4.5		6.5 ns
$t_{GCK}$	GCK buffer delay			2.5		3.0		3.0		3.0 ns
$t_{GSR}$	GSR buffer delay			4.5		6.0		7.5		9.5 ns
$t_{GTS}$	GTS buffer delay			7.0		10.0		15.0		20.0 ns
$t_{OUT}$	Output buffer delay			2.5		3.0		4.5		6.5 ns
$t_{EN}$	Output buffer enable/disable delay			0.0		0.0		0.0		0.0 ns
<b>Product Term Control Delays</b>										
$t_{PTCK}$	Product term clock delay			4.0		3.5		2.5		2.5 ns
$t_{PTSR}$	Product term set/reset delay			2.0		2.5		3.0		3.0 ns
$t_{PTTS}$	Product term 3-state delay			10.5		12.0		13.5		15.5 ns
<b>Internal Register and Combinatorial delays</b>										
$t_{PDI}$	Combinatorial logic propagation delay			0.5		1.0		3.0		4.0 ns
$t_{SUI}$	Register setup time			3.5		3.5		3.5		3.5 ns
$t_{HI}$	Register hold time			2.0		3.0		4.5		6.5 ns
$t_{COI}$	Register clock to output valid time			0.5		0.5		0.5		0.5 ns
$t_{AOI}$	Register async. S/R to output delay			6.5		7.0		8.0		9.0 ns
$t_{RAI}$	Register async. S/R recovery before clock	7.5		10.0		15.0		20.0		ns
$t_{LOGI}$	Internal logic delay			2.0		2.5		3.0		3.0 ns
$t_{LOGILP}$	Internal low power logic delay			10.0		11.0		11.5		11.5 ns
<b>Feedback Delays</b>										
$t_F$	FastCONNECT matrix feedback delay			6.0		8.5		11.0		13.0 ns
$t_{LF}$	Function Block local feedback delay			2.0		2.5		3.5		5.0 ns
<b>Time Adders</b>										
$t_{PTA}^3$	Incremental Product Term Allocator delay			1.0		1.0		1.5		1.5 ns
$t_{SLEW}$	Slew-rate limited delay			4.0		4.5		5.0		5.5 ns

**Note:** 3.  $t_{PTA}$  is multiplied by the span of the function as defined in the family data sheet.

**XC95108 I/O Pins**

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
1	1	—	—	—	25	321		3	1	—	—	—	45	213	
1	2	1	15	13	21	318		3	2	14	31	29	47	210	
1	3	2	16	14	22	315		3	3	15	32	30	49	207	
1	4	—	21	19	29	312		3	4	—	36	34	57	204	
1	5	3	17	15	23	309		3	5	17	34	32	54	201	
1	6	4	18	16	24	306		3	6	18	35	33	56	198	
1	7	—	—	—	27	303		3	7	—	—	—	50	195	
1	8	5	19	17	26	300		3	8	19	37	35	58	192	
1	9	6	20	18	28	297		3	9	20	38	36	59	189	
1	10	—	26	24	36	294		3	10	—	45	43	69	186	
1	11	7	22	20	30	291		3	11	21	39	37	60	183	
1	12	9	24	22	33	288	[1]	3	12	23	41	39	62	180	
1	13	—	—	—	34	285		3	13	—	—	—	52	177	
1	14	10	25	23	35	282	[1]	3	14	24	42	40	63	174	
1	15	11	27	25	37	279		3	15	25	43	41	64	171	
1	16	12	29	27	42	276	[1]	3	16	26	44	42	68	168	
1	17	13	30	28	44	273		3	17	31	51	49	77	165	
1	18	—	—	—	43	270		3	18	—	—	—	74	162	
2	1	—	—	—	158	267		4	1	—	—	—	123	159	
2	2	71	98	96	154	264		4	2	57	83	81	134	156	
2	3	72	99	97	156	261		4	3	58	84	82	135	153	
2	4	—	4	2	4	258		4	4	—	82	80	133	150	
2	5	74	1	99	159	255	[1]	4	5	61	87	85	138	147	
2	6	75	3	1	2	252		4	6	62	88	86	139	144	
2	7	—	—	—	9	249		4	7	—	—	—	128	141	
2	8	76	5	3	6	246	[1]	4	8	63	89	87	140	138	
2	9	77	6	4	8	243	[1]	4	9	65	91	89	142	135	
2	10	—	9	7	12	240		4	10	—	—	—	147	132	
2	11	79	8	6	11	237		4	11	66	92	90	143	129	
2	12	80	10	8	13	234		4	12	67	93	91	144	126	
2	13	—	—	—	14	231		4	13	—	—	—	153	123	
2	14	81	11	9	15	228		4	14	68	95	93	146	120	
2	15	82	12	10	17	225		4	15	69	96	94	148	117	
2	16	83	13	11	18	222		4	16	—	94	92	145	114	
2	17	84	14	12	19	219		4	17	70	97	95	152	111	
2	18	—	—	—	16	216		4	18	—	—	—	155	108	

**Notes:** [1] Global control pin

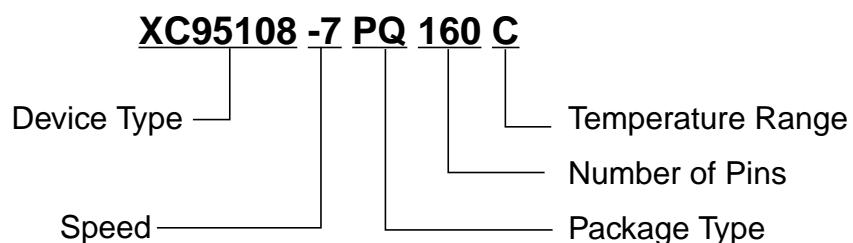
## XC95108 I/O Pins (continued)

Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes	Function Block	Macrocell	PC84	PQ100	TQ100	PQ160	BScan Order	Notes
5	1	—	—	—	76	105		6	1	—	—	—	91	51	
5	2	32	52	50	79	102		6	2	45	67	65	103	48	
5	3	33	54	52	82	99		6	3	46	68	66	104	45	
5	4	—	48	46	72	96		6	4	—	75	73	116	42	
5	5	34	55	53	86	93		6	5	47	69	67	106	39	
5	6	35	56	54	88	90		6	6	48	70	68	108	36	
5	7	—	—	—	78	87		6	7	—	—	—	105	33	
5	8	36	57	55	90	84		6	8	50	72	70	111	30	
5	9	37	58	56	92	81		6	9	51	73	71	113	27	
5	10	—	—	—	84	78		6	10	—	—	—	107	24	
5	11	39	60	58	95	75		6	11	52	74	72	115	21	
5	12	40	62	60	97	72		6	12	53	76	74	117	18	
5	13	—	—	—	87	69		6	13	—	—	—	112	15	
5	14	41	63	61	98	66		6	14	54	78	76	122	12	
5	15	43	65	63	101	63		6	15	55	79	77	124	9	
5	16	—	61	59	96	60		6	16	—	81	79	129	6	
5	17	44	66	64	102	57		6	17	56	80	78	126	3	
5	18	—	—	—	89	54		6	18	—	—	—	114	0	

## XC95108 Global, JTAG and Power Pins

Pin Type	PC84	PQ100	TQ100	PQ160
I/O/GCK1	9	24	22	33
I/O/GCK2	10	25	23	35
I/O/GCK3	12	29	27	42
I/O/GTS1	76	5	3	6
I/O/GTS2	77	6	4	8
I/O/GSR	74	1	99	159
TCK	30	50	48	75
TDI	28	47	45	71
TDO	59	85	83	136
TMS	29	49	47	73
V <sub>CCINT</sub> 5 V	38,73,78	7,59,100	5,57,98	10,46,94,157
V <sub>CCIO</sub> 3.3 V/5 V	22,64	28,40,53,90	26,38,51,88	1,41,61,81,121,141
GND	8,16,27,42,49,60	2,23,33,46,64,71,77,86	100,21,31,44,62,69,75,84	20,31,40,51,70,80,99
GND	—	—	—	100,110,120,127,137
GND	—	—	—	160
No connects	—	—	—	3,5,7,32,38,39,48,53,55,6 5,66,67,83,85,93,109, 118,119,125,130,131, 132,149,150,151

## Ordering Information



### Speed Options

- 20 20 ns pin-to-pin delay
- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay
- 7 7 ns pin-to-pin delay

### Packaging Options

- PC84 84-Pin Plastic Leaded Chip Carrier (PLCC)
- PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
- TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)
- PQ160 160-Pin Plastic Quad Flat Pack (PQFP)

### Temperature Options

- |   |            |               |
|---|------------|---------------|
| C | Commercial | 0°C to 70°C   |
| I | Industrial | -40°C to 85°C |

## Component Availability

Pins		84	100		160
Type		Plastic PLCC	Plastic PQFP	Plastic TQFP	Plastic PQFP
Code		PC84	PQ100	TQ100	PQ160
XC95108	-20	C,I	C,I	C,I	C,I
	-15	C,I	C,I	C,I	C,I
	-10	C,I	C,I	C,I	C,I
	-7	C	C	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C

November 21, 1997 (Version 3.0)

Preliminary Product Specification

## Features

- 7.5 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 111 MHz
- 144 macrocells with 3,200 usable gates
- Up to 133 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 100-pin PQFP, 100-pin TQFP, and 160-pin PQFP packages

## Description

The XC95144 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of eight 36V18 Function Blocks, providing 3,200 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC95144 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95144 device.

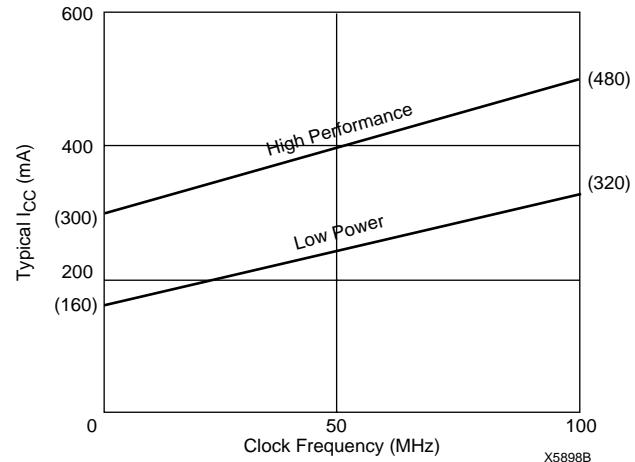
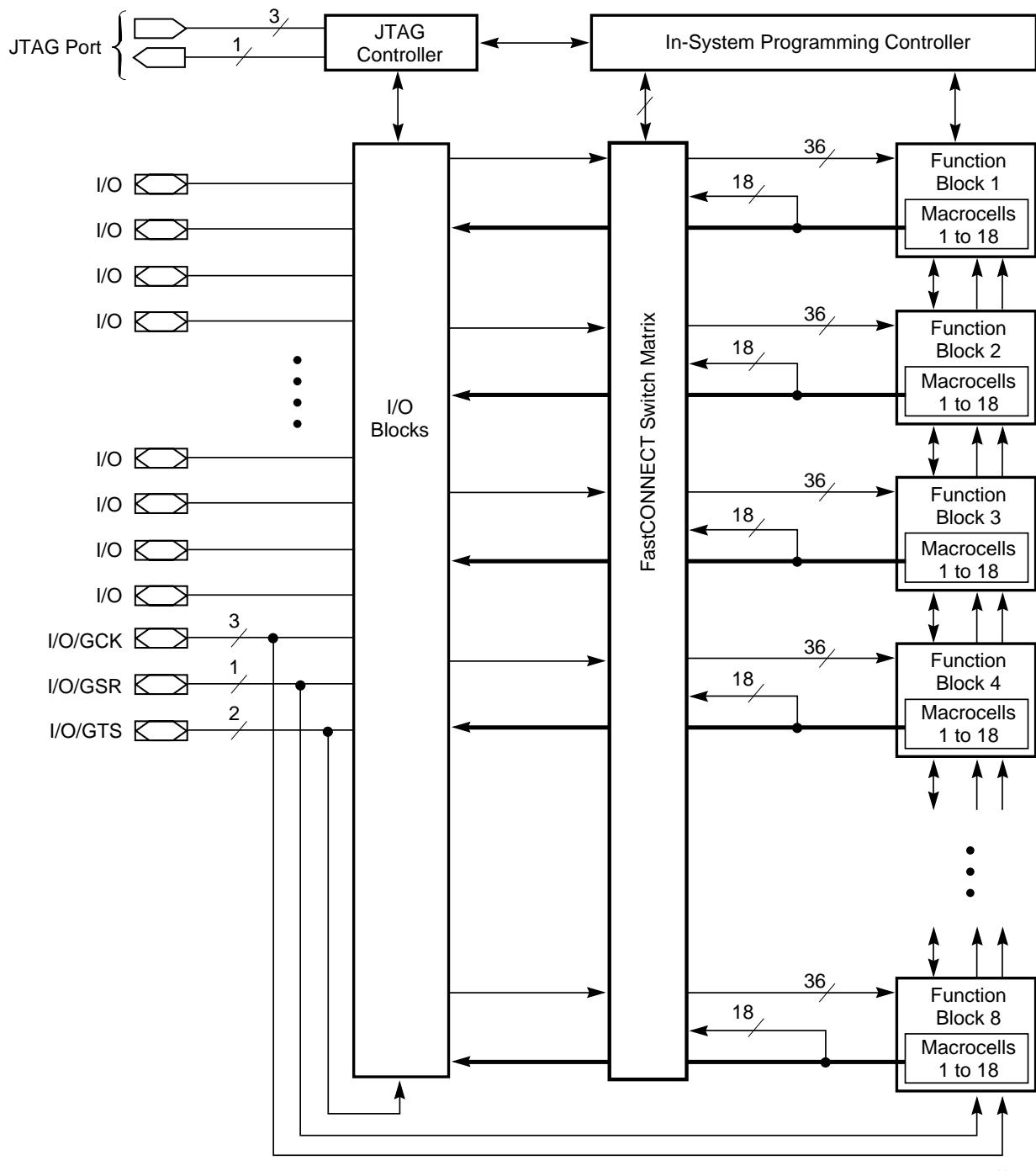


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC95144

**Figure 2: XC95144 Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

**Note:** 1. Numbers in parenthesis are for industrial-temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	160 (Typ)		ma

## AC Characteristics

Symbol	Parameter	XC95144-7		XC95144-10		XC95144-15		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		7.5		10.0		15.0	ns
$t_{SU}$	I/O setup time before GCK	5.5		6.5		8.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		0.0		ns
$t_{CO}$	GCK to output valid		5.5		6.5		8.0	ns
$f_{CNT}^1$	16-bit counter frequency	125		111		95		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	83		67		56		MHz
$t_{PSU}$	I/O setup time before p-term clock input	1.5		2.5		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		4.0		4.0		ns
$t_{PCO}$	P-term clock to output valid		9.5		10.5		12.0	ns
$t_{OE}$	GTS to output valid		7.0		10.0		15.0	ns
$t_{OD}$	GTS to output disable		7.0		10.0		15.0	ns
$t_{POE}$	Product term OE to output enabled		13.0		15.5		18.0	ns
$t_{POD}$	Product term OE to output disabled		13.0		15.5		18.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		4.0		4.5		5.5	ns
Preliminary								

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available, using the local feedback when applicable.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.

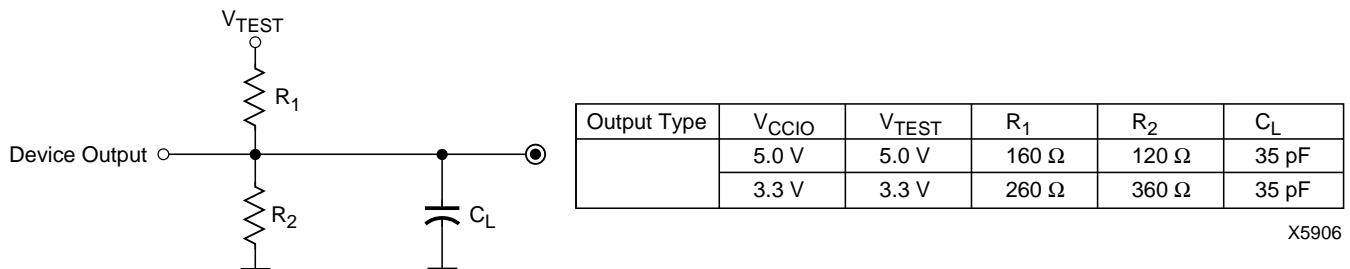


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95144-7		XC95144-10		XC95144-15		Units
		Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>								
$t_{IN}$	Input buffer delay		2.5		3.5		4.5	ns
$t_{GCK}$	GCK buffer delay		2.5		3.0		3.0	ns
$t_{GSR}$	GSR buffer delay		4.5		6.0		7.5	ns
$t_{GTS}$	GTS buffer delay		7.0		10.0		15.0	ns
$t_{OUT}$	Output buffer delay		2.5		3.0		4.5	ns
$t_{EN}$	Output buffer enable/disable delay		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>								
$t_{PTCK}$	Product term clock delay		4.0		3.5		2.5	ns
$t_{PTSR}$	Product term set/reset delay		2.0		2.5		3.0	ns
$t_{PTTS}$	Product term 3-state delay		10.5		12.0		13.5	ns
<b>Internal Register and Combinatorial delays</b>								
$t_{PDI}$	Combinatorial logic propagation delay		0.5		1.0		3.0	ns
$t_{SUI}$	Register setup time	3.5		3.5		3.5		ns
$t_{HI}$	Register hold time	2.0		3.0		4.5		ns
$t_{COI}$	Register clock to output valid time		0.5		0.5		0.5	ns
$t_{AOI}$	Register async. S/R to output delay		6.5		7.0		8.0	ns
$t_{RAI}$	Register async. S/R recovery before clock	7.5		10.0		15.0		ns
$t_{LOGI}$	Internal logic delay		2.0		2.5		3.0	ns
$t_{LOGILP}$	Internal low power logic delay		10.0		11.0		11.5	ns
<b>Feedback Delays</b>								
$t_F$	FastCONNECT matrix feedback delay		6.0		8.5		11.0	ns
$t_{LF}$	Function Block local feedback delay		2.0		2.5		3.5	ns
<b>Time Adders</b>								
$t_{PTA}^3$	Incremental Product Term Allocator delay		1.0		1.0		1.5	ns
$t_{SLEW}$	Slew-rate limited delay		4.0		4.5		5.0	ns
Preliminary								

**Note:** 3.  $t_{PTA}$  is multiplied by the span of the function as defined in the family data sheet.

## XC95144 I/O Pins

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
1	1	—	—	25	429	
1	2	11	13	18	426	
1	3	12	14	19	423	
1	4	—	—	27	420	
1	5	13	15	21	417	
1	6	14	16	22	414	
1	7	—	—	32	411	
1	8	15	17	23	408	
1	9	16	18	24	405	
1	10	—	—	34	402	
1	11	17	19	26	399	
1	12	18	20	28	396	
1	13	—	—	38	393	
1	14	19	21	29	390	
1	15	20	22	30	387	
1	16	—	—	39	384	
1	17	22	24	33	381	[1]
1	18	—	—	—	378	
2	1	—	—	158	375	
2	2	99	1	159	372	[1]
2	3	—	—	3	369	
2	4	—	—	5	366	
2	5	1	3	2	363	[1]
2	6	2	4	4	360	[1]
2	7	—	—	7	357	
2	8	3	5	6	354	[1]
2	9	4	6	8	351	[1]
2	10	—	—	9	348	
2	11	6	8	11	345	
2	12	7	9	12	342	
2	13	—	—	14	339	
2	14	8	10	13	336	
2	15	9	11	15	333	
2	16	—	—	16	330	
2	17	10	12	17	327	
2	18	—	—	—	324	

**Notes:** [1] Global control pin.

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
3	1	—	—	43	321	
3	2	23	25	35	318	[1]
3	3	—	—	45	315	
3	4	—	—	48	312	
3	5	24	26	36	309	
3	6	25	27	37	306	
3	7	—	—	50	303	
3	8	27	29	42	300	[1]
3	9	28	30	44	297	
3	10	—	—	52	294	
3	11	29	31	47	291	
3	12	30	32	49	288	
3	13	—	—	53	285	
3	14	32	34	54	282	
3	15	33	35	56	279	
3	16	—	—	55	276	
3	17	34	36	57	273	
3	18	—	—	—	270	
4	1	—	—	132	267	
4	2	87	89	140	264	
4	3	—	—	147	261	
4	4	—	—	149	258	
4	5	89	91	142	255	
4	6	90	92	143	252	
4	7	—	—	150	249	
4	8	91	93	144	246	
4	9	92	94	145	243	
4	10	—	—	151	240	
4	11	93	95	146	237	
4	12	94	96	148	234	
4	13	—	—	153	231	
4	14	95	97	152	228	
4	15	96	98	154	225	
4	16	—	—	155	222	
4	17	97	99	156	219	
4	18	—	—	—	216	

## XC95144 I/O Pins (continued)

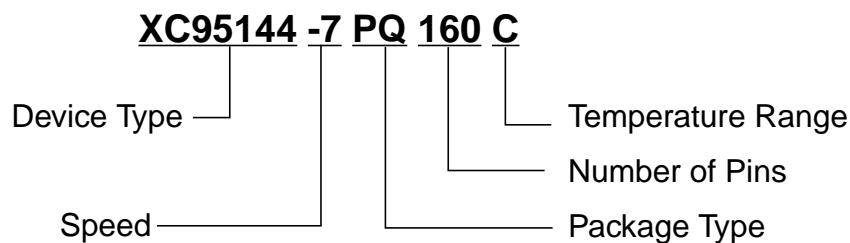
Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
5	1	—	—	65	213	
5	2	35	37	58	210	
5	3	—	—	66	207	
5	4	—	—	67	204	
5	5	36	38	59	201	
5	6	37	39	60	198	
5	7	—	—	74	195	
5	8	39	41	62	192	
5	9	40	42	63	189	
5	10	—	—	76	186	
5	11	41	43	64	183	
5	12	42	44	68	180	
5	13	—	—	78	177	
5	14	43	45	69	174	
5	15	46	48	72	171	
5	16	—	—	83	168	
5	17	49	51	77	165	
5	18	—	—	—	162	
6	1	—	—	—	159	
6	2	74	76	117	156	
6	3	—	—	119	153	
6	4	—	—	123	150	
6	5	76	78	122	147	
6	6	77	79	124	144	
6	7	—	—	125	141	
6	8	78	80	126	138	
6	9	79	81	129	135	
6	10	—	—	128	132	
6	11	80	82	133	129	
6	12	81	83	134	126	
6	13	—	—	130	123	
6	14	82	84	135	120	
6	15	85	87	138	117	
6	16	—	—	131	114	
6	17	86	88	139	111	
6	18	—	—	—	108	

Function Block	Macrocell	TQ 100	PQ 100	PQ 160	BScan Order	Notes
7	1	—	—	—	105	
7	2	50	52	79	102	
7	3	—	—	84	99	
7	4	—	—	85	96	
7	5	52	54	82	93	
7	6	53	55	86	90	
7	7	—	—	87	87	
7	8	54	56	88	84	
7	9	55	57	90	81	
7	10	—	—	89	78	
7	11	56	58	92	75	
7	12	58	60	95	72	
7	13	—	—	91	69	
7	14	59	61	96	66	
7	15	60	62	97	63	
7	16	—	—	93	60	
7	17	61	63	98	57	
7	18	—	—	—	54	
8	1	—	—	—	51	
8	2	63	65	101	48	
8	3	—	—	105	45	
8	4	—	—	107	42	
8	5	64	66	102	39	
8	6	65	67	103	36	
8	7	—	—	109	33	
8	8	66	68	104	30	
8	9	67	69	106	27	
8	10	—	—	112	24	
8	11	68	70	108	21	
8	12	70	72	111	18	
8	13	—	—	114	15	
8	14	71	73	113	12	
8	15	72	74	115	9	
8	16	—	—	118	6	
8	17	73	75	116	3	
8	18	—	—	—	0	

**XC95144 Global, JTAG and Power Pins**

<b>Pin Type</b>	<b>TQ100</b>	<b>PQ100</b>	<b>PQ160</b>
I/O/GCK1	22	24	33
I/O/GCK2	23	25	35
I/O/GCK3	27	29	42
I/O/GTS1	3	5	6
I/O/GTS2	4	6	8
I/O/GTS3	1	3	2
I/O/GTS4	2	4	4
I/O/GSR	99	1	159
TCK	48	50	75
TDI	45	47	71
TDO	83	85	136
TMS	47	49	73
V <sub>CCINT</sub> 5 V	5, 57, 98	7, 59, 100	10, 46, 94, 157
V <sub>CCIO</sub> 3.3 V/5 V	26, 38, 51, 88	28, 40, 53, 90	1, 41, 61, 81, 121, 141
GND	100, 21, 31, 44, 62, 69, 75, 84	2, 23, 33, 46, 64, 71, 77, 86	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160
No Connects	—	—	—

## Ordering Information



### Speed Options

- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay
- 7 7 ns pin-to-pin delay

### Packaging Options

- PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
- TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)
- PQ160 160-Pin Plastic Quad Flat Pack (PQFP)

### Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

## Component Availability

Pins		100		160
Type		Plastic PQFP	Plastic TQFP	Plastic PQFP
Code		PQ100	TQ100	PQ160
XC95144	-15	C,I	C,I	C,I
	-10	C,I	C,I	C,I
	-7	C	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C



October 28, 1997 (Version 2.0)

Product Specification

## Features

- 10 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 111 MHz
- 216 macrocells with 4800 usable gates
- Up to 166 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 160-pin PQFP, 352-pin BGA, and 208-pin HQFP packages

## Description

The XC95216 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twelve 36V18 Function Blocks, providing 4,800 usable gates with propagation delays of 10 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC95216 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95216 device.

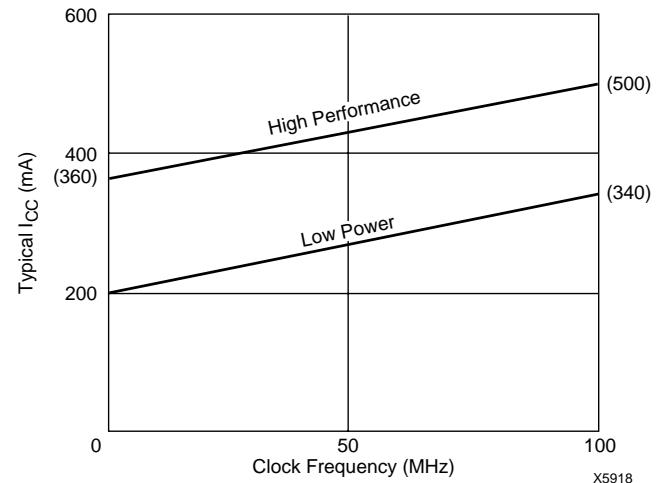
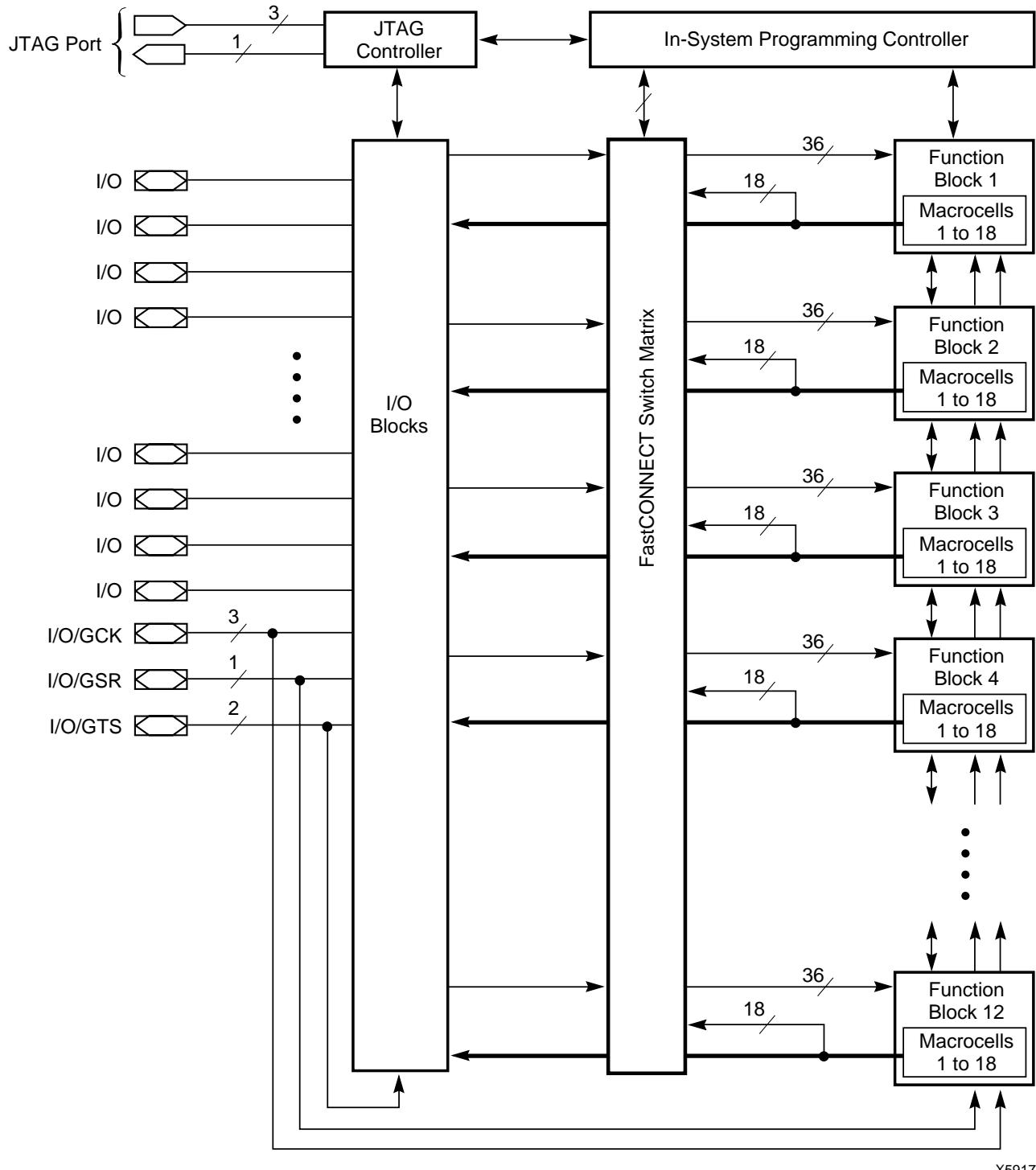


Figure 1: Typical  $I_{CC}$  vs. Frequency For XC95216



X5917

**Figure 2: XC95216 Architecture**

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

**Note:** 1. Numbers in parenthesis are for industrial-temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	200 (typ)		ma

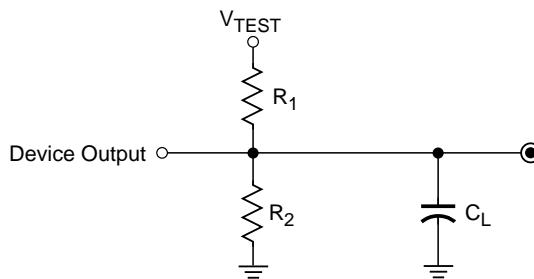
## AC Characteristics

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		10.0		15.0		20.0	ns
$t_{SU}$	I/O setup time before GCK	6.5		8.0		10.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		0.0		ns
$t_{CO}$	GCK to output valid		6.5		8.0		10.0	ns
$f_{CNT}^1$	16-bit counter frequency	111		95		83		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	67		56		50		MHz
$t_{PSU}$	I/O setup time before p-term clock input	2.5		4.0		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		4.0		6.0		ns
$t_{PCO}$	P-term clock to output valid		10.5		12.0		16.0	ns
$t_{OE}$	GTS to output valid		10.0		15.0		20.0	ns
$t_{OD}$	GTS to output disable		10.0		15.0		20.0	ns
$t_{POE}$	Product term OE to output enabled		15.5		18.0		22.0	ns
$t_{POD}$	Product term OE to output disabled		15.5		18.0		22.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		4.5		5.5		5.5	ns

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available, using the local feedback when applicable.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V <sub>CCIO</sub>	V <sub>TEST</sub>	R <sub>1</sub>	R <sub>2</sub>	C <sub>L</sub>
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
<b>Buffer Delays</b>								
t <sub>IN</sub>	Input buffer delay		3.5		4.5		6.5	ns
t <sub>GCK</sub>	GCK buffer delay		3.0		3.0		3.0	ns
t <sub>GSR</sub>	GSR buffer delay		6.0		7.5		9.5	ns
t <sub>GTS</sub>	GTS buffer delay		10.0		15.0		20.0	ns
t <sub>OUT</sub>	Output buffer delay		3.0		4.5		6.5	ns
t <sub>EN</sub>	Output buffer enable/disable delay		0.0		0.0		0.0	ns
<b>Product Term Control Delays</b>								
t <sub>PTCK</sub>	Product term clock delay		3.5		2.5		2.5	ns
t <sub>PTSR</sub>	Product term set/reset delay		2.5		3.0		3.0	ns
t <sub>PTTS</sub>	Product term 3-state delay		12.0		13.5		15.5	ns
<b>Internal Register and Combinatorial delays</b>								
t <sub>PDI</sub>	Combinatorial logic propagation delay		1.0		3.0		4.0	ns
t <sub>SUI</sub>	Register setup time	3.5		3.5		3.5		ns
t <sub>HI</sub>	Register hold time	3.0		4.5		6.5		ns
t <sub>COI</sub>	Register clock to output valid time		0.5		0.5		0.5	ns
t <sub>AOI</sub>	Register async. S/R to output delay		7.0		8.0		9.0	ns
t <sub>RAI</sub>	Register async. S/R recovery before clock	10.0		15.0		20.0		ns
t <sub>LOGI</sub>	Internal logic delay		2.5		3.0		3.0	ns
t <sub>LOGILP</sub>	Internal low power logic delay		11.0		11.5		11.5	ns
<b>Feedback Delays</b>								
t <sub>F</sub>	FastCONNECT matrix feedback delay		8.5		11.0		13.0	ns
t <sub>LF</sub>	Function Block local feedback delay		2.5		3.5		5.0	ns
<b>Time Adders</b>								
t <sub>PTA</sub> <sup>3</sup>	Incremental Product Term Allocator delay		1.0		1.5		1.5	ns
t <sub>SLEW</sub>	Slew-rate limited delay		4.5		5.0		5.5	ns

**Note:** 3. t<sub>PTA</sub> is multiplied by the span of the function as defined in the family data sheet.

**XC95216 I/O Pins**

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
1	1	—	—	—	645	
1	2	18	22	M25	642	
1	3	19	23	M26	639	
1	4	—	28	N26	636	
1	5	21	25	N25	633	
1	6	22	30	P23	630	
1	7	—	—	—	627	
1	8	23	31	P24	624	
1	9	24	32	R26	621	
1	10	—	12	G26	618	
1	11	25	33	R24	615	
1	12	26	34	T26	612	
1	13	—	—	—	609	
1	14	27	35	T25	606	
1	15	28	36	T23	603	
1	16	29	37	V26	600	
1	17	30	38	U24	597	
1	18	—	—	—	594	
2	1	—	—	—	591	
2	2	6	7	E25	588	[1]
2	3	7	8	G24	585	
2	4	—	29	P25	582	
2	5	8	9	F26	579	[1]
2	6	9	10	H23	576	
2	7	—	—	—	573	
2	8	11	15	K23	570	
2	9	12	16	K24	567	
2	10	—	-	—	564	
2	11	13	17	J25	561	
2	12	14	18	L24	558	
2	13	—	—	—	555	
2	14	15	19	K25	552	
2	15	16	20	L26	549	
2	16	—	14	H25	546	
2	17	17	21	M24	543	
2	18	—	—	—	540	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
3	1	—	—	—	537	
3	2	32	43	AA26	534	
3	3	33	44	Y24	531	[1]
3	4	—	39	U23	528	
3	5	34	45	AB25	525	
3	6	35	46	AA24	522	[1]
3	7	—	—	—	519	
3	8	36	47	Y23	516	
3	9	37	49	AA23	513	
3	10	—	67	AD18	510	
3	11	38	50	AB24	507	
3	12	39	51	AD25	504	
3	13	—	—	—	501	
3	14	42	55	AD23	498	[1]
3	15	43	56	AF24	495	
3	16	—	80	AE12	492	
3	17	44	57	AE23	489	
3	18	—	—	—	486	
4	1	—	—	—	483	
4	2	152	198	D18	480	
4	3	153	199	A21	477	
4	4	—	196	B19	474	
4	5	154	200	B20	471	
4	6	155	201	C20	468	
4	7	—	—	—	465	
4	8	156	202	B22	462	
4	9	158	205	B24	459	
4	10	—	-	—	456	
4	11	159	206	C23	453	[1]
4	12	2	3	E23	450	[1]
4	13	—	—	—	447	
4	14	3	4	C26	444	
4	15	4	5	E24	441	[1]
4	16	—	203	D20	438	
4	17	5	6	F24	435	
4	18	—	—	—	432	

## XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
5	1	—	—	—	429	
5	2	45	58	AE22	426	
5	3	47	60	AE21	423	
5	4	—	41	W25	420	
5	5	48	61	AF21	417	
5	6	49	63	AD19	414	
5	7	—	—	—	411	
5	8	50	64	AE20	408	
5	9	52	70	AF18	405	
5	10	—	109	AD1	402	
5	11	53	71	AE17	399	
5	12	54	72	AE16	396	
5	13	—	—	—	393	
5	14	55	73	AF16	390	
5	15	56	74	AE14	387	
5	16	—	40	Y26	384	
5	17	57	75	AF14	381	
5	18	—	—	—	378	
6	1	—	—	—	375	
6	2	140	180	A12	372	
6	3	142	182	A13	369	
6	4	—	208	D22	366	
6	5	143	185	C14	363	
6	6	144	186	A15	360	
6	7	—	—	—	357	
6	8	145	187	B15	354	
6	9	146	188	C15	351	
6	10	—	183	B14	348	
6	11	147	191	A16	345	
6	12	148	192	C16	342	
6	13	—	—	—	339	
6	14	149	193	C17	336	
6	15	150	194	B18	333	
6	16	—	169	D9	330	
6	17	151	197	C19	327	
6	18	—	—	—	324	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
7	1	—	—	—	321	
7	2	58	76	AE13	318	
7	3	59	77	AC13	315	
7	4	—	54	AE24	312	
7	5	60	78	AD13	309	
7	6	62	82	AD12	306	
7	7	—	—	—	303	
7	8	63	83	AC12	300	
7	9	64	84	AF11	297	
7	10	—	91	AD8	294	
7	11	65	85	AE11	291	
7	12	66	86	AE9	288	
7	13	—	—	—	285	
7	14	67	87	AD9	282	
7	15	68	88	AC10	279	
7	16	—	48	AC26	276	
7	17	69	89	AF7	273	
7	18	—	—	—	270	
8	1	—	—	—	267	
8	2	126	162	B5	264	
8	3	128	164	B6	261	
8	4	—	143	J1	258	
8	5	129	166	D8	255	
8	6	130	167	B7	252	
8	7	—	—	—	249	
8	8	131	170	C10	246	
8	9	132	171	B9	243	
8	10	—	195	A20	240	
8	11	133	173	A9	237	
8	12	134	174	D11	234	
8	13	—	—	—	231	
8	14	135	175	B11	228	
8	15	138	178	C12	225	
8	16	—	189	D15	222	
8	17	139	179	B12	219	
8	18	—	—	—	216	

**XC95216 I/O Pins (continued)**

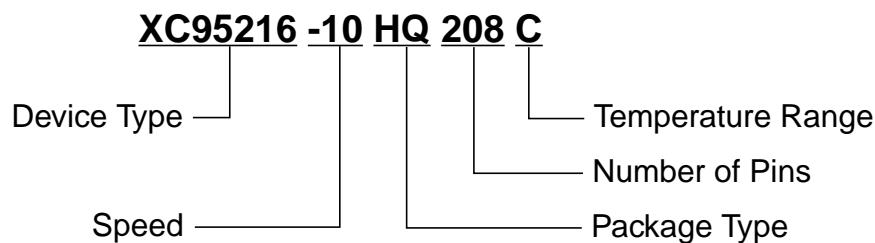
Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
9	1	—	—	—	213	
9	2	72	95	AD7	210	
9	3	74	97	AE5	207	
9	4	—	101	AD4	204	
9	5	76	99	AC7	201	
9	6	77	100	AE3	198	
9	7	—	—	—	195	
9	8	78	102	AC5	192	
9	9	79	103	AD3	189	
9	10	—	90	AE8	186	
9	11	82	110	AA4	183	
9	12	83	111	AB2	180	
9	13	—	—	—	177	
9	14	84	112	AC1	174	
9	15	85	113	AA2	171	
9	16	—	62	AC19	168	
9	17	86	114	AA1	165	
9	18	—	—	—	162	
10	1	—	—	—	159	
10	2	113	147	H3	156	
10	3	114	148	J4	153	
10	4	—	144	K3	150	
10	5	115	149	G2	147	
10	6	116	150	G3	144	
10	7	—	—	—	141	
10	8	117	152	E2	138	
10	9	118	154	D2	135	
10	10	—	168	A7	132	
10	11	119	155	F4	129	
10	12	122	158	B3	126	
10	13	—	—	—	123	
10	14	123	159	A3	120	
10	15	124	160	D6	117	
10	16	—	165	A6	114	
10	17	125	161	C6	111	
10	18	—	—	—	108	

Function Block	Macrocell	PQ160	HQ208	BG352	BScan Order	Notes
11	1	—	—	—	105	
11	2	87	115	Y1	102	
11	3	88	116	V4	99	
11	4	—	119	U4	96	
11	5	89	117	V3	93	
11	6	90	118	W2	90	
11	7	—	—	—	87	
11	8	91	121	V2	84	
11	9	92	122	U2	81	
11	10	—	107	AC3	78	
11	11	93	123	T2	75	
11	12	95	125	R4	72	
11	13	—	—	—	69	
11	14	96	126	R3	66	
11	15	97	127	R2	63	
11	16	—	120	U3	60	
11	17	98	128	R1	57	
11	18	—	—	—	54	
12	1	—	—	—	51	
12	2	101	131	P1	48	
12	3	102	133	N2	45	
12	4	—	106	AD2	42	
12	5	103	134	N4	39	
12	6	104	135	N3	36	
12	7	—	—	—	33	
12	8	105	136	M1	30	
12	9	106	137	M3	27	
12	10	—	151	F2	24	
12	11	107	138	M4	21	
12	12	108	139	L1	18	
12	13	—	—	—	15	
12	14	109	140	L2	12	
12	15	111	145	G1	9	
12	16	—	142	L3	6	
12	17	112	146	H2	3	
12	18	—	—	—	0	

## XC95216 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208	BG352
I/O/GCK1	33	44	Y24
I/O/GCK2	35	46	AA24
I/O/GCK3	42	55	AD23
I/O/GTS1	6	7	E25
I/O/GTS2	8	9	F26
I/O/GTS3	2	3	E23
I/O/GTS4	4	5	E24
I/O/GSR	159	206	C23
TCK	75	98	AD6
TDI	71	94	AF6
TDO	136	176	D12
TMS	73	96	AE6
V <sub>CCINT</sub> 5 V	10,46,94,157	11, 59, 124, 153, 204	H24, AF23, T1, G4, C22
V <sub>CCIO</sub> 3.3 V/5 V	1,41,61,81,121,141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184	A10, A17, B2, B25, D7, D13, D19, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC8, AC14, AC20, AE25, AF10, AF17
GND	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160	2, 13, 24, 27, 42, 52, 66, 68, 69, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, C7, E1, E26, H1, H26, N1, P3, P26, V23, W1, W26, AB1, AB4, AB26, AC9, AC17, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF20, AF22, AF25, AF26
No Connects	—	—	A4, A11, A18, A23, A24, B4, B8, B10, B13, B16, B17, B21, B23, C1, C2, C3, C4, C5, C8, C9, C11, C13, C18, C21, C24, C25, D1, D3, D4, D5, D10, D14, D16, D17, D21, D23, D24, D25, D26, E3, E4, F1, F3, F23, F25, G25, J2, J3, J23, J24, J26, K2, K4, L4, L23, L25, M2, M23, N24, P2, R23, R25, T3, T4, T24, U25, V1, V24, V25, W3, W4, W24, Y2, Y3, Y25, AA3, AA25, AB3, AB23, AC2, AC4, AC6, AC11, AC15, AC16, AC18, AC21, AC22, AC23, AC24, AC25, AD5, AD10, AD11, AD14, AD15, AD16, AD17, AD20, AD21, AD22, AD24, AD26, AE2, AE4, AE7, AE10, AE15, AE18, AE19, AF3, AF4, AF9, AF12, AF15

## Ordering Information



### Speed Options

- 20 20 ns pin-to-pin delay
- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay

### Packaging Options

- PQ160 160-Pin Plastic Quad Flat Pack (PQFP)
- HQ208 208-Pin Heat Sink Quad Flat Pack (HQFP)
- BG352 352-Pin Ball Grid Array (BGA)

### Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

## Component Availability

Pins		160	160	352
Type		Plastic PQFP	Power QFP	Plastic BGA
Code		PQ160	HQ208	BG352
XC95216	-20	C,I	C,I	C,I
	-15	C	C	C,I
	-10	C	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C

November 12, 1997 (Version 2.0)

Preliminary Product Specification

## Features

- 15 ns pin-to-pin logic delays on all pins
- $f_{CNT}$  to 95 MHz
- 288 macrocells with 6,400 usable gates
- Up to 192 user I/O pins
- 5 V in-system programmable
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 352-pin BGA and 208-pin HQFP packages

## Description

The XC95288 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of sixteen 36V18 Function Blocks, providing 6,400 usable gates with propagation delays of 10 ns. See Figure 2 for the architecture overview.

## Power Management

Power dissipation can be reduced in the XC95288 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} (\text{mA}) =$$

$$MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode

$MC_{LP}$  = Macrocells in low-power mode

$MC$  = Total number of macrocells used

$f$  = Clock frequency (MHz)

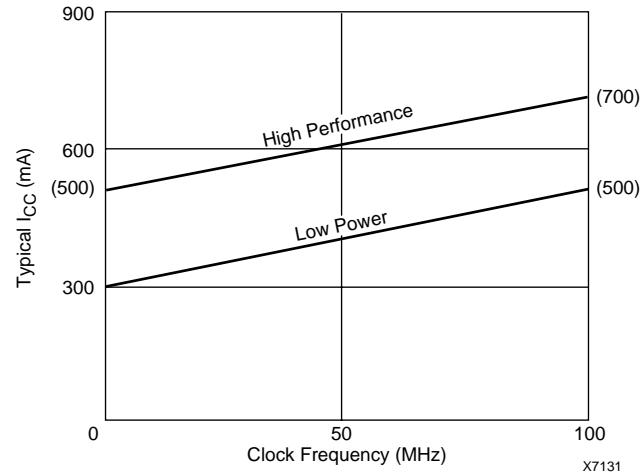
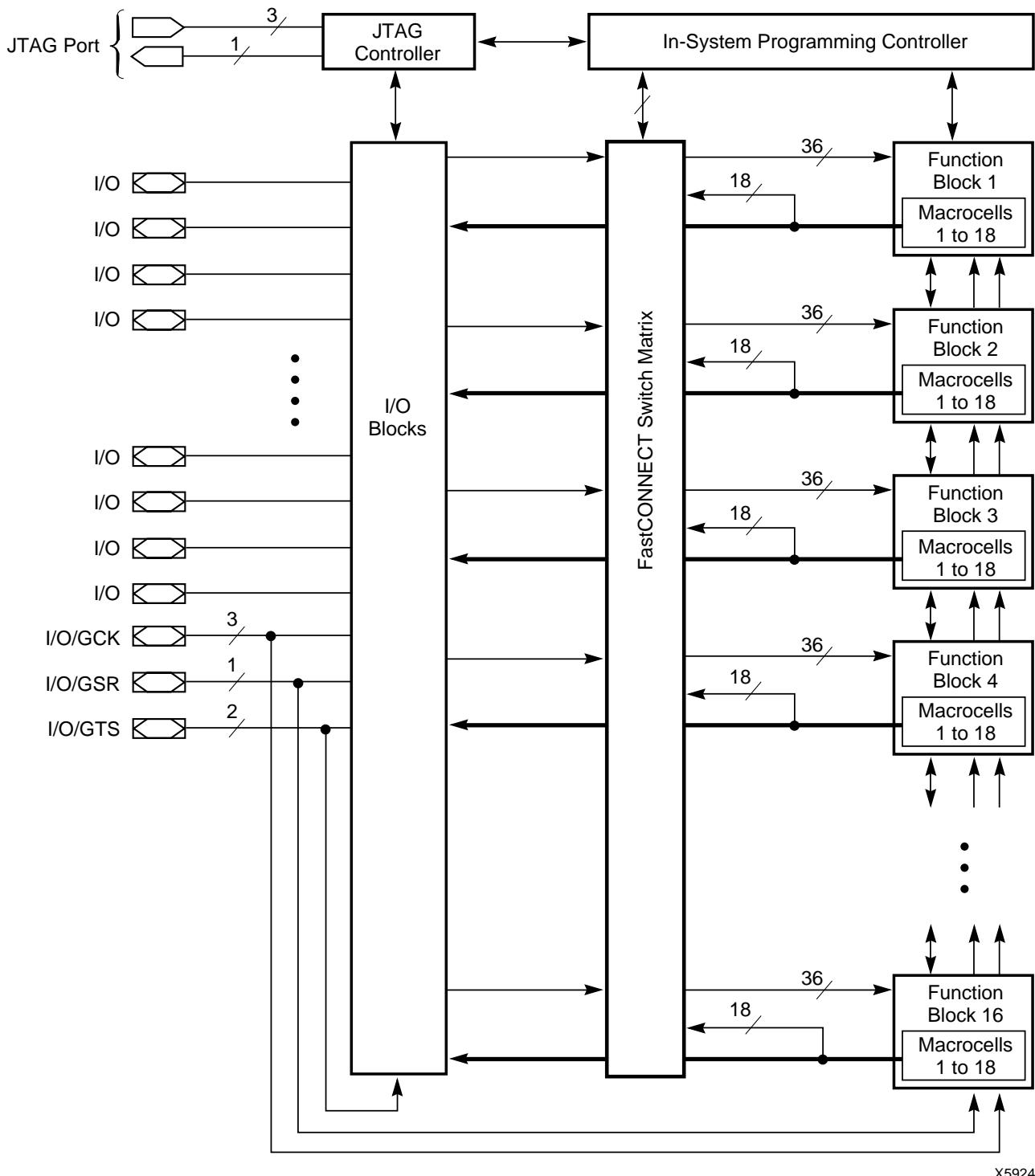


Figure 1: Typical  $I_{CC}$  vs. Frequency For XC95288



X5924

**Figure 2: XC95288 Architecture**

**Note:** Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 7.0	V
$V_{IN}$	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## Recommended Operation Conditions<sup>1</sup>

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
$V_{CCIO}$	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.80	V
$V_{IH}$	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V

**Note:** 1. Numbers in parenthesis are for industrial-temperature range versions.

## Endurance Characteristics

Symbol	Parameter	Min	Max	Units
$t_{DR}$	Data Retention	20	-	Years
$N_{PE}$	Program/Erase Cycles	10,000	-	Cycles

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$I_{IH}$	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}$	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	300 (Typ)		ma

## AC Characteristics

Symbol	Parameter	XC95288-15		XC95288-20		Units
		Min	Max	Min	Max	
$t_{PD}$	I/O to output valid		15.0		20.0	ns
$t_{SU}$	I/O setup time before GCK	8.0		10.0		ns
$t_H$	I/O hold time after GCK	0.0		0.0		ns
$t_{CO}$	GCK to output valid		8.0		10.0	ns
$f_{CNT}^1$	16-bit counter frequency	95		83		MHz
$f_{SYSTEM}^2$	Multiple FB internal operating frequency	56		50		MHz
$t_{PSU}$	I/O setup time before p-term clock input	4.0		4.0		ns
$t_{PH}$	I/O hold time after p-term clock input	4.0		6.0		ns
$t_{PCO}$	P-term clock to output valid		12.0		16.0	ns
$t_{OE}$	GTS to output valid		15.0		20.0	ns
$t_{OD}$	GTS to output disable		15.0		20.0	ns
$t_{POE}$	Product term OE to output enabled		18.0		22.0	ns
$t_{POD}$	Product term OE to output disabled		18.0		22.0	ns
$t_{WLH}$	GCK pulse width (High or Low)		5.5		5.5	ns

**Note:** 1.  $f_{CNT}$  is the fastest 16-bit counter frequency available, using the local feedback when applicable.

$f_{CNT}$  is also the Export Control Maximum flip-flop toggle rate,  $f_{TOG}$ .

2.  $f_{SYSTEM}$  is the internal operating frequency for general purpose system designs spanning multiple FBs.

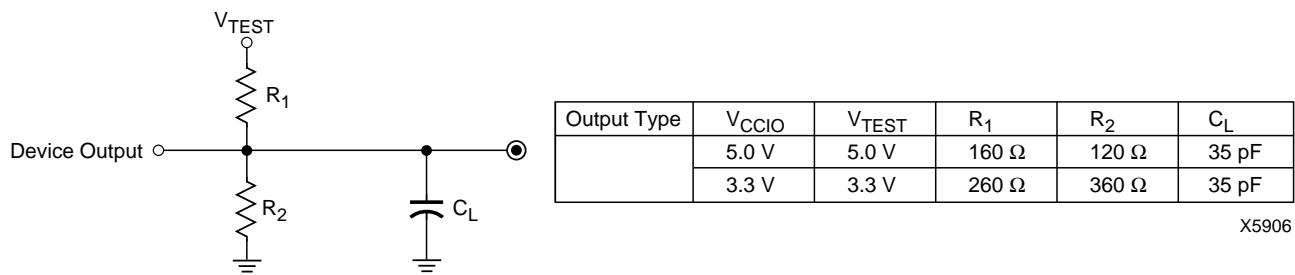


Figure 3: AC Load Circuit

## Internal Timing Parameters

Symbol	Parameter	XC95288-15		XC95288-20		Units
		Min	Max	Min	Max	
<b>Buffer Delays</b>						
$t_{IN}$	Input buffer delay		4.5		6.5	ns
$t_{GCK}$	GCK buffer delay		3.0		3.0	ns
$t_{GSR}$	GSR buffer delay		7.5		9.5	ns
$t_{GTS}$	GTS buffer delay		15.0		20.0	ns
$t_{OUT}$	Output buffer delay		4.5		6.5	ns
$t_{EN}$	Output buffer enable/disable delay		0.0		0.0	ns
<b>Product Term Control Delays</b>						
$t_{PTCK}$	Product term clock delay		2.5		2.5	ns
$t_{PTSR}$	Product term set/reset delay		3.0		3.0	ns
$t_{PTTS}$	Product term 3-state delay		13.5		15.5	ns
<b>Internal Register and Combinatorial delays</b>						
$t_{PDI}$	Combinatorial logic propagation delay		3.0		4.0	ns
$t_{SUI}$	Register setup time	3.5		3.5		ns
$t_{HI}$	Register hold time	4.5		6.5		ns
$t_{COI}$	Register clock to output valid time		0.5		0.5	ns
$t_{AOI}$	Register async. S/R to output delay		8.0		9.0	ns
$t_{RAI}$	Register async. S/R recovery before clock	15.0		20.0		ns
$t_{LOGI}$	Internal logic delay		3.0		3.0	ns
$t_{LOGILP}$	Internal low power logic delay		11.5		11.5	ns
<b>Feedback Delays</b>						
$t_F$	FastCONNECT matrix feedback delay		11.0		13.0	ns
$t_{LF}$	Function Block local feedback delay		3.5		5.0	ns
<b>Time Adders</b>						
$t_{PTA}^3$	Incremental Product Term Allocator delay		1.5		1.5	ns
$t_{SLEW}$	Slew-rate limited delay		5.0		5.5	ns

**Note:** 3.  $t_{PTA}$  is multiplied by the span of the function as defined in the family data sheet.

**XC95288 I/O Pins**

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
1	1	—	—	861	
1	2	28	N26	858	
1	3	29	P25	855	
1	4	—	—	852	
1	5	30	P23	849	
1	6	31	P24	846	
1	7	—	—	843	
1	8	32	R26	840	
1	9	—	R25	837	
1	10	33	R24	834	
1	11	—	R23	831	
1	12	34	T26	828	
1	13	—	—	825	
1	14	35	T25	822	
1	15	36	T23	819	
1	16	—	—	816	
1	17	37	V26	813	
1	18	—	—	810	
2	1	—	—	807	
2	2	15	K23	804	
2	3	16	K24	801	
2	4	—	—	798	
2	5	17	J25	795	
2	6	18	L24	792	
2	7	—	—	789	
2	8	19	K25	786	
2	9	—	L25	783	
2	10	20	L26	780	
2	11	—	M23	777	
2	12	21	M24	774	
2	13	—	—	771	
2	14	22	M25	768	
2	15	23	M26	765	
2	16	—	—	762	
2	17	25	N25	759	
2	18	—	—	756	

**Notes:** [1] Global control pin

Macrocell outputs to package pins subject to change, contact factory for latest information. Power, GND, JTAG and Global Signals are fixed.

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
3	1	—	—	753	
3	2	38	U24	750	
3	3	39	U23	747	
3	4	—	—	744	
3	5	40	Y26	741	
3	6	41	W25	738	
3	7	—	—	735	
3	8	43	AA26	732	
3	9	—	Y25	729	
3	10	44	Y24	726	[1]
3	11	—	AA25	723	
3	12	45	AB25	720	
3	13	—	—	717	
3	14	46	AA24	714	[1]
3	15	47	Y23	711	
3	16	—	—	708	
3	17	48	AC26	705	
3	18	—	—	702	
4	1	—	—	699	
4	2	3	E23	696	[1]
4	3	4	C26	693	
4	4	—	—	690	
4	5	5	E24	687	[1]
4	6	6	F24	684	
4	7	—	—	681	
4	8	7	E25	678	[1]
4	9	—	D26	675	
4	10	8	G24	672	
4	11	—	F25	669	
4	12	9	F26	666	[1]
4	13	—	—	663	
4	14	10	H23	660	
4	15	12	G26	657	
4	16	—	—	654	
4	17	14	H25	651	
4	18	—	—	648	

## XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
5	1	—	—	645	
5	2	49	AA23	642	
5	3	50	AB24	639	
5	4	—	—	636	
5	5	51	AD25	633	
5	6	54	AE24	630	
5	7	—	—	627	
5	8	55	AD23	624	[1]
5	9	—	AC22	621	
5	10	56	AF24	618	
5	11	—	AD22	615	
5	12	57	AE23	612	
5	13	—	—	609	
5	14	58	AE22	606	
5	15	60	AE21	603	
5	16	—	—	600	
5	17	61	AF21	597	
5	18	—	—	594	
6	1	—	—	591	
6	2	197	C19	588	
6	3	198	D18	585	
6	4	—	—	582	
6	5	199	A21	579	
6	6	200	B20	576	
6	7	—	—	573	
6	8	201	C20	570	
6	9	—	B21	567	
6	10	202	B22	564	
6	11	—	C21	561	
6	12	203	D20	558	
6	13	—	—	555	
6	14	205	B24	552	
6	15	206	C23	549	[1]
6	16	—	—	546	
6	17	208	D22	543	
6	18	—	—	540	

**Note:** [1] Global control pin

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
7	1	—	—	537	
7	2	62	AC19	534	
7	3	63	AD19	531	
7	4	—	—	528	
7	5	64	AE20	525	
7	6	66	AC18	522	
7	7	—	—	519	
7	8	67	AD18	516	
7	9	—	AE19	513	
7	10	69	AD17	510	
7	11	—	AE18	507	
7	12	70	AF18	504	
7	13	—	—	501	
7	14	71	AE17	498	
7	15	72	AE16	495	
7	16	—	—	492	
7	17	73	AF16	489	
7	18	—	—	486	
8	1	—	—	483	
8	2	186	A15	480	
8	3	187	B15	477	
8	4	—	—	474	
8	5	188	C15	471	
8	6	189	D15	468	
8	7	—	—	465	
8	8	191	A16	462	
8	9	—	B16	459	
8	10	192	C16	456	
8	11	—	B17	453	
8	12	193	C17	450	
8	13	—	—	447	
8	14	194	B18	444	
8	15	195	A20	441	
8	16	—	—	438	
8	17	196	B19	435	
8	18	—	—	432	

**XC95288 I/O Pins (continued)**

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
9	1	—	—	429	
9	2	74	AE14	426	
9	3	75	AF14	423	
9	4	—	—	420	
9	5	76	AE13	417	
9	6	77	AC13	414	
9	7	—	—	411	
9	8	78	AD13	408	
9	9	—	AF12	405	
9	10	80	AE12	402	
9	11	82	AD12	399	
9	12	83	AC12	396	
9	13	—	—	393	
9	14	84	AF11	390	
9	15	85	AE11	387	
9	16	—	—	384	
9	17	86	AE9	381	
9	18	—	—	378	
10	1	—	—	375	
10	2	170	C10	372	
10	3	171	B9	369	
10	4	—	—	366	
10	5	173	A9	363	
10	6	174	D11	360	
10	7	—	—	357	
10	8	175	B11	354	
10	9	—	A11	351	
10	10	178	C12	348	
10	11	179	B12	345	
10	12	180	A12	342	
10	13	—	—	339	
10	14	182	A13	336	
10	15	183	B14	333	
10	16	—	—	330	
10	17	185	C14	327	
10	18	—	—	324	

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
11	1	—	—	321	
11	2	87	AD9	318	
11	3	88	AC10	315	
11	4	—	—	312	
11	5	89	AF7	309	
11	6	90	AE8	306	
11	7	—	—	303	
11	8	91	AD8	300	
11	9	—	AE7	297	
11	10	95	AD7	294	
11	11	97	AE5	291	
11	12	99	AC7	288	
11	13	—	—	285	
11	14	100	AE3	282	
11	15	101	AD4	279	
11	16	—	—	276	
11	17	102	AC5	273	
11	18	—	—	270	
12	1	—	—	267	
12	2	158	B3	264	
12	3	159	A3	261	
12	4	—	—	258	
12	5	160	D6	255	
12	6	161	C6	252	
12	7	—	—	249	
12	8	162	B5	246	
12	9	—	A4	243	
12	10	164	B6	240	
12	11	165	A6	237	
12	12	166	D8	234	
12	13	—	—	231	
12	14	167	B7	228	
12	15	168	A7	225	
12	16	—	—	222	
12	17	169	D9	219	
12	18	—	—	216	

## XC95288 I/O Pins (continued)

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
13	1	—	—	213	
13	2	103	AD3	210	
13	3	106	AD2	207	
13	4	—	—	204	
13	5	107	AC3	201	
13	6	109	AD1	198	
13	7	—	—	195	
13	8	110	AA4	192	
13	9	—	AA3	189	
13	10	111	AB2	186	
13	11	112	AC1	183	
13	12	113	AA2	180	
13	13	—	—	177	
13	14	114	AA1	174	
13	15	115	Y1	171	
13	16	—	—	168	
13	17	116	V4	165	
13	18	—	—	162	
14	1	—	—	159	
14	2	144	K3	156	
14	3	145	G1	153	
14	4	—	—	150	
14	5	146	H2	147	
14	6	147	H3	144	
14	7	—	—	141	
14	8	148	J4	138	
14	9	—	F1	135	
14	10	149	G2	132	
14	11	150	G3	129	
14	12	151	F2	126	
14	13	—	—	123	
14	14	152	E2	120	
14	15	154	D2	117	
14	16	—	—	114	
14	17	155	F4	111	
14	18	—	—	108	

Function Block	Macrocell	HQ208	BG352	BScan Order	Notes
15	1	—	—	105	
15	2	117	V3	102	
15	3	118	W2	99	
15	4	—	—	96	
15	5	119	U4	93	
15	6	120	U3	90	
15	7	—	—	87	
15	8	121	V2	84	
15	9	—	V1	81	
15	10	122	U2	78	
15	11	123	T2	75	
15	12	125	R4	72	
15	13	—	—	69	
15	14	126	R3	66	
15	15	127	R2	63	
15	16	—	—	60	
15	17	128	R1	57	
15	18	—	—	54	
16	1	—	—	51	
16	2	131	P1	48	
16	3	133	N2	45	
16	4	—	—	42	
16	5	134	N4	39	
16	6	135	N3	36	
16	7	—	—	33	
16	8	136	M1	30	
16	9	—	M2	27	
16	10	137	M3	24	
16	11	138	M4	21	
16	12	139	L1	18	
16	13	—	—	15	
16	14	140	L2	12	
16	15	142	L3	9	
16	16	—	—	6	
16	17	143	J1	3	
16	18	—	—	0	

**XC95288 Global, JTAG and Power Pins**

<b>Pin Type</b>	<b>HQ208</b>	<b>BG352</b>
I/O/GCK1	44	Y24
I/O/GCK2	46	AA24
I/O/GCK3	55	AD23
I/O/GTS1	7	E25
I/O/GTS2	9	F26
I/O/GTS3	3	E23
I/O/GTS4	5	E24
I/O/GSR	206	C23
TCK	98	AD6
TDI	94	AF6
TDO	176	D12
TMS	96	AE6
V <sub>CCINT</sub> 5 V	11, 59, 124, 153, 204	J23, V24, AF23, AC15, AF15, AD11, AD5, Y3, T1, J3, G4, D5, D10, B13, D17, C22, H24
V <sub>CCIO</sub> 3.3 V/5 V	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184	A10, A17, B2, B25, D7, D13, D19, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC8, AC14, AC20, AE25, AF10, AF17
GND	2, 13, 24, 27, 42, 52, 68, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, C7, C9, C13, C18, D24, E1, E26, H1, H26, K4, N1, N24, P3, P26, V23, W1, W4, W26, AB1, AB4, AB26, AC9, AD10, AD14, AD15, AD20, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26
No Connects		A18, A23, A24, B4, B8, B10, B23, C1, C2, C3, C4, C5, C8, C11, C24, C25, D1, D3, D4, D14, D16, D21, D23, D25, E3, E4, F3, F23, G25, J2, J24, J26, K2, L4, L23, P2, T3, T4, T24, U25, V25, W3, W24, Y2, AB3, AB23, AC2, AC4, AC6, AC11, AC16, AC17, AC21, AC23, AC24, AC25, AD16, AD21, AD24, AD26, AE2, AE4, AE10, AE15, AF3, AF4, AF9, AF20

## Ordering Information

### XC95288 -15 HQ 208 C

Device Type

Speed

Temperature Range

Number of Pins

Package Type

#### Speed Options

- 20 20 ns pin-to-pin delay
- 15 15 ns pin-to-pin delay

#### Packaging Options

- HQ208 208-Pin Heat Sink Quad Flat Pack (HQFP)
- BG352 352-Pin Plastic Ball Grid Array (BGA)

#### Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C

## Component Availability

Pins		208	352
Type		Plastic HQFP	Plastic BGA
Code		HQ	BG
XC95288	-20	C,I	C,I
	-15	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C





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# Virtex™ 2.5 V Field Programmable Gate Arrays

October 20, 1998 (Version 1.0)

Advance Product Specification

## Features

- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 50k to 1M system gates
  - System performance up to 150 MHz
  - 66-MHz PCI Compliant
  - Hot-swappable for Compact PCI
- Multi-standard SelectIO™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM™ devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device

- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.25-µm five-layer metal process
- 100% factory tested

## Description

The Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.25-µm CMOS process. These advances make Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the nine members shown in [Table 1](#).

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Table 1: Virtex Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	BlockRAM Bits	Max Select RAM Bits
XCV50	57,906	16x24	1,728	180	32,768	24,576
XCV100	108,904	20x30	2,700	180	40,960	38,400
XCV150	164,674	24x36	3,888	260	49,152	55,296
XCV200	236,666	28x42	5,292	260	57,344	75,264
XCV300	322,970	32x48	6,912	316	65,536	98,304
XCV400	468,252	40x60	10,800	404	81,920	153,600
XCV600	661,111	48x72	15,552	404	98,304	221,184
XCV800	888,439	56x84	21,168	404	114,688	301,056
XCV1000	1,124,022	64x96	27,648	404	131,072	393,216

## Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (Select-MAP™ and slave serial modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through floorplanning, simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

## Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates over 100 MHz including I/O; internal clock rates can easily exceed 100 MHz.

Table 2: Performance for Common Circuit Functions

Function	Bits	Virtex -6
<b>Register-to-Register</b>		
Adder	16	5.0 ns
	64	7.2 ns
Pipelined Multiplier	8 x 8	5.1 ns
	16 x 16	6.0 ns
Address Decoder	16	4.4 ns
	64	6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9	4.1 ns
	18	5.0 ns
	36	6.9 ns
<b>Chip-to-Chip</b>		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many tested designs operated internally at speeds in excess of 100 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

## Architectural Description

### Virtex Array

The Virtex user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

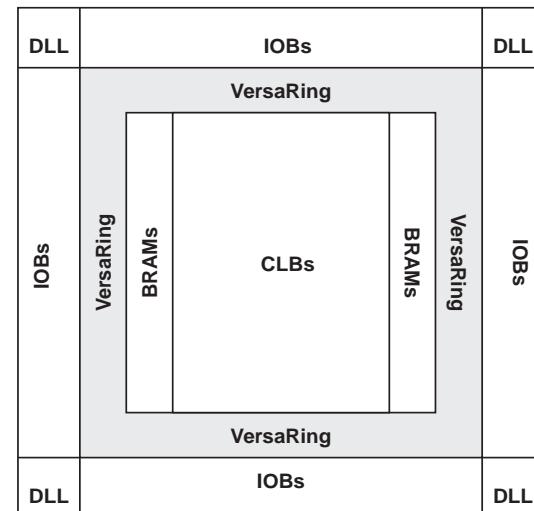
CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.



vao\_b.eps

Figure 1: Virtex Architecture Overview

A set of Supplementary Description documents published separately augment the following description of the various Virtex-architecture components. The Supplementary Descriptions provide more detailed information and cover the following topics.

- Input/Output Block
- Configurable Logic Block
- Memory Resources
- Clock Distribution
- Routing Resources
- Configuration and Readback
- Boundary Scan
- Power Consumption

## Input/Output Block

The Virtex IOB, [Figure 2](#), features SelectIO™ inputs and outputs that support a wide variety of I/O signalling standards, see [Table 3](#). These high-speed inputs and outputs are capable of supporting PCI interfaces up to 66 MHz.

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal

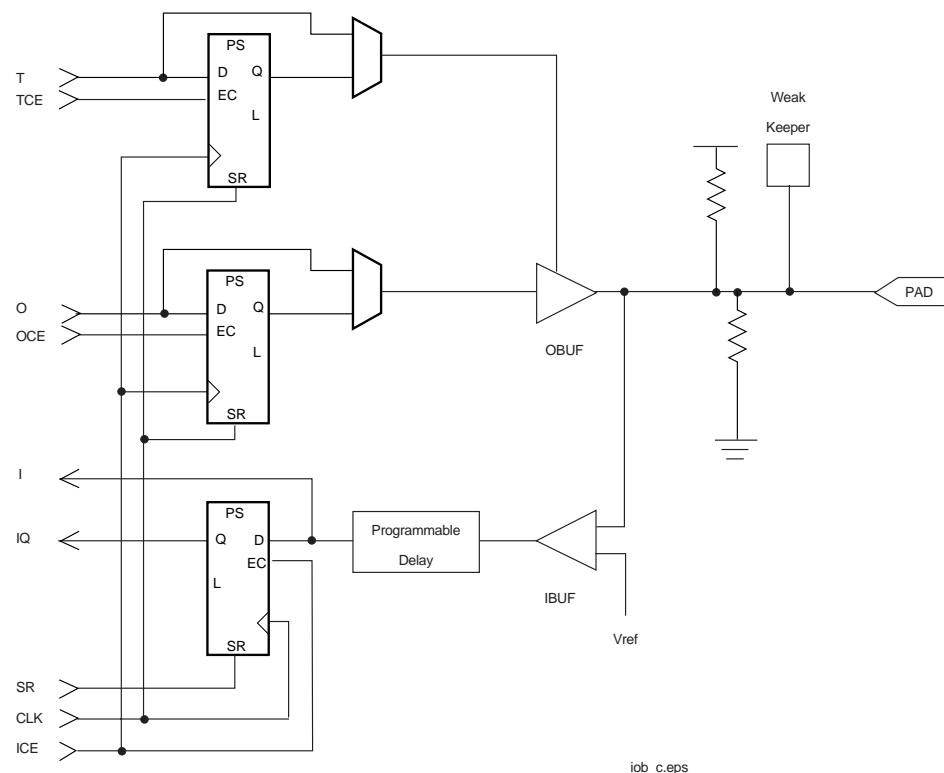
can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The input and output buffers and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5-V compliance, and one that does not. For 5-V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When 5-V compliance is not required, a conventional clamp diode may be connected to the output supply voltage,  $V_{CCO}$ . The type of over-voltage protection can be selected independently for each pad.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs are forced into their high-impedance state. The pull-up and pull-down resistors and the weak-keeper circuit are inactive, and input floats. If the design requires a defined input logic level prior to configuration, an external resistor must be used.

All Virtex IOBs support IEEE 1149.1-compatible boundary scan testing.



**Figure 2: Virtex Input/Output Block (IOB)**

**Table 3: Supported Select I/O Standards**

I/O Standard	Input Reference Voltage ( $V_{REF}$ )	Output Source Voltage ( $V_{CCO}$ )	Board Termination Voltage ( $V_{TT}$ )
LV-TTL	N/A	3.3	N/A
LVC-MOS2	N/A	2.5	N/A
PCI	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	1.5
HSTL Class III	0.75	1.5	1.5
HSTL Class IV	0.75	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.125	2.5	1.125
CTT	1.5	3.3	1.5
AGP	1.32	3.3	N/A

### ***Input Path***

A buffer in the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage,  $V_{REF}$ . The need to supply  $V_{REF}$  imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 4.

Optional pull-up and pull-down resistors exist at each input with a value of approximately 50 – 150 kohms.

### ***Output Path***

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flop that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 40mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied  $V_{CCO}$  voltage. The need to supply  $V_{CCO}$  imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 4.

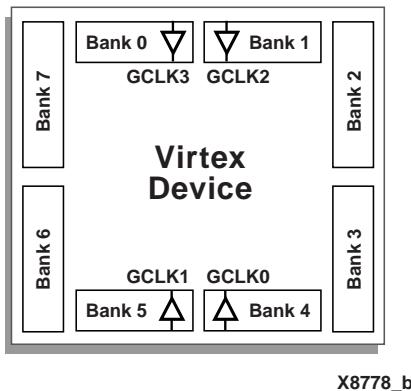
An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate  $V_{REF}$  voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

### ***I/O Banking***

Some of the I/O standards described above require  $V_{CCO}$  and/or  $V_{REF}$  voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple  $V_{CCO}$  pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.



**Figure 3: Virtex I/O Banks**

Within a bank, output standards may be mixed only if they use the same  $V_{CCO}$ . Compatible standards are shown in [Table 4](#). GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on  $V_{CCO}$ .

**Table 4: Compatible Output Standards**

$V_{CCO}$	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage,  $V_{REF}$ . In this case, certain user-I/O pins are automatically configured as inputs for the  $V_{REF}$  voltage. Approximately one in six of the I/O pins in the bank assume this role.

The  $V_{REF}$  pins within a bank are interconnected internally and consequently only one  $V_{REF}$  voltage can be used within each bank. All  $V_{REF}$  pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require  $V_{REF}$  can be mixed with those that do not. However, only one  $V_{REF}$  voltage may be used within a bank. Input buffers that use  $V_{REF}$  are not 5V-tolerant.

The  $V_{CCO}$  and  $V_{REF}$  pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of  $V_{REF}$  and  $V_{CCO}$  pins can vary depending on the size of device. In larger devices, more I/O pins convert to  $V_{REF}$  pins. Since these are always a superset of the  $V_{REF}$  pins used for smaller devices, it is possible to design a PCB that permits migration to a larger

device if necessary. All the  $V_{REF}$  pins for the largest device anticipated must be connected to the  $V_{REF}$  voltage, and not used for I/O.

In smaller devices, some  $V_{CCO}$  pins used in larger devices do not connect connected within the package. These unconnected pins may be left unconnected externally, or may be connected to the  $V_{CCO}$  voltage to permit migration to a larger device if necessary.

In HQ and PQ packages, all  $V_{CCO}$  pins are bonded together internally, and consequently the same  $V_{CCO}$  voltage must be connected to all of them. The  $V_{REF}$  pins remain internally connected as eight banks, and may be used as described previously.

## Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in [Figure 4](#). [Figure 5](#) shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

## Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a  $16 \times 1$ -bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a  $16 \times 2$ -bit or  $32 \times 1$ -bit synchronous RAM, or a  $16 \times 1$ -bit dual-port synchronous RAM.

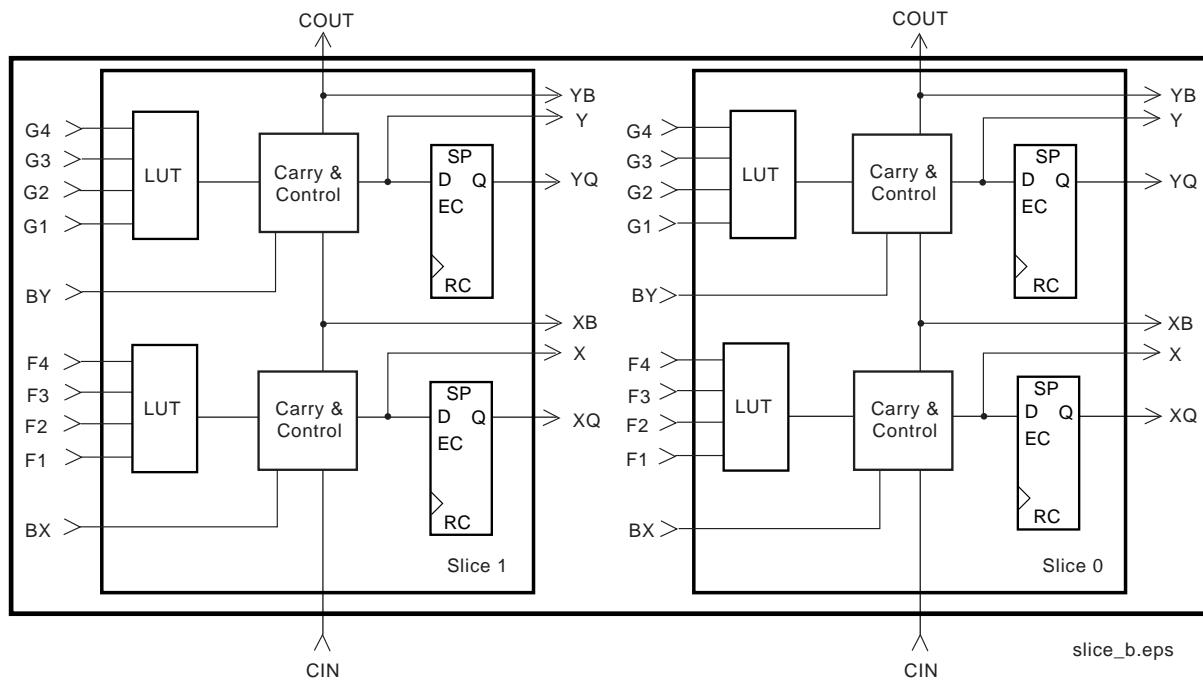
The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

## Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous Set and Reset signals (SR and BY). Alternatively, these signals may be configured as asynchronous Preset and Clear.

All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.



**Figure 4: Virtex CLB**

### Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

### Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### BUFTs

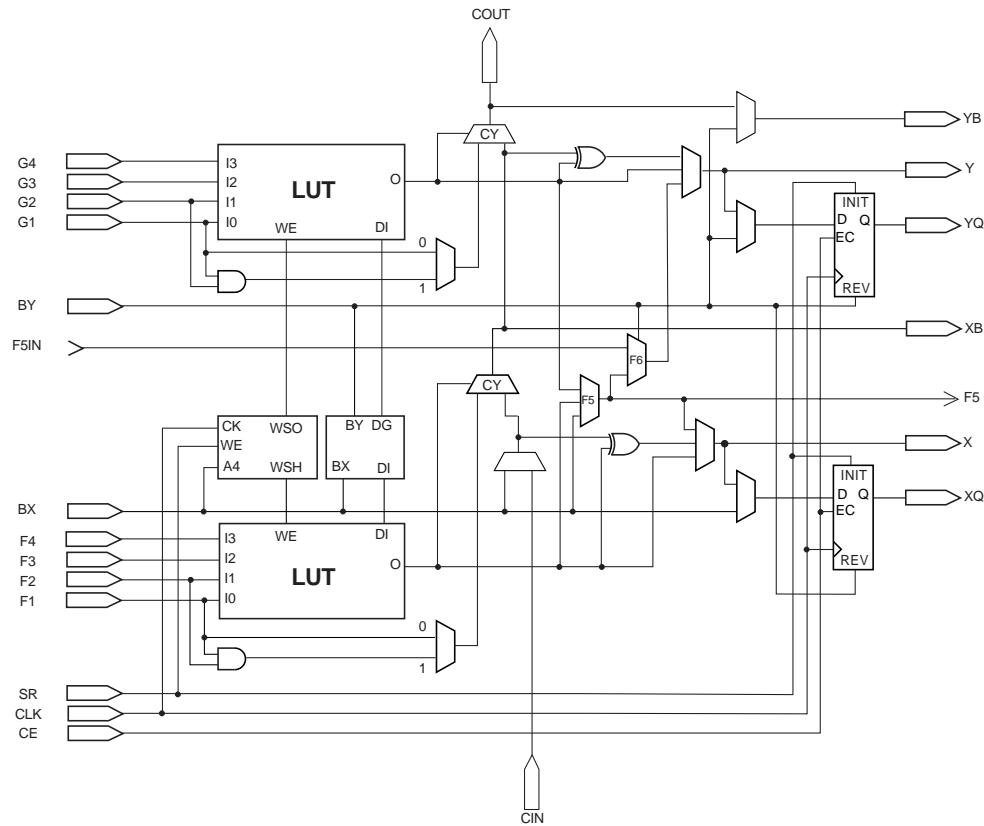
Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See “Dedicated Routing” on

[page 9](#). Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

### Block RAM

Virtex FPGAs incorporate several large BlockSelectRAM+ memories. These complement the distributed SelectRAM+ LUTRAMs that provide shallow RAM structures implemented in CLBs.

BlockSelectRAM+ memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high will contain 16 memory blocks per column, and a total of 32 blocks.



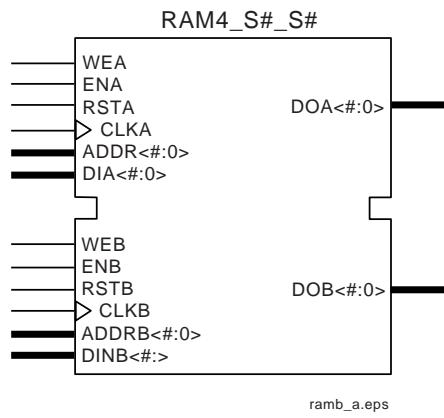
**Figure 5: Detailed View of Virtex Slice**

Table 5 shows the amount of Block SelectRAM+ memory that is available in each Virtex device.

Each BlockSelectRAM+ cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

**Table 5: Virtex Block SelectRAM+ Amounts**

Virtex Device	# of Blocks	Total Block SelectRAM+ Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072



**Figure 6: Dual-Port Block Select Ram+**

**Table 6** shows the depth and width aspect ratios for the Block SelectRAM+.

**Table 6: Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

## Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

## Local Routing

The VersaBlock provides local routing resources, as shown in [Figure 7](#), providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

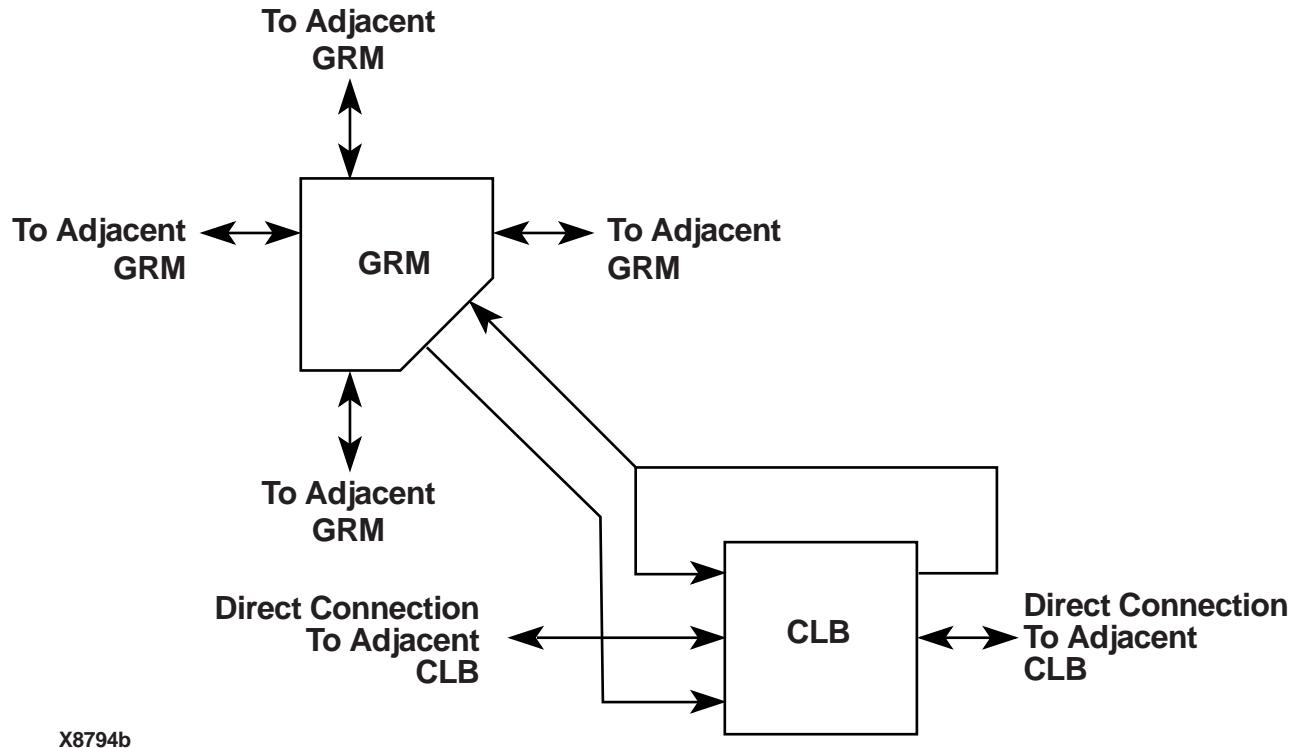
## General Purpose Routing

Most Virtex signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

## I/O Routing

Virtex devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.



**Figure 7: Virtex Local Routing**

### Dedicated Routing

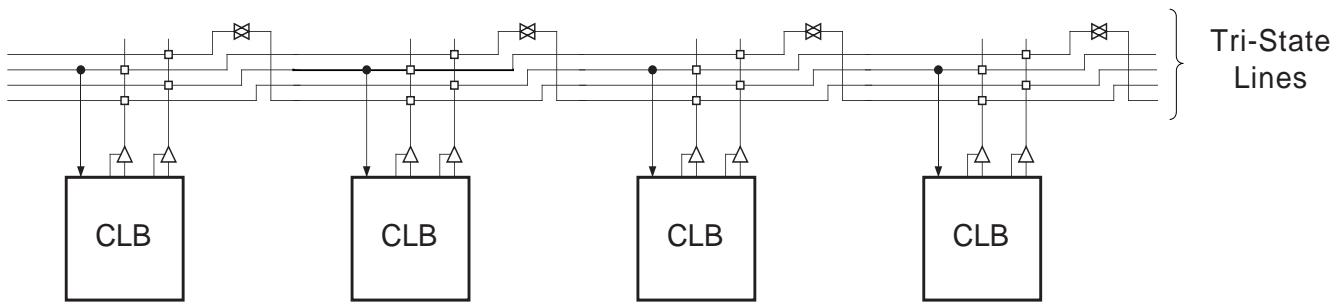
Some classes of signal require dedicated routing resources to maximize performance. In the Virtex architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in [Figure 8](#).
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

### Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only



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**Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines**

- be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

## Clock Distribution

Virtex provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in [Figure 9](#).

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

### Delay-Locked Loop (DLL)

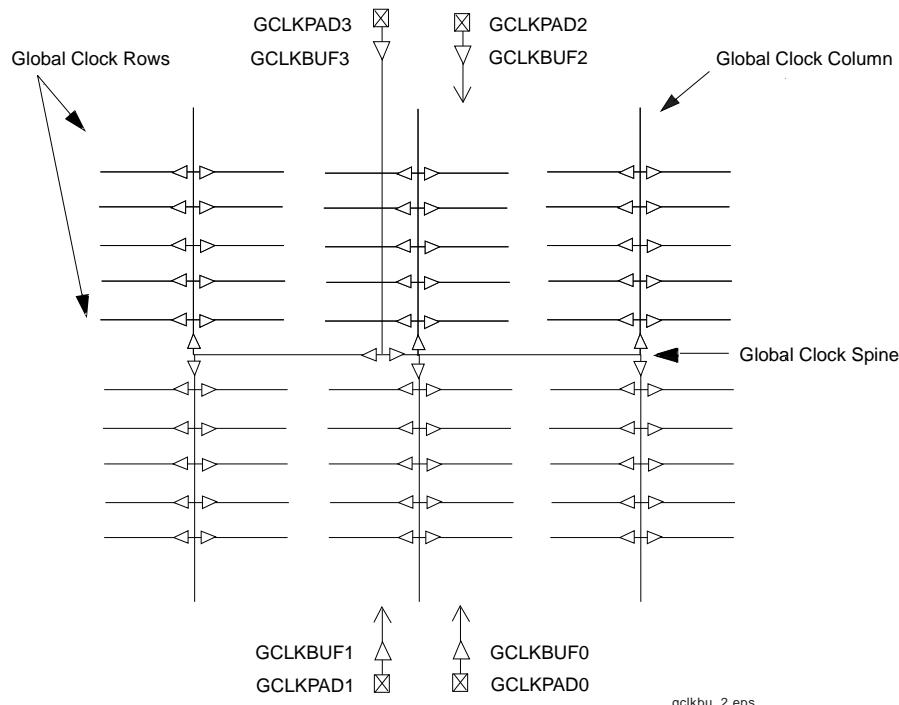
Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew

between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.+

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.



**Figure 9: Global Clock Distribution Network**

## Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

**Table 7** lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins. This technique partially compensates for the absence of INTEST support.

**Table 7: Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan in-test operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Tri-states output pins while enabling the Bypass Register
BUS_RST	01011	Reset the Configuration Bus
JSTART	01100	Clock the startup sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

For details on boundary scan, refer to the Application Note *Boundary Scan in XC4000 Devices* on the Xilinx web site.

## Development System

Virtex FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Virtex design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Leonardo)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The "soft macro" portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others may be re-used as general purpose inputs and outputs once configuration is complete.

The dedicated pins are the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the configuration mode chosen, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

For a more detailed description than that given below, see the Supplementary Description on Configuration and Readback.

## Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select these configuration modes. The selection codes are listed in [Table 8](#). Note that unlisted selection codes are reserved.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

**Table 8: Configuration Codes**

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D <sub>out</sub>
Master-serial mode	0	0	0	Out	1	Yes
Boundary-scan mode	1	0	1	N/A	1	No
SelectMAP mode	1	1	0	In	8	No
Slave-serial mode	1	1	1	In	1	Yes

### Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The capture of DIN on the rising edge of CCLK differs from previous families, but will not cause a problem for mixed

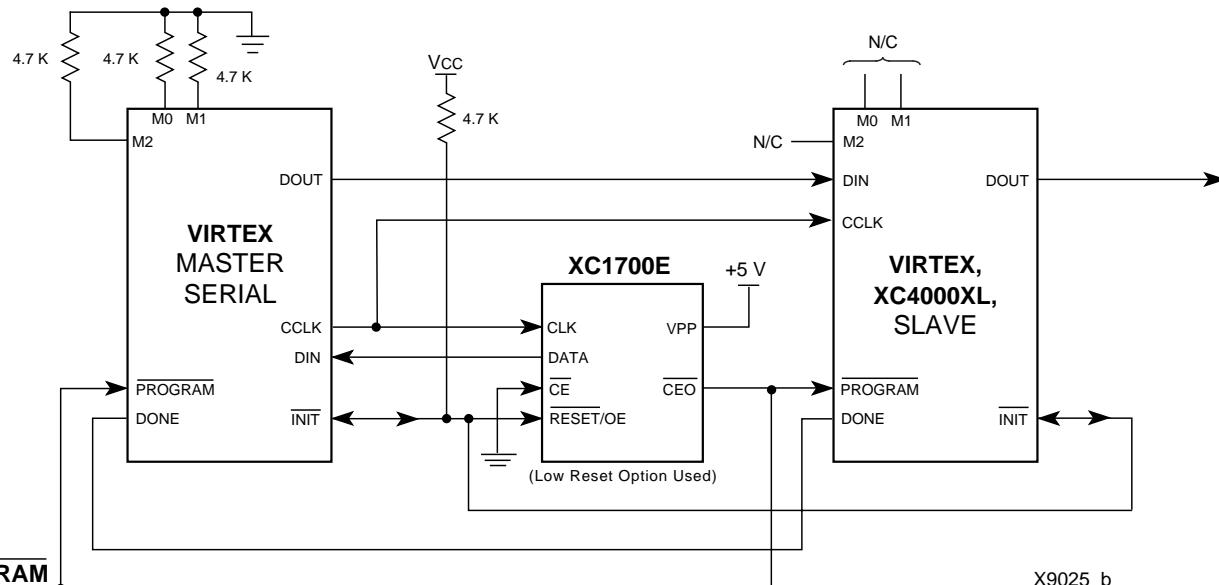
configuration chains. This change was made to improve serial-configuration rates for Virtex only chains.

[Figure 10](#) shows a full master/slave system. A Virtex device in slave serial mode should be connected as shown in the third device from the left

Slave-serial mode is selected by applying <111> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. [Figure 11](#) shows slave-serial configuration timing.

[Table 9](#) provides more detail about the characteristics shown in [Figure 11](#). Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

**NOTE:**  
M2, M1, M0 can be shorted  
to Ground if not used as I/O



**Figure 10: Master/Slave Serial Mode Circuit Diagram**

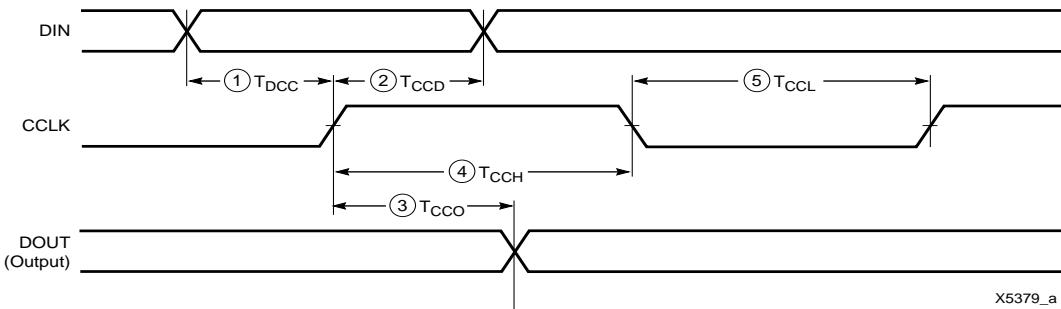


Figure 11: Slave Serial Mode Programming Switch

Table 9: Slave Serial Mode Programming Switching

	Description	Symbol		Units
CCLK	DIN setup/hold	1/2	T <sub>DCC</sub> /T <sub>CCD</sub>	2.0/0.0 ns, min
	DOUT	3	T <sub>CCO</sub>	9.0 ns, max
	High time	4	T <sub>CCH</sub>	5.0 ns, min
	Low time	5	T <sub>CCL</sub>	5.0 ns, min
	Maximum Frequency	F <sub>cc</sub>		MHz, max

### Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The preamble is also forwarded to other devices in the daisy-chain.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. When selecting a CCLK

frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support this rate.

Figure 10 shows a full master/slave system. In this system, the leftmost device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and CE input is driven by DONE. There is, therefore, the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 12.

Figure 13 shows the timing of master-serial configuration. Master serial mode is selected by a <000> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 13

At power-up, V<sub>cc</sub> must rise from 2.0 V to V<sub>cc</sub> min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until V<sub>cc</sub> is valid.

Table 10: Master Serial Mode Programming Switching

	Description	Symbol		Units
CCLK	DIN setup/hold	1/2	T <sub>DSCK</sub> /T <sub>SCKD</sub>	2.0/0.0 ns, min

Note: Master serial mode timing is based on testing in slave mode.

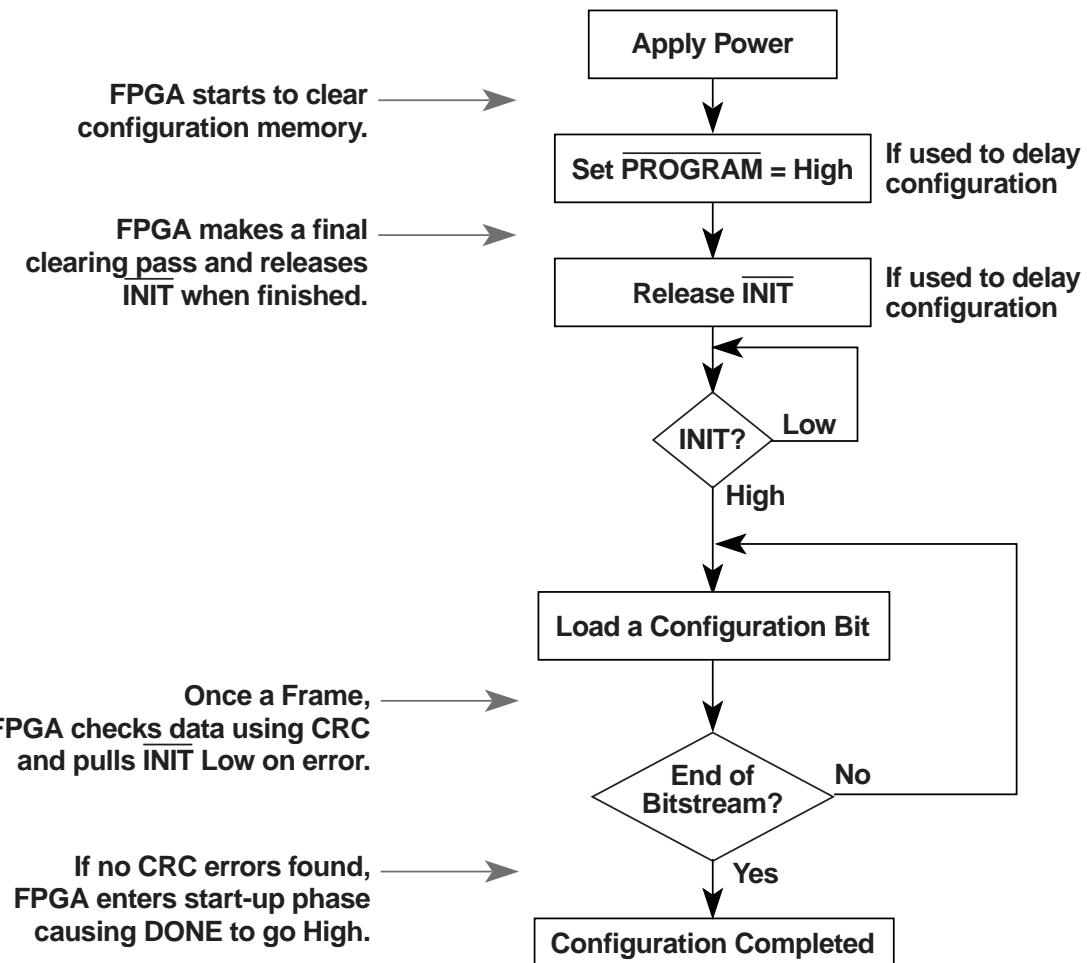
### SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-serial data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ( $\bar{CS}$ ) signal and a Write signal ( $\bar{WRITE}$ ). If

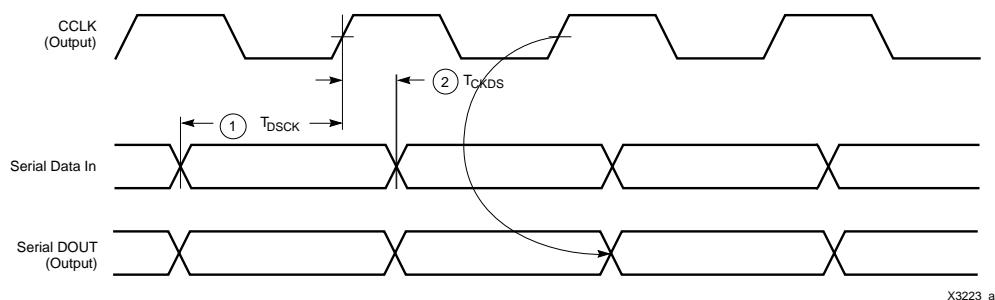
BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If  $\bar{WRITE}$  is not asserted, configuration data is read out of the FPGA as part of a readback operation.



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Figure 12: Serial Configuration Flowchart



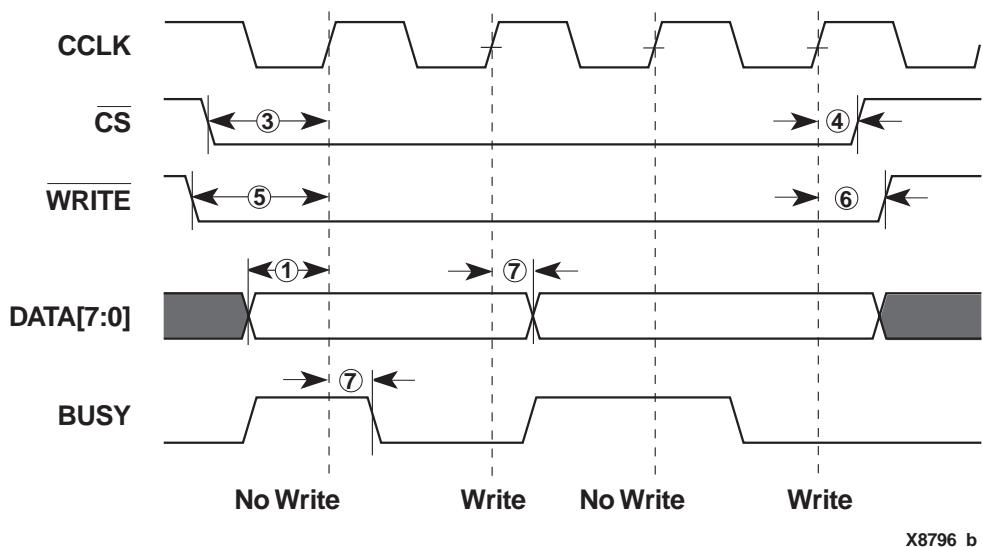
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Figure 13: Master Serial Mode Programming Switching Characteristics

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data.



**Figure 14: SelectMAP Write Waveforms**

### Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 14.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or deasserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and

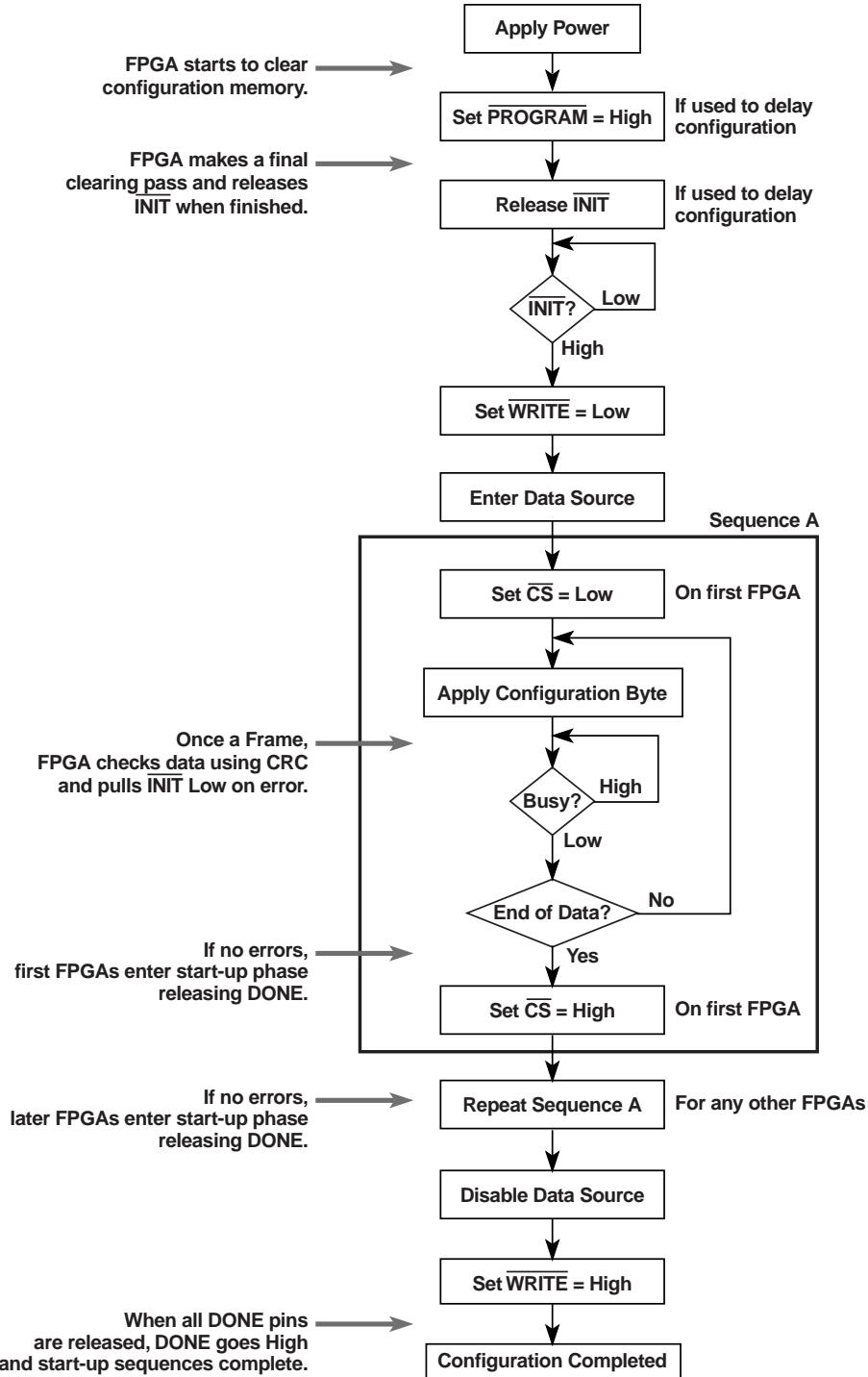
WRITE is High. Similarly, while WRITE is High, no more than one CS should be asserted.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High from a previous write, the data is not be accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. Deassert CS and WRITE.

A flowchart for the write operation appears in Figure 14. Note that if CCLK is slower than  $f_{CCNH}$ , the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

**Table 11: SelectMAP Write Timing Characteristics**

	Description		Symbol		Units
CCLK	D <sub>0-7</sub> Setup/Hold	1/2	$T_{SMDCC}/T_{SMCCD}$	2.0/0.0	ns, min
	CS Setup/Hold	34	$T_{SMCSCC}/T_{SMCCCS}$	2.0/0.0	ns, min
	WRITE Setup/Hold	5/6	$T_{SMCCW}/T_{SMWCC}$	2.0/0.0	ns, min
	BUSY Propagation Delay	7	$T_{SMCKBY}$	9.0	ns, max
	Maximum Frequency with no handshake		$f_{CCNH}$	50	MHz, max



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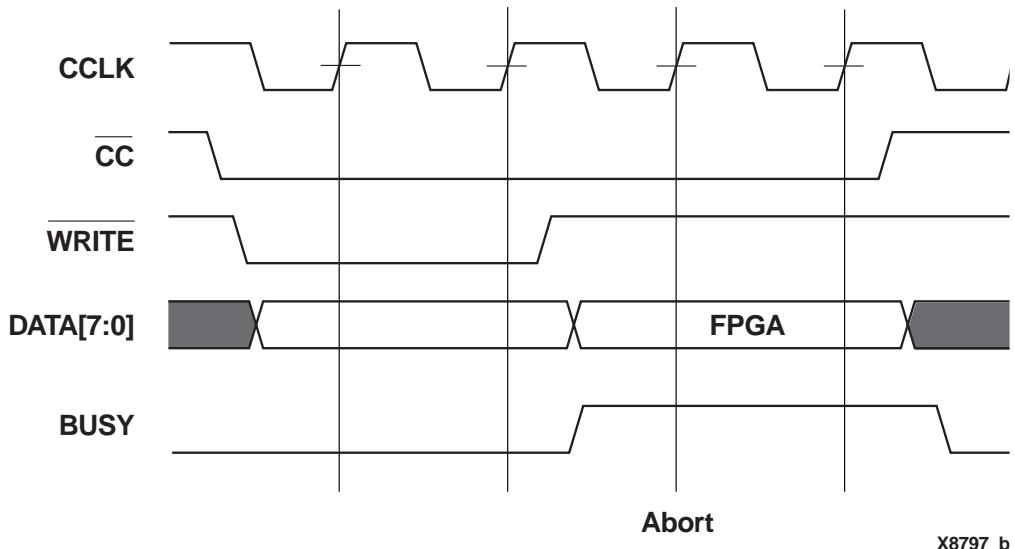
Figure 14: SelectMAP Flowchart for Write Operation

## Abort

During a given assertion of CS, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word bound-

aries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, deassert WRITE. At the rising edge of CCLK, an abort is initiated, as shown in [Figure 15](#).



**Figure 15:** SelectMAP Write Abort Waveforms

## Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG\_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

6. Load the CFG\_IN instruction into the boundary-scan instruction register (IR)
7. Enter the Shift-DR (SDR) state
8. Shift a standard configuration bitstream into TDI
9. Return to Run-Test-Idle (RTI)
10. Load the JSTART instruction into IR
11. Enter the SDR state
12. Clock TCK for the length of the sequence (the length is programmable)
13. Return to RTI

As noted above, configuration and readback is always available. The boundary-scan mode simply locks out the

other modes. The boundary-scan mode is selected by a <101> on the mode pins (M2, M1, M0).

## Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process may also be initiated by asserting PROGRAM. The end of the memory-clearing phase is signalled by INIT going High, and the completion of the entire process is signalled by asserting DONE.

## Delaying Configuration

Configuration of the FPGA can be delayed by holding the PROGRAM pin Low until the system is ready for the device to configure. During the memory clearance phase, the configuration sequences continuously cycles through the configuration memory clearing all addresses. This activity continues until the completion of one full address cycle after the PROGRAM pin goes High. Thus, configuration is delayed by extending the memory clearance phase.

Alternatively, **INIT** can be held Low using an open-drain driver. An open-drain is required since **INIT** is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to act as if the configuration memory is still being cleared. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

### **Start-Up Sequence**

The default Start-up sequence is that one CCLK cycle after **DONE** goes High, the global tri-state signal (**GTS**) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (**GSR**) and Global Write Enable (**GWE**) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events may be changed. In addition, the **GTS**, **GSR**, and **GWE** events may be made dependent on the **DONE** pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence may also be paused at any stage until DLL lock has been achieved.

### **Data Stream Format**

Virtex devices are configured by sequentially loading frames of data that have been concatenated into a bitstream. **Table 12** lists the total number of bits required to configure each device.

**Table 12: Virtex Bit-stream Lengths**

Device	# of Configuration Bits
XCV50	559,232
XCV100	781,248
XCV150	1,041,128
XCV200	1,335,872
XCV300	1,751,840
XCV400	2,546,080
XCV600	3,608,000
XCV800	4,715,584
XCV1000	6,127,772

### **Readback**

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For a detailed description, see the Supplementary Description on Configuration and Readback.

## Pin Definitions

Table 13: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode are pins used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectRAM and slave-serial modes, and output in master-serial mode
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Output	Indicates that configuration loading is complete, and that the start-up sequence is in progress.
INIT	No	Bidir (open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input	In SelectMAP mode, D0-7 are configuration data input pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, Cathode: DXN)
V <sub>CCINT</sub>	Yes	Input	Power-supply pins for the internal core logic.
V <sub>CCO</sub>	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V <sub>REF</sub>	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

## Virtex DC Characteristics

### Definition of Terms

Data sheets may be designated as Advance or Preliminary. The status of specifications in these data sheets is as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed information, see the appropriate family supplements available on the Xilinx WEBLINX at <http://www.xilinx.com>.

All specifications are subject to change without notice.

### Virtex Absolute Maximum Ratings

Symbol	Description			Units
$V_{CCINT}$	Supply voltage relative to GND		-0.5 to 3.0	V
$V_{CCO}$	Supply voltage relative to GND		-0.5 to 4.0	V
$V_{REF}$	Input Reference Voltage		-0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND, differential inputs		-0.5 to 3.6	V
$V_{IN}$	Input voltage relative to GND, other pins		-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output		-0.5 to 5.5	V
$V_{CC}$	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
$T_{STG}$	Storage temperature (ambient)		-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
$T_J$	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Virtex Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CCINT}$	Supply voltage relative to GND, $T_J = 0$ °C to +85°C	Commercial	2.5 - 5%	2.5 + 5%	V
	Supply voltage relative to GND, $T_J = -40$ °C to +100°C	Industrial	2.5 - 5%	2.5 + 5%	V
$V_{CCO}$	Supply voltage relative to GND, $T_J = 0$ °C to +85°C	Commercial		3.6	V
	Supply voltage relative to GND, $T_J = -40$ °C to +100°C	Industrial		3.6	V
$T_{IN}$	Input signal transition time			250	ns

Notes: Correct operation is guaranteed with a minimum  $V_{CCINT}$  of 2.25 V (Nominal  $V_{CCINT}$  -10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50-mV reduction in  $V_{CCINT}$  below the specified range. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C. Input and output measurement threshold is ~50% of  $V_{CC}$ .

## Virtex DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Max	Units
$V_{DRINT}$	Data Retention $V_{CCINT}$ Voltage (below which configuration data may be lost)	2.0		V
$V_{DRIQ}$	Data Retention $V_{CCO}$ Voltage (below which configuration data may be lost)	1.2		V
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current (Note 1)			mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current (Note 1)			mA
$I_{REF}$	$V_{REF}$ current per $V_{REF}$ pin		20	$\mu A$
$I_L$	Input or output leakage current	-10	+10	$\mu A$
$C_{IN}$	Input capacitance (sample tested)	BGA, PQ, HQ, packages	8	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)	Note 2	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)	Note 2	0.15	mA

Note 1: With no output current loads, no active input pull-up resistors, all I/O pins Tri-stated and floating.

Note 2: Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

## Virtex DC Input and Output levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $V_{OL}$  and  $V_{OH}$  are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum  $V_{CCO}$  with the respective  $I_{OL}$  and  $I_{OH}$  currents shown. Other standards are sample tested.

Input/Output Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	$V$ , min	$V$ , max	$V$ , min	$V$ , max	$V$ , Max	$V$ , Min	mA	mA
LVTTL (Note 1)	0.0	0.8	2.0	5.5	0.4	2.4	24	- 24
LVCMOS2	0.0	44% $V_{CCINT}$	60% $V_{CCINT}$	5.5	10% $V_{CCO}$	90% $V_{CCO}$	1.5	- 0.5
PCI, 3.3 V	- 0.5	44% $V_{CCINT}$	60% $V_{CCINT}$	$V_{CCO} + 0.5$	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2
PCI, 5.0 V	- 0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	0.0	$V_{REF} - 0.5$	$V_{REF} + 0.5$	3.6	0.4	n/a	40	n/a
GTL+	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	0.6	n/a	36	n/a
HSTL I	0.0	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	- 8
HSTL III	0.0	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	- 8
HSTL IV	0.0	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	- 8
SSTL3 I	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	- 8
SSTL3 II	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	- 16
SSTL2 I	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.45$	$V_{REF} + 0.45$	6	- 6
SSTL2 II	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	12	- 12
CTT	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.4$	$V_{REF} + 0.4$	8	- 8
AGP	0.0	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	10% $V_{CCO}$	90% $V_{CCO}$	Note 2	Note 2

Note1:  $V_{OL}$  and  $V_{OH}$  for lower drive currents are sample tested.

Note 2: Tested according to the relevant specifications.

## Virtex Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and expressed in nanoseconds unless otherwise noted.

### Virtex IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, these delays typically vary by less than 0.1 ns. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
<b>Propagation Delays</b>					
Pad to I output, no delay	$T_{IOPI}$	0.8	0.9	1.0	ns, max
Pad to I output, with delay	$T_{IOPID}$	1.4	1.6	1.8	ns, max
Pad to output IQ via transparent latch, no delay	$T_{IOPLI}$	1.7	1.9	2.2	ns, max
Pad to output IQ via transparent latch, with delay	$T_{IOPLID}$	3.3	3.8	4.4	ns, max
<b>Sequential Delays</b>					
Clock CLK to output IQ	$T_{ILOCKIQ}$	1.1	1.2	1.4	ns, max
<b>Setup and Hold Times with respect to Clock CLK</b>					
Pad, no delay	$T_{IOPICK}/T_{IOICKP}$	1.9/0.0	2.2/0.0	2.5/0.0	ns, min
Pad, with delay (Note 1)	$T_{IOPICKD}/T_{IOICKPD}$	3.5/<0	4.1/<0	4.7/<0	ns, min
ICE input	$T_{IOICECK}/T_{ILOCKICE}$	0.8/0.0	0.9/0.0	1.0/0.0	ns, min
SR input (IFF, synchronous)	$T_{IOSRCK}/T_{ILOCKISR}$	0.8/0.0	1.0/0.0	1.1/0.0	ns, min
<b>Set/Reset Delays</b>					
SR input to IQ (asynchronous)	$T_{IOSRIQ}$	1.2	1.4	1.6	ns, max
<b>Global Set/Reset</b>					
GSR to output IQ	$T_{GSRQ}$				ns, max

Note 1: With delay, the IOB hold time is negative. This reduces or eliminates pad-to-pad hold time.

## Virtex IOB Output Switching Characteristics

Output delays terminating at the pad are specified for LVTTL levels with 12 mA drive and slow slew rate (the default output standard). For other standards, these delays should be increased by the values shown.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
<b>Propagation Delays</b>					
O input to Pad	$T_{IOOP}$	4.1	5.3	6.1	ns, max
O input to Pad via transparent latch	$T_{IOOLP}$	4.3	5.5	6.4	ns, max
<b>3-State Delays</b>					
T input to Pad high-impedance	$T_{IOTHZ}$	1.1	1.3	1.5	ns, max
T input to valid data on Pad	$T_{IOTON}$	5.0	5.8	6.6	ns, max
T input to Pad high-impedance via transparent latch	$T_{IOTLPHZ}$	1.7	1.9	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	5.0	5.8	6.6	ns, max
<b>Sequential Delays</b>					
Clock CLK to Pad	$T_{IOCKP}$	5.8	6.7	7.7	ns, max
Clock CLK to Pad high-impedance (synchronous)	$T_{IOCKHZ}$	2.1	2.4	2.8	ns, max
Clock CLK to valid data on Pad (synchronous)	$T_{IOCKON}$	5.8	6.7	7.7	ns, max
<b>Setup Times before Clock CLK</b>					
O input	$T_{IOOCK}$	0.5	0.5	0.6	ns, min
OCE input	$T_{IOOCECK}$	0.8	0.9	1.0	ns, min
SR input (OFF)	$T_{IOSRCKO}$	0.8	1.0	1.1	ns, min
<b>3-State SetupTimes</b>					
TCE input	$T_{IOTCECK}$	0.8	0.9	1.0	ns, min
T input	$T_{IOTCK}$	0.2	0.2	0.3	ns, min
SR input (TFF)	$T_{IOSRCKT}$	0.8	1.0	1.1	ns, min
<b>Hold Times after Clock CLK</b>					
All Hold Times		0.0	0.0	0.0	ns, min
<b>Set/Reset Delays</b>					
SR input to Pad (asynchronous)	$T_{IOSRP}$	5.0	5.8	6.6	ns, max
SR input to Pad high-impedance (asynchronous)	$T_{IOSRHZ}$	2.3	2.6	3.0	ns, max
SR input to valid data on Pad (asynchronous)	$T_{IOSRON}$	6.0	6.8	7.9	ns, max
<b>Global Set/Reset</b>					
GSR to Pad	$T_{GSRQ}$				ns, max
<b>Global 3-State</b>					
GTS to Pad high impedance	$T_{GTS}$	5.0	5.8	6.7	ns, max
<b>Output Delay Adjustments</b>					
Standard-specific increments for delays terminating at pads	LVTTL, Slow,2 mA	13.3	15.2	17.5	ns
	4 mA	5.8	6.6	7.6	ns
	6 mA	3.0	3.5	4.0	ns
	8 mA	1.2	1.4	1.6	ns
	12 mA	0.0	0.0	0.0	ns
	24 mA	- 0.6	- 0.7	- 0.8	ns
	LVTTL, Fast,2 mA	11.5	13.3	15.3	ns
	4 mA	3.5	4.1	4.7	ns
	6 mA	1.3	1.5	1.7	ns
	8 mA	- 0.9	- 1.0	- 1.2	ns
	12 mA	- 1.9	- 2.2	- 2.5	ns
	24 mA	- 2.3	- 2.6	- 3.0	ns
	LVCMOS2	- 2.0	- 2.3	- 2.7	ns
	PCI, 33 MHz, 3.3 V	0.3	0.4	0.4	ns
	PCI, 33 MHz, 5.0 V	- 0.9	- 1.1	- 1.2	ns
	PCI, 66 MHz, 3.3 V	- 2.7	- 3.1	- 3.6	ns
	GTL	- 2.6	- 3.0	- 3.5	ns
	GTL+	- 1.9	- 2.2	- 2.5	ns
	HSTL I	- 2.8	- 3.2	- 3.7	ns
	HSTL III	- 2.8	- 3.3	- 3.7	ns
	HSTL IV	- 3.0	- 3.4	- 3.9	ns
	SSTL3 I	- 2.5	- 2.8	- 3.3	ns
	SSTL3 II	- 3.0	- 3.4	- 3.9	ns
	SSTL2 I	- 2.4	- 2.7	- 3.2	ns
	SSTL2 II	- 2.8	- 3.2	- 3.7	ns
	CTT	- 2.5	- 2.9	- 3.4	ns
	AGP	- 2.8	- 3.3	- 3.8	ns

## Virtex CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
<b>Combinatorial Delays</b>					
4-input function: F/G inputs to X/Y outputs	$T_{ILO}$	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	$T_{IF5}$	1.0	1.1	1.2	ns, max
5-input function: F/G inputs to X output	$T_{IF5X}$	1.0	1.2	1.3	ns, max
6-input function: F/G inputs to Y output via F6 MUX	$T_{IF6Y}$	1.2	1.4	1.6	ns, max
6-input function: F5IN input to Y output	$T_{F5INY}$	0.4	0.5	0.6	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	$T_{IFNCTL}$	0.4	0.5	0.6	ns, max
BY input to YB output	$T_{BYYB}$	0.5	0.6	0.7	ns, max
<b>Sequential Delays</b>					
FF Clock CLK to XQ/YQ outputs	$T_{CKO}$	1.1	1.3	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	$T_{CKLO}$	0.7	0.7	0.9	ns, max
<b>Setup Times before Clock CLK</b>					
4-input function: F/G Inputs	$T_{ICK}$	1.0	1.1	1.2	ns, min
5-input function: F/G inputs	$T_{IF5CK}$	1.4	1.6	1.8	ns, min
6-input function: F5IN input	$T_{F5INCK}$	0.8	0.9	1.0	ns, min
6-input function: F/G inputs via F6 MUX	$T_{IF6CK}$	1.6	1.8	2.0	ns, min
BX/BY inputs	$T_{DICK}$	1.6	1.8	2.0	ns, min
CE input	$T_{CECK}$	0.8	0.9	1.0	ns, min
SR/BY inputs (synchronous)	$T_{RCK}$	1.3	1.5	1.7	ns, min
<b>Hold Times after Clock CLK</b>					
All Hold Times		0.0	0.0	0.0	ns, min
<b>Clock CLK</b>					
Minimum Pulse Width, High	$T_{CH}$	2.0	2.3	2.6	ns, min
Minimum Pulse Width, Low	$T_{CL}$	2.0	2.3	2.6	ns, min
<b>Set/Reset</b>					
Minimum Pulse Width, SR/BY inputs	$T_{RPW}$	2.9	3.4	3.9	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	$T_{RQ}$	1.6	1.9	2.2	ns, max
<b>Global Set/Reset</b>					
Delay from GSR to XQ/YQ outputs	$T_{GSRQ}$				ns, max

## Virtex CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
<b>Combinatorial Delays</b>					
F operand inputs to X via XOR	$T_{OPX}$	0.8	0.9	1.0	ns, max
F operand input to XB output	$T_{OPXB}$	1.2	1.4	1.6	ns, max
F operand input to Y via XOR	$T_{OPY}$	1.6	1.9	2.2	ns, max
F operand input to YB output	$T_{OPYB}$	1.3	1.5	1.7	ns, max
F operand input to COUT output	$T_{OPCYF}$	1.3	1.5	1.7	ns, max
G operand inputs to Y via XOR	$T_{OPGY}$	1.0	1.1	1.3	ns, max
G operand input to YB output	$T_{OPGYB}$	1.4	1.6	1.9	ns, max
G operand input to COUT output	$T_{OPCYG}$	1.4	1.6	1.8	ns, max
BX initialization input to COUT	$T_{BXYC}$	0.8	0.9	1.0	ns, max
CIN input to X output via XOR	$T_{CINX}$	0.5	0.5	0.6	ns, max
CIN input to XB	$T_{CINXB}$	0.1	0.1	0.1	ns, max
CIN input to Y via XOR	$T_{CINY}$	0.5	0.6	0.7	ns, max
CIN input to YB	$T_{CINYB}$	0.2	0.2	0.2	ns, max
CIN input to COUT output	$T_{BYP}$	0.1	0.2	0.2	ns, max
<b>Multiplier Operation</b>					
F1/2 operand inputs to XB output via AND	$T_{FANDXB}$	0.4	0.5	0.6	ns, max
F1/2 operand inputs to YB output via AND	$T_{FANDYB}$	0.5	0.6	0.6	ns, max
F1/2 operand inputs to COUT output via AND	$T_{FANDCY}$	0.5	0.5	0.6	ns, max
G1/2 operand inputs to YB output via AND	$T_{GANDYB}$	0.4	0.4	0.5	ns, max
G1/2 operand inputs to COUT output via AND	$T_{GANDCY}$	0.4	0.4	0.5	ns, max
<b>Setup Times before Clock CLK</b>					
CIN input to FFX	$T_{CCKX}$	0.8/	0.9	1.1	ns, min
CIN input to FFY	$T_{CCKY}$	0.90	1.0	1.1	ns, min
Setup Time Adjustment					ns
<b>Hold Times after Clock CLK</b>					
All Hold Times		0.0	0.0	0.0	ns, min

## Virtex CLB SelectRAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-6	-5	-4	
<b>Sequential Delays</b>					
Clock CLK to X/Y outputs (WE active)					ns, max
<b>Shift-Register Mode</b>					
Clock CLK to X/Y outputs	$T_{SHCKO}$				ns, max
<b>Setup Times before Clock CLK</b>					
F/G address inputs	$T_{AS/T_{AH}}$	0.6	0.7	0.8	ns, min
BX/BY data inputs (DIN)	$T_{DS/T_{DH}}$	1.0	1.2	1.3	ns, min
CE input (WE)	$T_{WS/T_{WH}}$	0.6	0.6	0.7	ns, min
<b>Shift-Register Mode</b>					
BX/BY data inputs (DIN)	$T_{SHDICK}$				ns, min
CE input (WS)	$T_{SHCECK}$				ns, min
<b>Hold Times after Clock CLK</b>					
All Hold Times		0.0	0.0	0.0	ns, min
<b>Clock CLK</b>					
Minimum Pulse Width, High	$T_{WPH}$	2.9	3.4	3.9	ns, min
Minimum Pulse Width, Low	$T_{WPL}$	2.9	3.4	3.9	ns, min
Minimum clock period to meet address write cycle time	$T_{WC}$	5.8	6.7	7.7	ns, min

## Virtex BLOCKRAM Switching Characteristics

Description		Symbol	Speed Grade			Units
			-6	-5	-4	
<b>Sequential Delays</b>						
Clock CLK to DOUT output		T <sub>BCKO</sub>	3.3	3.8	4.4	ns, max
<b>Setup Times before Clock CLK</b>						
ADDR inputs		T <sub>BACK</sub>	1.2	1.4	1.6	ns, min
DIN inputs		T <sub>BDCK</sub>	1.2	1.4	1.6	ns, min
EN input		T <sub>BECK</sub>	2.7	3.1	3.6	ns, min
RST input		T <sub>BRCK</sub>	2.5	2.9	3.3	ns, min
WEN input		T <sub>BWCK</sub>	2.4	2.8/	3.2	ns, min
<b>Hold Times after Clock CLK</b>						
All Hold Times			0.0	0.0	0.0	ns, min
<b>Clock CLK</b>						
Minimum Pulse Width, High		T <sub>BPWH</sub>	2.0	2.3	2.6	ns, min
Minimum Pulse Width, Low		T <sub>BPWL</sub>	2.0	2.3	2.6	ns, min
CLKA -> CLKB setup time for different ports		T <sub>BCCS</sub>				ns, max ns, min

## Virtex Clock Distribution Switching Characteristics

Description		Symbol	Speed Grade			Units
			-6	-5	-4	
<b>GCLK IOB and Buffer</b>						
Global Clock PAD to output. IN input to OUT output		T <sub>GPID</sub> T <sub>GIO</sub>	1.0 0.9	1.1 1.0	1.3 1.2	ns, max ns, max

## Virtex TBUF Switching Characteristics

Description		Symbol	Speed Grade			Units
			-6	-5	-4	
<b>Combinatorial Delays</b>						
IN input to OUT output TRI input to OUT output high-impedance Tri input to valid data on OUT output		T <sub>IO</sub> T <sub>OFF</sub> T <sub>ON</sub>	0.2 0.2 0.2	0.2 0.2 0.2	0.2 0.2 0.2	ns, max ns, max ns, max

## Virtex Clock Distribution Guidelines

The following clock-distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Description		Symbol	Speed Grade			Units
			-6	-5	-4	
<b>GCLK Distribution</b>						
From GCLK pad to any flip-flop	XCV50 XCV100 XCV150 XCV200 XCV300 XCV400 XCV600 XCV800 XCV1000					ns, max ns, max ns, max ns, max ns, max ns, max ns, max ns, max ns, max

## Virtex Pin Outs

### Pin-Out Tables

For full pin-out listings of Virtex devices, see the separate publication Virtex FPGA Family Pin Outs. For convenience, [Table 14](#) and [Table 15](#) list the locations of special-purpose and power-supply pins. Pins not listed are user I/Os.

**Table 14: Virtex Pin-out Tables (Non-BGA)**

Pin Name	Device	PQ/HQ240
GCK0	All	92
GCK1	All	89
GCK2	All	210
GCK3	All	213
M0	All	60
M1	All	58
M2	All	62
CCLK	All	179
PROGRAM	All	122
DONE	All	120
INIT	All	123
BUSY/DOUT	All	178
D0/DIN	All	177
D1	All	167
D2	All	163
D3	All	156
D4	All	145
D5	All	138
D6	All	134
D7	All	124
WRITE	All	185
CS	All	184
TDI	All	183
TDO	All	181

**Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)**

Pin Name	Device	PQ/HQ240
TMS	All	2
TCK	All	239
V <sub>CCINT</sub>	All	16, 32, 43, 77, 88, 104, 137, 148, 164, 198, 214, 225
V <sub>CCO</sub>	All	15, 30, 44, 61, 76, 90, 105, 121, 136, 150, 165, 180, 197, 212, 226, 240
V <sub>REF</sub> , Bank 0	XCV50	218, 232
(V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)		XCV100/150 ... + 229
		XCV200/300 ... + 236
		XCV400 ... + 215
		XCV600 ... + 230
		XCV800 ... + 222
V <sub>REF</sub> , Bank 1	XCV50	191, 205
(V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)		XCV100/150 ... + 194
		XCV200/300 ... + 187
		XCV400 ... + 208
		XCV600 ... + 193
		XCV800 ... + 201
V <sub>REF</sub> , Bank 2	XCV50	157, 171
(V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)		XCV100/150 168
		XCV200/300 ... + 175
		XCV400 ... + 154
		XCV600 ... + 169
		XCV800 ... + 161

**Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)**

Pin Name	Device	PQ/HQ240
$V_{REF}$ , Bank 3  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	130, 144
	XCV100/150	... + 133
	XCV200/300	... + 126
	XCV400	... + 147
	XCV600	... + 132
	XCV800	... + 140
$V_{REF}$ , Bank 4  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	97, 111
	XCV100/150	... + 108
	XCV200/300	... + 115
	XCV400	... + 94
	XCV600	... + 109
	XCV800	... + 101
$V_{REF}$ , Bank 5  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	70, 84
	XCV100/150	... + 73
	XCV200/300	... + 66
	XCV400	... + 87
	XCV600	... + 72
	XCV800	... + 80
$V_{REF}$ , Bank 6  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	36, 50
	XCV100/150	... + 47
	XCV200/300	... + 54
	XCV400	... + 33
	XCV600	... + 48
	XCV800	... + 40

**Table 14: Virtex Pin-out Tables (Non-BGA) (Continued)**

Pin Name	Device	PQ/HQ240
$V_{REF}$ , Bank 7  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	9, 23
	XCV100/150	... + 12
	XCV200/300	... + 5
	XCV400	... + 26
	XCV600	... + 11
	XCV800	... + 19
GND	All	1, 8, 14, 22, 29, 37, 45, 51, 59, 69, 75, 83, 91, 98, 106, 112, 119, 129, 135, 143, 151, 158, 166, 172, 182, 190, 196, 204, 211, 219, 227, 233

**Table 15: Virtex Pin-out Tables (BGA)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
GCK0	All	Y11	AE13	AL16	AL17
GCK1	All	Y10	AF14	AK16	AJ17
GCK2	All	A10	B14	A16	D17
GCK3	All	B10	D14	D17	A17
M0	All	Y1	AD24	AH28	AJ29
M1	All	U3	AB23	AH29	AK30
M2	All	W2	AC23	AJ28	AN32
CCLK	All	B19	C3	D4	C4
PROGRAM	All	Y20	AC4	AH3	AM1
DONE	All	W19	AD3	AH4	AJ5
INIT	All	U18	AD2	AJ2	AH5
BUSY/DOUT	All	D18	E4	D3	D4
D0/DIN	All	C19	D3	C2	E4
D1	All	E20	G1	K4	K3
D2	All	G19	J3	K2	L4
D3	All	J19	M3	P4	P3
D4	All	M19	R3	V4	W4
D5	All	P19	U4	AB1	AB5
D6	All	T20	V3	AB3	AC4
D7	All	V19	AC3	AG4	AJ4
WRITE	All	A19	D5	B4	D6
CS	All	B18	C4	D5	A2
TDI	All	C17	B3	B3	D5
TDO	All	A20	D4	C4	E6
TMS	All	D3	D23	D29	B33
TCK	All	A1	C24	D28	E29
DXN	All	W3	AD23	AH27	AK29
DXP	All	V4	AE24	AK29	AJ28

**Table 15: Virtex Pin-out Tables (BGA) (Continued)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
$V_{CCINT}$  ( $V_{CCINT}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50/100/150/200	C10, D6, D15, F4, F17, L3, L18, R4, R17, U6, U15, V10	A20, C14, D10, J24, K4, P2, P25, V24, W2, AC10, AE14, AE19		
	XCV300		... + B16, D12, L1, L25, R23, T1, AF11, AF16	A10, A17, B23, C14, C19, K3, K29, N2, N29, T1, T29, W2, W31, AB2, AB30, AJ10, AJ16, AK13, AK19, AK22	
	XCV400/600			... + B26, C7, F1, F30, AE29, AF1, AH8, AH24	A21, B14, B18, B28, C24, E9, E12, F2, H30, J1, K32, N1, N33, U5, U30, Y2, Y31, AD2, AD32, AG3, AG31, AK8, AK11, AK17, AK20, AL14, AL27, AN25
	XCV800/1000				... + B12, C22, M3, N29, AB2, AB32, AJ13, AL22,
$V_{CCO}$ , Bank 0	All	D7, D8	A17, B25, D19	A21, C29, D21	A22, A26, A30, B19, B32
$V_{CCO}$ , Bank 1	All	D13, D14	A10, D7, D13	A1, A11, D11	A10, A16, B13, C3, E5
$V_{CCO}$ , Bank 2	All	G17, H17	B2, H4, K1	C3, L1, L4	B2, D1, H1, M1, R2

**Table 15: Virtex Pin-out Tables (BGA) (Continued)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
V <sub>CCO</sub> , Bank 3	All	N17, P17	P4, U1, Y4	AA1, AA4, AJ3	V1, AA2, AD1, AK1, AL2
V <sub>CCO</sub> , Bank 4	All	U13, U14	AC8, AE2, AF10	AH11, AL1, AL11	AM2, AM15, AN4, AN8, AN12
V <sub>CCO</sub> , Bank 5	All	U7, U8	AC14, AC20, AF17	AH21, AJ29, AL21	AL31, AM21, AN18, AN24, AN30
V <sub>CCO</sub> , Bank 6	All	N4, P4	U26, W23, AE25	AA28, AA31, AL31	W32, AB33, AF33, AK33, AM32
V <sub>CCO</sub> , Bank 7	All	G4, H4	G23, K26, N23	A31, L28, L31	C32, D33, K33, N32, T33
V <sub>REF</sub> , Bank 0  (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	A8, B4			
	XCV100/150	... + A4	A16,C19, C21		
	XCV200/300		... + D21	B19, D22, D24, D26	
	XCV400		... + B15	... + C18	A19, D20, D26, E23, E27
	XCV600			... + C24	... + E24
	XCV800			... + B21	... + E21
	XCV1000				... + D29

**Table 15: Virtex Pin-out Tables (BGA) (Continued)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
V <sub>REF</sub> , Bank 1  (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	A17, B12			
	XCV100/150	... + B15	B6, C9, C12		
	XCV200/300		... + D6	A13, B7, C6, C10	
	XCV400		... + C13	... + B15	A6, D7, D11, D16, E15
	XCV600			... + D10	... + D10
	XCV800			... + B12	... + D13
	XCV1000				... + E7
V <sub>REF</sub> , Bank 2  (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	C20, J18			
	XCV100/150	... + F19	E2, H2, M4		
	XCV200/300		... + D2	E2, G3, J2, N1	
	XCV400		... + M1	... + R3	G5, H4, L5, P4, R1
	XCV600			... + H1	... + K5
	XCV800			... + M3	... + N5
	XCV1000				... + B3
V <sub>REF</sub> , Bank 3  (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	M18, V20			
	XCV100/150	... + R19	R4, V4, Y3		
	XCV200/300		... + AC2	V2, AB4, AD4, AF3	
	XCV400		. + R1	... + U2	V4, W5, AD3, AE5, AK2
	XCV600			... + AC3	... + AF1
	XCV800			... + Y3	... + AA4
	XCV1000				... + AH4

**Table 15: Virtex Pin-out Tables (BGA) (Continued)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
$V_{REF}$ , Bank 4  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	V12, Y18			
	XCV100/150	... + W15	AC12, AE5, AE8,		
	XCV200/300		... + AE4	AJ7, AL4, AL8, AL13	
	XCV400		... + AF12	... + AK15	AL7, AL10, AL16, AM4, AM14
	XCV600			... + AK8	... + AL9
	XCV800			... + AJ12	... + AK13
	XCV1000				... + AN3
$V_{REF}$ , Bank 5  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	V9, Y3			
	XCV100/150	... + W6	AC15, AC18, AD20		
	XCV200/300		... + AE23	AJ18, AJ25, AK23, AK27	
	XCV400		... + AF15	... + AJ17	AJ18, AJ25, AL20, AL24, AL29
	XCV600			... + AL24	... + AM26
	XCV800			... + AH19	... + AN23
	XCV1000				... + AK28
$V_{REF}$ , Bank 6  ( $V_{REF}$ pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	M2, R3			
	XCV100/150	... + T1	R24, Y26, AA25,		
	XCV200/300		... + AD26	V28, AB28, AE30, AF28	
	XCV400		... + P24	... + U28	V29, Y32, AD31, AE29, AK32
	XCV600			... + AC28	... + AE31
	XCV800			... + Y30	... + AA30
	XCV1000				... + AH30

**Table 15: Virtex Pin-out Tables (BGA) (Continued)**

<b>Pin Name</b>	<b>Device</b>	<b>BG256</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>
V <sub>REF</sub> , Bank 7  (V <sub>REF</sub> pins are listed incrementally. Connect all pins listed for both the required device and all smaller devices listed in the same package.)	XCV50	G3, H1			
	XCV100/150	... + D1	D26, G26, L26		
	XCV200/300		... + E24	F28, F31, J30, N30	
	XCV400		... + M25	... + R31	E31, G31, K31, P31, T31
	XCV600			... + J28	... + H32
	XCV800			... + M28	... + L33
	XCV1000				... + D31
GND	All	C3, C18, D4, D5, D9, D10, D11, D12, D16, D17, E4, E17, J4, J9, J10, J11, J12, J17, K4, K9, K10, K11, K12, K17, L4, L9, L10, L11, L12, L17, M4, M9, M10, M11, M12, M17, T4, T17, U4, U5, U9, U10, U11, U12, U16, U17, V3, V18	A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF2, AF5, AF8, AF13, AF19, AF22, AF25, AF26	A2, A3, A7, A9, A14, A18, A23, A25, A29, A30, B1, B2, B30, B31, C1, C31, D16, G1, G31, J1, J31, P1, P31, T4, T28, V1, V31, AC1, AC31, AE1, AE31, AH16, AJ1, AJ31, AK1, AK2, AK30, AK31, AL2, AL3, AL7, AL9, AL14, AL18, AL23, AL25, AL29, AL30	A1, A7, A12, A14, A18, A20, A24, A29, A32, A33, B1, B6, B9, B15, B23, B27, B31, C2, E1, F32, G2, G33, J32, K1, L2, M33, P1, P33, R32, T1, V33, W2, Y1, Y33, AB1, AC32, AD33, AE2, AG1, AG32, AH2, AJ33, AL32, AM3, AM7, AM11, AM19, AM25, AM28, AM33, AN1, AN2, AN5, AN10, AN14, AN16, AN20, AN22, AN27, AN33
No Connect					C31, AC2, AK4, AL3

## Pin-Out Diagrams

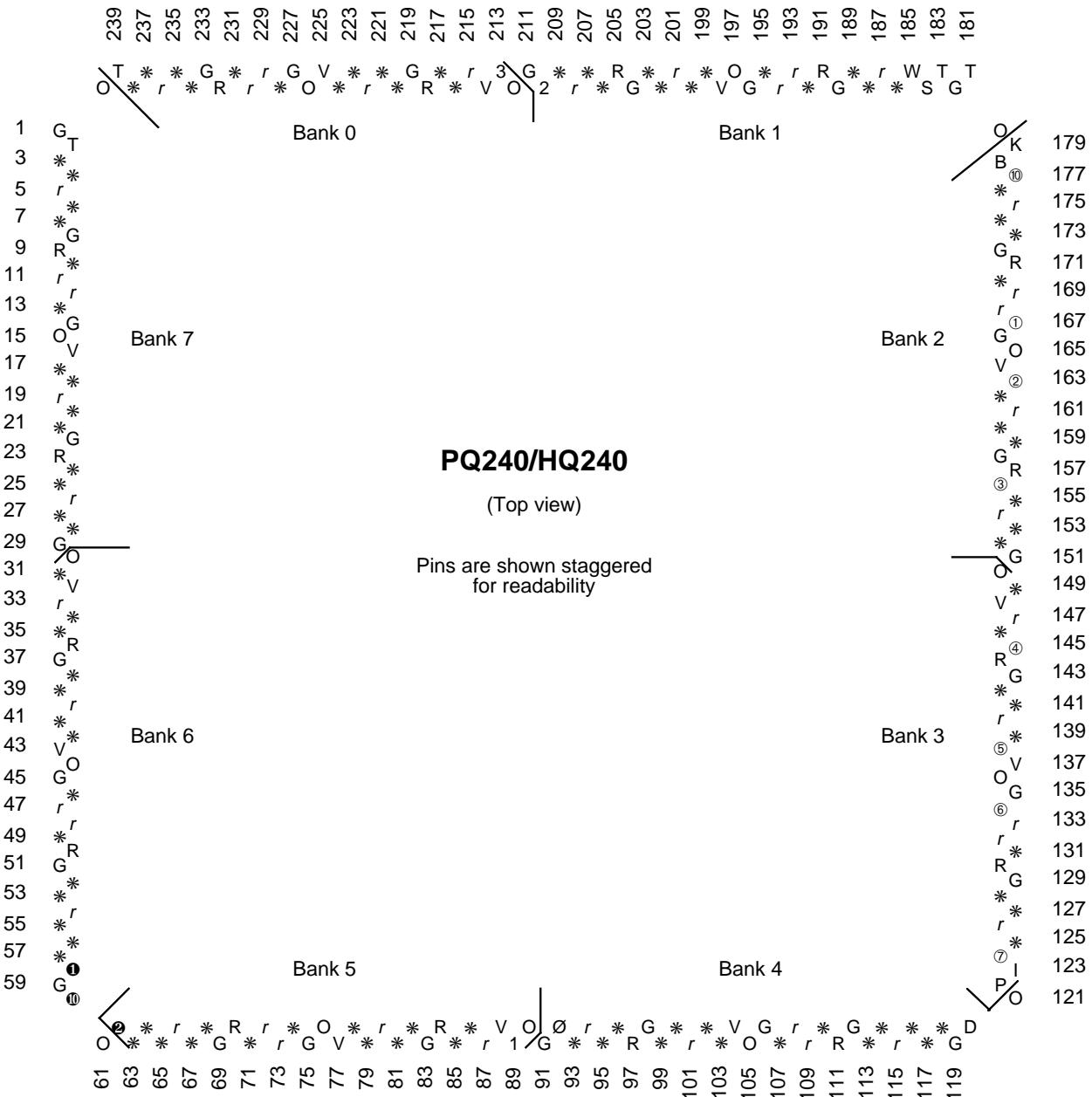
The following diagrams (see pages 39 through 44) illustrate the locations of special-purpose pins on Virtex FPGAs.

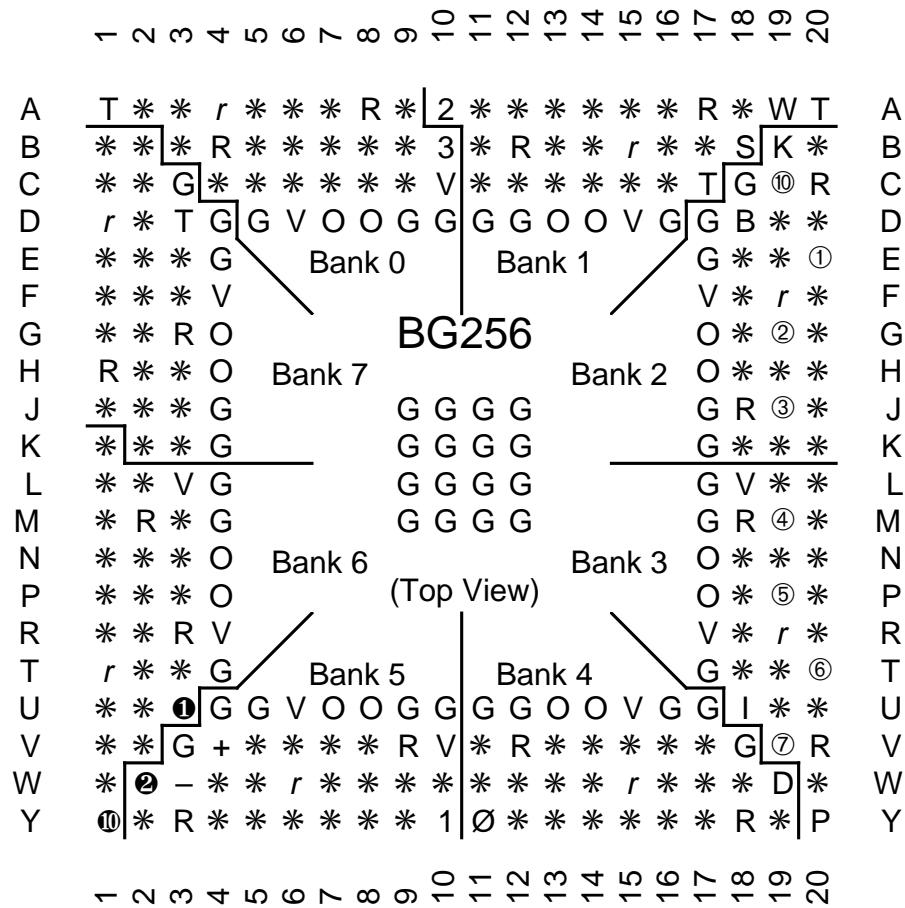
**Table 16: Pin-out Diagram Symbols**

Symbol	Pin Function
*	General I/O
V	$V_{CCINT}$
v	Device-dependent $V_{CCINT}$ , n/c on smaller devices
O	$V_{CCO}$
R	$V_{REF}$
r	Device-dependent $V_{REF}$ , remains I/O on smaller devices
G	Ground
$\emptyset, 1, 2, 3$	Global Clocks
$\textcircled{10}, \textcircled{1}, \textcircled{2}$	M0, M1, M2
$\textcircled{10}, \textcircled{1}, \textcircled{2}, \textcircled{3}, \textcircled{4}, \textcircled{5}, \textcircled{6}, \textcircled{7}$	D0/DIN, D1, D2, D3, D4, D5, D6, D7
B	DOUT/BUSY
D	DONE
P	PROGRAM
I	INIT
K	CCLK
W	WRITE
S	CS
T	Boundary-scan Test Access Port
+	Temperature diode, anode
-	Temperature diode, cathode
n	No connect

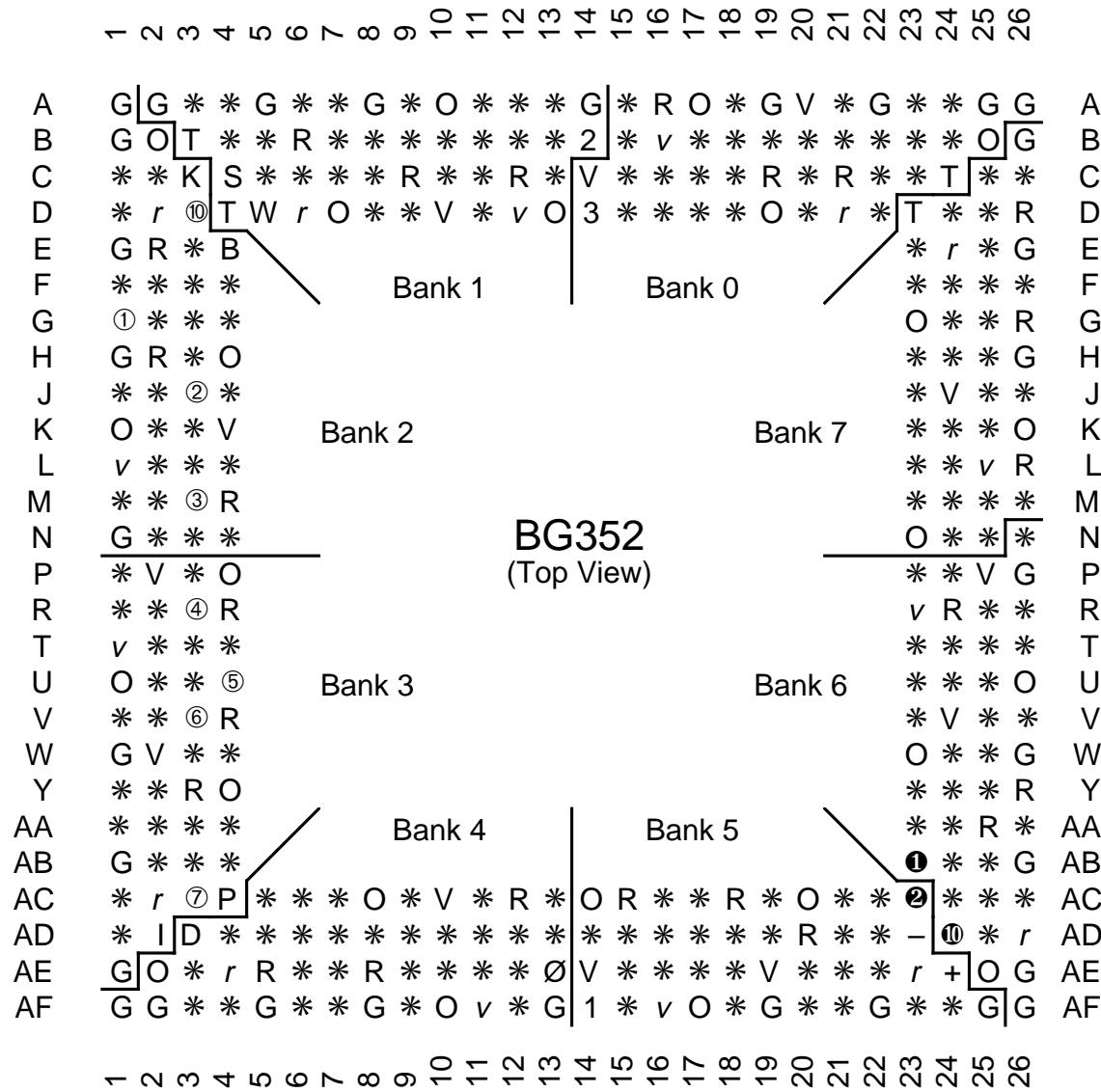
**Table 16** lists the symbols used in these diagrams. The diagrams also show I/O-bank boundaries.

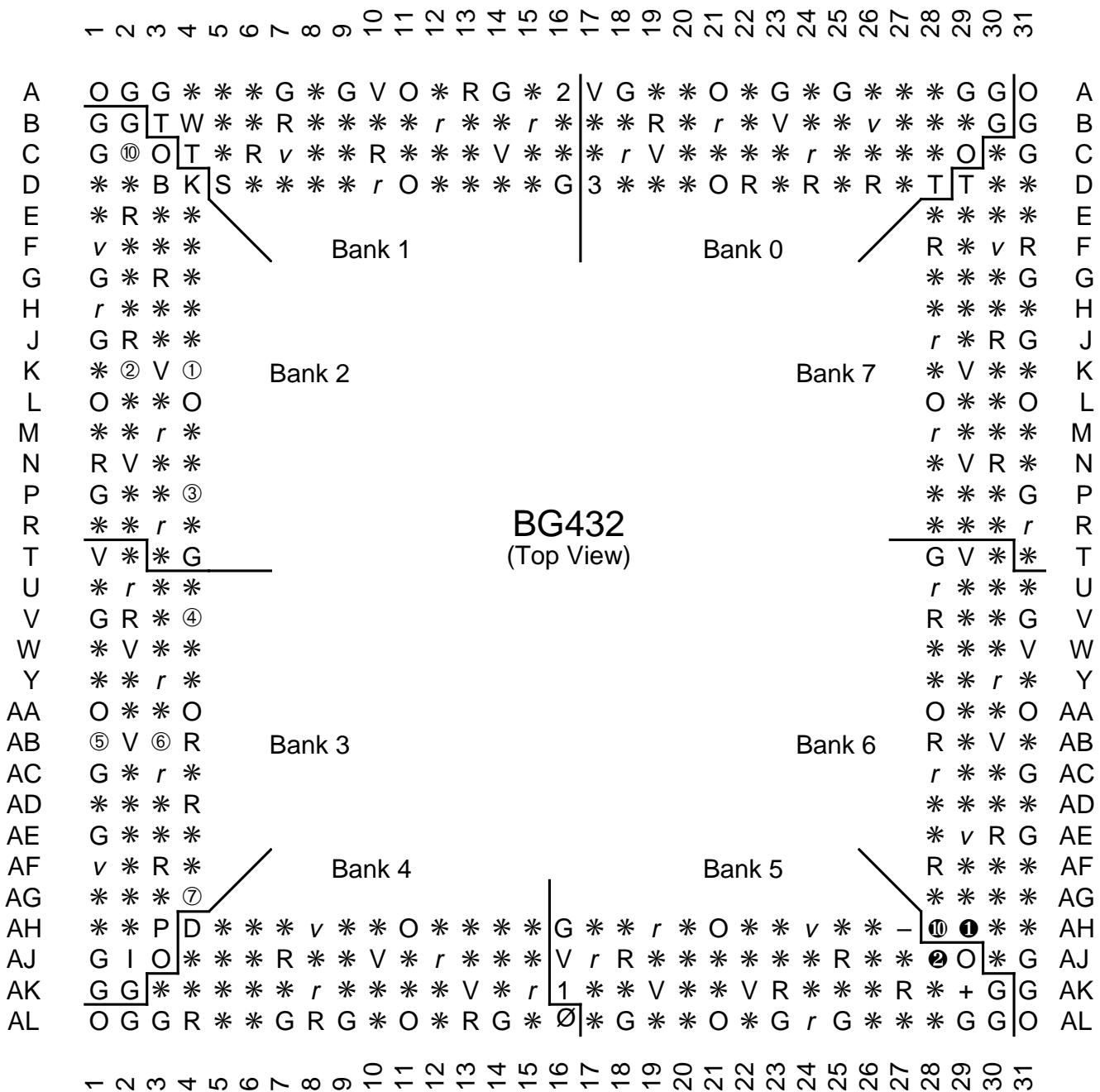
## PQ240/HQ240 Pin-out Diagram



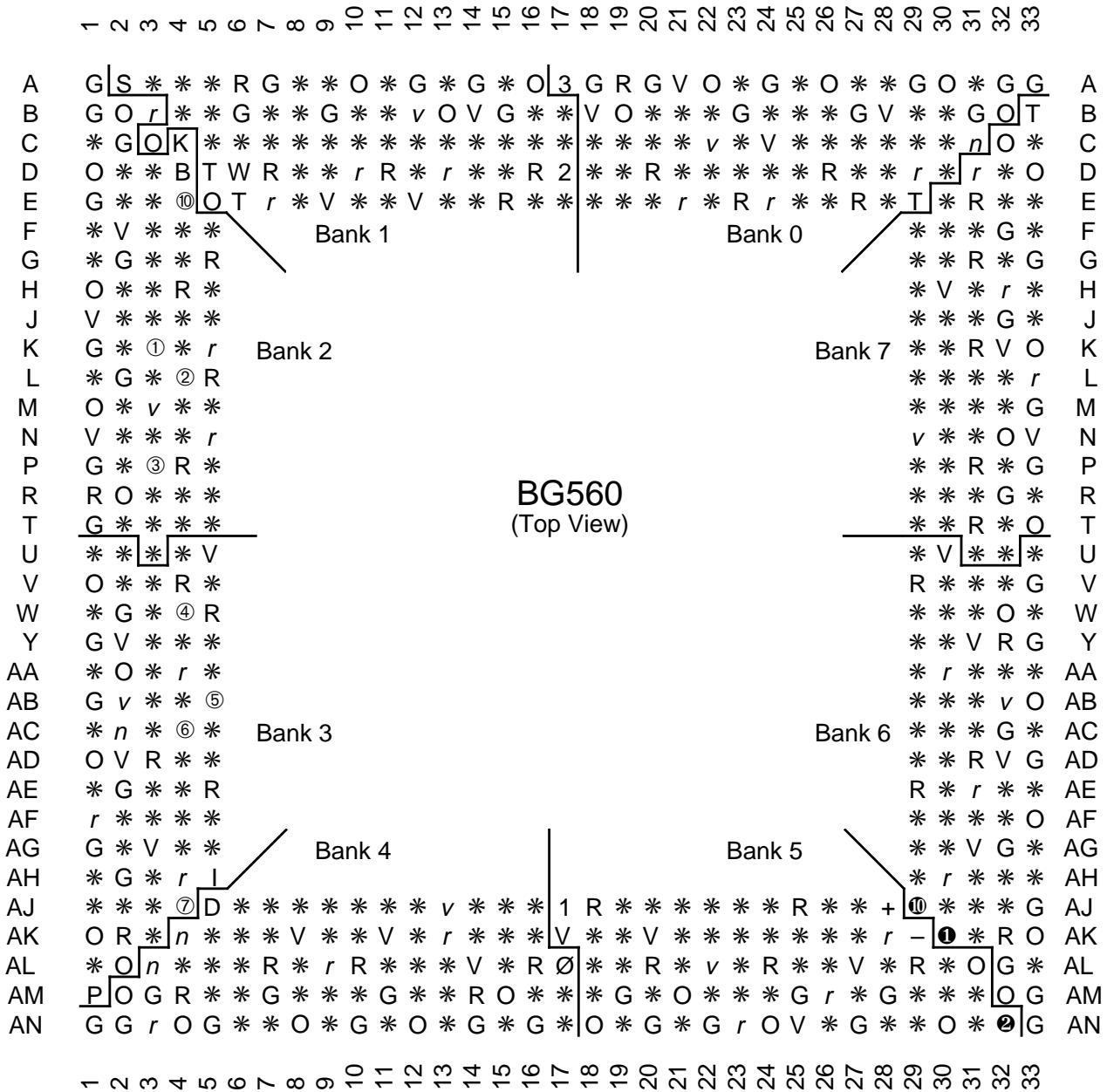
**BG226 Pin-out Diagram**

## **BG352 Pin-out Diagram**



**BG432 Pin-out Diagram**

## *BG560 Pin-out Diagram*



**XC4000E and XC4000X Series Field Programmable Gate Arrays**

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## XC4000E and XC4000X Series Features

**Note:** XC4000 Series devices described in this data sheet include the XC4000E family and XC4000X Series. XC4000X Series devices described in this data sheet include the XC4000EX and XC4000XL families. Separate data sheets are available for two other Families in the XC4000X series, the XC4000XLT and XC4000XV. This information does not apply to the older Xilinx families: XC4000, XC4000A, XC4000D, XC4000H, or XC4000L. For information on these devices, see the Xilinx WEBLINX at <http://www.xilinx.com>.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Fully PCI compliant (speed grades -2 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 80 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XC4000E output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

## Low-Voltage Versions Available

- Low-Voltage Devices Function at 3.0 - 3.6 Volts
- XC4000XL: High Performance Low-Voltage Versions of XC4000EX devices

## Additional XC4000X Series Features

- Highest Performance — 3.3 V XC4000XL
- Highest Capacity — Over 180,000 Usable Gates
- 5V tolerant I/Os on XC4000XL
- 0.35µ SRAM process for XC4000XL
- Additional Routing Over XC4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
- 12-mA Sink Current Per XC4000X Output
- Flexible New High-Speed Clock Network
  - 8 additional Early Buffers for shorter clock delays
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 4 Additional Address Bits in Master Parallel Configuration Mode
- XC4000XLT devices, optimized for PCI applications, are available.
- The XC4000XV Family offers the highest density with 0.25 micron 2.5 volt technology.

## Introduction

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

The XC4000E and XC4000X Series currently have 20 members, as shown in [Table 2](#).

**Note:** All functionality in low-voltage families is the same as in the corresponding 5-Volt family, except where numerical references are made to timing or power.

Table 2: XC4000E and XC4000X Series Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XC4002XL	152	1,600	2,048	1,000 - 3,000	8 x 8	64	256	64
XC4003E	238	3,000	3,200	2,000 - 5,000	10 x 10	100	360	80
XC4005E/XL	466	5,000	6,272	3,000 - 9,000	14 x 14	196	616	112
XC4006E	608	6,000	8,192	4,000 - 12,000	16 x 16	256	768	128
XC4008E	770	8,000	10,368	6,000 - 15,000	18 x 18	324	936	144
XC4010E/XL	950	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	160
XC4013E/XL	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192
XC4020E/XL	1862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224
XC4025E	2432	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	256
XC4028EX/XL	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256
XC4036EX/XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288
XC4044XL	3800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320
XC4052XL	4598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352
XC4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384
XC4085XL	7448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448

\* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

## Description

XC4000 Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave and peripheral modes).

XC4000 Series FPGAs are supported by powerful and sophisticated software, covering every aspect of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications.

FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lowest high-volume unit cost, a design can first be implemented in the XC4000E or XC4000X, then migrated to one of Xilinx' compatible HardWire mask-programmed devices.

## Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

## XC4000E and XC4000X Series Compared to the XC4000

For readers already familiar with the XC4000 family of Xilinx Field Programmable Gate Arrays, the major new features in the XC4000 Series devices are listed in this section. The biggest advantages of XC4000E and XC4000X devices are significantly increased system speed, greater capacity, and new architectural features, particularly Select-RAM memory. The XC4000X devices also offer many new routing features, including special high-speed clock buffers that can be used to capture input data with minimal delay.

Any XC4000E device is pinout- and bitstream-compatible with the corresponding XC4000 device. An existing XC4000 bitstream can be used to program an XC4000E device. However, since the XC4000E includes many new features, an XC4000E bitstream cannot be loaded into an XC4000 device.

XC4000X Series devices are not bitstream-compatible with equivalent array size devices in the XC4000 or XC4000E families. However, equivalent array size devices, such as the XC4025, XC4025E, XC4028EX, and XC4028XL, are pinout-compatible.

## Improvements in XC4000E and XC4000X

### Increased System Speed

XC4000E and XC4000X devices can run at synchronous system clock rates of up to 80 MHz, and internal performance can exceed 150 MHz. This increase in performance over the previous families stems from improvements in both device processing and system architecture. XC4000 Series devices use a sub-micron multi-layer metal process. In addition, many architectural improvements have been made, as described below.

The XC4000XL family is a high performance 3.3V family based on 0.35 $\mu$  SRAM technology and supports system speeds to 80 MHz.

### PCI Compliance

XC4000 Series -2 and faster speed grades are fully PCI compliant. XC4000E and XC4000X devices can be used to implement a one-chip PCI solution.

### Carry Logic

The speed of the carry logic chain has increased dramatically. Some parameters, such as the delay on the carry chain through a single CLB (TBYP), have improved by as

much as 50% from XC4000 values. See “Fast Carry Logic” on page 4-18 for more information.

### Select-RAM Memory: Edge-Triggered, Synchronous RAM Modes

The RAM in any CLB can be configured for synchronous, edge-triggered, write operation. The read operation is not affected by this change to an edge-triggered write.

### Dual-Port RAM

A separate option converts the 16x2 RAM in any CLB into a 16x1 dual-port RAM with simultaneous Read/Write.

The function generators in each CLB can be configured as either level-sensitive (asynchronous) single-port RAM, edge-triggered (synchronous) single-port RAM, edge-triggered (synchronous) dual-port RAM, or as combinatorial logic.

### Configurable RAM Content

The RAM content can now be loaded at configuration time, so that the RAM starts up with user-defined data.

### H Function Generator

In current XC4000 Series devices, the H function generator is more versatile than in the original XC4000. Its inputs can come not only from the F and G function generators but also from up to three of the four control input lines. The H function generator can thus be totally or partially independent of the other two function generators, increasing the maximum capacity of the device.

### IOB Clock Enable

The two flip-flops in each IOB have a common clock enable input, which through configuration can be activated individually for the input or output flip-flop or both. This clock enable operates exactly like the EC pin on the XC4000 CLB. This new feature makes the IOBs more versatile, and avoids the need for clock gating.

### Output Drivers

The output pull-up structure defaults to a TTL-like totem-pole. This driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc, just like the XC4000 family outputs. Alternatively, XC4000 Series devices can be globally configured with CMOS outputs, with p-channel pull-up transistors pulling to Vcc. Also, the configurable pull-up resistor in the XC4000 Series is a p-channel transistor that pulls to Vcc, whereas in the original XC4000 family it is an n-channel transistor that pulls to a voltage one transistor threshold below Vcc.

## Input Thresholds

The input thresholds of 5V devices can be globally configured for either TTL (1.2 V threshold) or CMOS (2.5 V threshold), just like XC2000 and XC3000 inputs. The two global adjustments of input threshold and output level are independent of each other. The XC4000XL family has an input threshold of 1.6V, compatible with both 3.3V CMOS and TTL levels.

## Global Signal Access to Logic

There is additional access from global clocks to the F and G function generator inputs.

## Configuration Pin Pull-Up Resistors

During configuration, the three mode pins, M0, M1, and M2, have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected.

The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors after configuration.

The **PROGRAM** input pin has a permanent weak pull-up.

## Soft Start-up

Like the XC3000A, XC4000 Series devices have “Soft Start-up.” When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. Immediately after start-up, the slew rate of the individual outputs is, as in the XC4000 family, determined by the individual configuration option.

## XC4000 and XC4000A Compatibility

Existing XC4000 bitstreams can be used to configure an XC4000E device. XC4000A bitstreams must be recompiled for use with the XC4000E due to improved routing resources, although the devices are pin-for-pin compatible.

## Additional Improvements in XC4000X Only

### Increased Routing

New interconnect in the XC4000X includes twenty-two additional vertical lines in each column of CLBs and twelve new horizontal lines in each row of CLBs. The twelve “Quad Lines” in each CLB row and column include optional repowering buffers for maximum speed. Additional high-performance routing near the IOBs enhances pin flexibility.

### Faster Input and Output

A fast, dedicated early clock sourced by global clock buffers is available for the IOBs. To ensure synchronization with the regular global clocks, a Fast Capture latch driven by the early clock is available. The input data can be initially loaded into the Fast Capture latch with the early clock, then transferred to the input flip-flop or latch with the low-skew global clock. A programmable delay on the input can be used to avoid hold-time requirements. See [“IOB Input Signals” on page 4-21](#) for more information.

### Latch Capability in CLBs

Storage elements in the XC4000X CLB can be configured as either flip-flops or latches. This capability makes the FPGA highly synthesis-compatible.

### IOB Output MUX From Output Clock

A multiplexer in the IOB allows the output clock to select either the output data or the IOB clock enable as the output to the pad. Thus, two different data signals can share a single output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. This multiplexer can also be configured as an AND-gate to implement a very fast pin-to-pin path. See [“IOB Output Signals” on page 4-24](#) for more information.

### Additional Address Bits

Larger devices require more bits of configuration data. A daisy chain of several large XC4000X devices may require a PROM that cannot be addressed by the eighteen address bits supported in the XC4000E. The XC4000X Series therefore extends the addressing in Master Parallel configuration mode to 22 bits.

## Detailed Functional Description

XC4000 Series devices achieve high speed through advanced semiconductor technology and improved architecture. The XC4000E and XC4000X support system clock rates of up to 80 MHz and internal performance in excess of 150 MHz. Compared to older Xilinx FPGA families, XC4000 Series devices are more powerful. They offer on-chip edge-triggered and dual-port RAM, clock enables on I/O flip-flops, and wide-input decoders. They are more versatile in many applications, especially those involving RAM. Design cycles are faster due to a combination of increased routing resources and more sophisticated software.

## Basic Building Blocks

Xilinx user-programmable gate arrays include two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.

Three other types of circuits are also available:

- 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
- Wide edge decoders are available around the periphery of each device.
- An on-chip oscillator is provided.

Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements to the appropriate networks.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. Each of these available circuits is described in this section.

## Configurable Logic Blocks (CLBs)

Configurable Logic Blocks implement most of the logic in an FPGA. The principal CLB elements are shown in [Figure 2](#). Two 4-input function generators (F and G) offer unrestricted versatility. Most combinatorial logic functions need four or fewer inputs. However, a third function generator (H) is provided. The H function generator has three inputs. Either zero, one, or two of these inputs can be the outputs of F and G; the other input(s) are from outside the CLB. The CLB can, therefore, implement certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

Each CLB contains two storage elements that can be used to store the function generator outputs. However, the storage elements and function generators can also be used independently. These storage elements can be configured as flip-flops in both XC4000E and XC4000X devices; in the XC4000X they can optionally be configured as latches. DIN can be used as a direct input to either of the two storage elements. H1 can drive the other through the H function generator. Function generator outputs can also drive two outputs independent of the storage element outputs. This versatility increases logic capacity and simplifies routing.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and storage elements. These inputs and outputs connect to the programmable interconnect resources outside the block.

## Function Generators

Four independent inputs are provided to each of two function generators (F1 - F4 and G1 - G4). These function generators, with outputs labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of four inputs. The function generators are implemented as memory look-up tables. The propagation delay is therefore independent of the function implemented.

A third function generator, labeled H', can implement any Boolean function of its three inputs. Two of these inputs can optionally be the F' and G' functional generator outputs. Alternatively, one or both of these inputs can come from outside the CLB (H2, H0). The third input must come from outside the block (H1).

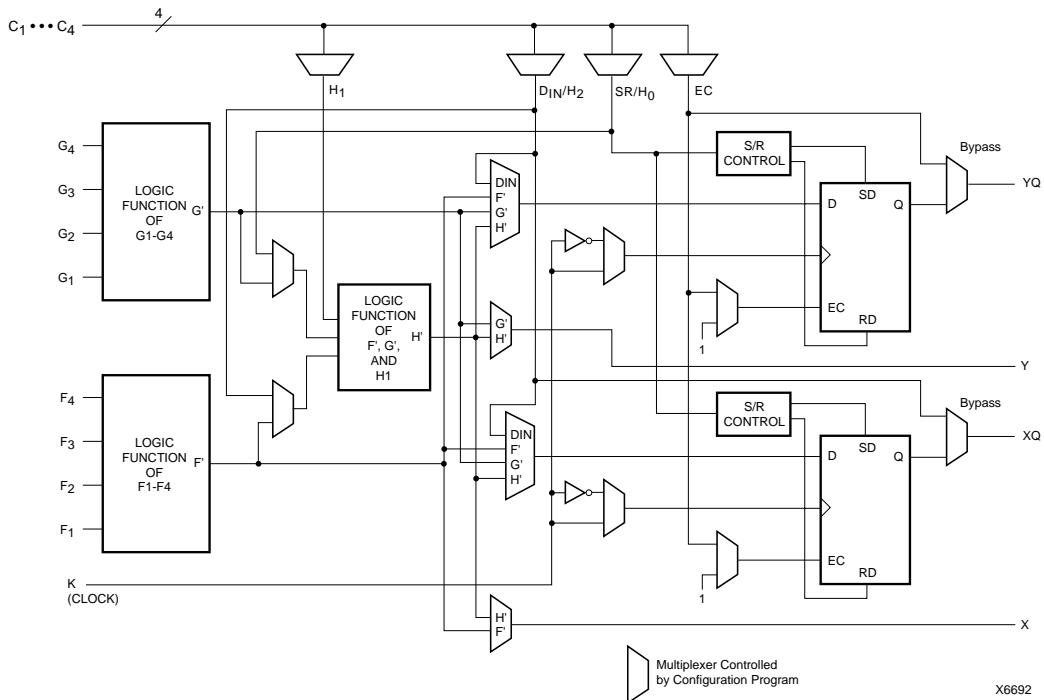
Signals from the function generators can exit the CLB on two outputs. F' or H' can be connected to the X output. G' or H' can be connected to the Y output.

A CLB can be used to implement any of the following functions:

- any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables<sup>1</sup>
- any single function of five variables
- any function of four variables together with some functions of six variables
- some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.



**Figure 2: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)**

### Flip-Flops

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well.

The two edge-triggered D-type flip-flops have common clock (K) and clock enable (EC) inputs. Either or both clock inputs can also be permanently enabled. Storage element functionality is described in [Table 3](#).

### Latches (XC4000X only)

The CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Storage element functionality is described in [Table 3](#).

### Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The clock pin is shared by both storage elements. However, the clock is individually invertible for each storage element. Any inverter placed on the clock input is automatically absorbed into the CLB.

### Clock Enable

The clock enable signal (EC) is active High. The EC pin is shared by both storage elements. If left unconnected for either, the clock enable for that storage element defaults to the active state. EC is not invertible within the CLB.

**Table 3: CLB Storage Element Functionality  
(active rising edge is shown)**

Mode	K	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop	X	X	1	X	SR
	<u>—</u>	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:



Don't care



Rising edge



Set or Reset value. Reset is default.



Input is Low or unconnected (default value)



Input is High or unconnected (default value)

## Set/Reset

An asynchronous storage element input (SR) can be configured as either set or reset. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a Global Set/Reset pulse during normal operation, and the effect of a pulse on the SR pin of the CLB. All three set/reset functions for any single flip-flop are controlled by the same configuration data bit.

The set/reset state can be independently specified for each flip-flop. This input can also be independently disabled for either flip-flop.

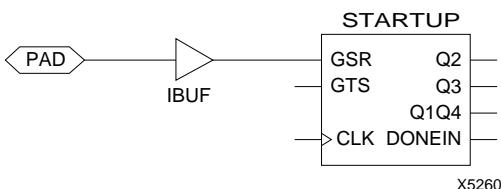
The set/reset state is specified by using the INIT attribute, or by placing the appropriate set or reset flip-flop library symbol.

SR is active High. It is not invertible within the CLB.

## Global Set/Reset

A separate Global Set/Reset line (not shown in [Figure 2](#)) sets or clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, a reset flip-flop is reset by both SR and GSR.



**Figure 3:** Schematic Symbols for Global Set/Reset

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See [Figure 3](#).) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Set/Reset signal.

Alternatively, GSR can be driven from any internal node.

## Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by any of the functions F', G', and H', or by the Direct In (DIN) block input. The flip-flops or latches drive the XQ and YQ CLB outputs.

Two fast feed-through paths are available, as shown in [Figure 2](#). A two-to-one multiplexer on each of the XQ and YQ outputs selects between a storage element output and any of the control inputs. This bypass is sometimes used by the automated router to repower internal signals.

## Control Signals

Multiplexers in the CLB map the four control inputs (C1 - C4 in [Figure 2](#)) into the four internal control signals (H1, DIN/H2, SR/H0, and EC). Any of these inputs can drive any of the four internal control signals.

When the logic function is enabled, the four inputs are:

- EC — Enable Clock
- SR/H0 — Asynchronous Set/Reset or H function generator Input 0
- DIN/H2 — Direct In or H function generator Input 2
- H1 — H function generator Input 1.

When the memory function is enabled, the four inputs are:

- EC — Enable Clock
- WE — Write Enable
- D0 — Data Input to F and/or G function generator
- D1 — Data input to G function generator (16x1 and 16x2 modes) or 5th Address bit (32x1 mode).

## Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC4000 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol (for the XC4000X only) is called LDCE.

In XC4000 Series devices, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input K. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

## Using Function Generators as RAM

Optional modes for each CLB make the memory look-up tables in the F' and G' function generators usable as an array of Read/Write memory cells. Available modes are level-sensitive (similar to the XC4000/A/H families), edge-triggered, and dual-port edge-triggered. Depending on the

selected mode, a single CLB can be configured as either a 16x2, 32x1, or 16x1 bit array.

Supported CLB memory configurations and timing modes for single- and dual-port modes are shown in [Table 4](#).

XC4000 Series devices are the first programmable logic devices with edge-triggered (synchronous) and dual-port RAM accessible to the user. Edge-triggered RAM simplifies system timing. Dual-port RAM doubles the effective throughput of FIFO applications. These features can be individually programmed in any XC4000 Series CLB.

### Advantages of On-Chip and Edge-Triggered RAM

The on-chip RAM is extremely fast. The read access time is the same as the logic delay. The write access time is slightly slower. Both access times are much faster than any off-chip solution, because they avoid I/O delays.

Edge-triggered RAM, also called synchronous RAM, is a feature never before available in a Field Programmable Gate Array. The simplicity of designing with edge-triggered RAM, and the markedly higher achievable performance, add up to a significant improvement over existing devices with on-chip RAM.

Three application notes are available from Xilinx that discuss edge-triggered RAM: "XC4000E Edge-Triggered and Dual-Port RAM Capability," "Implementing FIFOs in XC4000E RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both XC4000E and XC4000X RAM.

**Table 4: Supported RAM Modes**

	16 x 1	16 x 2	32 x 1	Edge- Triggered Timing	Level- Sensitive Timing
Single-Port	✓	✓	✓	✓	✓
Dual-Port	✓			✓	

### RAM Configuration Options

The function generators in any CLB can be configured as RAM arrays in the following sizes:

- Two 16x1 RAMs: two data inputs and two data outputs with identical or, if preferred, different addressing for each RAM
- One 32x1 RAM: one data input and one data output.

One F or G function generator can be configured as a 16x1 RAM while the other function generators are used to implement any function of up to 5 inputs.

Additionally, the XC4000 Series RAM may have either of two timing modes:

- Edge-Triggered (Synchronous): data written by the designated edge of the CLB clock. WE acts as a true clock enable.

- Level-Sensitive (Asynchronous): an external WE signal acts as the write strobe.

The selected timing mode applies to both function generators within a CLB when both are configured as RAM.

The number of read ports is also programmable:

- Single Port: each function generator has a common read and write port
- Dual Port: both function generators are configured together as a single 16x1 dual-port RAM with one write port and two read ports. Simultaneous read and write operations to the same or different addresses are supported.

RAM configuration options are selected by placing the appropriate library symbol.

### Choosing a RAM Configuration Mode

The appropriate choice of RAM mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Recommended usage is shown in [Table 5](#).

The difference between level-sensitive, edge-triggered, and dual-port RAM is only in the write operation. Read operation and timing is identical for all modes of operation.

**Table 5: RAM Mode Selection**

	Level- Sensitive	Edge- Triggered	Dual-Port Edge- Triggered
Use for New Designs?	No	Yes	Yes
Size (16x1, Registered)	1/2 CLB	1/2 CLB	1 CLB
Simultaneous Read/Write	No	No	Yes
Relative Performance	X	2X	2X (4X effective)

### RAM Inputs and Outputs

The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table.

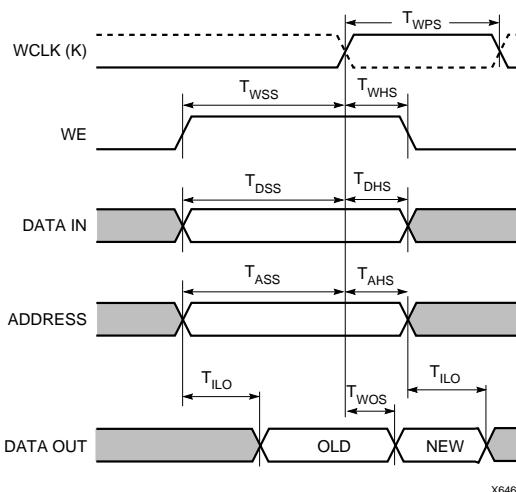
The functionality of the CLB control signals changes when the function generators are configured as RAM. The DIN/H2, H1, and SR/H0 lines become the two data inputs (D0, D1) and the Write Enable (WE) input for the 16x2 memory. When the 32x1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input.

The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs. They can exit the CLB through its X and Y outputs, or can be captured in the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other portions of the CLB, with the exception of the redefinition of the control signals. In 16x2 and 16x1 modes, the H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

### Single-Port Edge-Triggered Mode

Edge-triggered (synchronous) RAM simplifies timing requirements. XC4000 Series edge-triggered RAM timing operates like writing to a data register. Data and address are presented. The register is enabled for writing by a logic High on the write enable input, WE. Then a rising or falling clock edge loads the data into the register, as shown in Figure 4.



**Figure 4: Edge-Triggered RAM Write Timing**

Complex timing relationships between address, data, and write enable signals are not required, and the external write enable pulse becomes a simple clock enable. The active

edge of WCLK latches the address, input data, and WE signals. An internal write pulse is generated that performs the write. See Figure 5 and Figure 6 for block diagrams of a CLB configured as 16x2 and 32x1 edge-triggered, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port, edge-triggered mode are shown in Table 6.

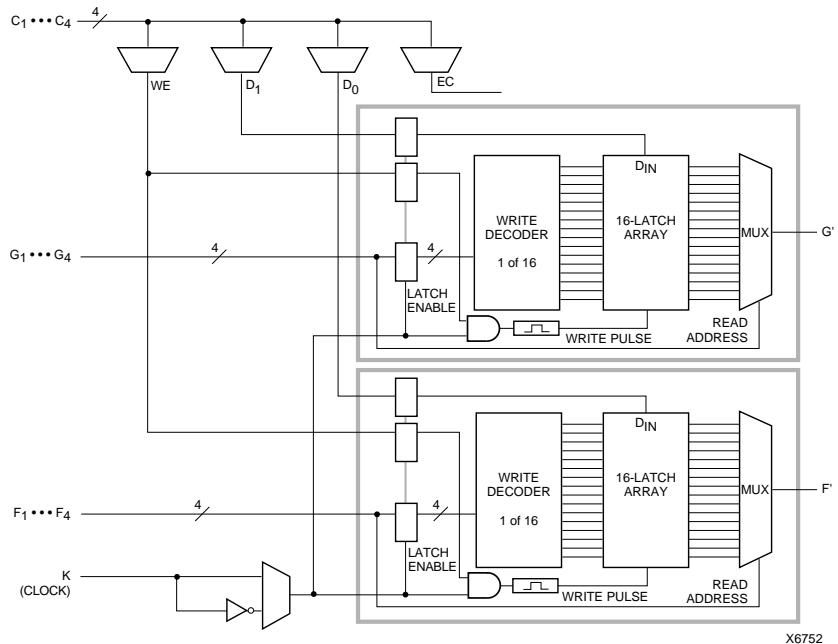
The Write Clock input (WCLK) can be configured as active on either the rising edge (default) or the falling edge. It uses the same CLB pin (K) used to clock the CLB flip-flops, but it can be independently inverted. Consequently, the RAM output can optionally be registered within the same CLB either by the same clock edge as the RAM, or by the opposite edge of this clock. The sense of WCLK applies to both function generators in the CLB when both are configured as RAM.

The WE pin is active-High and is not invertible within the CLB.

**Note:** The pulse following the active edge of WCLK (T<sub>WPS</sub> in Figure 4) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

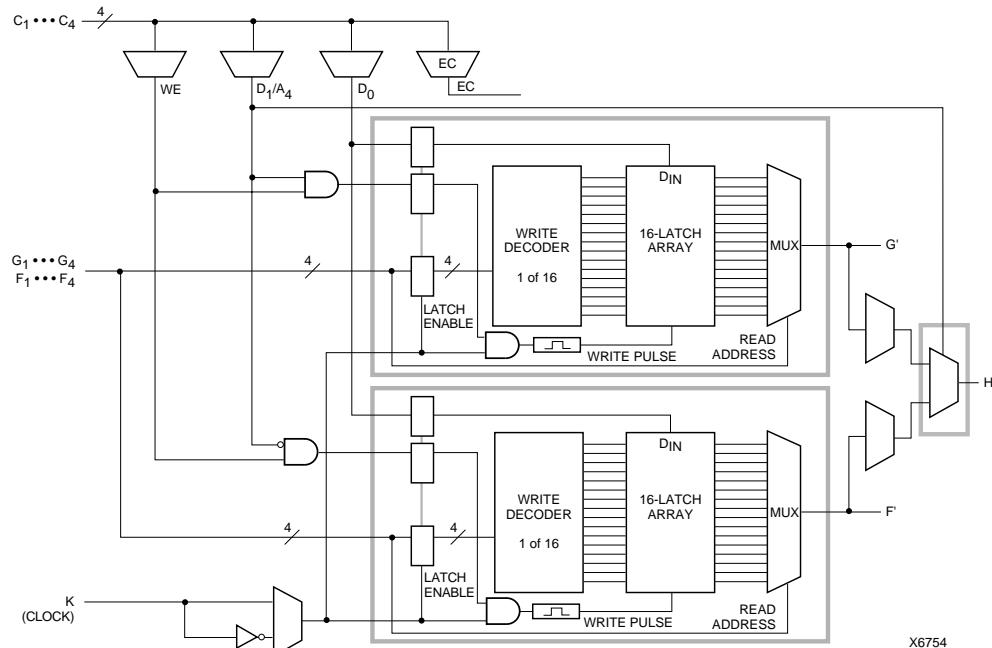
**Table 6: Single-Port Edge-Triggered RAM Signals**

RAM Signal	CLB Pin	Function
D	D0 or D1 (16x2, 16x1), D0 (32x1)	Data In
A[3:0]	F1-F4 or G1-G4	Address
A[4]	D1 (32x1)	Address
WE	WE	Write Enable
WCLK	K	Clock
SPO (Data Out)	F' or G'	Single Port Out (Data Out)



X6752

Figure 5: 16x2 (or 16x1) Edge-Triggered Single-Port RAM



X6754

Figure 6: 32x1 Edge-Triggered Single-Port RAM (F and G addresses are identical)

## Dual-Port Edge-Triggered Mode

In dual-port mode, both the F and G function generators are used to create a single 16x1 RAM array with one write port and two read ports. The resulting RAM array can be read and written simultaneously at two independent addresses. Simultaneous read and write operations at the same address are also supported.

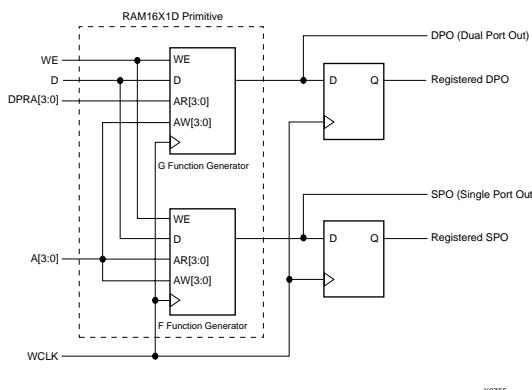
Dual-port mode always has edge-triggered write timing, as shown in [Figure 4](#).

[Figure 7](#) shows a simple model of an XC4000 Series CLB configured as dual-port RAM. One address port, labeled A[3:0], supplies both the read and write address for the F function generator. This function generator behaves the same as a 16x1 single-port edge-triggered RAM array. The RAM output, Single Port Out (SPO), appears at the F function generator output. SPO, therefore, reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the G function generator. The write address for the G function generator, however, comes from the address A[3:0]. The output from this 16x1 RAM array, Dual Port Out (DPO), appears at the G function generator output. DPO, therefore, reflects the data at address DPRA[3:0].

Therefore, by using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. Simultaneous access doubles the effective throughput of the FIFO.

The relationships between CLB pins and RAM inputs and outputs for dual-port, edge-triggered mode are shown in [Table 7](#). See [Figure 8 on page 4-16](#) for a block diagram of a CLB configured in this mode.



**Figure 7: XC4000 Series Dual-Port RAM, Simple Model**

**Table 7: Dual-Port Edge-Triggered RAM Signals**

RAM Signal	CLB Pin	Function
D	D0	Data In
A[3:0]	F1-F4	Read Address for F, Write Address for F and G
DPRA[3:0]	G1-G4	Read Address for G
WE	WE	Write Enable
WCLK	K	Clock
SPO	F'	Single Port Out (addressed by A[3:0])
DPO	G'	Dual Port Out (addressed by DPRA[3:0])

**Note:** The pulse following the active edge of WCLK ( $T_{WPS}$  in [Figure 4](#)) must be less than one millisecond wide. For most applications, this requirement is not overly restrictive; however, it must not be forgotten. Stopping WCLK at this point in the write cycle could result in excessive current and even damage to the larger devices if many CLBs are configured as edge-triggered RAM.

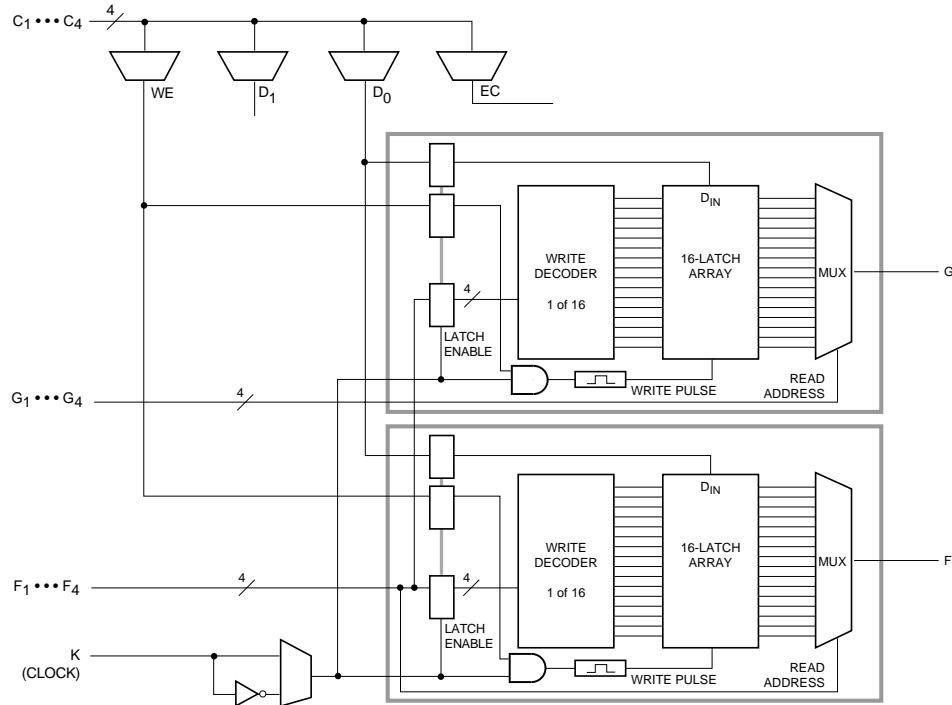
## Single-Port Level-Sensitive Timing Mode

**Note:** Edge-triggered mode is recommended for all new designs. Level-sensitive mode, also called asynchronous mode, is still supported for XC4000 Series backward-compatibility with the XC4000 family.

Level-sensitive RAM timing is simple in concept but can be complicated in execution. Data and address signals are presented, then a positive pulse on the write enable pin (WE) performs a write into the RAM at the designated address. As indicated by the “level-sensitive” label, this RAM acts like a latch. During the WE High pulse, changing the data lines results in new data written to the old address. Changing the address lines while WE is High results in spurious data written to the new address—and possibly at other addresses as well, as the address lines inevitably do not all change simultaneously.

The user must generate a carefully timed WE signal. The delay on the WE signal and the address lines must be carefully verified to ensure that WE does not become active until after the address lines have settled, and that WE goes inactive before the address lines change again. The data must be stable before and after the falling edge of WE.

In practical terms, WE is usually generated by a 2X clock. If a 2X clock is not available, the falling edge of the system clock can be used. However, there are inherent risks in this approach, since the WE pulse must be guaranteed inactive before the next rising edge of the system clock. Several older application notes are available from Xilinx that discuss the design of level-sensitive RAMs. These application notes include XAPP031, “*Using the XC4000 RAM Capability*,” and XAPP042, “*High-Speed RAM Design in XC4000*.” However, the edge-triggered RAM available in the XC4000 Series is superior to level-sensitive RAM for almost every application.



X6748

**Figure 8:** 16x1 Edge-Triggered Dual-Port RAM

**Figure 9** shows the write timing for level-sensitive, single-port RAM.

The relationships between CLB pins and RAM inputs and outputs for single-port level-sensitive mode are shown in **Table 8**.

**Figure 10** and **Figure 11** show block diagrams of a CLB configured as 16x2 and 32x1 level-sensitive, single-port RAM.

#### Initializing RAM at Configuration

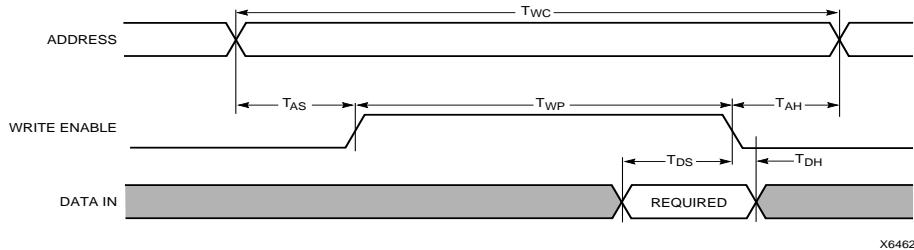
Both RAM and ROM implementations of the XC4000 Series devices are initialized during configuration. The initial contents are defined via an INIT attribute or property

attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to all zeros, by default.

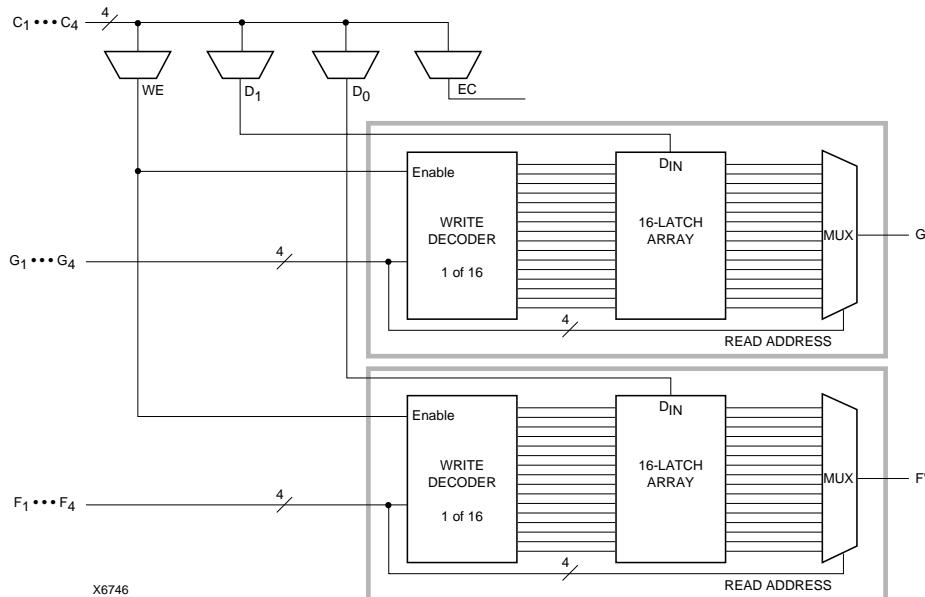
RAM initialization occurs only during configuration. The RAM content is not affected by Global Set/Reset.

**Table 8: Single-Port Level-Sensitive RAM Signals**

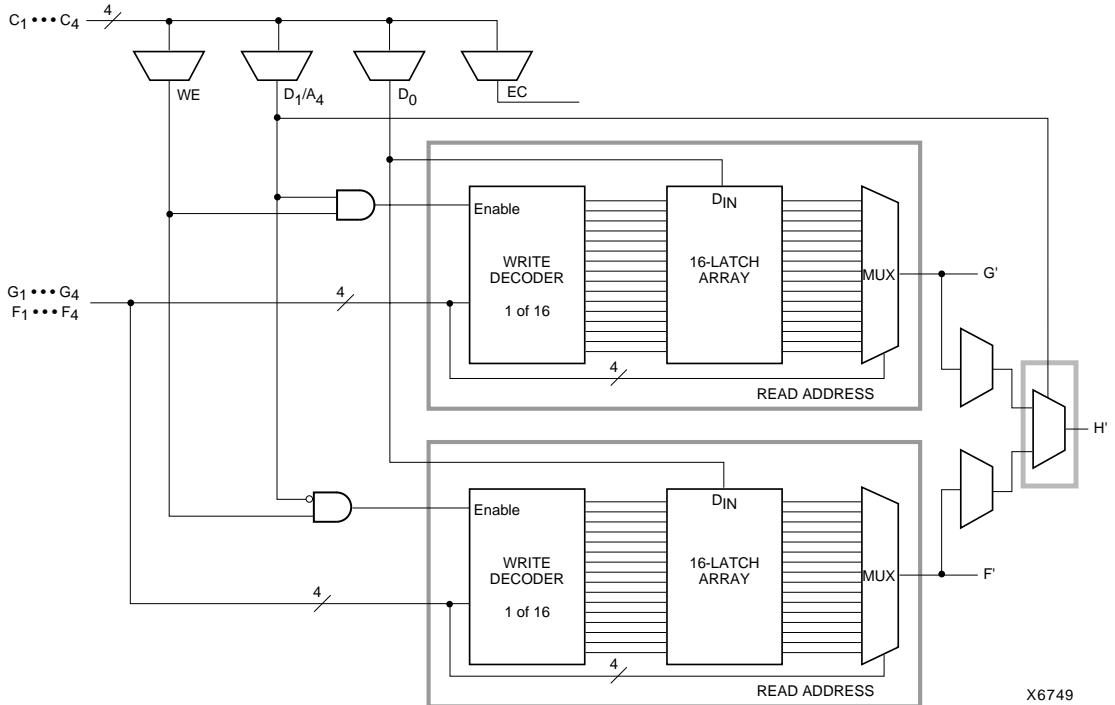
RAM Signal	CLB Pin	Function
D	D0 or D1	Data In
A[3:0]	F1-F4 or G1-G4	Address
WE	WE	Write Enable
O	F' or G'	Data Out



**Figure 9:** Level-Sensitive RAM Write Timing



**Figure 10:** 16x2 (or 16x1) Level-Sensitive Single-Port RAM



**Figure 11: 32x1 Level-Sensitive Single-Port RAM (F and G addresses are identical)**

### Fast Carry Logic

Each CLB F and G function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources.

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

This fast carry logic is one of the more significant features of the XC4000 Series, speeding up arithmetic and counting into the 70 MHz range.

The carry chain in XC4000E devices can run either up or down. At the top and bottom of the columns where there are no CLBs above or below, the carry is propagated to the right. (See [Figure 12](#).) In order to improve speed in the high-capacity XC4000X devices, which can potentially have very long carry chains, the carry chain travels upward only, as shown in [Figure 13](#). Additionally, standard interconnect can be used to route a carry signal in the downward direction.

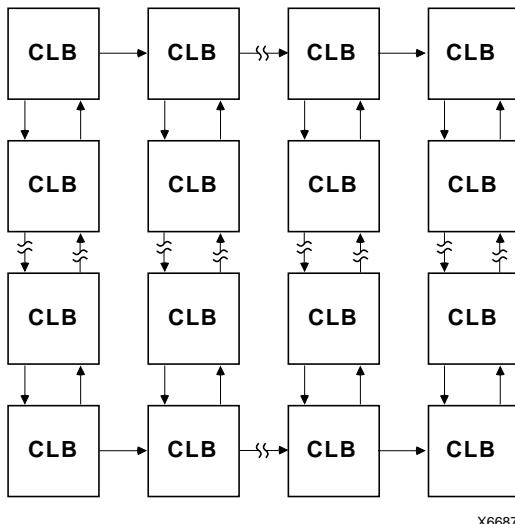
[Figure 14 on page 4-20](#) shows an XC4000E CLB with dedicated fast carry logic. The carry logic in the XC4000X is similar, except that COUT exits at the top only, and the signal CINDOWN does not exist. As shown in [Figure 14](#), the carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

[Figure 15 on page 4-21](#) shows the details of the carry logic for the XC4000E. This diagram shows the contents of the box labeled "CARRY LOGIC" in [Figure 14](#). The XC4000X carry logic is very similar, but a multiplexer on the pass-through carry chain has been eliminated to reduce delay. Additionally, in the XC4000X the multiplexer on the G4 path has a memory-programmable 0 input, which permits G4 to

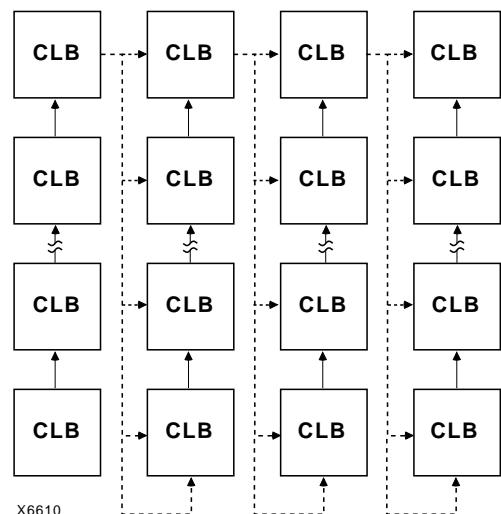
directly connect to COUT. G4 thus becomes an additional high-speed initialization path for carry-in.

The dedicated carry logic is discussed in detail in Xilinx document XAPP 013: “*Using the Dedicated Carry Logic in XC4000*.” This discussion also applies to XC4000E devices, and to XC4000X devices when the minor logic changes are taken into account.

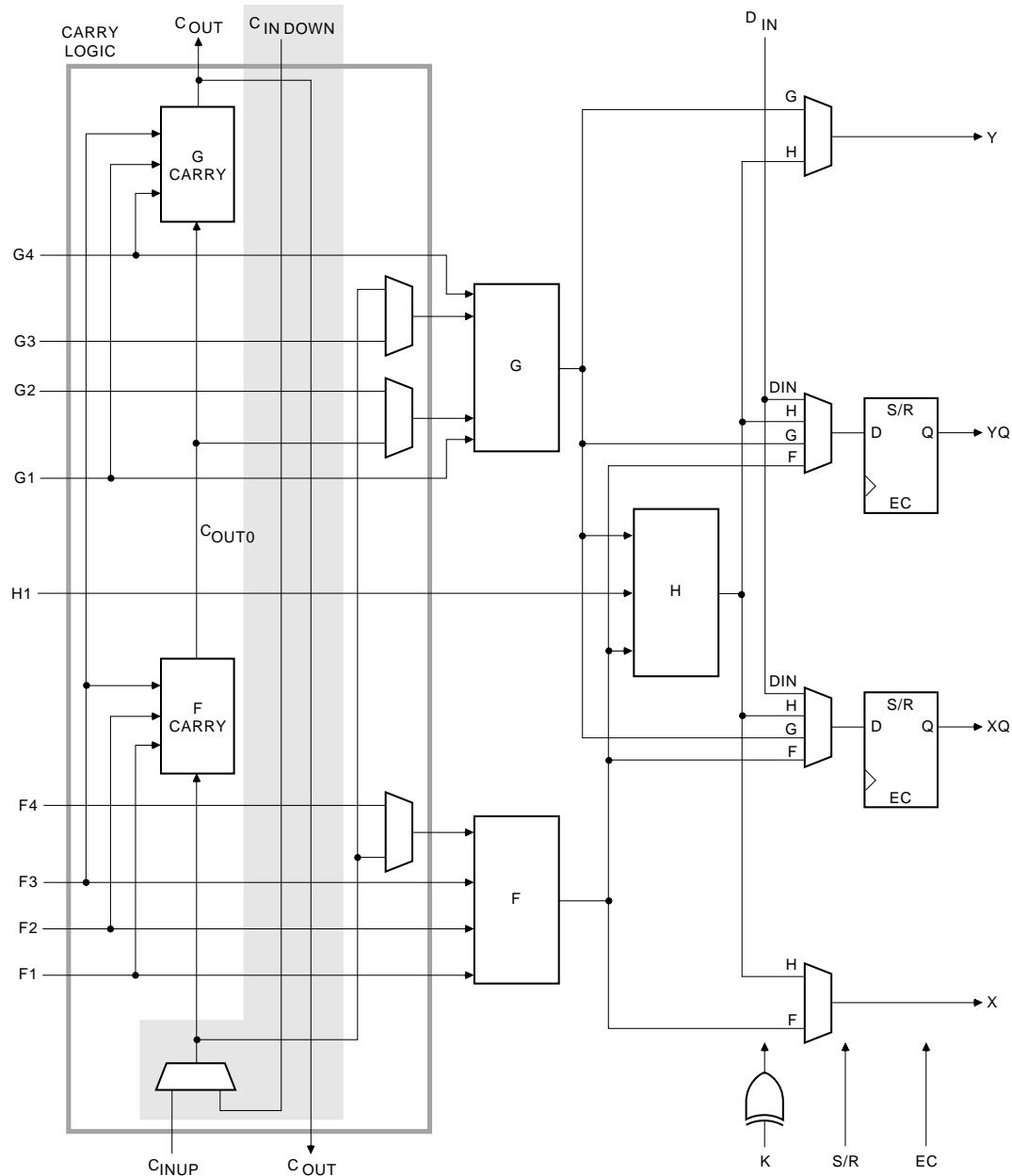
The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.



**Figure 12: Available XC4000E Carry Propagation Paths**

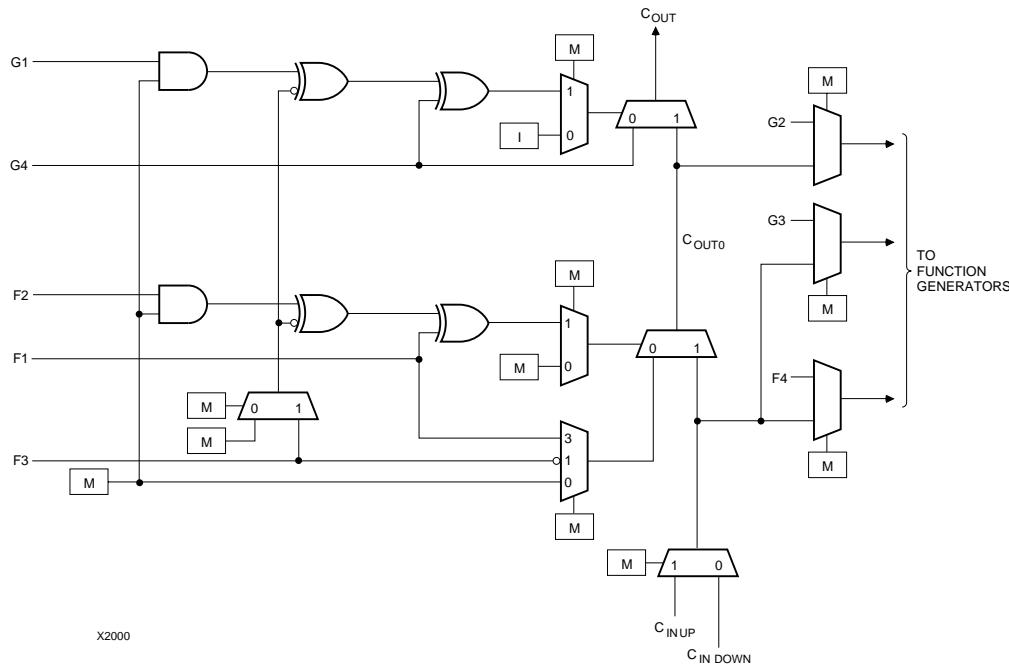


**Figure 13: Available XC4000X Carry Propagation Paths (dotted lines use general interconnect)**



X6699

Figure 14: Fast Carry Logic in XC4000E CLB (shaded area not present in XC4000X)



**Figure 15:** Detail of XC4000E Dedicated Carry Logic

## Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

**Figure 16** shows a simplified block diagram of the XC4000E IOB. A more complete diagram which includes the boundary scan logic of the XC4000E IOB can be found in [Figure 41 on page 4-44](#), in the “Boundary Scan” section.

The XC4000X IOB contains some special features not included in the XC4000E IOB. These features are highlighted in a simplified block diagram found in [Figure 17](#), and discussed throughout this section. When XC4000X special features are discussed, they are clearly identified in the text. Any feature not so identified is present in both XC4000E and XC4000X devices.

### IOB Input Signals

Two paths, labeled I1 and I2 in [Figure 16](#) and [Figure 17](#), bring input signals into the array. Inputs also connect to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive latch.

The choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are available, and some combinations of latches and flip-flops can be implemented in a single IOB, as described in the *XACT Libraries Guide*.

The XC4000E inputs can be globally configured for either TTL (1.2V) or 5.0 volt CMOS thresholds, using an option in the bitstream generation software. There is a slight input hysteresis of about 300mV. The XC4000E output levels are also configurable; the two global adjustments of input threshold and output level are independent.

Inputs on the XC4000XL are TTL compatible and 3.3V CMOS compatible. Outputs on the XC4000XL are pulled to the 3.3V positive supply.

The inputs of XC4000 Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC4000 Series device inputs are shown in [Table 9](#).

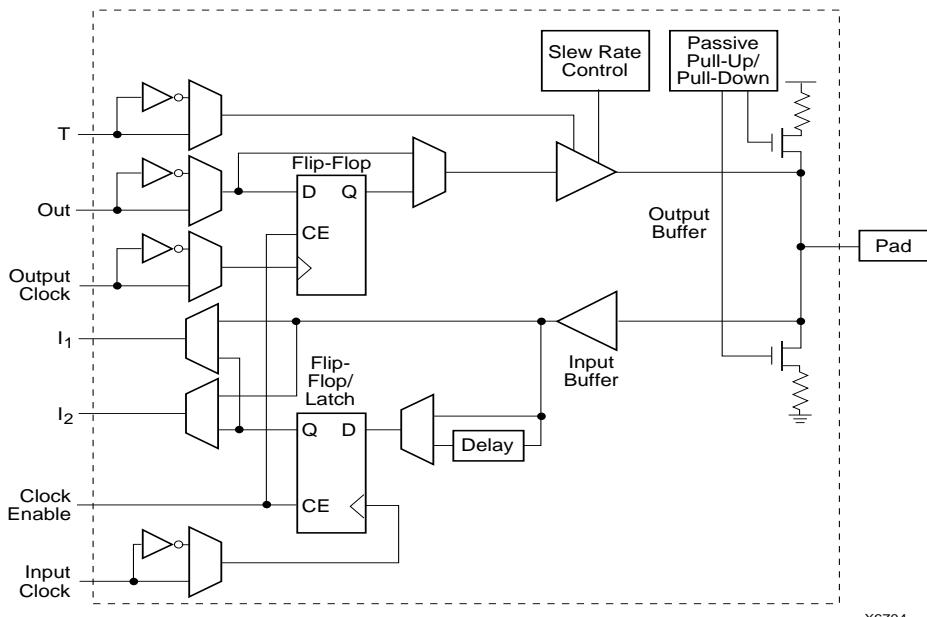


Figure 16: Simplified Block Diagram of XC4000E IOB

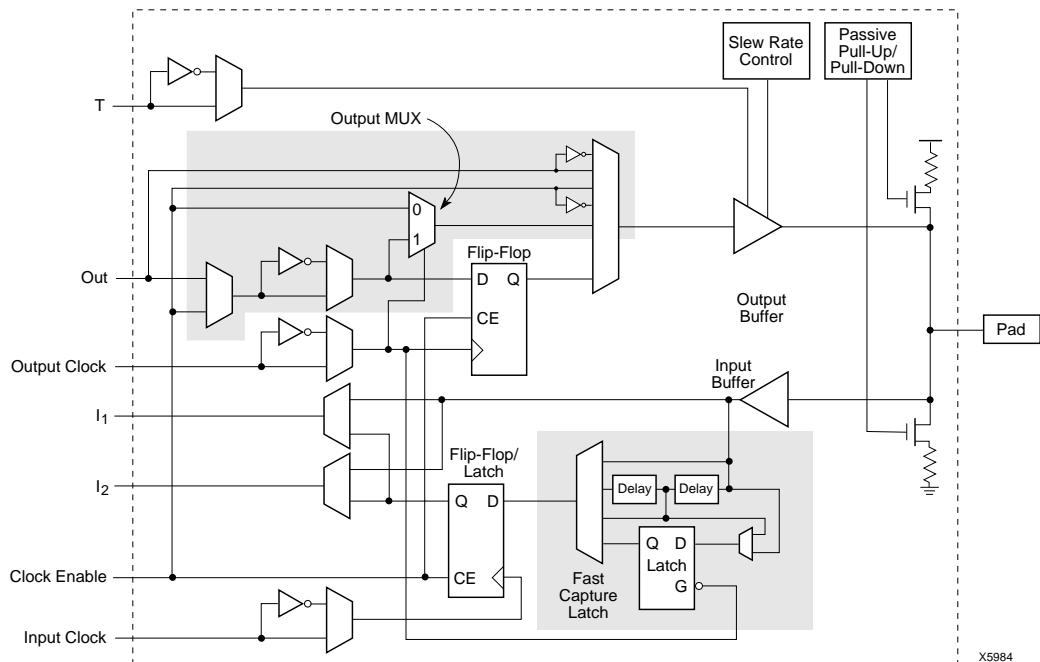


Figure 17: Simplified Block Diagram of XC4000X IOB (shaded areas indicate differences from XC4000E)

**Table 9: Supported Sources for XC4000 Series Device Inputs**

Source	XC4000E/EX Series Inputs		XC4000XL Series Inputs
	5 V, TTL	5 V, CMOS	3.3 V CMOS
Any device, Vcc = 3.3 V, CMOS outputs	✓		✓
XC4000 Series, Vcc = 5 V, TTL outputs	✓	Unreliable Data	✓
Any device, Vcc = 5 V, TTL outputs ( $V_{oh} \leq 3.7$ V)	✓		✓
Any device, Vcc = 5 V, CMOS outputs	✓	✓	✓

#### XC4000XL 5-Volt Tolerant I/Os

The I/Os on the XC4000XL are fully 5-volt tolerant even though the  $V_{CC}$  is 3.3 volts. This allows 5 V signals to directly connect to the XC4000XL inputs without damage, as shown in [Table 9](#). In addition, the 3.3 volt  $V_{CC}$  can be applied before or after 5 volt signals are applied to the I/Os. This makes the XC4000XL immune to power supply sequencing problems.

#### Registered Inputs

The I1 and I2 signals that exit the block can each carry either the direct or registered input signal.

The input and output storage elements in each IOB have a common clock enable input, which, through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC pin on the XC4000 Series CLB. It cannot be inverted within the IOB.

The storage element behavior is shown in [Table 10](#).

**Table 10: Input Register Functionality  
(active rising edge is shown)**

Mode	Clock	Clock Enable	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	/	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X

Don't care

SR

Rising edge

0\*

Set or Reset value. Reset is default.

1\*

Input is Low or unconnected (default value)

Input is High or unconnected (default value)

#### Optional Delay Guarantees Zero Hold Time

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the IOB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the IOB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the default.

The XC4000E IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC4000E global clock buffers. (See "[Global Nets and Buffers \(XC4000E only\)](#)" on page 4-36 for a description of the global clock buffers in the XC4000E.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop.

The XC4000X IOB has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The attributes or properties used to select the desired delay are shown in [Table 11](#). The choices are no added attribute, MEDDELAY, and NODELAY. The default setting, with no added attribute, ensures no hold time with respect to any of the XC4000X clock buffers, including the Global Low-Skew buffers. MEDDELAY ensures no hold time with respect to the Global Early buffers. Inputs with NODELAY may have a positive hold time with respect to all clock buffers. For a description of each of these buffers, see "[Global Nets and Buffers \(XC4000X only\)](#)" on page 4-38.

**Table 11: XC4000X IOB Input Delay Element**

Value	When to Use
full delay (default, no attribute added)	Zero Hold with respect to Global Low-Skew Buffer, Global Early Buffer
MEDDELAY	Zero Hold with respect to Global Early Buffer
NODELAY	Short Setup, positive Hold time

### Additional Input Latch for Fast Capture (XC4000X only)

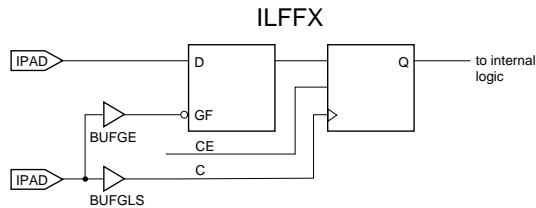
The XC4000X IOB has an additional optional latch on the input. This latch, as shown in [Figure 17](#), is clocked by the output clock — the clock used for the output flip-flop — rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the very fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To use this Fast Capture technique, drive the output clock pin (the Fast Capture latching signal) from the output of one of the Global Early buffers supplied in the XC4000X. The second storage element should be clocked by a Global Low-Skew buffer, to synchronize the incoming data to the internal logic. (See [Figure 18](#).) These special buffers are described in “[Global Nets and Buffers \(XC4000X only\)](#)” on [page 4-38](#).

The Fast Capture latch (FCL) is designed primarily for use with a Global Early buffer. For Fast Capture, a single clock signal is routed through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) The Fast Capture latch is clocked by the Global Early buffer, and the standard IOB flip-flop or latch is clocked by the Global Low-Skew buffer. This mode is the safest way to use the Fast Capture latch, because the clock buffers on both storage elements are driven by the same pad. There is no external skew between clock pads to create potential problems.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB. If a single BUFG output is used to drive both clock inputs, the software automatically runs the clock through both a Global Low-Skew buffer and a Global Early buffer, and clocks the Fast Capture latch appropriately.

[Figure 17](#) on [page 4-22](#) also shows a two-tap delay on the input. By default, if the Fast Capture latch is used, the Xilinx software assumes a Global Early buffer is driving the clock, and selects MEDDELAY to ensure a zero hold time. Select



**Figure 18:** Examples Using XC4000X FCL

the desired delay based on the discussion in the previous subsection.

### IOB Output Signals

Output signals can be optionally inverted within the IOB, and can pass directly to the pad or be stored in an edge-triggered flip-flop. The functionality of this flip-flop is shown in [Table 12](#).

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The 4-mA maximum output current specification of many FPGAs often forces the user to add external buffers, which are especially cumbersome on bidirectional I/O lines. The XC4000E and XC4000EX/XL devices solve many of these problems by providing a guaranteed output sink current of 12 mA. Two adjacent outputs can be interconnected externally to sink up to 24 mA. The XC4000E and XC4000EX/XL FPGAs can thus directly drive buses on a printed circuit board.

By default, the output pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable. In the XC4000XL, all outputs are pulled to the positive supply rail.

**Table 12: Output Flip-Flop Functionality (active rising edge is shown)**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	/	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

- X Don't care
- / Rising edge
- SR Set or Reset value. Reset is default.
- 0\* Input is Low or unconnected (default value)
- 1\* Input is High or unconnected (default value)
- Z 3-state

Any XC4000 Series 5-Volt device with its outputs configured in TTL mode can drive the inputs of any typical 3.3-Volt device. (For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

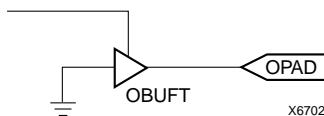
Supported destinations for XC4000 Series device outputs are shown in [Table 13](#).

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See [Figure 19](#).)

**Table 13: Supported Destinations for XC4000 Series Outputs**

Destination	XC4000 Series Outputs		
	3.3 V, CMOS	5 V, TTL	5 V, CMOS
Any typical device, Vcc = 3.3 V, CMOS-threshold inputs	✓	✓	some <sup>1</sup>
Any device, Vcc = 5 V, TTL-threshold inputs	✓	✓	✓
Any device, Vcc = 5 V, CMOS-threshold inputs	Unreliable Data		✓

1. Only if destination device has 5-V tolerant inputs



**Figure 19: Open-Drain Output**

### Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC4000E devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground

pin pair. For XC4000X devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce. Therefore, the maximum total capacitive load is 300 pF between each external Power/Ground pin pair. Maximum loading may vary for the low-voltage devices.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC4000E devices and 600 pF for XC4000X devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC4000 Series.

XC4000 Series devices have a feature called “Soft Startup,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

### Global Three-State

A separate Global 3-State line (not shown in [Figure 16](#) or [Figure 17](#)) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to GSR. See [Figure 3 on page 4-11](#) for details.

Alternatively, GTS can be driven from any internal node.

## Output Multiplexer/2-Input Function Generator (XC4000X only)

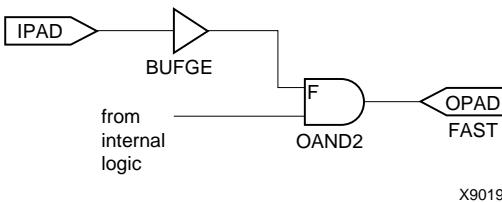
As shown in [Figure 17 on page 4-22](#), the output path in the XC4000X IOB contains an additional multiplexer not available in the XC4000E IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass-gate, AND-gate, OR-gate, or XOR-gate, with 0, 1, or 2 inverted inputs. The logic used to implement these functions is shown in the upper gray area of [Figure 17](#).

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package.

When the MUX is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global Early buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe Driven by a BUFGE buffer, as shown in [Figure 20](#). The critical-path pin-to-pin delay of this circuit is less than 6 nanoseconds.

As shown in [Figure 17](#), the IOB input pins Out, Output Clock, and Clock Enable have different delays and different flexibilities regarding polarity. Additionally, Output Clock sources are more limited than the other inputs. Therefore, the Xilinx software does not move logic into the IOB function generators unless explicitly directed to do so.

The user can specify that the IOB function generator be used, by placing special library symbols beginning with the letter "O." For example, a 2-input AND-gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in [Figure 21](#).



**Figure 20:** Fast Pin-to-Pin Path in XC4000X



**Figure 21:** AND & MUX Symbols in XC4000X IOB

## Other IOB Options

There are a number of other programmable options in the XC4000 Series IOB.

### Pull-up and Pull-down Resistors

Programmable pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 50 k $\Omega$  – 100 k $\Omega$ . This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See [Table 23 on page 4-59](#) for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

### Independent Clocks

Separate clock signals are provided for the input and output flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent, except that in the XC4000X, the Fast Capture latch shares an IOB input with the output clock pin.

### Early Clock for IOBs (XC4000X only)

Special early clocks are available for IOBs. These clocks are sourced by the same sources as the Global Low-Skew buffers, but are separately buffered. They have fewer loads and therefore less delay. The early clock can drive either the IOB output clock or the IOB input clock, or both. The early clock allows fast capture of input data, and fast clock-to-output on output data. The Global Early buffers that drive these clocks are described in ["Global Nets and Buffers \(XC4000X only\)" on page 4-38](#).

### Global Set/Reset

As with the CLB registers, the Global Set/Reset signal (GSR) can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set

or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops. The choice of set or clear applies to both the initial state of the flip-flop and the response to the Global Set/Reset pulse. See “[Global Set/Reset](#)” on page [4-11](#) for a description of how to use GSR.

### JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, permitting easy chip and board-level testing. More information is provided in “[Boundary Scan](#)” on page [4-43](#).

## Three-State Buffers

A pair of 3-state buffers is associated with each CLB in the array. (See [Figure 28](#) on page [4-31](#).) These 3-state buffers can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources. Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in [Table 14](#).

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. (See [Figure 34](#) on page [4-35](#).)

The horizontal longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Special longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal longlines. These longlines form the wide edge decoders discussed in “[Wide Edge Decoders](#)” on page [4-28](#).

### Three-State Buffer Modes

The 3-state buffers can be configured in three modes:

- Standard 3-state buffer
- Wired-AND with input on the I pin
- Wired OR-AND

### Standard 3-State Buffer

All three pins are used. Place the library element BUFT. Connect the input to the I pin and the output to the O pin. The T pin is an active-High 3-state (i.e. an active-Low enable). Tie the T pin to Ground to implement a standard buffer.

### Wired-AND with Input on the I Pin

The buffer can be used as a Wired-AND. Use the WAND1 library symbol, which is essentially an open-drain buffer. WAND4, WAND8, and WAND16 are also available. See the *XACT Libraries Guide* for further information.

The T pin is internally tied to the I pin. Connect the input to the I pin and the output to the O pin. Connect the outputs of all the WAND1s together and attach a PULLUP symbol.

### Wired OR-AND

The buffer can be configured as a Wired OR-AND. A High level on either input turns off the output. Use the WOR2AND library symbol, which is essentially an open-drain 2-input OR gate. The two input pins are functionally equivalent. Attach the two inputs to the I0 and I1 pins and tie the output to the O pin. Tie the outputs of all the WOR2ANDs together and attach a PULLUP symbol.

### Three-State Buffer Examples

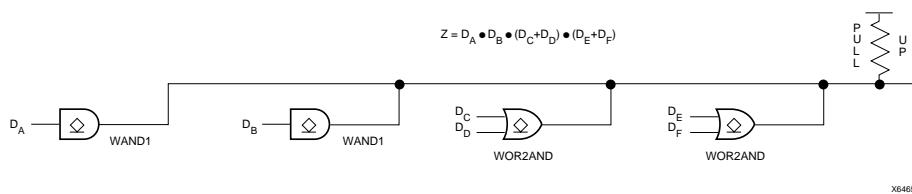
[Figure 22](#) shows how to use the 3-state buffers to implement a wired-AND function. When all the buffer inputs are High, the pull-up resistor(s) provide the High output.

[Figure 23](#) shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in [Table 14](#).

**Table 14: Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN



**Figure 22: Open-Drain Buffers Implement a Wired-AND Function**

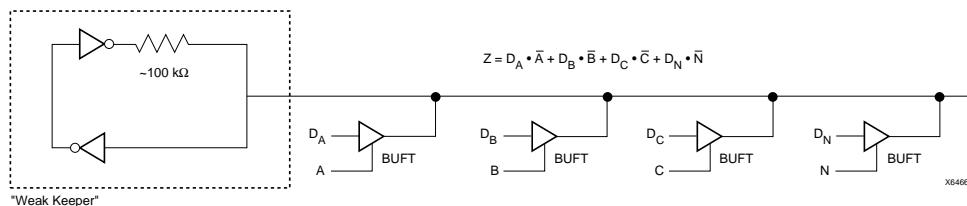


Figure 23: 3-State Buffers Implement a Multiplexer

## Wide Edge Decoders

Dedicated decoder circuitry boosts the performance of wide decoding functions. When the address or data field is wider than the function generator inputs, FPGAs need multi-level decoding and are thus slower than PALs. XC4000 Series CLBs have nine inputs. Any decoder of up to nine inputs is, therefore, compact and fast. However, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems.

An XC4000 Series FPGA has four programmable decoders located on each edge of the device. The inputs to each decoder are any of the IOB I1 signals on that edge plus one local interconnect per CLB row or column. Each row or column of CLBs provides up to three variables or their complements., as shown in Figure 24. Each decoder generates a High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to a product term in typical PAL devices.

Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005E and 72 on the XC4013E. There are up to 96 inputs for each decoder on the XC4028X and 132 on the XC4052X. The decoders may also be split in two when a larger number of narrower decoders are required, for a maximum of 32 decoders per device.

The decoder outputs can drive CLB inputs, so they can be combined with other logic to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of older FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 Series device can implement these functions fast and efficiently.

To use the wide edge decoders, place one or more of the WAND library symbols (WAND1, WAND4, WAND8, WAND16). Attach a DECODE attribute or property to each WAND symbol. Tie the outputs together and attach a PUL-

LUP symbol. Location attributes or properties such as L (left edge) or TR (right half of top edge) should also be used to ensure the correct placement of the decoder inputs.

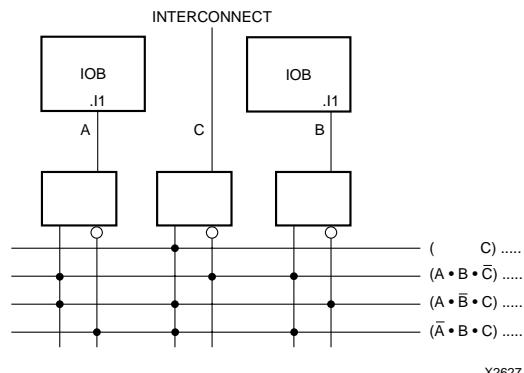


Figure 24: XC4000 Series Edge Decoding Example

## OSC4

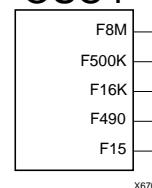


Figure 25: XC4000 Series Oscillator Symbol

## On-Chip Oscillator

XC4000 Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration modes. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16kHz, 490Hz and 15Hz (up to 10% lower for low-voltage devices). These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code (see [Figure 25](#)).

The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

## Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing resources is provided to achieve efficient automated routing.

The XC4000E and XC4000X share a basic interconnect structure. XC4000X devices, however, have additional routing not available in the XC4000E. The extra routing resources allow high utilization in high-capacity devices. All XC4000X-specific routing resources are clearly identified throughout this section. Any resources not identified as XC4000X-specific are present in all XC4000 Series devices.

This section describes the varied routing resources available in XC4000 Series devices. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design.

## Interconnect Overview

There are several types of interconnect.

- CLB routing is associated with each row and column of the CLB array.
- IOB routing forms a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the internal logic blocks.

- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

Five interconnect types are distinguished by the relative length of their segments: single-length lines, double-length lines, quad and octal lines (XC4000X only), and longlines. In the XC4000X, direct connects allow fast data flow between adjacent CLBs, and between IOBs and CLBs.

Extra routing is included in the IOB pad ring. The XC4000X also includes a ring of octal interconnect lines near the IOBs to improve pin-swapping and routing to locked pins.

XC4000E/X devices include two types of global buffers. These global buffers have different properties, and are intended for different purposes. They are discussed in detail later in this section.

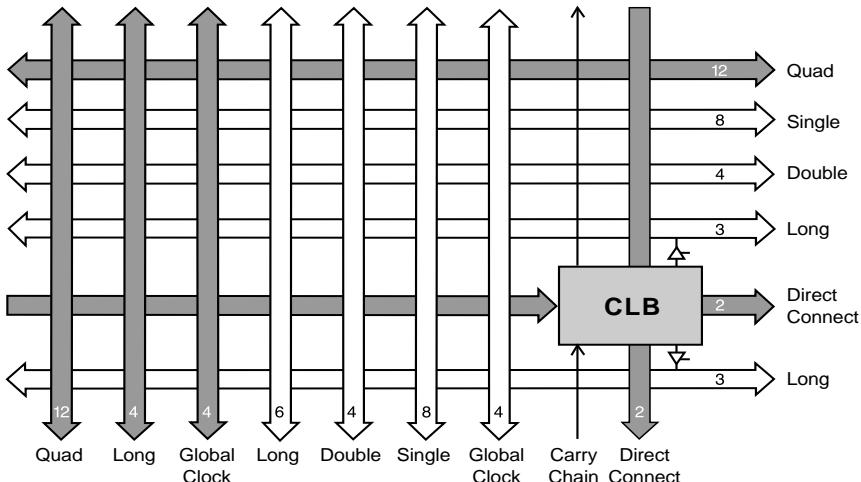
## CLB Routing Connections

A high-level diagram of the routing resources associated with one CLB is shown in [Figure 26](#). The shaded arrows represent routing present only in XC4000X devices.

[Table 15](#) shows how much routing of each type is available in XC4000E and XC4000X CLB arrays. Clearly, very large designs, or designs with a great deal of interconnect, will route more easily in the XC4000X. Smaller XC4000E designs, typically requiring significantly less interconnect, do not require the additional routing.

[Figure 28 on page 4-31](#) is a detailed diagram of both the XC4000E and the XC4000X CLB, with associated routing. The shaded square is the programmable switch matrix, present in both the XC4000E and the XC4000X. The L-shaped shaded area is present only in XC4000X devices. As shown in the figure, the XC4000X block is essentially an XC4000E block with additional routing.

CLB inputs and outputs are distributed on all four sides, providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.



x5994

Figure 26: High-Level Routing Diagram of XC4000 Series CLB (shaded arrows indicate XC4000X only)

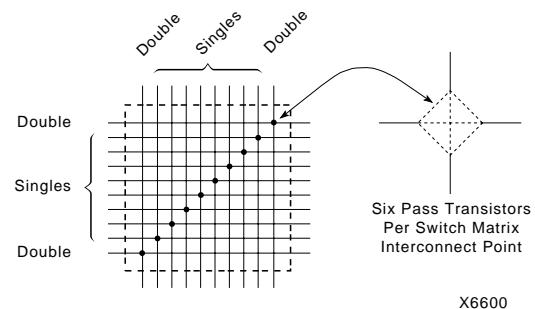
Table 15: Routing per CLB in XC4000 Series Devices

	XC4000E		XC4000X	
	Vertical	Horizontal	Vertical	Horizontal
Singles	8	8	8	8
Doubles	4	4	4	4
Quads	0	0	12	12
Longlines	6	6	10	6
Direct Connects	0	0	2	2
Globals	4	0	8	0
Carry Logic	2	0	1	0
Total	24	18	45	32

### Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each switch matrix consists of programmable pass transistors used to establish connections between the lines (see [Figure 27](#)).

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.



x6600

Figure 27: Programmable Switch Matrix (PSM)

### Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and a column of CLBs.

Single-length lines are connected by way of the programmable switch matrices, as shown in [Figure 29](#). Routing connectivity is shown in [Figure 28](#).

Single-length lines incur a delay whenever they go through a switching matrix. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

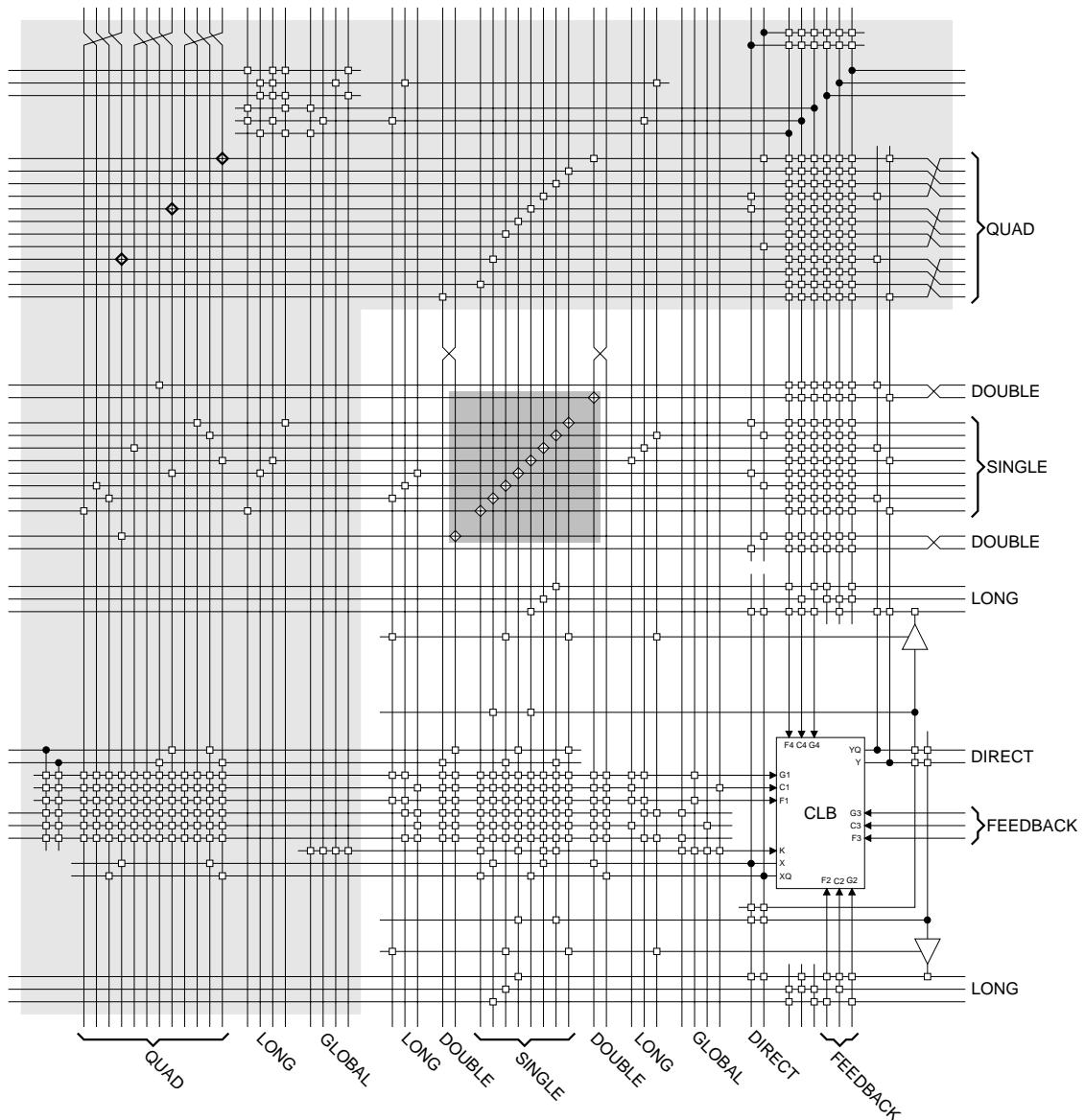
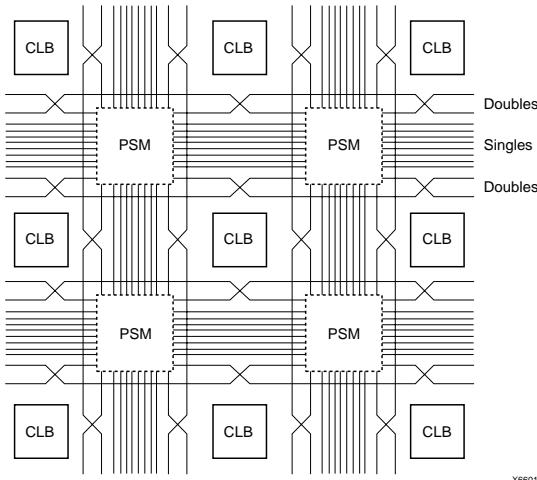


Figure 28: Detail of Programmable Interconnect Associated with XC4000 Series CLB



**Figure 29: Single- and Double-Length Lines, with Programmable Switch Matrices (PSMs)**

### Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a switch matrix. Double-length lines are grouped in pairs with the switch matrices staggered, so that each line goes through a switch matrix at every other row or column of CLBs (see [Figure 29](#)).

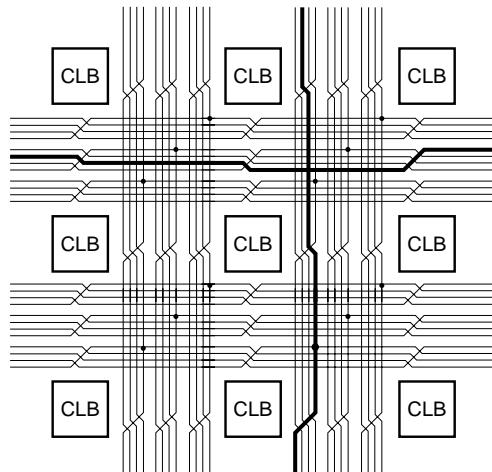
There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility. Double-length lines are connected by way of the programmable switch matrices. Routing connectivity is shown in [Figure 28](#).

### Quad Lines (XC4000X only)

XC4000X devices also include twelve vertical and twelve horizontal quad lines per CLB row and column. Quad lines are four times as long as the single-length lines. They are interconnected via buffered switch matrices (shown as diamonds in [Figure 28 on page 4-31](#)). Quad lines run past four CLBs before entering a buffered switch matrix. They are grouped in fours, with the buffered switch matrices staggered, so that each line goes through a buffered switch matrix at every fourth CLB location in that row or column. (See [Figure 30](#).)

The buffered switch matrices have four pins, one on each edge. All of the pins are bidirectional. Any pin can drive any or all of the other pins.

Each buffered switch matrix contains one buffer and six pass transistors. It resembles the programmable switch matrix shown in [Figure 27](#), with the addition of a programmable buffer. There can be up to two independent inputs



**Figure 30: Quad Lines (XC4000X only)**

and up to two independent outputs. Only one of the independent inputs can be buffered.

The place and route software automatically uses the timing requirements of the design to determine whether or not a quad line signal should be buffered. A heavily loaded signal is typically buffered, while a lightly loaded one is not. One scenario is to alternate buffers and pass transistors. This allows both vertical and horizontal quad lines to be buffered at alternating buffered switch matrices.

Due to the buffered switch matrices, quad lines are very fast. They provide the fastest available method of routing heavily loaded signals for long distances across the device.

### Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances. In XC4000X devices, quad lines are preferred for critical nets, because the buffered switch matrices make them faster for high fan-out nets.

Two horizontal longlines per CLB can be driven by 3-state or open-drain drivers (TBUFs). They can therefore implement unidirectional or bidirectional buses, wide multiplexers, or wired-AND functions. (See “[Three-State Buffers](#)” on [page 4-27](#) for more details.)

Each horizontal longline driven by TBUFs has either two (XC4000E) or eight (XC4000X) pull-up resistors. To activate these resistors, attach a PULLUP symbol to the longline net. The software automatically activates the appropriate number of pull-ups. There is also a weak keeper at each end of these two horizontal longlines. This circuit pre-

vents undefined floating levels. However, it is overridden by any driver, even a pull-up resistor.

Each XC4000E longline has a programmable splitter switch at its center, as does each XC4000X longline driven by TBUFs. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Each XC4000X longline not driven by TBUFs has a buffered programmable splitter switch at the 1/4, 1/2, and 3/4 points of the array. Due to the buffering, XC4000X longline performance does not deteriorate with the larger array sizes. If the longline is split, the resulting partial longlines are independent.

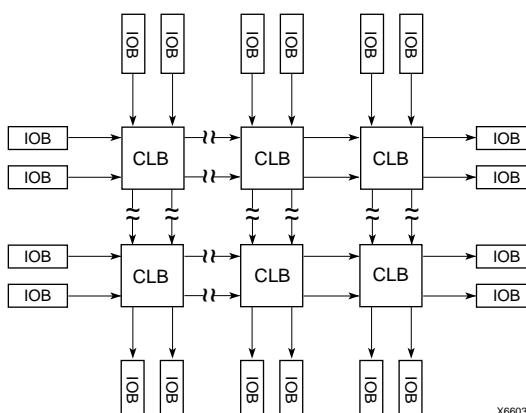
Routing connectivity of the longlines is shown in [Figure 28 on page 4-31](#).

### **Direct Interconnect (XC4000X only)**

The XC4000X offers two direct, efficient and fast connections between adjacent CLBs. These nets facilitate a data flow from the left to the right side of the device, or from the top to the bottom, as shown in [Figure 31](#). Signals routed on the direct interconnect exhibit minimum interconnect propagation delay and use no general routing resources.

The direct interconnect is also present between CLBs and adjacent IOBs. Each IOB on the left and top device edges has a direct path to the nearest CLB. Each CLB on the right and bottom edges of the array has a direct path to the nearest two IOBs, since there are two IOBs for each row or column of CLBs.

The place and route software uses direct interconnect whenever possible, to maximize routing resources and minimize interconnect delays.



**Figure 31: XC4000X Direct Interconnect**

## **I/O Routing**

XC4000 Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines spanning two CLBs (four IOBs), and four longlines. Global lines and Wide Edge Decoder lines are provided. XC4000X devices also include eight octal lines.

A high-level diagram of the VersaRing is shown in [Figure 32](#). The shaded arrows represent routing present only in XC4000X devices.

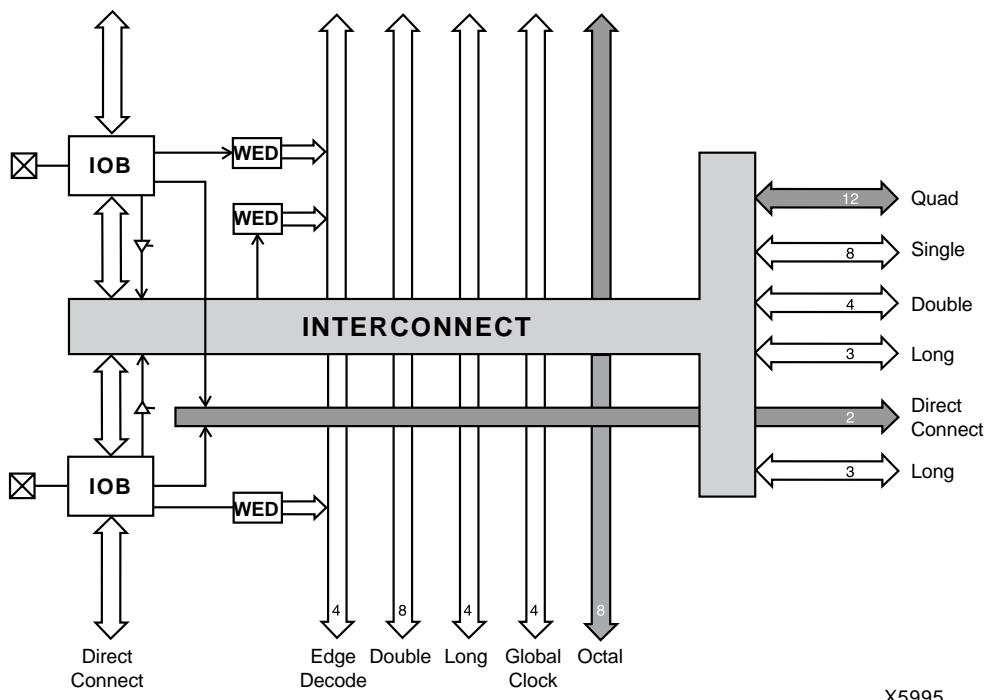
[Figure 34 on page 4-35](#) is a detailed diagram of the XC4000E and XC4000X VersaRing. The area shown includes two IOBs. There are two IOBs per CLB row or column, therefore this diagram corresponds to the CLB routing diagram shown in [Figure 28 on page 4-31](#). The shaded areas represent routing and routing connections present only in XC4000X devices.

### **Octal I/O Routing (XC4000X only)**

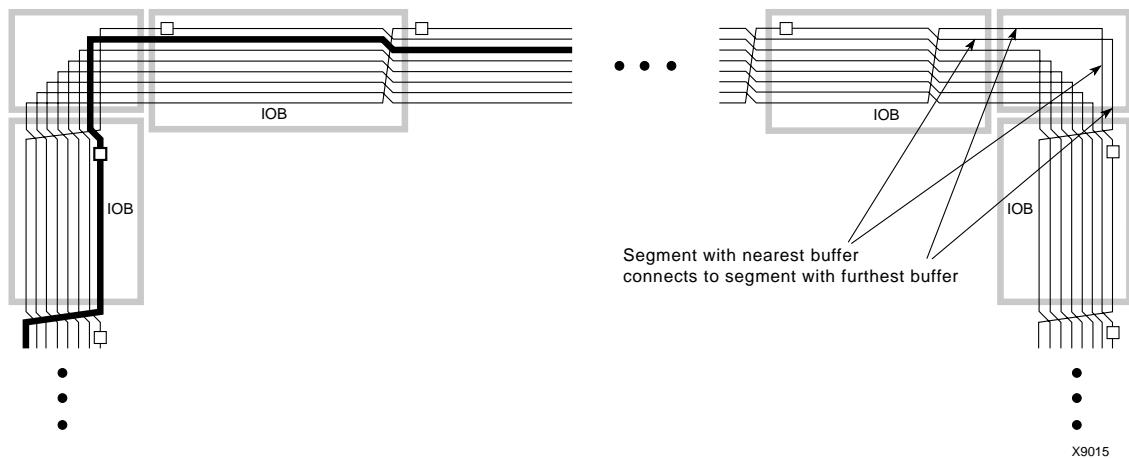
Between the XC4000X CLB array and the pad ring, eight interconnect tracks provide for versatility in pin assignment and fixed pinout flexibility. (See [Figure 33 on page 4-34](#).)

These routing tracks are called octals, because they can be broken every eight CLBs (sixteen IOBs) by a programmable buffer that also functions as a splitter switch. The buffers are staggered, so each line goes through a buffer at every eighth CLB location around the device edge.

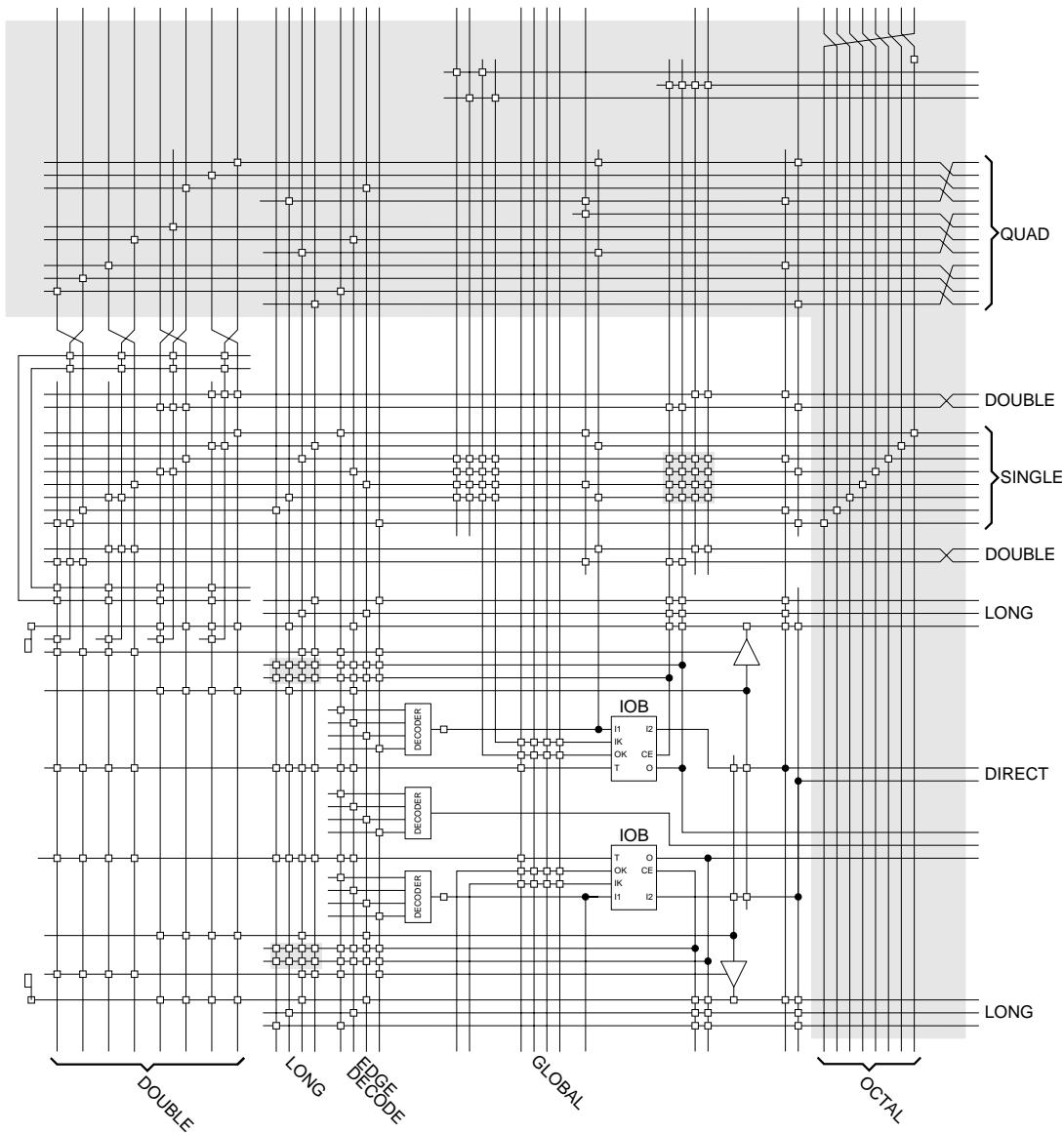
The octal lines bend around the corners of the device. The lines cross at the corners in such a way that the segment most recently buffered before the turn has the farthest distance to travel before the next buffer, as shown in [Figure 33](#).



**Figure 32: High-Level Routing Diagram of XC4000 Series VersaRing (Left Edge)**  
**WED = Wide Edge Decoder, IOB = I/O Block (shaded arrows indicate XC4000X only)**



**Figure 33: XC4000X Octal I/O Routing**



- Common to XC4000E and XC4000X
- XC4000X only

Figure 34: Detail of Programmable Interconnect Associated with XC4000 Series IOB (Left Edge)

IOB inputs and outputs interface with the octal lines via the single-length interconnect lines. Single-length lines are also used for communication between the octals and double-length lines, quads, and longlines within the CLB array.

Segmentation into buffered octals was found to be optimal for distributing signals over long distances around the device.

## Global Nets and Buffers

Both the XC4000E and the XC4000X have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew. The global buffers are described in detail in the following sections. The text descriptions and diagrams are summarized in [Table 16](#). The table shows which CLB and IOB clock pins can be sourced by which global buffers.

In both XC4000E and XC4000X devices, placement of a library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. The detailed information in these sections is included only for reference.

### Global Nets and Buffers (XC4000E only)

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The four global lines can be driven by either of two types of global buffers. The clock pins of every CLB and IOB can also be sourced from local interconnect.

Two different types of clock buffers are available in the XC4000E:

- Primary Global Buffers (BUFGP)
- Secondary Global Buffers (BUFGS)

Four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs.

The Primary Global buffers must be driven by the semi-dedicated pads. The Secondary Global buffers can be sourced by either semi-dedicated pads or internal nets.

Each CLB column has four dedicated vertical Global lines. Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in [Figure 35](#). Each corner of the device has one Primary buffer and one Secondary buffer.

IOBs along the left and right edges have four vertical global longlines. Top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), or BUFG (either primary or secondary buffer) element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=L attribute or property to a BUFGS symbol to direct that a buffer be placed in one of the two Secondary Global buffers on the left edge of the device, or a LOC=BL to indicate the Secondary Global buffer on the bottom edge of the device, on the left.

**Table 16: Clock Pin Access**

	XC4000E		XC4000X			Local Inter-connect
	BUFGP	BUFGS	BUFGS	L & R BUFGE	T & B BUFGE	
All CLBs in Quadrant	✓	✓	✓	✓	✓	✓
All CLBs in Device	✓	✓	✓			✓
IOBs on Adjacent Vertical Half Edge	✓	✓	✓	✓	✓	✓
IOBs on Adjacent Vertical Full Edge	✓	✓	✓	✓		✓
IOBs on Adjacent Horizontal Half Edge (Direct)				✓		✓
IOBs on Adjacent Horizontal Half Edge (through CLB globals)	✓	✓	✓	✓	✓	✓
IOBs on Adjacent Horizontal Full Edge (through CLB globals)	✓	✓	✓			✓

L = Left, R = Right, T = Top, B = Bottom

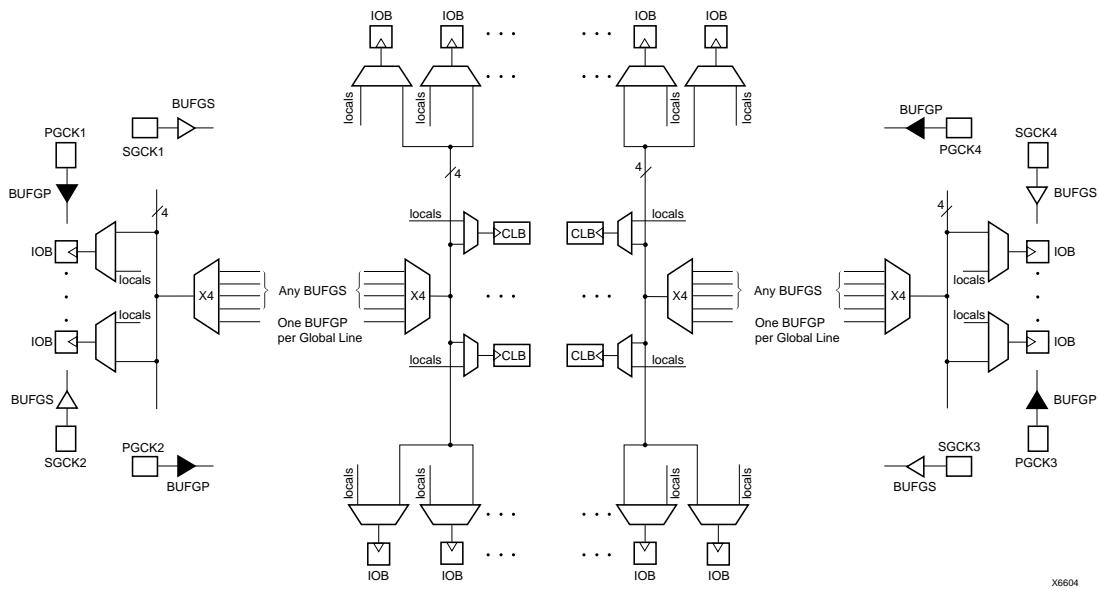


Figure 35: XC4000E Global Net Distribution

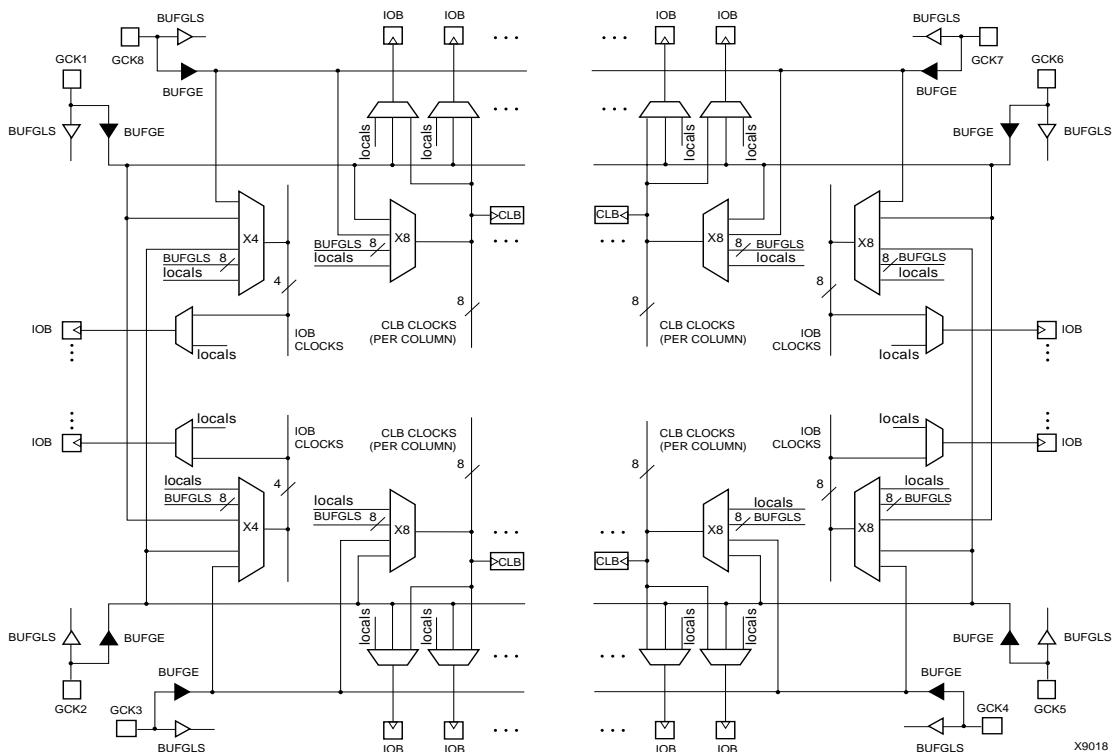


Figure 36: XC4000X Global Net Distribution

## Global Nets and Buffers (XC4000X only)

Eight vertical longlines in each CLB column are driven by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. The global lines are broken in the center of the array, to allow faster distribution and to minimize skew across the whole array. Each half-column global line has its own buffered multiplexer, as shown in [Figure 36](#). The top and bottom global lines cannot be connected across the center of the device, as this connection might introduce unacceptable skew. The top and bottom halves of the global lines must be separately driven — although they can be driven by the same global buffer.

The eight global lines in each CLB column can be driven by either of two types of global buffers. They can also be driven by internal logic, because they can be accessed by single, double, and quad lines at the top, bottom, half, and quarter points. Consequently, the number of different clocks that can be used simultaneously in an XC4000X device is very large.

There are four global lines feeding the IOBs at the left edge of the device. IOBs along the right edge have eight global lines. There is a single global line along the top and bottom edges with access to the IOBs. All IOB global lines are broken at the center. They cannot be connected across the center of the device, as this connection might introduce unacceptable skew.

IOB global lines can be driven from two types of global buffers, or from local interconnect. Alternatively, top and bottom IOBs can be clocked from the global lines in the adjacent CLB column.

Two different types of clock buffers are available in the XC4000X:

- Global Low-Skew Buffers (BUFGLS)
- Global Early Buffers (BUFGE)

Global Low-Skew Buffers are the standard clock buffers. They should be used for most internal clocking, whenever a large portion of the device must be driven.

Global Early Buffers are designed to provide a faster clock access, but CLB access is limited to one-fourth of the device. They also facilitate a faster I/O interface.

[Figure 36](#) is a conceptual diagram of the global net structure in the XC4000X.

Global Early buffers and Global Low-Skew buffers share a single pad. Therefore, the same IPAD symbol can drive one buffer of each type, in parallel. This configuration is particularly useful when using the Fast Capture latches, as described in ["IOB Input Signals" on page 4-21](#). Paired Global Early and Global Low-Skew buffers share a common input; they cannot be driven by two different signals.

## Choosing an XC4000X Clock Buffer

The clocking structure of the XC4000X provides a large variety of features. However, it can be simple to use, without understanding all the details. The software automatically handles clocks, along with all other routing, when the appropriate clock buffer is placed in the design. In fact, if a buffer symbol called BUFG is placed, rather than a specific type of buffer, the software even chooses the buffer most appropriate for the design. The detailed information in this section is provided for those users who want a finer level of control over their designs.

If fine control is desired, use the following summary and [Table 16 on page 4-36](#) to choose an appropriate clock buffer.

- The simplest thing to do is to use a Global Low-Skew buffer.
- If a faster clock path is needed, try a BUFG. The software will first try to use a Global Low-Skew Buffer. If timing requirements are not met, a faster buffer will automatically be used.
- If a single quadrant of the chip is sufficient for the clocked logic, and the timing requires a faster clock than the Global Low-Skew buffer, use a Global Early buffer.

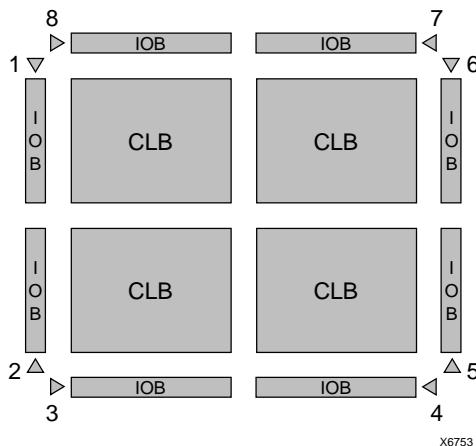
### Global Low-Skew Buffers

Each corner of the XC4000X device has two Global Low-Skew buffers. Any of the eight Global Low-Skew buffers can drive any of the eight vertical Global lines in a column of CLBs. In addition, any of the buffers can drive any of the four vertical lines accessing the IOBs on the left edge of the device, and any of the eight vertical lines accessing the IOBs on the right edge of the device. (See [Figure 37 on page 4-39](#).)

IOBs at the top and bottom edges of the device are accessed through the vertical Global lines in the CLB array, as in the XC4000E. Any Global Low-Skew buffer can, therefore, access every IOB and CLB in the device.

The Global Low-Skew buffers can be driven by either semi-dedicated pads or internal logic.

To use a Global Low-Skew buffer, instantiate a BUFGLS element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGLS be placed in one of the two Global Low-Skew buffers on the top edge of the device, or a LOC=TR to indicate the Global Low-Skew buffer on the top edge of the device, on the right.



**Figure 37: Any BUFGLS (GCK1 - GCK8) Can Drive Any or All Clock Inputs on the Device**

### Global Early Buffers

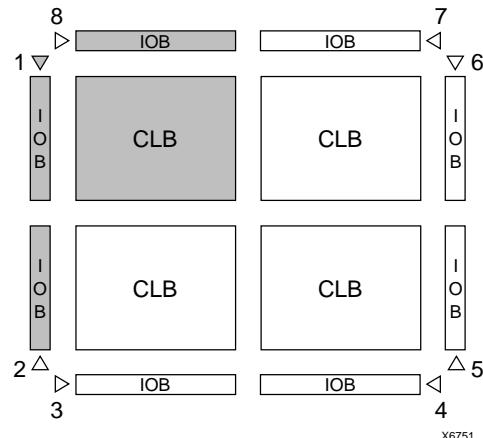
Each corner of the XC4000X device has two Global Early buffers. The primary purpose of the Global Early buffers is to provide an earlier clock access than the potentially heavily-loaded Global Low-Skew buffers. A clock source applied to both buffers will result in the Global Early clock edge occurring several nanoseconds earlier than the Global Low-Skew buffer clock edge, due to the lighter loading.

Global Early buffers also facilitate the fast capture of device inputs, using the Fast Capture latches described in “[IOB Input Signals](#)” on page 4-21. For Fast Capture, take a single clock signal, and route it through both a Global Early buffer and a Global Low-Skew buffer. (The two buffers share an input pad.) Use the Global Early buffer to clock the Fast Capture latch, and the Global Low-Skew buffer to clock the normal input flip-flop or latch, as shown in [Figure 18](#) on page 4-24.

The Global Early buffers can also be used to provide a fast Clock-to-Out on device output pins. However, an early clock in the output flip-flop IOB must be taken into consideration when calculating the internal clock speed for the design.

The Global Early buffers at the left and right edges of the chip have slightly different capabilities than the ones at the top and bottom. Refer to [Figure 38](#), [Figure 39](#), and [Figure 36](#) on page 4-37 while reading the following explanation.

Each Global Early buffer can access the eight vertical Global lines for all CLBs in the quadrant. Therefore, only one-fourth of the CLB clock pins can be accessed. This restriction is in large part responsible for the faster speed of the buffers, relative to the Global Low-Skew buffers.

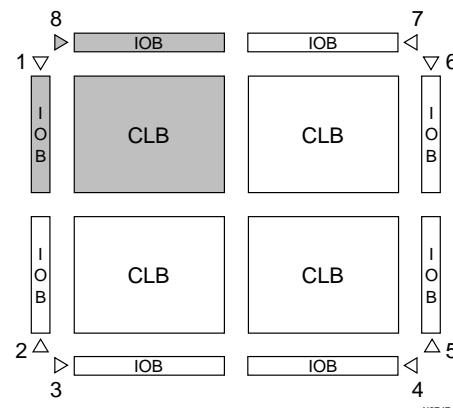


**Figure 38: Left and Right BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant or Edge (GCK1 is shown. GCK2, GCK5 and GCK6 are similar.)**

The left-side Global Early buffers can each drive two of the four vertical lines accessing the IOBs on the entire left edge of the device. The right-side Global Early buffers can each drive two of the eight vertical lines accessing the IOBs on the entire right edge of the device. (See [Figure 38](#).)

Each left and right Global Early buffer can also drive half of the IOBs along either the top or bottom edge of the device, using a dedicated line that can only be accessed through the Global Early buffers.

The top and bottom Global Early buffers can drive half of the IOBs along either the left or right edge of the device, as shown in [Figure 39](#). They can only access the top and bottom IOBs via the CLB global lines.



**Figure 39: Top and Bottom BUFGEs Can Drive Any or All Clock Inputs in Same Quadrant (GCK8 is shown. GCK3, GCK4 and GCK7 are similar.)**

The top and bottom Global Early buffers are about 1 ns slower clock to out than the left and right Global Early buffers.

The Global Early buffers can be driven by either semi-dedicated pads or internal logic. They share pads with the Global Low-Skew buffers, so a single net can drive both global buffers, as described above.

To use a Global Early buffer, place a BUFGE element in a schematic or in HDL code. If desired, attach a LOC attribute or property to direct placement to the designated location. For example, attach a LOC=T attribute or property to direct that a BUFGE be placed in one of the two Global Early buffers on the top edge of the device, or a LOC=TR to indicate the Global Early buffer on the top edge of the device, on the right.

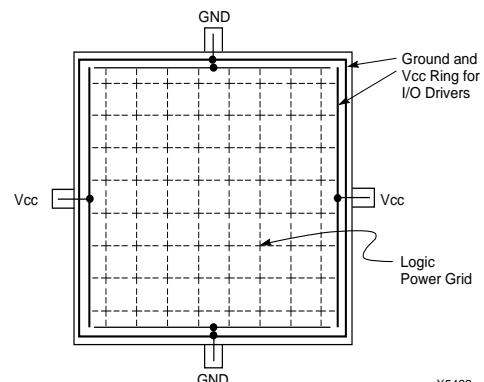
## Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in [Figure 40](#). An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1  $\mu$ F capacitor connected between each Vcc pin and the board's Ground plane will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 12 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.



**Figure 40: XC4000 Series Power Distribution**

## Pin Descriptions

There are three types of pins in the XC4000 Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with a 50 k $\Omega$  - 100 k $\Omega$  pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 50 k $\Omega$  - 100 k $\Omega$  pull-up resistor.

XC4000 Series devices have no dedicated Reset input. Any user I/O can be configured to drive the Global Set/Reset net, GSR. See ["Global Set/Reset" on page 4-11](#) for more information on GSR.

XC4000 Series devices have no Powerdown control input, as the XC3000 and XC2000 families do. The XC3000/XC2000 Powerdown control also 3-stated all of the device I/O pins. For XC4000 Series devices, use the global 3-state net, GTS, instead. This net 3-states all outputs, but does not place the device in low-power mode. See ["IOB Output Signals" on page 4-24](#) for more information on GTS.

Device pins for XC4000 Series devices are described in [Table 17](#). Pin functions during configuration for each of the seven configuration modes are summarized in [Table 23 on page 4-59](#), in the "Configuration Timing" section.

**Table 17: Pin Descriptions**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
<b>Permanently Dedicated Pins</b>			
VCC	I	I	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for low-voltage devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 $\mu$ F capacitor to Ground.
GND	I	I	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode and Synchronous Peripheral mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on XC4000 Series devices, except during Readback. See “Violating the Maximum High and Low Time Specification for the Readback Clock” on page 4-57 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the XACTstep program that creates the configuration bitstream. The resistor is included by default.
PROGRAM	I	I	PROGRAM is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT. The PROGRAM pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
<b>User I/O Pins That Can Have Special Functions</b>			
RDY/BUSY	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/BUSY is a user-programmable I/O pin. RDY/BUSY is pulled High with a high-impedance pull-up prior to INIT going High.
RCLK	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs (A0 - A21 for XC4000X) is preceded by a rising edge on RCLK, a redundant output signal. RCLK is useful for clocked PROMs. It is rarely used during configuration. After configuration, RCLK is a user-programmable I/O pin.
M0, M1, M2	I	I (M0), O (M1), I (M2)	As Mode inputs, these pins are sampled after INIT goes High to determine the configuration mode to be used. After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. The three mode inputs can be individually configured with or without weak pull-up or pull-down resistors. A pull-down resistor value of 4.7 k $\Omega$ is recommended. These pins can only be used as inputs or outputs when called out by special schematic definitions. To use these pins, place the library components MD0, MD1, and MD2 instead of the usual pad symbols. Input or output buffers must still be used.
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

Table 17: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{LDC}$	O	I/O	Low During Configuration ( $\overline{LDC}$ ) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin.
$\overline{INIT}$	I/O	I/O	Before and during configuration, $\overline{INIT}$ is a bidirectional signal. A $1\text{ k}\Omega$ - $10\text{ k}\Omega$ external pull-up resistor is recommended. As an active-Low open-drain output, $\overline{INIT}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 $\mu\text{s}$ after $\overline{INIT}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin.
PGCK1 - PGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (XC4000E only)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (XC4000X only)	Weak Pull-up	I or I/O	Eight inputs can each drive a Global Low-Skew buffer. In addition, each can drive a Global Early buffer. Each pair of global buffers can also be driven from internal logic, but must share an input signal. If not used to drive a global buffer, any of these pins is a user-programmable I/O. Any input pad symbol connected directly to the input of a BUFGLS or BUFGE symbol is automatically placed on one of these pins.
$\overline{CS0}$ , CS1, WS, RS	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when $\overline{CS0}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ( $\overline{WS}$ ) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe ( $\overline{RS}$ ) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. WS and RS should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
A0 - A17	O	I/O	During Master Parallel configuration, these 18 output pins address the configuration EPROM. After configuration, they are user-programmable I/O pins.

**Table 17: Pin Descriptions (Continued)**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
A18 - A21 (XC4000X only)	O	I/O	During Master Parallel configuration with an XC4000X master, these 4 output pins add 4 more bits to address the configuration EPROM. After configuration, they are user-programmable I/O pins. (See Master Parallel Configuration section for additional details.)
D0 - D7	I	I/O	During Master Parallel and Peripheral configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
<b>Unrestricted User-Programmable I/O Pins</b>			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (25 kΩ - 100 kΩ) that defines the logic level as High.

## Boundary Scan

The ‘bed of nails’ has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The XC4000 Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin,

a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: “*Boundary Scan in XC4000 Devices*.”

[Figure 41 on page 4-44](#) shows a simplified block diagram of the XC4000E Input/Output Block with boundary scan implemented. XC4000X boundary scan logic is identical.

[Figure 42 on page 4-45](#) is a diagram of the XC4000 Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

XC4000 Series devices can also be configured through the boundary scan logic. See “[Readback](#)” on page 4-56.

## Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

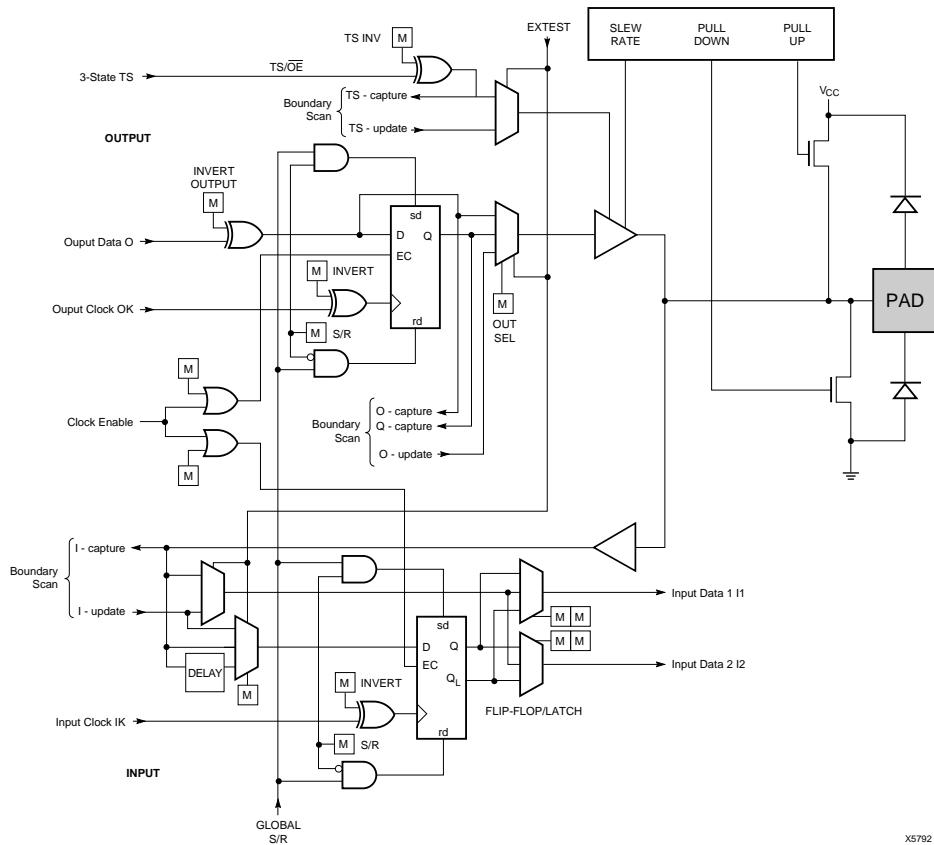
The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is

always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

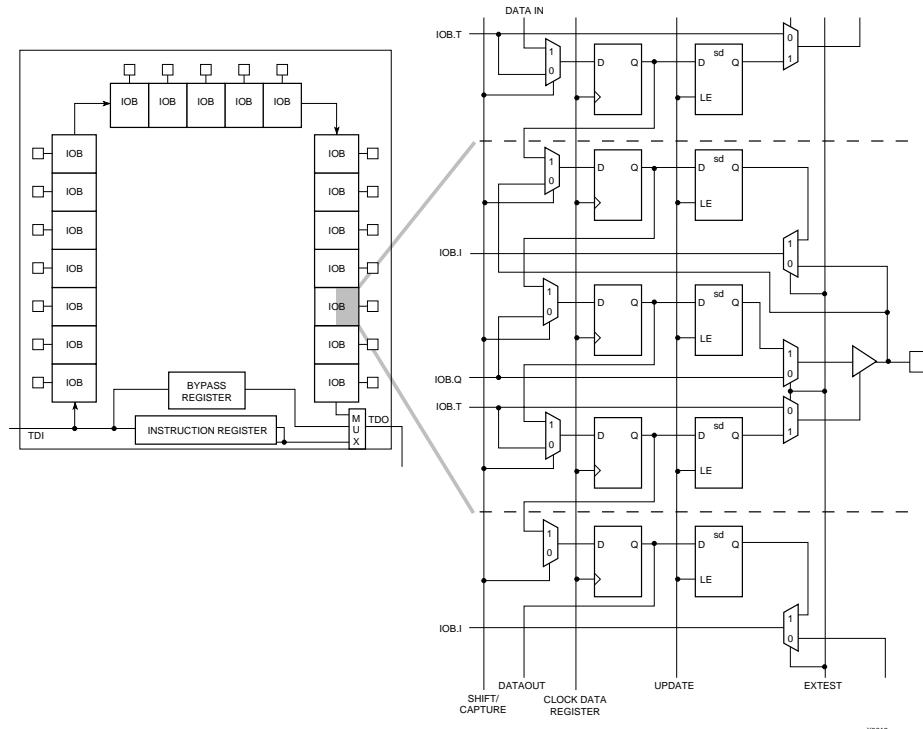
The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides

two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).



X5792

**Figure 41: Block Diagram of XC4000E IOB with Boundary Scan (some details not shown). XC4000X Boundary Scan Logic is Identical.**



**Figure 42: XC4000 Series Boundary Scan Logic**

## Instruction Set

The XC4000 Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in [Table 18](#).

## Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only M0 and M2 mode pins contribute only the In bit to the boundary scan I/O data register, while the output-only M1 pin contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in [Figure 43](#). The device-specific pinout tables for the XC4000 Series include the boundary scan locations for each IOB pin.

BSDL (Boundary Scan Description Language) files for XC4000 Series devices are available on the Xilinx FTP site.

## Including Boundary Scan in a Schematic

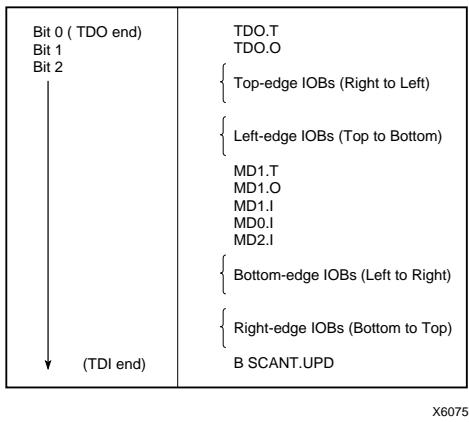
If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in [Figure 44](#).

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

**Table 18: Boundary Scan Instructions**

Instruction I2 I1 I0	Test Selected	TDO Source	I/O Data Source
0 0 0	EXTEST	DR	DR
0 0 1	SAMPLE/ PRELOAD	DR	Pin/Logic
0 1 0	USER 1	BSCAN. TDO1	User Logic
0 1 1	USER 2	BSCAN. TDO2	User Logic
1 0 0	READBACK	Readback Data	Pin/Logic
1 0 1	CONFIGURE	DOUT	Disabled
1 1 0	Reserved	—	—
1 1 1	BYPASS	Bypass Register	—

**Figure 43: Boundary Scan Bit Sequence**

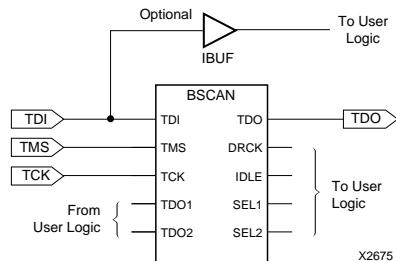
## Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—don't toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017.001, “Boundary Scan in XC4000E Devices.”

**Figure 44: Boundary Scan Schematic Example**

## Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC4000 Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT-step development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

## Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary connections. M2 and M0 can be used as inputs, and M1 can be used as an output. The XACT-step development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC4000 Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

## Configuration Modes

XC4000E devices have six configuration modes. XC4000X devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chained devices. The coding for mode selection is shown in [Table 19](#).

**Table 19: Configuration Modes**

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Reserved	0	1	0	—	—
Reserved	0	0	1	—	—

Note: \* Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in [Table 23 on page 4-59](#).

### Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFF (3FFFFFF when 22 address lines are used), for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

### Additional Address lines in XC4000 devices

The XC4000X devices have additional address lines (A18-A21) allowing the additional address space required to daisy-chain several large devices.

The extra address lines are programmable in XC4000EX devices. By default these address lines are not activated. In the default mode, the devices are compatible with existing XC4000 and XC4000E products. If desired, the extra address lines can be used by specifying the address lines option in bitgen as 22 (bitgen -g AddressLines:22). The lines (A18-A21) are driven when a master device detects, via the bitstream, that it should be using all 22 address lines. Because these pins will initially be pulled high by internal pull-ups, designers using Master Parallel Up mode should use external pull down resistors on pins A18-A21. If Master Parallel Down mode is used external resistors are not necessary.

All 22 address lines are always active in Master Parallel modes with XC4000XL devices. The additional address lines behave identically to the lower order address lines. If the Address Lines option in bitgen is set to 18, it will be ignored by the XC4000XL device.

The additional address lines (A18-A21) are not available in the PC84 package.

### Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

### Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

### Serial Daisy Chain

Multiple devices with different configurations can be connected together in a “daisy chain,” and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in [Figure 52 on page 4-61](#). Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count,

is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. [Figure 48 on page 4-54](#) shows the start-up timing for an XC4000 Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

### Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, and XC4000 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000 Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in [Figure 48 on page 4-54](#). Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of [Figure 48](#). The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC4000 Series device, not reaching F means that readback cannot be ini-

tiated and most boundary scan instructions cannot be used.

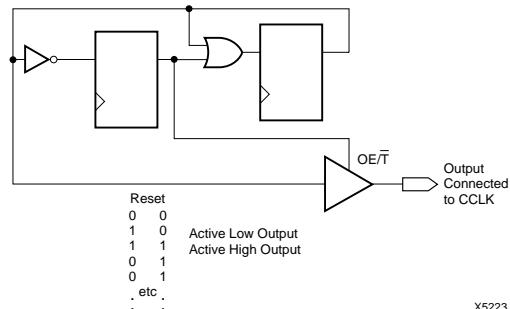
The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

### XC3000 Master with an XC4000 Series Slave

Some designers want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000 Series devices all available for user I/O. [Figure 45](#) provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC4000 Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.



**Figure 45: CCLK Generation for XC3000 Master Driving an XC4000 Series Slave**

## Setting CCLK Frequency

For Master modes, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for XC4000E and XC4000EX devices and from 0.6 MHz to 1.8 MHz for XC4000XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for XC4000EX devices and from 5 MHz to 15 MHz for XC4000XL devices. The frequency is selected by an option when running the bitstream generation software. If an XC4000 Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. In addition, an XC4000XL device driving a XC4000E or XC4000EX should use slow mode. Slow mode is the default.

**Table 20: XC4000 Series Data Stream Formats**

Data Type	All Other Modes (D0...)
Fill Byte	11111111b
Preamble Code	0010b
Length Count	COUNT(23:0)
Fill Bits	1111b
Start Field	0b
Data Frame	DATA(n-1:0)
CRC or Constant Field Check	xxxx (CRC) or 0110b
Extend Write Cycle	—
Postamble	01111111b
Start-Up Bytes	xxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

## Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes.

The data stream formats are shown in [Table 20](#). Bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones. This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see [Table 21](#) and [Table 22](#)). Each frame begins with a start field and ends with an error check. A postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the INIT pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect INIT and initialize a new configuration by pulsing the PROGRAM pin Low or cycling Vcc.

**Table 21: XC4000E Program Data**

Device	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E
<b>Max Logic Gates</b>	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
<b>CLBs (Row x Col.)</b>	100 (10 x 10)	196 (14 x 14)	256 (16 x 16)	324 (18 x 18)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)
<b>IOBs</b>	80	112	128	144	160	192	224	256
<b>Flip-Flops</b>	360	616	768	936	1,120	1,536	2,016	2,560
<b>Bits per Frame</b>	126	166	186	206	226	266	306	346
<b>Frames</b>	428	572	644	716	788	932	1,076	1,220
<b>Program Data</b>	53,936	94,960	119,792	147,504	178,096	247,920	329,264	422,128
<b>PROM Size (bits)</b>	53,984	95,008	119,840	147,552	178,144	247,968	329,312	422,176

Notes: 1. Bits per Frame =  $(10 \times \text{number of rows}) + 7$  for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits

Number of Frames =  $(36 \times \text{number of columns}) + 26$  for the left edge + 41 for the right edge + 1

Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits

PROM Size = Program Data + 40 (header) + 8

2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.

**Table 22: XC4000EX/XL Program Data**

Device	XC4005	XC4010	XC4013	XC4020	XC4028	XC4036	XC4044	XC4052	XC4062	XC4085
<b>Max Logic Gates</b>	5,000	10,000	13,000	20,000	28,000	36,000	44,000	52,000	62,000	85,000
<b>CLBs (Row x Column)</b>	196 (14 x 14)	400 (20 x 20)	576 (24 x 24)	784 (28 x 28)	1,024 (32 x 32)	1,296 (36 x 36)	1,600 (40 x 40)	1,936 (44 x 44)	2,304 (48 x 48)	3,136 (56 x 56)
<b>IOBs</b>	112	160	192	224	256	288	320	352	384	448
<b>Flip-Flops</b>	616	1,120	1,536	2,016	2,560	3,168	3,840	4,576	5,376	7,168
<b>Bits per Frame</b>	205	277	325	373	421	469	517	565	613	709
<b>Frames</b>	741	1,023	1,211	1,399	1,587	1,775	1,963	2,151	2,339	2,715
<b>Program Data</b>	151,910	283,376	393,580	521,832	668,132	832,480	1,014,876	1,215,320	1,433,812	1,924,940
<b>PROM Size (bits)</b>	151,960	283,424	393,632	521,880	668,184	832,528	1,014,928	1,215,368	1,433,864	1,924,992

Notes: 1. Bits per frame =  $(12 \times \text{number of rows}) + 8$  for the top + 16 for the bottom + 8 + 1 start bit + 4 error check bits.

Frames =  $(47 \times \text{number of columns}) + 27$  for the left edge + 52 for the right edge + 4.

Program data = (bits per frame x number of frames) + 5 postamble bits.

PROM size = (program data + 40 header bits + 8 start bits) rounded up to the nearest byte.

2. The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading "ones" at the beginning of the header.

## Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system

performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in [Table 20](#). If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 46. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

## Configuration Sequence

There are four major steps in the XC4000 Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 47.

### Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms, and up to 10% longer in the low-voltage devices. The delay is four times as long when in Master Modes (M0 Low), to allow ample time for all slaves to reach a stable Vcc. When all INIT pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the PROGRAM pin

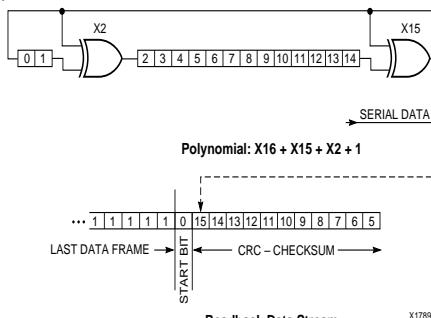


Figure 46: Circuit for Generating CRC-16

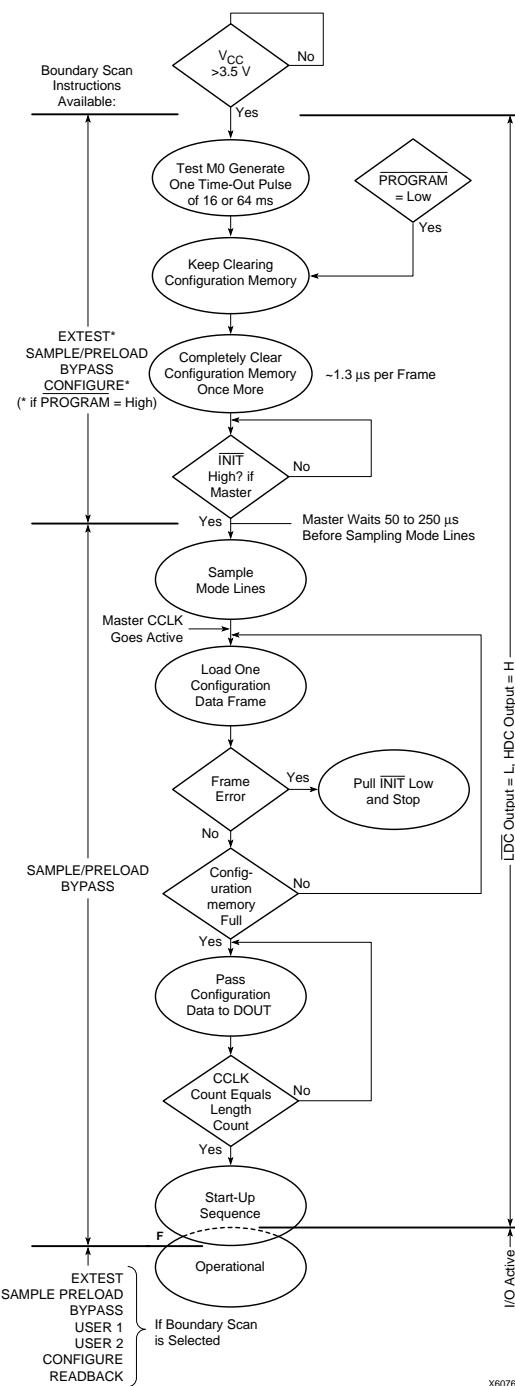


Figure 47: Power-up Configuration Sequence

Low. During this time delay, or as long as the PROGRAM input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the PROGRAM pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the INIT input.

### **Initialization**

During initialization and configuration, user pins HDC, LDC, INIT and DONE provide status outputs for the system interface. The outputs LDC, INIT and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain INIT pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250  $\mu$ s (up to 10% longer for low-voltage devices) before a Master-mode device recognizes an inactive INIT. Two internal clocks after the INIT pin is recognized as High, the FPGA samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded. Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain INIT pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device.

### **Delaying Configuration After Power-Up**

There are two methods of delaying configuration after power-up: put a logic Low on the PROGRAM input, or pull the bidirectional INIT pin Low, using an open-collector (open-drain) driver. (See [Figure 47 on page 4-51](#).)

A Low on the PROGRAM input is the more radical approach, and is recommended when the power-supply

rise time is excessive or poorly defined. As long as PROGRAM is Low, the FPGA keeps clearing its configuration memory. When PROGRAM goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the PROGRAM input automatically forces a Low on the INIT output. The XC4000 Series PROGRAM pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold INIT Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When INIT is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250  $\mu$ s to make sure that any slaves in the optional daisy chain have seen that INIT is High.

### **Start-Up**

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic ‘wakes up’ gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

[Figure 48](#) describes start-up timing for the three Xilinx families in detail. The configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

### **Start-up Timing**

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000 Series offers additional flexibility. The three events — DONE going High, the internal Set/Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in [Figure 48](#), but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

XC4000 Series offers another start-up clocking option, UCLK\_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK\_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bit-stream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

### Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks

received since INIT went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in [Figure 49](#). Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

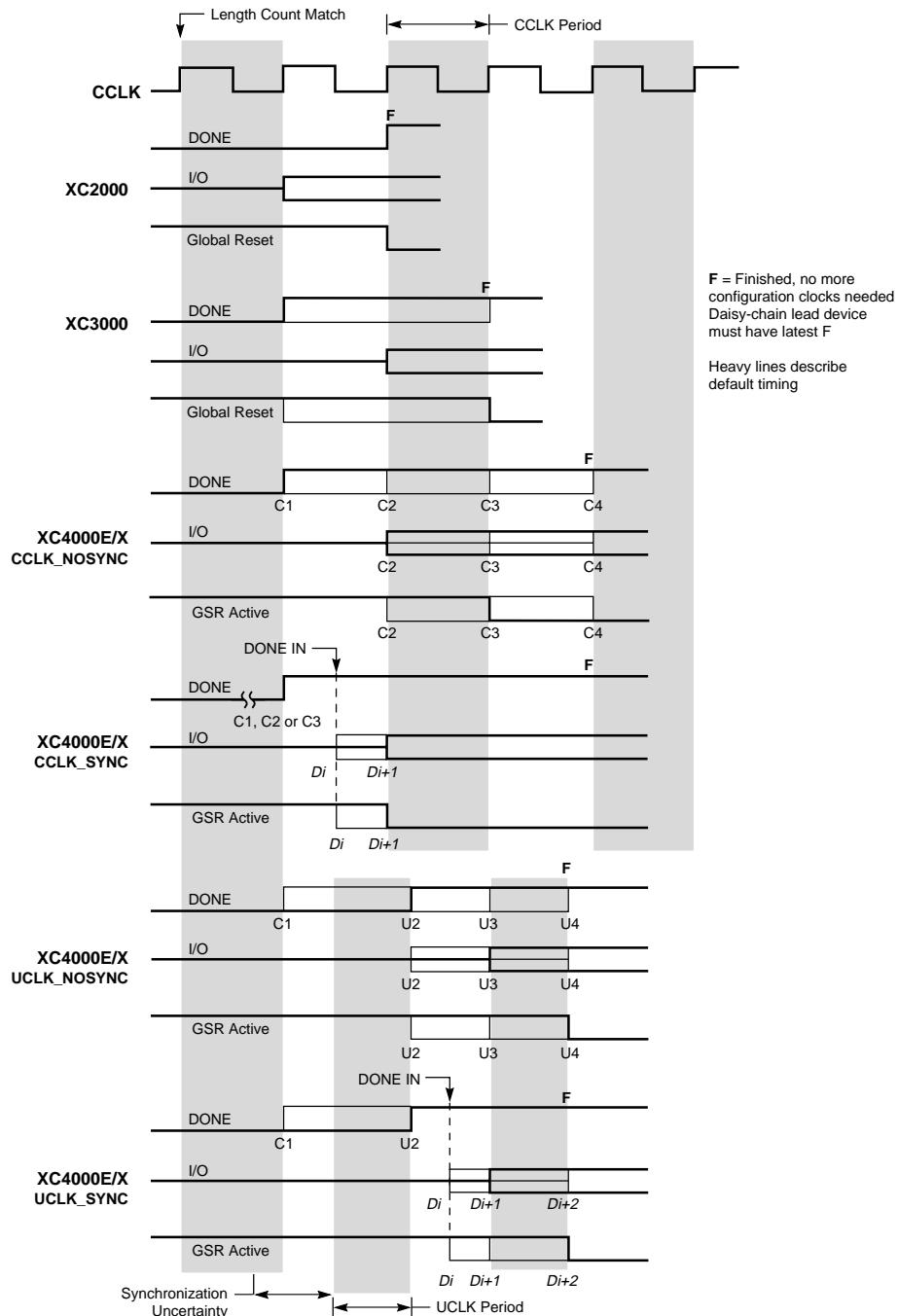
The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK\_SYNC or UCLK\_SYNC.

When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK\_NOSYNC or UCLK\_NOSYNC.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

### Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in [Figure 48](#) show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.



X9024

Figure 48: Start-up Timing

## Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

## DONE Goes High to Signal End of Configuration

XC4000 Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly*.

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [ $2^{24} * \text{CCLK period}$ ] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value. The *XACT User Guide* includes detailed information about manually altering the length count.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

## Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 50 kΩ - 100 kΩ pull-up. The delay from DONE High to active user I/O is controlled by an option to the bitstream generation software.

## Release of Global Set/Reset After DONE Goes High

By default, Global Set/Reset (GSR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial set or reset state. The delay from DONE High to GSR inactive is controlled by an option to the bitstream generation software.

## Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in [Figure 48 on page 4-54](#). If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

## Configuration Through the Boundary Scan Pins

XC4000 Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.
- Issue the CONFIG command to the TMS input
- Wait for INIT to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note XAPP017, "Boundary Scan in XC4000 Devices." This application note also applies to XC4000E and XC4000X devices.

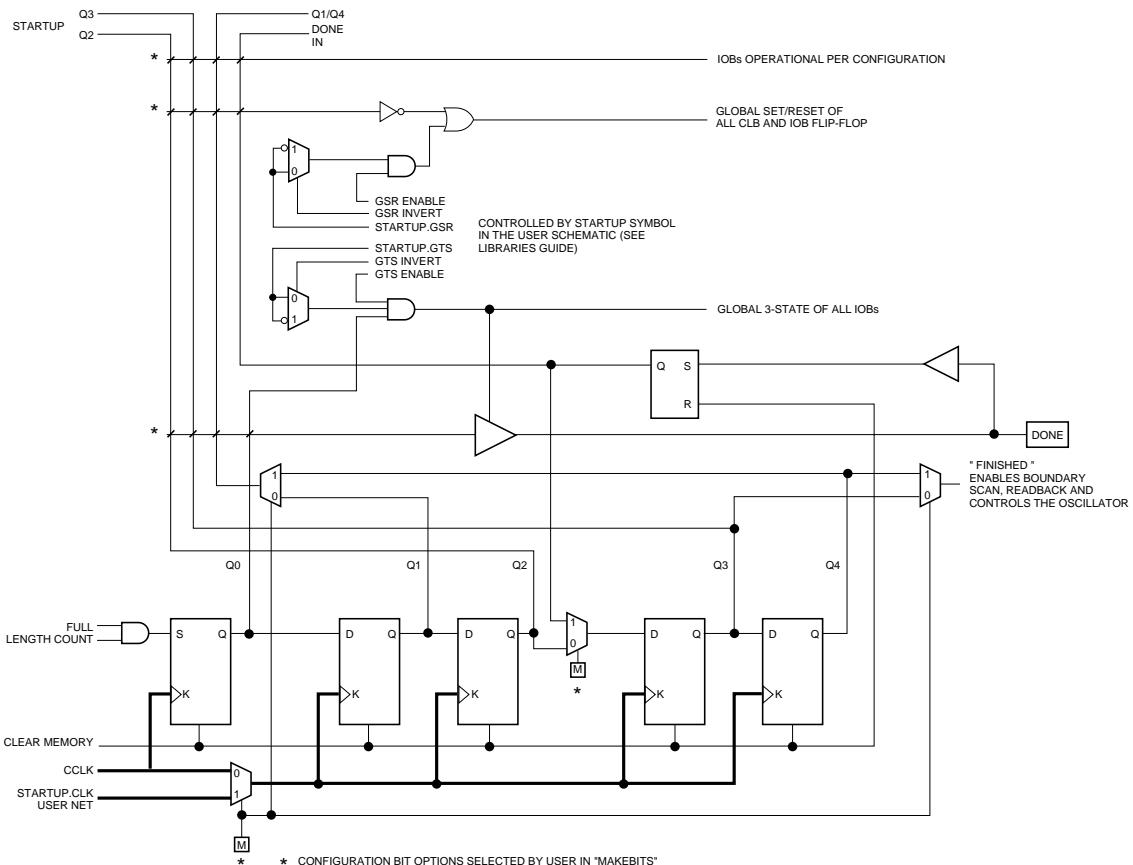


Figure 49: Start-up Logic

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Note that in XC4000 Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

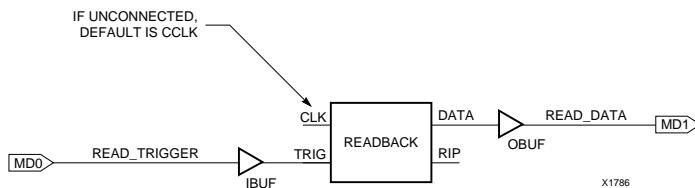
XC4000 Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback sig-

nals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 50.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.



**Figure 50: Readback Schematic Example**

## Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with the bitstream generation software.

### Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals are inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

RDBK.TRIG is located in the lower-left corner of the device, as shown in [Figure 51](#).

### Read Abort

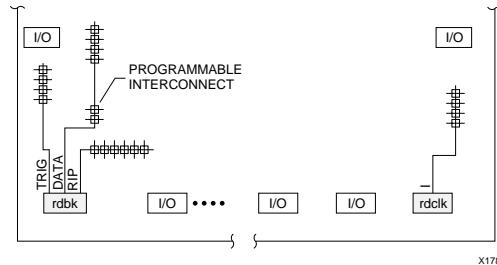
When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

### Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

RDBK.CLK is located in the lower right chip corner, as shown in [Figure 51](#).



**Figure 51: READBACK Symbol in Graphical Editor**

## Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 20](#), [Table 21](#) and [Table 22](#).

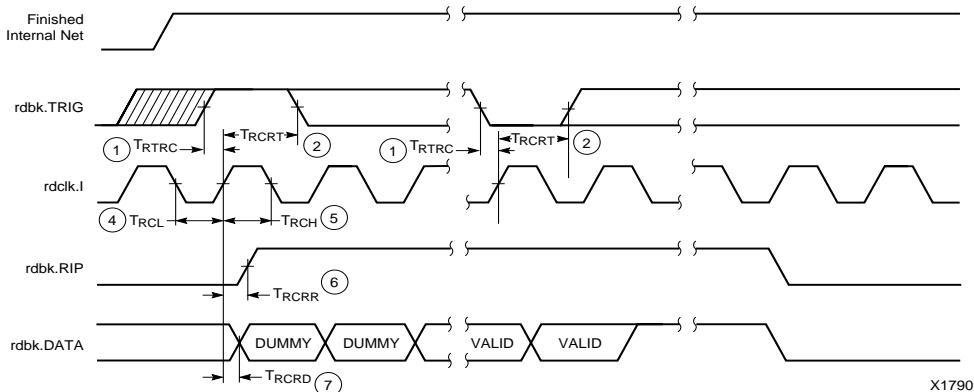
## Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

## XC4000E/EX/XL Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



### E/EX

	Description	Symbol	Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1 $T_{RTRC}$	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2 $T_{RCRT}$	50	-	ns
rdclk.1	rdbk.DATA delay	7 $T_{RCRD}$	-	250	ns
	rdbk.RIP delay	6 $T_{RCRR}$	-	250	ns
	High time	5 $T_{RCH}$	250	500	ns
	Low time	4 $T_{RCL}$	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

### XL

	Description	Symbol	Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1 $T_{RTRC}$	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2 $T_{RCRT}$	50	-	ns
rdclk.1	rdbk.DATA delay	7 $T_{RCRD}$	-	250	ns
	rdbk.RIP delay	6 $T_{RCRR}$	-	250	ns
	High time	5 $T_{RCH}$	250	500	ns
	Low time	4 $T_{RCL}$	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

**Table 23: Pin Functions During Configuration**

CONFIGURATION MODE < M2:M1:M0 >						
SLAVE SERIAL <1:1:1>	MASTER SERIAL <0:0:0>	SYNCH. PERIPHERAL <0:1:1>	ASYNCH. PERIPHERAL <1:0:1>	MASTER PARALLEL DOWN <1:1:0>	MASTER PARALLEL UP <1:0:0>	USER OPERATION
M2(HIGH) (I)	M2(LOW) (I)	M2(LOW) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(HIGH) (I)	(I)
M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	(O)
M0(HIGH) (I)	M0(LOW) (I)	M0(HIGH) (I)	M0(HIGH) (I)	M0(LOW) (I)	M0(LOW) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
INIT	INIT	INIT	INIT	INIT	INIT	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)
		RDY/BUSY (O)	RDY/BUSY (O)	RCLK (O)	RCLK (O)	I/O
			RS (I)			I/O
			CS0 (I)			I/O
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			WS (I)	A0	A0	I/O
				A1	A1	PGCK4-GCK6-I/O
			CS1	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGCK1-GCK7-I/O
				A16	A16	PGCK1-GCK8-I/O
				A17	A17	I/O
				A18*	A18*	I/O
				A19*	A19*	I/O
				A20*	A20*	I/O
				A21*	A21*	I/O
						ALL OTHERS

Table 24: Pin Functions During Configuration

CONFIGURATION MODE < M2:M1:M0 >						
SLAVE SERIAL <1:1:1>	MASTER SERIAL <0:0:0>	SYNCH. PERIPHERAL <0:1:1>	ASYNCH. PERIPHERAL <1:0:1>	MASTER PARALLEL DOWN <1:1:0>	MASTER PARALLEL UP <1:0:0>	USER OPERATION
M2(HIGH) (I)	M2(LOW) (I)	M2(LOW) (I)	M2(HIGH) (I)	M2(HIGH) (I)	M2(HIGH) (I)	(I)
M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1(HIGH) (I)	M1(LOW) (I)	(O)
M0(HIGH) (I)	M0(LOW) (I)	M0(HIGH) (I)	M0(HIGH) (I)	M0(LOW) (I)	M0(LOW) (I)	(I)
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
INIT	INIT	INIT	INIT	INIT	INIT	I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)
		RDY/BUSY (O)	RDY/BUSY (O)	RCLK (O)	RCLK (O)	I/O
			RS (I)			I/O
			CS0 (I)			I/O
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGCK4-GCK5-I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			WS (I)	A0	A0	I/O
				A1	A1	PGCK4-GCK6-I/O
			CS1	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGCK1-GCK7-I/O
				A16	A16	PGCK1-GCK8-I/O
				A17	A17	I/O
				A18*	A18*	I/O
				A19*	A19*	I/O
				A20*	A20*	I/O
				A21*	A21*	I/O
						ALL OTHERS

\* XC4000X only

Notes 1. A shaded table cell represents a 50 kΩ - 100 kΩ pull-up before and during configuration.

2. (I) represents an input; (O) represents an output.

3. INIT is an open-drain output during configuration.

## Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

### Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 52 shows a full master/slave system. An XC4000 Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

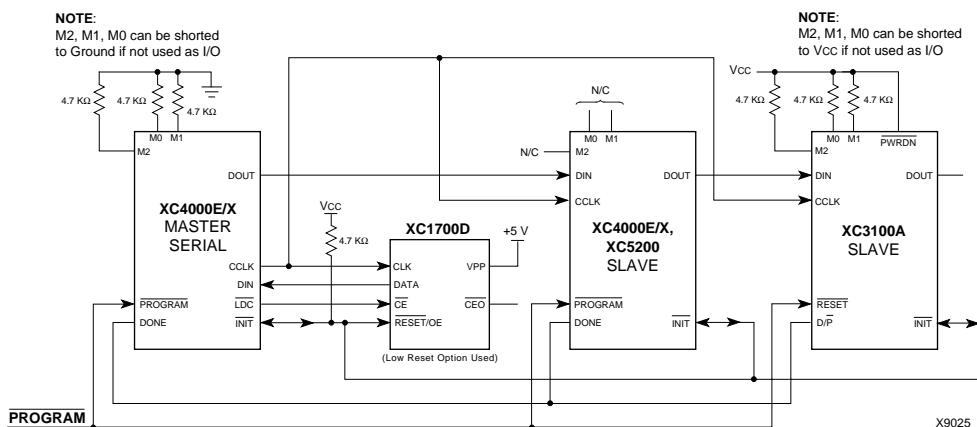
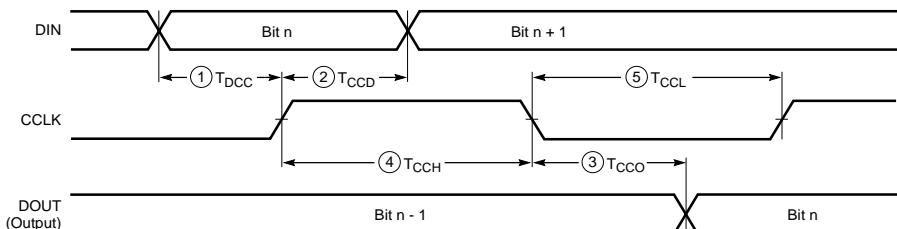


Figure 52: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1	T <sub>DCC</sub>	20	ns
	DIN hold	2	T <sub>CCD</sub>	0	ns
	DIN to DOUT	3	T <sub>CCO</sub>	30	ns
	High time	4	T <sub>CCH</sub>	45	ns
	Low time	5	T <sub>CCL</sub>	45	ns
	Frequency	F <sub>CC</sub>		10	MHz

Note: Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

Figure 53: Slave Serial Mode Programming Switching Characteristics

## Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

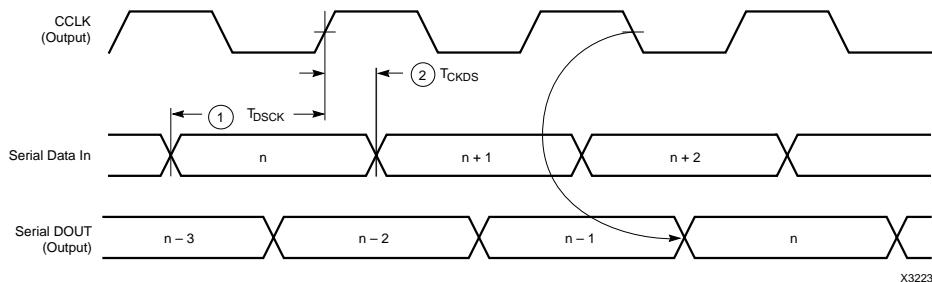
In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first

frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to “[Configuration Switching Characteristics](#)” on page 4-69. Be sure that the serial PROM and slaves are fast enough to support this data rate. XC2000, XC3000/A, and XC3100A devices do not support the Fast ConfigRate option.

The SPROM CE input can be driven from either  $\overline{\text{LDC}}$  or DONE. Using LDC avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but  $\overline{\text{LDC}}$  is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

[Figure 52 on page 4-61](#) shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1	$T_{DSCK}$	20	ns
	DIN hold	2	$T_{CKDS}$	0	ns

Notes:

- At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.
- Master Serial mode timing is based on testing in slave mode.

**Figure 54: Master Serial Mode Programming Switching Characteristics**

## Master Parallel Modes

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFF and decrement.

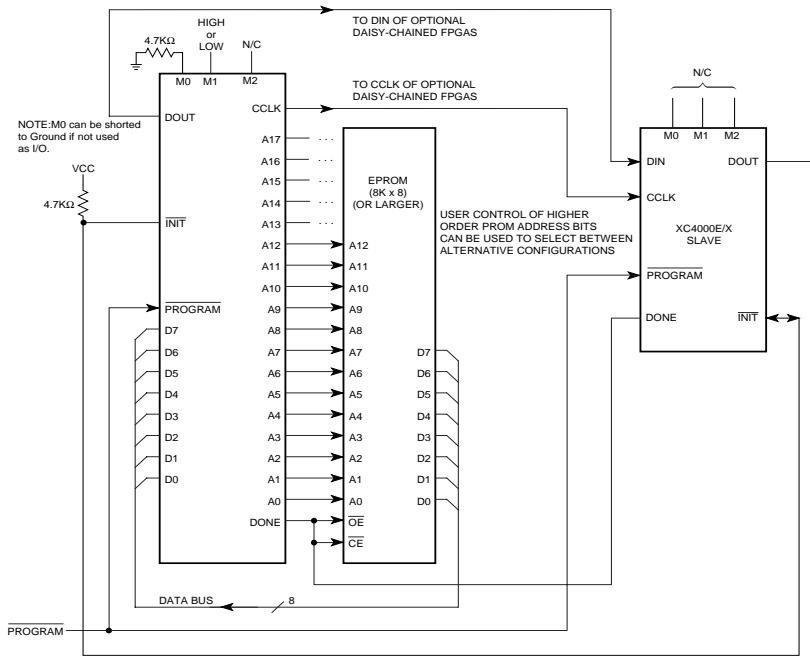
### Additional Address lines in XC4000 devices

The XC4000X devices have additional address lines (A18-A21) allowing the additional address space required to daisy-chain several large devices.

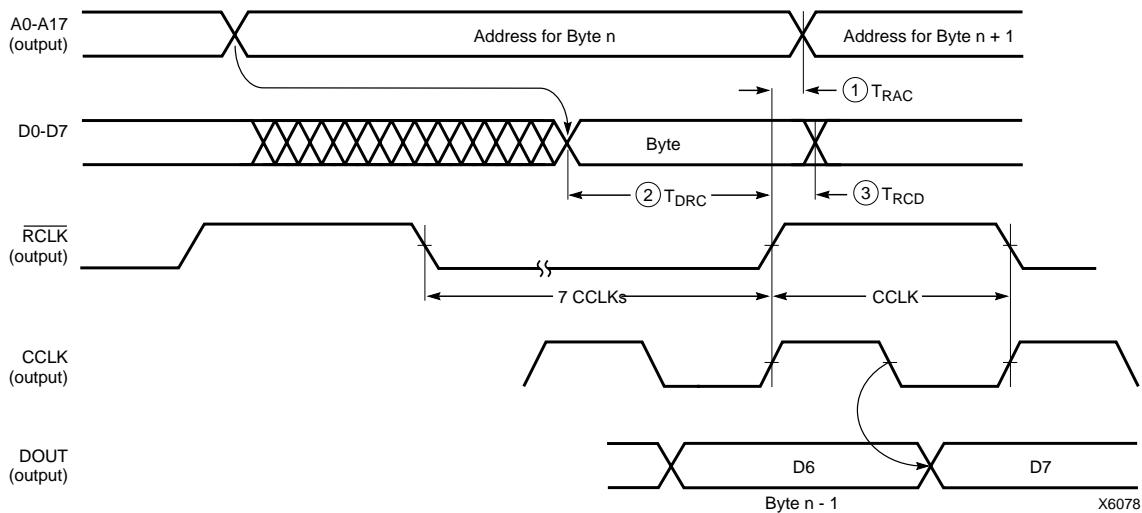
The extra address lines are programmable in XC4000EX devices. By default these address lines are not activated. In the default mode, the devices are compatible with existing XC4000 and XC4000E products. If desired, the extra address lines can be used by specifying the address lines option in bitgen as 22 (bitgen -g AddressLines:22). The lines (A18-A21) are driven when a master device detects, via the bitstream, that it should be using all 22 address lines. Because these pins will initially be pulled high by internal pull-ups, designers using Master Parallel Up mode should use external pull down resistors on pins A18-A21. If Master Parallel Down mode is used external resistors are not necessary.

All 22 address lines are always active in Master Parallel modes with XC4000XL devices. The additional address lines behave identically to the lower order address lines. If the Address Lines option in bitgen is set to 18, it will be ignored by the XC4000XL device.

The additional address lines (A18-A21) are not available in the PC84 package.



**Figure 55: Master Parallel Mode Circuit Diagram**



	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	$T_{RAC}$	0	200	ns
	Data setup time	2	$T_{DRC}$	60		ns
	Data hold time	3	$T_{RCD}$	0		ns

Notes:

- At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling **PROGRAM** Low until Vcc is valid.
- The first Data byte is loaded and CCLK starts at the end of the first  $\overline{\text{RCLK}}$  active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

**Figure 56: Master Parallel Mode Programming Switching Characteristics**

## Synchronous Peripheral Mode

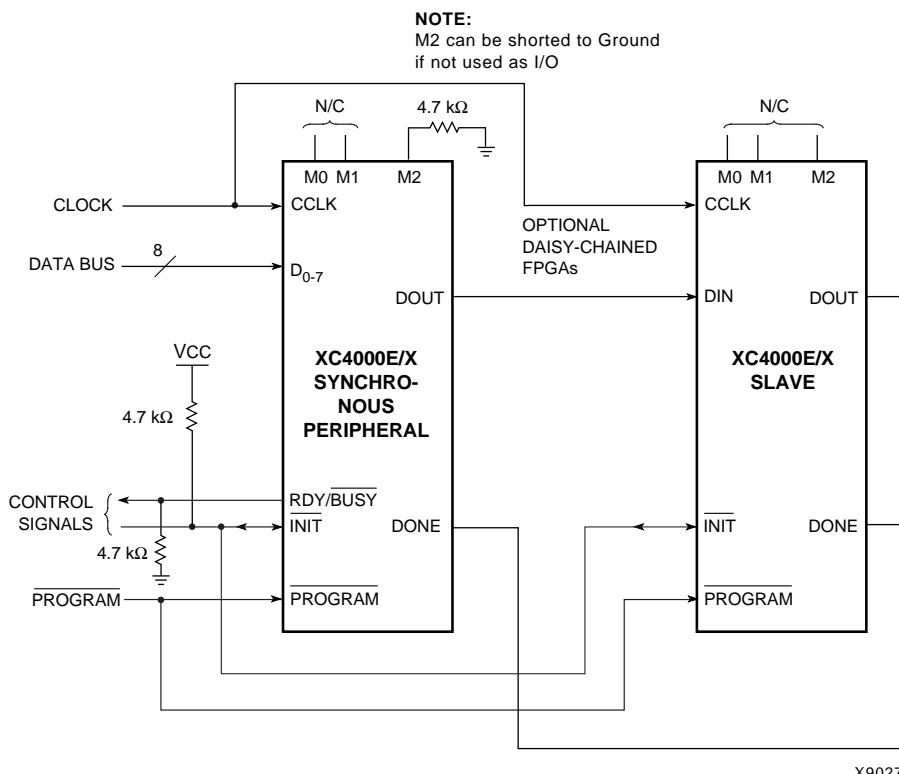
Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/**BUSY** output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/**BUSY** is pulled High with a high-impedance pullup prior to **INIT** going High.

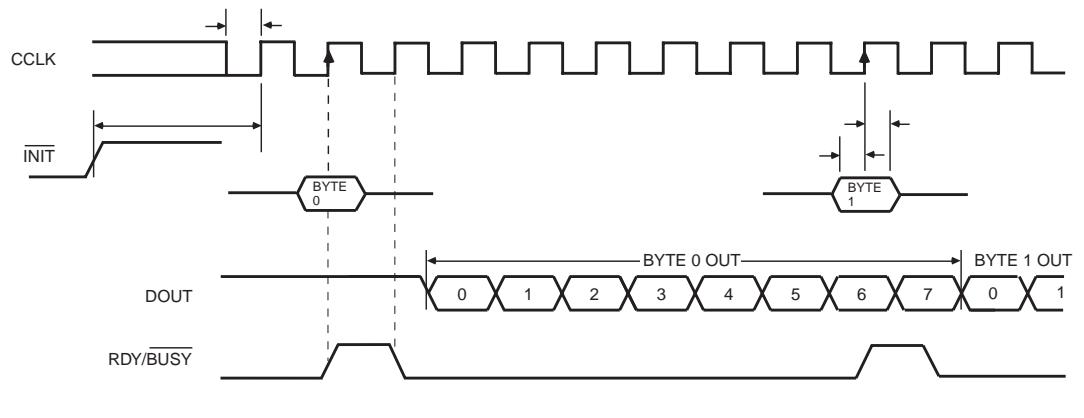
The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a `<011>` on the mode pins (M2, M1, M0).



**Figure 57: Synchronous Peripheral Mode Circuit Diagram**



X6096

	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	$T_{IC}$	5		$\mu s$
	D0 - D7 setup time	$T_{DC}$	60		ns
	D0 - D7 hold time	$T_{CD}$	0		ns
	CCLK High time	$T_{CCH}$	50		ns
	CCLK Low time	$T_{CCL}$	60		ns
	CCLK Frequency	$F_{CC}$		8	MHz

- Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
  2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
  3. The pin name RDY/BUSY is a misnomer. In Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.
  4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 58: Synchronous Peripheral Mode Programming Switching Characteristics

## Asynchronous Peripheral Mode

### Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of  $\overline{WS}$  and  $\overline{CS0}$  being Low and  $RS$  and  $CS1$  being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its  $DOUT$  pin. The  $RDY/BUSY$  output from the lead FPGA acts as a handshake signal to the microprocessor.  $RDY/BUSY$  goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the  $RDY/BUSY$  output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until  $RDY/BUSY$  is High again for one CCLK period. Note that  $RDY/BUSY$  is pulled High with a high-impedance pull-up prior to  $\overline{INIT}$  going High.

The length of the  $BUSY$  signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the  $BUSY$  signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the  $BUSY$  signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with  $DOUT$  equal to bit 6 (the next-to-last bit) of the last byte entered.

The  $READY/BUSY$  handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

### Status Read

The logic AND condition of the  $\overline{CS0}$ ,  $CS1$  and  $\overline{RS}$  inputs puts the device status on the Data bus.

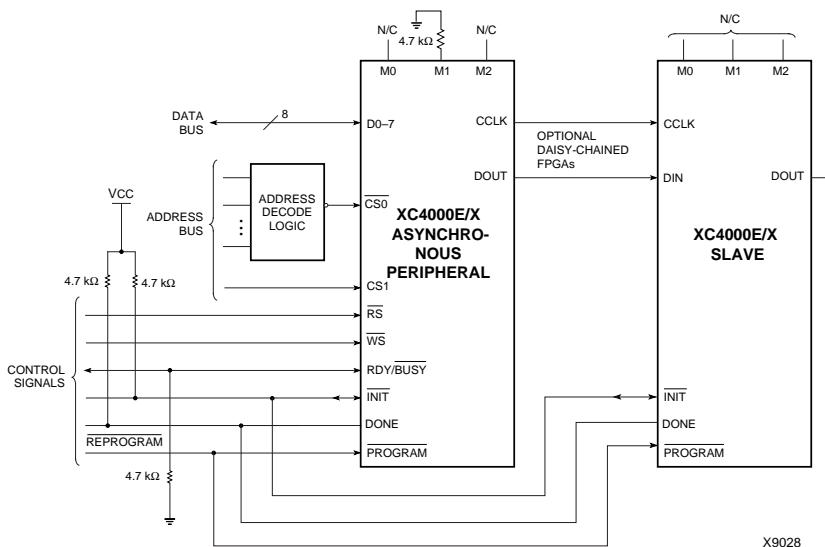
- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in [Figure 48 on page 4-54](#)).

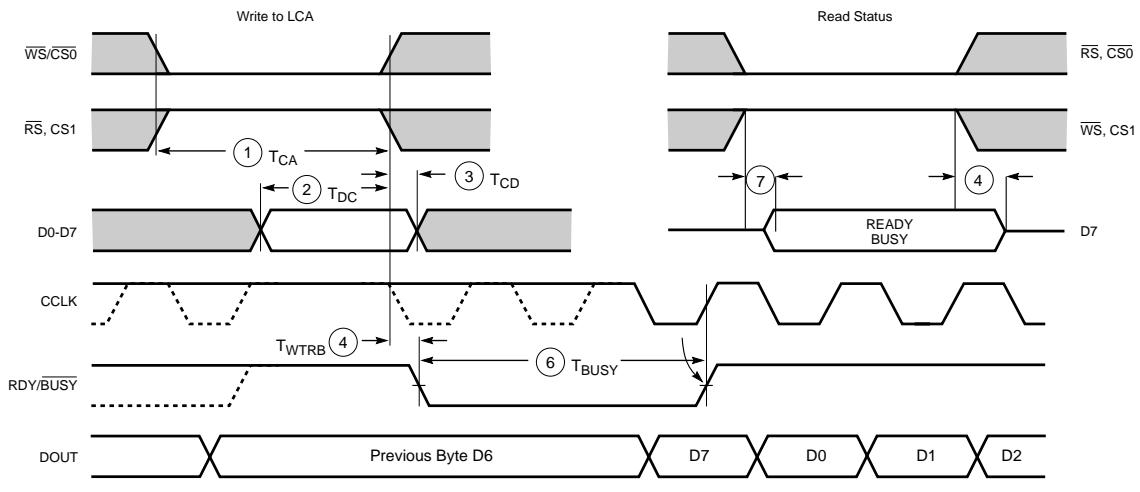
In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by the XACTstep software, ensures that these problems never occur.

Although  $RDY/BUSY$  is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the  $RDY/BUSY$  status when  $RS$  is Low,  $WS$  is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).



**Figure 59: Asynchronous Peripheral Mode Circuit Diagram**



X6097

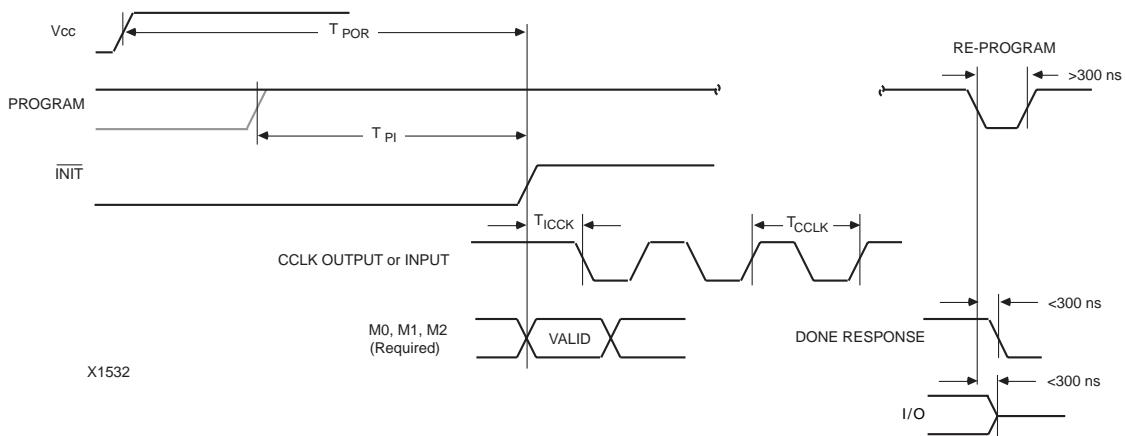
	Description	Symbol	Min	Max	Units
Write	Effective Write time ( $CS_0$ , $\overline{WS}$ =Low; $\overline{RS}$ , $CS_1$ =High)	1 $T_{CA}$	100		ns
	DIN setup time	2 $T_{DC}$	60		ns
	DIN hold time	3 $T_{CD}$	0		ns
RDY	RDY/BUSY delay after end of Write or Read	4 $T_{WTRB}$		60	ns
	RDY/BUSY active after beginning of Read	7		60	ns
	RDY/BUSY Low output (Note 4)	6 $T_{BUSY}$	2	9	CCLK periods

- Notes:
- Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.
  - The time from the end of  $\overline{WS}$  to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of the internal timing generator for CCLK.
  - CCLK and DOUT timing is tested in slave mode.
  - $T_{BUSY}$  indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest  $T_{BUSY}$  occurs when a byte is loaded into an empty parallel-to-serial converter. The longest  $T_{BUSY}$  occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of  $\overline{WS}$ . RDY/BUSY will go active within 60 ns after the end of  $\overline{WS}$ . A new write may be asserted immediately after RDY/BUSY goes Low, but write may not be terminated until RDY/BUSY has been High for one CCLK period.

**Figure 60: Asynchronous Peripheral Mode Programming Switching Characteristics**

## Configuration Switching Characteristics



### Master Modes (XC4000E/EX)

Description	Symbol	Min	Max	Units
Power-On Reset	$T_{POR}$	10	40	ms
	$T_{POR}$	40	130	ms
Program Latency	$T_{PI}$	1	4	$\mu\text{s}$ per CLB column
CCLK (output) Delay	$T_{ICCK}$	40	250	$\mu\text{s}$
CCLK (output) Period, slow	$T_{CCLK}$	640	2000	ns
CCLK (output) Period, fast	$T_{CCLK}$	80	250	ns

### Master Modes (XC4000XL)

Description	Symbol	Min	Max	Units
Power-On Reset	$T_{POR}$	10	40	ms
	$T_{POR}$	40	130	ms
Program Latency	$T_{PI}$	1	4	$\mu\text{s}$ per CLB column
CCLK (output) Delay	$T_{ICCK}$	40	250	$\mu\text{s}$
CCLK (output) Period, slow	$T_{CCLK}$	540	1600	ns
CCLK (output) Period, fast	$T_{CCLK}$	67	200	ns

### Slave and Peripheral Modes(All)

Description	Symbol	Min	Max	Units
Power-On Reset	$T_{POR}$	10	33	ms
Program Latency	$T_{PI}$	1	4	$\mu\text{s}$ per CLB column
CCLK (input) Delay (required)	$T_{ICCK}$	4		$\mu\text{s}$
CCLK (input) Period (required)	$T_{CCLK}$	100		ns

## XC4000XL Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered final.

All specifications subject to change without notice.

### Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

### Absolute Maximum Ratings

Symbol	Description		Units	
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V	
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V	
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V	
$V_{CCt}$	Longest Supply Voltage Rise Time from 1 V to 3V	50	ms	
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C	
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C	
$T_J$	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Except for pin-to-pin input and out

- Notes:
1. Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
  2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Recommended Operating Conditions

Symbol	Description		Min	Max	Unit s
$V_{CC}$	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	Industrial	3.0	3.6	V
$V_{IH}$	High-level input voltage		50% of $V_{CC}$	5.5	V
$V_{IL}$	Low-level input voltage		0	30% of $V_{CC}$	V
$T_{IN}$	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.  
Input and output measurement threshold is ~50% of  $V_{CC}$ .

## DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0$ mA, $V_{CC}$ min (LVTTL)		2.4		V
	High-level output voltage @ $I_{OH} = -500$ $\mu$ A, (LVC MOS)		90% $V_{CC}$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0$ mA, $V_{CC}$ min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ $I_{OL} = 1500$ $\mu$ A, (LVC MOS)			10% $V_{CC}$	V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)			5	mA
$I_L$	Input or output leakage current		-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V (sample tested)		0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)		0.02	0.15	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

## XC4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

### XC4000XL Global Low Skew Buffer to Clock K

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>		<b>All</b>	<b>-3</b>	<b>-2</b>	<b>-1</b>	<b>-09</b>	<b>-08</b>	<b>Units</b>
			<b>Min</b>	<b>Max</b>							
Delay from pad through GLS buffer to any clock input, K	T <sub>GLS</sub>	XC4002XL	0.3	2.1	1.8	1.6	1.5				ns
		XC4005XL	0.4	2.7	2.3	2.0	1.9				ns
		XC4010XL	0.5	3.2	2.8	2.4	2.3				ns
		XC4013XL	0.6	3.6	3.1	2.7	2.6		2.3		ns
		XC4020XL	0.7	4.0	3.5	3.0	2.9				ns
		XC4028XL	0.9	4.4	3.8	3.3	3.2				ns
		XC4036XL	1.1	4.8	4.2	3.6	3.5	3.1			ns
		XC4044XL	1.2	5.3	4.6	4.0	3.9				ns
		XC4052XL	1.3	5.7	5.0	4.5	4.4				ns
		XC4062XL	1.4	6.3	5.4	4.7	4.6	4.0			ns
		XC4085XL	1.6	7.2	6.2	5.7	5.5				ns

## XC4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

### XC4000XL Global Early BUFGE #s 1, 2, 5, and 6 to IOB Clock

Speed Grade			All	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Max	Max	Max	Max	Max	
Delay from pad through GE buffer to any IOB clock input.	T <sub>GE</sub>	XC4002XL	0.1	1.6	1.4	1.3	1.2		ns
		XC4005XL	0.3	1.9	1.8	1.7	1.6		ns
		XC4010XL	0.3	2.2	1.9	1.7	1.7		ns
		XC4013XL	0.4	2.4	2.1	1.8	1.7	1.5	ns
		XC4020XL	0.4	2.6	2.2	2.1	2.0		ns
		XC4028XL	0.3	2.8	2.4	2.1	2.0		ns
		XC4036XL	0.3	3.1	2.7	2.3	2.2	1.9	ns
		XC4044XL	0.2	3.5	3.0	2.6	2.4		ns
		XC4052XL	0.3	4.0	3.5	3.0	3.0		ns
		XC4062XL	0.3	4.9	4.3	3.7	3.4	3.0	ns
		XC4085XL	0.4	5.8	5.1	4.7	4.3		ns

### XC4000XL Global Early BUFGE #s 3, 4, 7, and 8 to IOB Clock

Speed Grade			All	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Max	Max	Max	Max	Max	
Delay from pad through GE buffer to any IOB clock input.	T <sub>GE</sub>	XC4002XL	0.5	2.8	2.5	2.1	1.7		ns
		XC4005XL	0.7	3.1	2.8	2.7	2.5		ns
		XC4010XL	0.7	3.5	3.1	2.8	2.7		ns
		XC4013XL	0.7	3.8	3.3	2.9	2.8	2.4	ns
		XC4020XL	0.8	4.1	3.6	3.4	3.2		ns
		XC4028XL	0.9	4.4	3.9	3.4	3.3		ns
		XC4036XL	0.9	4.7	4.2	3.7	3.6	3.1	ns
		XC4044XL	1.0	5.1	4.5	4.0	3.7		ns
		XC4052XL	1.1	5.5	4.8	4.3	4.3		ns
		XC4062XL	1.2	5.9	5.2	4.8	4.5	4.0	ns
		XC4085XL	1.3	6.8	6.0	5.5	5.2		ns

## XC4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

Description	Symbol	Speed Grade		-3		-2		-1		-09		-08	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
<b>Combinatorial Delays</b>													
F/G inputs to X/Y outputs	$T_{ILO}$			1.6		1.5		1.3		1.2		1.1	
F/G inputs via H' to X/Y outputs	$T_{IHO}$			2.7		2.4		2.2		2.0		1.9	
F/G inputs via transparent latch to Q outputs	$T_{ITO}$			2.9		2.6		2.2		2.0		1.8	
C inputs via SR/H0 via H to X/Y outputs	$T_{HH0O}$			2.5		2.2		2.0		1.8		1.8	
C inputs via H1 via H to X/Y outputs	$T_{HH1O}$			2.4		2.1		1.9		1.6		1.5	
C inputs via DIN/H2 via H to X/Y outputs	$T_{HH2O}$			2.5		2.2		2.0		1.8		1.8	
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	$T_{CBYP}$			1.5		1.3		1.1		1.0		0.9	
<b>CLB Fast Carry Logic</b>													
Operand inputs (F1, F2, G1, G4) to $C_{OUT}$	$T_{OPCY}$			2.7		2.3		2.0		1.6		1.6	
Add/Subtract input (F3) to $C_{OUT}$	$T_{ASCY}$			3.3		2.9		2.5		1.8		1.8	
Initialization inputs (F1, F3) to $C_{OUT}$	$T_{INCY}$			2.0		1.8		1.5		1.0		0.9	
$C_{IN}$ through function generators to X/Y outputs	$T_{SUM}$			2.8		2.6		2.4		1.7		1.5	
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$			0.26		0.23		0.20		0.14		0.14	
Carry Net Delay, $C_{OUT}$ to $C_{IN}$	$T_{NET}$			0.32		0.28		0.25		0.24		0.24	
<b>Sequential Delays</b>													
Clock K to Flip-Flop outputs Q	$T_{CKO}$			2.1		1.9		1.6		1.5		1.4	
Clock K to Latch outputs Q	$T_{CKLO}$			2.1		1.9		1.6		1.5		1.4	
<b>Setup Time before Clock K</b>													
F/G inputs	$T_{ICK}$	1.1		1.0		0.9		0.8		0.8			
F/G inputs via H	$T_{IHCK}$	2.2		1.9		1.7		1.6		1.5			
C inputs via H0 through H	$T_{HH0CK}$	2.0		1.7		1.6		1.4		1.4			
C inputs via H1 through H	$T_{HH1CK}$	1.9		1.6		1.4		1.2		1.1			
C inputs via H2 through H	$T_{HH2CK}$	2.0		1.7		1.6		1.4		1.4			
C inputs via DIN	$T_{DICK}$	0.9		0.8		0.7		0.6		0.6			
C inputs via EC	$T_{ECCK}$	1.0		0.9		0.8		0.7		0.7			
C inputs via S/R, going Low (inactive)	$T_{RCK}$	0.6		0.5		0.5		0.4		0.4			
CIN input via F/G	$T_{CCK}$	2.3		2.1		1.9		1.3		1.2			
CIN input via F/G and H	$T_{CHCK}$	3.4		3.0		2.7		2.1		2.0			
<b>Hold Time after Clock K</b>													
F/G inputs	$T_{CKI}$	0		0		0		0		0		0	
F/G inputs via H	$T_{CKIH}$	0		0		0		0		0		0	
C inputs via SR/H0 through H	$T_{CKHH0}$	0		0		0		0		0		0	
C inputs via H1 through H	$T_{CKHH1}$	0		0		0		0		0		0	
C inputs via DIN/H2 through H	$T_{CKHH2}$	0		0		0		0		0		0	
C inputs via DIN/H2	$T_{CKDI}$	0		0		0		0		0		0	
C inputs via EC	$T_{CKEC}$	0		0		0		0		0		0	
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		0		0		0		0		0	
<b>Clock</b>													
Clock High time	$T_{CH}$	3.0		2.8		2.5		2.3		2.1			
Clock Low time	$T_{CL}$	3.0		2.8		2.5		2.3		2.1			
<b>Set/Reset Direct</b>													
Width (High)	$T_{RPW}$	3.0		3.7		2.8		2.5		2.3		2.3	
Delay from C inputs via S/R, going High to Q	$T_{RIO}$			3.2		2.8		2.8		2.7		2.3	
<b>Global Set/Reset</b>													
Minimum GSR Pulse Width	$T_{MRW}$			19.8		17.3		15.0		14.0		14.0	
Delay from GSR input to any Q	$T_{MRQ}$			See page 14 for $T_{RRI}$ values per device.									
Toggle Frequency (MHz) (for export control)	$F_{TOG}$ (MHz)			166		179		200		217		238	

## XC4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

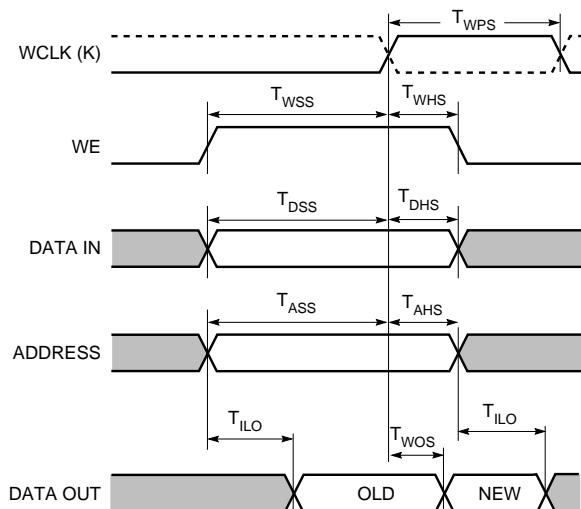
<b>Single Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>-2</b>		<b>-1</b>		<b>-09</b>		<b>-08</b>		
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>									
<b>Write Operation</b>													
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCTS}$	9.0 9.0		8.4 8.4		7.7 7.7		7.4 7.4		7.4 7.4		
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPTS}$	4.5 4.5		4.2 4.2		3.9 3.9		3.7 3.7		3.7 3.7		
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.2 2.2		2.0 2.0		1.7 1.7		1.7 1.7		1.6 1.7		
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHTS}$	0 0										
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	2.0 2.5		1.9 2.3		1.7 2.1		1.7 2.1		1.7 2.1		
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHTS}$	0 0										
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.0 1.8		1.8 1.7		1.6 1.5		1.6 1.5		1.6 1.5		
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHTS}$	0 0										
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$		6.8 8.1		6.3 7.5		5.8 6.9		5.8 6.7		5.7 6.7	
<b>Read Operation</b>													
Address read cycle time	16x2 32x1	$T_{RC}$ $T_{RCT}$	4.5 6.5		3.1 5.5		2.6 3.8		2.6 3.8		2.6 3.8		
Data Valid after address change (no Write Enable)	16x2 32x1	$T_{ILO}$ $T_{IHO}$		1.6 2.7		1.5 2.4		1.3 2.2		1.2 2.0		1.1 1.9	
Address setup time before clock K	16x2 32x1	$T_{ICK}$ $T_{IHCK}$	1.1 2.2		1.0 1.9		0.9 1.7		0.8 1.6		0.8 1.5		

## XC4000XL CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

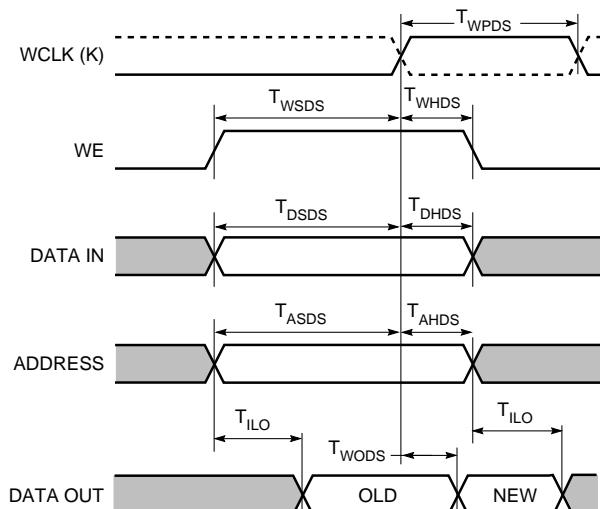
Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted.

Dual Port RAM	Speed Grade		-3		-2		-1		-09		-08	
	Size	Symbol	Min	Max								
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	9.0		8.4		7.7		7.4		7.4	
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	4.5		4.2		3.9		3.7		3.7	
Address setup time before clock K	16x1	$T_{ASDS}$	2.5		2.0		1.7		1.7		1.6	
Address hold time after clock K	16x1	$T_{AHDS}$	0		0		0		0		0	
DIN setup time before clock K	16x1	$T_{DSDS}$	2.5		2.3		2.0		2.0		2.0	
DIN hold time after clock K	16x1	$T_{DHDS}$	0		0		0		0		0	
WE setup time before clock K	16x1	$T_{WSDS}$	1.8		1.7		1.6		1.6		1.6	
WE hold time after clock K	16x1	$T_{WHDS}$	0		0		0		0		0	
Data valid after clock K	16x1	$T_{WODS}$		7.8		7.3		6.7		6.7		6.6

## XC4000XL CLB RAM Synchronous (Edge-Triggered) Write Timing



X6461



X6474

## XC4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XC4000XL Output Flip-Flop, Clock to Out

Speed Grade			All	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Max	Max	Max	Max	Max	
Global Low Skew Clock to Output using Output Flip Flop	T <sub>ICKOF</sub>	XC4002XL	1.2	7.1	6.1	5.4	5.1		ns
		XC4005XL	1.3	7.7	6.6	5.8	5.4		ns
		XC4010XL	1.4	8.2	7.1	6.2	5.8		ns
		XC4013XL	1.5	8.6	7.4	6.5	6.1	5.6	ns
		XC4020XL	1.6	9.0	7.8	6.8	6.4		ns
		XC4028XL	1.8	9.4	8.1	7.1	6.7		ns
		XC4036XL	2.0	9.8	8.5	7.4	7.0	6.4	ns
		XC4044XL	2.1	10.3	8.9	7.8	7.4		ns
		XC4052XL	2.2	10.7	9.3	8.3	7.9		ns
		XC4062XL	2.3	11.3	9.7	8.5	8.1	7.3	ns
		XC4085XL	2.5	12.2	10.5	9.5	9.0		ns
For output SLOW option add	T <sub>SLOW</sub>	All Devices	0.5	3.0	2.5	2.0	1.7	1.6	ns

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.

Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load. For different loads, see Figure 1.

### Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

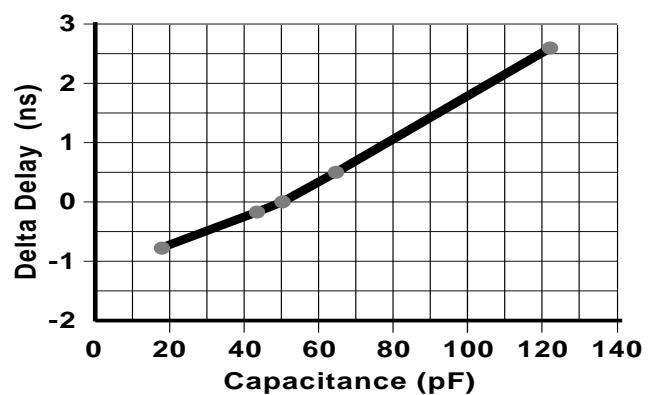


Figure 1: Delay Factor at Various Capacitive Loads

X8257

## XC4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XC4000XL Output Flip-Flop, Clock to Out, BUFGE #s 1, 2, 5, and 6

Speed Grade			All	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Max	Max	Max	Max	Max	
Global Early Clock to Output using Output Flip Flop. Values are for BUFGE #s 1, 2, 5, and 6.	$T_{ICKEOF}$	XC4002XL	1.0	6.6	5.7	5.1	4.8		ns
		XC4005XL	1.2	6.9	6.1	5.5	5.2		ns
		XC4010XL	1.2	7.2	6.2	5.5	5.3		ns
		XC4013XL	1.3	7.4	6.4	5.6	5.3	4.8	ns
		XC4020XL	1.3	7.6	6.5	5.9	5.6		ns
		XC4028XL	1.2	7.8	6.7	5.9	5.6		ns
		XC4036XL	1.2	8.1	7.0	6.1	5.8	5.2	ns
		XC4044XL	1.1	8.5	7.3	6.4	6.0		ns
		XC4052XL	1.2	9.0	7.8	6.8	6.6		ns
		XC4062XL	1.2	9.9	8.6	7.5	7.0	6.3	ns
		XC4085XL	1.3	10.8	9.4	8.5	7.9		ns

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.

Output timing is measured at ~50%  $V_{CC}$  threshold with 50 pF external capacitive load. For different loads, see Figure 1.

### XC4000XL Output Flip-Flop, Clock to Out, BUFGE #s 3, 4, 7, and 8

Speed Grade			All	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Max	Max	Max	Max	Max	
Global Early Clock to Output using Output Flip Flop. Values are for BUFGE #s 3, 4, 7, and 8.	$T_{ICKEOF}$	XC4002XL	1.3	7.8	6.8	5.9	5.3		ns
		XC4005XL	1.5	8.1	7.1	6.5	6.1		ns
		XC4010XL	1.6	8.5	7.4	6.6	6.3		ns
		XC4013XL	1.6	8.8	7.6	6.7	6.4	5.7	ns
		XC4020XL	1.7	9.1	7.9	7.2	6.8		ns
		XC4028XL	1.7	9.4	8.2	7.2	6.9		ns
		XC4036XL	1.8	9.7	8.5	7.5	7.2	6.4	ns
		XC4044XL	1.9	10.1	8.8	7.8	7.3		ns
		XC4052XL	2.0	10.5	9.1	8.1	7.9		ns
		XC4062XL	2.0	10.9	9.5	8.6	8.1	7.3	ns
		XC4085XL	2.2	11.8	10.3	9.3	8.8		ns

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs for FAST mode configurations.

Output timing is measured at ~50%  $V_{CC}$  threshold with 50 pF external capacitive load. For different loads, see Figure 1.

## XC4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XC4000XL Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Min	Min	Min	Min	
Input Setup and Hold Times								
<b>No Delay</b> Global Low Skew Clock and IFF Global Low Skew Clock and FCL	$T_{PSN}/T_{PHN}$	XC4002XL XC4005XL XC4010XL XC4013XL XC4020XL XC4028XL XC4036XL XC4044XL XC4052XL XC4062XL XC4085XL	2.5 / 1.5 1.2 / 2.6 1.2 / 3.0 1.2 / 3.2 1.2 / 3.7 1.2 / 4.4 1.2 / 5.5 1.2 / 5.8 1.2 / 7.1 1.2 / 7.0 1.2 / 9.4	2.2 / 1.3 1.1 / 2.2 1.1 / 2.6 1.1 / 2.8 1.1 / 3.2 1.1 / 3.8 1.1 / 4.8 1.1 / 5.0 1.1 / 6.2 1.1 / 6.1 1.1 / 8.2	1.9 / 1.2 0.9 / 2.0 0.9 / 2.3 0.9 / 2.4 0.9 / 2.8 0.9 / 3.3 0.9 / 4.1 0.9 / 4.4 0.9 / 5.4 0.9 / 5.3 0.9 / 7.1	1.7 / 1.0 0.8 / 1.7 0.8 / 2.0 0.8 / 2.1 0.8 / 2.4 0.8 / 2.9 0.8 / 3.6 0.8 / 3.8 0.8 / 4.7 0.8 / 4.6 0.8 / 6.2	0.8 / 2.1 0.0 / 3.6	ns ns ns ns ns ns ns ns ns ns ns
<b>Partial Delay</b> Global Low Skew Clock and IFF Global Low Skew Clock and FCL	$T_{PSP}/T_{PHP}$	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	8.4 / 0.0 10.5 / 0.0 11.1 / 0.0 6.1 / 1.0 11.9 / 1.0 12.3 / 1.0 6.4 / 1.0 13.1 / 1.0 11.9 / 1.0 6.7 / 1.2 12.9 / 1.2	7.3 / 0.0 9.1 / 0.0 9.7 / 0.0 5.3 / 1.0 10.3 / 1.0 10.7 / 1.0 5.6 / 1.0 11.4 / 1.0 10.3 / 1.0 5.8 / 1.2 11.2 / 1.2	6.3 / 0.0 7.9 / 0.0 8.4 / 0.0 4.6 / 1.0 9.0 / 1.0 9.3 / 1.0 4.8 / 1.0 9.9 / 1.0 9.0 / 1.0 5.1 / 1.2 9.8 / 1.2	5.5 / 0.0 6.9 / 0.0 7.3 / 0.0 4.0 / 1.0 7.8 / 1.0 8.1 / 1.0 4.2 / 1.0 8.6 / 1.0 7.8 / 1.0 4.4 / 1.2 8.5 / 1.2	3.7 / 0.5 4.0 / 0.8 4.2 / 1.0	ns ns ns ns ns ns ns ns ns ns ns
<b>Full Delay</b> Global Low Skew Clock and IFF	$T_{PSD}/T_{PHD}$	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	6.8 / 0.0 8.8 / 0.0 9.0 / 0.0 6.4 / 0.0 8.8 / 0.0 9.3 / 0.0 6.6 / 0.0 10.6 / 0.0 11.2 / 0.0 6.8 / 0.0 12.7 / 0.0	6.0 / 0.0 7.6 / 0.0 7.8 / 0.0 6.0 / 0.0 7.6 / 0.0 8.1 / 0.0 6.2 / 0.0 9.2 / 0.0 9.7 / 0.0 6.4 / 0.0 11.0 / 0.0	5.2 / 0.0 6.6 / 0.0 6.8 / 0.0 5.6 / 0.0 6.6 / 0.0 7.0 / 0.0 5.8 / 0.0 8.0 / 0.0 8.4 / 0.0 6.0 / 0.0 9.6 / 0.0	4.5 / 0.0 5.6 / 0.0 5.8 / 0.0 4.8 / 0.0 6.2 / 0.0 6.4 / 0.0 5.3 / 0.0 6.8 / 0.0 7.0 / 0.0 5.5 / 0.0 8.4 / 0.0	4.8 / 0.0 5.3 / 0.0 5.5 / 0.0	ns ns ns ns ns ns ns ns ns ns ns

IFF = Input Flip-Flop or Latch

Notes: Input setup time is measured with the fastest route and the lightest load.

Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

\* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

**XC4000XL BUFGE #s 1, 2, 5, and 6 Global Early Clock, Set-up and Hold for IFF and FCL**

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>	-3	-2	-1	-09	-08	<b>Units</b>
			Min	Min	Min	Min	Min	Min	
Input Setup and Hold Times									
<b>No Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEN}/T_{PHEN}$ $T_{PFSEN}/T_{PFHEN}$	XC4002XL XC4005XL XC4010XL XC4013XL XC4020XL XC4028XL XC4036XL XC4044XL XC4052XL XC4062XL XC4085XL	2.8 / 1.5 1.2 / 4.1 1.2 / 4.4 1.2 / 4.7 1.2 / 4.6 1.2 / 5.3 1.2 / 6.7 1.2 / 6.5 1.2 / 6.7 1.2 / 8.4 1.2 / 8.7	2.5 / 1.3 1.1 / 3.6 1.1 / 3.8 1.1 / 4.1 1.1 / 4.0 1.1 / 4.6 1.1 / 5.8 1.1 / 5.7 1.1 / 5.8 1.1 / 7.3 1.1 / 7.5	2.2 / 1.2 0.9 / 3.1 0.9 / 3.3 0.9 / 3.6 0.9 / 3.5 0.9 / 4.0 0.9 / 5.1 0.9 / 4.9 0.9 / 5.1 0.9 / 6.3 0.9 / 6.6	1.9 / 1.0 0.8 / 2.7 0.8 / 2.9 0.8 / 3.1 0.8 / 3.0 0.8 / 3.5 0.8 / 4.4 0.8 / 4.3 0.8 / 4.4 0.8 / 5.5 0.8 / 5.7		0.5 / 2.7 0.5 / 3.7 0.5 / 4.7	ns ns ns ns ns ns ns ns ns ns ns
<b>Partial Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEP}/T_{PHEP}$ $T_{PFSEP}/T_{PFHEP}$	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	8.1 / 0.9 9.0 / 0.0 11.9 / 0.0 6.4 / 0.0 10.8 / 0.0 14.0 / 0.0 7.0 / 0.0 14.6 / 0.0 16.4 / 0.0 9.0 / 0.8 16.7 / 0.0	7.0 / 0.8 8.5 / 0.0 10.4 / 0.0 5.9 / 0.0 10.3 / 0.0 12.2 / 0.0 6.6 / 0.0 12.7 / 0.0 14.3 / 0.0 8.6 / 0.8 14.5 / 0.0	6.1 / 0.7 8.0 / 0.0 9.0 / 0.0 5.4 / 0.0 9.8 / 0.0 10.6 / 0.0 6.2 / 0.0 11.0 / 0.0 12.4 / 0.0 8.2 / 0.8 12.6 / 0.0	5.3 / 0.6 7.5 / 0.0 8.0 / 0.0 4.9 / 0.0 9.0 / 0.0 9.8 / 0.0 5.2 / 0.0 10.8 / 0.0 11.4 / 0.0 7.0 / 0.8 11.6 / 0.0		4.4 / 0.0 4.7 / 0.0 6.3 / 0.5	ns ns ns ns ns ns ns ns ns ns ns
<b>Full Delay</b> Global Early Clock and IFF	$T_{PSED}/T_{PHED}$	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	6.7 / 0.0 10.8 / 0.0 10.3 / 0.0 10.0 / 0.0 12.0 / 0.0 12.6 / 0.0 12.2 / 0.0 13.8 / 0.0 14.1 / 0.0 13.1 / 0.0 17.9 / 0.0	5.8 / 0.0 9.4 / 0.0 9.0 / 0.0 8.7 / 0.0 10.4 / 0.0 11.0 / 0.0 10.6 / 0.0 12.0 / 0.0 12.3 / 0.0 11.4 / 0.0 15.6 / 0.0	5.1 / 0.0 8.2 / 0.0 7.8 / 0.0 7.6 / 0.0 9.1 / 0.0 9.5 / 0.0 9.2 / 0.0 10.5 / 0.0 10.7 / 0.0 9.9 / 0.0 13.6 / 0.0	4.4 / 0.0 7.1 / 0.0 6.8 / 0.0 6.6 / 0.0 7.9 / 0.0 8.3 / 0.0 8.0 / 0.0 9.1 / 0.0 9.3 / 0.0 8.6 / 0.0 11.8 / 0.0		6.0 / 0.0 7.2 / 0.0 7.8 / 0.0	ns ns ns ns ns ns ns ns ns ns ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Input setup time is measured with the fastest route and the lightest load.

Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

\* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XC4000XL BUFGE #s 3, 4, 7, and 8 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade		-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Min	Min	Min	Min	Min	
Input Setup & Hold Times									
<b>No Delay</b> Global Early Clock and IFF Global Early Clock and FCL	T <sub>PSEN</sub> /T <sub>PHEN</sub> T <sub>PFSEN</sub> /T <sub>PFHEN</sub>	XC4002XL XC4005XL XC4010XL XC4013XL XC4020XL XC4028XL XC4036XL XC4044XL XC4052XL XC4062XL XC4085XL	3.0 / 2.0 1.2 / 4.1 1.2 / 4.4 1.2 / 4.7 1.2 / 4.6 1.2 / 5.3 1.2 / 6.7 1.2 / 6.5 1.2 / 6.7 1.2 / 8.4 1.2 / 8.7	2.6 / 1.7 1.1 / 3.6 1.1 / 3.8 1.1 / 4.1 1.1 / 4.0 1.1 / 4.6 1.1 / 5.8 1.1 / 5.7 1.1 / 5.8 1.1 / 7.3 1.1 / 7.5	2.3 / 1.5 0.9 / 3.1 0.9 / 3.3 0.9 / 3.6 0.9 / 3.5 0.9 / 4.0 0.9 / 5.1 0.9 / 4.9 0.9 / 5.1 0.9 / 6.3 0.9 / 6.6	2.0 / 1.3 0.8 / 2.7 0.8 / 2.9 0.8 / 3.1 0.8 / 3.0 0.8 / 3.5 0.8 / 4.4 0.8 / 4.3 0.8 / 4.4 0.8 / 5.5 0.8 / 5.7		0.5 / 2.7 0.5 / 3.7 0.5 / 4.7	ns ns ns ns ns ns ns ns ns ns ns
<b>Partial Delay</b> Global Early Clock and IFF Global Early Clock and FCL	T <sub>PSEP</sub> /T <sub>PHEP</sub> T <sub>PFSEP</sub> /T <sub>PFHEP</sub>	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	7.3 / 1.5 8.4 / 0.0 10.3 / 0.0 5.4 / 0.0 9.8 / 0.0 12.7 / 0.0 6.4 / 0.8 13.8 / 0.0 14.5 / 0.0 8.4 / 1.5 14.5 / 0.0	6.4 / 1.3 7.9 / 0.0 9.0 / 0.0 4.9 / 0.0 9.3 / 0.0 11.0 / 0.0 5.9 / 0.8 12.0 / 0.0 12.7 / 0.0 7.9 / 1.5 12.7 / 0.0	5.5 / 1.2 7.4 / 0.0 7.8 / 0.0 4.4 / 0.0 8.8 / 0.0 9.6 / 0.0 5.4 / 0.8 10.4 / 0.0 11.0 / 0.0 7.4 / 1.5 11.0 / 0.0	4.8 / 1.0 7.2 / 0.0 7.4 / 0.0 4.3 / 0.0 8.5 / 0.0 9.3 / 0.0 5.0 / 0.8 10.2 / 0.0 10.7 / 0.0 6.8 / 1.5 10.8 / 0.0		4.0 / 0.0 4.6 / 0.2 6.2 / 0.0	ns ns ns ns ns ns ns ns ns ns ns
<b>Full Delay</b> Global Early Clock and IFF	T <sub>PSED</sub> /T <sub>PHED</sub>	XC4002XL XC4005XL XC4010XL XC4013XL* XC4020XL XC4028XL XC4036XL* XC4044XL XC4052XL XC4062XL* XC4085XL	5.9 / 0.0 10.8 / 0.0 10.3 / 0.0 10.0 / 0.0 12.0 / 0.0 12.6 / 0.0 12.2 / 0.0 13.8 / 0.0 14.1 / 0.0 13.1 / 0.0 17.9 / 0.0	5.2 / 0.0 9.4 / 0.0 9.0 / 0.0 8.7 / 0.0 10.4 / 0.0 11.0 / 0.0 10.6 / 0.0 12.0 / 0.0 12.3 / 0.0 11.4 / 0.0 15.6 / 0.0	4.5 / 0.0 8.2 / 0.0 7.8 / 0.0 7.6 / 0.0 9.1 / 0.0 9.5 / 0.0 9.2 / 0.0 10.5 / 0.0 10.7 / 0.0 9.9 / 0.0 13.6 / 0.0	3.9 / 0.0 7.1 / 0.0 6.8 / 0.0 6.6 / 0.0 7.9 / 0.0 8.3 / 0.0 8.0 / 0.0 9.1 / 0.0 9.3 / 0.0 8.6 / 0.0 11.8 / 0.0		6.0 / 0.0 7.2 / 0.0 7.8 / 0.0	ns ns ns ns ns ns ns ns ns ns ns

IFF = Input Flip Flop or Latch. FCL = Fast Capture Latch

Notes: Input setup time is measured with the fastest route and the lightest load.

Input hold time is measured using the furthest distance and a reference load of one clock pin per IOB as well as driving all accessible CLB flip-flops. For designs with a smaller number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be used as a worst-case pin-to-pin no-delay input hold specification.

\* The XC4013XL, XC4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XC4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade		-3	-2	-1	-09	-08	Units	
Description	Symbol	Device		Min	Min	Min	Min	Min		
<b>Clocks</b>										
Clock Enable (EC) to Clock (IK)	$T_{ECIK}$	All devices		0.1	0.1	0.1	0.1	0.1	ns	
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	$T_{OKIK}$	XC4002XL XC4013, 36, 62XL Balance of Family		3.0 2.2 2.2	2.7 1.9 1.9	2.3 1.6 1.6	2.3 1.6 1.6	1.6	ns ns ns	
<b>Setup Times</b>										
Pad to Clock (IK), no delay	$T_{PICK}$	XC4002XL XC4013, 36, 62XL Balance of Family		2.6 1.7 1.7	2.3 1.5 1.5	2.0 1.3 1.3	2.0 1.3 1.3	1.2	ns ns ns	
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	$T_{PICKF}$	XC4002XL XC4013, 36, 62XL Balance of Family		3.2 2.3 2.3	2.9 2.0 2.0	2.5 1.8 1.8	2.4 1.7 1.7	1.6	ns ns ns	
Pad to Fast Capture Latch Enable (OK), no delay	$T_{POCK}$	XC4013, 36, 62XL Balance of Family		1.2 1.2	1.0 1.0	0.9 0.9	0.9 0.9	0.9	ns ns	
<b>Hold Times</b>										
All Hold Times		All Devices		0	0	0	0	0		
<b>Global Set/Reset</b>										
Minimum GSR Pulse Width	$T_{MRW}$	All devices		19.8	17.3	15.0	14.0	14.0	ns	
<b>Global Set/Reset</b>										
Delay from GSR input to any Q	$T_{RRI^*}$	XC4002XL XC4005XL XC4010XL XC4013XL XC4020XL XC4028XL XC4036XL XC4044XL XC4052XL XC4062XL XC4085XL		9.8 11.3 13.9 15.9 18.6 20.5 22.5 25.1 27.2 29.1 34.4	8.5 9.8 12.1 13.8 16.1 17.9 19.6 21.9 23.6 25.3 29.9	7.4 8.5 10.5 12.0 14.0 15.5 17.0 19.0 20.5 22.0 26.0	7.0 8.1 10.0 11.4 13.3 14.3 16.2 18.1 19.5 20.9 24.7	10.9 16.2 20.4	ns ns ns ns ns ns ns ns ns ns ns	

\* Indicates Minimum Amount of Time to Assure Valid Data. IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch.

## XC4000XL IOB Input Switching Characteristic Guidelines (Cont)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Device	Speed Grade		-3	-2	-1	-09	-08	Units	
			Max	Max	Max	Max	Max	Max	Max		
<b>Propagation Delays</b>											
Pad to I1, I2	$T_{PID}$	All devices	1.6	1.4	1.2	1.1	1.0			ns	
Pad to I1, I2 via transparent input latch, no delay	$T_{PLI}$	XC4002XL	4.7	4.2	3.6	3.5				ns	
		XC4013, 36, 62XL	3.1	2.7	2.4	2.2			2.1	ns	
		Balance of Family	3.1	2.7	2.4	2.2				ns	
Pad to I1, I2 via transparent FCL and in- put latch, no delay	$T_{PFLI}$	X4002XL	5.4	4.7	4.1	3.9				ns	
		XC4013, 36, 62XL	3.7	3.3	2.8	2.7			2.5	ns	
		Balance of Family	3.7	3.3	2.8	2.7				ns	
Clock (IK) to I1, I2 (flip-flop) Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKRI}$ $T_{IKLI}$	All devices	1.7	1.5	1.3	1.2	1.2			ns	
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	$T_{OKLI}$	All devices	1.8	1.6	1.4	1.3	1.3			ns	
		XC4002XL	5.2	4.6	4.0	3.8				ns	
		XC4013, 36, 62XL	3.6	3.1	2.7	2.6			2.5	ns	
Balance of Family											
IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch											

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

## XC4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

		-3		-2		-1		-09		-08	
Description	Symbol	Min	Max								
<b>Clocks</b>											
Clock High Clock Low	T <sub>CH</sub> T <sub>CL</sub>	3.0 3.0		2.8 2.8		2.5 2.5		2.3 2.3		2.1 2.1	
<b>Propagation Delays</b>											
Clock (OK) to Pad Output (O) to Pad 3-state to Pad hi-Z (slew-rate independent) 3-state to Pad active and valid Output (O) to Pad via Fast Output MUX Select (OK) to Pad via Fast MUX	T <sub>OKPOF</sub> T <sub>OPF</sub> T <sub>TSHZ</sub> T <sub>TSONF</sub> T <sub>OFPF</sub> T <sub>OKFPF</sub>		5.0 4.1 4.0 4.4 5.5 5.1		4.3 3.6 3.5 3.8 4.8 4.5		3.8 3.1 3.0 3.3 4.2 3.9		3.5 3.0 2.9 3.3 4.0 3.7		3.3 2.8 2.9 3.3 3.7 3.4
<b>Setup and Hold Times</b>											
Output (O) to clock (OK) setup time Output (O) to clock (OK) hold time Clock Enable (EC) to clock (OK) setup time Clock Enable (EC) to clock (OK) hold time	T <sub>OOK</sub> T <sub>OKO</sub> T <sub>ECOK</sub> T <sub>OKEC</sub>	0.5 0.0 0.0 0.3		0.4 0.0 0.0 0.2		0.3 0.0 0.0 0.1		0.3 0.0 0.0 0.0		0.3 0.0 0.0 0.0	
<b>Global Set/Reset</b>											
Minimum GSR pulse width Delay from GSR input to any Pad XC4002XL XC4005XL XC4010XL XC4013XL XC4020XL XC4028XL XC4036XL XC4044XL XC4052XL XC4062XL XC4085XL	T <sub>MRW</sub> T <sub>RPO*</sub>	19.8 14.3 15.9 18.5 20.5 23.2 25.1 27.1 29.7 31.7 33.7 39.0		17.3 12.5 13.8 16.1 17.8 20.1 21.9 23.6 25.9 27.6 29.3 33.9		15.0 10.9 12.0 14.0 15.5 17.5 19.0 20.5 22.5 24.0 25.5 29.5		14.0 10.3 11.4 13.3 14.7 16.6 17.6 19.4 21.4 22.8 24.2 28.0		14.0 10.3 11.4 13.3 14.7 16.6 17.6 19.4 21.4 22.8 24.2 28.0	
<b>Slew Rate Adjustment</b>											
For output SLOW option add	T <sub>SLOW</sub>		3.0		2.5		2.0		1.7		1.6

Note: Output timing is measured at ~50% V<sub>CC</sub> threshold, with 50 pF external capacitive loads.

\* Indicates Minimum Amount of Time to Assure Valid Data.

## Revision Record

### Revisions from Version 2.0:

Internal Data Sheet Reference: ADSXC4000XL002, September 24, 1998 (Version 0.02); PDSXC4000XL0012, September 24, 1998 (Version 0.01.2; PDSXC4000XL0011, September 2, 1998 (Version 0.01.1)

### Incorporated Speed Tables Version 2.9 dated September 21, 1998, which included:

1. adding -08 specifications as final.
2. adding XC4002XL table values as final.
3. on pages 4, 5, 9, 10, adding minimum table values as final.
4. on page 9 through 13: Modifying table notes.
5. on page 10, adding bottom table for BUFGE #3, 4, 7, and 8.
6. on pages 4 through 16, changing all -09 column table values to final with the following changes:
  - a. Page 10, top table, -09 column: For all devices EXCEPT XC4002XL, table values increased by 0.1 ns.
  - b. Page 16, switching table values for  $t_{TSHZ}$  row and  $t_{TSONG}$  which were swapped in error in version 2.0
  - c. Page 16, -09 column, parameter  $T_{TSHZ}$  (new - see b above) decreased by 0.1 ns.

### The following modifications were made to pre-existing final specifications for -3, -2 and -1 bins:

1. Page 9, -2 column: For XC4005XL, XC4010XL, XC4013XL, XC4020XL, XC4028XL, and XC4044X table value tightened by 0.1 ns.
2. Page 9, -3 column, XC4010XL: Table value reduced from 8.3 ns to 8.2 ns.
3. Page 14,  $T_{ECIK}$  parameter, row 1: changed to 0.1 ns for -1, -2 and -3 columns.
4. Page 15, -3 column: Table values for parameters  $T_{IKRI}$ , and  $T_{IKLI}$  decreased by 0.1 ns.
5. Page 15, -2 column: Table value for parameter  $T_{IKLI}$  decreased by 0.1 ns.
6. Page 16, -2 column: Parameter  $T_{OKPOF}$  decreased by 0.1 ns.
7. Page 16, switched table values for  $t_{TSHZ}$  row and  $t_{TSONG}$  which were swapped in error in version 2.0
8. Page 16, -1, -2, -3 columns: parameter  $T_{TSHZ}$  (new - see 7 above) decreased by 0.1 ns.

## XC4000EX Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

**All specifications subject to change without notice.**

### XC4000EX Absolute Maximum Ratings

Symbol	Description	Value	Units	
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V	
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to $V_{CC}$ +0.5	V	
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to $V_{CC}$ +0.5	V	
$V_{CCt}$	Longest Supply Voltage Rise Time from 1 V to 4 V	50	ms	
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C	
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C	
$T_J$	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to  $V_{CC}$  + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### XC4000EX Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_J = 0$ °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, $T_J = -40$ °C to +100°C	Industrial	4.5	5.5	V
$V_{IH}$	High-level input voltage	TTL inputs	2.0	$V_{CC}$	V
		CMOS inputs	70%	100%	$V_{CC}$
$V_{IL}$	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

Note 3: All timing parameters are specified for Commercial temperature range only.

## XC4000EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description			Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0$ mA, $V_{CC}$ min	TTL outputs	2.4			V
	High-level output voltage @ $I_{OH} = -1.0$ mA	CMOS outputs	$V_{CC}-0.5$			V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0$ mA, $V_{CC}$ min (Note 1)	TTL outputs		0.4		V
		CMOS outputs		0.4		V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)			3.0		V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)				25	mA
$I_L$	Input or output leakage current			-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10		pF
		PGA packages		16		pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V (sample tested)			0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 5.5$ V (sample tested)			0.02	0.25	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low			0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND.

## XC4000EX Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Device	Speed Grade			Units
			-4	-3	-2	
From pad through Global Low Skew buffer, to any clock K	$T_{GLS}$	XC4028EX	9.2	7.5	6.4	ns
		XC4036EX	9.8	7.9	7.1	ns
From pad through Global Early buffer, to any clock K in same quadrant	$T_{GE}$	XC4028EX	5.7	4.4	4.2	ns
		XC4036EX	5.9	4.6	4.4	ns

## XC4000EX Longline and Wide Decoder Timing Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted. Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

### XC4000EX Horizontal Longline Switching Characteristic Guidelines

Description	Symbol	Device	Speed Grade		-4	-3	-2	Units
			Max	Max	Max	Max	Max	
<b>TBUF driving a Horizontal Longline</b>								
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	$T_{IO1}$	XC4028EX XC4036EX	13.7 16.5	11.3 13.6	10.9 13.2	ns ns	ns	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	$T_{ON}$	XC4028EX XC4036EX	14.7 17.4	12.1 14.4	11.7 14.0	ns ns	ns	ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	$T_{PU2}$	XC4028EX XC4036EX					ns ns	ns
<b>TBUF driving Half a Horizontal Longline</b>								
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	$T_{HIO1}$	XC4028EX XC4036EX	6.3 7.3	5.6 6.0	4.6 5.7	ns ns	ns	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	$T_{HON}$	XC4028EX XC4036EX	7.2 8.2	6.4 6.8	5.4 6.5	ns ns	ns	ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	$T_{HPU4}$	XC4028EX XC4036EX					ns ns	ns

Note 1: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the statictiming analyzer to determine the delay for each destination.

### XC4000EX Wide Decoder Switching Characteristic Guidelines

Description	Symbol	Device	Speed Grade		-4	-3	-2	Units
			Max	Max	Max	Max	Max	
Full length, two pull-ups, inputs from IOB I-pins	$T_{WAF2}$	XC4028EX XC4036EX						ns ns
Full length, two pull-ups, inputs from internal logic	$T_{WAF2L}$	XC4028EX XC4036EX						ns ns
Half length, two pull-ups, inputs from IOB I-pins	$T_{WAO2}$	XC4028EX XC4036EX						ns ns
Half length, two pull-ups, inputs from internal logic	$T_{WAO2L}$	XC4028EX XC4036EX						ns ns

Note 1: These delays are specified from the decoder input to the decoder output.

## XC4000EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devicees unless otherwise noted.

Speed Grade		-4		-3		-2		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	
<b>Combinatorial Delays</b>								
F/G inputs to X/Y outputs	$T_{ILO}$			2.2		1.8		1.5 ns
F/G inputs via H' to X/Y outputs	$T_{IHO}$			3.8		3.2		2.7 ns
F/G inputs via transparent latch to Q outputs	$T_{ITO}$			3.2		2.7		2.5 ns
C inputs via SR/H0 via H' to X/Y outputs	$T_{HH00}$			3.6		3.0		2.5 ns
C inputs via H1 via H' to X/Y outputs	$T_{HH10}$			3.0		2.5		2.3 ns
C inputs via DIN/H2 via H' to X/Y outputs	$T_{HH20}$			3.6		3.0		2.5 ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	$T_{CBYP}$			2.0		1.6		1.4 ns
<b>CLB Fast Carry Logic</b>								
Operand inputs (F1, F2, G1, G4) to COUT	$T_{OPCY}$			2.5		2.2		1.9 ns
Add/Subtract input (F3) to COUT	$T_{ASCY}$			4.1		3.6		3.1 ns
Initialization inputs (F1, F3) to COUT	$T_{INCY}$			1.9		1.6		1.4 ns
CIN through function generators to X/Y outputs	$T_{SUM}$			3.0		2.6		2.2 ns
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$			0.60		0.50		0.40 ns
Carry Net Delay, $C_{OUT}$ to $C_{IN}$	$T_{NET}$			0.18		0.15		0.15 ns
<b>Sequential Delays</b>								
Clock K to Flip-Flop outputs Q	$T_{CKO}$			2.2		1.9		1.7 ns
Clock K to Latch outputs Q	$T_{CKLO}$			2.2		1.9		1.7 ns
<b>Setup Time before Clock K</b>								
F/G inputs	$T_{ICK}$	1.3		1.1		1.1		ns
F/G inputs via H'	$T_{IHCK}$	3.0		2.5		2.2		ns
C inputs via H0 through H'	$T_{HH0CK}$	2.8		2.3		2.0		ns
C inputs via H1 through H'	$T_{HH1CK}$	2.2		1.8		1.8		ns
C inputs via H2 through H'	$T_{HH2CK}$	2.8		2.3		2.0		ns
C inputs via DIN	$T_{DICK}$	1.2		0.9		0.9		ns
C inputs via EC	$T_{ECK}$	1.2		1.0		0.9		ns
C inputs via S/R, going Low (inactive)	$T_{TRCK}$	0.8		0.7		0.6		ns
CIN input via F/G'	$T_{CCK}$	2.2		1.8		2.1		ns
CIN input via F/G' and H'	$T_{CHCK}$	3.9		3.2		3.2		ns
<b>Hold Time after Clock K</b>								
F/G inputs	$T_{CKI}$	0		0		0		ns
F/G inputs via H'	$T_{CKIH}$	0		0		0		ns
C inputs via SR/H0 through H'	$T_{CKHH0}$	0		0		0		ns
C inputs via H1 through H'	$T_{CKHH1}$	0		0		0		ns
C inputs via DIN/H2 through H'	$T_{CKHH2}$	0		0		0		ns
C inputs via DIN/H2	$T_{CKDI}$	0		0		0		ns
C inputs via EC	$T_{CKEC}$	0		0		0		ns
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		0		0		ns
<b>Clock</b>								
Clock High time	$T_{CH}$	3.5		3.0		3.0		ns
Clock Low time	$T_{CL}$	3.5		3.0		3.0		ns
<b>Set/Reset Direct</b>								
Width (High)	$T_{RPW}$	3.5		4.5		3.0		ns
Delay from C inputs via S/R, going High to Q	$T_{TRIO}$					3.8		3.6 ns
<b>Global Set/Reset</b>								
Minimum GSR Pulse Width	$T_{MRW}$			13.0		11.5		11.5 ns
Delay from GSR input to any Q (XC4028EX)	$T_{MRQ}$			22.8		19.0		19.0 ns
Delay from GSR input to any Q (XC4036EX)	$T_{MRQ}$			24.0		21.0		21.0 ns
<b>Toggle Frequency</b> (for export control purposes)	$F_{TOG}$			143		166		166 MHz

## XC4000EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

<b>Single Port RAM</b>	<b>Speed Grade</b>		<b>-4</b>		<b>-3</b>		<b>-2</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>									
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCTS}$	11.0 11.0		9.0 9.0		9.0 9.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPPTS}$	5.5 5.5		4.5 4.5		4.5 4.5		ns ns
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.7 2.6		2.3 2.2		2.2 2.2		ns ns
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHTS}$	0 0		0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	2.4 2.9		2.0 2.5		2.0 2.5		ns ns
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHTS}$	0 0		0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.3 2.1		2.0 1.8		2.0 1.8		ns ns
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHTS}$	0 0		0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$		8.2 10.1		6.8 8.4		6.8 8.2	ns ns

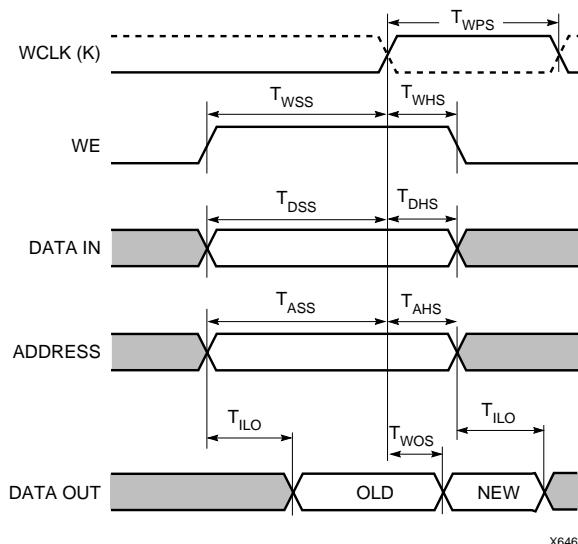
Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

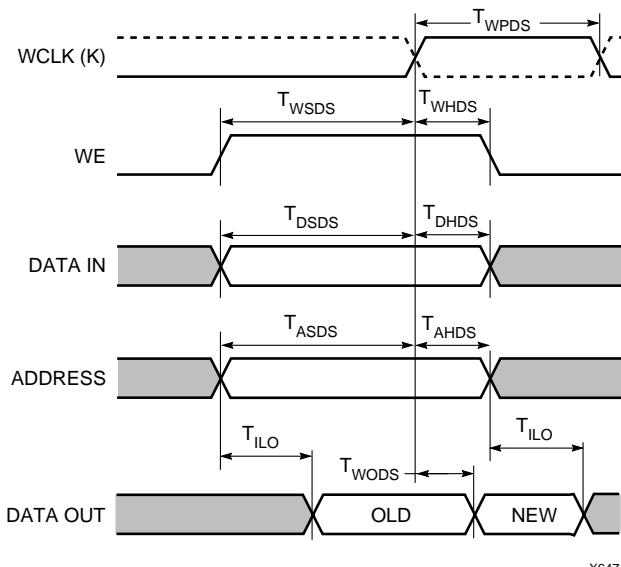
<b>Dual-Port RAM</b>	<b>Speed Grade</b>		<b>-4</b>		<b>-3</b>		<b>-2</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>									
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	11.0		9.0		9.0		ns
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	5.5		4.5		4.5		ns
Address setup time before clock K	16x1	$T_{ASDS}$	3.1		2.6		2.5		ns
Address hold time after clock K	16x1	$T_{AHDS}$	0		0		0		ns
DIN setup time before clock K	16x1	$T_{DSDS}$	2.9		2.5		2.5		ns
DIN hold time after clock K	16x1	$T_{DHDS}$	0		0		0		ns
WE setup time before clock K	16x1	$T_{WSDS}$	2.1		1.8		1.8		ns
WE hold time after clock K	16x1	$T_{WHDS}$	0		0		0		ns
Data valid after clock K	16x1	$T_{WODS}$		9.4		7.8		7.8	ns

Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

## XC4000EX CLB RAM Synchronous (Edge-Triggered) Write Timing



## XC4000EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



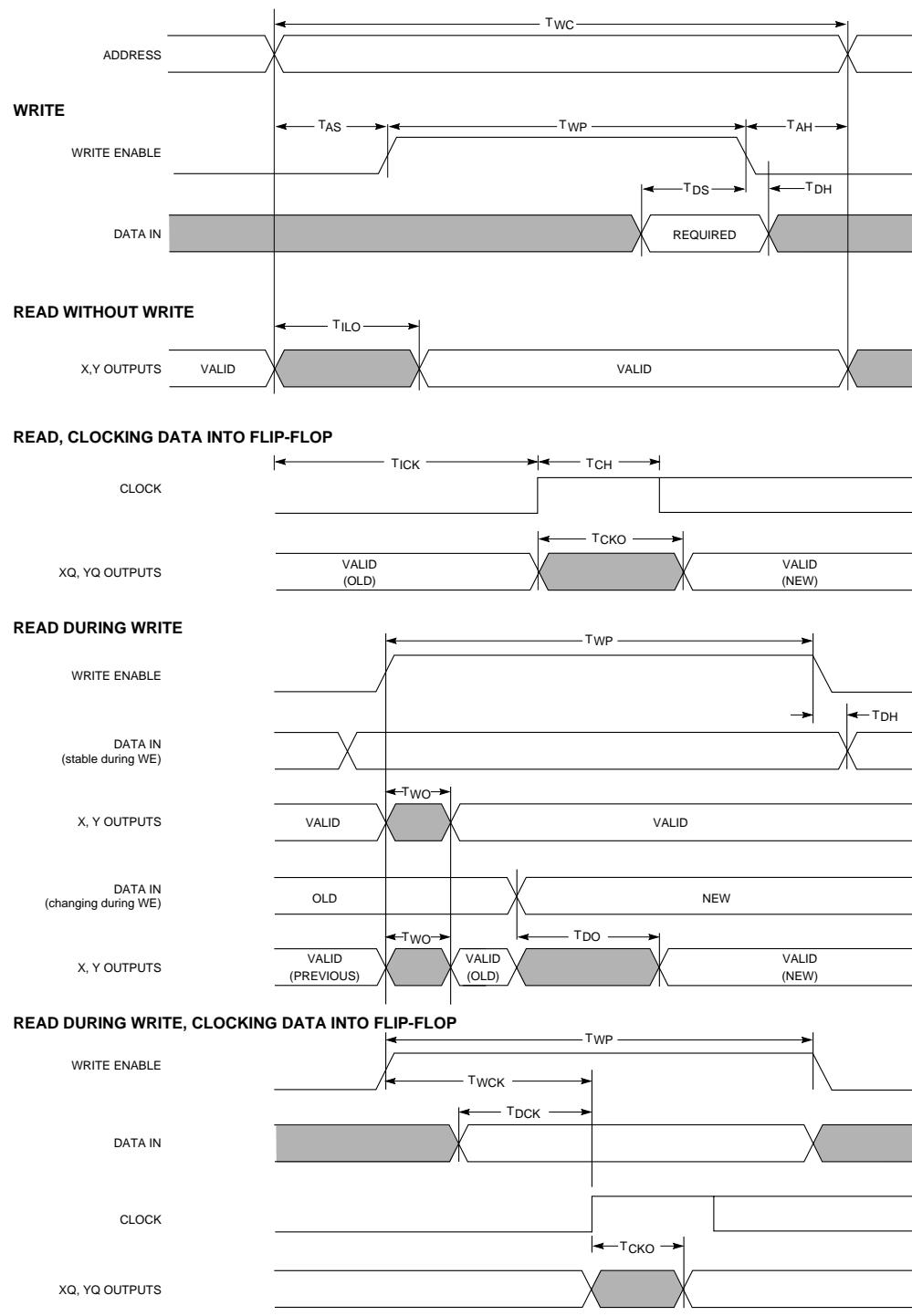
## XC4000EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

Speed Grade			-4		-3		-2		Units
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	
<b>Write Operation</b>									
Address write cycle time	16x2 32x1	$T_{WC}$ $T_{WCT}$	10.6 10.6		9.2 9.2		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	$T_{WP}$ $T_{WPT}$	5.3 5.3		4.6 4.6		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	$T_{AS}$ $T_{AST}$	2.8 2.9		2.4 2.5		2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	$T_{AH}$ $T_{AHT}$	1.7 1.7		1.4 1.4		1.4 1.4		ns ns
DIN setup time before end of WE	16x2 32x1	$T_{DS}$ $T_{DST}$	1.1 1.1		0.9 0.9		0.8 0.8		ns ns
DIN hold time after end of WE	16x2 32x1	$T_{DH}$ $T_{DHT}$	6.6 6.6		5.7 5.7		5.0 5.0		ns ns
<b>Read Operation</b>									
Address read cycle time	16x2 32x1	$T_{RC}$ $T_{RCT}$	4.5 6.5		3.1 5.5		3.1 5.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	$T_{ILO}$ $T_{IHO}$		2.2 3.8		1.8 3.2		1.5 2.7	ns ns
<b>Read Operation, Clocking Data into Flip-Flop</b>									
Address setup time before clock K	16x2 32x1	$T_{ICK}$ $T_{IHCK}$	1.5 3.2		1.2 2.6		1.2 2.6		ns ns
<b>Read During Write</b>									
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	$T_{WO}$ $T_{WOT}$		6.5 7.4		5.7 6.5		4.9 5.6	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	$T_{DO}$ $T_{DOT}$		7.7 8.2		6.7 7.2		5.8 6.2	ns ns
<b>Read During Write, Clocking Data into Flip-Flop</b>									
WE setup time before clock K	16x2 32x1	$T_{WCK}$ $T_{WCKT}$	7.1 9.2		6.2 8.1		5.5 7.0		ns ns
Data setup time before clock K	16x2 32x1	$T_{DCK}$ $T_{DCKT}$	5.9 8.4		5.2 7.4		4.6 6.4		ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

## XC4000EX CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



X2640

## XC4000EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted.

### XC4000EX Output Flip-Flop, Clock to Out

Speed Grade			-4	-3	-2	Units
Description	Symbol	Device	Max	Max	Max	
Global Low Skew Clock to TTL Output (fast) using OFF	$T_{ICKOF}$	XC4028EX XC4036EX	16.6 17.2	13.7 14.1	12.4 13.1	ns ns
Global Early Clock to TTL Output (fast) using OFF	$T_{ICKEOF}$	XC4028EX XC4036EX	13.1 13.3	10.6 10.8	10.2 10.4	ns ns

OFF = Output Flip Flop

### XC4000EX Output MUX, Clock to Out

Speed Grade			-4	-3	-2	Units
Description	Symbol	Device	Max	Max	Max	
Global Low Skew Clock to TTL Output (fast) using OMUX	$T_{PFPF}$	XC4028EX XC4036EX	15.9 16.5	13.1 13.5	11.8 12.5	ns ns
Global Early Clock to TTL Output (fast) using OMUX	$T_{PEFPF}$	XC4028EX XC4036EX	12.4 12.6	10.0 10.2	9.6 9.8	ns ns

OMUX = Output MUX

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at TTL threshold with 50 pF external capacitive load.

Note 3: Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

### XC4000EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

Speed Grade			-4	-3	-2	Units
Description	Symbol	Device	Max	Max	Max	
For TTL output FAST add	$T_{TTLOF}$	All Devices	0	0	0	ns
For TTL output SLOW add	$T_{TTLO}$	All Devices	2.9	2.4	2.4	ns
For CMOS FAST output add	$T_{CMOSOF}$	All Devices	1.0	0.8	0.8	ns
For CMOS SLOW output add	$T_{CMOSO}$	All Devices	3.6	3.0	3.0	ns

## XC4000EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted.

### XC4000EX Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-4	-3	-2	Units
Description	Symbol	Device	Min	Min	Min	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	$T_{PSD}$	XC4028EX	8.0	6.8	6.8	ns
		XC4036EX	8.0	6.8	6.8	ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	$T_{PHD}$	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

IFF = Flip-Flop or Latch

### XC4000EX Global Early Clock, Set-Up and Hold for IFF

		Speed Grade	-4	-3	-2	Units
Description	Symbol	Device	Min	Min	Min	
Input Setup Time, using Global Early clock and IFF (partial delay)	$T_{PSEP}$	XC4028EX	6.5	5.4	5.4	ns
		XC4036EX	6.5	5.4	5.4	ns
Input Hold Time, using Global Early clock and IFF (partial delay)	$T_{PHEP}$	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

IFF = Flip-Flop or Latch

Note 1: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

### XC4000EX Global Early Clock, Set-Up and Hold for FCL

		Speed Grade	-4	-3	-2	Units
Description	Symbol	Device	Min	Min	Min	
Input Setup Time, using Global Early clock and FCL (partial delay)	$T_{PFSEP}$	XC4028EX	3.4	3.4	3.4	ns
		XC4036EX	4.4	4.2	4.2	ns
Input Hold Time, using Global Early clock and FCL (partial delay)	$T_{PFHEP}$	XC4028EX	0	0	0	ns
		XC4036EX	0	0	0	ns

FCL = Fast Capture Latch

Note 1: For CMOS input levels, see the "XC4000EX Input Threshold Adjustments" on page -93.

Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time.

Note 2: under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Note 3: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

### XC4000EX Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

Description	Speed Grade		-4	-3	-2	Units
	Symbol	Device	Max	Max	Max	
For TTL input add	$T_{TTLI}$	All Devices	0	0	0	ns
For CMOS input add	$T_{CMOSI}$	All Devices	0.3	0.2	0.2	ns

## XC4000EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade		-4	-3	-2	Units
Description	Symbol	Device	Min	Min	Min		
<b>Clocks</b>							
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T <sub>OKIK</sub>	All devices	3.2	2.6	2.6	ns	
<b>Propagation Delays</b>							
Pad to I1, I2	T <sub>PID</sub>	All devices	2.2	1.9	1.8	ns	
Pad to I1, I2 via transparent input latch, no delay	T <sub>PLI</sub>	All devices	3.8	3.2	3.0	ns	
Pad to I1, I2 via transparent input latch, partial delay	T <sub>PPLI</sub>	XC4028EX XC4036EX	13.3 14.5	11.1 12.1	10.9 11.9	ns ns	
Pad to I1, I2 via transparent input latch, full delay	T <sub>PDLI</sub>	XC4028EX XC4036EX	18.2 19.4	15.2 16.2	14.9 15.9	ns ns	
Pad to I1, I2 via transparent FCL and input latch, no delay	T <sub>PFLI</sub>	All devices	5.3	4.4	4.2	ns	
Pad to I1, I2 via transparent FCL and input latch, partial delay	T <sub>PPFLI</sub>	XC4028EX XC4036EX	13.6 14.8	11.3 12.3	11.1 12.1	ns ns	
<b>Propagation Delays</b>							
Clock (IK) to I1, I2 (flip-flop)	T <sub>IKRI</sub>	All devices	3.0	2.5	2.4	ns	
Clock (IK) to I1, I2 (latch enable, active Low)	T <sub>IKLI</sub>	All devices	3.2	2.7	2.6	ns	
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T <sub>OKLI</sub>	All devices	6.2	5.2	5.0	ns	
<b>Global Set/Reset</b>							
Minimum GSR Pulse Width	T <sub>MRW</sub>	All devices	13.0	11.5	11.5	ns	
Delay from GSR input to any Q	T <sub>RRI</sub>	XC4028EX	22.8	19.0	19.0	ns	
Delay from GSR input to any Q	T <sub>RRI</sub>	XC4036EX	24.0	21.0	21.0	ns	

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

Note 1: For CMOS input levels, see the "XC4000EX Input Threshold Adjustments" on page -93.

Note 2: For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page -93.

## XC4000EX IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

Description	Symbol	Device	Speed Grade -4	-3	-2	Units
			Min	Min	Min	
<b>Setup Times</b>						
Pad to Clock (IK), no delay	$T_{PICK}$	All devices	2.5	2.0	2.0	ns
Pad to Clock (IK), partial delay	$T_{PICKP}$	XC4028EX XC4036EX	10.8 12.0	9.0 10.0	9.0 10.0	ns ns
Pad to Clock (IK), full delay	$T_{PICKD}$	XC4028EX XC4036EX	15.7 16.9	13.1 14.1	13.1 14.1	ns ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	$T_{PICKF}$	All devices	3.9	3.3	3.3	ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	$T_{PICKFP}$	XC4028EX XC4036EX	12.3 13.5	10.2 11.2	10.2 11.2	ns ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{POCK}$	All devices	0.8	0.7	0.7	ns
Pad to Fast Capture Latch Enable (OK), partial delay	$T_{POCKP}$	XC4028EX XC4036EX	9.1 10.3	7.6 8.6	7.6 8.6	ns ns
<b>Setup Times (TTL or CMOS Inputs)</b>						
Clock Enable (EC) to Clock (IK)	$T_{ECIK}$	All devices	0.3	0.2	0.2	ns
<b>Hold Times</b>						
Pad to Clock (IK), no delay	$T_{IKPI}$	All devices	0	0	0	ns
Pad to Clock (IK), partial delay	$T_{IKPIP}$	All devices	0	0	0	ns
Pad to Clock (IK), full delay	$T_{IKPID}$	All devices	0	0	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch, no delay	$T_{IKFPI}$	All devices	0	0	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch, partial delay	$T_{IKFPPIP}$	All devices	0	0	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch, full delay	$T_{IKFPID}$	All devices	0	0	0	ns
Clock Enable (EC) to Clock (IK), no delay	$T_{IKEC}$	All devices	0	0	0	ns
Clock Enable (EC) to Clock (IK), partial delay	$T_{IKECP}$	All devices	0	0	0	ns
Clock Enable (EC) to Clock (IK), full delay	$T_{IKECD}$	All devices	0	0	0	ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{OKPI}$	All devices	0	0	0	ns
Pad to Fast Capture Latch Enable (OK), partial delay	$T_{OKPIP}$	All devices	0	0	0	ns

Note 1: For CMOS input levels, see the "XC4000EX Input Threshold Adjustments" on page -93.

Note 2: For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page -93.

## XC4000EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000EX devices unless otherwise noted.

Description	Symbol	Speed Grade		-4		-3		-2		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
<b>Propagation Delays</b>										
Clock (OK) to Pad	$T_{OKPOF}$			7.4		6.2		6.0		ns
Output (O) to Pad	$T_{OPF}$			6.2		5.2		5.0		ns
3-state to Pad hi-Z (slew-rate independent)	$T_{TSHZ}$			4.9		4.1		4.1		ns
3-state to Pad active and valid	$T_{TSONF}$			6.2		5.2		5.0		ns
Output MUX Select (OK) to Pad	$T_{OKFPF}$			6.7		5.6		5.4		ns
Fast Path Output MUX Input (EC) to Pad	$T_{CEFPF}$			6.2		5.1		5.0		ns
Slowest Path Output MUX Input (O) to Pad	$T_{OFPF}$			7.3		6.0		5.9		ns
<b>Setup and Hold Times</b>										
Output (O) to clock (OK) setup time	$T_{OOK}$	0.6		0.5		0.5				ns
Output (O) to clock (OK) hold time	$T_{OKO}$	0		0		0				ns
Clock Enable (EC) to clock (OK) setup	$T_{ECOK}$	0		0		0				ns
Clock Enable (EC) to clock (OK) hold	$T_{OKEC}$	0		0		0				ns
<b>Clock</b>										
Clock High	$T_{CH}$	3.5		3.0		3.0				ns
Clock Low	$T_{CL}$	3.5		3.0		3.0				ns
<b>Global Set/Reset</b>										
Minimum GSR pulse width	$T_{MRW}$	13.0		11.5		11.5				ns
Delay from GSR input to any Pad (XC4028EX)	$T_{RPO}$	<b>30.2</b>		<b>25.2</b>		<b>25.0</b>				ns
Delay from GSR input to any Pad (XC4036EX)	$T_{RPO}$	<b>31.4</b>		<b>27.2</b>		<b>27.0</b>				ns

Note 1: Output timing is measured at TTL threshold, with 35pF external capacitive loads.

Note 2: For CMOS output levels, see the "XC4000EX Output Level and Slew Rate Adjustments" on page -92.

## XC4000E Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.<sup>1</sup>

### XC4000E Absolute Maximum Ratings

Symbol	Description	Value	Units	
V <sub>CC</sub>	Supply voltage relative to GND	-0.5 to +7.0	V	
V <sub>IN</sub>	Input voltage relative to GND (Note 1)	-0.5 to V <sub>CC</sub> +0.5	V	
V <sub>TS</sub>	Voltage applied to 3-state output (Note 1)	-0.5 to V <sub>CC</sub> +0.5	V	
T <sub>TSG</sub>	Storage temperature (ambient)	-65 to +150	°C	
T <sub>SOL</sub>	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C	
T <sub>J</sub>	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above V<sub>CC</sub> or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to V<sub>CC</sub> + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### XC4000E Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V <sub>CC</sub>	Supply voltage relative to GND, T <sub>J</sub> = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T <sub>J</sub> = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T <sub>C</sub> = -55°C to +125°C	Military	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	TTL inputs	2.0	V <sub>CC</sub>	V
		CMOS inputs	70%	100%	V <sub>CC</sub>
V <sub>IL</sub>	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V <sub>CC</sub>
T <sub>IN</sub>	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

## XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0\text{mA}$ , $V_{CC}$ min	TTL outputs	2.4		V
	High-level output voltage @ $I_{OH} = -1.0\text{mA}$ , $V_{CC}$ min	CMOS outputs	$V_{CC}-0.5$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0\text{mA}$ , $V_{CC}$ min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
		Military		6.0	mA
$I_L$	Input or output leakage current		-10	+10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
$I_{RIN^*}$	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ (sample tested)		-0.02	-0.25	mA
$I_{RLL^*}$	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a Development system Tie option.

Note 3: \*Characterized Only.

## XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
From pad through Primary buffer, to any clock K	$T_{PG}$	XC4003E	7.0	4.7	4.0	3.5	ns
		XC4005E	7.0	4.7	4.3	3.8	ns
		XC4006E	7.5	5.3	5.2	4.6	ns
		XC4008E	8.0	6.1	5.2	4.6	ns
		XC4010E	11.0	6.3	5.4	4.8	ns
		XC4013E	11.5	6.8	5.8	5.2	ns
		XC4020E	12.0	7.0	6.4	6.0	ns
		XC4025E	12.5	7.2	6.9	—	ns
From pad through Secondary buffer, to any clock K	$T_{SG}$	XC4003E	7.5	5.2	4.4	4.0	ns
		XC4005E	7.5	5.2	4.7	4.3	ns
		XC4006E	8.0	5.8	5.6	5.1	ns
		XC4008E	8.5	6.6	5.6	5.1	ns
		XC4010E	11.5	6.8	5.8	5.3	ns
		XC4013E	12.0	7.3	6.2	5.7	ns
		XC4020E	12.5	7.5	6.7	6.5	ns
		XC4025E	13.0	7.7	7.2	—	ns

Preliminary

## XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade		-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	
<b>TBUF driving a Horizontal Longline (LL):</b>								
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T <sub>IO1</sub>	XC4003E	5.0	4.2	3.4	2.9	ns	
		XC4005E	5.0	5.0	4.0	3.4	ns	
		XC4006E	6.0	5.9	4.7	4.0	ns	
		XC4008E	7.0	6.3	5.0	4.3	ns	
		XC4010E	8.0	6.4	5.1	4.4	ns	
		XC4013E	9.0	7.2	5.7	4.9	ns	
		XC4020E	10.0	8.2	7.3	5.6	ns	
		XC4025E	11.0	9.1	7.3	—	ns	
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T <sub>IO2</sub>	XC4003E	5.0	4.2	3.6	3.1	ns	
		XC4005E	6.0	5.3	4.5	3.8	ns	
		XC4006E	7.8	6.4	5.4	4.6	ns	
		XC4008E	8.1	6.8	5.8	4.9	ns	
		XC4010E	10.5	6.9	5.9	5.0	ns	
		XC4013E	11.0	7.7	6.5	5.5	ns	
		XC4020E	12.0	8.7	8.7	7.4	ns	
		XC4025E	12.0	9.6	9.6	—	ns	
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T <sub>ON</sub>	XC4003E	5.5	4.6	3.9	3.5	ns	
		XC4005E	7.0	6.0	5.7	4.7	ns	
		XC4006E	7.5	6.7	5.7	4.9	ns	
		XC4008E	8.0	7.1	6.0	5.2	ns	
		XC4010E	8.5	7.3	6.2	5.4	ns	
		XC4013E	8.7	7.5	7.0	6.2	ns	
		XC4020E	11.0	8.4	7.1	6.3	ns	
		XC4025E	11.0	8.4	7.1	—	ns	
T going High to TBUF going inactive, not driving LL	T <sub>OFF</sub>	All devices	1.8	1.5	1.3	1.1	ns	
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	T <sub>PUS</sub>	XC4003E	20.0	14.0	14.0	12.0	ns	
		XC4005E	23.0	16.0	16.0	14.0	ns	
		XC4006E	25.0	18.0	18.0	16.0	ns	
		XC4008E	27.0	20.0	20.0	16.0	ns	
		XC4010E	29.0	22.0	22.0	18.0	ns	
		XC4013E	32.0	26.0	26.0	21.0	ns	
		XC4020E	35.0	32.5	32.5	26.0	ns	
		XC4025E	42.0	39.1	39.1	—	ns	
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T <sub>PUF</sub>	XC4003E	9.0	7.0	6.0	5.4	ns	
		XC4005E	10.0	8.0	6.8	5.8	ns	
		XC4006E	11.5	9.0	7.7	6.5	ns	
		XC4008E	12.5	10.0	8.5	7.5	ns	
		XC4010E	13.5	11.0	9.4	8.0	ns	
		XC4013E	15.0	13.0	11.7	9.4	ns	
		XC4020E	16.0	14.8	14.8	10.5	ns	
		XC4025E	18.0	16.5	16.5	—	ns	

Preliminary

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

## XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2	-1	
Description	Symbol	Device	Max	Max	Max	Max	Units
Full length, both pull-ups, inputs from IOB I-pins	$T_{WAF}$	XC4003E	9.2	5.0	5.0	4.3	ns
		XC4005E	9.5	6.0	6.0	5.1	ns
		XC4006E	12.0	7.0	7.0	6.0	ns
		XC4008E	12.5	8.0	8.0	6.5	ns
		XC4010E	15.0	9.0	9.0	7.5	ns
		XC4013E	16.0	11.0	11.0	8.6	ns
		XC4020E	17.0	13.9	13.9	10.1	ns
		XC4025E	18.0	16.9	16.9	—	ns
Full length, both pull-ups, inputs from internal logic	$T_{WAFL}$	XC4003E	12.0	7.0	7.0	5.5	ns
		XC4005E	12.5	8.0	8.0	6.4	ns
		XC4006E	14.0	9.0	9.0	7.0	ns
		XC4008E	16.0	10.0	10.0	7.5	ns
		XC4010E	18.0	11.0	11.0	8.5	ns
		XC4013E	19.0	13.0	13.0	10.0	ns
		XC4020E	20.0	15.5	15.5	11.8	ns
		XC4025E	21.0	18.9	18.9	—	ns
Half length, one pull-up, inputs from IOB I-pins	$T_{WAO}$	XC4003E	10.5	6.0	6.0	5.1	ns
		XC4005E	10.5	7.0	7.0	6.0	ns
		XC4006E	13.5	8.0	8.0	6.5	ns
		XC4008E	14.0	9.0	9.0	7.0	ns
		XC4010E	16.0	10.0	10.0	7.5	ns
		XC4013E	17.0	12.0	12.0	10.0	ns
		XC4020E	18.0	15.0	15.0	11.8	ns
		XC4025E	19.0	17.6	17.6	—	ns
Half length, one pull-up, inputs from internal logic	$T_{WAOL}$	XC4003E	12.0	8.0	8.0	6.0	ns
		XC4005E	12.5	9.0	9.0	7.0	ns
		XC4006E	14.0	10.0	10.0	7.6	ns
		XC4008E	16.0	11.0	11.0	8.4	ns
		XC4010E	18.0	12.0	12.0	9.2	ns
		XC4013E	19.0	14.0	14.0	10.8	ns
		XC4020E	20.0	16.8	16.8	12.6	ns
		XC4025E	21.0	19.6	19.6	—	ns

Preliminary

Note 1: These delays are specified from the decoder input to the decoder output.

Note 2: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

## XC4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Combinatorial Delays</b>										
F/G inputs to X/Y outputs	T <sub>ILO</sub>		2.7		2.0		1.6		1.3	ns
F/G inputs via H to X/Y outputs	T <sub>IHO</sub>		4.7		4.3		2.7		2.2	ns
C inputs via SR through H to X/Y outputs	T <sub>HH0O</sub>		4.1		3.3		2.4		1.9	ns
C inputs via H to X/Y outputs	T <sub>HH1O</sub>		3.7		3.6		2.2		1.6	ns
C inputs via DIN through H to X/Y outputs	T <sub>HH2O</sub>		4.5		3.6		2.6		1.9	ns
<b>CLB Fast Carry Logic</b>										
Operand inputs (F1, F2, G1, G4) to COUT	T <sub>OPCY</sub>		3.2		2.6		2.1		1.7	ns
Add/Subtract input (F3) to COUT	T <sub>ASCY</sub>		5.5		4.4		3.7		2.5	ns
Initialization inputs (F1, F3) to COUT	T <sub>INCY</sub>		1.7		1.7		1.4		1.2	ns
CIN through function generators to X/Y outputs	T <sub>SUM</sub>		3.8		3.3		2.6		1.8	ns
CIN to COUT, bypass function generators	T <sub>BYP</sub>		1.0		0.7		0.6		0.5	ns
<b>Sequential Delays</b>										
Clock K to outputs Q	T <sub>CKO</sub>		3.7		2.8		2.8		1.9	ns
<b>Setup Time before Clock K</b>										
F/G inputs	T <sub>IICK</sub>	4.0		3.0		2.4		1.8		ns
F/G inputs via H	T <sub>IHCK</sub>	6.1		4.6		3.9		2.8		ns
C inputs via H0 through H	T <sub>HH0CK</sub>	4.5		3.6		3.5		2.4		ns
C inputs via H1 through H	T <sub>HH1CK</sub>	5.0		4.1		3.3		2.1		ns
C inputs via H2 through H	T <sub>HH2CK</sub>	4.8		3.8		3.7		2.5		ns
C inputs via DIN	T <sub>DICK</sub>	3.0		2.4		2.0		1.0		ns
C inputs via EC	T <sub>ECKK</sub>	4.0		3.0		2.6		2.0		ns
C inputs via S/R, going Low (inactive)	T <sub>RCK</sub>	4.2		4.0		4.0		1.5		ns
C <sub>IN</sub> input via F/G	T <sub>CCK</sub>	2.5		2.1						ns
C <sub>IN</sub> input via F/G and H	T <sub>CHCK</sub>	4.2		3.5						ns

Preliminary

## XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Hold Time after Clock K</b>										
F/G inputs	$T_{CKI}$	0		0		0		0		ns
F/G inputs via H	$T_{CKIH}$	0		0		0		0		ns
C inputs via H0 through H	$T_{CKHH0}$	0		0		0		0		ns
C inputs via H1 through H	$T_{CKHH1}$	0		0		0		0		ns
C inputs via H2 through H	$T_{CKHH2}$	0		0		0		0		ns
C inputs via DIN	$T_{CKDI}$	0		0		0		0		ns
C inputs via EC	$T_{CKEC}$	0		0		0		0		ns
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		0		0		0		ns
<b>Clock</b>										
Clock High time	$T_{CH}$	4.5		4.0		4.0		3.0		ns
Clock Low time	$T_{CL}$	4.5		4.0		4.0		3.0		ns
<b>Set/Reset Direct</b>										
Width (High)	$T_{RPW}$	5.5		4.0		4.0		3.0		ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		6.5		4.0		4.0		3.0	ns
<b>Master Set/Reset (Note 1)</b>										
Width (High or Low)	$T_{MRW}$	13.0		23.0		11.5		11.5		ns
Delay from Global Set/Reset net to Q	$T_{MRQ}$				18.7		17.4		15.0	ns
Global Set/Reset inactive to first active clock K edge	$T_{MRK}$									
Toggle Frequency (Note 2)	$F_{TOG}$		111		125		125		166	MHz
<b>Preliminary</b>										

Note 1: Timing is based on the XC4005E. For other devices see the static timing analyzer.

Note 2: Export Control Max. flip-flop toggle rate.

## XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

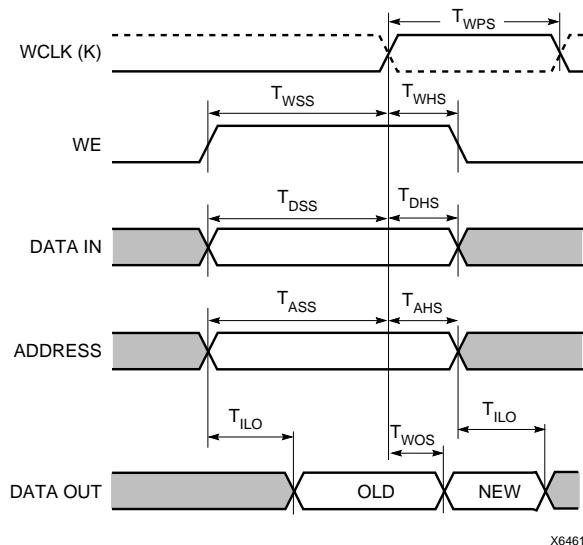
Single Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Write Operation</b>											
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCSTS}$	15.0 15.0		14.4 14.4		11.6 11.6		8.0 8.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPSTS}$	7.5 7.5	1 ms 1 ms	7.2 7.2	1 ms 1 ms	5.8 5.8	1 ms 1 ms	4.0 4.0		ns ns
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.8 2.8		2.4 2.4		2.0 2.0		1.5 1.5		ns ns
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHHTS}$	0 0		0 0		0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	3.5 2.5		3.2 1.9		2.7 1.7		1.5 1.5		ns ns
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHHTS}$	0 0		0 0		0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.2 2.2		2.0 2.0		1.6 1.6		1.5 1.5		ns ns
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHTS}$	0 0		0 0		0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$		10.3 11.6		8.8 10.3		7.9 9.3		6.5 7.0	ns ns
											Preliminary

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

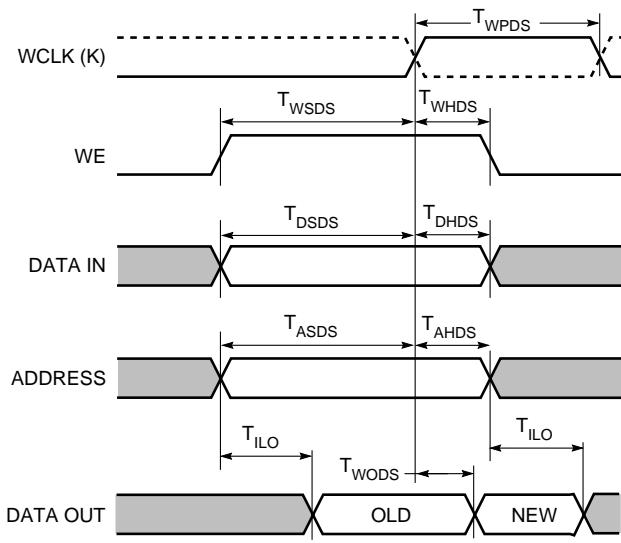
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Dual-Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Write Operation</b>											
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	15.0		14.4		11.6		8.0		ns
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	7.5	1 ms	7.2	1 ms	5.8	1 ms	4.0		ns
Address setup time before clock K	16x1	$T_{ASDS}$	7.5		2.5		2.1		1.5		ns
Address hold time after clock K	16x1	$T_{AHDS}$	2.8		0		0		0		ns
DIN setup time before clock K	16x1	$T_{DSDS}$	0		2.5		1.6		1.5		ns
DIN hold time after clock K	16x1	$T_{DHDS}$	2.2		0		0		0		ns
WE setup time before clock K	16x1	$T_{WSDS}$	0		1.8		1.6		1.5		ns
WE hold time after clock K	16x1	$T_{WHDS}$	2.2		0		0		0		ns
Data valid after clock K	16x1	$T_{WODS}$	0.3	10.0		7.8		7.0		6.5	ns
											Preliminary

Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

**XC4000E CLB RAM Synchronous (Edge-Triggered) Write Timing**

X6461

**XC4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing**

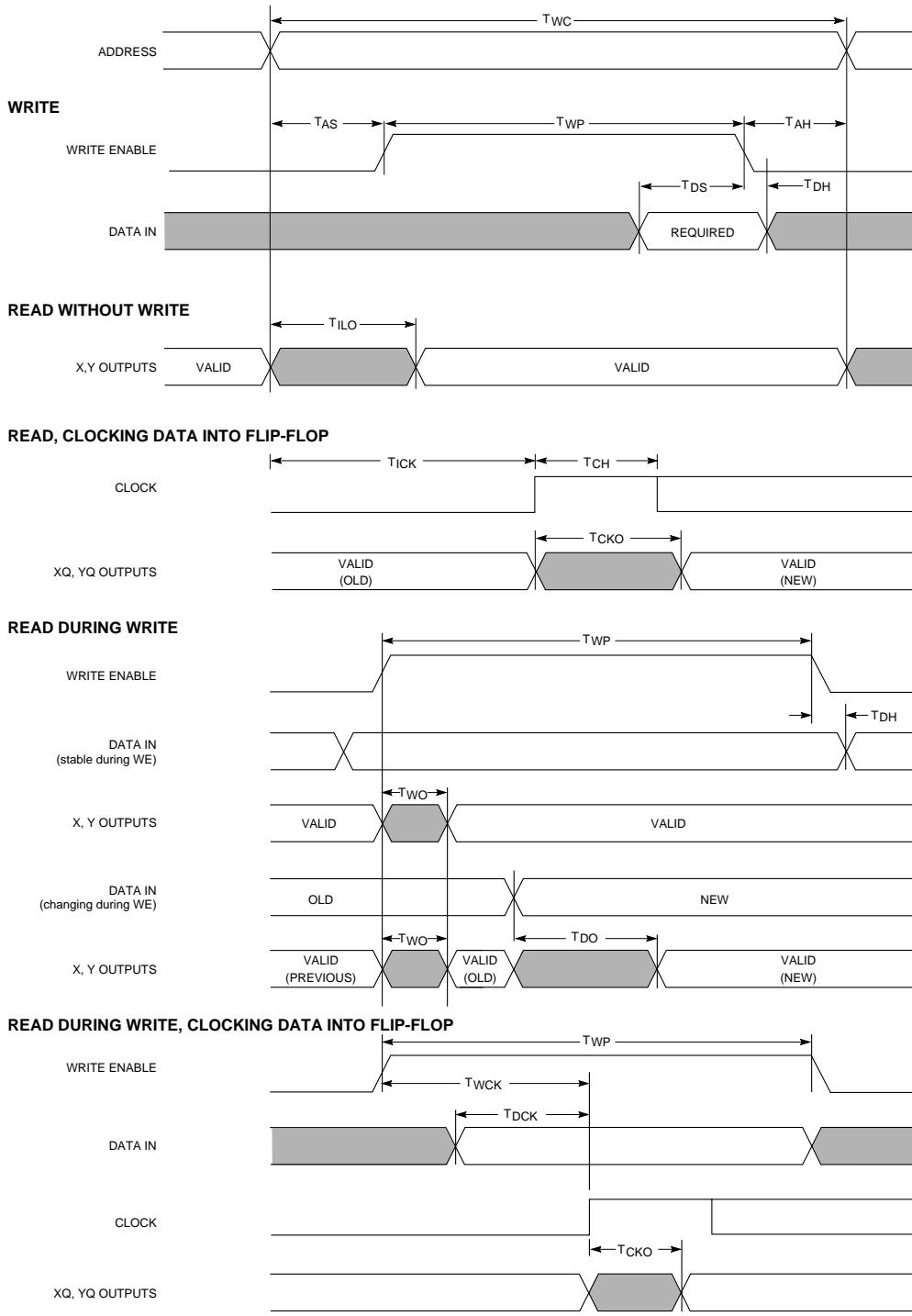
X6474

## XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1		Units		
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max			
<b>Write Operation</b>													
Address write cycle time	16x2 32x1	T <sub>WC</sub> T <sub>WCT</sub>	8.0 8.0		8.0 8.0		8.0 8.0		8.0 8.0		ns ns		
Write Enable pulse width (High)	16x2 32x1	T <sub>WP</sub> T <sub>WPT</sub>	4.0 4.0		4.0 4.0		4.0 4.0		4.0 4.0		ns ns		
Address setup time before WE	16x2 32x1	T <sub>AS</sub> T <sub>AST</sub>	2.0 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns		
Address hold time after end of WE	16x2 32x1	T <sub>AH</sub> T <sub>AHT</sub>	2.5 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns		
DIN setup time before end of WE	16x2 32x1	T <sub>DS</sub> T <sub>DST</sub>	4.0 5.0		2.2 2.2		0.8 0.8		0.8 0.8		ns ns		
DIN hold time after end of WE	16x2 32x1	T <sub>DH</sub> T <sub>DHT</sub>	2.0 2.0		2.0 2.0		2.0 2.0		2.0 2.0		ns ns		
<b>Read Operation</b>													
Address read cycle time	16x2 32x1	T <sub>RC</sub> T <sub>RCT</sub>	4.5 6.5		3.1 5.5		2.6 3.8		2.6 3.8		ns ns		
Data valid after address change (no Write Enable)	16x2 32x1	T <sub>ILO</sub> T <sub>IHO</sub>		2.7 4.7		1.8 3.2		1.6 2.7		1.6 2.7	ns ns		
<b>Read Operation, Clocking Data into Flip-Flop</b>													
Address setup time before clock K	16x2 32x1	T <sub>ICK</sub> T <sub>IHK</sub>	4.0 6.1		3.0 4.6		2.4 3.9		2.4 3.9		ns ns		
<b>Read During Write</b>													
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T <sub>WO</sub> T <sub>WOT</sub>		10.0 12.0		6.0 7.3		4.9 5.6		4.9 5.6	ns ns		
Data valid after DIN (DIN changes during WE)	16x2 32x1	T <sub>DO</sub> T <sub>DOT</sub>		9.0 11.0		6.6 7.6		5.8 6.2		5.8 6.2	ns ns		
<b>Read During Write, Clocking Data into Flip-Flop</b>													
WE setup time before clock K	16x2 32x1	T <sub>WCK</sub> T <sub>WCKT</sub>	8.0 9.6		6.0 6.8		5.1 5.8		5.1 5.8		ns ns		
Data setup time before clock K	16x2 32x1	T <sub>DCK</sub> T <sub>DCKT</sub>	7.0 8.0		5.2 6.2		4.4 5.3		4.4 5.3		ns ns		
<b>Preliminary</b>													

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

**XC4000E CLB Level-Sensitive RAM Timing Characteristics**

X2640

## XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4	-3	-2	-1	Units
Description	Symbol	Device				
Global Clock to Output (fast) using OFF	(Max)	XC4003E	12.5	10.2	8.7	5.8
		XC4005E	14.0	10.7	9.1	6.2
		XC4006E	14.5	10.7	9.1	6.4
		XC4008E	15.0	10.8	9.2	6.6
		XC4010E	16.0	10.9	9.3	6.8
		XC4013E	16.5	11.0	9.4	7.2
		XC4020E	17.0	11.0	10.2	7.4
		XC4025E	17.0	12.6	10.8	—
Global Clock to Output (slew-limited) using OFF	(Max)	XC4003E	16.5	14.0	11.5	7.8
		XC4005E	18.0	14.7	12.0	8.2
		XC4006E	18.5	14.7	12.0	8.4
		XC4008E	19.0	14.8	12.1	8.6
		XC4010E	20.0	14.9	12.2	8.8
		XC4013E	20.5	15.0	12.8	9.2
		XC4020E	21.0	15.1	12.8	9.4
		XC4025E	21.0	15.3	13.0	—
Input Setup Time, using IFF (no delay)	(Min)	XC4003E	2.5	2.3	2.3	1.5
		XC4005E	2.0	1.2	1.2	0.8
		XC4006E	1.9	1.0	1.0	0.6
		XC4008E	1.4	0.6	0.6	0.2
		XC4010E	1.0	0.2	0.2	0
		XC4013E	0.5	0	0	0
		XC4020E	0	0	0	0
		XC4025E	0	0	0	—
Input Hold Time, using IFF (no delay)	(Min)	XC4003E	4.0	4.0	4.0	1.5
		XC4005E	4.6	4.5	4.5	2.0
		XC4006E	5.0	4.7	4.7	2.0
		XC4008E	6.0	5.1	5.1	2.5
		XC4010E	6.0	5.5	5.5	2.5
		XC4013E	7.0	6.5	5.5	3.0
		XC4020E	7.5	6.7	5.7	3.5
		XC4025E	8.0	7.0	5.9	—
Input Setup Time, using IFF (with delay)	(Min)	XC4003E	8.5	7.0	6.0	5.0
		XC4005E	8.5	7.0	6.0	5.0
		XC4006E	8.5	7.0	6.0	5.0
		XC4008E	8.5	7.0	6.0	5.0
		XC4010E	8.5	7.0	6.0	5.0
		XC4013E	8.5	7.0	6.0	5.0
		XC4020E	9.5	7.0	6.8	5.0
		XC4025E	9.5	7.6	6.8	—
Input Hold Time, using IFF (with delay)	(Min)	XC4003E	0	0	0	0
		XC4005E	0	0	0	0
		XC4006E	0	0	0	0
		XC4008E	0	0	0	0
		XC4010E	0	0	0	0
		XC4013E	0	0	0	0
		XC4020E	0	0	0	0
		XC4025E	0	0	0	—

OFF = Output Flip-Flop

IFF = Input Flip-Flop or Latch

Preliminary

## XC4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Device	Min	Max	Min	Max	Min	Max	Min	Max
<b>Propagation Delays (TTL Inputs)</b>										
Pad to I1, I2										
Pad to I1, I2 via transparent latch, no delay with delay	$T_{PID}$ $T_{PLI}$ $T_{PDLI}$	All devices	3.0		2.5		2.0		1.4	ns
		All devices	4.8		3.6		3.6		2.8	ns
		XC4003E	10.4		9.3		6.9		6.4	ns
		XC4005E	10.8		9.6		7.4		6.5	ns
		XC4006E	10.8		10.2		8.1		6.9	ns
		XC4008E	10.8		10.6		8.2		7.0	ns
		XC4010E	11.0		10.8		8.3		7.3	ns
		XC4013E	11.4		11.2		9.8		8.4	ns
		XC4020E	13.8		12.4		11.5		9.0	ns
		XC4025E	13.8		13.7		12.4		—	ns
<b>Propagation Delays (CMOS Inputs)</b>										
Pad to I1, I2	$T_{PIDC}$ $T_{PLIC}$ $T_{PDLC}$	All devices	5.5		4.1		3.7		1.9	ns
Pad to I1, I2 via transparent latch, no delay with delay		All devices	8.8		6.8		6.2		3.3	ns
		XC4003E	16.5		12.4		11.0		6.9	ns
		XC4005E	16.5		13.2		11.9		7.0	ns
		XC4006E	16.8		13.4		12.1		7.4	ns
		XC4008E	17.3		13.8		12.4		7.4	ns
		XC4010E	17.5		14.0		12.6		7.8	ns
		XC4013E	18.0		14.4		13.0		9.0	ns
		XC4020E	20.8		15.6		14.0		9.5	ns
		XC4025E	20.8		15.6		14.0		—	ns
<b>Propagation Delays</b>										
Clock (IK) to I1, I2 (flip-flop)	$T_{IKRI}$	All devices	5.6		2.8		2.8		2.7	ns
Clock (IK) to I1, I2 (latch enable, active Low)		All devices	6.2		4.0		3.9		3.2	ns
<b>Hold Times (Note 1)</b>										
Pad to Clock (IK), no delay with delay	$T_{IKPI}$ $T_{IKPID}$	All devices	0		0		0		0	ns
Clock Enable (EC) to Clock (IK), no delay with delay		All devices	0		0		0		0	ns
	$T_{IKEC}$ $T_{IKECD}$	All devices	1.5		1.5		0.9		0	ns
		All devices	0		0		0		0	ns

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Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Device	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
<b>Setup Times (TTL Inputs)</b>												
Pad to Clock (IK), no delay with delay	$T_{PICK}$	All devices	4.0		2.6		2.0		1.5		ns	
	$T_{PICKD}$	XC4003E	10.9		8.2		6.0		4.8		ns	
		XC4005E	10.9		8.7		6.1		5.1		ns	
		XC4006E	10.9		9.2		6.2		5.8		ns	
		XC4008E	11.1		9.6		6.3		5.8		ns	
		XC4010E	11.3		9.8		6.4		6.0		ns	
		XC4013E	11.8		10.2		7.9		7.6		ns	
		XC4020E	14.0		11.4		9.4		8.2		ns	
		XC4025E	14.0		11.4		10.0		—		ns	
<b>Setup Time (CMOS Inputs)</b>												
Pad to Clock (IK), no delay with delay	$T_{PICKC}$	All devices	6.0		3.3		2.4		2.4		ns	
	$T_{PICKDC}$	XC4003E	12.0		8.8		6.9		5.3		ns	
		XC4005E	12.0		9.7		8.0		5.6		ns	
		XC4006E	12.3		9.9		8.1		6.3		ns	
		XC4008E	12.8		10.3		8.2		6.3		ns	
		XC4010E	13.0		10.5		8.3		6.5		ns	
		XC4013E	13.5		10.9		10.0		7.9		ns	
		XC4020E	16.0		12.1		12.1		8.1		ns	
		XC4025E	16.0		12.1		12.1		—		ns	
<b>(TTL or CMOS)</b>												
Clock Enable (EC) to Clock (IK), no delay with delay	$T_{ECIK}$	All devices	3.5		2.5		2.1		1.5		ns	
	$T_{ECIKD}$	XC4003E	10.4		8.1		4.3		4.3		ns	
		XC4005E	10.4		8.5		5.6		5.0		ns	
		XC4006E	10.4		9.1		6.7		6.0		ns	
		XC4008E	10.4		9.5		6.9		6.0		ns	
		XC4010E	10.7		9.7		7.1		6.5		ns	
		XC4013E	11.1		10.1		9.0		8.0		ns	
		XC4020E	14.0		11.3		10.6		9.0		ns	
		XC4025E	14.0		11.3		11.0		—		ns	
<b>Global Set/Reset (Note 3)</b>												
Delay from GSR net through Q to I1, I2	$T_{RRI}$			12.0		7.8		6.8		6.8		ns
GSR width	$T_{MRW}$		13.0		11.5		11.5		10.0			ns
GSR inactive to first active Clock (IK) edge	$T_{MRI}$											

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Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

## XC4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Propagation Delays (TTL Output Levels)</b>										
Clock (OK) to Pad, fast slew-rate limited	$T_{OKPOF}$			7.5		6.5		4.5		3.0 ns
Output (O) to Pad, fast slew-rate limited	$T_{OKPOS}$			11.5		9.5		7.0		5.0 ns
3-state to Pad hi-Z (slew-rate independent)	$T_{OPF}$			8.0		5.5		4.8		3.2 ns
3-state to Pad active and valid, fast slew-rate limited	$T_{OPS}$			12.0		8.5		7.3		5.2 ns
	$T_{TSHZ}$			5.0		4.2		3.8		3.0 ns
	$T_{TSONF}$			9.7		8.1		7.3		6.8 ns
	$T_{TSONS}$			13.7		11.1		9.8		8.8 ns
<b>Propagation Delays (CMOS Output Levels)</b>										
Clock (OK) to Pad, fast slew-rate limited	$T_{OKPOFC}$			9.5		7.8		7.0		4.0 ns
Output (O) to Pad, fast slew-rate limited	$T_{OKPOSC}$			13.5		11.6		10.4		7.0 ns
3-state to Pad hi-Z (slew-rate independent)	$T_{OPFC}$			10.0		9.7		8.7		4.0 ns
3-state to Pad active and valid, fast slew-rate limited	$T_{OPSC}$			14.0		13.4		12.1		6.0 ns
	$T_{TSHZC}$			5.2		4.3		3.9		3.9 ns
	$T_{TSONFC}$			9.1		7.6		6.8		6.8 ns
	$T_{TSONSC}$			13.1		11.4		10.2		8.8 ns

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Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Setup and Hold</b>										
Output (O) to clock (OK) setup time	$T_{OOK}$	5.0		4.6		3.8		2.3		ns
Output (O) to clock (OK) hold time	$T_{OKO}$	0		0		0		0		ns
Clock Enable (EC) to clock (OK) setup	$T_{ECOK}$	4.8		3.5		2.7		2.0		ns
Clock Enable (EC) to clock (OK) hold	$T_{OKEC}$	1.2		1.2		0.5		0		ns
<b>Clock</b>										
Clock High	$T_{CH}$	4.5		4.0		4.0		3.0		ns
Clock Low	$T_{CL}$	4.5		4.0		4.0		3.0		ns
<b>Global Set/Reset (Note 3)</b>										
Delay from GSR net to Pad GSR width	$T_{RPO}$	13.0	15.0	11.5	11.8	11.5	8.7		7.0	ns
GSR inactive to first active clock (OK) edge	$T_{MRW}$									ns
	$T_{MRO}$									

Preliminary

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

## XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
<b>Setup and Hold</b>										
Input (TDI) to clock (TCK) setup time	$T_{TDITCK}$	30.0		30.0		30.0		20.0		ns
Input (TDI) to clock (TCK) hold time	$T_{TCKTDI}$	0		0		0		0		ns
Input (TMS) to clock (TCK) setup time	$T_{TMSTCK}$	15.0		15.0		15.0		10.0		ns
Input (TMS) to clock (TCK) hold time	$T_{TCKTMS}$	0		0		0		0		ns
<b>Propagation Delay</b>										
Clock (TCK) to Pad (TDO)	$T_{TCKPO}$		30.0		30.0		30.0		20.0	ns
<b>Clock</b>										
Clock (TCK) High	$T_{TCKH}$	5.0		5.0		5.0		4.0		ns
Clock (TCK) Low	$T_{TCKL}$	5.0		5.0		5.0		4.0		ns
$F_{MAX}$ (MHz)	$F_{MAX}$		15.0		15.0		15.0		25.0	ns
<b>Preliminary</b>										

- Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
- Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.
- Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## Device-Specific Pinout Tables

Device-specific tables include all packages for each XC4000 and XC4000X Series device. They follow the pad locations around the die, and include boundary scan register locations..

### Pin Locations for XC4003E Devices

XC4003E Pad Name	PC84	PQ100	VQ100	PG120	Bndry Scan
VCC	P2	P92	P89	G3	-
I/O (A8)	P3	P93	P90	G1	32
I/O (A9)	P4	P94	P91	F1	35
I/O	-	P95	P92	E1	38
I/O	-	P96	P93	F2	41
I/O (A10)	P5	P97	P94	F3	44
I/O (A11)	P6	P98	P95	D1	47
I/O (A12)	P7	P99	P96	C1	50
I/O (A13)	P8	P100	P97	D2	53
I/O (A14)	P9	P1	P98	C2	56
I/O, SGCK1 (A15)	P10	P2	P99	D3	59
VCC	P11	P3	P100	C3	-
GND	P12	P4	P1	C4	-
I/O, PGCK1 (A16)	P13	P5	P2	B2	62
I/O (A17)	P14	P6	P3	B3	65
I/O, TDI	P15	P7	P4	C5	68
I/O, TCK	P16	P8	P5	B4	71
I/O, TMS	P17	P9	P6	B5	74
I/O	P18	P10	P7	A4	77
I/O	-	-	-	C6	80
I/O	-	P11	P8	A5	83
I/O	P19	P12	P9	B6	86
I/O	P20	P13	P10	A6	89
GND	P21	P14	P11	B7	-
VCC	P22	P15	P12	C7	-
I/O	P23	P16	P13	A7	92
I/O	P24	P17	P14	A8	95
I/O	-	P18	P15	A9	98
I/O	-	-	-	B8	101
I/O	P25	P19	P16	C8	104
I/O	P26	P20	P17	A10	107
I/O	P27	P21	P18	B9	110
I/O	-	P22	P19	A11	113
I/O	P28	P23	P20	C9	116
I/O, SGCK2	P29	P24	P21	A12	119
O (M1)	P30	P25	P22	B11	122
GND	P31	P26	P23	C10	-
I (M0)	P32	P27	P24	C11	125
VCC	P33	P28	P25	D11	-
I (M2)	P34	P29	P26	B12	126
I/O, PGCK2	P35	P30	P27	C12	127
I/O (HDC)	P36	P31	P28	A13	130
I/O	-	P32	P29	D12	133
I/O (LDC)	P37	P33	P30	C13	136
I/O	P38	P34	P31	E12	139
I/O	P39	P35	P32	D13	142
I/O	-	P36	P33	F11	145
I/O	-	P37	P34	E13	148
I/O	P40	P38	P35	F12	151
I/O (INIT)	P41	P39	P36	F13	154
VCC	P42	P40	P37	G12	-
GND	P43	P41	P38	G11	-
I/O	P44	P42	P39	G13	157
I/O	P45	P43	P40	H13	160
I/O	-	P44	P41	J13	163
I/O	-	P45	P42	H12	166
I/O	P46	P46	P43	H11	169

XC4003E Pad Name	PC84	PQ100	VQ100	PG120	Bndry Scan
I/O	P47	P47	P44	K13	172
I/O	P48	P48	P45	J12	175
I/O	P49	P49	P46	L13	178
I/O	P50	P50	P47	M13	181
I/O, SGCK3	P51	P51	P48	L12	184
GND	P52	P52	P49	K11	-
DONE	P53	P53	P50	L11	-
VCC	P54	P54	P51	L10	-
PROGRAM	P55	P55	P52	M12	-
I/O (D7)	P56	P56	P53	M11	187
I/O, PGCK3	P57	P57	P54	N13	190
I/O (D6)	P58	P58	P55	M10	193
I/O	-	P59	P56	N11	196
I/O (D5)	P59	P60	P57	M9	199
I/O (CS0)	P60	P61	P58	N10	202
I/O	-	P62	P59	L8	205
I/O	-	P63	P60	N9	208
I/O (D4)	P61	P64	P61	M8	211
I/O	P62	P65	P62	N8	214
VCC	P63	P66	P63	M7	-
GND	P64	P67	P64	L7	-
I/O (D3)	P65	P68	P65	N7	217
I/O (RS)	P66	P69	P66	N6	220
I/O	-	P70	P67	N5	223
I/O	-	-	-	M6	226
I/O (D2)	P67	P71	P68	L6	229
I/O	P68	P72	P69	N4	232
I/O (D1)	P69	P73	P70	M5	235
I/O (RCLK, RDY/BUSY)	P70	P74	P71	N3	238
I/O (D0, DIN)	P71	P75	P72	N2	241
I/O, SGCK4 (DOUT)	P72	P76	P73	M3	244
CCLK	P73	P77	P74	L4	-
VCC	P74	P78	P75	L3	-
O, TDO	P75	P79	P76	M2	0
GND	P76	P80	P77	K3	-
I/O (A0, WS)	P77	P81	P78	L2	2
I/O, PGCK4 (A1)	P78	P82	P79	N1	5
I/O (CS1, A2)	P79	P83	P80	K2	8
I/O (A3)	P80	P84	P81	L1	11
I/O (A4)	P81	P85	P82	J2	14
I/O (A5)	P82	P86	P83	K1	17
I/O	-	P87	P84	H3	20
I/O	-	P88	P85	J1	23
I/O (A6)	P83	P89	P86	H2	26
I/O (A7)	P84	P90	P87	H1	29
GND	P1	P91	P88	G2	-

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### Additional XC4003E Package Pins

#### PG120

Not Connected Pins					
A1	A2	A3	B1	B10	B13
E2	E3	E11	J3	J11	K12
L5	L9	M1	M4	N12	-

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## Pin Locations for XC4005E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
VCC	P2	P92	P89	P128	H3	P142	P183	-
I/O (A8)	P3	P93	P90	P129	H1	P143	P184	44
I/O (A9)	P4	P94	P91	P130	G1	P144	P185	47
I/O (A19) ††	-	P95	P92	P131	G2	P145	P186	50
I/O (A18) ††	-	P96	P93	P132	G3	P146	P187	53
I/O (A10)	P5	P97	P94	P133	F1	P147	P190	56
I/O (A11)	P6	P98	P95	P134	F2	P148	P191	59
I/O	-	-	-	P135	E1	P149	P192	62
I/O	-	-	-	P136	E2	P150	P193	65
GND	-	-	-	P137	F3	P151	P194	-
I/O (A12)	P7	P99	P96	P138	E3	P154	P199	68
I/O (A13)	P8	P100	P97	P139	C1	P155	P200	71
I/O	-	-	-	P140	C2	P156	P201	74
I/O	-	-	-	P141	D3	P157	P202	77
I/O (A14)	P9	P1	P98	P142	B1	P158	P203	80
I/O, SGCK1 †, GCK8 †† (A15)	P10	P2	P99	P143	B2	P159	P204	83
VCC	P11	P3	P100	P144	C3	P160	P205	-
GND	P12	P4	P1	P1	C4	P1	P2	-
I/O, PGCK1 †, GCK1 †† (A16)	P13	P5	P2	P2	B3	P2	P4	86
I/O (A17)	P14	P6	P3	P3	A1	P3	P5	89
I/O	-	-	-	P4	A2	P4	P6	92
I/O	-	-	-	P5	C5	P5	P7	95
I/O, TDI	P15	P7	P4	P6	B4	P6	P8	98
I/O, TCK	P16	P8	P5	P7	A3	P7	P9	101
GND	-	-	-	P8	C6	P10	P14	-
I/O	-	-	-	P9	B5	P11	P15	104
I/O	-	-	-	P10	B6	P12	P16	107
I/O, TMS	P17	P9	P6	P11	A5	P13	P17	110
I/O	P18	P10	P7	P12	C7	P14	P18	113
I/O	-	-	-	P13	B7	P15	P21	116
I/O	-	P11	P8	P14	A6	P16	P22	119
I/O	P19	P12	P9	P15	A7	P17	P23	122
I/O	P20	P13	P10	P16	A8	P18	P24	125
GND	P21	P14	P11	P17	C8	P19	P25	-
VCC	P22	P15	P12	P18	B8	P20	P26	-
I/O	P23	P16	P13	P19	C9	P21	P27	128
I/O	P24	P17	P14	P20	B9	P22	P28	131
I/O	-	P18	P15	P21	A9	P23	P29	134
I/O	-	-	-	P22	B10	P24	P30	137
I/O	P25	P19	P16	P23	C10	P25	P33	140
I/O	P26	P20	P17	P24	A10	P26	P34	143
I/O	-	-	-	P25	A11	P27	P35	146
I/O	-	-	-	P26	B11	P28	P36	149
GND	-	-	-	P27	C11	P29	P37	-
I/O	P27	P21	P18	P28	B12	P32	P42	152
I/O	-	P22	P19	P29	A13	P33	P43	155
I/O	-	-	-	P30	A14	P34	P44	158
I/O	-	-	-	P31	C12	P35	P45	161
I/O	P28	P23	P20	P32	B13	P36	P46	164
I/O, SGCK2 †, GCK2 ††	P29	P24	P21	P33	B14	P37	P47	167
O (M1)	P30	P25	P22	P34	A15	P38	P48	170
GND	P31	P26	P23	P35	C13	P39	P49	-
I (M0)	P32	P27	P24	P36	A16	P40	P50	173
VCC	P33	P28	P25	P37	C14	P41	P55	-
I (M2)	P34	P29	P26	P38	B15	P42	P56	174
I/O, PGCK2 †, GCK3 ††	P35	P30	P27	P39	B16	P43	P57	175
I/O (HDC)	P36	P31	P28	P40	D14	P44	P58	178
I/O	-	-	-	P41	C15	P45	P59	181
I/O	-	-	-	P42	D15	P46	P60	184
I/O	-	P32	P29	P43	E14	P47	P61	187
I/O (LDC)	P37	P33	P30	P44	C16	P48	P62	190

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PQ 156†	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
GND	-	-	-	-	-	P45	F14	P51	P67	-
I/O	-	-	-	-	-	P46	F15	P52	P68	193
I/O	-	-	-	-	-	P47	E16	P53	P69	196
I/O	P38	P34	P31	P48	F16	P54	P70	199		
I/O	P39	P35	P32	P49	G14	P55	P71	202		
I/O	-	P36	P33	P50	G15	P56	P74	205		
I/O	-	P37	P34	P51	G16	P57	P75	208		
I/O	P40	P38	P35	P52	H16	P58	P76	211		
I/O (INIT)	P41	P39	P36	P53	H15	P59	P77	214		
VCC	P42	P40	P37	P54	H14	P60	P78	-		
GND	P43	P41	P38	P55	J14	P61	P79	-		
I/O	P44	P42	P39	P56	J15	P62	P80	217		
I/O	P45	P43	P40	P57	J16	P63	P81	220		
I/O	-	P44	P41	P58	K16	P64	P82	223		
I/O	-	P45	P42	P59	K15	P65	P83	226		
I/O	P46	P46	P43	P60	K14	P66	P86	229		
I/O	P47	P47	P44	P61	L16	P67	P87	232		
I/O	-	-	-	P62	M16	P68	P88	235		
I/O	-	-	-	P63	L15	P69	P89	238		
GND	-	-	-	P64	L14	P70	P90	-		
I/O	P48	P48	P45	P65	P16	P73	P95	241		
I/O	P49	P49	P46	P66	M14	P74	P96	244		
I/O	-	-	-	P67	N15	P75	P97	247		
I/O	-	-	-	P68	P15	P76	P98	250		
I/O	P50	P50	P47	P69	N14	P77	P99	253		
I/O, SGCK3 †, GCK4 ††	P51	P51	P48	P70	R16	P78	P100	256		
GND	P52	P52	P49	P71	P14	P79	P101	-		
DONE	P53	P53	P50	P72	R15	P80	P103	-		
VCC	P54	P54	P51	P73	P13	P81	P106	-		
PROGRAM	P55	P55	P52	P74	R14	P82	P108	-		
I/O (D7)	P56	P56	P53	P75	T16	P83	P109	259		
I/O, PGCK3 †, GCK5 ††	P57	P57	P54	P76	T15	P84	P110	262		
I/O	-	-	-	P77	R13	P85	P111	265		
I/O	-	-	-	P78	P12	P86	P112	268		
I/O (D6)	P58	P58	P55	P79	T14	P87	P113	271		
I/O	-	P59	P56	P80	T13	P88	P114	274		
GND	-	-	-	P81	P11	P91	P119	-		
I/O	-	-	-	P82	R11	P92	P120	277		
I/O	-	-	-	P83	T11	P93	P121	280		
I/O (D5)	P59	P60	P57	P84	T10	P94	P122	283		
I/O (CS0)	P60	P61	P58	P85	P10	P95	P123	286		
I/O	-	P62	P59	P86	R10	P96	P126	289		
I/O	-	P63	P60	P87	T9	P97	P127	292		
I/O (D4)	P61	P64	P61	P88	R9	P98	P128	295		
I/O	P62	P65	P62	P89	P9	P99	P129	298		
VCC	P63	P66	P63	P90	R8	P100	P130	-		
GND	P64	P67	P64	P91	P8	P101	P131	-		
I/O (D3)	P65	P68	P65	P92	T8	P102	P132	301		
I/O (RS)	P66	P69	P66	P93	T7	P103	P133	304		
I/O	-	P70	P67	P94	T6	P104	P134	307		
I/O	-	-	-	P95	R7	P105	P135	310		
I/O (D2)	P67	P71	P68	P96	P7	P106	P138	313		
I/O	P68	P72	P69	P97	T5	P107	P139	316		
I/O	-	-	-	P98	R6	P108	P140	319		
I/O	-	-	-	P99	T4	P109	P141	322		
GND	-	-	-	P100	P6	P110	P142	-		
I/O (D1)	P69	P73	P70	P101	T3	P113	P147	325		
I/O (RCLK, RDY/BUSY)	P70	P74	P71	P102	P5	P114	P148	328		
I/O	-	-	-	P103	R4	P115	P149	331		
I/O	-	-	-	P104	R3	P116	P150	334		
I/O (D0, DIN)	P71	P75	P72	P105	P4	P117	P151	337		

XC4005E/XL Pad Name	PC 84	PQ 100	VQ 100††	TQ 144	PG 156†	PQ 160	PQ 208	Bndry Scan
I/O, SGCK4 †, GCK6 †† (DOUT)	P72	P76	P73	P106	T2	P118	P152	340
CCLK	P73	P77	P74	P107	R2	P119	P153	-
VCC	P74	P78	P75	P108	P3	P120	P154	-
O, TDO	P75	P79	P76	P109	T1	P121	P159	0
GND	P76	P80	P77	P110	N3	P122	P160	-
I/O (A0, WS)	P77	P81	P78	P111	R1	P123	P161	2
I/O, PGCK4 †, GCK7 †† (A1)	P78	P82	P79	P112	P2	P124	P162	5
I/O	-	-	-	P113	N2	P125	P163	8
I/O	-	-	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P83	P80	P115	P1	P127	P165	14
I/O (A3)	P80	P84	P81	P116	N1	P128	P166	17
GND	-	-	-	P118	L3	P131	P171	-
I/O	-	-	-	P119	L2	P132	P172	20
I/O	-	-	-	P120	L1	P133	P173	23
I/O (A4)	P81	P85	P82	P121	K3	P134	P174	26
I/O (A5)	P82	P86	P83	P122	K2	P135	P175	29
I/O (A21) ††	-	P87	P84	P123	K1	P137	P178	32
I/O (A20) ††	-	P88	P85	P124	J1	P138	P179	35
I/O (A6)	P83	P89	P86	P125	J2	P139	P180	38
I/O (A7)	P84	P90	P87	P126	J3	P140	P181	41
GND	P1	P91	P88	P127	H2	P141	P182	-

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† = E only

†† = XL only

## Additional XC4005E/XL Package Pins

TQ144

Not Connected Pins					
P117	-	-	-	-	-

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PQ156

Not Connected Pins					
A4	A12	D1	D2	D16	E15
M1	M2	M15	N16	R5	R12
T12	-	-	-	-	-

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PQ160

Not Connected Pins					
P8	P9	P30	P31	P49	P50
P71	P72	P89	P90	P111	P112

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PQ208

Not Connected Pins					
P1	P3	P10	P11	P12	P13
P19	P20	P31	P32	P38	P39
P40	P41	P51	P52	P53	P54
P63	P64	P65	P66	P72	P73
P84	P85	P91	P92	P93	P94
P102	P104	P105	P107	P115	P116
P117	P118	P124	P125	P136	P137
P143	P144	P145	P146	P155	P156
P157	P158	P167	P168	P169	P170
P176	P177	P188	P189	P195	P196
P197	P198	P206	P207	P208	-

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## Pin Locations for XC4006E Devices

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
VCC	P2	P128	H3	P142	P183	-
I/O (A8)	P3	P129	H1	P143	P184	50
I/O (A9)	P4	P130	G1	P144	P185	53
I/O	-	P131	G2	P145	P186	56
I/O	-	P132	G3	P146	P187	59
I/O (A10)	P5	P133	F1	P147	P190	62
I/O (A11)	P6	P134	F2	P148	P191	65
I/O	-	P135	E1	P149	P192	68
I/O	-	P136	E2	P150	P193	71
GND	-	P137	F3	P151	P194	-
I/O	-	-	D1	P152	P197	74
I/O	-	-	D2	P153	P198	77
I/O (A12)	P7	P138	E3	P154	P199	80
I/O (A13)	P8	P139	C1	P155	P200	83
I/O	-	P140	C2	P156	P201	86
I/O	-	P141	D3	P157	P202	89
I/O (A14)	P9	P142	B1	P158	P203	92
I/O, SGCK1 (A15)	P10	P143	B2	P159	P204	95
VCC	P11	P144	C3	P160	P205	-
GND	P12	P1	C4	P1	P2	-
I/O, PGCK1 (A16)	P13	P2	B3	P2	P4	98
I/O (A17)	P14	P3	A1	P3	P5	101
I/O	-	P4	A2	P4	P6	104
I/O	-	P5	C5	P5	P7	107
I/O, TDI	P15	P6	B4	P6	P8	110
I/O, TCK	P16	P7	A3	P7	P9	113
I/O	-	-	A4	P8	P10	116
I/O	-	-	-	P9	P11	119
GND	-	P8	C6	P10	P14	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I/O	-	P9	B5	P11	P15	122
I/O	-	P10	B6	P12	P16	125
I/O, TMS	P17	P11	A5	P13	P17	128
I/O	P18	P12	C7	P14	P18	131
I/O	-	P13	B7	P15	P21	134
I/O	-	P14	A6	P16	P22	137
I/O	P19	P15	A7	P17	P23	140
I/O	P20	P16	A8	P18	P24	143
GND	P21	P17	C8	P19	P25	-
VCC	P22	P18	B8	P20	P26	-
I/O	P23	P19	C9	P21	P27	146
I/O	P24	P20	B9	P22	P28	149
I/O	-	P21	A9	P23	P29	152
I/O	-	P22	B10	P24	P30	155
I/O	P25	P23	C10	P25	P33	158
I/O	P26	P24	A10	P26	P34	161
I/O	-	P25	A11	P27	P35	164
I/O	-	P26	B11	P28	P36	167
GND	-	P27	C11	P29	P37	-
I/O	-	-	A12	P30	P40	170
I/O	-	-	-	P31	P41	173
I/O	P27	P28	B12	P32	P42	176
I/O	-	P29	A13	P33	P43	179
I/O	-	P30	A14	P34	P44	182
I/O	-	P31	C12	P35	P45	185
I/O	P28	P32	B13	P36	P46	188
I/O, SGCK2	P29	P33	B14	P37	P47	191
O (M1)	P30	P34	A15	P38	P48	194
GND	P31	P35	C13	P39	P49	-

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I (M0)	P32	P36	A16	P40	P50	197
VCC	P33	P37	C14	P41	P55	-
I (M2)	P34	P38	B15	P42	P56	198
I/O, PGCK2	P35	P39	B16	P43	P57	199
I/O (HDC)	P36	P40	D14	P44	P58	202
I/O	-	P41	C15	P45	P59	205
I/O	-	P42	D15	P46	P60	208
I/O	-	P43	E14	P47	P61	211
I/O (LDC)	P37	P44	C16	P48	P62	214
I/O	-	-	E15	P49	P63	217
I/O	-	-	D16	P50	P64	220
GND	-	P45	F14	P51	P67	-
I/O	-	P46	F15	P52	P68	223
I/O	-	P47	E16	P53	P69	226
I/O	P38	P48	F16	P54	P70	229
I/O	P39	P49	G14	P55	P71	232
I/O	-	P50	G15	P56	P74	235
I/O	-	P51	G16	P57	P75	238
I/O	P40	P52	H16	P58	P76	241
I/O (INIT)	P41	P53	H15	P59	P77	244
VCC	P42	P54	H14	P60	P78	-
GND	P43	P55	J14	P61	P79	-
I/O	P44	P56	J15	P62	P80	247
I/O	P45	P57	J16	P63	P81	250
I/O	-	P58	K16	P64	P82	253
I/O	-	P59	K15	P65	P83	256
I/O	P46	P60	K14	P66	P86	259
I/O	P47	P61	L16	P67	P87	262
I/O	-	P62	M16	P68	P88	265
I/O	-	P63	L15	P69	P89	268
GND	-	P64	L14	P70	P90	-
I/O	-	-	N16	P71	P93	271
I/O	-	-	M15	P72	P94	274
I/O	P48	P65	P16	P73	P95	277
I/O	P49	P66	M14	P74	P96	280
I/O	-	P67	N15	P75	P97	283
I/O	-	P68	P15	P76	P98	286
I/O	P50	P69	N14	P77	P99	289
I/O, SGCK3	P51	P70	R16	P78	P100	292
GND	P52	P71	P14	P79	P101	-
DONE	P53	P72	R15	P80	P103	-
VCC	P54	P73	P13	P81	P106	-
PROGRAM	P55	P74	R14	P82	P108	-
I/O (D7)	P56	P75	T16	P83	P109	295
I/O, PGCK3	P57	P76	T15	P84	P110	298
I/O	-	P77	R13	P85	P111	301
I/O	-	P78	P12	P86	P112	304
I/O (D6)	P58	P79	T14	P87	P113	307
I/O	-	P80	T13	P88	P114	310
I/O	-	-	R12	P89	P115	313
I/O	-	-	T12	P90	P116	316
GND	-	P81	P11	P91	P119	-
I/O	-	P82	R11	P92	P120	319
I/O	-	P83	T11	P93	P121	322
I/O (D5)	P59	P84	T10	P94	P122	325
I/O (CS0)	P60	P85	P10	P95	P123	328
I/O	-	P86	R10	P96	P126	331
I/O	-	P87	T9	P97	P127	334
I/O (D4)	P61	P88	R9	P98	P128	337
I/O	P62	P89	P9	P99	P129	340
VCC	P63	P90	R8	P100	P130	-
GND	P64	P91	P8	P101	P131	-
I/O (D3)	P65	P92	T8	P102	P132	343
I/O (RS)	P66	P93	T7	P103	P133	346

XC4006E Pad Name	PC 84	TQ 144	PG 156	PQ 160	PQ 208	Bndry Scan
I/O	-	P94	T6	P104	P134	349
I/O	-	P95	R7	P105	P135	352
I/O (D2)	P67	P96	P7	P106	P138	355
I/O	P68	P97	T5	P107	P139	358
I/O	-	P98	R6	P108	P140	361
I/O	-	P99	T4	P109	P141	364
GND	-	P100	P6	P110	P142	-
I/O	-	-	R5	P111	P145	367
I/O	-	-	-	P112	P146	370
I/O (D1)	P69	P101	T3	P113	P147	373
I/O (RCLK, RDY/BUSY)	P70	P102	P5	P114	P148	376
I/O	-	P103	R4	P115	P149	379
I/O	-	P104	R3	P116	P150	382
I/O (D0, DIN)	P71	P105	P4	P117	P151	385
I/O, SGCK4 (DOUT)	P72	P106	T2	P118	P152	388
CCLK	P73	P107	R2	P119	P153	-
VCC	P74	P108	P3	P120	P154	-
O, TDO	P75	P109	T1	P121	P159	0
GND	P76	P110	N3	P122	P160	-
I/O (A0, WS)	P77	P111	R1	P123	P161	2
I/O, PGCK4 (A1)	P78	P112	P2	P124	P162	5
I/O	-	P113	N2	P125	P163	8
I/O	-	P114	M3	P126	P164	11
I/O (CS1, A2)	P79	P115	P1	P127	P165	14
I/O (A3)	P80	P116	N1	P128	P166	17
I/O	-	P117	M2	P129	P167	20
I/O	-	-	M1	P130	P168	23
GND	-	P118	L3	P131	P171	-
I/O	-	P119	L2	P132	P172	26
I/O	-	P120	L1	P133	P173	29
I/O (A4)	P81	P121	K3	P134	P174	32
I/O (A5)	P82	P122	K2	P135	P175	35
I/O	-	P123	K1	P137	P178	38
I/O	-	P124	J1	P138	P179	41
I/O (A6)	P83	P125	J2	P139	P180	44
I/O (A7)	P84	P126	J3	P140	P181	47
GND	P1	P127	H2	P141	P182	-

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## Additional XC4006E Package Pins

PQ160

Not Connected Pins				
P136	-	-	-	-

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PQ208

Not Connected Pins				
P1	P3	P12	P13	P19
P20	P31	P32	P38	P39
P51	P52	P53	P54	P65
P66	P72	P73	P84	P85
P91	P92	P102	P104	P105
P107	P117	P118	P124	P125
P136	P137	P143	P144	P155
P156	P157	P158	P169	P170
P176	P177	P188	P189	P195
P196	P206	P207	P208	-

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## Pin Locations for XC4008E Devices

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
VCC	P2	P142	J4	P183	-
I/O (A8)	P3	P143	J3	P184	56
I/O (A9)	P4	P144	J2	P185	59
I/O	-	P145	J1	P186	62
I/O	-	P146	H1	P187	65
I/O	-	-	H2	P188	68
I/O	-	-	H3	P189	71
I/O (A10)	P5	P147	G1	P190	74
I/O (A11)	P6	P148	G2	P191	77
I/O	-	P149	F1	P192	80
I/O	-	P150	E1	P193	83
GND	-	P151	G3	P194	-
I/O	-	P152	C1	P197	86
I/O	-	P153	E2	P198	89
I/O (A12)	P7	P154	F3	P199	92
I/O (A13)	P8	P155	D2	P200	95
I/O	-	P156	B1	P201	98
I/O	-	P157	E3	P202	101
I/O (A14)	P9	P158	C2	P203	104
I/O, SGCK1 (A15)	P10	P159	B2	P204	107
VCC	P11	P160	D3	P205	-
GND	P12	P1	D4	P2	-
I/O, PGCK1 (A16)	P13	P2	C3	P4	110
I/O (A17)	P14	P3	C4	P5	113
I/O	-	P4	B3	P6	116
I/O	-	P5	C5	P7	119
I/O, TDI	P15	P6	A2	P8	122
I/O, TCK	P16	P7	B4	P9	125
I/O	-	P8	C6	P10	128
I/O	-	P9	A3	P11	131
GND	-	P10	C7	P14	-
I/O	-	P11	A4	P15	134
I/O	-	P12	A5	P16	137
I/O, TMS	P17	P13	B7	P17	140
I/O	P18	P14	A6	P18	143
I/O	-	-	C8	P19	146
I/O	-	-	A7	P20	149
I/O	-	P15	B8	P21	152
I/O	-	P16	A8	P22	155
I/O	P19	P17	B9	P23	158
I/O	P20	P18	C9	P24	161
GND	P21	P19	D9	P25	-
VCC	P22	P20	D10	P26	-
I/O	P23	P21	C10	P27	164
I/O	P24	P22	B10	P28	167
I/O	-	P23	A9	P29	170
I/O	-	P24	A10	P30	173
I/O	-	-	A11	P31	176
I/O	-	-	C11	P32	179
I/O	P25	P25	B11	P33	182
I/O	P26	P26	A12	P34	185
I/O	-	P27	B12	P35	188
I/O	-	P28	A13	P36	191
GND	-	P29	C12	P37	-
I/O	-	P30	A15	P40	194
I/O	-	P31	C13	P41	197
I/O	P27	P32	B14	P42	200
I/O	-	P33	A16	P43	203
I/O	-	P34	B15	P44	206
I/O	-	P35	C14	P45	209
I/O	P28	P36	A17	P46	212
I/O, SGCK2	P29	P37	B16	P47	215
O (M1)	P30	P38	C15	P48	218
GND	P31	P39	D15	P49	-
I (M0)	P32	P40	A18	P50	221
VCC	P33	P41	D16	P55	-
I (M2)	P34	P42	C16	P56	222
I/O, PGCK2	P35	P43	B17	P57	223

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
I/O (HDC)	P36	P44	E16	P58	226
I/O	-	P45	C17	P59	229
I/O	-	P46	D17	P60	232
I/O	-	P47	B18	P61	235
I/O (LDC)	P37	P48	E17	P62	238
I/O	-	P49	F16	P63	241
I/O	-	P50	C18	P64	244
GND	-	P51	G16	P67	-
I/O	-	P52	E18	P68	247
I/O	-	P53	F18	P69	250
I/O	P38	P54	G17	P70	253
I/O	P39	P55	G18	P71	256
I/O	-	-	H16	P72	259
I/O	-	-	H17	P73	262
I/O	-	P56	H18	P74	265
I/O	-	P57	J18	P75	268
I/O	P40	P58	J17	P76	271
I/O (INIT)	P41	P59	J16	P77	274
VCC	P42	P60	J15	P78	-
GND	P43	P61	K15	P79	-
I/O	P44	P62	K16	P80	277
I/O	P45	P63	K17	P81	280
I/O	-	P64	K18	P82	283
I/O	-	P65	L18	P83	286
I/O	-	-	L17	P84	289
I/O	-	-	L16	P85	292
I/O	P46	P66	M18	P86	295
I/O	P47	P67	M17	P87	298
I/O	-	P68	N18	P88	301
I/O	-	P69	P18	P89	304
GND	-	P70	M16	P90	-
I/O	-	P71	T18	P93	307
I/O	-	P72	P17	P94	310
I/O	P48	P73	N16	P95	313
I/O	P49	P74	T17	P96	316
I/O	-	P75	R17	P97	319
I/O	-	P76	P16	P98	322
I/O	P50	P77	U18	P99	325
I/O, SGCK3	P51	P78	T16	P100	328
GND	P52	P79	R16	P101	-
DONE	P53	P80	U17	P103	-
VCC	P54	P81	R15	P106	-
PROGRAM	P55	P82	V18	P108	-
I/O (D7)	P56	P83	T15	P109	331
I/O, PGCK3	P57	P84	U16	P110	334
I/O	-	P85	T14	P111	337
I/O	-	P86	U15	P112	340
I/O (D6)	P58	P87	V17	P113	343
I/O	-	P88	V16	P114	346
I/O	-	P89	T13	P115	349
I/O	-	P90	U14	P116	352
GND	-	P91	T12	P119	-
I/O	-	P92	U13	P120	355
I/O	-	P93	V13	P121	358
I/O (D5)	P59	P94	U12	P122	361
I/O (CS0)	P60	P95	V12	P123	364
I/O	-	-	T11	P124	367
I/O	-	-	U11	P125	370
I/O	-	P96	V11	P126	373
I/O	-	P97	V10	P127	376
I/O (D4)	P61	P98	U10	P128	379
I/O	P62	P99	T10	P129	382
VCC	P63	P100	R10	P130	-
GND	P64	P101	R9	P131	-
I/O (D3)	P65	P102	T9	P132	385
I/O (RS)	P66	P103	U9	P133	388
I/O	-	P104	V9	P134	391
I/O	-	P105	V8	P135	394
I/O	-	-	U8	P136	397

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
I/O	-	-	T8	P137	400
I/O (D2)	P67	P106	V7	P138	403
I/O	P68	P107	U7	P139	406
I/O	-	P108	V6	P140	409
I/O	-	P109	U6	P141	412
GND	-	P110	T7	P142	-
I/O	-	P111	U5	P145	415
I/O	-	P112	T6	P146	418
I/O (D1)	P69	P113	V3	P147	421
I/O (RCLK, RDY/BUSY)	P70	P114	V2	P148	424
I/O	-	P115	U4	P149	427
I/O	-	P116	T5	P150	430
I/O (D0, DIN)	P71	P117	U3	P151	433
I/O, SGCK4 (DOUT)	P72	P118	T4	P152	436
CCLK	P73	P119	V1	P153	-
VCC	P74	P120	R4	P154	-
O, TDO	P75	P121	U2	P159	0
GND	P76	P122	R3	P160	-
I/O (A0, WS)	P77	P123	T3	P161	2
I/O, PGCK4 (A1)	P78	P124	U1	P162	5
I/O	-	P125	P3	P163	8
I/O	-	P126	R2	P164	11
I/O (CS1, A2)	P79	P127	T2	P165	14
I/O (A3)	P80	P128	N3	P166	17
I/O	-	P129	P2	P167	20
I/O	-	P130	T1	P168	23
GND	-	P131	M3	P171	-
I/O	-	P132	P1	P172	26
I/O	-	P133	N1	P173	29
I/O (A4)	P81	P134	M2	P174	32
I/O (A5)	P82	P135	M1	P175	35

XC4008E Pad Name	PC84	PQ160	PG191	PQ208	Bndry Scan
I/O	-	-	L3	P176	38
I/O	-	P136	L2	P177	41
I/O	-	P137	L1	P178	44
I/O	-	P138	K1	P179	47
I/O (A6)	P83	P139	K2	P180	50
I/O (A7)	P84	P140	K3	P181	53
GND	P1	P141	K4	P182	-

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## Additional XC4008E Package Pins

PG191

Not Connected Pins					
A14	B5	B6	B13	D1	D18
F2	F17	N2	N17	R1	R18
V4	V5	V14	V15	-	-

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PQ208

Not Connected Pins					
P1	P3	P12	P13	P38	P39
P51	P52	P53	P54	P65	P66
P91	P92	P102	P104	P105	P107
P117	P118	P143	P144	P155	P156
P157	P158	P169	P170	P195	P196
P206	P207	P208	-	-	-

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## Pin Locations for XC4010E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191††	PQ/HQ 208	BG 225††	BG 256††	Bndry Scan
VCC	P2	P92	P128	P142	P155	VCC*	P183	VCC*	VCC*	-
I/O (A8)	P3	P93	P129	P143	P156	J3	P184	E8	C10	62
I/O (A9)	P4	P94	P130	P144	P157	J2	P185	B7	D10	65
I/O (A9)	-	P95	P131	P145	P158	J1	P186	A7	A9	68
I/O (18)	-	P96	P132	P146	P159	H1	P187	C7	B9	71
I/O	-	-	-	P160	H2	P188	D7	C9	J4	74
I/O	-	-	-	P161	H3	P189	E7	D9	J7	77
I/O (A10)	P5	P97	P133	P147	P162	G1	P190	A6	A8	80
I/O (A11)	P6	P98	P134	P148	P163	G2	P191	B6	B8	83
VCC	-	-	-	-	VCC*	-	VCC*	VCC*	-	-
I/O	-	-	P135	P149	P164	F1	P192	A5	B6	86
I/O	-	-	P136	P150	P165	E1	P193	B5	A5	89
GND	-	-	P137	P151	P166	GND*	P194	GND*	GND*	-
I/O	-	-	-	-	F2	P195	D6	C6	92	
I/O	-	-	-	P167	D1	P196	C5	B5	95	
I/O	-	-	-	P152	P168	C1	P197	A4	A4	98
I/O	-	-	P153	P169	E2	P198	E6	C5	101	
I/O (A12)	P7	P99	P138	P154	P170	F3	P199	B4	B4	104
I/O (A13)	P8	P100	P139	P155	P171	D2	P200	D5	A3	107
I/O	-	-	P140	P156	P172	B1	P201	B3	B3	110
I/O	-	-	P141	P157	P173	E3	P202	F6	B2	113
I/O (A14)	P9	P1	P142	P158	P174	C2	P203	A2	A2	116
I/O, SGCK1†, GCK8†† (A15)	P10	P2	P143	P159	P175	B2	P204	C3	C3	119
VCC	P11	P3	P144	P160	P176	VCC*	P205	VCC*	VCC*	-
GND	P12	P4	P1	P1	P1	GND*	P2	GND*	GND*	-
I/O, PGCK1†, GCK1†† (A16)	P13	P5	P2	P2	P2	C3	P4	D4	B1	122
I/O (A17)	P14	P6	P3	P3	P3	C4	P5	B1	C2	125

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191††	PQ/HQ 208	BG 225††	BG 256††	Bndry Scan
I/O	-	-	P4	P4	P4	B3	P6	C2	D2	128
I/O	-	-	P5	P5	P5	C5	P7	E5	D3	131
I/O, TDI	P15	P7	P6	P6	P6	A2	P8	D3	E4	134
I/O, TCK	P16	P8	P7	P7	P7	B4	P9	C1	C1	137
I/O	-	-	-	P8	P8	C6	P10	D2	D1	140
I/O	-	-	-	P9	P9	A3	P11	G6	E3	143
I/O	-	-	-	-	-	B5	P12	E4	E2	146
I/O	-	-	-	-	-	B6	P13	D1	E1	149
GND	-	-	P8	P10	P10	GND*	P14	GND*	GND*	-
I/O	-	-	P9	P11	P11	A4	P15	F5	G3	152
I/O	-	-	P10	P12	P12	A5	P16	E1	G2	155
I/O, TMS	P17	P9	P11	P13	P13	B7	P17	F4	G1	158
I/O	P18	P10	P12	P14	P14	A6	P18	F3	H3	161
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	-	-	-	P15	C8	P19	G4	164
I/O	-	-	-	-	-	P16	A7	P20	G3	167
I/O	-	-	P13	P15	P17	B8	P21	G2	K2	170
I/O	-	P11	P14	P16	P18	A8	P22	G1	K3	173
I/O	P19	P12	P15	P17	P19	B9	P23	G5	K1	176
I/O	P20	P13	P16	P18	P20	C9	P24	H3	L1	179
GND	P21	P14	P17	P19	P21	GND*	P25	GND*	GND*	-
VCC	P22	P15	P18	P20	P22	VCC*	P26	VCC*	VCC*	-
I/O	P23	P16	P19	P21	P23	C10	P27	H4	L2	182
I/O	P24	P17	P20	P22	P24	B10	P28	H5	L3	185
I/O	-	P18	P21	P23	P25	A9	P29	J2	L4	188
I/O	-	-	P22	P24	P26	A10	P30	J1	M1	191
I/O	-	-	-	P27	A11	P31	J3	M2	194	
I/O	-	-	-	-	P28	C11	P32	J4	M3	197
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	P25	P19	P23	P25	P29	B11	P33	K2	P1	200
I/O	P26	P20	P24	P26	P30	A12	P34	K3	P2	203

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/HQ 208	BG 225†	BG 256††	Bndry Scan
I/O	-	-	P25	P27	P31	B12	P35	J6	R1	206
I/O	-	-	P26	P28	P32	A13	P36	L1	P3	209
GND	-	-	P27	P29	P33	GND*	P37	GND*	GND*	-
I/O	-	-	-	-	B13	P38	L3	T2	212	
I/O	-	-	-	-	A14	P39	M1	U1	215	
I/O	-	-	-	P30	P34	A15	P40	K5	T3	218
I/O	-	-	-	P31	P35	C13	P41	M2	U2	221
I/O	P27	P21	P28	P32	P36	B14	P42	L4	V1	224
I/O	-	P22	P29	P33	P37	A16	P43	N1	T4	227
I/O	-	-	P30	P34	P38	B15	P44	M3	U3	230
I/O	-	-	P31	P35	P39	C14	P45	N2	V2	233
I/O	P28	P23	P32	P36	P40	A17	P46	K6	W1	236
I/O, SGCK2 †, GCK2 ††	P29	P24	P33	P37	P41	B16	P47	P1	V3	239
(M1)	P30	P25	P34	P38	P42	C15	P48	N3	W2	242
GND	P31	P26	P35	P39	P43	GND*	P49	GND*	GND*	-
I (M0)	P32	P27	P36	P40	P44	A18	P50	P2	Y1	245
VCC	P33	P28	P37	P41	P45	VCC*	P55	VCC*	VCC*	-
I (M2)	P34	P29	P38	P42	P46	C16	P56	M4	W3	246
I/O, PGCK2 †, GCK3 ††	P35	P30	P39	P43	P47	B17	P57	R2	Y2	247
I/O (HDC)	P36	P31	P40	P44	P48	E16	P58	P3	W4	250
I/O	-	-	P41	P45	P49	C17	P59	L5	V4	253
I/O	-	-	P42	P46	P50	D17	P60	N4	U5	256
I/O	-	P32	P43	P47	P51	B18	P61	R3	Y3	259
I/O (LDC)	P37	P33	P44	P48	P52	E17	P62	P4	Y4	262
I/O	-	-	-	P49	P53	F16	P63	K7	V5	265
I/O	-	-	-	P50	P54	C18	P64	M5	W5	268
I/O	-	-	-	-	D18	P65	R4	Y5	271	
I/O	-	-	-	-	F17	P66	N5	V6	274	
GND	-	-	P45	P51	P55	GND*	P67	GND*	GND*	-
I/O	-	-	P46	P52	P56	E18	P68	R5	W7	277
I/O	-	-	P47	P53	P57	F18	P69	M6	Y7	280
I/O	P38	P34	P48	P54	P58	G17	P70	N6	V8	283
I/O	P39	P35	P49	P55	P59	G18	P71	P6	W8	286
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	-	-	P60	H16	P72	R6	Y8	289
I/O	-	-	-	-	P61	H17	P73	M7	U9	292
I/O	-	P36	P50	P56	P62	H18	P74	R7	V10	295
I/O	-	P37	P51	P57	P63	J18	P75	L7	Y10	298
I/O	P40	P38	P52	P58	P64	J17	P76	N8	Y11	301
I/O (INIT)	P41	P39	P53	P59	P65	J16	P77	P8	W11	304
VCC	P42	P40	P54	P60	P66	VCC*	P78	VCC*	VCC*	-
GND	P43	P41	P55	P61	P67	GND*	P79	GND*	GND*	-
I/O	P44	P42	P56	P62	P68	K16	P80	L8	V11	307
I/O	P45	P43	P57	P63	P69	K17	P81	P9	U11	310
I/O	-	P44	P58	P64	P70	K18	P82	R9	Y12	313
I/O	-	P45	P59	P65	P71	L18	P83	N9	W12	316
I/O	-	-	-	-	P72	L17	P84	M9	V12	319
I/O	-	-	-	-	P73	L16	P85	L9	U12	322
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	P46	P46	P60	P66	P74	M18	P86	N10	Y15	325
I/O	P47	P47	P61	P67	P75	M17	P87	K9	V14	328
I/O	-	-	P62	P68	P76	N18	P88	R11	W15	331
I/O	-	-	P63	P69	P77	P18	P89	P11	Y16	334
GND	-	-	P64	P70	P78	GND*	P90	GND*	GND*	-
I/O	-	-	-	-	-	N17	P91	R12	Y17	337
I/O	-	-	-	-	-	R18	P92	L10	V16	340
I/O	-	-	-	P71	P79	T18	P93	P12	W17	343
I/O	-	-	-	P72	P80	P17	P94	M11	Y18	346
I/O	P48	P48	P65	P73	P81	N16	P95	R13	U16	349
I/O	P49	P49	P66	P74	P82	T17	P96	N12	V17	352
I/O	-	-	P67	P75	P83	R17	P97	P13	W18	355
I/O	-	-	P68	P76	P84	P16	P98	K10	Y19	358
I/O	P50	P50	P69	P77	P85	U18	P99	R14	V18	361
I/O, SGCK3 †, GCK4 ††	P51	P51	P70	P78	P86	T16	P100	N13	W19	364
GND	P52	P52	P71	P79	P87	GND*	P101	GND*	GND*	-
DONE	P53	P53	P72	P80	P88	U17	P103	P14	Y20	-
VCC	P54	P54	P73	P81	P89	VCC*	P106	VCC*	VCC*	-
PROGRAM	P55	P55	P74	P82	P90	V18	P108	M12	V19	-
I/O (D7)	P56	P56	P75	P83	P91	T15	P109	P15	U19	367
I/O, PGCK3 †, GCK5 ††	P57	P57	P76	P84	P92	U16	P110	N14	U18	370

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/HQ 208	BG 225†	BG 256††	Bndry Scan
I/O	-	-	P77	P85	P93	T14	P111	L11	T17	373
I/O	-	-	P78	P86	P94	U15	P112	M13	V20	376
I/O (D6)	P58	P58	P79	P87	P95	V17	P113	J10	T19	379
I/O	-	P59	P80	P88	P96	V16	P114	L12	T20	382
I/O	-	-	-	P89	P97	T13	P115	M15	R18	385
I/O	-	-	-	P90	P98	U14	P116	L13	R19	388
I/O	-	-	-	-	-	V15	P117	L14	R20	391
GND	-	-	P81	P91	P99	GND*	P119	GND*	GND*	-
I/O	-	-	P82	P92	P100	U13	P120	K13	N19	397
I/O (CS0)	P60	P61	P85	P95	P103	V12	P123	J12	M18	406
I/O	-	-	-	P104	T11	P124	J13	M20	A09	
I/O	-	-	-	P105	U11	P125	J14	L19	A12	
I/O	-	P62	P86	P96	P106	V11	P126	J15	L18	415
I/O	-	P63	P87	P97	P107	V10	P127	J11	L20	418
I/O (D4)	P61	P64	P88	P98	P108	U10	P128	H13	K20	421
I/O	P62	P65	P89	P99	P109	T10	P129	H14	K19	424
VCC	P63	P66	P90	P100	P110	VCC*	P130	VCC*	VCC*	-
GND	P64	P67	P91	P101	P111	GND*	P131	GND*	GND*	-
I/O (D3)	P65	P68	P92	P102	P112	T9	P132	H12	K18	427
I/O (RS)	P66	P69	P93	P103	P113	U9	P133	H11	K17	430
I/O	-	P70	P94	P104	P114	V9	P134	G14	J20	433
I/O	-	-	P95	P105	P115	V8	P135	G15	J19	436
I/O	-	-	-	P116	U8	P136	G13	J18	A49	
I/O	-	-	-	P117	T8	P137	G12	J17	A42	
I/O (D2)	P67	P71	P96	P106	P118	V7	P138	H11	K19	445
I/O	P68	P72	P97	P107	P119	U7	P139	F15	H18	448
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O	-	-	P98	P108	P120	V6	P140	F14	G19	451
I/O	-	-	P99	P109	P121	U6	P141	F13	F20	454
GND	-	-	P100	P110	P122	GND*	P142	GND*	GND*	-
I/O	-	-	-	-	-	V5	P143	E13	D20	457
I/O	-	-	-	-	-	V4	P144	E15	E46	
I/O	-	-	-	P111	P123	U5	P145	F11	D19	463
I/O	-	-	-	P112	P124	T6	P146	D14	C20	466
I/O (D1)	P69	P73	P101	P113	P125	V3	P147	E12	E47	
I/O (RCLK, RDY/BUSY)	P70	P74	P102	P114	P126	V2	P148	C15	D18	472
I/O	-	-	P103	P115	P127	U4	P149	D13	C19	475
I/O	-	-	P104	P116	P128	T5	P150	C14	B20	478
I/O (D, DIN)	P71	P75	P105	P117	P129	U3	P151	F10	C18	481
I/O, SGCK4 †, GCK6 †† (DOUT)	P72	P76	P106	P118	P130	T4	P152	B15	B19	484
CCLK	P73	P77	P107	P119	P131	V1	P153	C13	A20	-
VCC	P74	P78	P108	P120	P132	VCC*	P154	VCC*	VCC*	-
O, TDO	P75	P79	P109	P121	P133	U2	P159	A15	A19	0
GND	P76	P80	P110	P122	P134	GND*	P160	GND*	GND*	-
I/O (A0, WS)	P77	P81	P111	P123	P135	T3	P161	A14	A18	2
I/O, PGCK4 †, GCK7 †† (A1)	P78	P82	P112	P124	P136	U1	P162	B13	B17	5
I/O	-	-	P113	P125	P137	P3	P163	E11	C17	8
I/O	-	-	P114	P126	P138	R2	P164	C12	D16	11
I/O (CS1, A2)	P79	P83	P115	P127	P139	T2	P165	A13	A18	14
I/O (A3)	P80	P84	P116	P128	P140	N3	P166	B12	A17	17
I/O	-	-	P117	P129	P141	P2	P167	A12	A16	20
I/O	-	-	-	P130	P142	T1	P168	C11	C15	23
I/O	-	-	-	-	-	R1	P169	B11	B15	26
I/O	-	-	-	-	-	N2	P170	E10	A15	29
GND	-	-	P118	P131	P143	GND*	P171	GND*	GND*	-
I/O	-	-	P119	P132	P144	P1	P172	A11	B14	32
I/O	-	-	P120	P133	P145	N1	P173	D10	A14	35
VCC	-	-	-	-	-	VCC*	-	VCC*	VCC*	-
I/O (A4)	P81	P85	P121	P134	P146	M2	P174	A10	C12	38
I/O (A5)	P82	P86	P122	P135	P147	M1	P175	D9	B12	41
I/O	-	-	-	P148	L3	P176	C9	A12	A44	
I/O	-	-	P136	P149	L2	P177	B9	B11	A7	
I/O (A21)††	-	P87	P123	P137	P150	L1	P178	A9	C11	50
I/O (A20)††	-	P88	P124	P138	P151	K1	P179	E9	A11	53
I/O (A6)	P83	P89	P125	P139	P152	K2	P180	C8	A10	56
I/O (A7)	P84	P90	P126	P140	P153	K3	P181	B8	B10	59

XC4010E/XL Pad Name	PC 84	PQ 100††	TQ 144††	PQ 160	TQ 176††	PG 191†	PQ/ HQ 208	BG 225†	BG 256††	Bndry Scan
GND	P1	P91	P127	P141	P154	GND*	P182	GND*	GND*	-

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

† = E only

†† = XL only

## Additional XC4010E/XL Package Pins

PQ/HQ208

Not Connected Pins						
P1	P3	P51	P52	P53	P54	P102
P104	P105	P107	P155	P156	P157	P158
P206	P207	P208	-	-	-	-

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PG191

VCC Pins						
D3	D10	D16	J4	J15	R4	R10
R15	-	-	-	-	-	-
GND Pins						
C7	C12	D4	D9	D15	G3	G16
K4	K15	M3	M16	R3	R9	R16
T7	T12	-	-	-	-	-

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BG225

VCC Pins						
B2	B14	D8	H1	H15	R1	R8
R15	-	-	-	-	-	-
GND Pins						
A1	A8	D12	F8	G7	G8	G9
H2	H6	H7	H8	H9	H10	J7
J8	J9	K8	M8	-	-	-
Not Connected Pins						
A3	B10	C4	C6	C10	D11	E2
E3	E14	E15	F1	F2	F7	F9
F12	G10	J5	K1	K4	K12	L2
L6	L15	M10	M14	N7	N11	N15
P5	P7	P10	R10	-	-	-

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BG256

VCC Pins						
C14	D6	D7	D11	D14	D15	E20
F1	F4	F17	G4	G17	K4	L17
P4	P17	P19	R2	R4	R17	U6
U7	U10	U14	U15	V7	W20	-
GND Pins						
A1	B7	D4	D8	D13	D17	G20
H4	H17	N3	N4	N17	U4	U8
U13	U17	W14	-	-	-	-
Not Connected Pins						
A6	A7	A13	B13	B16	C4	C7
C8	C13	C16	D5	D12	E19	F2
F3	F18	F19	G18	H1	H2	H20
J3	J4	M4	M19	N1	N2	N18
P20	R3	T1	T18	U20	V9	V13
V15	W6	W9	W10	W13	W16	Y6
Y9	Y13	Y14	-	-	-	-

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## Pin Locations for XC4013E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
VCC	P128	P142	P155	P183	VCC*	P212	VCC*	-	
I/O (A8)	P129	P143	P156	P184	J3	E8	P213	C10	74
I/O (A9)	P130	P144	P157	P185	J2	B7	P214	D10	77
I/O (A19) ††	P131	P145	P158	P186	J1	A7	P215	A9	80
I/O (A18) ††	P132	P146	P159	P187	H1	C7	P216	B9	83
I/O	-	-	P160	P188	H2	D7	P217	C9	86
I/O	-	-	P161	P189	H3	E7	P218	D9	89
I/O (A10)	P133	P147	P162	P190	G1	A6	P220	A8	92
I/O (A11)	P134	P148	P163	P191	G2	B6	P221	B8	95
VCC	-	-	-	VCC*	VCC*	P222	VCC*	-	
I/O	-	-	-	-	H4	C6	P223	A6	98
I/O	-	-	-	-	G4	F7	P224	C7	101
I/O	P135	P149	P164	P192	F1	A5	P225	B6	104
I/O	P136	P150	P165	P193	E1	B5	P226	A5	107
GND	P137	P151	P166	P194	GND*	GND*	P227	GND*	-
I/O	-	-	-	P195	F2	D6	P228	C6	110
I/O	-	-	P167	P196	D1	C5	P229	B5	113
I/O	-	P152	P168	P197	C1	A4	P230	A4	116
I/O	-	P153	P169	P198	E2	E6	P231	C5	119
I/O (A12)	P138	P154	P170	P199	F3	B4	P232	B4	122
I/O (A13)	P139	P155	P171	P200	D2	D5	P233	A3	125
I/O	-	-	-	-	F4	A3	P234	D5	128
I/O	-	-	-	-	E4	C4	P235	C4	131
I/O	P140	P156	P172	P201	B1	B3	P236	B3	134
I/O	P141	P157	P173	P202	E3	F6	P237	B2	137

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
I/O (A14)	P142	P158	P174	P203	C2	A2	P238	A2	140
I/O, SGCK1 †, GCK8 †† (A15)	P143	P159	P175	P204	B2	C3	P239	C3	143
VCC Pins									
GND	P1	P1	P1	P2	GND*	GND*	P1	GND*	-
I/O, PGCK1 †, GCK1 †† (A16)	P2	P2	P2	P4	C3	D4	P2	B1	146
I/O (A17)	P3	P3	P3	P5	C4	B1	P3	C2	149
I/O	P4	P4	P4	P6	B3	C2	P4	D2	152
I/O	P5	P5	P5	P7	C5	P5	D3	D3	155
I/O, TDI	P6	P6	P6	P8	A2	D3	P6	E4	158
I/O, TCK	P7	P7	P7	P9	B4	C1	P7	C1	161
I/O	-	P8	P8	P10	C6	D2	P8	D1	164
I/O	-	P9	P9	P11	A3	G6	P9	E3	167
I/O	-	-	-	P12	B5	E4	P10	E2	170
I/O	-	-	-	P13	B6	D1	P11	E1	173
I/O	-	-	-	-	D5	E3	P12	F3	176
GND	P8	P10	P10	P14	GND*	GND*	P14	GND*	-
I/O	P9	P11	P11	P15	A4	F5	P15	G3	182
I/O	P10	P12	P12	P16	A5	E1	P16	G2	185
I/O, TMS	P11	P13	P13	P17	B7	F4	P17	G1	188
I/O	P12	P14	P14	P18	A6	F3	P18	H3	191
VCC	-	-	-	-	VCC*	VCC*	P19	VCC*	-

<b>XC4013E /XL Pad Name</b>	<b>HT 144††</b>	<b>PQ 160</b>	<b>HT 176††</b>	<b>PQ/HQ 208</b>	<b>PG 223†</b>	<b>BG 225†</b>	<b>PQ/HQ 240</b>	<b>BG 256††</b>	<b>Bndry Scan</b>
I/O	-	-	-	-	D7	F2	P20	H2	194
I/O	-	-	-	-	D8	F1	P21	H1	197
I/O	-	-	P15	P19	C8	G4	P23	J2	200
I/O	-	-	P16	P20	A7	G3	P24	J1	203
I/O	P13	P15	P17	P21	B8	G2	P25	K2	206
I/O	P14	P16	P18	P22	A8	G1	P26	K3	209
I/O	P15	P17	P19	P23	B9	G5	P27	K1	212
I/O	P16	P18	P20	P24	C9	H3	P28	L1	215
GND	P17	P19	P21	P25	GND*	GND*	P29	GND*	-
VCC	P18	P20	P22	P26	VCC*	VCC*	P30	VCC*	-
I/O	P19	P21	P23	P27	C10	H4	P31	L2	218
I/O	P20	P22	P24	P28	B10	H5	P32	L3	221
I/O	P21	P23	P25	P29	A9	J2	P33	L4	224
I/O	P22	P24	P26	P30	A10	J1	P34	M1	227
I/O	-	-	P27	P31	A11	J3	P35	M2	230
I/O	-	-	P28	P32	C11	J4	P36	M3	233
I/O	-	-	-	-	D11	J5	P38	N1	236
I/O	-	-	-	-	D12	K1	P39	N2	239
VCC	-	-	-	-	VCC*	VCC*	P40	VCC*	-
I/O	P23	P25	P29	P33	B11	K2	P41	P1	242
I/O	P24	P26	P30	P34	A12	K3	P42	P2	245
I/O	P25	P27	P31	P35	B12	J6	P43	R1	248
I/O	P26	P28	P32	P36	A13	L1	P44	P3	251
GND	P27	P29	P33	P37	GND*	GND*	P45	GND*	-
I/O	-	-	-	-	D13	L2	P46	T1	254
I/O	-	-	-	-	D14	K4	P47	R3	257
I/O	-	-	-	P38	B13	L3	P48	T2	260
I/O	-	-	-	P39	A14	M1	P49	U1	263
I/O	-	P30	P34	P40	A15	K5	P50	T3	266
I/O	-	P31	P35	P41	C13	M2	P51	U2	269
I/O	P28	P32	P36	P42	B14	L4	P52	V1	272
I/O	P29	P33	P37	P43	A16	N1	P53	T4	275
I/O	P30	P34	P38	P44	B15	M3	P54	U3	278
I/O	P31	P35	P39	P45	C14	N2	P55	V2	281
I/O	P32	P36	P40	P46	A17	K6	P56	W1	284
I/O,	P33	P37	P41	P47	B16	P1	P57	V3	287
SGCK2 †, GCK2 ††									
O (M1)	P34	P38	P42	P48	C15	N3	P58	W2	290
GND	P35	P39	P43	P49	GND*	GND*	P59	GND*	-
I (M0)	P36	P40	P44	P50	A18	P2	P60	Y1	293
VCC	P37	P41	P45	P55	VCC*	VCC*	P61	VCC*	-
I (M2)	P38	P42	P46	P56	C16	M4	P62	W3	294
I/O, PGCK2 †, GCK3 ††	P39	P43	P47	P57	B17	R2	P63	Y2	295
I/O (HDC)	P40	P44	P48	P58	E16	P3	P64	W4	298
I/O	P41	P45	P49	P59	C17	L5	P65	V4	301
I/O	P42	P46	P50	P60	D17	N4	P66	U5	304
I/O	P43	P47	P51	P61	B18	R3	P67	Y3	307
I/O (LDC)	P44	P48	P52	P62	E17	P4	P68	Y4	310
I/O	-	P49	P53	P63	F16	K7	P69	V5	313
I/O	-	P50	P54	P64	C18	M5	P70	W5	316
I/O	-	-	-	P65	D18	R4	P71	Y5	319
I/O	-	-	-	P66	F17	N5	P72	V6	322
I/O	-	-	-	-	E15	P5	P73	W6	325
I/O	-	-	-	-	F15	L6	P74	Y6	328
GND	P45	P51	P55	P67	GND*	GND*	P75	GND*	-
I/O	P46	P52	P56	P68	E18	R5	P76	W7	331
I/O	P47	P53	P57	P69	F18	M6	P77	Y7	334
I/O	P48	P54	P58	P70	G17	N6	P78	V8	337
I/O	P49	P55	P59	P71	G18	P6	P79	W8	340
VCC	-	-	-	-	VCC*	VCC*	P80	VCC*	-
I/O	-	-	P60	P72	H16	R6	P81	Y8	343
I/O	-	-	P61	P73	H17	M7	P82	U9	346
I/O	-	-	-	-	G15	N7	P84	Y9	349
I/O	-	-	-	-	H15	P7	P85	W10	352
I/O	P50	P56	P62	P74	H18	R7	P86	V10	355
I/O	P51	P57	P63	P75	J18	L7	P87	Y10	358
I/O	P52	P58	P64	P76	J17	N8	P88	Y11	361
I/O (INIT)	P53	P59	P65	P77	J16	P8	P89	W11	364
VCC	P54	P60	P66	P78	VCC*	VCC*	P90	VCC*	-
GND	P55	P61	P67	P79	GND*	GND*	P91	GND*	-
I/O	P56	P62	P68	P80	K16	L8	P92	V11	367

<b>XC4013E /XL Pad Name</b>	<b>HT 144††</b>	<b>PQ 160</b>	<b>HT 176††</b>	<b>PQ/HQ 208</b>	<b>PG 223†</b>	<b>BG 225†</b>	<b>PQ/HQ 240</b>	<b>BG 256††</b>	<b>Bndry Scan</b>
I/O	P57	P63	P69	P81	K17	P9	P93	U11	370
I/O	P58	P64	P70	P82	K18	R9	P94	Y12	373
I/O	P59	P65	P71	P83	L18	N9	P95	W12	376
I/O	-	-	P72	P84	L17	M9	P96	V12	379
I/O	-	-	P73	P85	L16	L9	P97	U12	382
I/O	-	-	-	-	L15	R10	P99	V13	385
VCC	-	-	-	-	M15	P10	P100	Y14	388
I/O	P60	P66	P74	P86	M18	N10	P102	Y15	391
I/O	P61	P67	P75	P87	M17	K9	P103	V14	394
I/O	P62	P68	P76	P88	N18	R11	P104	W15	397
I/O	P63	P69	P77	P89	P18	P11	P105	Y16	400
GND	P64	P70	P78	P90	GND*	GND*	P106	GND*	-
I/O	-	-	-	-	N15	M10	P107	V15	403
I/O	-	-	-	-	P15	N11	P108	W16	406
I/O	-	-	-	P91	N17	R12	P109	Y17	409
I/O	-	-	-	P92	R18	L10	P110	V16	412
I/O	-	P71	P79	P93	T18	P12	P111	W17	415
I/O	-	P72	P80	P94	P17	M11	P112	Y18	418
I/O	P65	P73	P81	P95	N16	R13	P113	U16	421
I/O	P66	P74	P82	P96	T17	N12	P114	V17	424
I/O	P67	P75	P83	P97	R17	P13	P115	W18	427
I/O	P68	P76	P84	P98	P16	K10	P116	Y19	430
I/O	P69	P77	P85	P99	U18	R14	P117	V18	433
I/O	P70	P78	P86	P100	T16	N13	P118	W19	436
GND	P71	P79	P87	P101	GND*	GND*	P119	GND*	-
DONE	P72	P80	P88	P103	U17	P14	P120	Y20	-
VCC	P73	P81	P89	P106	VCC*	VCC*	P121	VCC*	-
PRO-GRAM	P74	P82	P90	P108	V18	M12	P122	V19	-
I/O (D7)	P75	P83	P91	P109	T15	P15	P123	U19	439
I/O	P76	P84	P92	P110	U16	N14	P124	U18	442
I/O	P77	P85	P93	P111	T14	L11	P125	T17	445
I/O	P78	P86	P94	P112	U15	M13	P126	V20	448
I/O	-	-	-	-	R14	N15	P127	U20	451
I/O	-	-	-	-	R13	M14	P128	T18	454
I/O (D6)	P79	P87	P95	P113	V17	J10	P129	T19	457
I/O	P80	P88	P96	P114	V16	L12	P130	T20	460
I/O	-	P89	P97	P115	T13	M15	P131	R18	463
I/O	-	P90	P98	P116	U14	L13	P132	R19	466
I/O	-	-	-	P117	V15	L14	P133	R20	469
I/O	-	-	-	P118	V14	K11	P134	P18	472
GND	P81	P91	P99	P119	GND*	GND*	P135	GND*	-
I/O	-	-	-	-	R12	L15	P136	P20	475
I/O	-	-	-	-	R11	K12	P137	N18	478
I/O	P82	P92	P100	P120	U13	K13	P138	N19	481
I/O	P83	P93	P101	P121	V13	K14	P139	N20	484
VCC	-	-	-	-	VCC*	VCC*	P140	VCC*	-
I/O (D5)	P84	P94	P102	P122	U12	K15	P141	M17	487
I/O (CS0)	P85	P95	P103	P123	V12	J12	P142	M18	490
I/O	-	-	P104	P124	T11	J13	P144	M20	493
I/O	-	-	P105	P125	U11	J14	P145	L19	496
I/O	P86	P96	P106	P126	V11	J15	P146	L18	499
I/O	P87	P97	P107	P127	V10	J11	P147	L20	502
I/O (D4)	P88	P98	P108	P128	U10	H13	P148	K20	505
I/O	P89	P99	P109	P129	T10	H14	P149	K19	508
VCC	P90	P100	P110	P130	VCC*	VCC*	P150	VCC*	-
GND	P91	P101	P111	P131	GND*	GND*	P151	GND*	-
I/O (D3)	P92	P102	P112	P132	T9	H12	P152	K18	511
I/O (RS)	P93	P103	P113	P133	U9	H11	P153	K17	514
I/O	P94	P104	P114	P134	V9	G14	P154	J20	517
I/O	P95	P105	P115	P135	V8	G15	P155	J19	520
I/O	-	-	P116	P136	U8	G13	P156	J18	523
I/O	-	-	P117	P137	T8	G12	P157	J17	526
I/O (D2)	P96	P106	P118	P138	V7	G11	P159	H19	529
I/O	P97	P107	P119	P139	U7	F15	P160	H18	532
VCC	-	-	-	-	VCC*	VCC*	P161	VCC*	-
I/O	P98	P108	P120	P140	V6	F14	P162	G19	535
I/O	P99	P109	P121	P141	U6	F13	P163	F20	538
I/O	-	-	-	-	R8	G10	P164	G18	541

XC4013E /XL Pad Name	HT 144††	PQ 160	HT 176††	PQ/HQ 208	PG 223†	BG 225†	PQ/ HQ 240	BG 256††	Bndry Scan
I/O	-	-	-	-	R7	E15	P165	F19	544
GND	P100	P110	P122	P142	GND*	P166	GND*	-	
I/O	-	-	-	-	R6	E14	P167	F18	547
I/O	-	-	-	-	R5	F12	P168	E19	550
I/O	-	-	-	P143	V5	E13	P169	D20	553
I/O	-	-	-	P144	V4	D15	P170	E18	556
I/O	-	P111	P123	P145	U5	F11	P171	D19	559
I/O	-	P112	P124	P146	T6	D14	P172	C20	562
I/O (D1)	P101	P113	P125	P147	V3	E12	P173	E17	565
I/O (RCLK, RDY/ BUSY)	P102	P114	P126	P148	V2	C15	P174	D18	568
I/O	P103	P115	P127	P149	U4	D13	P175	C19	571
I/O	P104	P116	P128	P150	T5	C14	P176	B20	574
I/O (D0, DIN)	P105	P117	P129	P151	U3	F10	P177	C18	577
I/O, SGCCK4 †, GCK6 †† (DOUT)	P106	P118	P130	P152	T4	B15	P178	B19	580
CCLK	P107	P119	P131	P153	V1	C13	P179	A20	-
VCC	P108	P120	P132	P154	VCC*	VCC*	P180	VCC*	-
O, TDO	P109	P121	P133	P159	U2	A15	P181	A19	0
GND	P110	P122	P134	P160	GND*	GND*	P182	GND*	-
I/O (A0, WS)	P111	P123	P135	P161	T3	A14	P183	B18	2
I/O, PGCCK4 †, GCK7 †† (A1)	P112	P124	P136	P162	U1	B13	P184	B17	5
I/O	P113	P125	P137	P163	P3	E11	P185	C17	8
I/O	P114	P126	P138	P164	R2	C12	P186	D16	11
I/O (CS1, A2)	P115	P127	P139	P165	T2	A13	P187	A18	14
I/O (A3)	P116	P128	P140	P166	N3	B12	P188	A17	17
I/O	-	-	-	-	P4	F9	P189	C16	20
I/O	-	-	-	-	N4	D11	P190	B16	23
I/O	P117	P129	P141	P167	P2	A12	P191	A16	26
I/O	-	P130	P142	P168	T1	C11	P192	C15	29
I/O	-	-	-	P169	R1	B11	P193	B15	32
I/O	-	-	-	P170	N2	E10	P194	A15	35
GND	P118	P131	P143	P171	GND*	GND*	P196	GND*	-
I/O	P119	P132	P144	P172	P1	A11	P197	B14	38
I/O	P120	P133	P145	P173	N1	D10	P198	A14	41
I/O	-	-	-	-	M4	C10	P199	C13	44
I/O	-	-	-	-	L4	B10	P200	B13	47
VCC	-	-	-	VCC*	VCC*	P201	VCC*	-	
I/O (A4)	P121	P134	P146	P174	M2	A10	P202	C12	50
I/O (A5)	P122	P135	P147	P175	M1	D9	P203	B12	53
I/O	-	-	P148	P176	L3	C9	P205	A12	56
I/O	-	P136	P149	P177	L2	B9	P206	B11	59
I/O (A21) ††	P123	P137	P150	P178	L1	A9	P207	C11	62
I/O (A20) ††	P124	P138	P151	P179	K1	E9	P208	A11	65
I/O (A6)	P125	P139	P152	P180	K2	C8	P209	A10	68
I/O (A7)	P126	P140	P153	P181	K3	B8	P210	B10	71
GND	P127	P141	P154	P182	GND*	GND*	P211	GND*	-

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

† = E only, †† = XL only

## Additional XC4013E/XL Package Pins

### PQ/HQ208

Not Connected Pins					
P1	P3	P51	P52	P53	P54
P102	P104	P105	P107	P155	P156
P157	P158	P206	P207	P208	-

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### PG223

VCC Pins					
D3	D10	D16	J4	J15	R4
R10	R15	-	-	-	-
GND Pins					
C7	C12	D4	D9	D15	G3
G16	K4	K15	M3	M16	R3
R9	R16	T7	T12	-	-

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### BG225

VCC Pins				
B2	B14	D8	H1	H15
R1	R8	R15	-	-
GND Pins				
A1	A8	D12	F8	G7
G8	G9	H2	H6	H7
H8	H9	H10	J7	J8
J9	K8	M8	-	-

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The BG225 package pins in this table are bonded to an internal Ground plane on the XC4013E die. They must all be externally connected to Ground.

### PQ/HQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

### BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-

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### GND Pins

A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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## Pin Locations for XC4020E/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
VCC	P128	P142	P155	P183	VCC*	P212	VCC*	-
I/O (A8)	P129	P143	P156	P184	J3	P213	C10	86
I/O (A9)	P130	P144	P157	P185	J2	P214	D10	89
I/O (A19) ††	P131	P145	P158	P186	J1	P215	A9	92
I/O (A18) ††	P132	P146	P159	P187	H1	P216	B9	95
I/O	-	-	P160	P188	H2	P217	C9	98
I/O	-	-	P161	P189	H3	P218	D9	101
I/O (A10)	P133	P147	P162	P190	G1	P220	A8	104
I/O (A11)	P134	P148	P163	P191	G2	P221	B8	107
I/O	-	-	-	-	-	-	C8	110
I/O	-	-	-	-	-	-	A7	113
VCC	-	-	-	-	VCC*	P222	VCC*	-
I/O	-	-	-	-	H4	P223	A6	116
I/O	-	-	-	-	G4	P224	C7	119
I/O	P135	P149	P164	P192	F1	P225	B6	122
I/O	P136	P150	P165	P193	E1	P226	A5	125
GND	P137	P151	P166	P194	GND*	P227	GND*	-
I/O	-	-	-	P195	F2	P228	C6	128
I/O	-	-	P167	P196	D1	P229	B5	131
I/O	-	P152	P168	P197	C1	P230	A4	134
I/O	-	P153	P169	P198	E2	P231	C5	137
I/O (A12)	P138	P154	P170	P199	F3	P232	B4	140
I/O (A13)	P139	P155	P171	P200	D2	P233	A3	143
I/O	-	-	-	F4	P234	D5	152	
I/O	-	-	-	E4	P235	C4	155	
I/O	P140	P156	P172	P201	B1	P236	B3	158
I/O	P141	P157	P173	P202	E3	P237	B2	161
I/O (A14)	P142	P158	P174	P203	C2	P238	A2	164
I/O, SGCK1 †, GCK8 †† (A15)	P143	P159	P175	P204	B2	P239	C3	167
VCC	P144	P160	P176	P205	VCC*	P240	VCC*	-
GND	P1	P1	P1	P2	GND*	P1	GND*	-
I/O, PGCK1 †, GCK1 †† (A16)	P2	P2	P2	P4	C3	P2	B1	170
I/O (A17)	P3	P3	P3	P5	C4	P3	C2	173
I/O	P4	P4	P4	P6	B3	P4	D2	176
I/O	P5	P5	P5	P7	C5	P5	D3	179
I/O, TDI	P6	P6	P6	P8	A2	P6	E4	182
I/O, TCK	P7	P7	P7	P9	B4	P7	C1	185
I/O	-	P8	P8	P10	C6	P8	D1	194
I/O	-	P9	P9	P11	A3	P9	E3	197
I/O	-	-	-	P12	B5	P10	E2	200
I/O	-	-	-	P13	B6	P11	E1	203
I/O	-	-	-	-	D5	P12	F3	206
I/O	-	-	-	-	D6	P13	F2	209
GND	P8	P10	P10	P14	GND*	P14	GND*	-
I/O	P9	P11	P11	P15	A4	P15	G3	212
I/O	P10	P12	P12	P16	A5	P16	G2	215
I/O, TMS	P11	P13	P13	P17	B7	P17	G1	218
I/O	P12	P14	P14	P18	A6	P18	H3	221
VCC	-	-	-	-	VCC*	P19	VCC*	-
I/O	-	-	-	-	D7	P20	H2	224
I/O	-	-	-	-	D8	P21	H1	227
I/O	-	-	-	-	-	J4	Z30	
I/O	-	-	-	-	-	J3	Z33	
I/O	-	-	P15	P19	C8	P23	J2	236
I/O	-	-	P16	P20	A7	P24	J1	239
I/O	P13	P15	P17	P21	B8	P25	K2	242
I/O	P14	P16	P18	P22	A8	P26	K3	245
I/O	P15	P17	P19	P23	B9	P27	K1	248
I/O	P16	P18	P20	P24	C9	P28	L1	251
GND	P17	P19	P21	P25	GND*	P29	GND*	-
VCC	P18	P20	P22	P26	VCC*	P30	VCC*	-
I/O	P19	P21	P23	P27	C10	P31	L2	254
I/O	P20	P22	P24	P28	B10	P32	L3	257
I/O	P21	P23	P25	P29	A9	P33	L4	260
I/O	P22	P24	P26	P30	A10	P34	M1	263
I/O	-	-	P27	P31	A11	P35	M2	266
I/O	-	-	P28	P32	C11	P36	M3	269
I/O	-	-	-	-	-	M4	272	
I/O	-	-	-	D11	P38	N1	278	
I/O	-	-	-	D12	P39	N2	281	
VCC	-	-	-	-	VCC*	P40	VCC*	-
I/O	P23	P25	P29	P33	B11	P41	P1	284

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
I/O	P24	P26	P30	P34	A12	P42	P2	287
I/O	P25	P27	P31	P35	B12	P43	R1	290
I/O	P26	P28	P32	P36	A13	P44	P3	293
GND	P27	P29	P33	P37	GND*	P45	GND*	-
I/O	-	-	-	-	D13	P46	T1	296
I/O	-	-	-	-	D14	P47	R3	299
I/O	-	-	-	P38	B13	P48	T2	302
I/O	-	-	-	P39	A14	P49	U1	305
I/O	-	P30	P34	P40	A15	P50	T3	308
I/O	-	P31	P35	P41	C13	P51	U2	311
I/O	P28	P32	P36	P42	B14	P52	V1	320
I/O	P29	P33	P37	P43	A16	P53	T4	323
I/O	P30	P34	P38	P44	B15	P54	U3	326
I/O	P31	P35	P39	P45	C14	P55	V2	329
I/O	P32	P36	P40	P46	A17	P56	W1	332
I/O, SGCK2 †, GCK2 ††	P33	P37	P41	P47	B16	P57	V3	335
O (M1)	P34	P38	P42	P48	C15	P58	W2	338
GND	P35	P39	P43	P49	GND*	P59	GND*	-
I (M0)	P36	P40	P44	P50	A18	P60	Y1	341
VCC	P37	P41	P45	P55	VCC*	P61	VCC*	-
I (M2)	P38	P42	P46	P56	C16	P62	W3	342
I/O PGCK2 †, P39	P43	P47	P57	P63	Y2	P64	Y3	343
I/O (HDC)	P40	P44	P48	P58	E16	P64	W4	346
I/O	P41	P45	P49	P59	C17	P65	V4	349
I/O	P42	P46	P50	P60	D17	P66	U5	352
I/O	P43	P47	P51	P61	B18	P67	Y3	355
I/O (LDC)	P44	P48	P52	P62	E17	P68	Y4	358
I/O	-	P49	P53	P63	F16	P69	V5	367
I/O	-	P50	P54	P64	C18	P70	W5	370
I/O	-	-	-	P65	D18	P71	Y5	373
I/O	-	-	-	P66	F17	P72	V6	376
I/O	-	-	-	-	E15	P73	W6	379
I/O	-	-	-	-	F15	P74	Y6	382
GND	P45	P51	P55	P67	GND*	P75	GND*	-
I/O	P46	P52	P56	P68	E18	P76	W7	385
I/O	P47	P53	P57	P69	F18	P77	Y7	388
I/O	P48	P54	P58	P70	G17	P78	V8	391
I/O	P49	P55	P59	P71	G18	P79	W8	394
VCC	-	-	-	-	VCC*	P80	VCC*	-
I/O	-	-	P60	P72	H16	P81	Y8	397
I/O	-	-	P61	P73	H17	P82	U9	400
I/O	-	-	-	-	-	V9	403	
I/O	-	-	-	-	-	W9	406	
I/O	-	-	-	-	G15	P84	Y9	409
I/O	-	-	-	-	H15	P85	W10	412
I/O	P50	P56	P62	P74	H18	P86	V10	415
I/O	P51	P57	P63	P75	J18	P87	Y10	418
I/O	P52	P58	P64	P76	J17	P88	Y11	421
I/O (INIT)	P53	P59	P65	P77	J16	P89	W11	424
VCC	P54	P60	P66	P78	VCC*	P90	VCC*	-
GND	P55	P61	P67	P79	GND*	P91	GND*	-
I/O	P56	P62	P68	P80	K16	P92	V11	427
I/O	P57	P63	P69	P81	K17	P93	U11	430
I/O	P58	P64	P70	P82	K18	P94	Y12	433
I/O	P59	P65	P71	P83	L18	P95	W12	436
I/O	-	-	P72	P84	L17	P96	V12	439
I/O	-	-	P73	P85	L16	P97	U12	442
I/O	-	-	-	-	-	-	Y13	445
I/O	-	-	-	-	-	-	W13	448
I/O	-	-	-	-	L15	P99	V13	451
I/O	-	-	-	-	M15	P100	Y14	454
VCC	-	-	-	-	VCC*	P101	VCC*	-
I/O	P60	P66	P74	P86	M18	P102	Y15	457
I/O	P61	P67	P75	P87	M17	P103	V14	460
I/O	P62	P68	P76	P88	N18	P104	W15	463
I/O	P63	P69	P77	P89	P18	P105	Y16	466
GND	P64	P70	P78	P90	GND*	P106	GND*	-
I/O	-	-	-	-	N15	P107	V15	469
I/O	-	-	-	-	P15	P108	W16	472
I/O	-	-	-	P91	N17	P109	Y17	475
I/O	-	-	-	P92	R18	P110	V16	478
I/O	-	P71	P79	P93	T18	P111	W17	481
I/O	-	P72	P80	P94	P17	P112	Y18	484

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
I/O	P65	P73	P81	P95	N16	P113	U16	493
I/O	P66	P74	P82	P96	T17	P114	V17	496
I/O	P67	P75	P83	P97	R17	P115	W18	499
I/O	P68	P76	P84	P98	P16	P116	Y19	502
I/O	P69	P77	P85	P99	U18	P117	V18	505
I/O, SGCK3 †, GCK4 ††	P70	P78	P86	P100	T16	P118	W19	508
GND	P71	P79	P87	P101	GND*	P119	GND*	-
DONE	P72	P80	P88	P103	U17	P120	Y20	-
VCC	P73	P81	P89	P106	VCC*	P121	VCC*	-
PROGRAM	P74	P82	P90	P108	V18	P122	V19	-
I/O (D7)	P75	P83	P91	P109	T15	P123	U19	511
I/O, PGCK3 †, GCK5 ††	P76	P84	P92	P110	U16	P124	U18	514
I/O	P77	P85	P93	P111	T14	P125	T17	517
I/O	P78	P86	P94	P112	U15	P126	V20	520
I/O	-	-	-	R14	P127	U20	523	
I/O	-	-	-	R13	P128	T18	526	
I/O (D6)	P79	P87	P95	P113	V17	P129	T19	535
I/O	P80	P88	P96	P114	V16	P130	T20	538
I/O	-	P89	P97	P115	T13	P131	R18	541
I/O	-	P90	P98	P116	U14	P132	R19	544
I/O	-	-	-	P117	V15	P133	R20	547
I/O	-	-	-	P118	V14	P134	P18	550
GND	P81	P91	P99	P119	GND*	P135	GND*	-
I/O	-	-	-	R12	P136	P20	553	
I/O	-	-	-	R11	P137	N18	556	
I/O	P82	P92	P100	P120	U13	P138	N19	559
I/O	P83	P93	P101	P121	V13	P139	N20	562
VCC	-	-	-	VCC*	P140	VCC*	-	
I/O (D5)	P84	P94	P102	P122	U12	P141	M17	565
I/O (CS0)	P85	P95	P103	P123	V12	P142	M18	568
I/O	-	-	-	-	-	M19	574	
I/O	-	-	P104	P124	T11	P144	M20	577
I/O	-	-	P105	P125	U11	P145	L19	580
I/O	P86	P96	P106	P126	V11	P146	L18	583
I/O	P87	P97	P107	P127	V10	P147	L20	586
I/O (D4)	P88	P98	P108	P128	U10	P148	K20	589
I/O	P89	P99	P109	P129	T10	P149	K19	592
VCC	P90	P100	P110	P130	VCC*	P150	VCC*	-
GND	P91	P101	P111	P131	GND*	P151	GND*	-
I/O (D3)	P92	P102	P112	P132	T9	P152	K18	595
I/O (RS)	P93	P103	P113	P133	U9	P153	K17	598
I/O	P94	P104	P114	P134	V9	P154	J20	601
I/O	P95	P105	P115	P135	V8	P155	J19	604
I/O	-	-	P116	P136	U8	P156	J18	607
I/O	-	-	P117	P137	T8	P157	J17	610
I/O	-	-	-	-	-	H20	613	
I/O (D2)	P96	P106	P118	P138	V7	P159	H19	619
I/O	P97	P107	P119	P139	U7	P160	H18	622
VCC	-	-	-	VCC*	P161	VCC*	-	
I/O	P98	P108	P120	P140	V6	P162	G19	625
I/O	P99	P109	P121	P141	U6	P163	F20	628
I/O	-	-	-	R8	P164	G18	631	
I/O	-	-	-	R7	P165	F19	634	
GND	P100	P110	P122	P142	GND*	P166	GND*	-
I/O	-	-	-	R6	P167	F18	637	
I/O	-	-	-	R5	P168	E19	640	
I/O	-	-	-	P143	V5	P169	D20	643
I/O	-	-	-	P144	V4	P170	E18	646
I/O	-	P111	P123	P145	U5	P171	D19	649
I/O	-	P112	P124	P146	T6	P172	C20	652
I/O (D1)	P101	P113	P125	P147	V3	P173	E17	655
I/O (RCLK, RDY/BUSY)	P102	P114	P126	P148	V2	P174	D18	658
I/O	P103	P115	P127	P149	U4	P175	C19	667
I/O	P104	P116	P128	P150	T5	P176	B20	670
I/O (D0, DIN)	P105	P117	P129	P151	U3	P177	C18	673
I/O, SGCK4 †, GCK6 †† (DOUT)	P106	P118	P130	P152	T4	P178	B19	676
CCLK	P107	P119	P131	P153	V1	P179	A20	-
VCC	P108	P120	P132	P154	VCC*	P180	VCC*	-
O, TDO	P109	P121	P133	P159	U2	P181	A19	0
GND	P110	P122	P134	P160	GND*	P182	GND*	-
I/O (A0, WS)	P111	P123	P135	P161	T3	P183	B18	2
I/O, PGCK4 †, GCK7 †† (A1)	P112	P124	P136	P162	U1	P184	B17	5
I/O	P113	P125	P137	P163	P3	P185	C17	8
I/O	P114	P126	P138	P164	R2	P186	D16	11
I/O (CS1, A2)	P115	P127	P139	P165	T2	P187	A18	14
I/O (A3)	P116	P128	P140	P166	N3	P188	A17	17

XC4020E/XL Pad Name	HT 144††	PQ 160††	HT 176††	HQ208† PQ208††	PG 223†	HQ240† PQ240††	BG 256††	Bndry Scan
I/O	-	-	-	-	-	P4	P189	C16
I/O	-	-	-	-	-	N4	P190	B16
I/O	P117	P129	P141	P167	P2	P191	A16	32
I/O	-	P130	P142	P168	T1	P192	C15	35
I/O	-	-	-	P170	N2	P194	A15	41
GND	P118	P131	P143	P171	GND*	P196	GND*	-
I/O	P119	P132	P144	P172	P1	P197	B14	44
P120	P133	P145	P173	N1	P198	A14	47	
I/O	-	-	-	M4	P199	C13	50	
VCC	-	-	-	VCC*	P201	VCC*	-	
I/O	-	-	-	-	-	A13	56	
I/O	-	-	-	-	-	D12	59	
I/O (A4)	P121	P134	P146	P174	M2	P202	C12	62
I/O (A5)	P122	P135	P147	P175	M1	P203	B12	65
I/O	-	-	P148	P176	L3	P205	A12	68
I/O	-	P136	P149	P177	L2	P206	B11	71
I/O (A21) ††	P123	P137	P150	P178	L1	P207	C11	74
I/O (A20) ††	P124	P138	P151	P179	K1	P208	A11	77
I/O (A6)	P125	P139	P152	P180	K2	P209	A10	80
I/O (A7)	P126	P140	P153	P181	K3	P210	B10	83
GND	P127	P141	P154	P182	GND*	P211	GND*	-

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† = E only  
†† = XL only

## Additional XC4020E/XL Package Pins

### PQ/HQ208

Not Connected Pins					
P1	P3	P51	P52	P53	P54
P102	P104	P105	P107	P155	P156
P157	P158	P206	P207	P208	-

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### PQ223

VCC Pins					
D3	D10	D16	J4	J15	R4
R10	R15	-	-	-	-
C7	C12	D4	D9	D15	G3
G16	K4	K15	M3	M16	R3
R9	R16	T7	T12	-	-

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GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
C4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

6/17/97

## Pin Locations for XC4025E, XC4028EX/XL Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan	XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan		
VCC	P142	P183	VCC*	P212	VCC*	VCC*	P38	VCC*	-	I/O	-	-	-	-	-	B5	P288	G26	239		
I/O (A8)	P143	P184	J3	P213	C10	K2	P37	D14	98	I/O	P10	P14	GND*	P14	GND*	GND*	P287	GND*	-		
I/O (A9)	P144	P185	J2	P214	D10	K3	P36	C14	101	I/O	P11	P15	A4	P15	G3	B6	P286	J23	242		
I/O (A19)‡	P145	P186	J1	P215	A9	K5	P35	A15	104	I/O, TMS	P13	P17	B7	P17	G1	C7	P284	H25	248		
I/O (A18)‡	P146	P187	H1	P216	B9	K4	P34	B15	107	I/O	P14	P18	A6	P18	H3	B7	P283	K23	251		
I/O	-	P188	H2	P217	C9	J1	P33	C15	110	VCC	-	-	VCC*	P19	VCC*	VCC*	P282	VCC*	-		
I/O	-	P189	H3	P218	D9	J2	P32	D15	113	I/O	-	-	D7	P20	H2	C8	P280	K24	254		
I/O (A10)	P147	P190	G1	P220	A8	H1	P31	A16	116	I/O	-	-	D8	P21	H1	E9	J29	J25	257		
I/O (A11)	P148	P191	G2	P221	B8	J3	P30	B16	119	I/O	-	-	-	-	-	-	A7	P278	L24	260	
GND	-	-	-	-	GND*	GND*	-	GND*	-	I/O	-	-	-	-	-	D9	P277	K25	263		
I/O	-	-	-	-	-	J4	P29	C16	122	GND	-	-	-	P22	GND*	GND*	-	GND*	-		
I/O	-	-	-	-	-	J5	P28	B17	125	I/O	-	-	-	-	-	-	J4	B8	P276	L25	266
I/O	-	-	-	-	C8	H2	P27	C17	128	I/O	-	-	-	-	-	-	J3	A8	P275	L26	269
I/O	-	-	-	-	A7	G1	P26	B18	131	VCC	-	-	VCC*	P222	VCC*	VCC*	P25	VCC*	-		
VCC	-	-	VCC*	P222	VCC*	VCC*	P25	VCC*	-	I/O	-	P19	C8	P23	J2	C9	P274	M23	272		
I/O	-	-	H4	P223	A6	H3	P23	C18	134	I/O	-	P20	A7	P24	J1	B9	P273	M24	275		
I/O	-	-	G4	P224	C7	G2	P22	D17	137	I/O	P15	P21	B8	P25	K2	E10	P272	M25	278		
I/O	P149	P192	F1	P225	B6	H4	P21	A20	140	I/O	P16	P22	A8	P26	K3	A9	P271	M26	281		
I/O	P150	P193	E1	P226	A5	F2	P20	B19	143	I/O	P17	P23	B9	P27	K1	D10	P270	N24	284		
GND	P151	P194	GND*	P227	GND*	GND*	P19	GND*	-	I/O	P18	P24	C9	P28	L1	C10	P269	N25	287		
I/O	-	-	-	-	-	H5	P18	C19	146	GND	P19	P25	GND*	P29	GND*	GND*	P268	GND*	-		
I/O	-	-	-	-	-	G3	P17	D18	149	VCC	P20	P26	VCC*	P30	VCC*	VCC*	P267	VCC*	-		
I/O	-	P195	F2	P228	C6	D1	P16	A21	152	I/O	P21	P27	C10	P31	L2	B10	P266	N26	290		
I/O	-	P196	D1	P229	B5	G4	P15	B20	155	I/O	P22	P28	B10	P32	L3	B11	P265	P25	293		
I/O	P152	P197	C1	P230	A4	E2	P14	C20	158	I/O	P23	P29	A9	P33	L4	C11	P264	P23	296		
I/O	P153	P198	E2	P231	C5	F3	P13	B21	161	I/O	P24	P30	A10	P34	M1	E11	P263	P24	299		
I/O (A12)	P154	P199	F3	P232	B4	G5	P12	B22	164	I/O	-	P31	A11	P35	M2	D11	P262	R26	302		
I/O (A13)	P155	P200	D2	P233	A3	C1	P10	C21	167	I/O	-	P32	C11	P36	M3	A12	P261	R25	305		
GND	-	-	-	-	GND*	GND*	-	GND*	-	I/O	-	-	-	M4	B12	P260	R24	308			
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-	I/O	-	-	-	A13	P259	R23	311				
I/O	-	-	-	-	-	F4	P9	D20	170	GND	-	-	-	P37	GND*	GND*	-	GND*	-		
I/O	-	-	-	-	-	E3	P8	A23	173	I/O	-	-	-	-	C12	P258	T26	314			
I/O	-	-	F4	P234	D5	D2	P7	D21	176	I/O	-	-	-	-	D12	P257	T25	317			
I/O	-	-	E4	P235	C4	C2	P6	C22	179	I/O	-	-	D11	P38	N1	E12	P256	T23	320		
I/O	P156	P201	B1	P236	B3	F5	P5	B24	182	I/O	-	-	D12	P39	N2	B13	P255	V26	323		
I/O	P157	P202	E3	P237	B2	E4	P4	C23	185	VCC	-	-	VCC*	P40	VCC*	VCC*	P253	VCC*	-		
I/O (A14)	P158	P203	C2	P238	A2	D3	P3	D22	188	I/O	P25	P33	B11	P41	P1	A14	P252	U24	326		
I/O, SGCK1†, GCK8‡ (A15)	P159	P204	B2	P239	C3	C3	P2	C24	191	I/O	P26	P34	A12	P42	P2	C13	P251	V25	329		
VCC	P160	P205	VCC*	P240	VCC*	VCC*	P1	VCC*	-	I/O	P27	P35	B12	P43	R1	B14	P250	V24	332		
GND	P1	P2	GND*	P1	GND*	GND*	P304	GND*	-	I/O	P28	P36	A13	P44	P3	D13	P249	U23	335		
I/O, PGCK1†, GCK1‡ (A16)	P2	P4	C3	P2	B1	D4	P303	D23	194	GND	P29	P37	GND*	P45	GND*	P248	GND*	-			
I/O (A17)	P3	P5	C4	P3	C2	B2	P302	C25	197	I/O	-	-	-	-	B15	P247	Y26	338			
I/O	P4	P6	B3	P4	D2	B3	P301	D24	200	I/O	-	-	-	-	E13	P246	W25	341			
I/O	P5	P7	C5	P5	D3	E6	P300	E23	203	I/O	-	-	D13	P46	T1	C14	P245	W24	344		
I/O, TDI	P6	P8	A2	P6	E4	D5	P299	C26	206	I/O	-	-	D14	P47	R3	A17	P244	V23	347		
I/O, TCK	P7	P9	B4	P7	C1	C4	P298	E24	209	I/O	-	P38	B13	P48	T2	D14	P243	AA26	350		
I/O	-	-	-	-	-	A3	P297	F24	212	I/O	-	P39	A14	P49	U1	B16	P242	Y25	353		
I/O	-	-	-	-	-	D6	P296	E25	215	I/O	P30	P40	A15	P50	T3	C15	P241	Y24	356		
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-	I/O	P31	P41	C13	P51	U2	E14	P240	AA25	359		
GND	-	-	-	-	GND*	GND*	-	GND*	-	GND	-	-	-	GND*	-	GND*	-	-			
I/O	P8	P10	C6	P8	D1	E7	P295	D26	218	VCC	-	-	-	VCC*	VCC*	-	VCC*	-			
I/O	P9	P11	A3	P9	E3	B4	P294	G24	221	I/O	-	-	-	-	-	A18	P239	AB25	362		
I/O	-	P12	B5	P10	E2	C5	P293	F25	224	I/O	-	-	-	-	D15	P238	AA24	365			
I/O	-	P13	B6	P11	E1	A4	P292	F26	227	I/O	P32	P42	B14	P52	V1	C16	P237	Y23	368		
I/O	-	-	D5	P12	F3	D7	P291	H23	230	I/O	P33	P43	A16	P53	T4	B17	P236	AC26	371		
I/O	-	-	D6	P13	F2	C6	P290	H24	233	I/O	P34	P44	B15	P54	U3	B18	P235	AA23	374		
I/O	-	-	-	-	-	E8	P289	G25	236	I/O	P35	P45	C14	P55	V2	E15	P234	AB24	377		
I/O	-	-	-	-	-	-	-	-	-	I/O	P36	P46	A17	P56	W1	D16	P233	AD25	380		
I/O, SGCK2†, GCK2‡	P37	P47	B16	P57	V3	C17	P232	AC24	383	I/O	P37	P47	B16	P57	V3	C17	P232	AC24	386		
O (M1)	P38	P48	C15	P58	W2	A20	P231	AB23	386	GND	P39	P49	GND*	P59	GND*	P230	GND*	-			

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan
I (M0)	P40	P50	A18	P60	Y1	C18	P229	AD24	389
VCC	P41	P55	VCC*	P61	VCC*	VCC*	P228	VCC*	-
I (M2)	P42	P56	C16	P62	W3	D17	P227	AC23	390
I/O, PGCK2 †, GCK3 ‡	P43	P57	B17	P63	Y2	B19	P226	AE24	391
I/O (HDC)	P44	P58	E16	P64	W4	C19	P225	AD23	394
I/O	P45	P59	C17	P65	V4	F16	P224	AC22	397
I/O	P46	P60	D17	P66	U5	E17	P223	AF24	400
I/O	P47	P61	B18	P67	Y3	D18	P222	AD22	403
I/O (LDC)	P48	P62	E17	P68	Y4	C20	P221	AE23	406
I/O	-	-	-	-	-	F17	P220	AE22	409
I/O	-	-	-	-	-	G16	P219	AF23	412
VCC	-	-	-	-	-	VCC*	VCC*	-	VCC*
GND	-	-	-	-	-	GND*	GND*	-	GND*
I/O	P49	P63	F16	P69	V5	D19	P218	AD20	415
I/O	P50	P64	C18	P70	W5	E18	P217	AE21	418
I/O	-	P65	D18	P71	Y5	D20	P216	AF21	421
I/O	-	P66	F17	P72	V6	G17	P215	AC19	424
I/O	-	-	E15	P73	W6	F18	P214	AD19	427
I/O	-	-	F15	P74	Y6	H16	P213	AE20	430
I/O	-	-	-	-	-	E19	P212	AF20	433
I/O	-	-	-	-	-	F19	P211	AC18	436
GND	P51	P67	GND*	P75	GND*	GND*	P210	GND*	-
I/O	P52	P68	E18	P76	W7	H17	P209	AD18	439
I/O	P53	P69	F18	P77	Y7	G18	P208	AE19	442
I/O	P54	P70	G17	P78	V8	G19	P207	AC17	445
I/O	P55	P71	G18	P79	W8	H18	P206	AD17	448
VCC	-	-	VCC*	P80	VCC*	VCC*	P204	VCC*	-
I/O	-	P72	H16	P81	Y8	J16	P203	AE18	451
I/O	-	P73	H17	P82	U9	G20	P202	AF18	454
I/O	-	-	-	-	-	J17	P201	AE17	457
I/O	-	-	-	-	-	H19	P200	AE16	460
GND	-	-	-	P83	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	V9	H20	P199	AF16
I/O	-	-	-	-	-	W9	J18	P198	AC15
I/O	-	-	G15	P84	Y9	J19	P197	AD15	469
I/O	-	-	H15	P85	W10	K16	P196	AE15	472
I/O	P56	P74	H18	P86	V10	J20	P195	AF15	475
I/O	P57	P75	J18	P87	Y10	K17	P194	AD14	478
I/O	P58	P76	J17	P88	Y11	K18	P193	AE14	481
I/O (INIT)	P59	P77	J16	P89	W11	K19	P192	AF14	484
VCC	P60	P78	VCC*	P90	VCC*	VCC*	P191	VCC*	-
GND	P61	P79	GND*	P91	GND*	GND*	P190	GND*	-
I/O	P62	P80	K16	P92	V11	L19	P189	AE13	487
I/O	P63	P81	K17	P93	U11	L18	P188	AC13	490
I/O	P64	P82	K18	P94	Y12	L16	P187	AD13	493
I/O	P65	P83	L18	P95	W12	L17	P186	AF12	496
I/O	-	P84	L17	P96	V12	M20	P185	AE12	499
I/O	-	P85	L16	P97	U12	M19	P184	AD12	502
I/O	-	-	-	-	-	Y13	N20	P183	AC12
I/O	-	-	-	-	-	W13	M18	P182	AF11
GND	-	-	-	P98	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	M17	P181	AE11	511
I/O	-	-	-	-	-	M16	P180	AD11	514
I/O	-	-	L15	P99	V13	N19	P179	AF9	517
I/O	-	-	M15	P100	Y14	P20	P178	AD10	520
VCC	-	-	VCC*	P101	VCC*	VCC*	P177	VCC*	-
I/O	P66	P86	M18	P102	Y15	N18	P175	AE9	523
I/O	P67	P87	M17	P103	V14	P19	P174	AD9	526
I/O	P68	P88	N18	P104	W15	N17	P173	AC10	529
I/O	P69	P89	P18	P105	Y16	R19	P172	AF7	532
GND	P70	P90	GND*	P106	GND*	GND*	P171	GND*	-
I/O	-	-	-	-	-	N16	P170	AE8	535
I/O	-	-	-	-	-	P18	P169	AD8	538
I/O	-	-	N15	P107	V15	U20	P168	AC9	541
I/O	-	-	P15	P108	W16	P17	P167	AF6	544
I/O	-	P91	N17	P109	Y17	T19	P166	AE7	547

XC4025E, XC4028 EX/XL Pad Name	HQ 160††	HQ 208‡	PG 223†	HQ 240	BG 256††	PG 299	HQ 304	BG 352‡	Bndry Scan	
I/O	-	P92	R18	P110	V16	R18	P165	AD7	550	
I/O	P71	P93	T18	P111	W17	P16	P164	AE6	553	
I/O	P72	P94	P17	P112	Y18	V20	P163	AE5	556	
GND	-	-	-	-	GND*	GND*	-	GND*	-	
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-	
I/O	-	-	-	-	-	R17	P162	AD6	559	
I/O	P73	P95	N16	P113	U16	U19	P160	AF4	565	
I/O	P74	P96	T17	P114	V17	V19	P159	AF3	568	
I/O	P75	P97	R17	P115	W18	R16	P158	AD5	571	
I/O	P76	P98	P16	P116	Y19	T17	P157	AE3	574	
I/O	P77	P99	U18	P117	V18	U18	P156	AD4	577	
I/O, SGCK3 †, GCK4 ‡	P78	P100	T16	P118	W19	X20	P155	AC5	580	
GND	P79	P101	GND*	P119	GND*	GND*	P154	GND*	-	
DONE	P80	P103	U17	P120	Y20	V18	P153	AD3	-	
VCC	P81	P106	VCC*	P121	VCC*	VCC*	P152	VCC*	-	
PRO- GRAM	P82	P108	V18	P122	V19	U17	P151	AC4	-	
I/O (D7)	P83	P109	T15	P123	U19	W19	P150	AD2	583	
I/O, PGCK3 †, GCK5 ‡	P84	P110	U16	P124	U18	W18	P149	AC3	586	
I/O	P85	P111	T14	P125	T17	T15	P148	AB4	589	
I/O	P86	P112	U15	P126	V20	U16	P147	AD1	592	
I/O	-	-	R14	P127	U20	V17	P146	AA4	595	
I/O	-	-	R13	P128	T18	X18	P145	AA3	598	
I/O	-	-	-	-	-	U15	P144	AB2	601	
I/O	-	-	-	-	-	T14	P143	AC1	604	
VCC	-	-	-	-	-	VCC*	VCC*	-	VCC*	
GND	-	-	-	-	-	GND*	GND*	-	GND*	
I/O (D6)	P87	P113	V17	P129	T19	W17	P142	Y3	607	
I/O	P88	P114	V16	P130	T20	V16	P141	AA2	610	
I/O	P89	P115	T13	P131	R18	X17	P140	AA1	613	
I/O	P90	P116	U14	P132	R19	U14	P139	W4	616	
I/O	-	P117	V15	P133	R20	V15	P138	W3	619	
I/O	-	P118	V14	P134	P18	T13	P137	Y2	622	
I/O	-	-	-	-	-	W16	P136	Y1	625	
GND	P91	P119	GND*	P135	GND*	GND*	P134	GND*	-	
I/O	-	-	R12	P136	P20	U13	P133	V3	631	
I/O	-	-	R11	P137	N18	V14	P132	W2	634	
I/O	P92	P120	U13	P138	N19	W14	P131	U4	637	
I/O	P93	P121	V13	P139	N20	V13	P130	U3	640	
VCC	-	-	VCC*	P140	VCC*	VCC*	P129	VCC*	-	
I/O (D5)	P94	P122	U12	P141	M17	T12	P127	V2	643	
I/O (CS0)	P95	P123	V12	P142	M18	X14	P126	V1	646	
I/O	-	-	-	-	-	U12	P125	U2	649	
I/O	-	-	-	-	-	W13	P124	T2	652	
GND	-	-	-	P143	GND*	GND*	-	GND*	-	
I/O	-	-	-	-	-	-	X13	P123	T1	655
I/O	-	-	-	-	-	M19	V12	P122	R4	658
I/O	-	P124	T11	P144	M20	W12	P121	R3	661	
I/O	-	P125	U11	P145	L19	T11	P120	R2	664	
I/O	P96	P126	V11	P146	L18	X12	P119	R1	667	
I/O	P97	P127	T10	P147	L20	U11	P118	P3	670	
I/O (D4)	P98	P128	U10	P148	K20	V11	P117	P2	673	
I/O	P99	P129	T10	P149	K19	W11	P116	P1	676	
VCC	P100	P130	VCC*	P150	VCC*	VCC*	P115	VCC*	-	
GND	P101	P131	GND*	P151	GND*	GND*	P114	GND*	-	
I/O (D3)	P102	P132	T9	P152	K18	W10	P113	N2	679	
I/O (RS)	P103	P133	U9	P153	K17	V10	P112	N4	682	
I/O	P104	P134	V9	P154	J20	T10	P111	N3	685	
I/O	P105	P135	V8	P155	J19	U10	P110	M1	688	
I/O	-	P136	U8	P156	J18	X9	P109	M2	691	
I/O	-	P137	T8	P157	J17	W9	P108	M3	694	
I/O	-	-	-	-	-	H20	X8	P107	M4	697

<b>XC4025E, XC4028 EX/XL Pad Name</b>	<b>HQ 160††</b>	<b>HQ 208‡</b>	<b>PG 223†</b>	<b>HQ 240</b>	<b>BG 256††</b>	<b>PG 299</b>	<b>HQ 304</b>	<b>BG 352‡</b>	<b>Bndry Scan</b>
I/O	-	-	-	-	-	V9	P106	L1	700
GND	-	-	-	P158	GND*	GND*	-	GND*	-
I/O	-	-	-	-	-	U9	P105	L2	703
I/O	-	-	-	-	-	T9	P104	L3	706
I/O (D2)	P106	P138	V7	P159	H19	W8	P103	J1	709
I/O	P107	P139	U7	P160	H18	X7	P102	K3	712
VCC	-	-	VCC*	P161	VCC*	VCC*	P101	VCC*	-
I/O	P108	P140	V6	P162	G19	V8	P99	J2	715
I/O	P109	P141	U6	P163	F20	W7	P98	J3	718
I/O	-	-	R8	P164	G18	U8	P97	K4	721
I/O	-	-	R7	P165	F19	W6	P96	G1	724
GND	P110	P142	GND*	P166	GND*	GND*	P95	GND*	-
I/O	-	-	-	-	-	T8	P94	H2	727
I/O	-	-	-	-	-	V7	P93	H3	730
I/O	-	-	R6	P167	F18	X4	P92	J4	733
I/O	-	-	R5	P168	E19	U7	P91	F1	736
I/O	-	P143	V5	P169	D20	W5	P90	G2	739
I/O	-	P144	V4	P170	E18	V6	P89	G3	742
I/O	P111	P145	U5	P171	D19	T7	P88	F2	745
I/O	P112	P146	T6	P172	C20	X3	P87	E2	748
GND	-	-	-	GND*	GND*	-	GND*	-	-
VCC	-	-	-	VCC*	VCC*	-	VCC*	-	-
I/O (D1)	P113	P147	V3	P173	E17	U6	P86	F3	751
I/O (RCLK, RDY/ BUSY)	P114	P148	V2	P174	D18	V5	P85	G4	754
I/O	-	-	-	-	-	W4	P84	D2	757
I/O	-	-	-	-	-	W3	P83	F4	760
I/O	P115	P149	U4	P175	C19	T6	P82	E3	763
I/O	P116	P150	T5	P176	B20	U5	P81	C2	766
I/O (D0, DIN)	P117	P151	U3	P177	C18	V4	P80	D3	769
I/O, SGCK4 †, GCK6‡ (DOUT)	P118	P152	T4	P178	B19	X1	P79	E4	772
CCLK	P119	P153	V1	P179	A20	V3	P78	C3	-
VCC	P120	P154	VCC*	P180	VCC*	VCC*	P77	VCC*	-
O, TDO	P121	P159	U2	P181	A19	U4	P76	D4	0
GND	P122	P160	GND*	P182	GND*	GND*	P75	GND*	-
I/O (A0, WS)	P123	P161	T3	P183	B18	W2	P74	B3	2
I/O, PGCK4 †, GCK7‡ (A1)	P124	P162	U1	P184	B17	V2	P73	C4	5
I/O	P125	P163	P3	P185	C17	R5	P72	D5	8
I/O	P126	P164	R2	P186	D16	T4	P71	A3	11
I/O (CS1, A2)	P127	P165	T2	P187	A18	U3	P70	D6	14
I/O (A3)	P128	P166	N3	P188	A17	V1	P69	C6	17
I/O	-	-	-	-	-	R4	P68	B5	20
I/O	-	-	-	-	-	P5	P67	A4	23
VCC	-	-	-	-	VCC*	VCC*	-	VCC*	-
GND	-	-	-	GND*	GND*	-	GND*	-	-
I/O	-	-	P4	P189	C16	U2	P66	C7	26
I/O	-	-	N4	P190	B16	T3	P65	B6	29
I/O	P129	P167	P2	P191	A16	U1	P64	A6	32
I/O	P130	P168	T1	P192	C15	P4	P63	D8	35
I/O	-	P169	R1	P193	B15	R3	P62	B7	38
I/O	-	P170	N2	P194	A15	N5	P61	A7	41
I/O	-	-	P195	-	T2	P60	D9	44	
I/O	-	-	-	-	R2	P59	C9	47	
GND	P131	P171	GND*	P196	GND*	GND*	P58	GND*	-
I/O	P132	P172	P1	P197	B14	N4	P57	B8	50
I/O	P133	P173	N1	P198	A14	P3	P56	D10	53
I/O	-	-	M4	P199	C13	P2	P55	C10	56
I/O	-	-	L4	P200	B13	N3	P54	B9	59
VCC	-	-	VCC*	P201	VCC*	VCC*	P52	VCC*	-

<b>XC4025E, XC4028 EX/XL Pad Name</b>	<b>HQ 160††</b>	<b>HQ 208‡</b>	<b>PG 223†</b>	<b>HQ 240</b>	<b>BG 256††</b>	<b>PG 299</b>	<b>HQ 304</b>	<b>BG 352‡</b>	<b>Bndry Scan</b>
I/O	-	-	-	-	-	-	A13	M5	P51
I/O	-	-	-	-	-	-	D12	P1	P50
I/O	-	-	-	-	-	-	M4	P49	B11
I/O	-	-	-	-	-	-	N2	P48	A11
GND	-	-	-	-	-	GND*	GND*	-	GND*
I/O (A4)	P134	P174	M2	P202	C12	N1	P47	D12	74
I/O (A5)	P135	P175	M1	P203	B12	M3	P46	C12	77
I/O	-	P176	L3	P205	A12	M2	P45	B12	80
I/O (A21)‡	P137	P178	L2	P206	B11	L5	P44	A12	83
I/O (A20)‡	P138	P179	L1	P207	C11	M1	P43	C13	86
I/O (A6)	P139	P180	K2	P208	A11	L4	P42	B13	89
I/O (A7)	P140	P181	K3	P210	B10	L2	P40	B14	95
GND	P141	P182	GND*	P211	GND*	GND*	P39	GND*	-

6/19/97

\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

† = E only

†† = XL only

‡ = EX, XL only

## Additional XC4025E, XC4028EX/XL Package Pins

HQ208

Not Connected Pins					
P1	P52	P102	P107	P157	P207
P3	P53	P104	P155	P158	P208
P51	P54	P105	P156	P206	

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PG223

VCC Pins			
D3	D10	D16	J4
J15	R4	R10	R15
GND Pins			
C7	C12	D4	D9
D15	G3	G16	K4
K15	M3	M16	R3
R9	R16	T7	T12

5/9/97

Note: These pins may be Not Connected for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

HQ240

GND Pins	
P204	P219

5/9/97

**BG256**

VCC Pins			
C14	D6	D7	D11
D14	D15	E20	F1
F4	F17	G4	G17
K4	L17	P4	P17
P19	R2	R4	R17
U6	U7	U10	U14
U15	V7	W20	-

GND Pins			
A1	B7	D4	D8
D13	D17	G20	H4
H17	N3	N4	N17
U4	U8	U13	U17
W14	-	-	-

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**PG299**

VCC Pins			
A2	A6	A11	A16
B20	E1	E5	F20
K1	L20	R1	T16
T20	W1	X5	X10
X15	X19	-	-

GND Pins			
A5	A10	A15	A19
B1	E16	E20	F1
K20	L1	R20	T1
T5	W20	X2	X6
X11	X16	-	-

6/18/97

**HQ304**

Not Connected Pins				
P11	P53	P128	P205	P281
P24	P100	P176	P254	-

5/15/97

Note: In XC4025 (no extension) devices in the HQ304 package, P101 is a No Connect (N.C.) pin. P101 is Vcc in XC4025E and XC4028EX/XL devices. Where necessary for compatibility, this pin can be left unconnected.

**BG352**

VCC Pins					
A10	A17	B2	B25	D7	D13
D19	G23	H4	K1	K26	N23
P4	U1	U26	W23	Y4	AC8
AC14	AC20	AE2	AE25	AF10	AF17

GND Pins					
A1	A2	A5	A8	A14	A19
A22	A25	A26	B1	B26	E1
E26	H1	H26	N1	P26	W1
W26	AB1	AB26	AE1	AE26	AF1
AF2	AF5	AF8	AF13	AF19	AF22
AF25	AF26	-	-	-	-

Not Connected Pins					
A18	A24	B4	B10	B23	C1
C5	C8	C11	D1	D16	D25
F23	J26	K2	L4	L23	T3
T4	T24	U25	AB3	AC2	AC6
AC11	AC16	AC21	AC25	AD16	AD21
AD26	AE4	AE10	-	-	-

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**Pin Locations for XC4036EX/XL**

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC4000 Series data sheet for availability information.

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
VCC	P142	P183	P212	P38	VCC*	VCC*	VCC*	-
I/O (A8)	P143	P184	P213	P37	D14	W3	D17	110
I/O (A9)	P144	P185	P214	P36	C14	Y2	A17	113
I/O (A19)	P145	P186	P215	P35	A15	V4	C18	116
I/O (A18)	P146	P187	P216	P34	B15	T2	D18	119
I/O	-	P188	P217	P33	C15	U1	B18	122
I/O	-	P189	P218	P32	D15	V6	A19	125
I/O (A10)	P147	P190	P220	P31	A16	U3	B19	128
I/O (A11)	P148	P191	P221	P30	B16	R1	C19	131
VCC	-	-	-	VCC*	VCC*	VCC*	-	
GND	-	-	-	GND*	GND*	GND*	-	
I/O	-	-	-	P29	C16	U5	D19	134
I/O	-	-	-	P28	B17	T4	A20	137
I/O	-	-	-	-	D16	P2	B20	140
I/O	-	-	-	-	A18	N1	C20	143
I/O	-	-	-	P27	C17	R5	C21	146
I/O	-	-	-	P26	B18	M2	A22	149
VCC	-	-	P222	P25	VCC*	VCC*	VCC*	-
I/O	-	-	P223	P23	C18	L3	B22	152
I/O	-	-	P224	P22	D17	T6	C22	155
I/O	P149	P192	P225	P21	A20	N5	B23	158
I/O	P150	P193	P226	P20	B19	M4	A24	161
GND	P151	P194	P227	P19	GND*	GND*	GND*	-
I/O	-	-	-	P18	C19	K2	D22	164
I/O	-	-	-	P17	D18	K4	C23	167
I/O	-	P195	P228	P16	A21	P6	B24	170
I/O	-	P196	P229	P15	B20	M6	C24	173
I/O	P152	P197	P230	P14	C20	J3	A26	176
I/O	P153	P198	P231	P13	B21	H2	C25	179
I/O (A12)	P154	P199	P232	P12	B22	H4	D24	182

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O (A13)	P155	P200	P233	P10	C21	G3	B26	185
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	-	P9	D20	K6	A27
I/O	-	-	-	-	P8	A23	G1	D25
I/O	-	-	-	-	A24	E1	C26	194
I/O	-	-	-	-	B23	E3	B27	197
I/O	-	-	-	P234	P7	D21	J7	200
I/O	-	-	P235	P6	C22	H6	B28	203
I/O	P156	P201	P236	P5	B24	C3	D27	206
I/O	P157	P202	P237	P4	C23	D2	B29	209
I/O (A14)	P158	P203	P238	P3	D22	E5	C28	212
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	G7	D28	215
VCC	P160	P205	P240	P1	VCC*	VCC*	VCC*	-
GND	P1	P2	P1	P304	GND*	GND*	GND*	-
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	H8	D29	218
I/O (A17)	P3	P5	P3	P302	C25	F6	C30	221
I/O	P4	P6	P4	P301	D24	B4	E28	224
I/O	P5	P7	P5	P300	E23	D4	E29	227
I/O, TDI	P6	P8	P6	P299	C26	B2	D30	230
I/O, TCK	P7	P9	P7	P298	E24	G9	D31	233
I/O	-	-	-	-	D25	F8	E30	236
I/O	-	-	-	-	F23	C5	E31	239
I/O	-	-	-	P297	F24	A7	G28	242
I/O	-	-	-	P296	E25	A5	G29	245
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	P8	P10	P8	P295	D26	B8	H28	248
I/O	P9	P11	P9	P294	G24	C9	H29	251
I/O	-	P12	P10	P293	F25	E9	G30	254

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O	-	P13	P11	P292	F26	F12	H30	257
I/O	-	-	P12	P291	H23	D10	J28	260
I/O	-	-	P13	P290	H24	B10	J29	263
I/O	-	-	-	P289	G25	F10	H31	266
I/O	-	-	-	P288	G26	F14	J30	269
GND	P10	P14	P14	P287	GND*	GND*	GND*	-
I/O	P11	P15	P15	P286	J23	C11	K28	272
I/O	P12	P16	P16	P285	J24	B12	K29	275
I/O, TMS	P13	P17	P17	P284	H25	E11	K30	278
I/O	P14	P18	P18	P283	K23	E15	K31	281
VCC	-	-	P19	P282	VCC*	VCC*	VCC*	-
I/O	-	-	P20	P280	K24	F16	L29	284
I/O	-	-	P21	P279	J25	C13	L30	287
I/O	-	-	-	J26	B14	M29	M29	290
I/O	-	-	-	L23	E17	M31	M31	293
I/O	-	-	-	P278	L24	E13	N31	296
I/O	-	-	-	P277	K25	A15	N28	299
GND	-	-	P22	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P276	L25	B16	P30	302
I/O	-	-	-	P275	L26	D16	P28	305
I/O	-	P19	P23	P274	M23	D18	P29	308
I/O	-	P20	P24	P273	M24	A17	R31	311
I/O	P15	P21	P25	P272	M25	E19	R30	314
I/O	P16	P22	P26	P271	M26	B18	R28	317
I/O	P17	P23	P27	P270	N24	C17	R29	320
I/O	P18	P24	P28	P269	N25	C19	T31	323
GND	P19	P25	P29	P268	GND*	GND*	GND*	-
VCC	P20	P26	P30	P267	VCC*	VCC*	VCC*	-
I/O	P21	P27	P31	P266	N26	F20	T30	326
I/O	P22	P28	P32	P265	P25	B20	T29	329
I/O	P23	P29	P33	P264	P23	C21	U31	332
I/O	P24	P30	P34	P263	P24	B22	U30	335
I/O	-	P31	P35	P262	R26	E21	U28	338
I/O	-	P32	P36	P261	R25	D22	U29	341
I/O	-	-	-	P260	R24	A23	V30	344
I/O	-	-	-	P259	R23	B24	V29	347
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P37	-	GND*	GND*	GND*	-
I/O	-	-	-	P258	T26	A25	W30	350
I/O	-	-	-	P257	T25	D24	W29	353
I/O	-	-	-	-	T24	B26	Y30	356
I/O	-	-	-	-	U25	A27	Y29	359
I/O	-	-	-	P38	P256	T23	C27	Y28
I/O	-	-	P39	P255	V26	F24	AA30	365
VCC	-	-	P40	P253	VCC*	VCC*	VCC*	-
I/O	P25	P33	P41	P252	U24	E25	AA29	368
I/O	P26	P34	P42	P251	V25	E27	AB31	371
I/O	P27	P35	P43	P250	V24	B28	AB30	374
I/O	P28	P36	P44	P249	U23	C29	AB29	377
GND	P29	P37	P45	P248	GND*	GND*	GND*	-
I/O	-	-	-	P247	Y26	F26	AB28	380
I/O	-	-	-	P246	W25	D28	AC30	383
I/O	-	-	-	P46	P245	W24	B30	AC29
I/O	-	-	P47	P244	V23	E29	AC28	389
I/O	-	P38	P48	P243	AA26	F28	AD29	392
I/O	-	P39	P49	P242	Y25	F30	AD28	395
I/O	P30	P40	P50	P241	Y24	C31	AE30	398
I/O	P31	P41	P51	P240	AA25	E31	AE29	401
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P239	AB25	B32	AF31	404
I/O	-	-	-	P238	AA24	A33	AE28	407
I/O	P32	P42	P52	P237	Y23	A35	AG31	410
I/O	P33	P43	P53	P236	AC26	F32	AF28	413
I/O	-	-	-	-	AD26	C35	AG30	416
I/O	-	-	-	-	AC25	B38	AG29	419
I/O	P34	P44	P54	P235	AA23	E33	AH31	422
I/O	P35	P45	P55	P234	AB24	G31	AG28	425
I/O	P36	P46	P56	P233	AD25	H32	AH30	428
I/O, GCK2	P37	P47	P57	P232	AC24	B36	AJ30	431
O (M1)	P38	P48	P58	P231	AB23	A39	AH29	434
GND	P39	P49	P59	P230	GND*	GND*	GND*	-
I (M0)	P40	P50	P60	P229	AD24	E35	AH28	437
VCC	P41	P55	P61	P228	VCC*	VCC*	VCC*	-

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I (M2)	P42	P56	P62	P227	AC23	G33	AJ28	438
I/O, GCK3	P43	P57	P63	P226	AE24	D36	AK29	439
I/O (HDC)	P44	P58	P64	P225	AD23	C37	AH27	442
I/O	P45	P59	P65	P224	AC22	F34	AK28	445
I/O	P46	P60	P66	P223	AF24	J33	AJ27	448
I/O	P47	P61	P67	P222	AD22	D38	AL28	451
I/O (LDC)	P48	P62	P68	P221	AE23	G35	AH26	454
I/O	-	-	-	-	AC21	E39	AL27	457
I/O	-	-	-	P220	AE22	F38	AK26	463
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	P49	P63	P69	P218	AD20	H38	AH24	469
I/O	P50	P64	P70	P217	AE21	J37	AJ25	472
I/O	-	P65	P71	P216	AF21	G39	AK25	475
I/O	-	P66	P72	P215	AC19	M34	AJ24	478
I/O	-	-	P73	P214	AD19	N35	AL24	481
I/O	-	-	P74	P213	AE20	P34	AH22	484
I/O	-	-	-	P212	AF20	J35	AJ23	487
I/O	-	-	P211	AC18	L37	AK23	490	
GND	P51	P67	P75	P210	GND*	GND*	GND*	-
I/O	P52	P68	P76	P209	AD18	M38	AJ22	493
I/O	P53	P69	P77	P208	AE19	R35	AK22	496
I/O	P54	P70	P78	P207	AC17	H36	AL22	499
I/O	P55	P71	P79	P206	AD17	T34	AJ21	502
VCC	-	-	P80	P204	VCC*	VCC*	VCC*	-
I/O	-	P72	P81	P203	AE18	N37	AH20	505
I/O	-	P73	P82	P202	AF18	N39	AK21	508
I/O	-	-	-	AC16	U35	AK20	511	
I/O	-	-	-	AD16	R39	AJ19	514	
I/O	-	-	P201	AE17	M36	AL20	517	
I/O	-	-	P200	AE16	V34	AH18	520	
GND	-	-	P83	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	P199	AF16	R37	AK19	523	
I/O	-	-	P198	AC15	T38	AJ18	526	
I/O	-	P84	P197	AD15	T36	AL19	529	
I/O	-	P85	P196	AE15	V36	AK18	532	
I/O	P56	P74	P86	P195	AF15	U37	AH17	535
I/O	P57	P75	P87	P194	AD14	U39	AJ17	538
I/O	P58	P76	P88	P193	AE14	V38	AJ16	541
I/O (INIT)	P59	P77	P89	P192	AF14	W37	AK16	544
VCC	P60	P78	P90	P191	VCC*	VCC*	VCC*	-
GND	P61	P79	P91	P190	GND*	GND*	GND*	-
I/O	P62	P80	P92	P189	AE13	Y34	AL16	547
I/O	P63	P81	P93	P188	AC13	AC37	AH15	550
I/O	P64	P82	P94	P187	AD13	AB38	AK15	553
I/O	P65	P83	P95	P186	AF12	AD36	AJ14	556
I/O	-	P64	P96	P185	AE12	AA35	AH14	559
I/O	-	P85	P97	P184	AD12	AE37	AK14	562
I/O	-	-	P183	AC12	AB36	AL13	565	
I/O	-	-	P182	AF11	AB38	AK13	568	
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P98	-	GND*	GND*	GND*	-
I/O	-	-	-	P181	AE11	AB34	AJ13	571
I/O	-	-	-	P180	AD11	AE39	AH13	574
I/O	-	-	-	P181	AE10	AM36	AL12	577
I/O	-	-	-	AC11	AC35	AK12	580	
I/O	-	-	P99	P179	AF9	AG39	AH12	583
I/O	-	-	P100	P178	AD10	AG37	AJ11	586
VCC	-	-	P101	P177	VCC*	VCC*	VCC*	-
I/O	P66	P86	P102	P175	AE6	AD34	AL10	589
I/O	P67	P87	P103	P174	AD9	AN39	AK10	592
I/O	P68	P88	P104	P173	AC10	AE35	AJ10	595
I/O	P69	P89	P105	P172	AF7	AH38	AK9	598
GND	P70	P90	P106	P171	GND*	GND*	GND*	-
I/O	-	-	-	P170	AE8	AJ37	AL8	601
I/O	-	-	-	P169	AD8	AG35	AH10	604
I/O	-	-	P107	P168	AC9	AF34	AJ7	607
I/O	-	-	P108	P167	AF6	AH36	AK8	610
I/O	-	P91	P109	P166	AE7	AK36	AK7	613
I/O	-	P92	P110	P165	AD7	AM34	AL6	616
I/O	P71	P93	P111	P164	AE6	AH34	AJ7	619
I/O	P72	P94	P112	P163	AE5	AJ35	AH8	622

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P162	AD6	AL37	AK6	625
I/O	-	-	-	P161	AC7	AT38	AL5	628
I/O	P73	P95	P113	P160	AF4	AM38	AH7	631
I/O	P74	P96	P114	P159	AF3	AN37	J6	634
I/O	-	-	-	-	AE4	AK34	AK5	637
I/O	-	-	-	-	AC6	AR39	AL4	640
I/O	P75	P97	P115	P158	AD5	AN35	AK4	643
I/O	P76	P98	P116	P157	AE3	AL33	AH5	646
I/O	P77	P99	P117	P156	AD4	AV38	AK3	649
I/O, GCK4	P78	P100	P118	P155	AC5	AT36	AJ4	652
GND	P79	P101	P119	P154	GND*	GND*	GND*	-
DONE	P80	P103	P120	P153	AD3	AR35	AH4	-
VCC	P81	P106	P121	P152	VCC*	VCC*	VCC*	-
PROGRAM	P82	P108	P122	P151	AC4	AN33	AH3	-
I/O (D7)	P83	P109	P123	P150	AD2	AM32	AJ2	655
I/O, GCK5	P84	P110	P124	P149	AC3	AP34	AG4	658
I/O	P85	P111	P125	P148	AB4	AW39	AG3	661
I/O	P86	P112	P126	P147	AD1	AN31	AH2	664
I/O	-	-	-	-	AB3	AV36	AH1	667
I/O	-	-	-	-	AC2	AR33	AF4	670
I/O	-	-	P127	P146	AA4	AP32	AF3	673
I/O	-	-	P128	P145	AA3	AU35	AG2	676
I/O	-	-	-	P144	AB2	AW33	AE3	679
I/O	-	-	-	P143	AC1	AU33	AF2	682
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O (D6)	P87	P113	P129	P142	Y3	AV32	AF1	685
I/O	P88	P114	P130	P141	AA2	AU31	AD4	688
I/O	P89	P115	P131	P140	AA1	AR31	AD3	691
I/O	P90	P116	P132	P139	W4	AP28	AE2	694
I/O	-	P117	P133	P138	W3	AT32	AC3	697
I/O	-	P118	P134	P137	Y2	AV30	AD1	700
I/O	-	-	-	P136	Y1	AR29	AC2	703
I/O	-	-	-	P135	V4	AP26	AB4	706
GND	P91	P119	P135	P134	GND*	GND*	GND*	-
I/O	-	-	P136	P133	V3	AU29	AB3	709
I/O	-	-	P137	P132	W2	AV28	AB2	712
I/O	P92	P120	P138	P131	U4	AT28	AB1	715
I/O	P93	P121	P139	P130	U3	AR25	AA3	718
VCC	-	-	P140	P129	VCC*	VCC*	VCC*	-
I/O (D5)	P94	P122	P141	P127	V2	AP24	AA2	721
I/O (CS0)	P95	P123	P142	P126	V1	AU27	Y2	724
I/O	-	-	-	-	T4	AR27	Y4	727
I/O	-	-	-	-	T3	AW27	Y3	730
I/O	-	-	-	P125	U2	AT24	W4	733
I/O	-	-	-	P124	T2	AR23	W3	736
GND	-	-	P143	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O	-	-	-	P123	T1	AP22	V4	739
I/O	-	-	-	P122	R4	AV24	V3	742
I/O	-	P124	P144	P121	R3	AU23	U1	745
I/O	-	P125	P145	P120	R2	AT22	U2	748
I/O	P96	P126	P146	P119	R1	AR21	U4	751
I/O	P97	P127	P147	P118	P3	AV22	U3	754
I/O (D4)	P98	P128	P148	P117	P2	AP20	T1	757
I/O	P99	P129	P149	P116	P1	AU21	T2	760
VCC	P100	P130	P150	P115	VCC*	VCC*	VCC*	-
GND	P101	P131	P151	P114	GND*	GND*	GND*	-
I/O (D3)	P102	P132	P152	P113	N2	AU19	T3	763
I/O (RS)	P103	P133	P153	P112	N4	AV20	R1	766
I/O	P104	P134	P154	P111	N3	AV18	R2	769
I/O	P105	P135	P155	P110	M1	AR19	R4	772
I/O	-	P136	P156	P109	M2	AT18	R3	775
I/O	-	P137	P157	P108	M3	AW17	P2	778
I/O	-	-	-	P107	M4	AV16	P3	781
I/O	-	-	-	P106	L1	AP18	P4	784
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	P158	-	GND*	GND*	GND*	-
I/O	-	-	-	P105	L2	AR17	N3	787
I/O	-	-	-	P104	L3	AT16	N4	790
I/O	-	-	-	-	K2	AV14	M1	793
I/O	-	-	-	-	L4	AW13	M2	796
I/O (D2)	P106	P138	P159	P103	J1	AR15	L2	799

XC4036EX/XL Pad Name	PQ 160††	HQ 208††	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
I/O	P107	P139	P160	P102	K3	AP16	L3	802
VCC	-	-	P161	P101	VCC*	VCC*	VCC*	-
I/O	P108	P140	P162	P99	J2	AV12	K1	805
I/O	P109	P141	P163	P98	J3	AR13	K2	808
I/O	-	-	P164	P97	K4	AU11	K3	811
I/O	-	-	P165	P96	G1	AT12	K4	814
GND	P110	P142	P166	P95	GND*	GND*	GND*	-
I/O	-	-	-	P94	H2	AP14	J2	817
I/O	-	-	-	P93	H3	AR11	J3	820
I/O	-	-	P167	P92	J4	AV10	J4	823
I/O	-	-	P168	P91	F1	AT8	H1	826
I/O	-	P143	P169	P90	G2	AT10	H2	829
I/O	-	P144	P170	P89	G3	AP10	H3	832
I/O	P111	P145	P171	P88	F2	AP12	H4	835
I/O	P112	P146	P172	P87	E2	AR9	G2	838
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O (D1)	P113	P147	P173	P86	F3	AU7	G4	841
I/O (RCLK, RDY/ BUSY)	P114	P148	P174	P85	G4	AW7	F2	844
I/O	-	-	-	-	D1	AW5	F3	847
I/O	-	-	-	-	C1	AV6	E1	850
I/O	-	-	-	P84	D2	AR7	E3	853
I/O	-	-	-	P83	F4	AV4	D1	856
I/O	P115	P149	P175	P82	E3	AN9	E4	859
I/O	P116	P150	P176	P81	C2	AW1	D2	862
I/O (D0, DIN)	P117	P151	P177	P80	D3	AP6	C2	865
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	AU3	D3	868
CCLK	P119	P153	P179	P78	C3	AR5	D4	-
VCC	P120	P154	P180	P77	VCC*	VCC*	VCC*	-
O, TDO	P121	P159	P181	P76	D4	AN7	C4	0
GND	P122	P160	P182	P75	GND*	GND*	GND*	-
I/O (A0, WS)	P123	P161	P183	P74	B3	AT4	B3	2
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	AV2	D5	5
I/O	P125	P163	P185	P72	D5	AM8	B4	8
I/O	P126	P164	P186	P71	A3	AL7	C5	11
I/O	-	-	-	-	C5	AR3	B5	14
I/O	-	-	-	-	B4	AR1	C6	17
I/O (CS1, A2)	P127	P165	P187	P70	D6	AK6	A5	20
I/O (A3)	P128	P166	P188	P69	C6	AN3	D7	23
I/O	-	-	-	P68	B5	AM6	B6	26
I/O	-	-	-	P67	A4	AM2	A6	29
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
GND	-	-	-	-	GND*	GND*	GND*	-
I/O	-	-	P189	P66	C7	AL3	D8	32
I/O	-	-	P190	P65	B6	AH6	C7	35
I/O	P129	P167	P191	P64	A6	AP2	B7	38
I/O	P130	P168	P192	P63	D8	AK4	D9	41
I/O	-	P169	P193	P62	B7	AG5	D10	44
I/O	-	P170	P194	P61	A7	AF6	C9	47
I/O	-	-	P195	P60	D9	AL5	B9	50
I/O	-	-	-	P59	C9	AJ3	C10	53
GND	P131	P171	P196	P58	GND*	GND*	GND*	-
I/O	P132	P172	P197	P57	B8	AH2	B10	56
I/O	P133	P173	P198	P56	D10	AE5	A10	59
I/O	-	-	P199	P55	C10	AM4	C11	62
I/O	-	-	P200	P54	B9	AD6	D12	65
VCC	-	-	P201	P52	VCC*	VCC*	VCC*	-
I/O	-	-	-	P51	A9	AG3	B11	68
I/O	-	-	-	P50	D11	AG1	C12	71
I/O	-	-	-	-	C11	AC5	C13	74
I/O	-	-	-	-	B10	AE1	A12	77
I/O	-	-	-	P49	B11	AH4	D14	80
I/O	-	-	-	P48	A11	AB6	B13	83
GND	-	-	-	-	GND*	GND*	GND*	-
VCC	-	-	-	-	VCC*	VCC*	VCC*	-
I/O (A4)	P134	P174	P202	P47	D12	AD2	C14	86
I/O (A5)	P135	P175	P203	P46	C12	AB4	A13	89
I/O	-	P176	P205	P45	B12	AE3	B14	92
I/O	P136	P177	P206	P44	A12	AC1	D15	95
I/O (A21)	P137	P178	P207	P43	C13	AD4	C15	98
I/O (A20)	P138	P179	P208	P42	B13	AA5	B15	101
I/O (A6)	P139	P180	P209	P41	A13	AA3	B16	104
I/O (A7)	P140	P181	P210	P40	B14	Y6	A16	107

XC4036EX/XL Pad Name	PQ 160†	HQ 208†	HQ 240	HQ 304	BG 352	PG 411	BG 432	Bndry Scan
GND	P141	P182	P211	P39	GND*	GND*	GND*	-

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

†† = XL only

## Additional XC4036EX/XL Package Pins

### HQ208

Not Connected Pins				
P1	P3	P51	P52	P53
P54	P102	P104	P105	P107
P155	P156	P157	P158	P206
P207	P208	-	-	-

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### HQ240

GND Pins				
P204	P219	-	-	-

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The Ground (GND) package pins in the above table should be externally connected to Ground if possible; however, they can be left unconnected if necessary for compatibility with other devices.

### HQ304

Not Connected Pins				
P11	P24	P53	P100	P128
P176	P205	P254	P281	-

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### BG352

VCC Pins					
A10	A17	B2	B25	D7	D13
D19	G23	H4	K1	K26	N23
P4	U1	U26	W23	Y4	AC8
AC14	AC20	AE2	AE25	AF10	AF17
GND Pins					
A1	A2	A5	A8	A14	A19
A22	A25	A26	B1	B26	E1
E26	H1	H26	N1	P26	W1
W26	AB1	AB26	AE1	AE26	AF1
AF2	AF5	AF8	AF13	AF19	AF22
AF25	AF26	-	-	-	-
Not Connected Pins					
C8	-	-	-	-	-

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### BG411

VCC Pins					
A3	A11	A21	A31	C39	D6
F36	J1	L39	W1	AA39	AJ1
AL39	AP4	AT34	AU1	AW9	AW19
AW29	AW37	-	-	-	-

### GND Pins

A9	A19	A29	A37	C1	D14
D20	D26	D34	F4	J39	L1
P4	P36	W39	Y4	Y36	AA1
AF4	AF36	AJ39	AL1	AP36	AT6
AT14	AT20	AT26	AU39	AW3	AW11
AW21	AW31	-	-	-	-

### Not Connected Pins

A13	B6	B34	C7	C15	C23
C25	C33	D8	D12	D30	D32
E7	E23	E37	F2	F18	F22
G5	H34	J5	K36	K38	L5
L35	N3	P38	R3	V2	W5
W35	Y38	AA37	AB2	AC3	AC39
AF2	AF38	AJ5	AK2	AK38	AL35
AN1	AN5	AP8	AP30	AP38	AR37
AT2	AT30	AU5	AU9	AU13	AU15
AU17	AU25	AU37	AV8	AV26	AV34
AW15	AW23	AW25	AW35	-	-

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### BG432

VCC Pins					
A1	A11	A21	A31	C3	C29
D11	D21	L1	L4	L28	L31
AA1	AA4	AA28	AA31	AH11	AH21
AJ3	AJ29	AL1	AL11	AL21	AL31

### GND Pins

A2	A3	A7	A9	A14	A18
A23	A25	A29	A30	B1	B2
B30	B31	C1	C31	D16	G1
G31	J1	J31	P1	P31	T4
T28	V1	V31	AC1	AC31	AE1
AE31	AH16	AJ1	AJ31	AK1	AK2
AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30

### Not Connected Pins

A4	A8	A15	A28	B8	B12
B17	B21	B25	C8	C16	C17
D6	D13	D20	D23	D26	E2
F1	F4	F28	F29	F30	F31
G3	M3	M4	M28	M30	N1
N2	N29	N30	V2	V28	W1
W2	W28	W31	Y1	Y31	AC4
AD2	AD30	AD31	AE4	AF29	AF30
AG1	AH6	AH9	AH19	AH23	AJ5
AJ8	AJ12	AJ15	AJ20	AJ26	AK11
AK17	AK24	AK27	AL15	AL17	-

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## Pin Locations for XC4044XL Devices

(Note: XC4044XL is also available in the HQ304 package. The pinout is identical to the XC4036XL in the HQ304. )

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
VCC	P142	P183	P212	VCC*	VCC*	VCC*
I/O (A8)	P143	P184	P213	D14	W3	D17
I/O (A9)	P144	P185	P214	C14	Y2	A17
I/O	-	-	-	-	V2	C17
I/O	-	-	-	-	W5	B17
I/O (A19)	P145	P186	P215	A15	V4	C18

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	-	-	D16	P2	B20
I/O	-	-	-	A18	N1	C20
I/O	-	-	-	C17	R5	C21
I/O	-	-	-	B18	M2	A22
VCC	-	-	P222	VCC*	VCC*	VCC*
I/O	-	-	P223	C18	L3	B22
I/O	-	-	P224	D17	T6	C22
I/O	P149	P192	P225	A20	N5	B23
I/O	P150	P193	P226	B19	M4	A24
GND	P151	P194	P227	GND*	GND*	GND*
I/O	-	-	-	C19	K2	D22
I/O	-	-	-	D18	K4	C23
I/O	-	P195	P228	A21	P6	B24
I/O	-	P196	P229	B20	M6	C24
I/O	-	-	-	-	L5	D23
I/O	-	-	-	-	J5	B25
I/O	P152	P197	P230	C20	J3	A26
I/O	P153	P198	P231	B21	H2	C25
I/O (A12)	P154	P199	P232	B22	H4	D24
I/O (A13)	P155	P200	P233	C21	G3	B26
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	D20	K6	A27
I/O	-	-	-	A23	G1	D25
I/O	-	-	-	A24	E1	C26
I/O	-	-	-	B23	E3	B27
I/O	-	-	P234	D21	J7	C27
I/O	-	-	P235	C22	H6	B28
I/O	P156	P201	P236	B24	C3	D27
I/O	P157	P202	P237	C23	D2	B29
I/O (A14)	P158	P203	P238	D22	E5	C28
I/O, GCK8 (A15)	P159	P204	P239	C24	G7	D28
VCC	P160	P205	P240	VCC*	VCC*	VCC*
GND	P1	P2	P1	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	D23	H8	D29
I/O (A17)	P3	P5	P3	C25	F6	C30
I/O	P4	P6	P4	D24	B4	E28
I/O	P5	P7	P5	E23	D4	E29
I/O, TDI	P6	P8	P6	C26	B2	D30
I/O, TCK	P7	P9	P7	E24	G9	D31
I/O	-	-	-	D25	F8	E30
I/O	-	-	-	F23	C5	E31
I/O	-	-	-	F24	A7	G28
I/O	-	-	-	E25	A5	G29
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	C7	F30
I/O	-	-	-	-	D8	F31
I/O	P8	P10	P8	D26	B8	H28
I/O	P9	P11	P9	G24	C9	H29
I/O	-	P12	P10	F25	E9	G30
I/O	-	P13	P11	F26	F12	H30
I/O	-	-	P12	H23	D10	J28
I/O	-	-	P13	H24	B10	J29
I/O	-	-	-	G25	F10	H31
I/O	-	-	-	G26	F14	J30
GND	P10	P14	P14	GND*	GND*	GND*
I/O	P11	P15	P15	J23	C11	K28
I/O	P12	P16	P16	J24	B12	K29
I/O, TMS	P13	P17	P17	H25	E11	K30
I/O	P14	P18	P18	K23	E15	K31
VCC	-	-	P19	VCC*	VCC*	VCC*
I/O	-	-	P20	K24	F16	L29
I/O	-	-	P21	J25	C13	L30
I/O	-	-	-	J26	B14	M29
I/O	-	-	-	L23	E17	M31
I/O	-	-	-	L24	E13	N31
I/O	-	-	-	K25	A15	N28
GND	-	-	P22	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	F18	N29
I/O	-	-	-	-	C15	N30
I/O	-	-	-	L25	B16	P30
I/O	-	-	-	L26	D16	P28
I/O	-	P19	P23	M23	D18	P29

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	P20	P24	M24	A17	R31
I/O	P15	P21	P25	M25	E19	R30
I/O	P16	P22	P26	M26	B18	R28
I/O	P17	P23	P27	N24	C17	R29
I/O	P18	P24	P28	N25	C19	T31
GND	P19	P25	P29	GND*	GND*	GND*
VCC	P20	P26	P30	VCC*	VCC*	VCC*
I/O	P21	P27	P31	N26	F20	T30
I/O	P22	P28	P32	P25	B20	T29
I/O	P23	P29	P33	P23	C21	U31
I/O	P24	P30	P34	P24	B22	U30
I/O	-	P31	P35	R26	E21	U28
I/O	-	P32	P36	R25	D22	U29
I/O	-	-	-	R24	A23	V30
I/O	-	-	-	R23	B24	V29
I/O	-	-	-	-	C23	V28
I/O	-	-	-	-	F22	W31
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P37	GND*	GND*	GND*
I/O	-	-	-	T26	A25	W30
I/O	-	-	-	T25	D24	W29
I/O	-	-	-	T24	B26	Y30
I/O	-	-	-	U25	A27	Y29
I/O	-	-	P38	T23	C27	Y28
I/O	-	-	P39	V26	F24	AA30
VCC	-	-	P40	VCC*	VCC*	VCC*
I/O	P25	P33	P41	U24	E25	AA29
I/O	P26	P34	P42	V25	E27	AB31
I/O	P27	P35	P43	V24	B28	AB30
I/O	P28	P36	P44	U23	C29	AB29
GND	P29	P37	P45	GND*	GND*	GND*
I/O	-	-	-	Y26	F26	AB28
I/O	-	-	-	W25	D28	AC30
I/O	-	-	P46	W24	B30	AC29
I/O	-	-	P47	V23	E29	AC28
I/O	-	-	-	D30	AD31	-
I/O	-	-	-	D32	AD30	-
I/O	-	P38	P48	AA26	F28	AD29
I/O	-	P39	P49	Y25	F30	AD28
I/O	P30	P40	P50	Y24	C31	AE30
I/O	P31	P41	P51	AA25	E31	AE29
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	AB25	B32	AF31
I/O	-	-	-	AA24	A33	AE28
I/O	P32	P42	P52	Y23	A35	AG31
I/O	P33	P43	P53	AC26	F32	AF28
I/O	-	-	-	AD26	C35	AG30
I/O	-	-	-	AC25	B38	AG29
I/O	P34	P44	P54	AA23	E33	AH31
I/O	P35	P45	P55	AB24	G31	AG28
I/O	P36	P46	P56	AD25	H32	AH30
I/O, GCK2	P37	P47	P57	AC24	B36	AJ30
O (M1)	P38	P48	P58	AB23	A39	AH29
GND	P39	P49	P59	GND*	GND*	GND*
I (M0)	P40	P50	P60	AD24	E35	AH28
VCC	P41	P55	P61	VCC*	VCC*	VCC*
I (M2)	P42	P56	P62	AC23	G33	AJ28
I/O, GCK3	P43	P57	P63	AE24	D36	AK29
I/O (HDC)	P44	P58	P64	AD23	C37	AH27
I/O	P45	P59	P65	AC22	F34	AK28
I/O	P46	P60	P66	AF24	J33	AJ27
I/O	P47	P61	P67	AD22	D38	AL28
I/O (LDC)	P48	P62	P68	AE23	G35	AH26
I/O	-	-	-	AC21	E39	AL27
I/O	-	-	-	AD21	K34	AH25
I/O	-	-	-	AE22	F38	AK26
I/O	-	-	-	AF23	G37	AL26
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	P49	P63	P69	AD20	H38	AH24
I/O	P50	P64	P70	AE21	J37	AJ25
I/O	-	P65	P71	AF21	G39	AK25
I/O	-	-	P66	P72	AC19	M34
I/O	-	-	-	K36	AH23	-

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	-	-	-	K38	AK24
I/O	-	-	P73	AD19	N35	AL24
I/O	-	-	P74	AE20	P34	AH22
I/O	-	-	-	AF20	J35	AJ23
I/O	-	-	-	AC18	L37	AK23
GND	P51	P67	P75	GND*	GND*	GND*
I/O	P52	P68	P76	AD18	M38	AJ22
I/O	P53	P69	P77	AE19	R35	AK22
I/O	P54	P70	P78	AC17	H36	AL22
I/O	P55	P71	P79	AD17	T34	AJ21
VCC	-	-	P80	VCC*	VCC*	VCC*
I/O	-	-	P72	P81	AE18	N37
I/O	-	-	P73	P82	AF18	N39
I/O	-	-	-	AC16	U35	AK20
I/O	-	-	-	AD16	R39	AJ19
I/O	-	-	-	AE17	M36	AL20
I/O	-	-	-	AE16	V34	AH18
GND	-	-	P83	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	AF16	R37
I/O	-	-	-	AC15	T38	AJ18
I/O	-	-	P84	AD15	T36	AL19
I/O	-	-	P85	AE15	V36	AK18
I/O	P56	P74	P86	AF15	U37	AH17
I/O	P57	P75	P87	AD14	U39	AJ17
I/O	-	-	-	-	W35	AK17
I/O	-	-	-	-	AC39	AL17
I/O	P58	P76	P88	AE14	V38	AJ16
I/O (INIT)	P59	P77	P89	AF14	W37	AK16
VCC	P60	P78	P90	VCC*	VCC*	VCC*
GND	P61	P79	P91	GND*	GND*	GND*
I/O	P62	P80	P92	AE13	Y34	AL16
I/O	P63	P81	P93	AC13	AC37	AH15
I/O	-	-	-	-	Y38	AL15
I/O	-	-	-	-	AA37	AJ15
I/O	P64	P82	P94	AD13	AB38	AK15
I/O	P65	P83	P95	AF12	AD36	AJ14
I/O	-	P84	P96	AE12	AA35	AH14
I/O	-	P85	P97	AD12	AE37	AK14
I/O	-	-	-	AC12	AB36	AL13
I/O	-	-	-	AF11	AD38	AK13
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P98	GND*	GND*	GND*
I/O	-	-	-	AE11	AB34	AJ13
I/O	-	-	-	AD11	AE39	AH13
I/O	-	-	-	AE10	AM36	AL12
I/O	-	-	-	AC11	AC35	AK12
I/O	-	-	P99	AF9	AG39	AH12
I/O	-	-	P100	AD10	AG37	AJ11
VCC	-	-	P101	VCC*	VCC*	VCC*
I/O	P66	P86	P102	AE9	AD34	AL10
I/O	P67	P87	P103	AD9	AN39	AK10
I/O	P68	P88	P104	AC10	AE35	AJ10
I/O	P69	P89	P105	AF7	AH38	AK9
GND	P70	P90	P106	GND*	GND*	GND*
I/O	-	-	-	AE8	AJ37	AL8
I/O	-	-	-	AD8	AG35	AH10
I/O	-	-	P107	AC9	AF34	AJ9
I/O	-	-	P108	AF6	AH36	AK8
I/O	-	-	-	-	AK38	AJ8
I/O	-	-	-	-	AP38	AH9
I/O	-	P91	P109	AE7	AK36	AK7
I/O	-	P92	P110	AD7	AM34	AL6
I/O	P71	P93	P111	AE6	AH34	AJ7
I/O	P72	P94	P112	AE5	AJ35	AH8
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	AD6	AL37	AK6
I/O	-	-	-	AC7	AT38	AL5
I/O	P73	P95	P113	AF4	AM38	AH7
I/O	P74	P96	P114	AF3	AN37	AJ6
I/O	-	-	-	AE4	AK34	AK5
I/O	-	-	-	AC6	AR39	AL4
I/O	P75	P97	P115	AD5	AN35	AK4
I/O	P76	P98	P116	AE3	AL33	AH5

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	P77	P99	P117	AD4	AV38	AK3
I/O, GCK4	P78	P100	P118	AC5	AT36	AJ4
GND	P79	P101	P119	GND*	GND*	GND*
DONE	P80	P103	P120	AD3	AR35	AH4
VCC	P81	P106	P121	VCC*	VCC*	VCC*
PROGRAM	P82	P108	P122	AC4	AN33	AH3
I/O (D7)	P83	P109	P123	AD2	AM32	AJ2
I/O, GCK5	P84	P110	P124	AC3	AP34	AG4
I/O	P85	P111	P125	AB4	AW39	AG3
I/O	P86	P112	P126	AD1	AN31	AH2
I/O	-	-	-	AB3	AV36	AH1
I/O	-	-	-	AC2	AR33	AF4
I/O	-	-	P127	AA4	AP32	AF3
I/O	-	-	P128	AA3	AU35	AG2
I/O	-	-	-	AB2	AW33	AE3
I/O	-	-	-	AC1	AU33	AF2
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O (D6)	P87	P113	P129	Y3	AV32	AF1
I/O	P88	P114	P130	AA2	AU31	AD4
I/O	P89	P115	P131	AA1	AR31	AD3
I/O	P90	P116	P132	W4	AP28	AE2
I/O	-	-	-	-	AP30	AD2
I/O	-	-	-	-	AT30	AC4
I/O	-	P117	P133	W3	AT32	AC3
I/O	-	P118	P134	Y2	AV30	AD1
I/O	-	-	-	Y1	AR29	AC2
I/O	-	-	-	V4	AP26	AB4
GND	P91	P119	P135	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O (D5)	P94	P122	P141	V2	AP24	AA2
I/O (CS0)	P95	P123	P142	V1	AU27	Y2
I/O	-	-	-	T4	AR27	Y4
I/O	-	-	-	T3	AW27	Y3
I/O	-	-	-	U2	AT24	W4
I/O	-	-	-	T2	AT23	W3
GND	-	-	P143	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	AW25	W2
I/O	-	-	-	-	AW23	V2
I/O	-	-	-	T1	AP22	V4
I/O	-	-	-	R4	AV24	V3
I/O	-	P124	P144	R3	AU23	U1
I/O	-	P125	P145	R2	AT22	U2
I/O	P96	P126	P146	R1	AR21	U4
I/O	P97	P127	P147	P3	AV22	U3
I/O (D4)	P98	P128	P148	P2	AP20	T1
I/O	P99	P129	P149	P1	AU21	T2
VCC	P100	P130	P150	VCC*	VCC*	VCC*
GND	P101	P131	P151	GND*	GND*	GND*
I/O (D3)	P102	P132	P152	N2	AU19	T3
I/O (RS)	P103	P133	P153	N4	AV20	R1
I/O	P104	P134	P154	N3	AV18	R2
I/O	P105	P135	P155	M1	AR19	R4
I/O	-	P136	P156	M2	AT18	R3
I/O	-	P137	P157	M3	AW17	P2
I/O	-	-	-	M4	AV16	P3
I/O	-	-	-	L1	AP18	P4
I/O	-	-	-	-	AU17	N1
I/O	-	-	-	-	AW15	N2
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P158	GND*	GND*	GND*
I/O	-	-	-	L2	AR17	N3
I/O	-	-	-	L3	AT16	N4
I/O	-	-	-	K2	AV14	M1
I/O	-	-	-	L4	AW13	M2
I/O (D2)	P106	P138	P159	J1	AR15	L2
I/O	P107	P139	P160	K3	AP16	L3
VCC	-	-	P161	VCC*	VCC*	VCC*
I/O	P108	P140	P162	J2	AV12	K1
I/O	P109	P141	P163	J3	AR13	K2

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
I/O	-	-	P164	K4	AU11	K3
I/O	-	-	P165	G1	AT12	K4
GND	P110	P142	P166	GND*	GND*	GND*
I/O	-	-	-	H2	AP14	J2
I/O	-	-	-	H3	AR11	J3
I/O	-	-	P167	J4	AV10	J4
I/O	-	-	P168	F1	AT8	H1
I/O	-	P143	P169	G2	AT10	H2
I/O	-	P144	P170	G3	AP10	H3
I/O	P111	P145	P171	F2	AP12	H4
I/O	P112	P146	P172	E2	AR9	G2
I/O	-	-	-	-	AU9	G3
I/O	-	-	-	-	AV8	F1
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O (D1)	P113	P147	P173	F3	AU7	G4
I/O (RCLK, RDY/BUSY)	P114	P148	P174	G4	AW7	F2
I/O	-	-	-	D1	AW5	F3
I/O	-	-	-	C1	AV6	E1
I/O	-	-	-	D2	AR7	E3
I/O	-	-	-	F4	AV4	D1
I/O	P115	P149	P175	E3	AN9	E4
I/O	P116	P150	P176	C2	AW1	D2
I/O (D0, DIN)	P117	P151	P177	D3	AP6	C2
I/O, GCK6 (DOUT)	P118	P152	P178	E4	AU3	D3
CCLK	P119	P153	P179	C3	AR5	D4
VCC	P120	P154	P180	VCC*	VCC*	VCC*
O, TDO	P121	P159	P181	D4	AN7	C4
GND	P122	P160	P182	GND*	GND*	GND*
I/O (A0, WS)	P123	P161	P183	B3	AT4	B3
I/O, GCK7 (A1)	P124	P162	P184	C4	AV2	D5
I/O	P125	P163	P185	D5	AM8	B4
I/O	P126	P164	P186	A3	AL7	C5
I/O	-	-	-	C5	AR3	B5
I/O	-	-	-	B4	AR1	C6
I/O (CS1,A2)	P127	P165	P187	D6	AK6	A5
I/O (A3)	P128	P166	P188	C6	AN3	D7
I/O	-	-	-	B5	AM6	B6
I/O	-	-	-	A4	AM2	A6
VCC	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	GND*	GND*	GND*
I/O	-	-	P189	C7	AL3	D8
I/O	-	-	P190	B6	AH6	C7
I/O	P129	P167	P191	A6	AP2	B7
I/O	P130	P168	P192	D8	AK4	D9
I/O	-	-	-	C8	AN1	B8
I/O	-	-	-	-	AK2	A8
I/O	-	P169	P193	B7	AG5	D10
I/O	-	P170	P194	A7	AF6	C9
I/O	-	-	P195	D9	AL5	B9
I/O	-	-	-	C9	AJ3	C10
GND	P131	P171	P196	GND*	GND*	GND*
I/O	P132	P172	P197	B8	AH2	B10
I/O	P133	P173	P198	D10	AE5	A10
I/O	-	-	P199	C10	AM4	C11
I/O	-	-	P200	B9	AD6	D12
VCC	-	-	P201	VCC*	VCC*	VCC*
I/O	-	-	-	A9	AG3	B11
I/O	-	-	-	D11	AG1	C12
I/O	-	-	-	C11	AC5	C13
I/O	-	-	-	B10	AE1	A12
I/O	-	-	-	B11	AH4	D14
I/O	-	-	-	A11	AB6	B13
GND	-	-	-	GND*	GND*	GND*
VCC	-	-	-	VCC*	VCC*	VCC*
I/O (A4)	P134	P174	P202	D12	AD2	C14
I/O (A5)	P135	P175	P203	C12	AB4	A13
I/O	-	P176	P205	B12	AE3	B14
I/O	P136	P177	P206	A12	AC1	D15
I/O (A21)	P137	P178	P207	C13	AD4	C15
I/O (A20)	P138	P179	P208	B13	AA5	B15
I/O	-	-	-	-	AB2	A15
I/O	-	-	-	-	AC3	C16
I/O (A6)	P139	P180	P209	A13	AA3	B16
I/O (A7)	P140	P181	P210	B14	Y6	A16

XC4044XL Pad Name	HQ 160	HQ 208	HQ 240	BG 352	PG 411	BG 432
GND	P141	P182	P211	GND*	GND*	GND*

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

## Additional XC4044XL Package Pins

### HQ208

Not Connected Pins						
P1	P3	P51	P52	P53	P54	P102
P104	P105	P107	P155	P156	P157	P158
P206	P207	P208	-	-	-	-

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### HQ240

GND Pins						
P204	P219	-	-	-	-	-

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Note: These pins may be Not Connected for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

### BG352

VCC Pins						
A10	A17	B2	B25	D7	D13	D19
G23	H4	K1	K26	N23	P4	U1
U26	W23	Y4	AC8	AC14	AC20	AE2
AE25	AF10	AF17	-	-	-	-

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### PG411

VCC Pins						
A3	A11	A21	A31	C39	D6	F36
J1	L39	W1	AA39	AJ1	AL39	AP4
AT34	AU1	AW9	AW19	AW29	AW37	-

GND Pins						
A9	A19	A29	A37	C1	D14	D20
D26	D34	F4	J39	L1	P4	P36
W39	Y4	Y36	AA1	AF4	AF36	AJ39
AL1	AP36	AT6	AT14	AT20	AT26	AU39
AW3	AW11	AW21	AW31	-	-	-

Not Connected Pins						
A13	B6	B34	C25	C33	D12	E7
E23	E37	F2	G5	H34	L35	N3
P38	R3	AF2	AF38	AJ5	AL35	AN5
AP8	AR37	AT2	AU5	AU13	AU15	AU25
AU37	AV26	AV34	AW35	-	-	-

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**BG432**

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
Not Connected Pins						
A4	A28	B12	B21	C8	D6	D13
D20	D26	E2	F4	F28	F29	M3
M4	M28	M30	W1	W28	Y1	Y31
AE4	AF29	AF30	AG1	AH6	AH19	AJ5
AJ12	AJ20	AJ26	AK11	AK27	-	-

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## Pin Locations for XC4052XL Devices

(Note: XC4052XL is also available in the HQ304 package. The pinout is identical to the XC4036XL in HQ304.)

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
VCC	P212	VCC*	VCC*	VCC*
I/O (A8)	P213	W3	D17	A17
I/O (A9)	P214	Y2	A17	B18
I/O	-	V2	C17	C18
I/O	-	W5	B17	E18
GND	-	GND*	GND*	GND*
I/O (A19)	P215	V4	C18	C19
I/O (A18)	P216	T2	D18	D19
I/O	P217	U1	B18	E19
I/O	P218	V6	A19	B20
I/O (A10)	P220	U3	B19	C20
I/O (A11)	P221	R1	C19	D20
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	U5	D19	A21
I/O	-	T4	A20	E20
I/O	-	P2	B20	B21
I/O	-	N1	C20	C21
I/O	-	R3	B21	D21
I/O	-	N3	D20	B22
GND	-	GND*	GND*	GND*
I/O	-	R5	C21	C23
I/O	-	M2	A22	E22
VCC	P222	VCC*	VCC*	VCC*
I/O	P223	L3	B22	B24
I/O	P224	T6	C22	D23
I/O	P225	N5	B23	C24
I/O	P226	M4	A24	A25
GND	P227	GND*	GND*	GND*
I/O	-	K2	D22	E23
I/O	-	K4	C23	B25
I/O	P228	P6	B24	D24
I/O	P229	M6	C24	C25
GND	-	GND*	GND*	GND*
I/O	-	L5	D23	E25
I/O	-	J5	B25	C27
I/O	P230	J3	A26	D26
I/O	P231	H2	C25	B28
I/O (A12)	P232	H4	D24	B29
I/O (A13)	P233	G3	B26	E26

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	K6	A27	C28
I/O	-	G1	D25	D27
I/O	-	E1	C26	B30
I/O	-	E3	B27	C29
I/O	-	F2	A28	E27
I/O	-	G5	D26	A31
GND	-	GND*	GND*	GND*
I/O	P234	J7	C27	D28
I/O	P235	H6	B28	C30
I/O	P236	C3	D27	D29
I/O	P237	D2	B29	E28
I/O (A14)	P238	E5	C28	D30
I/O, GCK8 (A15)	P239	G7	D28	E29
VCC	P240	VCC*	VCC*	VCC*
GND	P1	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	H8	D29	B33
I/O (A17)	P3	F6	C30	F29
I/O	P4	B4	E28	E30
I/O	P5	D4	E29	D31
I/O, TDI	P6	B2	D30	F30
I/O, TCK	P7	G9	D31	C33
GND	-	GND*	GND*	GND*
I/O	-	E7	F28	G29
I/O	-	B6	F29	E31
I/O	-	F8	E30	D32
I/O	-	C5	E31	G30
I/O	-	A7	G28	F31
I/O	-	A5	G29	H29
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	C7	F30	H30
I/O	-	D8	F31	G31
I/O	P8	B8	H28	J29
I/O	P9	C9	H29	F33
I/O	P10	E9	G30	G32
I/O	P11	F12	H30	J30
GND	-	GND*	GND*	GND*
I/O	P12	D10	J28	K30
I/O	P13	B10	J29	H33
I/O	-	F10	H31	L29
I/O	-	F14	J30	K31
GND	P14	GND*	GND*	GND*
I/O	P15	C11	K28	L30

<b>XC4052XL Pad Name</b>	<b>HQ 240</b>	<b>PG 411</b>	<b>BG 432</b>	<b>BG 560</b>
I/O	P16	B12	K29	K32
I/O, TMS	P17	E11	K30	J33
I/O	P18	E15	K31	M29
VCC	P19	VCC*	VCC*	VCC*
I/O	P20	F16	L29	L32
I/O	P21	C13	L30	M31
GND	-	GND*	GND*	GND*
I/O	-	A13	M30	N29
I/O	-	D12	M28	L33
I/O	-	B14	M29	M32
I/O	-	E17	M31	P29
I/O	-	E13	N31	P30
I/O	-	A15	N28	N33
GND	P22	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	F18	N29	P31
I/O	-	C15	N30	P32
I/O	-	B16	P30	R29
I/O	-	D16	P28	R30
I/O	P23	D18	P29	R31
I/O	P24	A17	R31	R33
GND	-	GND*	GND*	GND*
I/O	P25	E19	R30	T31
I/O	P26	B18	R28	T29
I/O	P27	C17	R29	U32
I/O	P28	C19	T31	U31
GND	P29	GND*	GND*	GND*
VCC	P30	VCC*	VCC*	VCC*
I/O	P31	F20	T30	U29
I/O	P32	B20	T29	U30
I/O	P33	C21	U31	V31
I/O	P34	B22	U30	V29
GND	-	GND*	GND*	GND*
I/O	P35	E21	U28	V30
I/O	P36	D22	U29	W33
I/O	-	A23	V30	W31
I/O	-	B24	V29	W30
I/O	-	C23	V28	W29
I/O	-	F22	W31	Y32
VCC	-	VCC*	VCC*	VCC*
GND	P37	GND*	GND*	GND*
I/O	-	A25	W30	Y31
I/O	-	D24	W29	Y30
I/O	-	E23	W28	AA32
I/O	-	C25	Y31	AA31
I/O	-	B26	Y30	AA30
I/O	-	A27	Y29	AB32
GND	-	GND*	GND*	GND*
I/O	P38	C27	Y28	AA29
I/O	P39	F24	AA30	AB31
VCC	P40	VCC*	VCC*	VCC*
I/O	P41	E25	AA29	AC31
I/O	P42	E27	AB31	AB29
I/O	P43	B28	AB30	AD32
I/O	P44	C29	AB29	AC30
GND	P45	GND*	GND*	GND*
I/O	-	F26	AB28	AD31
I/O	-	D28	AC30	AE33
I/O	P46	B30	AC29	AC29
I/O	P47	E29	AC28	AE32
GND	-	GND*	GND*	GND*
I/O	-	D30	AD31	AG33
I/O	-	D32	AD30	AH33
I/O	P48	F28	AD29	AE29
I/O	P49	F30	AD28	AG31
I/O	P50	C31	AE30	AF30
I/O	P51	E31	AE29	AH32
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	B32	AF31	AJ32

<b>XC4052XL Pad Name</b>	<b>HQ 240</b>	<b>PG 411</b>	<b>BG 432</b>	<b>BG 560</b>
I/O	-	A33	AE28	AF29
I/O	-	C33	AF30	AH31
I/O	-	B34	AF29	AG30
I/O	P52	A35	AG31	AK32
I/O	P53	F32	AF28	AJ31
GND	-	GND*	GND*	GND*
I/O	-	C35	AG30	AG29
I/O	-	B38	AG29	AL33
I/O	P54	E33	AH31	AH30
I/O	P55	G31	AG28	AK31
I/O	P56	H32	AH30	AJ30
I/O, GCK2	P57	B36	AJ30	AH29
O (M1)	P58	A39	AH29	AK30
GND	P59	GND*	GND*	GND*
I (M0)	P60	E35	AH28	AJ29
VCC	P61	VCC*	VCC*	VCC*
I (M2)	P62	G33	AJ28	AN32
I/O, GCK3	P63	D36	AK29	AJ28
I/O (HDC)	P64	C37	AH27	AK29
I/O	P65	F34	AK28	AL30
I/O	P66	J33	AJ27	AK28
I/O	P67	D38	AL28	AM31
I/O (LDC)	P68	G35	AH26	AJ27
GND	-	GND*	GND*	GND*
I/O	-	E37	AK27	AN31
I/O	-	H34	AJ26	AL29
I/O	-	E39	AL27	AK27
I/O	-	K34	AH25	AL28
I/O	-	F38	AK26	AJ26
I/O	-	G37	AL26	AM30
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P69	H38	AH24	AM29
I/O	P70	J37	AJ25	AK26
I/O	P71	G39	AK25	AL27
I/O	P72	M34	AJ24	AJ25
I/O	-	K36	AH23	AN29
I/O	-	K38	AK24	AN28
GND	-	GND*	GND*	GND*
I/O	P73	N35	AL24	AL25
I/O	P74	P34	AH22	AJ23
I/O	-	J35	AJ23	AN26
I/O	-	L37	AK23	AL24
GND	P75	GND*	GND*	GND*
I/O	P76	M38	AJ22	AK23
I/O	P77	R35	AK22	AN25
I/O	P78	H36	AL22	AJ22
I/O	P79	T34	AJ21	AL23
VCC	P80	VCC*	VCC*	VCC*
I/O	P81	N37	AH20	AM24
I/O	P82	N39	AK21	AK22
GND	-	GND*	GND*	GND*
I/O	-	P38	AJ20	AK21
I/O	-	L35	AH19	AM22
I/O	-	U35	AK20	AJ20
I/O	-	R39	AJ19	AL21
I/O	-	M36	AL20	AN21
I/O	-	V34	AH18	AK20
GND	P83	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	R37	AK19	AL20
I/O	-	T38	AJ18	AJ19
I/O	P84	T36	AL19	AM20
I/O	P85	V36	AK18	AK19
I/O	P86	U37	AH17	AL19
I/O	P87	U39	AJ17	AN19
GND	-	GND*	GND*	GND*
I/O	-	W35	AK17	AL18
I/O	-	AC39	AL17	AM18
I/O	P88	V38	AJ16	AK17

<b>XC4052XL Pad Name</b>	<b>HQ 240</b>	<b>PG 411</b>	<b>BG 432</b>	<b>BG 560</b>
I/O (INIT)	P89	W37	AK16	AJ17
VCC	P90	VCC*	VCC*	VCC*
GND	P91	GND*	GND*	GND*
I/O	P92	Y34	AL16	AL17
I/O	P93	AC37	AH15	AM17
I/O	-	Y38	AL15	AN17
I/O	-	AA37	AJ15	AK16
GND	-	GND*	GND*	GND*
I/O	P94	AB38	AK15	AM16
I/O	P95	AD36	AJ14	AL15
I/O	P96	AA35	AH14	AK15
I/O	P97	AE37	AK14	AJ15
I/O	-	AB36	AL13	AN15
I/O	-	AD38	AK13	AM14
VCC	-	VCC*	VCC*	VCC*
GND	P98	GND*	GND*	GND*
I/O	-	AB34	AJ13	AL14
I/O	-	AE39	AH13	AK14
I/O	-	AM36	AL12	AJ14
I/O	-	AC35	AK12	AN13
I/O	-	AL35	AJ12	AM13
I/O	-	AF38	AK11	AL13
GND	-	GND*	GND*	GND*
I/O	P99	AG39	AH12	AK12
I/O	P100	AG37	AJ11	AN11
VCC	P101	VCC*	VCC*	VCC*
I/O	P102	AD34	AL10	AJ12
I/O	P103	AN39	AK10	AL11
I/O	P104	AE35	AJ10	AK11
I/O	P105	AH38	AK9	AM10
GND	P106	GND*	GND*	GND*
I/O	-	AJ37	AL8	AL10
I/O	-	AG35	AH10	AJ11
I/O	P107	AF34	AJ9	AN9
I/O	P108	AH36	AK8	AK10
GND	-	GND*	GND*	GND*
I/O	-	AK38	AJ8	AN7
I/O	-	AP38	AH9	AJ9
I/O	P109	AK36	AK7	AL7
I/O	P110	AM34	AL6	AK8
I/O	P111	AH34	AJ7	AN6
I/O	P112	AJ35	AH8	AM6
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AL37	AK6	AJ8
I/O	-	AT38	AL5	AL6
I/O	P113	AM38	AH7	AK7
I/O	P114	AN37	AJ6	AM5
I/O	-	AK34	AK5	AM4
I/O	-	AR39	AL4	AJ7
GND	-	GND*	GND*	GND*
I/O	-	AR37	AH6	AL5
I/O	-	AU37	AJ5	AK6
I/O	P115	AN35	AK4	AN3
I/O	P116	AL33	AH5	AK5
I/O	P117	AV38	AK3	AJ6
I/O, GCK4	P118	AT36	AJ4	AL4
GND	P119	GND*	GND*	GND*
DONE	P120	AR35	AH4	AJ5
VCC	P121	VCC*	VCC*	VCC*
PROGRAM	P122	AN33	AH3	AM1
I/O (D7)	P123	AM32	AJ2	AH5
I/O, GCK5	P124	AP34	AG4	AJ4
I/O	P125	AW39	AG3	AK3
I/O	P126	AN31	AH2	AH4
I/O	-	AV36	AH1	AL1
I/O	-	AR33	AF4	AG5
GND	-	GND*	GND*	GND*
I/O	P127	AP32	AF3	AJ3
I/O	P128	AU35	AG2	AK2

<b>XC4052XL Pad Name</b>	<b>HQ 240</b>	<b>PG 411</b>	<b>BG 432</b>	<b>BG 560</b>
I/O	-	AV34	AG1	AG4
I/O	-	AW35	AE4	AH3
I/O	-	AW33	AE3	AF5
I/O	-	AU33	AF2	AJ2
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O (D6)	P129	AV32	AF1	AJ1
I/O	P130	AU31	AD4	AF4
I/O	P131	AR31	AD3	AG3
I/O	P132	AP28	AE2	AE5
I/O	-	AP30	AD2	AH1
I/O	-	AT30	AC4	AF3
GND	-	GND*	GND*	GND*
I/O	P133	AT32	AC3	AE3
I/O	P134	AV30	AD1	AC5
I/O	-	AR29	AC2	AE1
I/O	-	AP26	AB4	AD3
GND	P135	GND*	GND*	GND*
I/O	P136	AU29	AB3	AC4
I/O	P137	AV28	AB2	AD2
I/O	P138	AT28	AB1	AB5
I/O	P139	AR25	AA3	AC3
VCC	P140	VCC*	VCC*	VCC*
I/O (D5)	P141	AP24	AA2	AA5
I/O (CS0)	P142	AU27	Y2	AB3
GND	-	GND*	GND*	GND*
I/O	-	AR27	Y4	AB2
I/O	-	AW27	Y3	AA4
I/O	-	AU25	Y1	AA3
I/O	-	AV26	W1	Y5
I/O	-	AT24	W4	Y3
I/O	-	AR23	W3	Y2
GND	P143	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AW25	W2	W5
I/O	-	AW23	V2	W4
I/O	-	AP22	V4	W3
I/O	-	AV24	V3	W1
I/O	P144	AU23	U1	V3
I/O	P145	AT22	U2	V5
GND	-	GND*	GND*	GND*
I/O	P146	AR21	U4	V4
I/O	P147	AV22	U3	V2
I/O (D4)	P148	AP20	T1	U5
I/O	P149	AU21	T2	U4
VCC	P150	VCC*	VCC*	VCC*
GND	P151	GND*	GND*	GND*
I/O (D3)	P152	AU19	T3	U3
I/O (RS)	P153	AV20	R1	T2
I/O	P154	AV18	R2	T4
I/O	P155	AR19	R4	R1
GND	-	GND*	GND*	GND*
I/O	P156	AT18	R3	R3
I/O	P157	AW17	P2	R4
I/O	-	AV16	P3	R5
I/O	-	AP18	P4	P2
I/O	-	AU17	N1	P3
I/O	-	AW15	N2	P4
VCC	-	VCC*	VCC*	VCC*
GND	P158	GND*	GND*	GND*
I/O	-	AR17	N3	N1
I/O	-	AT16	N4	P5
I/O	-	AV14	M1	N2
I/O	-	AW13	M2	N3
I/O	-	AU15	M3	N5
I/O	-	AU13	M4	M3
GND	-	GND*	GND*	GND*
I/O (D2)	P159	AR15	L2	M4
I/O	P160	AP16	L3	L1
VCC	P161	VCC*	VCC*	VCC*

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	P162	AV12	K1	K2
I/O	P163	AR13	K2	L4
I/O	P164	AU11	K3	J1
I/O	P165	AT12	K4	K3
GND	P166	GND*	GND*	GND*
I/O	-	AP14	J2	L5
I/O	-	AR11	J3	J2
I/O	P167	AV10	J4	K4
I/O	P168	AT8	H1	J3
GND	-	GND*	GND*	GND*
I/O	P169	AT10	H2	G1
I/O	P170	AP10	H3	F1
I/O	P171	AP12	H4	J5
I/O	P172	AR9	G2	G3
I/O	-	AU9	G3	H4
I/O	-	AV8	F1	F2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (D1)	P173	AU7	G4	F3
I/O (RCLK, RDY/BUSY)	P174	AW7	F2	G4
I/O	-	AW5	F3	D2
I/O	-	AV6	E1	E3
I/O	-	AU5	F4	G5
I/O	-	AP8	E2	C1
GND	-	GND*	GND*	GND*
I/O	-	AR7	E3	F4
I/O	-	AV4	D1	D3
I/O	P175	AN9	E4	B3
I/O	P176	AW1	D2	F5
I/O (D0, DIN)	P177	AP6	C2	E4
I/O, GCK6 (DOUT)	P178	AU3	D3	D4
CCLK	P179	AR5	D4	C4
VCC	P180	VCC*	VCC*	VCC*
O, TDO	P181	AN7	C4	E6
GND	P182	GND*	GND*	GND*
I/O (A0, WS)	P183	AT4	B3	D5
I/O, GCK7 (A1)	P184	AV2	D5	A2
I/O	P185	AM8	B4	D6
I/O	P186	AL7	C5	A3
I/O	-	AT2	A4	E7
I/O	-	AN5	D6	C5
GND	-	GND*	GND*	GND*
I/O	-	AR3	B5	B4
I/O	-	AR1	C6	D7
I/O (CS1, A2)	P187	AK6	A5	C6
I/O (A3)	P188	AN3	D7	E8
I/O	-	AM6	B6	B5
I/O	-	AM2	A6	A5
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P189	AL3	D8	D8
I/O	P190	AH6	C7	C7
I/O	P191	AP2	B7	E9
I/O	P192	AK4	D9	A6
I/O	-	AN1	B8	B7
I/O	-	AK2	A8	D9
GND	-	GND*	GND*	GND*
I/O	P193	AG5	D10	E11
I/O	P194	AF6	C9	A9
I/O	P195	AL5	B9	C10
I/O	-	AJ3	C10	D11
GND	P196	GND*	GND*	GND*
I/O	P197	AH2	B10	B10
I/O	P198	AE5	A10	E12
I/O	P199	AM4	C11	C11
I/O	P200	AD6	D12	B11
VCC	P201	VCC*	VCC*	VCC*
I/O	-	AG3	B11	D12
I/O	-	AG1	C12	A11
GND	-	GND*	GND*	GND*

XC4052XL Pad Name	HQ 240	PG 411	BG 432	BG 560
I/O	-	AF2	D13	C13
I/O	-	AJ5	B12	E14
I/O	-	AC5	C13	A13
I/O	-	AE1	A12	D14
I/O	-	AH4	D14	C14
I/O	-	AB6	B13	B14
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (A4)	P202	AD2	C14	E15
I/O (A5)	P203	AB4	A13	D15
I/O	P205	AE3	B14	C15
I/O	P206	AC1	D15	A15
I/O (A21)	P207	AD4	C15	C16
I/O (A20)	P208	AA5	B15	E16
GND	-	GND*	GND*	GND*
I/O	-	AB2	A15	B17
I/O	-	AC3	C16	C17
I/O (A6)	P209	AA3	B16	E17
I/O (A7)	P210	Y6	A16	D17
GND	P211	GND*	GND*	GND*

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

## Additional XC4052XL Package Pins

HQ240

GND Pins						
P204	P219	-	-	-	-	-

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Note: These pins may be Not Connected for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

PG411

VCC Pins						
A3	A11	A21	A31	C39	D6	F36
J1	L39	W1	AA39	AJ1	AL39	AP4
AT34	AU1	AW9	AW19	AW29	AW37	-
GND Pins						
A9	A19	A29	A37	C1	D14	D20
D26	D34	F4	J39	LI	P4	P36
W39	Y4	Y36	AA1	AF4	AF36	AJ39
AL1	AP36	AT6	AT14	AT20	AT26	AU39
AW3	AW11	AW21	AW31	-	-	-

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BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
Not Connected Pins						
C8	-	-	-	-	-	-

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## PG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM7	AM11	AM19	AM25	AM28	AM33	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
Not Connected Pins						
A1	A8	A19	A23	A27	A28	A33
B8	B12	B16	B26	C8	C9	C12
C22	C26	D10	D13	D16	D18	D22
D25	E2	E10	E13	E21	E24	E32
E33	H2	H3	H5	H31	H32	J4
J31	K5	K29	L3	L31	M2	M5
M30	N4	N30	N31	T3	T5	T30
T32	U1	U2	U33	V32	Y4	Y29
AA1	AA33	AB4	AB30	AC1	AC2	AC33
AD4	AD5	AD29	AD30	AE4	AE30	AE31
AF1	AF2	AF31	AF32	AG2	AJ10	AJ13
AJ16	AJ18	AJ21	AJ24	AK9	AK13	AK18
AK24	AK25	AL8	AL9	AL12	AL16	AL22
AL26	AM8	AM9	AM12	AM23	AM26	AM27
AN1	AN23	AN33	-	-	-	-

6/20/97

## Pin Locations for XC4062XL Devices

(Note: XC4062XL is also available in the HQ304 package.  
The pinout is identical to the XC4036XL in HQ304.)

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
VCC	P212	VCC*	VCC*	VCC*
I/O (A8)	P213	D17	Y2	A17
I/O (A9)	P214	A17	Y4	B18
I/O	-	C17	W5	C18
I/O	-	B17	Y6	E18
I/O	-	-	U3	D18
I/O	-	-	W3	A19
GND	-	GND*	GND*	GND*
I/O (A19)	P215	C18	W1	C19
I/O (A18)	P216	D18	U5	D19
I/O	P217	B18	W7	E19
I/O	P218	A19	U7	B20
I/O (A10)	P220	B19	V2	C20
I/O (A11)	P221	C19	V4	D20
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	D19	V6	A21
I/O	-	A20	R1	E20
I/O	-	B20	T6	B21
I/O	-	C20	R3	C21
I/O	-	B21	R5	D21
I/O	-	D20	T4	B22
GND	-	GND*	GND*	GND*
I/O	-	C21	P2	C23
I/O	-	A22	N1	E22
VCC	P222	VCC*	VCC*	VCC*
I/O	P223	B22	N3	B24

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	P224	C22	P4	D23
I/O	P225	B23	R7	C24
I/O	P226	A24	M2	A25
GND	P227	GND*	GND*	GND*
I/O	-	D22	M4	E23
I/O	-	C23	L3	B25
I/O	P228	B24	N5	D24
I/O	P229	C24	K2	C25
I/O	-	-	L5	B26
I/O	-	-	J1	E24
GND	-	GND*	GND*	GND*
I/O	-	D23	M6	E25
I/O	-	B25	K4	C27
I/O	P230	A26	J3	D26
I/O	P231	C25	J5	B28
I/O (A12)	P232	D24	H2	B29
I/O (A13)	P233	B26	G1	E26
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	A27	L7	C28
I/O	-	D25	K6	D27
I/O	-	C26	E1	B30
I/O	-	B27	H4	C29
I/O	-	A28	G5	E27
I/O	-	D26	F2	A31
GND	-	GND*	GND*	GND*
I/O	P234	C27	H6	D28
I/O	P235	B28	C3	C30
I/O	P236	D27	F4	D29
I/O	P237	B29	C5	E28

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O (A14)	P238	C28	E3	D30
I/O GCK8 (A15)	P239	D28	E5	E29
VCC	P240	VCC*	VCC*	VCC*
GND	P1	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	D29	G7	B33
I/O (A17)	P3	C30	D4	F29
I/O	P4	E28	A5	E30
I/O	P5	E29	B4	D31
I/O, TDI	P6	D30	D6	F30
I/O, TCK	P7	D31	F8	C33
GND	-	GND*	GND*	GND*
I/O	-	F28	B6	G29
I/O	-	F29	E7	E31
I/O	-	E30	D8	D32
I/O	-	E31	G9	G30
I/O	-	G28	E9	F31
I/O	-	G29	A7	H29
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	-	F30	B8	H30
I/O	-	F31	C9	G31
I/O	P8	H28	G11	J29
I/O	P9	H29	D10	F33
I/O	P10	G30	E11	G32
I/O	P11	H30	A9	J30
GND	-	GND*	GND*	GND*
I/O	-	-	B10	H32
I/O	-	-	C11	J31
I/O	P12	J28	F12	K30
I/O	P13	J29	D12	H33
I/O	-	H31	A11	L29
I/O	-	J30	G15	K31
GND	P14	GND*	GND*	GND*
I/O	P15	K28	B12	L30
I/O	P16	K29	E13	K32
I/O, TMS	P17	K30	C13	J33
I/O	P18	K31	A13	M29
VCC	P19	VCC*	VCC*	VCC*
I/O	P20	L29	B14	L32
I/O	P21	L30	C15	M31
GND	-	GND*	GND*	GND*
I/O	-	M30	G17	N29
I/O	-	M28	F14	L33
I/O	-	M29	D16	M32
I/O	-	M31	D14	P29
I/O	-	N31	A15	P30
I/O	-	N28	C17	N33
GND	P22	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	N29	D18	P31
I/O	-	N30	B18	P32
I/O	-	P30	F16	R29
I/O	-	P28	G19	R30
I/O	P23	P29	E17	R31
I/O	P24	R31	E19	R33
GND	-	GND*	GND*	GND*
I/O	P25	R30	A19	T31
I/O	P26	R28	F18	T29
I/O	-	-	C19	T30
I/O	-	-	D20	T32
I/O	P27	R29	F20	U32
I/O	P28	T31	B20	U31
GND	P29	GND*	GND*	GND*
VCC	P30	VCC*	VCC*	VCC*
I/O	P31	T30	C21	U29
I/O	P32	T29	A21	U30
I/O	-	-	D22	U33
I/O	-	-	B22	V32
I/O	P33	U31	E23	V31
I/O	P34	U30	F22	V29

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
GND	-	GND*	GND*	GND*
I/O	P35	U28	C23	V30
I/O	P36	U29	F24	W33
I/O	-	V30	A23	W31
I/O	-	V29	E25	W30
I/O	-	V28	G23	W29
I/O	-	W31	B24	Y32
VCC	-	VCC*	VCC*	VCC*
GND	P37	GND*	GND*	GND*
I/O	-	W30	D24	Y31
I/O	-	W29	C25	Y30
I/O	-	W28	D28	AA32
I/O	-	Y31	A27	AA31
I/O	-	Y30	E29	AA30
I/O	-	Y29	C27	AB32
GND	-	GND*	GND*	GND*
I/O	P38	Y28	G25	AA29
I/O	P39	AA30	D26	AB31
VCC	P40	VCC*	VCC*	VCC*
I/O	P41	AA29	F26	AC31
I/O	P42	AB31	B28	AB29
I/O	P43	AB30	D30	AD32
I/O	P44	AB29	A29	AC30
GND	P45	GND*	GND*	GND*
I/O	-	AB28	C29	AD31
I/O	-	AC30	G27	AE33
I/O	P46	AC29	F30	AC29
I/O	P47	AC28	B30	AE32
I/O	-	-	E31	AD30
I/O	-	-	C31	AE31
GND	-	GND*	GND*	GND*
I/O	-	AD31	F28	AG33
I/O	-	AD30	D32	AH33
I/O	P48	AD29	B32	AE29
I/O	P49	AD28	G31	AG31
I/O	P50	AE30	A33	AF30
I/O	P51	AE29	C33	AH32
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AF31	B34	AJ32
I/O	-	AE28	A35	AF29
I/O	-	AF30	E33	AH31
I/O	-	AF29	D34	AG30
I/O	P52	AG31	D36	AK32
I/O	P53	AF28	B36	AJ31
GND	-	GND*	GND*	GND*
I/O	-	AG30	F34	AG29
I/O	-	AG29	D38	AL33
I/O	P54	AH31	C37	AH30
I/O	P55	AG28	G37	AK31
I/O	P56	AH30	B38	AJ30
I/O, GCK2	P57	AJ30	F38	AH29
O (M1)	P58	AH29	A39	AK30
GND	P59	GND*	GND*	GND*
I (M0)	P60	AH28	E35	AJ29
VCC	P61	VCC*	VCC*	VCC*
I (M2)	P62	AJ28	G33	AN32
I/O, GCK3	P63	AK29	J37	AJ28
I/O (HDC)	P64	AH27	G35	AK29
I/O	P65	AK28	K36	AL30
I/O	P66	AJ27	C39	AK28
I/O	P67	AL28	K38	AM31
I/O (LDC)	P68	AH26	C41	AJ27
GND	-	GND*	GND*	GND*
I/O	-	AK27	D40	AN31
I/O	-	AJ26	L37	AL29
I/O	-	AL27	H36	AK27
I/O	-	AH25	M36	AL28
I/O	-	AK26	J35	AJ26
I/O	-	AL26	E41	AM30

<b>XC4062XL Pad Name</b>	<b>HQ240</b>	<b>BG432</b>	<b>PG475</b>	<b>BG560</b>
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P69	AH24	F40	AM29
I/O	P70	AJ25	H38	AK26
I/O	P71	AK25	N37	AL27
I/O	P72	AJ24	L35	AJ25
I/O	-	AH23	R35	AN29
I/O	-	AK24	G41	AN28
GND	-	GND*	GND*	GND*
I/O	-	-	H40	AM26
I/O	-	-	P38	AK24
I/O	P73	AL24	J39	AL25
I/O	P74	AH22	R37	AJ23
I/O	-	AJ23	J41	AN26
I/O	-	AK23	K40	AL24
GND	P75	GND*	GND*	GND*
I/O	P76	AJ22	L39	AK23
I/O	P77	AK22	M38	AN25
I/O	P78	AL22	T36	AJ22
I/O	P79	AJ21	M40	AL23
VCC	P80	VCC*	VCC*	VCC*
I/O	P81	AH20	N39	AM24
I/O	P82	AK21	N41	AK22
GND	-	GND*	GND*	GND*
I/O	-	AJ20	P40	AK21
I/O	-	AH19	T38	AM22
I/O	-	AK20	U35	AJ20
I/O	-	AJ19	U37	AL21
I/O	-	AL20	R39	AN21
I/O	-	AH18	R41	AK20
GND	P83	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AK19	V36	AL20
I/O	-	AJ18	U39	AJ19
I/O	P84	AL19	V38	AM20
I/O	P85	AK18	V40	AK19
I/O	P86	AH17	W37	AL19
I/O	P87	AJ17	W35	AN19
GND	-	GND*	GND*	GND*
I/O	-	-	W41	AJ18
I/O	-	-	Y36	AK18
I/O	-	AK17	W39	AL18
I/O	-	AL17	AB36	AM18
I/O	P88	AJ16	Y40	AK17
I/O (INIT)	P89	AK16	Y38	AJ17
VCC	P90	VCC*	VCC*	VCC*
GND	P91	GND*	GND*	GND*
I/O	P92	AL16	AA39	AL17
I/O	P93	AH15	AB38	AM17
I/O	-	AL15	AB40	AN17
I/O	-	AJ15	AC37	AK16
I/O	-	-	AC39	AJ16
I/O	-	-	AC41	AL16
GND	-	GND*	GND*	GND*
I/O	P94	AK15	AD36	AM16
I/O	P95	AJ14	AC35	AL15
I/O	P96	AH14	AE37	AK15
I/O	P97	AK14	AD40	AJ15
I/O	-	AL13	AD38	AN15
I/O	-	AK13	AE39	AM14
VCC	-	VCC*	VCC*	VCC*
GND	P98	GND*	GND*	GND*
I/O	-	AJ13	AG41	AL14
I/O	-	AH13	AG39	AJ14
I/O	-	AL12	AG37	AJ14
I/O	-	AK12	AE35	AN13
I/O	-	AJ12	AH38	AM13
I/O	-	AK11	AF38	AL13
GND	-	GND*	GND*	GND*
I/O	P99	AH12	AF36	AK12

<b>XC4062XL Pad Name</b>	<b>HQ240</b>	<b>BG432</b>	<b>PG475</b>	<b>BG560</b>
I/O	P100	AJ11	AH40	AN11
VCC	P101	VCC*	VCC*	VCC*
I/O	P102	AL10	AJ41	AJ12
I/O	P103	AK10	AJ39	AL11
I/O	P104	AJ10	AJ37	AK11
I/O	P105	AK9	AG35	AM10
GND	P106	GND*	GND*	GND*
I/O	-	AL8	AK40	AL10
I/O	-	AH10	AK38	AJ11
I/O	P107	AJ9	AL37	AN9
I/O	P108	AK8	AL39	AK10
I/O	-	-	AM38	AM9
I/O	-	-	AM40	AL9
GND	-	GND*	GND*	GND*
I/O	-	AJ8	AN41	AN7
I/O	-	AH9	AM36	AJ9
I/O	P109	AK7	AK36	AL7
I/O	P110	AL6	AU41	AK8
I/O	P111	AJ7	AN39	AN6
I/O	P112	AH8	AP40	AM6
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	AK6	AR41	AJ8
I/O	-	AL5	AL35	AL6
I/O	P113	AH7	AV40	AK7
I/O	P114	AJ6	AN37	AM5
I/O	-	AK5	AT38	AM4
I/O	-	AL4	AP38	AJ7
GND	-	GND*	GND*	GND*
I/O	-	AH6	AT40	AL5
I/O	-	AJ5	AW39	AK6
I/O	P115	AK4	AP36	AN3
I/O	P116	AH5	AU37	AK5
I/O	P117	AK3	AR37	AJ6
I/O, GCK4	P118	AJ4	AU39	AL4
GND	P119	GND*	GND*	GND*
DONE	P120	AH4	AR35	AJ5
VCC	P121	VCC*	VCC*	VCC*
PROGRAM	P122	AH3	AN35	AM1
I/O (D7)	P123	AJ2	AU35	AH5
I/O, GCK5	P124	AG4	AV38	AJ4
I/O	P125	AG3	AT34	AK3
I/O	P126	AH2	BA39	AH4
I/O	-	AH1	AU33	AL1
I/O	-	AF4	AY38	AG5
GND	-	GND*	GND*	GND*
I/O	P127	AF3	AV36	AJ3
I/O	P128	AG2	AR31	AK2
I/O	-	AG1	AR33	AG4
I/O	-	AE4	AV32	AH3
I/O	-	AE3	BA37	AF5
I/O	-	AF2	AY36	AJ2
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O (D6)	P129	AF1	AV34	AJ1
I/O	P130	AD4	BA35	AF4
I/O	P131	AD3	AU31	AG3
I/O	P132	AE2	AY34	AE5
I/O	-	AD2	AT30	AH1
I/O	-	AC4	AW33	AF3
GND	-	GND*	GND*	GND*
I/O	-	-	BA33	AF1
I/O	-	-	AV30	AD4
I/O	P133	AC3	AY32	AE3
I/O	P134	AD1	AU29	AC5
I/O	-	AC2	AW31	AE1
I/O	-	AB4	BA31	AD3
GND	P135	GND*	GND*	GND*
I/O	P136	AB3	AR27	AC4
I/O	P137	AB2	AT28	AD2

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	P138	AB1	AY30	AB5
I/O	P139	AA3	AW29	AC3
VCC	P140	VCC*	VCC*	VCC*
I/O (D5)	P141	AA2	BA29	AA5
I/O (CS0)	P142	Y2	AY28	AB3
GND	P143	GND*	GND*	GND*
I/O	-	Y4	AR25	AB2
I/O	-	Y3	AV28	AA4
I/O	-	Y1	AW27	AA3
I/O	-	W1	AT26	Y5
I/O	-	W4	AV26	Y3
I/O	-	W3	BA27	Y2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O	-	W2	AW25	W5
I/O	-	V2	AV24	W4
I/O	-	V4	AU25	W3
I/O	-	V3	AR23	W1
I/O	P144	U1	AT24	V3
I/O	P145	U2	AY24	V5
GND	-	GND*	GND*	GND*
I/O	P146	U4	BA23	V4
I/O	P147	U3	AU23	V2
I/O	-	-	AW23	U2
I/O	-	-	AV20	U1
I/O (D4)	P148	T1	AY22	U5
I/O	P149	T2	AV22	U4
VCC	P150	VCC*	VCC*	VCC*
GND	P151	GND*	GND*	GND*
I/O (D3)	P152	T3	AW21	U3
I/O (RS)	P153	R1	BA21	T2
I/O	-	-	AU19	T3
I/O	-	-	AY20	T5
I/O	P154	R2	AU17	T4
I/O	P155	R4	AW19	R1
GND	-	GND*	GND*	GND*
I/O	P156	R3	BA19	R3
I/O	P157	P2	AT16	R4
I/O	-	P3	AR19	R5
I/O	-	P4	AV14	P2
I/O	-	N1	AY18	P3
I/O	-	N2	AV18	P4
VCC	-	VCC*	VCC*	VCC*
GND	P158	GND*	GND*	GND*
I/O	-	N3	AT18	N1
I/O	-	N4	AW17	P5
I/O	-	M1	AR15	N2
I/O	-	M2	BA15	N3
I/O	-	M3	AT14	N5
I/O	-	M4	AR17	M3
GND	-	GND*	GND*	GND*
I/O (D2)	P159	L2	AW15	M4
I/O	P160	L3	AV16	L1
VCC	P161	VCC*	VCC*	VCC*
I/O	P162	K1	AY14	K2
I/O	P163	K2	BA13	L4
I/O	P164	K3	AU13	J1
I/O	P165	K4	AW13	K3
GND	P166	GND*	GND*	GND*
I/O	-	J2	AY12	L5
I/O	-	J3	BA11	J2
I/O	P167	J4	AV12	K4
I/O	P168	H1	AT12	J3
I/O	-	-	AW11	H2
I/O	-	-	AY10	K5
GND	-	GND*	GND*	GND*
I/O	P169	H2	BA9	G1
I/O	P170	H3	AU11	F1
I/O	P171	H4	AW9	J5
I/O	P172	G2	AV10	G3

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O	-	G3	AY8	H4
I/O	-	F1	BA7	F2
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (D1)	P173	G4	AV8	F3
I/O (RCLK, RDY/BUSY)	P174	F2	AY6	G4
I/O	-	F3	AR11	D2
I/O	-	E1	AT8	E3
I/O	-	F4	AU9	G5
I/O	-	E2	AW5	C1
GND	-	GND*	GND*	GND*
I/O	-	E3	AY4	F4
I/O	-	D1	BA5	D3
I/O	P175	E4	AV4	B3
I/O	P176	D2	AR9	F5
I/O (D0, DIN)	P177	C2	AU5	E4
I/O, GCK6 (DOUT)	P178	D3	AV6	D4
CCLK	P179	D4	AR5	C4
VCC	P180	VCC*	VCC*	VCC*
O, TDO	P181	C4	AN7	E6
GND	P182	GND*	GND*	GND*
I/O (A0, WS)	P183	B3	AR7	D5
I/O, GCK7 (A1)	P184	D5	AW3	A2
I/O	P185	B4	AU3	D6
I/O	P186	C5	AW1	A3
I/O	-	A4	AP6	E7
I/O	-	D6	AV2	C5
GND	-	GND*	GND*	GND*
I/O	-	B5	AT4	B4
I/O	-	C6	AN5	D7
I/O (CS1, A2)	P187	A5	AU1	C6
I/O (A3)	P188	D7	AM6	E8
I/O	-	B6	AT2	B5
I/O	-	A6	AL7	A5
VCC	-	VCC*	VCC*	VCC*
GND	-	GND*	GND*	GND*
I/O	P189	D8	AR1	D8
I/O	P190	C7	AP2	C7
I/O	P191	B7	AM4	E9
I/O	P192	D9	AN3	A6
I/O	-	B8	AL5	B7
I/O	-	A8	AK6	D9
GND	-	GND*	GND*	GND*
I/O	-	-	AN1	D10
I/O	-	-	AJ5	C9
I/O	P193	D10	AM2	E11
I/O	P194	C9	AH4	A9
I/O	P195	B9	AL3	C10
I/O	-	C10	AK4	D11
GND	P196	GND*	GND*	GND*
I/O	P197	B10	AG7	B10
I/O	P198	A10	AG5	E12
I/O	P199	C11	AK2	C11
I/O	P200	D12	AJ3	B11
VCC	P201	VCC*	VCC*	VCC*
I/O	-	B11	AJ1	D12
I/O	-	C12	AF6	A11
GND	-	GND*	GND*	GND*
I/O	-	D13	AH2	C13
I/O	-	B12	AF4	E14
I/O	-	C13	AE7	A13
I/O	-	A12	AE5	D14
I/O	-	D14	AG3	C14
I/O	-	B13	AG1	B14
GND	-	GND*	GND*	GND*
VCC	-	VCC*	VCC*	VCC*
I/O (A4)	P202	C14	AD6	E15
I/O (A5)	P203	A13	AD4	D15
I/O	P205	B14	AE3	C15
I/O	P206	D15	AC5	A15

XC4062XL Pad Name	HQ240	BG432	PG475	BG560
I/O (A21)	P207	C15	AD2	C16
I/O (A20)	P208	B15	AC7	E16
GND	-	GND*	GND*	GND*
I/O	-	-	AC1	D16
I/O	-	-	AC3	B16
I/O	-	A15	AB6	B17
I/O	-	C16	AB2	C17
I/O (A6)	P209	B16	AB4	E17
I/O (A7)	P210	A16	AA3	D17
GND	P211	GND*	GND*	GND*

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

## Additional XC4062XL Package Pins

HQ240

GND Pins					
P204	P219	-	-	-	-

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Note: These pins may be Not Connected for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-

GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1

Not Connected Pins						
C8	-	-	-	-	-	-

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PG475

VCC Pins					
A37	B2	B16	B26	B40	D2
E21	F6	F36	G13	G29	N7
N35	T2	T40	AA1	AA5	AA37
AA41	AF2	AF40	AJ7	AJ35	AR13
AR29	AT6	AT22	AT36	AU21	AW37
AW41	AY2	AY16	AY26	AY40	BA3

GND Pins					
A3	C1	C7	G3	L1	P6
U1	A17	A25	A41	AA7	AE1
AH6	AL1	AR3	AW7	BA1	C35
E15	E27	F10	F32	G21	G39
L41	P36	U41	AA35	AE41	AH36
AL41	AR21	AR39	AT10	AT20	AT32
AU15	AU27	AW35	BA17	BA25	BA41
E37	E39	A31	J7	AP4	AU7

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BG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-

GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM11	AM19	AM25	AM28	AM33	AM7	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27

Not Connected Pins						
A1	A8	A23	A27	A28	A33	B8
B12	C8	C12	C22	C26	D13	D22
D25	E2	E10	E13	E21	E32	E33
H3	H5	H31	J4	K29	L3	L31
M2	M5	M30	N4	N30	N31	Y4
Y29	AA1	AA33	AB4	AB30	AC1	AC2
AC33	AD5	AD29	AE4	AE30	AF2	AF31
AF32	AG2	AJ10	AJ13	AJ21	AJ24	AK9
AK13	AK25	AL8	AL12	AL22	AL26	AM8
AM12	AM23	AM27	AN1	AN23	AN33	-

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## Pin Locations for XC4085XL Devices

XC4085XL Pad Name	BG432	BG560	PG559
VCC	VCC	VCC*	VCC*
I/O (A8)	D17	A17	AB6
I/O (A9)	A17	B18	AB4
I/O	C17	C18	AA7
I/O	B17	E18	AC1
I/O	-	D18	AA5
I/O	-	A19	AA3
GND	GND*	GND*	GND*
I/O (A19)	C18	C19	Y8
I/O (A18)	D18	D19	AB2
I/O	B18	E19	Y6

XC4085XL Pad Name	BG432	BG560	PG559
I/O	A19	B20	AA1
I/O (A10)	B19	C20	Y4
I/O (A11)	C19	D20	W7
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	D19	A21	W5
I/O	A20	E20	V6
I/O	B20	B21	V4
I/O	C20	C21	Y2
I/O	B21	D21	U3
I/O	D20	B22	U7
I/O	-	E21	V2

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	-	C22	U5
GND	GND*	GND*	GND*
I/O	-	D22	T4
I/O	-	A23	U1
I/O	C21	C23	R3
I/O	A22	E22	R5
VCC	VCC	VCC*	VCC*
I/O	B22	B24	T8
I/O	C22	D23	T2
I/O	B23	C24	P4
I/O	A24	A25	R7
GND	GND*	GND*	GND*
I/O	D22	E23	N3
I/O	C23	B25	R1
I/O	B24	D24	N5
I/O	C24	C25	P2
I/O	-	B26	M4
I/O	-	E24	L1
I/O	-	C26	L3
I/O	-	D25	P8
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	-	A27	N7
I/O	-	A28	K2
I/O	D23	E25	M6
I/O	B25	C27	J1
I/O	A26	D26	L5
I/O	C25	B28	H2
I/O (A12)	D24	B29	K4
I/O (A13)	B26	E26	J3
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	A27	C28	L7
I/O	D25	D27	J5
I/O	C26	B30	G1
I/O	B27	C29	H4
I/O	A28	E27	F2
I/O	D26	A31	G5
GND	GND*	GND*	GND*
I/O	C27	D28	H6
I/O	B28	C30	K8
I/O	D27	D29	D2
I/O	B29	E28	J7
I/O (A14)	C28	D30	F4
I/O, GCK8 (A15)	D28	E29	E3
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O, GCK1 (A16)	D29	B33	C1
I/O (A17)	C30	F29	C3
I/O	E28	E30	F6
I/O	E29	D31	A3
I/O (TDI)	D30	F30	H8
I/O (TCK)	D31	C33	D4
GND	GND*	GND*	GND*
I/O	F28	G29	D6
I/O	F29	E31	C5
I/O	E30	D32	E7
I/O	E31	G30	B4
I/O	G28	F31	H10
I/O	G29	H29	G9

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	-	E32	F8
I/O	-	E33	D8
I/O	F30	H30	B6
I/O	F31	G31	E9
I/O	H28	J29	A7
I/O	H29	F33	G11
I/O	G30	G32	H14
I/O	H30	J30	F12
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	-	H31	G13
I/O	-	K29	E11
I/O	-	H32	B8
I/O	-	J31	D10
I/O	J28	K30	A9
I/O	J29	H33	G15
I/O	H31	L29	B10
I/O	J30	K31	H16
GND	GND*	GND*	GND*
I/O	K28	L30	C9
I/O	K29	K32	E13
I/O (TMS)	K30	J33	A11
I/O	K31	M29	D12
VCC	VCC*	VCC*	VCC*
I/O	-	L31	C11
I/O	-	M30	B14
I/O	L29	L32	G17
I/O	L30	M31	E15
GND	GND*	GND*	GND*
I/O	M30	N29	D14
I/O	M28	L33	A15
I/O	-	N30	C13
I/O	-	N31	B16
I/O	M29	M32	E17
I/O	M31	P29	F18
I/O	N31	P30	A17
I/O	N28	N33	G19
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	N29	P31	D16
I/O	N30	P32	C15
I/O	P30	R29	B18
I/O	P28	R30	H20
I/O	P29	R31	B20
I/O	R31	R33	E19
GND	GND*	GND*	GND*
I/O	R30	T31	D18
I/O	R28	T29	F20
I/O	-	T30	G21
I/O	-	T32	C17
I/O	R29	U32	D20
I/O	T31	U31	E21
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	T30	U29	C21
I/O	T29	U30	F22
I/O	-	U33	A21
I/O	-	V32	D22
I/O	U31	V31	B22

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	U30	V29	G23
GND	GND*	GND*	GND*
I/O	U28	V30	E23
I/O	U29	W33	C23
I/O	V30	W31	A23
I/O	V29	W30	D24
I/O	V28	W29	B24
I/O	W31	Y32	H24
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	W30	Y31	F24
I/O	W29	Y30	E25
I/O	-	AA33	B26
I/O	-	Y29	D26
I/O	W28	AA32	A27
I/O	Y31	AA31	G25
I/O	Y30	AA30	B28
I/O	Y29	AB32	C27
GND	GND*	GND*	GND*
I/O	Y28	AA29	F26
I/O	AA30	AB31	E27
I/O	-	AB30	A29
I/O	-	AC33	D28
VCC	VCC*	VCC*	VCC*
I/O	AA29	AC31	G27
I/O	AB31	AB29	B30
I/O	AB30	AD32	C29
I/O	AB29	AC30	E29
GND	GND*	GND*	GND*
I/O	AB28	AD31	D30
I/O	AC30	AE33	A33
I/O	AC29	AC29	C31
I/O	AC28	AE32	B34
I/O	-	AD30	H28
I/O	-	AE31	A35
I/O	-	AF32	G29
I/O	-	AD29	E31
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	-	AF31	D32
I/O	-	AE30	C35
I/O	AD31	AG33	C33
I/O	AD30	AH33	B36
I/O	AD29	AE29	H30
I/O	AD28	AG31	A37
I/O	AE30	AF30	G31
I/O	AE29	AH32	F32
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	AF31	AJ32	E33
I/O	AE28	AF29	D34
I/O	AF30	AH31	B38
I/O	AF29	AG30	G33
I/O	AG31	AK32	A41
I/O	AF28	AJ31	E35
GND	GND*	GND*	GND*
I/O	AG30	AG29	D36
I/O	AG29	AL33	F36
I/O	AH31	AH30	G35
I/O	AG28	AK31	H34
I/O	AH30	AJ30	B40

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O, GCK2	AJ30	AH29	E37
O (M1)	AH29	AK30	D38
GND	GND*	GND*	GND*
I (M0)	AH28	AJ29	C39
VCC	VCC*	VCC*	VCC*
I (M2)	AJ28	AN32	H36
I/O, GCK3	AK29	AJ28	F38
I/O (HDC)	AH27	AK29	C41
I/O	AK28	AL30	D40
I/O	AJ27	AK28	B42
I/O	AL28	AM31	J37
I/O (LDC)	AH26	AJ27	K36
GND	GND*	GND*	GND*
I/O	AK27	AN31	H38
I/O	AJ26	AL29	D42
I/O	AL27	AK27	G39
I/O	AH25	AL28	C43
I/O	AK26	AJ26	F40
I/O	AL26	AM30	E41
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	AH24	AM29	L37
I/O	AJ25	AK26	J39
I/O	AK25	AL27	F42
I/O	AJ24	AJ25	H40
I/O	AH23	AN29	G43
I/O	AK24	AN28	J41
I/O	-	AK25	H42
I/O	-	AL26	N37
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	-	AJ24	P36
I/O	-	AM27	M38
I/O	-	AM26	J43
I/O	-	AK24	L39
I/O	AL24	AL25	K42
I/O	AH22	AJ23	K40
I/O	AJ23	AN26	L43
I/O	AK23	AL24	L41
GND	GND*	GND*	GND*
I/O	AJ22	AK23	R37
I/O	AK22	AN25	P42
I/O	AL22	AJ22	T36
I/O	AJ21	AL23	N39
VCC	VCC*	VCC*	VCC*
I/O	AH20	AM24	M40
I/O	AK21	AK22	R43
I/O	-	AM23	N41
I/O	-	AJ21	R39
GND	GND*	GND*	GND*
I/O	-	AL22	U37
I/O	-	AN23	T42
I/O	AJ20	AK21	P40
I/O	AH19	AM22	U43
I/O	AK20	AJ20	R41
I/O	AJ19	AL21	V42
I/O	AL20	AN21	U39
I/O	AH18	AK20	V38
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	AK19	AL20	W37

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	AJ18	AJ19	T40
I/O	AL19	AM20	Y42
I/O	AK18	AK19	U41
I/O	AH17	AL19	Y36
I/O	AJ17	AN19	V40
GND	GND*	GND*	GND*
I/O	-	AJ18	W39
I/O	-	AK18	AA43
I/O	AK17	AL18	Y38
I/O	AL17	AM18	Y40
I/O	AJ16	AK17	AA37
I/O (INIT)	AK16	AJ17	AA39
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	AL16	AL17	AA41
I/O	AH15	AM17	AB38
I/O	AL15	AN17	AB42
I/O	AJ15	AK16	AB40
I/O	-	AJ16	AC37
I/O	-	AL16	AC39
GND	GND*	GND*	GND*
I/O	AK15	AM16	AD36
I/O	AJ14	AL15	AC41
I/O	AH14	AK15	AD38
I/O	AK14	AJ15	AC43
I/O	AL13	AN15	AD40
I/O	AK13	AM14	AE39
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	AJ13	AL14	AE37
I/O	AH13	AK14	AF40
I/O	AL12	AJ14	AD42
I/O	AK12	AN13	AF42
I/O	AJ12	AM13	AF38
I/O	AK11	AL13	AG39
I/O	-	AK13	AG43
I/O	-	AJ13	AG37
GND	GND*	GND*	GND*
I/O	-	AM12	AH40
I/O	-	AL12	AJ41
I/O	AH12	AK12	AG41
I/O	AJ11	AN11	AK40
VCC	VCC*	VCC*	VCC*
I/O	AL10	AJ12	AJ39
I/O	AK10	AL11	AH42
I/O	AJ10	AK11	AH36
I/O	AK9	AM10	AL39
GND	GND*	GND*	GND*
I/O	AL8	AL10	AJ37
I/O	AH10	AJ11	AJ43
I/O	AJ9	AN9	AM40
I/O	AK8	AK10	AK42
I/O	-	AM9	AN41
I/O	-	AL9	AL41
I/O	-	AJ10	AR41
I/O	-	AM8	AK36
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	-	AK9	AL37
I/O	-	AL8	AN43
I/O	AJ8	AN7	AM38

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	AH9	AJ9	AP42
I/O	AK7	AL7	AN39
I/O	AL6	AK8	AR43
I/O	AJ7	AN6	AP40
I/O	AH8	AM6	AT40
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	AK6	AJ8	AN37
I/O	AL5	AL6	AR39
I/O	AH7	AK7	AT42
I/O	AJ6	AM5	BA43
I/O	AK5	AM4	AU43
I/O	AL4	AJ7	AU39
GND	GND*	GND*	GND*
I/O	AH6	AL5	AT38
I/O	AJ5	AK6	AP36
I/O	AK4	AN3	AR37
I/O	AH5	AK5	AV42
I/O	AK3	AJ6	AV40
I/O, GCK4	AJ4	AL4	AW41
GND	GND*	GND*	GND*
DONE	AH4	AJ5	AY42
VCC	VCC*	VCC*	VCC*
PROGRAM	AH3	AM1	BB42
I/O (D7)	AJ2	AH5	BC41
I/O, GCK5	AG4	AJ4	AV38
I/O	AG3	AK3	BA39
I/O	AH2	AH4	AT36
I/O	AH1	AL1	BB40
I/O	AF4	AG5	AY40
GND	GND*	GND*	GND*
I/O	AF3	AJ3	BA41
I/O	AG2	AK2	BB38
I/O	AG1	AG4	AY38
I/O	AE4	AH3	BC37
I/O	AE3	AF5	AW37
I/O	AF2	AJ2	AT34
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O (D6)	AF1	AJ1	AU35
I/O	AD4	AF4	AV36
I/O	AD3	AG3	BB36
I/O	AE2	AE5	AY36
I/O	AD2	AH1	BC35
I/O	AC4	AF3	AW35
I/O	-	AE4	AU33
I/O	-	AG2	AT30
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	-	AD5	AV32
I/O	-	AF2	AU31
I/O	-	AF1	AW33
I/O	-	AD4	BB34
I/O	AC3	AE3	AY34
I/O	AD1	AC5	BC33
I/O	AC2	AE1	AU29
I/O	AB4	AD3	AT28
GND	GND*	GND*	GND*
I/O	AB3	AC4	BA35
I/O	AB2	AD2	BB30
I/O	AB1	AB5	AW31

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	AA3	AC3	AY32
VCC	VCC*	VCC*	VCC*
I/O	-	AB4	BA33
I/O	-	AC1	AU27
I/O (D5)	AA2	AA5	BC29
I/O (CS0)	Y2	AB3	AW29
GND	GND*	GND*	GND*
I/O	Y4	AB2	AY30
I/O	Y3	AA4	BA31
I/O	Y1	AA3	BB28
I/O	W1	Y5	AW27
I/O	-	AA1	BC27
I/O	-	Y4	AV26
I/O	W4	Y3	AU25
I/O	W3	Y2	AY28
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	W2	W5	BA29
I/O	V2	W4	AT24
I/O	V4	W3	BB26
I/O	V3	W1	AW25
I/O	U1	V3	BB24
I/O	U2	V5	AY26
GND	GND*	GND*	GND*
I/O	U4	V4	AV24
I/O	U3	V2	AU23
I/O	-	U2	BA27
I/O	-	U1	BC23
I/O (D4)	T1	U5	AY24
I/O	T2	U4	AW23
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O (D3)	T3	U3	BA23
I/O (RS)	R1	T2	AV22
I/O	-	T3	AY22
I/O	-	T5	BB22
I/O	R2	T4	AU21
I/O	R4	R1	AW21
GND	GND*	GND*	GND*
I/O	R3	R3	BA21
I/O	P2	R4	BC21
I/O	P3	R5	AY20
I/O	P4	P2	BB20
I/O	N1	P3	AT20
I/O	N2	P4	AV20
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	N3	N1	AW19
I/O	N4	P5	AY18
I/O	M1	N2	BB18
I/O	M2	N3	AU19
I/O	-	N4	BC17
I/O	-	M2	BA17
I/O	M3	N5	AV18
I/O	M4	M3	AW17
GND	GND*	GND*	GND*
I/O (D2)	L2	M4	AY16
I/O	L3	L1	BB16
I/O	-	L3	AU17
I/O	-	M5	BA15
VCC	VCC*	VCC*	VCC*

<b>XC4085XL Pad Name</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
I/O	K1	K2	AW15
I/O	K2	L4	BC15
I/O	K3	J1	AY14
I/O	K4	K3	BA13
GND	GND*	GND*	GND*
I/O	J2	L5	AT16
I/O	J3	J2	BB14
I/O	J4	K4	AU15
I/O	H1	J3	BC11
I/O	-	H2	AW13
I/O	-	K5	BB10
I/O	-	H3	AY12
I/O	-	J4	BA11
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O	H2	G1	AT14
I/O	H3	F1	AU13
I/O	H4	J5	AV12
I/O	G2	G3	BC9
I/O	G3	H4	AW11
I/O	F1	F2	BB8
I/O	-	E2	AY10
I/O	-	H5	AU11
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O (D1)	G4	F3	BA9
I/O (RCLK RDY/BUSY)	F2	G4	AW9
I/O	F3	D2	BC7
I/O	E1	E3	AY8
I/O	F4	G5	AV8
I/O	E2	C1	AT10
GND	GND*	GND*	GND*
I/O	E3	F4	AU9
I/O	D1	D3	BB6
I/O	E4	B3	AW7
I/O	D2	F5	BC3
I/O (D0, DIN)	C2	E4	AY6
I/O, GCK6 (DOUT)	D3	D4	BB4
CCLK	D4	C4	BA5
VCC	VCC*	VCC*	VCC*
O, TDO	C4	E6	BA3
GND	GND*	GND*	GND*
I/O (A0, WS)	B3	D5	AT8
I/O, GCK7 (A1)	D5	A2	AV6
I/O	B4	D6	BB2
I/O	C5	A3	AY4
I/O	A4	E7	AR7
I/O	D6	C5	AP8
GND	GND*	GND*	GND*
I/O	B5	B4	AT6
I/O	C6	D7	AY2
I/O (CS1, A2)	A5	C6	AU5
I/O (A3)	D7	E8	BA1
I/O	B6	B5	AV4
I/O	A6	A5	AW3
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	D8	D8	AN7
I/O	C7	C7	AR5

XC4085XL Pad Name	BG432	BG560	PG559
I/O	B7	E9	AV2
I/O	D9	A6	AT4
I/O	B8	B7	AU1
I/O	A8	D9	AR3
I/O	-	C8	AT2
I/O	-	E10	AL7
VCC	VCC*	VCC*	VCC*
GND	GND*	GND*	GND*
I/O	-	B8	AK8
I/O	-	A8	AM6
I/O	-	D10	AN5
I/O	-	C9	AR1
I/O	D10	E11	AP4
I/O	C9	A9	AN3
I/O	B9	C10	AP2
I/O	C10	D11	AJ7
GND	GND*	GND*	GND*
I/O	B10	B10	AH8
I/O	A10	E12	AL5
I/O	C11	C11	AN1
I/O	D12	B11	AM4
VCC	VCC*	VCC*	VCC*
I/O	B11	D12	AL3
I/O	C12	A11	AJ5
I/O	-	E13	AK2
I/O	-	C12	AG7
GND	GND*	GND*	GND*
I/O	-	B12	AK4
I/O	-	D13	AJ3
I/O	D13	C13	AG5
I/O	B12	E14	AJ1
I/O	C13	A13	AF6
I/O	A12	D14	AH2
I/O	D14	C14	AE7
I/O	B13	B14	AH4
GND	GND*	GND*	GND*
VCC	VCC*	VCC*	VCC*
I/O (A4)	C14	E15	AG3
I/O (A5)	A13	D15	AD8
I/O	B14	C15	AG1
I/O	D15	A15	AF4
I/O (A21)	C15	C16	AE5
I/O (A20)	B15	E16	AD6
GND	GND*	GND*	GND*
I/O	-	D16	AD4
I/O	-	B16	AF2
I/O	A15	B17	AC7
I/O	C16	C17	AD2
I/O (A6)	B16	E17	AC5
I/O (A7)	A16	D17	AC3
GND	GND*	GND*	GND*

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\*Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

## Additional XC4085XL Package Pins

### BG560

VCC Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM11	AM19	AM25	AM28	AM33	AM7	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
Not Connected Pins						
A1	A33	AC2	AN1	AN33	-	-

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**PG559**

VCC Pins						
A13	A31	A43	B2	C7	C19	C25
C37	F14	F30	G3	G7	G37	G41
H12	H18	H26	H32	M8	M36	N1
N43	P6	P38	V8	V36	W3	W41
AE3	AE41	AF8	AF36	AK6	AK38	AL1
AL43	AM8	AM36	AT12	AT18	AT26	AT32
AU3	AU7	AU37	AU41	AV14	AV30	BA7
BA19	BA25	BA37	BC1	BC13	BC31	BC43
GND Pins						
A5	A19	A25	A39	B12	B32	E1
E5	E39	E43	F10	F16	F28	F34
H22	K6	K38	M2	M42	T6	T38
W1	W43	AB8	AB36	AE1	AE43	AH6
AH38	AM2	AM42	AP6	AP38	AT22	AV10
AV16	AV28	AV34	AW1	AW5	AW39	AW43
BB12	BB32	BC5	BC19	BC25	BC39	-

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**BG432**

VCC Pins							
A1	A11	A21	A31	D11	D21	L1	
L4	L28	L31	AA1	AA4	AA28	AA31	
AH11	AH21	AL1	AL11	AL21	AL31	C3	
C29	AJ3	AJ29					
GND Pins							
A2	A3	A7	A9	A14	A18	A23	
A25	A29	A30	B1	B2	B30	B31	
C1	C31	D16	G1	G31	J1	J31	
P1	P31	T4	T28	V1	V31	AC1	
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1	
AK2	AK30	AK31	AL2	AL3	AL7	AL9	
AL14	AL18	AL23	AL25	AL29	AL30		
Not Connected Pins							
C8							

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## Product Availability

Table 25 - Table 27 show the planned packages and speed grades for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at <http://www.xilinx.com> for the latest revision of the specifications.

**Table 25: Component Availability Chart for XC4000XL FPGAs**

		PINS	84	Plast. PLCC	100	Plast. PQFP	100	Plast. VQFP	144	Plast. TQFP	144	High-Perf. TQFP	160	Plast. PQFP	160	Plast. PQFP	176	Plast. TQFP	176	High-Perf. TQFP	208	Plast. PQFP	208	Plast. PQFP	240	Plast. PQFP	240	Plast. BGA	256	Plast. BGA	299	Ceram. PGA	304	Plast. BGA	352	Ceram. PGA	411	Plast. BGA	432	Ceram. PGA	475	Ceram. PGA	559	Ceram. PGA	560	Plast. BGA
		TYPE	PC84	PQ100	VQ100	TQ144		HT144		HQ160		PQ160		TQ176		HT176		HQ208		PQ208		HQ240		PQ240		BG256		PG299		HQ304		BG352		PG411		BG432		PG475		PG559		BG560				
		CODE																																												
XC4005XL	-3	C I	C I	C I	C I				C I				C				C				C I				C				C				C													
	-2	C	C	C	C				C				C				C				C				C				C				C													
	-1	C	C	C	C				C				C				C				C				C				C				C													
XC4010XL	-3	C I	C I	C I				C I	C I			C I				C I				C I				C I				C				C														
	-2	C	C	C				C	C			C				C				C				C				C				C														
	-1	C	C	C				C	C			C				C				C				C				C				C														
XC4013XL	-3			C I			C I		C I		C I		C		C		C		C I		C I		C I		C I		C I		C I		C I		C I		C I											
	-2			C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C									
	-1			C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C									
XC4020XL	-3			C I			C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I											
	-2			C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C									
	-1			C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C									
XC4028XL	-3				C I					C I			C I			C I			C I		C I		C I		C I		C I		C I		C I		C I		C I		C I									
	-2				C				C			C			C			C		C		C		C		C		C		C		C		C		C		C								
	-1				C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C								
XC4036XL	-3				C			C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I										
	-2				C I			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C								
	-1				C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C								
XC4044XL	-3				C I			C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I		C I										
	-2				C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C								
	-1				C			C		C		C		C		C		C		C		C		C		C		C		C		C		C		C		C								
XC4052XL	-3																			C I																				C I						
	-2																			C																			C							
	-1																			C																			C							
XC4062XL	-3																			C I																			C I							
	-2																			C																			C							
	-1																			C																			C							
XC4085XL	-3																																							C I						
	-2																																						C							
	-1																																						C							

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C = Commercial T<sub>J</sub> = 0° to +85°CI= Industrial T<sub>J</sub> = -40°C to +100°C

Table 26: Component Availability Chart for XC4000E FPGAs

PINS TYPE CODE		84	100	100	120	144	156	160	191	208	208	223	225	240	240	299	304
		Plast. PLCC	Plast. PQFP	Plast. VQFP	Ceram. PGA	Plast. TQFP	Ceram. PGA	Plast. PQFP	Ceram. PGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	High-Perf. QF
		PC84	PQ100	VQ100	PG120	TQ144	PG156	PQ160	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304
XC4003E	-4	CI	CI	CI	CI												
	-3	C	C	C	C												
	-2	C	C	C	C												
	-1	C	C	C	C												
XC4005E	-4	CI	CI			CI	CI	CI			CI						
	-3	C	C			C	C	C			C						
	-2	C	C			C	C	C			C						
	-1	C	C			C	C	C			C						
XC4006E	-4	CI				CI	CI	CI			CI						
	-3	C				C	C	C			C						
	-2	C				C	C	C			C						
	-1	C				C	C	C			C						
XC4008E	-4	CI						CI	CI		CI						
	-3	C						C	C		C						
	-2	C						C	C		C						
	-1	C						C	C		C						
XC4010E	-4	CI						CI	CI	CI	CI						
	-3	C						C	C	C	C						
	-2	C						C	C	C	C						
	-1	C						C	C	C	C						
XC4013E	-4							CI	CI	CI	CI	CI	CI	CI	CI	CI	CI
	-3							C	C	C	C	C	C	C	C	C	C
	-2							C	C	C	C	C	C	C	C	C	C
	-1							C	C	C	C	C	C	C	C	C	C
XC4020E	-4									CI	CI	CI	CI	CI	CI	CI	CI
	-3									C	C	C	C	C	C	C	C
	-2									C	C	C	C	C	C	C	C
	-1									C	C	C	C	C	C	C	C
XC4025E	-4											CI	CI	CI	CI	CI	CI
	-3											C	C	C	C	C	C
	-2											C	C	C	C	C	C

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C = Commercial T<sub>J</sub> = 0° to +85°CI= Industrial T<sub>J</sub> = -40°C to +100°C

Table 27: Component Availability Chart for XC4000EX FPGAs

PINS TYPE CODE		208	240	299	304	352	411	432
		High-Perf. QFP	High-Perf. QFP	Ceram. PGA	High-Perf. QFP	Plast. BGA	Ceram. PGA	Plast. BGA
		HQ208	HQ240	PG299	HQ304	BG352	PG411	BG432
XC4028EX	-3	CI	CI	CI	CI	CI		
	-2	C	C	C	C	C		
	-1	C	C	C	C	C		
XC4036EX	-3				CI		CI	CI
	-2				C		C	C
	-1				C		C	C

8/4/97

C = Commercial T<sub>J</sub> = 0° to +85°CI= Industrial T<sub>J</sub> = -40°C to +100°C

## User I/O Per Package

Table 28 - Table 30 show the number of user I/Os available in each package for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at <http://www.xilinx.com> for the latest revision of the specifications.

**Table 28: User I/O Chart for XC4000XL FPGAs**

Device	Max I/O	Package Type																					
		PC84	PQ100	VQ100	TQ144	HT144	HQ160	PQ160	TQ176	HT176	HQ208	PQ208	HQ240	PQ240	BG256	PQ299	HQ304	BG352	PG411	BG432	PG475	PG559	BG560
XC4005XL	112	61	77	77	112			112			112												
XC4010XL	160	61	77		113			129	145		160			160									
XC4013XL	192				113		129		145		160		192	192									
XC4020XL	224				113		129		145		160		193	205									
XC4028XL	256					129				160		193		205	256	256	256						
XC4036XL	288					129				160		193				256	288	288	288				
XC4044XL	320					129				160		193				256	289	320	320				
XC4052XL	352										193				256	352	352					352	
XC4062XL	384										193				256		352	384				384	
XC4085XL	448																					448	448
XC40125XV	448																					448	432

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**Table 29: User I/O Chart for XC4000E FPGAs**

Device	Max I/O	Package Type															
		PC84	PQ100	VQ100	PG120	TQ144	PG156	PQ160	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304
XC4003E	80	61	77	77	80												
XC4005E	112	61	77			112	112	112			112						
XC4006E	128	61				113	125	128			128						
XC4008E	144	61						129	144		144						
XC4010E	160	61						129	160	160	160		160				
XC4013E	192							129		160	160	192	192	192	192		
XC4020E	224									160		192		193			
XC4025E	256										192		193		256	256	

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**Table 30: User I/O Chart for XC4000EX FPGAs**

Device	Max I/O	Package Type							
		HQ208	HQ240	PG299	HQ304	BG352	PG411	BG432	
XC4028EX	256	160	193	256	256	256			
XC4036EX	288		193		256	288	288	288	

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## Ordering Information

**Example:** **XC4013E-3HQ240C**

Device Type

Speed Grade

-6

-5

-4

-3

-2

-1

Package Type

Temperature Range

C = Commercial ( $T_J = 0$  to  $+85^\circ\text{C}$ )

I = Industrial ( $T_J = -40$  to  $+100^\circ\text{C}$ )

M = Military ( $T_C = -55$  to  $+125^\circ\text{C}$ )

Number of Pins

PC = Plastic Lead Chip Carrier

PQ = Plastic Quad Flat Pack

VQ = Very Thin Quad Flat Pack

TQ = Thin Quad Flat Pack

BG = Ball Grid Array

PG = Ceramic Pin Grid Array

HQ = High Heat Dissipation Quad Flat Pack

MQ = Metal Quad Flat Pack

CB = Top Brazed Ceramic Quad Flat Pack

X9020

**Table 31: Revisions**

Version	Description
March 30, 1998 (1.5)	Updated XC4000XL timing and added XC4002XL



# XC4000XLA/XV Field Programmable Gate Arrays

September 16, 1998 (Version 0.1)

Advance Product Specification

## XC4000XLA/XV Family FPGAs

**Note:** XC4000XLA devices are improved versions of XC4000XL devices. The XC4000XV devices have the same features as XLA devices, incorporate additional interconnect resources and extend gate capacity to 500,000 system gates. The XC4000XV devices require a separate 2.5V power supply for internal logic but maintain 5V I/O compatibility via a separate 3.3V I/O power supply. For a general description of the architecture of the XC4000XLA/XV devices, please see the XC4000X Description, v1.4 (11/97) on Xilinx WEBSITE at: <http://www.xilinx.com>.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Flexible function generators and abundant flip-flops
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- Flexible array architecture
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - Unlimited reprogrammability
- Readback capability
  - Program verification and internal node observability

Table 1: XC4000XLA Series Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Required Configuration Bits
XC4013XLA	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	393,632
XC4020XLA	1,862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224	521,880
XC4028XLA	2,432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256	668,184
XC4036XLA	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	832,528
XC4044XLA	3,800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320	1,014,928
XC4052XLA	4,598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352	1,215,368
XC4062XLA	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	1,433,864
XC4085XLA	7,448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448	1,924,992
XC40110XV	9,728	110,000	131,072	75,000 - 235,000	64 x 64	4,096	9,216	448	2,686,136
XC40150XV	12,312	150,000	165,888	100,000 - 300,000	72 x 72	5,184	11,520	448	3,373,448
XC40200XV	16,758	200,000	225,792	130,000 - 400,000	84 x 84	7,056	15,456	448	4,551,056
XC40250XV	20,102	250,000	270,848	180,000 - 500,000	92 x 92	8,464	18,400	448	5,433,888

\* Maximum values of gate range assume 20-30% of CLBs used as RAM

## Xilinx SRAM XC4000 Series FPGAs

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

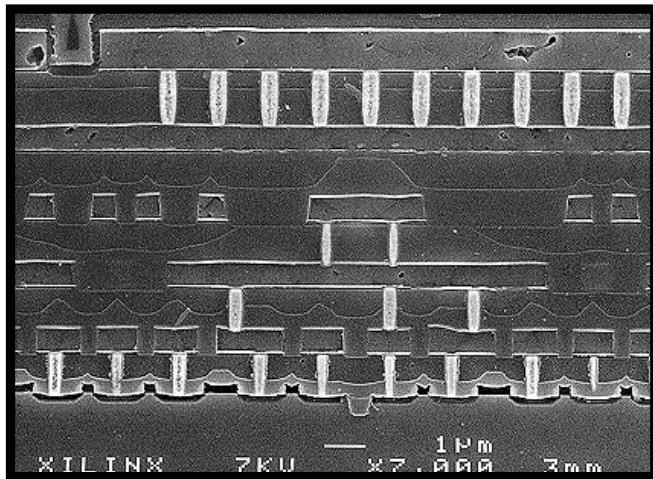


Figure 1. Cross section of Xilinx 0.25 micron, 5 layer metal XC4000XV FPGA. Visible features are five layers of metalization, tungsten plug vias and trench isolation. The small gaps above the lowest layer are 0.25 micron polysilicon MOSFET gates. The excellent planarity of each metal layer is due to the use of "chemical-mechanical polishing" or CMP. In effect each layer is ground flat before a new layer is added.

## XC4000XLA/XV FPGAs

XC4000XLA/XV FPGAs use 5 layer metal silicon technology to improve performance while reducing device cost and power. In addition, IOB enhancements provide full PCI compliance and the JTAG functionality is expanded.

## XC4000XV FPGAs

XC4000XV FPGAs incorporate all the features of the XLA devices but require a separate 2.5V power supply for internal logic. I/O pads are still driven from a 3.3V power supply. The 2.5V logic supply is named VCCINT and the 3.3 V IO supply is named VCCIO.

The XV devices also incorporate additional routing resources in the form of 8 octal-length segmented routing channels vertically and horizontally per row and column.

## Differences between the XC4000XLA/XV and XC4000XL FPGAs

The XC4000XLA/XV families of FPGAs are logically identical to XC4000EX and XC4000XL FPGAs, however I/O, configuration logic, JTAG functionality, and performance have been enhanced. In addition, they deliver:

- **Improved Performance**

XLA/XV devices benefit from advance processing technology and a reduction in interconnect capacitance which improves performance over XL devices by more than 30%.

- **Lower Power**

XLA/XV devices have reduced power requirements compared to equivalent XL devices.

- **Shorter routing delays**

The smaller die of XLA/XV devices directly reduces clock delays and the delay of high-fanout signals. The reduction in clock delay allows improved pin-to-pin I/O specifications.

- **Lower Cost**

XLA/XV device cost is directly related to the die size and has been reduced significantly from that of equivalent XL devices.

- **Express mode configuration**

Express mode configuration is available on the XLA and XV devices.

## IOB Enhancements

- **12/24 mA Output Drive**

The XLA/XV family of FPGAs allow individual IOBs to be configured as high drive outputs. Each output can be configured to have 24 mA drive strength as opposed to the standard default strength of 12 mA.

- **VCC Clamping Diode**

XLA and XV FPGAs have an optional clamping diode connected from each output to VCC (VCCIO for XV). When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. VCC clamping is a global option affecting all I/O pins. If enabled, TTL I/O compatibility is maintained, but full 5.0 Volt I/O tolerance is sacrificed.

- **Enhanced ESD protection**

An improved ESD structure allows XV devices to safely pass the stringent 5V PCI (4.2.1.3) ringing test. This test applies an 11V pulse to each IOB for 11 ns via a 55 ohm resistor.

- **Full 3.3V and 5.0V PCI compliance**

The addition of 12/24 mA drive, optional 3.3V clamping and improved ESD provides full compliance with either 3.3V or 5.0V PCI specifications.

- Three-State Register**

XC4000XLA/XV devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

- FastCLK clock buffers**

The XLA/XV devices incorporate FastCLK clock buffers. Two FastCLK buffers are available on each of the right and left edges of the die. Each FastCLK buffer can provide a fast clock signal (typically < 1.5 ns clock delay) to all the IOBs within the IOB octant containing the buffer. The FastCLK buffers can be instantiated by use of the BUFCCLK symbols. (In addition to FastCLK buffers, BUFGEs #1,#2,#5,#6 can also provide fast clock signals (typically < 1.5 ns clock delay) to IOBs on the top and bottom of the die.)

## XLA, XV Power Requirements

XC4000XLA devices require 40% less power per CLB than equivalent XL devices. XC4000XV devices require 42% less power per CLB than equivalent XLA devices and 65% less power than XL devices. The representative K-Factor for the following families can be found in Table 2. The K-Factor predicts device current for typical user designs and is based on filling the FPGA with active 16-Bit counters and measuring the device current at 1 MHz. This technique is described in XBRF14 "A simple method of estimating Power in XC4000XL/EX/E FPGAs". To predict device power (P) using the K-Factor use the following formula:

$$P = V * K * N * F; \text{ where:}$$

P = Device Power

V = Power supply voltage

K = the Device K-Factor

N = number of active registers

F = Frequency in MHz

**Table 2: K-Factor and relative power.**

FPGA Family	K-Factor	Power Relative To XL	Power Relative To XLA
XC4000XL	28	1.00	1.65
XC4000XLA	17	0.60	1.00
XC4000XV	13	0.35	0.58

## XLA, XV Logic Performance

XC4000XLA/XV devices feature 30% faster device speed than XL devices, and consistent performance is achieved across all family members. Table 3 illustrates the performance of the XLA devices. For details regarding the implementation of these benchmarks refer to XBRF15 "Speed Metrics for High Performance FPGAs".

**Table 3: XLA/XV Estimated Benchmark Performance**

Register - Register Benchmarks	Size	Maximum Frequency
Adder	8-Bit	172 MHz
	16-Bit	144 MHz
	32-Bit	108 MHz
2 Cascaded Adders	16-Bit	94 MHz
4 Cascaded Adders	16-Bit	57 MHz
Cascaded 4LUTs	1 Level	314 MHz
	2 Level	193 MHz
	4 Level	108 MHz
	6 Level	75 MHz
Interconnect (Manhattan Distance)	1 CLBs	325 MHz
	4 CLBs	260 MHz
	16 CLBs	185 MHz
	64 CLBs	108 MHz
	128 CLBs	81 MHz
Dual Port RAM (Pipelined)	8-Bits by 16	172 MHz
	8-Bits by 256	172 MHz

## XLA, XV I/O Performance

XLA/XV devices have reduced clock delay by 40% over XL devices. This allows pin-to-pin setup and clock-to-out times to be improved significantly. This reduced clock delay also improves no-delay input hold times. In addition, the delays associated with full and partial input delay mode are reduced. The improvement in clock delay is dramatic if the new FastCLK buffers are used in conjunction with Fast Capture Latches (FCL) and no-delay mode. These improvements are summarized in Table 4. The data in this table makes the following assumptions:

- 24mA drive reduces output delay by 0.5ns.
- XC4085XLA clock delays are the same as XC4036XL.
- XC40110XV clock delays are the same as XC4036XL.
- FastCLKs can reach every IOB within their I/O octant typically within 1.5 ns.
- BUFGEs 1,2,5 6 are used to drive IOBs within their I/O octant along the upper and lower edge of the die only.
- No-delay pin-pin setup to Fast Capture Latch (FCL) mode IOBs is the same as XL-08 devices = 0.5ns.
- The I/O clock to the FPGA may be advanced to the

FPGA by as much as the output hold time.

- The output delay may be reduced by 1.0ns if 24mA drive is used into a 20 pF load.

The delays in the table are defined as follows:

- **I/O clock delay** - The maximum delay from clock pad to IOB output flip-flop clock input
- **I/O clock advance** - The intentional skew (if any) between FPGA clock pad and a system reference clock neglecting jitter
- **Clock to Out** - The maximum delay between an active clock edge on a clock pad and a change on an output pad to 50% of VCC (XLA) or VCCIO (XV)
- **Output hold** - The minimum delay between an active clock edge on a clock pad and a change on an output pad to 50% of VCC (XLA) or VCCIO (XV)
- **Input hold** - The minimum amount of time data needs to be held valid on an input pad after the active clock edge on the associated clock input pad
- **Input setup** - The minimum amount of time data needs to be valid on an input pad before the active clock edge on the associated clock input pad

**Table 4: XLA/XV Estimated I/O Performance**

FPGA	I/O clock	Input Mode	Output Mode	I/O Clock delay (internal)	I/O Clock advance (external)	Clock to Out (max)	Output Hold (min)	Input Hold (min)	Input Setup (min)
XC4085XL-09	BUFGLS	Full-delay	12 mA, Fast 50 pF	5.5 ns	0.0 ns	9.0 ns	2.5 ns	0.0 ns	8.4 ns
XC4085XLA XC40110XV	BUFGLS	Full-delay	12 mA, Fast 50 pF	3.5 ns	0.0 ns	7.0 ns	2.5 ns	0.0 ns	5.3 ns
XC4085XLA XC40110XV	BUFGLS	Partial-delay	24 mA, Fast 50 pF	3.5 ns	0.0 ns	6.5 ns	2.5 ns	1.0 ns	4.2 ns
XC4085XLA XC40110XV	FastCLK 1,2,3,4, BUFGE 1,2,5,6	No-delay FCL	12 mA Fast, 50pF	1.0 ns	0.0 ns	4.5 ns	1.3 ns	1.0 ns	0.5 ns
XC4085XLA XC40110XV	FastCLK 1,2,3,4, BUFGE 1,2,5,6	No-delay FCL	24 mA, Fast, 20 pF	1.0 ns	0.0 ns	3.5 ns	1.3 ns	1.0 ns	0.5 ns
XC4085XLA XC40110XV	FastCLK 1,2,3,4, BUFGE 1,2,5,6	No-delay FCL	24 mA, Fast, 20 pF	1.0 ns	1.0 ns	2.5 ns	0.3 ns	0.0 ns	1.5 ns

## Using Fast I/O CLKS

There are several issues associated with implementing Fast I/O clocks by using multiple FastCLK and BUFGE clock buffers for I/O transfers and a BUFGLS clock for internal logic.

**Reduced Clock to Out Period** - When transferring data from an BUFGLS clocked register to an IOB output register which are clocked with a fast I/O clock, the total amount of time available for the transfer is reduced.

**Using Fast Capture Latch in IOB input** - It is necessary to transfer data captured with the fast I/O clock edge to a delayed BUFGLS clock without error. The use of the Fast Capture Latch in the IOBs provides this functionality.

**Driving multiple clock inputs** - Since each FastCLK input can only reach one octant of IOBs it will usually be necessary to drive multiple FastCLK and BUFGE input pads with a copy of the system clock. Xilinx recommends that systems which use multiple FastCLK and BUFGE input buffers use a "Zero Delay" clock buffer such as the Cypress CY2308 to drive up to 8 input pins. These devices contain a Phase locked loop to eliminate clock delay, and specify less than 250ps output jitter.

**PCB layout** - The recommended layout is to place the PLL underneath the FPGA on the reverse side of the PCB. All 8 clock lines should be of equal length. This arrangement will allow all the clock line to be less than 2 cm in length which will generally eliminate the need for clock termination.

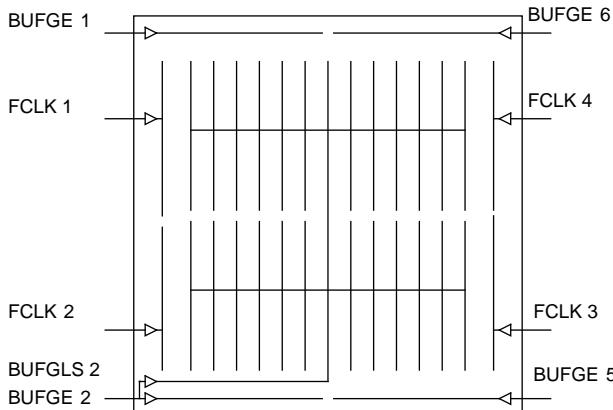


Figure 2. Location of FCLK, BUFGE and BUFGLS clock buffers in XC4000XLA/XV FPGAs

**Advancing the FPGAs clock** - An additional advantage to using a PLL-equipped clock buffer is that it can advance the FPGA clocks relative to the system clock by incorporating additional board delay in the feedback path. Approximately 6 inches of trace length are necessary to delay the signal by 1 ns.

Advancing the FPGA's clock directly reduces input hold requirements and improves clock to out delay. FPGA clocks should not be advanced more than the guaranteed minimum Output Hold Time (minus any associated clock jitter) or the outputs may change state before the system clock edge. For XLA and XV FPGAs the output hold time is 1.3 ns. With 300 ps of clock jitter, the maximum recommended clock advance is 1.0 ns.

**Instantiating I/O elements**- Depending on the design environment, it may be necessary to instantiate the fast I/O elements. They are found in the libraries as:

- **BUFGE (I,O)** - The Global Early Buffer
- **BUFGLS (I,O)** - The Global Low Skew Buffer
- **BUFFCLK (I,O)** - The FastCLK Buffer
- **ILFFX (D, GF, CE, C, Q)** - The Fast Capture Latch Macro

**Locating I/O elements** - It is necessary to connect these elements to a particular I/O pad in order to select which buffer or fast capture latch will be used.

**Restricted Clock Loading** - Because the input hold requirement is a function of internal clock delay, it may be necessary to restrict the routing of BUFGE to IOBs along the top and bottom of the die to obtain sub-ns clock delays.

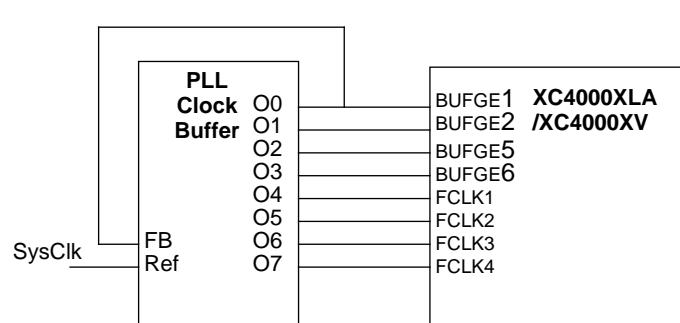


Figure 3. Diagram of XC4000XLA/XV FPGA connected to PLL Clock Buffer driving 4 BUFGE and 4 FCLK clock buffers.

## JTAG Enhancements

XC4000XLA/XV devices have improved JTAG functionality and performance in the following areas:

- IDCODE** - The IDCODE register in JTAG is now supported. All future Xilinx FPGAs will support the IDCODE register. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent upon the FPGA found. The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:cccl

Where

c = the company code;  
a = the array dimension in CLBs;  
f = the Family code;  
v = the die version number.

Family Codes = 01 for XLA;  
= 02 for SpartanXL;  
= 03 for Virtex;  
= 07 for XV.

Xilinx company code = 49 (hex)

Table 5: IDCODEs assigned to XC4000XLA/XV FPGAs

FPGA	IDCODE
XC4013XLA	0x00218093
XC4020XLA	0x0021c093
XC4028XLA	0x00220093
XC4036XLA	0x00224093
XC4044XLA	0x00228093
XC4052XLA	0x0022c093
XC4062XLA	0x00230093
XC4085XLA	0x00238093
XC40110XV	0x00e40093
XC40150XV	0x00e48093
XC40200XV	0x00e54093
XC40250XV	0x00e5c093

- Configuration State** - The configuration state is available to JTAG controllers.
- Configure Disable** - The JTAG port can be prevented from reconfiguring the FPGA
- TCK Startup** - TCK can now be used to clock the start-up block in addition to other user clocks.
- CCLK holdoff** - Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.
- Reissue configure** - The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.
- Bypass FF** - Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop and during EXTEST or SAMPLE/PRELOAD for the IOB register.

## Differences between the XC4000XV and XC4000XLA FPGAs

The high density of the XC4000XV family FPGAs is achieved by using advanced 0.25 micron silicon technology. A 2.5 Volt power supply (VCCINT) is necessary to provide the reduced supply voltage required by 0.25 micron internal logic, however to maintain TTL compatibility a 3.3V power supply (VCCIO) is required by the I/O.

To accommodate the higher gate capacity of XV devices, additional interconnect has been added. These differences are detailed below.

- VCCINT (2.5 Volt) Power Supply Pins**

The XV family of FPGAs requires a 2.5V power supply for internal logic, which is named VCCINT. The pins assigned to the VCCINT supply are named in the pinout guide for the XC4000XV FPGAs and in Table 6

- VCCIO (3.3 Volt) Power Supply Pins**

Both the XV and XLA FPGAs use a 3.3V power supply to power the I/O pins. The I/O supply is named VCCIO in the XV family.

- Octal-Length Interconnect Channels**

The XC40110XV, XC40150XV, XC40200XV, and XC40250XV have enhanced routing. Eight routing channels of octal length have been added to each CLB in both vertical and horizontal dimensions.

## XC4000XLA Socket Compatibility with XL FPGAs

The XC4000XLA devices are generally available in the same packages as equivalent XL devices, however the range of packages available for the XC4085XLA has been extended to include smaller packages such as the HQ240.

## XC4000XV Socket Compatibility with XL/XLA FPGAs

XC4000XV devices are available in five package options, pin-grid PG599 and ball-grid BG560, BG432, and BG352 and quad-flatpack HQ240. With the exception of the VCCINT power pins, XC4000XV FPGAs are compatible with XL and XLA devices in these packages if the following guidelines are followed:

- Lay out the PCB for the XV pinout.
- When an XL or XLA device is installed disconnect the VCCINT (2.5 V) supply. For the PG599, VCCINT should be connected to 3.3V. For BG560, BG432 and BG352 and HQ240 packages, the VCCINT voltage source should be left unconnected. The unused I/O pins in the XL/XLA devices connected to VCCINT will be pulled up to 3.3V. Care must be taken to insure that these pins are not driven when the XL/XLA device is operative.

- When an XC4000XV is installed, the VCCINT pins must be connected to a 2.5V power supply.

The differences between the XL and XV packages are detailed below:

**PG559** - XLA and XL devices in the PG599 package have 56 VCC pins. The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

**BG560** - XLA and XL devices in the BG560 package have 448 I/O pins. The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

**BG432** - XLA and XL devices in the BG432 package have 352 I/O pins. The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

**BG352** - XLA and XL devices in the BG352 package have 289 I/O pins. The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

**HQ240** - XLA and XL devices in the HQ240 package have 193 I/O pins. The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

**Table 6: VCCINT (2.5 V) Pins in XV Packages**

<b>HQ240</b>	<b>BG352</b>	<b>BG432</b>	<b>BG560</b>	<b>PG559</b>
P198	D10	A10	E12	H12
P185	D5	AB2	AD2	H18
P164	K4	AB30	AD32	H26
P154	N3	AG28	AK31	H32
P137	W2	AH15	AM17	M8
P116	AE3	AH5	AK5	M36
P104	AC10	AJ10	AK11	V8
P93	AC13	AK22	AN25	V36
P77	AE19	B23	C24	AF8
P55	AB24	B4	D6	AF36
P43	V24	C16	C17	AM8
P27	N24	E28	E30	AM36
P16	J24	K29	K32	AT12
P4	D24	K3	J1	AT18
P225	A20	R2	T3	AT26
-	-	R29	U32	AT32

## XC4000XLA/XV I/O Signalling Standards

XLA and XV devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 7 and the signalling environment is illustrated in figure 4.

### VCC Clamping

XLA/XV devices are fully 5V TTL I/O compatible if VCC clamping is not enabled. The I/O pins can withstand input voltages up to 7V. With VCC clamping enabled, the XLA/XV devices will begin to clamp input voltages to one diode voltage drop above VCC. In both cases negative voltage is clamped to one diode voltage drop below ground.

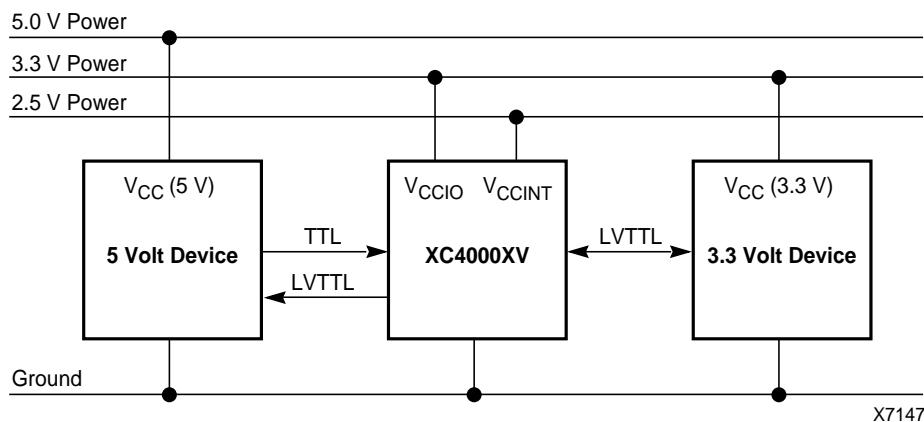
XLA/XV devices maintain LVTTL I/O compatibility when VCC clamping is enabled, however full 5.0V TTL I/O compatibility is sacrificed.

### Overshoot and Undershoot

Ringing wave forms are allowed on XLA/XV inputs as long as undershoot is limited to -2.0V and overshoot is limited to +7.0V and current is limited to 100 mA for less than 10 ns. If VCC clamping is enabled then overshoot will begin to be clamped at VCC/VCCIO plus one diode voltage drop and undershoot will be clamped to ground minus one diode voltage drop. In either case the current must be limited to 100 mA per pin for less than 10 ns.

**Table 7: I/O Standards supported by XC4000XLA and XV FPGAs**

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO
LVCMOS 3V	OK	12/24 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO



X7147

Figure 4. The signalling environment for XLA/XV FPGAs. For XLA devices the VCCIO and VCCINT supplies are replaced by a single 3.3 Volt VCC supply, however, all indicated I/O signalling is still supported.

## Serial PROM Recommendation

Table 8 shows the physical characteristics of each FPGA family member and the recommended Xilinx Serial PROM recommended for use as configuration storage.

**Table 8: Physical Characteristics and Recommended Serial PROM**

Device	Max. User I/O	CLB Matrix	Total CLBs	Logic Cells	Number of Flip-Flops	Max. RAM Bits (No Logic)	Required Configuration Bits	Serial PROM
XC4013XLA	192	24 x 24	576	1,368	1,536	18,432	393,632	XC17512L
XC4020XLA	224	28 x 28	784	1,862	2,016	25,088	521,880	XC17512L
XC4028XLA	256	32 x 32	1,024	2,432	2,560	32,768	668,184	XC1701L
XC4036XLA	288	36 x 36	1,296	3,078	3,168	41,472	832,528	XC1701L
XC4044XLA	320	40 x 40	1,600	3,800	3,840	51,200	1,014,928	XC1701L
XC4052XLA	352	44 x 44	1,936	4,598	4,576	61,952	1,215,368	XC1702L
XC4062XLA	384	48 x 48	2,304	5,472	5,376	73,728	1,433,864	XC1702L
XC4085XLA	448	56 x 56	3,136	7,448	7,168	100,352	1,924,992	XC1702L
XC40110XV	448	64 x 64	4,096	9,728	9,216	131,072	2,686,136	XC1704L
XC40150XV	448	72 x 72	5,184	12,312	11,520	165,888	3,373,448	XC1704L
XC40200XV	448	84 x 84	7,056	16,758	15,456	225,792	4,551,056	XC1704L+XC17512L
XC40250XV	448	92 x 92	8,464	20,102	18,400	270,848	5,433,888	XC1704L+XC1702L

## User I/O Per Package

Table 9 shows the number of user I/Os available in each package for XC4000XLA/XV-Series devices. Call your local sales office for the latest availability information.

Device	Max I/O	HQ160	PQ160	HQ208	PQ208	HQ240	PQ240	BG256	HQ304	BG352	BG432	PG559	BG560
XC4013XLA	192		129		160		192	192					
XC4020XLA	224		129		160		193	205					
XC4028XLA	256	129		160		193		205	256	256			
XC4036XLA	288	129		160		193			256	288	288		
XC4044XLA	320	129		160		193			256	289	320		
XC4052XLA	352	129		160		193			256	289	352		352
XC4062XLA	384	129		160		193			256	289	352		384
XC4085XLA	448	129		160		193			256	289	352		448
XC40110XV	448					178				274	336		432
XC40150XV	448					178				274	336	448	432
XC40200XV	448										336		432
XC40250XV	448										336	448	432

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## Revision Record

Internal Source ADSXC4000XLA\_XV010, September 16, 1998 (Version 0.1):

4000XLA\_XV010wr, September 16, 1998 (Version 0.1): Initial Release

## XC4000XLT Features

**Note:** This data sheet describes the XC4000XLT Family devices. This information does not necessarily apply to the other Xilinx families: XC4000, XC4000A, XC4000D, XC4000H, XC4000L, XC4000E, XC4000EX, XC4000XL or XC4000XV. For information on these devices, or for the most current information regarding the XC4000XLT family, see the Xilinx WEBLINX at <http://www.xilinx.com>.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System performance beyond 80 MHz
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
- Configured by loading binary file
  - Unlimited reprogrammability
- Readback capability
  - Program verification
  - Internal node observability

## XC4000XLT Family FPGAs

### • 3.3V PCI Compliant

XC4000XLT devices provide PCI compliant I/O. They differ from XC4000XL devices only in that they enable the positive input signal clamping function required by PCI specifications.

### • New Packages enable Positive Signal Clamping

The XC4000XLT family of FPGAs is a new packaging option for the XC4000XL FPGAs. For XLT devices, V<sub>tt</sub>, the positive clamping supply is made available to device pins. These V<sub>tt</sub> pins replace 8 normal I/O pins. By connecting the V<sub>tt</sub> pins to a positive power supply, the positive clamping diodes present in the IOBs are enabled.

## XC4000XLT Electrical Features

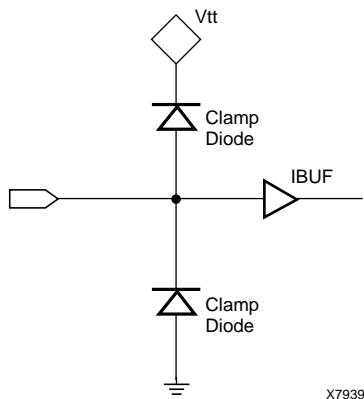
- Low-Voltage Device Functions at V<sub>cc</sub>=3.0 - 3.6 Volts
- V<sub>tt</sub> supply allows positive signal clamping to V<sub>tt</sub>+0.6 V
- Fully 3.3 V PCI compliant I/O (V<sub>tt</sub> connected to 3.3V)
- 5.0 V PCI compatible I/O for embedded systems with 8 loads or less (V<sub>tt</sub> connected to 5.0 V)
- 5.0 V TTL compatible I/O (V<sub>tt</sub> connected to 5.0V)
- 3.3 V LVTTI, LVCMSO compatible I/O

## Additional XC4000XLT Family Features

- **Highest Performance** — XC4000XL architecture
- **Highest Capacity** — Over 130,000 system gates
- **Low Power** — 3.3 V technology
- **Software Compatibility** — Bitstream compatible with XC4000XL devices
- **Package Compatibility** — Footprint compatible with XC4000XL devices (except for V<sub>tt</sub> power pins)
- **Advanced Technology** — 0.35 micron CMOS process
- Buffered interconnect for maximum speed
- New latch capability in configurable logic blocks
- Improved VersaRing™ I/O interconnect for better fixed pinout flexibility
- Flexible high-speed clock network
  - 8 additional Early Buffers for shorter clock delays
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input function generator on device outputs
- 26 Address bits in master parallel configuration mode

## PCI Compatible Features

- LogiCORE PCI Interface 2.0 available
  - 33 MHz 32-Bit PCI interface
  - Master or Target mode
  - Implemented entirely in programmable logic
  - Up to 100,000 gates available for user logic
- Fully compliant 3.3 V PCI I/O
  - < 7 nsec input setup time
  - 0 nsec input hold time
  - < 11 nsec clock to output
  - Positive and negative input signal clamping
  - Meets 5.0 V PCI timing for up to 8 loads
    - 80 mA sink current at minimum AC drive point (2.2V)



**Figure 1: Clamp Diodes Present in the XL, XLT IOBs**

### PCI Requirements for Clamp Diodes

Clamp diodes are electrical protection devices placed in the I/O buffer of a chip. Both 5 V PCI and 3.3 V PCI signalling environments require clamp diodes to ground, which all Xilinx 4K family devices have. The 3.3 V PCI specification also requires clamp diodes to 3.3 V. The clamp diode serves two purposes. It offers device protection and it controls the bus waveforms as signals are transitioning on the bus. The latter function is vital to the signal integrity of the bus and is why clamp diodes are mandatory in a 3.3 V PCI system.

### 5.0 V PCI Requirement for Maximum AC Ratings and Device Protection

The upper clamp diode is optional in 5 V systems. For 5 V signalling, the PCI specification simply requires the devices be able to withstand a maximum overshoot voltage of 11 V for a minimum of 11 nsec through a 55 ohm resistor. See the PCI Specification v2.1, p126 for more details on this particular test. XC4000XL/XLT devices have a maximum

input voltage requirement of 7.0 V (for < 10 nsec). In order to meet the PCI test requirements and provide device protection, it is necessary to connect the Vtt pins to the 5.0 V power supply.

## Difference Between the XC4000XLT and XC4000XL FPGAs

The only difference between XLT and XL devices is that in XLT devices, the Vtt supply is connected to package pins. By connecting the Vtt supply pins to a positive voltage, positive input signal clamping is enabled. The Vtt pins assigned to the Vtt supply are named in the pinout guide for the XC4013XLT, XC4028XLT, and XC4062XLT FPGAs. There are 8 Vtt pins in all package options.

### I/O Signaling Compliance

The I/O signaling compliance is a function of how the Vtt pins are connected. Connecting Vtt to a power supply programs the compliance for all the IOBs on the device. All 8 of the Vtt pins must be connected to the same voltage source.

- **Vtt floating**

When Vtt is left floating, the I/O characteristics of the XLT devices will be identical to XL devices. I/O will be LVTTL and LVCMSO compatible.

- **Vtt connected to 5.0V power.**

If Vtt is connected to the 5.0 V power supply, the XLT device will be TTL, LVTTL, LVCMSO and 5V-PCI compatible for up to 8 PCI loads.

- **Vtt connected to 3.3V power**

If Vtt is connected to 3.3V power, the I/O will be LVTTL, LVCMSO, and 3.3V-PCI compliant. Note that 5V TTL and 5V CMOS is not allowed.

**Table 1: XC4000XLT Family Field Programmable Gate Arrays**

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O
XC4013XLT	1368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	184
XC4028XLT	2432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	185
XC4062XLT	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	352

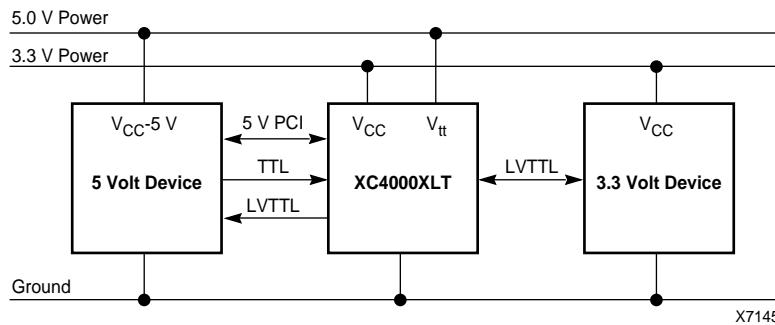


Figure 2: XLT Power supply and signaling environment with V<sub>tt</sub> connected to 5.0 V power supply

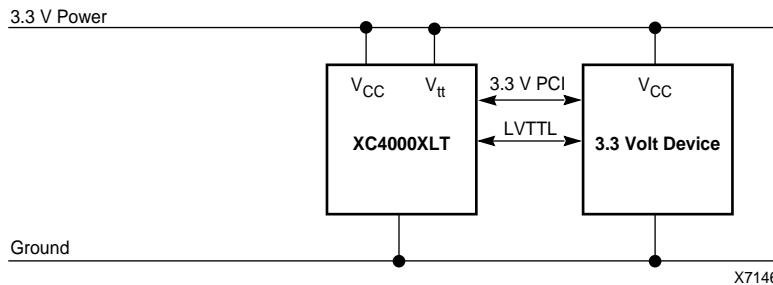


Figure 3: XLT Power supply and signaling environment with V<sub>tt</sub> connected to 3.3V power supply

## Pin Locations for XC4013XLT Devices

XC4013XLT Pad Name	PQ208	PQ240
VCC	P183	P212
I/O (A8)	P184	P213
I/O (A9)	P185	P214
I/O (A19)	P186	P215
I/O (A18)	P187	P216
I/O	P188	P217
I/O	P189	P218
I/O (A10)	P190	P220
I/O (A11)	P191	P221
VCC	-	P222
VTT	192	P223
I/O	-	P224
I/O	-	P225
I/O	P193	P226
GND	P194	P227
I/O	P195	P228
I/O	P196	P229
I/O	P197	P230
I/O	P198	P231
I/O (A12)	P199	P232
I/O (A13)	P200	P233
I/O	-	P234
I/O	-	P235
I/O	P201	P236
I/O	P202	P237
I/O (A14)	P203	P238
I/O, GCK8 (A15)	P204	P239
VCC	P205	P240
GND	P2	P1
I/O, GCK1 (A16)	P4	P2
I/O (A17)	P5	P3
I/O	P6	P4
I/O	P7	P5
I/O, TDI	P8	P6
I/O, TCK	P9	P7
I/O	P10	P8
I/O	P11	P9
I/O	P12	P10
I/O	P13	P11
I/O	-	P12
I/O	-	P13
GND	P14	P14
I/O	P15	P15
I/O	P16	P16
I/O, TMS	P17	P17
VTT	P18	P18
VCC	-	P19
I/O	-	P20
I/O	-	P21
I/O	P19	P23
I/O	P20	P24
I/O	P21	P25
I/O	P22	P26
I/O	P23	P27
I/O	P24	P28
GND	P25	P29
VCC	P26	P30
I/O	P27	P31
I/O	P28	P32
I/O	P29	P33
I/O	P30	P34
I/O	P31	P35
I/O	P32	P36
I/O	-	P38
I/O	-	P39
VCC	-	P40
VTT	P33	P41
I/O	P34	P42
I/O	P35	P43
I/O	P36	P44
GND	P37	P45
I/O	-	P46

XC4013XLT Pad Name	PQ208	PQ240
I/O	-	P47
I/O	P38	P48
I/O	P39	P49
I/O	P40	P50
I/O	P41	P51
I/O	P42	P52
I/O	P43	P53
I/O	P44	P54
I/O	P45	P55
I/O	P46	P56
I/O, GCK2	P47	P57
O (M1)	P48	P58
GND	P49	P59
I (M0)	P50	P60
VCC	P55	P61
I (M2)	P56	P62
I/O, GCK3	P57	P63
I/O (HDC)	P58	P64
I/O	P59	P65
I/O	P60	P66
I/O	P61	P67
I/O (LDC)	P62	P68
I/O	P63	P69
I/O	P64	P70
I/O	P65	P71
I/O	P66	P72
I/O	-	P73
I/O	-	P74
GND	P67	P75
I/O	P68	P76
I/O	P69	P77
I/O	P70	P78
VTT	P71	P79
VCC	-	P80
I/O	P72	P81
I/O	P73	P82
I/O	-	P84
I/O	-	P85
I/O	P74	P86
I/O	P75	P87
I/O	P76	P88
I/O (INIT)	P77	P89
VCC	P78	P90
GND	P79	P91
I/O	P80	P92
I/O	P81	P93
I/O	P82	P94
I/O	P83	P95
I/O	P84	P96
I/O	P85	P97
I/O	-	P99
I/O	-	P100
VCC	-	P101
VTT	P86	P102
I/O	P87	P103
I/O	P88	P104
I/O	P89	P105
GND	P90	P106
I/O	-	P107
I/O	-	P108
I/O	P91	P109
I/O	P92	P110
I/O	P93	P111
I/O	P94	P112
I/O	P95	P113
I/O	P96	P114
I/O	P97	P115
I/O	P98	P116
I/O	P99	P117
I/O, GCK4	P100	P118
GND	P101	P119
DONE	P103	P120

XC4013XLT Pad Name	PQ208	PQ240
VCC	P106	P121
PROGRAM	P108	P122
I/O (D7)	P109	P123
I/O, GCK5	P110	P124
I/O	P111	P125
I/O	P112	P126
I/O	-	P127
I/O	-	P128
I/O (D6)	P113	P129
I/O	P114	P130
I/O	P115	P131
I/O	P116	P132
I/O	P117	P133
I/O	P118	P134
GND	P119	P135
I/O	-	P136
I/O	-	P137
I/O	P120	P138
VTT	P121	P139
VCC	-	P140
I/O (D5)	P122	P141
I/O (CS0)	P123	P142
I/O	P124	P144
I/O	P125	P145
I/O	P126	P146
I/O	P127	P147
I/O (D4)	P128	P148
I/O	P129	P149
VCC	P130	P150
GND	P131	P151
I/O (D3)	P132	P152
I/O (RS)	P133	P153
I/O	P134	P154
I/O	P135	P155
I/O	P136	P156
I/O	P137	P157
I/O (D2)	P138	P159
I/O	P139	P160
VCC	-	P161
VTT	P140	P162
I/O	P141	P163
I/O	-	P164
I/O	-	P165
GND	P142	P166
I/O	-	P167
I/O	-	P168
I/O	P143	P169
I/O	P144	P170
I/O	P145	P171
I/O	P146	P172
I/O (D1)	P147	P173
I/O (RCLK, RDY/BUSY)	P148	P174
I/O	P149	P175
I/O	P150	P176
I/O (D0, DIN)	P151	P177
I/O, SGCK4 †, GCK6 ‡ (DOUT)	P152	P178
CCLK	P153	P179
VCC	P154	P180
O, TDO	P159	P181
GND	P160	P182
I/O (A0, WS)	P161	P183
I/O, GCK7 (A1)	P162	P184
I/O	P163	P185
I/O	P164	P186

XC4013XLT Pad Name	PQ208	PQ240
I/O (CS1, A2)	P165	P187
I/O (A3)	P166	P188
I/O	-	P189
I/O	-	P190
I/O	P167	P191
I/O	P168	P192
I/O	P169	P193
I/O	P170	P194
GND	P171	P196
I/O	P172	P197
I/O	-	P198
I/O	-	P199
VTT	173	P200
VCC	-	P201
I/O (A4)	P174	P202
I/O (A5)	P175	P203
I/O	P176	P205
I/O	P177	P206
I/O (A21)	P178	P207
I/O (A20)	P179	P208
I/O (A6)	P180	P209
I/O (A7)	P181	P210
GND	P182	P211

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

## Additional XC4013XLT Package Pins

PQ208

N.C. Pins					
P1	P3	P51	P52	P53	P54
P102	P104	P105	P107	P155	P156
P157	P158	P206	P207	P208	-

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PQ240

GND Pins					
P22‡	P37‡	P83‡	P98‡	P143‡	P158‡
P204‡	P219‡	-	-	-	-
N.C. Pins					
P195	-	-	-	-	-

6/9/97

‡ Pins marked with this symbol are used for Ground connections on some revisions of the device. These pins may not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

## Pin Locations for XC4028XLT Devices

XC4028XLT Pad Name	HQ 240
VCC	P212
I/O (A8)	P213
I/O (A9)	P214
I/O (A19)	P215
I/O (A18)	P216
I/O	P217
I/O	P218
I/O (A10)	P220
I/O (A11)	P221
GND	-
I/O	-
I/O	-
I/O	-
VCC	P222
VTT	P223
I/O	P224
I/O	P225
I/O	P226
GND	P227
I/O	-
I/O	-
I/O	P228
I/O	P229
I/O	P230
I/O	P231
I/O (A12)	P232
I/O (A13)	P233
GND	-
VCC	-
I/O	-
I/O	-
I/O	P234
I/O	P235
I/O	P236
I/O	P237
I/O (A14)	P238
I/O, GCK8, (A15)	P239
VCC	P240
GND	P1
I/O, GCK1, (A16)	P2
I/O (A17)	P3
I/O	P4
I/O	P5
I/O, TDI	P6
I/O, TCK	P7
I/O	-
I/O	-
VCC	-
GND	-
I/O	P8
I/O	P9
I/O	P10
I/O	P11
I/O	P12
I/O	P13
I/O	-
I/O	-
GND	P14
I/O	P15
I/O	P16
I/O, TMS	P17
VTT	P18
VCC	P19
I/O	P20
I/O	P21

XC4028XLT Pad Name	HQ 240
I/O	-
I/O	-
GND	P22
I/O	-
I/O	-
I/O	P23
I/O	P24
I/O	P25
I/O	P26
I/O	P27
I/O	P28
GND	P29
VCC	P30
I/O	P31
I/O	P32
I/O	P33
I/O	P34
I/O	P35
I/O	P36
I/O	-
I/O	-
GND	P37
I/O	-
I/O	-
I/O	P38
I/O	P39
VCC	P40
VTT	P41
I/O	P42
I/O	P43
I/O	P44
GND	P45
I/O	-
I/O	-
I/O	P46
I/O	P47
I/O	P48
I/O	P49
I/O	P50
I/O	P51
GND	-
VCC	-
I/O	-
I/O	-
I/O	P52
I/O	P53
I/O	P54
I/O	P55
I/O	P56
I/O, GCK2	P57
O (M1)	P58
GND	P59
I (M0)	P60
VCC	P61
I (M2)	P62
I/O, GCK3	P63
I/O (HDC)	P64
I/O	P65
I/O	P66
I/O	P67
I/O (LDC)	P68
I/O	-
I/O	-
VCC	-
GND	-
I/O	P69

<b>XC4028XLT Pad Name</b>	<b>HQ 240</b>
I/O	P70
I/O	P71
I/O	P72
I/O	P73
I/O	P74
I/O	-
I/O	-
GND	P75
I/O	P76
I/O	P77
I/O	P78
VTT	P79
VCC	P80
I/O	P81
I/O	P82
I/O	-
I/O	-
GND	P83
I/O	-
I/O	-
I/O	P84
I/O	P85
I/O	P86
I/O	P87
I/O	P88
I/O (INIT)	P89
VCC	P90
GND	P91
I/O	P92
I/O	P93
I/O	P94
I/O	P95
I/O	P96
I/O	P97
I/O	-
I/O	-
GND	P98
I/O	-
I/O	-
I/O	P99
I/O	P100
VCC	P101
VTT	P102
I/O	P103
I/O	P104
I/O	P105
GND	P106
I/O	-
I/O	-
I/O	P107
I/O	P108
I/O	P109
I/O	P110
I/O	P111
I/O	P112
GND	-
VCC	-
I/O	-
I/O	-
I/O	P113
I/O	P114
I/O	P115
I/O	P116
I/O	P117
I/O, GCK4	P118
GND	P119
DONE	P120
VCC	P121
PRO- GRAM	P122

<b>XC4028XLT Pad Name</b>	<b>HQ 240</b>
I/O (D7)	P123
I/O, GCK5	P124
I/O	P125
I/O	P126
I/O	P127
I/O	P128
I/O	-
I/O	-
VCC	-
GND	-
I/O (D6)	P129
I/O	P130
I/O	P131
I/O	P132
I/O	P133
I/O	P134
I/O	-
I/O	-
GND	P135
I/O	P136
I/O	P137
I/O	P138
VTT	P139
VCC	P140
I/O (D5)	P141
I/O (CS0)	P142
I/O	-
I/O	-
GND	P143
I/O	-
I/O	-
I/O	P144
I/O	P145
I/O	P146
I/O	P147
I/O (D4)	P148
I/O	P149
VCC	P150
GND	P151
I/O (D3)	P152
I/O (RS)	P153
I/O	P154
I/O	P155
I/O	P156
I/O	P157
I/O	-
GND	P158
I/O	-
I/O	-
I/O (D2)	P159
I/O	P160
VCC	P161
VTT	P162
I/O	P163
I/O	P164
I/O	P165
GND	P166
I/O	-
I/O	-
I/O	P167
I/O	P168
I/O	P169
I/O	P170
I/O	P171
I/O	P172
GND	-
VCC	-
I/O (D1)	P173
I/O (RCLK, RDY/BUSY)	P174

XC4028XLT Pad Name	HQ 240
I/O	-
I/O	-
I/O	P175
I/O	P176
I/O (D0, DIN)	P177
I/O, GCK6 (DOUT)	P178
CCLK	P179
VCC	P180
O, TDO	P181
GND	P182
I/O (A0, WS)	P183
I/O, GCK7 (A1)	P184
I/O	P185
I/O	P186
I/O (CS1, A2)	P187
I/O (A3)	P188
I/O	-
I/O	-
VCC	-
GND	-
I/O	P189
I/O	P190
I/O	P191
I/O	P192
I/O	P193
I/O	P194
I/O	P195
I/O	-
GND	P196
I/O	P197

XC4028XLT Pad Name	HQ 240
I/O	P198
I/O	P199
VTT	P200
VCC	P201
I/O	-
I/O	-
I/O	-
GND	-
I/O (A4)	P202
I/O (A5)	P203
I/O	P205
I/O	P206
I/O (A21)	P207
I/O (A20)	P208
I/O (A6)	P209
I/O (A7)	P210
GND	P211

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**Additional XC4028XLT Package Pins**

HQ240

GND Pins					
P204	P219	-	-	-	-

10/7/97

Note: These pins may be N.C. for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

## Pin Locations for XC4062XLT Devices

XC4062XLT Pad Name	HQ240	BG432
VCC	P212	VCC*
I/O (A8)	P213	D17
I/O (A9)	P214	A17
I/O	-	C17
I/O	-	B17
I/O	-	-
GND	-	GND*
I/O (A19)	P215	C18
I/O (A18)	P216	D18
I/O	P217	B18
I/O	P218	A19
I/O (A10)	P220	B19
I/O (A11)	P221	C19
VCC	-	VCC*
GND	-	GND*
I/O	-	D19
I/O	-	A20
I/O	-	B20
I/O	-	C20
I/O	-	B21
I/O	-	D20
GND	-	GND*
I/O	-	C21
I/O	-	A22
VCC	P222	VCC*
VTT	P223	B22
I/O	P224	C22
I/O	P225	B23
I/O	P226	A24
GND	P227	GND*
I/O	-	D22
I/O	-	C23
I/O	P228	B24
I/O	P229	C24
I/O	-	-
I/O	-	-
GND	-	GND*
I/O	-	D23
I/O	-	B25
I/O	P230	A26
I/O	P231	C25
I/O (A12)	P232	D24
I/O (A13)	P233	B26
GND	-	GND*
VCC	-	VCC*
I/O	-	A27
I/O	-	D25
I/O	-	C26
I/O	-	B27
I/O	-	A28
I/O	-	D26
GND	-	GND*
I/O	P234	C27
I/O	P235	B28
I/O	P236	D27
I/O	P237	B29
I/O (A14)	P238	C28
I/O, GCK8 (A15)	P239	D28
VCC	P240	VCC*
GND	P1	GND*
I/O, GCK1 (A16)	P2	D29
I/O (A17)	P3	C30
I/O	P4	E28
I/O	P5	E29
I/O, TDI	P6	D30

XC4062XLT Pad Name	HQ240	BG432
I/O, TCK	P7	D31
GND	-	GND*
I/O	-	F28
I/O	-	F29
I/O	-	E30
I/O	-	E31
I/O	-	G28
I/O	-	G29
VCC	-	VCC*
GND	-	GND*
I/O	-	F30
I/O	P8	F31
I/O	P9	H28
I/O	P10	H29
I/O	P11	G30
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	P12	J28
I/O	P13	J29
I/O	-	H31
I/O	-	J30
GND	P14	GND*
I/O	P15	K28
I/O	P16	K29
I/O, TMS	P17	K30
VTT	P18	K31
VCC	P19	VCC*
I/O	P20	L29
I/O	P21	L30
GND	-	GND*
I/O	-	M30
I/O	-	M28
I/O	-	M29
I/O	-	M31
I/O	-	N31
I/O	-	N28
GND	P22	GND*
VCC	-	VCC*
I/O	-	N29
I/O	-	N30
I/O	-	P30
I/O	-	P28
I/O	P23	P29
I/O	P24	R31
GND	-	GND*
I/O	P25	R30
I/O	P26	R28
I/O	-	-
I/O	-	-
I/O	P27	R29
I/O	P28	T31
GND	P29	GND*
VCC	P30	VCC*
I/O	P31	T30
I/O	P32	T29
I/O	-	-
I/O	-	-
I/O	P33	U31
I/O	P34	U30
GND	-	-
I/O	P35	U28
I/O	P36	U29
I/O	-	V30
I/O	-	V29

XC4062XLT Pad Name	HQ240	BG432
I/O	-	V28
I/O	-	W31
VCC	-	VCC*
GND	P37	GND*
I/O	-	W30
I/O	-	W29
I/O	-	W28
I/O	-	Y31
I/O	-	Y30
I/O	-	Y29
GND	-	GND*
I/O	P38	Y28
I/O	P39	AA30
VCC	P40	VCC*
VTT	P41	AA29
I/O	P42	AB31
I/O	P43	AB30
I/O	P44	AB29
GND	P45	GND*
I/O	-	AB28
I/O	-	AC30
I/O	P46	AC29
I/O	P47	AC28
I/O	-	-
I/O	-	-
GND	-	GND*
I/O	-	AD31
I/O	-	AD30
I/O	P48	AD29
I/O	P49	AD28
I/O	P50	AE30
I/O	P51	AE29
GND	-	GND*
VCC	-	VCC*
I/O	-	AF31
I/O	-	AE28
I/O	-	AF30
I/O	-	AF29
I/O	P52	AG31
I/O	P53	AF28
GND	-	GND*
I/O	-	AG30
I/O	-	AG29
I/O	P54	AH31
I/O	P55	AG28
I/O	P56	AH30
I/O, GCK2	P57	AJ30
O (M1)	P58	AH29
GND	P59	GND*
I (M0)	P60	AH28
VCC	P61	VCC*
I (M2)	P62	AJ28
I/O, GCK3	P63	AK29
I/O (HDC)	P64	AH27
I/O	P65	AK28
I/O	P66	AJ27
I/O	P67	AL28
I/O (LDC)	P68	AH26
GND	-	GND*
I/O	-	AK27
I/O	-	AJ26
I/O	-	AL27
I/O	-	AH25
I/O	-	AK26
I/O	-	AL26
VCC	-	VCC*
GND	-	GND*
I/O	P69	AH24
I/O	P70	AJ25
I/O	P71	AK25

XC4062XLT Pad Name	HQ240	BG432
I/O	P72	AJ24
I/O	-	AH23
I/O	-	AK24
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	P73	AL24
I/O	P74	AH22
I/O	-	AJ23
I/O	-	AK23
GND	P75	GND*
I/O	P76	AJ22
I/O	P77	AK22
I/O	P78	AL22
VTT	P79	AJ21
VCC	P80	VCC*
I/O	P81	AH20
I/O	P82	AK21
GND	-	GND*
I/O	-	AJ20
I/O	-	AH19
I/O	-	AK20
I/O	-	AJ19
I/O	-	AL20
I/O	-	AH18
GND	P83	GND*
VCC	-	VCC*
I/O	-	AK19
I/O	-	AJ18
I/O	P84	AL19
I/O	P85	AK18
I/O	P86	AH17
I/O	P87	AJ17
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	-	AK17
I/O	-	AL17
I/O	P88	AJ16
I/O (INIT)	P89	AK16
VCC	P90	VCC*
GND	P91	GND*
I/O	P92	AL16
I/O	P93	AH15
I/O	-	AL15
I/O	-	AJ15
I/O	-	-
GND	-	GND*
I/O	P94	AK15
I/O	P95	AJ14
I/O	P96	AH14
I/O	P97	AK14
I/O	-	AL13
I/O	-	AK13
VCC	-	VCC*
GND	P98	GND*
I/O	-	AJ13
I/O	-	AH13
I/O	-	AL12
I/O	-	AK12
I/O	-	AJ12
I/O	-	AK11
GND	-	GND*
I/O	P99	AH12
I/O	P100	AJ11
VCC	P101	VCC*
VTT	P102	AL10
I/O	P103	AK10
I/O	P104	AJ10

XC4062XLT Pad Name	HQ240	BG432
I/O	P105	AK9
GND	P106	GND*
I/O	-	AL8
I/O	-	AH10
I/O	P107	AJ9
I/O	P108	AK8
I/O	-	-
I/O	-	-
GND	-	GND*
I/O	-	AJ8
I/O	-	AH9
I/O	P109	AK7
I/O	P110	AL6
I/O	P111	AJ7
I/O	P112	AH8
GND	-	GND*
VCC	-	VCC*
I/O	-	AK6
I/O	-	AL5
I/O	P113	AH7
I/O	P114	AJ6
I/O	-	AK5
I/O	-	AL4
GND	-	GND*
I/O	-	AH6
I/O	-	AJ5
I/O	P115	AK4
I/O	P116	AH5
I/O	P117	AK3
I/O, GCK4	P118	AJ4
GND	P119	GND*
DONE	P120	AH4
VCC	P121	VCC*
PROGRAM	P122	AH3
I/O (D7)	P123	AJ2
I/O, GCK5	P124	AG4
I/O	P125	AG3
I/O	P126	AH2
I/O	-	AH1
I/O	-	AF4
GND	-	GND*
I/O	P127	AF3
I/O	P128	AG2
I/O	-	AG1
I/O	-	AE4
I/O	-	AE3
I/O	-	AF2
VCC	-	VCC*
GND	-	GND*
I/O (D6)	P129	AF1
I/O	P130	AD4
I/O	P131	AD3
I/O	P132	AE2
I/O	-	AD2
I/O	-	AC4
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	P133	AC3
I/O	P134	AD1
I/O	-	AC2
I/O	-	AB4
GND	P135	GND*
I/O	P136	AB3
I/O	P137	AB2
I/O	P138	AB1
VTT	P139	AA3
VCC	P140	VCC*
I/O (D5)	P141	AA2
I/O (CS0)	P142	Y2

XC4062XLT Pad Name	HQ240	BG432
GND	P143	GND*
I/O	-	Y4
I/O	-	Y3
I/O	-	Y1
I/O	-	W1
I/O	-	W4
I/O	-	W3
GND	-	GND*
VCC	-	VCC*
I/O	-	W2
I/O	-	V2
I/O	-	V4
I/O	P144	U1
I/O	P145	U2
GND	-	GND*
I/O	P146	U4
I/O	P147	U3
I/O	-	-
I/O	-	-
I/O (D4)	P148	T1
I/O	P149	T2
VCC	P150	VCC*
GND	P151	GND*
I/O (D3)	P152	T3
I/O (RS)	P153	R1
I/O	-	-
I/O	-	-
I/O	P154	R2
I/O	P155	R4
GND	-	GND*
I/O	P156	R3
I/O	P157	P2
I/O	-	P3
I/O	-	P4
I/O	-	N1
I/O	-	N2
VCC	-	VCC*
GND	P158	GND*
I/O	-	N3
I/O	-	N4
I/O	-	M1
I/O	-	M2
I/O	-	M3
I/O	-	M4
GND	-	GND*
I/O (D2)	P159	L2
I/O	P160	L3
VCC	P161	VCC*
VTT	P162	K1
I/O	P163	K2
I/O	P164	K3
I/O	P165	K4
GND	P166	GND*
I/O	-	J2
I/O	-	J3
I/O	P167	J4
I/O	P168	H1
I/O	-	-
I/O	-	-
GND	-	GND*
I/O	P169	H2
I/O	P170	H3
I/O	P171	H4
I/O	P172	G2
I/O	-	G3
GND	-	GND*
VCC	-	VCC*
I/O (D1)	P173	G4

XC4062XLT Pad Name	HQ240	BG432
I/O (RCLK, RDY/BUSY)	P174	F2
I/O	-	F3
I/O	-	E1
I/O	-	F4
I/O	-	E2
GND	-	GND*
I/O	-	E3
I/O	-	D1
I/O	P175	E4
I/O	P176	D2
I/O (D0, DIN)	P177	C2
I/O, GCK6 (DOUT)	P178	D3
CCLK	P179	D4
VCC	P180	VCC*
O, TDO	P181	C4
GND	P182	GND*
I/O (A0, WS)	P183	B3
I/O, GCK7 (A1)	P184	D5
I/O	P185	B4
I/O	P186	C5
I/O	-	A4
I/O	-	D6
GND	-	GND*
I/O	-	B5
I/O	-	C6
I/O (CS1, A2)	P187	A5
I/O (A3)	P188	D7
I/O	-	B6
I/O	-	A6
VCC	-	VCC*
GND	-	GND*
I/O	P189	D8
I/O	P190	C7
I/O	P191	B7
I/O	P192	D9
I/O	-	B8
I/O	-	A8
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	P193	D10
I/O	P194	C9
I/O	P195	B9
I/O	-	C10
GND	P196	GND*
I/O	P197	B10
I/O	P198	A10
I/O	P199	C11
VTT	P200	D12
VCC	P201	VCC*
I/O	-	B11
I/O	-	C12
GND	-	GND*
I/O	-	D13
I/O	-	B12

XC4062XLT Pad Name	HQ240	BG432
I/O	-	C13
I/O	-	A12
I/O	-	D14
I/O	-	B13
GND	-	GND*
VCC	-	VCC*
I/O (A4)	P202	C14
I/O (A5)	P203	A13
I/O	P205	B14
I/O	P206	D15
I/O (A21)	P207	C15
I/O (A20)	P208	B15
GND	-	GND*
I/O	-	-
I/O	-	-
I/O	-	A15
I/O	-	C16
I/O (A6)	P209	B16
I/O (A7)	P210	A16
GND	P211	GND*

8/21/1997

\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package. They have no direct connection to any specific package pin.

## Additional XC4062XLT Package Pins

### HQ240

GND Pins						
P204	P219	-	-	-	-	-
5/5/97						

Note: These pins may be N.C. for this device revision, however for compatibility with other devices in this package, these pins should be tied to GND.

### BG432

VCC Pins						
A1	A11	A21	A31	C3	C29	D11
D21	L1	L4	L28	L31	AA1	AA4
AA28	AA31	AH11	AH21	AJ3	AJ29	AL1
AL11	AL21	AL31	-	-	-	-
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	-
N.C. Pins						
C8	-	-	-	-	-	-

5/5/97



# Spartan and SpartanXL Families Field Programmable Gate Arrays

September 28, 1998 (Version 1.2)

Preliminary Product Specification

## Introduction

The Spartan™ Series is the first high-volume production FPGA solution to deliver all the key requirements for ASIC replacement up to 40,000 gates. These requirements include high performance, on-chip RAM, Core Solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan Series is the result of more than thirteen years of FPGA design experience and feedback from thousands of customers. By streamlining the Spartan feature set, leveraging advanced hybrid process technologies and focusing on total cost management, the Spartan Series delivers the key features required by ASIC and other high volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs. The Spartan Series currently has 10 members, as shown in [Table 1](#).

## Spartan Series Features

Note: The Spartan Series devices described in this data sheet include the 5 V Spartan family of devices and the 3.3 V SpartanXL™ family of devices.

- Next generation ASIC replacement technology
  - First ASIC replacement FPGA for high-volume production with on-chip RAM
  - Advanced process technology
  - Density up to 1862 logic cells or 40,000 system gates
  - Streamlined feature set based on XC4000 architecture
  - System performance beyond 80 MHz
  - Broad set of AllianceCORE™ and LogiCORE™ pre-defined solutions available
  - Unlimited reprogrammability
  - Low cost

- System level features
  - Available in both 5.0 Volt and 3.3 Volt versions
  - On-chip SelectRAM™ memory
  - Fully PCI compliant
  - Low power segmented routing architecture
  - Full readback capability for program verification and internal node observability
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal networks
  - IEEE 1149.1-compatible boundary scan logic
- Versatile I/O and packaging
  - Low cost plastic packages available in all densities
  - Footprint compatibility in common packages across all Spartan and SpartanXL devices
  - Individually programmable output slew-rate control maximizes performance and reduces noise
  - Zero input register hold time simplifies system timing
- Fully supported by powerful Xilinx development system
  - Foundation series: Integrated, shrink-wrap software
  - Alliance series: Over 100 PC and workstation 3<sup>RD</sup> party development systems supported
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

## Additional SpartanXL Features

- 3.3V supply for low power with 5V tolerant I/Os
- Higher performance
- Faster carry logic
- More flexible high-speed clock network
- Latch capability in Configurable Logic Blocks
- Input fast capture latch
- Optional mux or 2-input function generator on outputs
- 12 mA or 24 mA output drive
- 5V/3.3V PCI compatible
- Enhanced Boundary Scan
- Express Mode configuration

**Table 1: Spartan and SpartanXL Series Field Programmable Gate Arrays**

Device	Logic Cells	Max System Gates	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Available User I/O
XCS05 & XCS05XL	238	5,000	2,000 - 5,000	10 x 10	100	360	77
XCS10 & XCS10XL	466	10,000	3,000 - 10,000	14 x 14	196	616	112
XCS20 & XCS20XL	950	20,000	7,000 - 20,000	20 x 20	400	1,120	160
XCS30 & XCS30XL	1368	30,000	10,000 - 30,000	24 x 24	576	1,536	192
XCS40 & XCS40XL	1862	40,000	13,000 - 40,000	28 x 28	784	2,016	205

\* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

## General Overview

Spartan Series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in [Figure 1](#). They have generous routing resources to accommodate the most complex interconnect patterns.

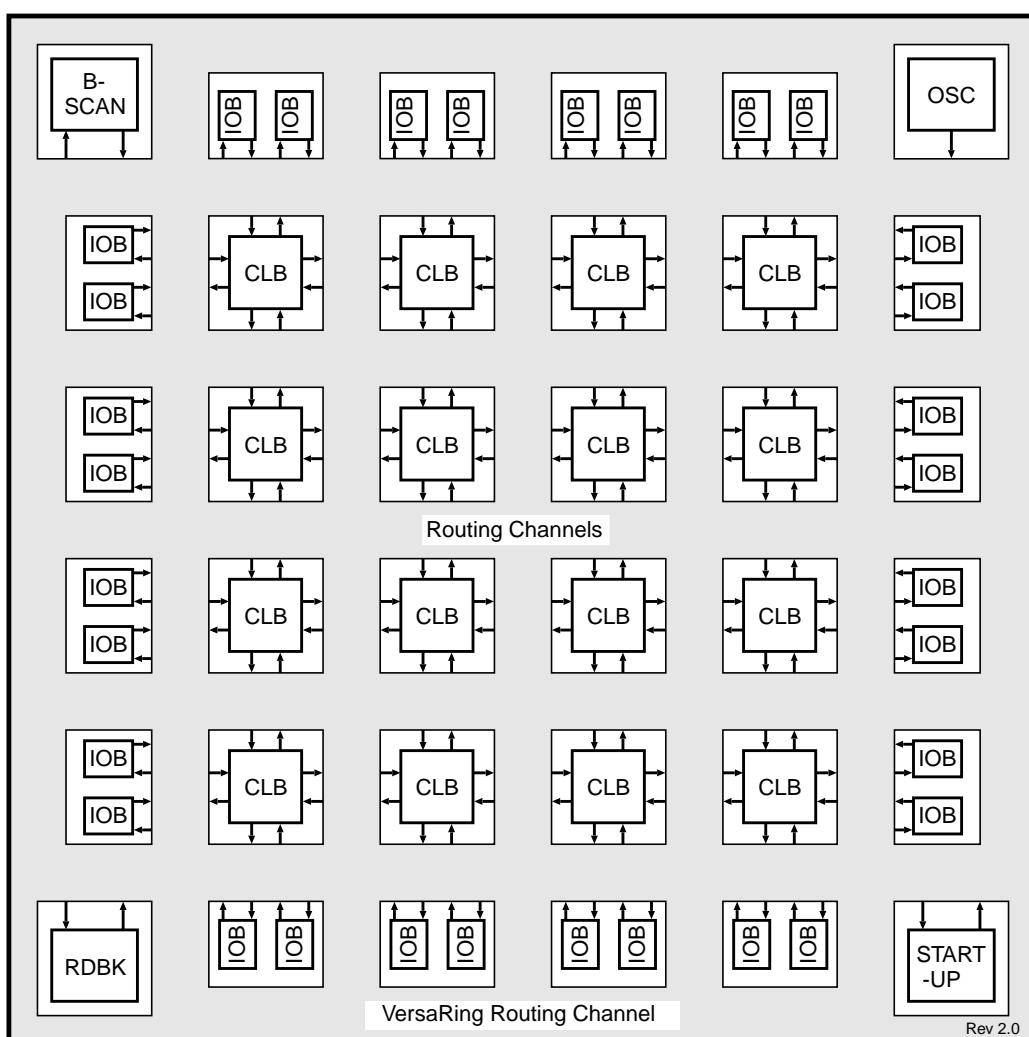
The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for

shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

Spartan Series devices achieve high-performance, low-cost operation through the use of an advanced architecture and semiconductor technology. Spartan and SpartanXL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In contrast to other FPGA devices, Spartan FPGAs offer the most cost-effective solution while maintaining leading-edge performance. In addition to the conventional benefit of high volume programmable logic solutions Spartan FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan Series leverages the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA and XC4000XV process developments.



**Figure 1: Basic FPGA Block Diagram**

## Logic Functional Description

The Spartan Series uses a standard FPGA structure as shown in [Figure 1 on page 1-2](#). The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

## Configurable Logic Blocks (CLBs)

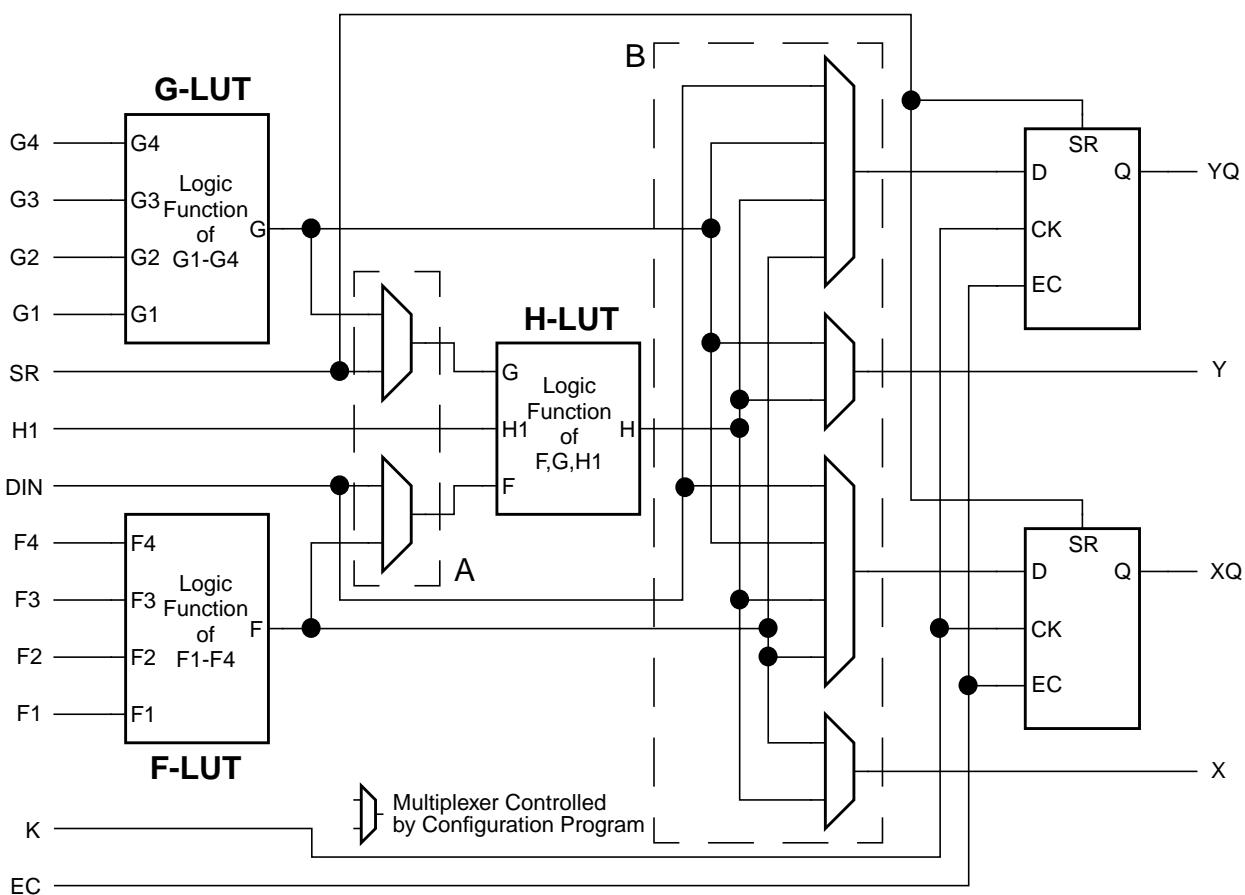
The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in [Figure 2](#).

fied block diagram in [Figure 2](#). There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the “[Advanced Features Description](#)” on page 1-12.

### Function Generators

Two 16x1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box “A” of [Figure 2](#)). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.



**Figure 2: Spartan Simplified CLB Logic Diagram (some features not shown)**

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables<sup>1</sup>
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

### Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see [Figure 2 on page 1-3](#)). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in [“Global Signals: GSR and GTS” on page 1-18](#).

### Latches (SpartanXL only)

The SpartanXL CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in [Table 2](#).

**Table 2: CLB Storage Element Functionality**

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
	/	1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (SpartanXL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X

Don't care

/

Rising edge (clock not inverted)

SR

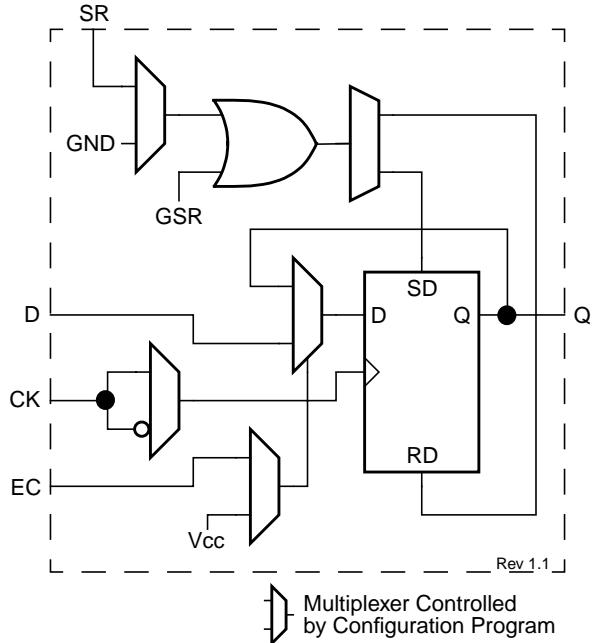
Set or Reset value. Reset is default.

0\*

Input is Low or unconnected (default value)

1\*

Input is High or unconnected (default value)



**Figure 3: CLB Flip-Flop Functional Block Diagram**

### Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in [Figure 3](#)). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

### Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

### Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

## ***CLB Signal Flow Control***

In addition to the H-LUT input control multiplexers (shown in box "A" of [Figure 2 on page 1-3](#)) there are signal flow control multiplexers (shown in box "B" of [Figure 2](#)) which select the signals which drive the flip-flop inputs and the combinatorial CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

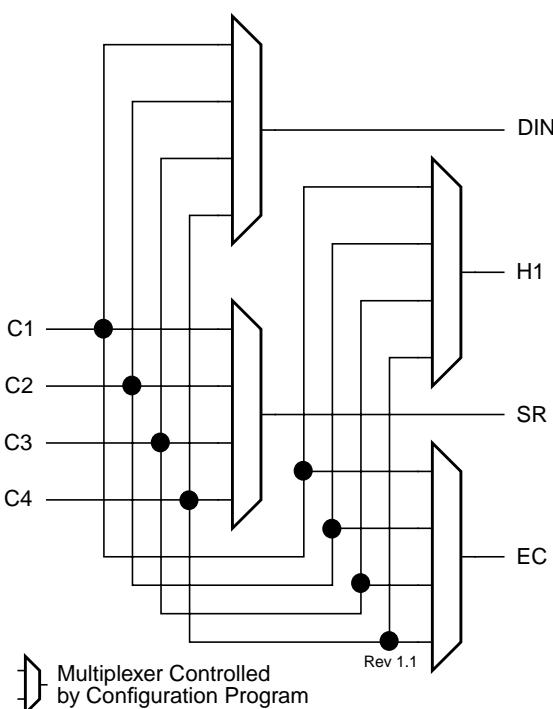
Each combinatorial output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

## Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in [Figure 2](#) and [Figure 4](#)) to be driven from any of the four general control inputs (C1 - C4 in [Figure 4](#)) into the CLB. Any of these inputs can drive any of the four internal control signals.

The four internal control signals are:

- EC - Enable Clock
  - SR - Asynchronous Set/Reset or H function generator Input 0
  - DIN - Direct In or H function generator Input 2
  - H1 - H function generator Input 1.



**Figure 4: CLB Control Signal Interface**

## **Input/Output Blocks (IOBs)**

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 5 on page 1-6 shows a simplified functional block diagram of the Spartan IOB.

## ***IOB Input Signal Path***

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in [Figure 5](#)) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in [Table 3](#), and a simplified block diagram of the register can be seen in [Figure 6](#).

**Table 3: Input Register Functionality**

<b>Mode</b>	<b>CK</b>	<b>EC</b>	<b>D</b>	<b>Q</b>
Power-Up or GSR	X	X	X	SR
Flip-Flop	/	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

**Legend:**

X

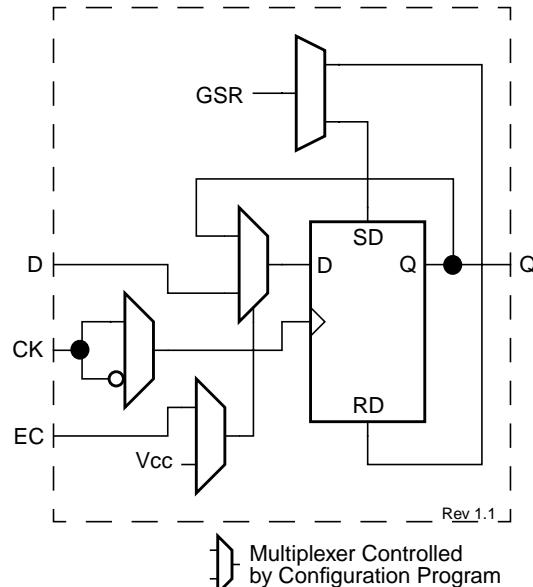
Don't care

CP Rising edge (clock not inverted)  
S1, R1, P1, S2, R2, P2, S3, R3, P3

**SR** Set or Reset value. Reset is default.

- 0\* Input is Low or unconnected (default value)
- 1\* Input is High or unconnected

1\* Input is High or unconnected (default value)



**Figure 6: IOB Flip-Flop/Latch Functional Block Diagram**

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in [Figure 6](#) on the CK line.

The Spartan IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The SpartanXL IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the Spartan global clock buffers. (See “[Global Nets and Buffers](#)” on page 1-11 for a description of the global clock buffers in the Spartan Series.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.

The output of the input register goes to the routing channels (via I1 and I2 in [Figure 5](#)). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan input buffers can be globally configured for either TTL (1.2 V) or CMOS ( $V_{CC}/2$ ) thresholds, using an option in the bitstream generation software. The Spartan output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs

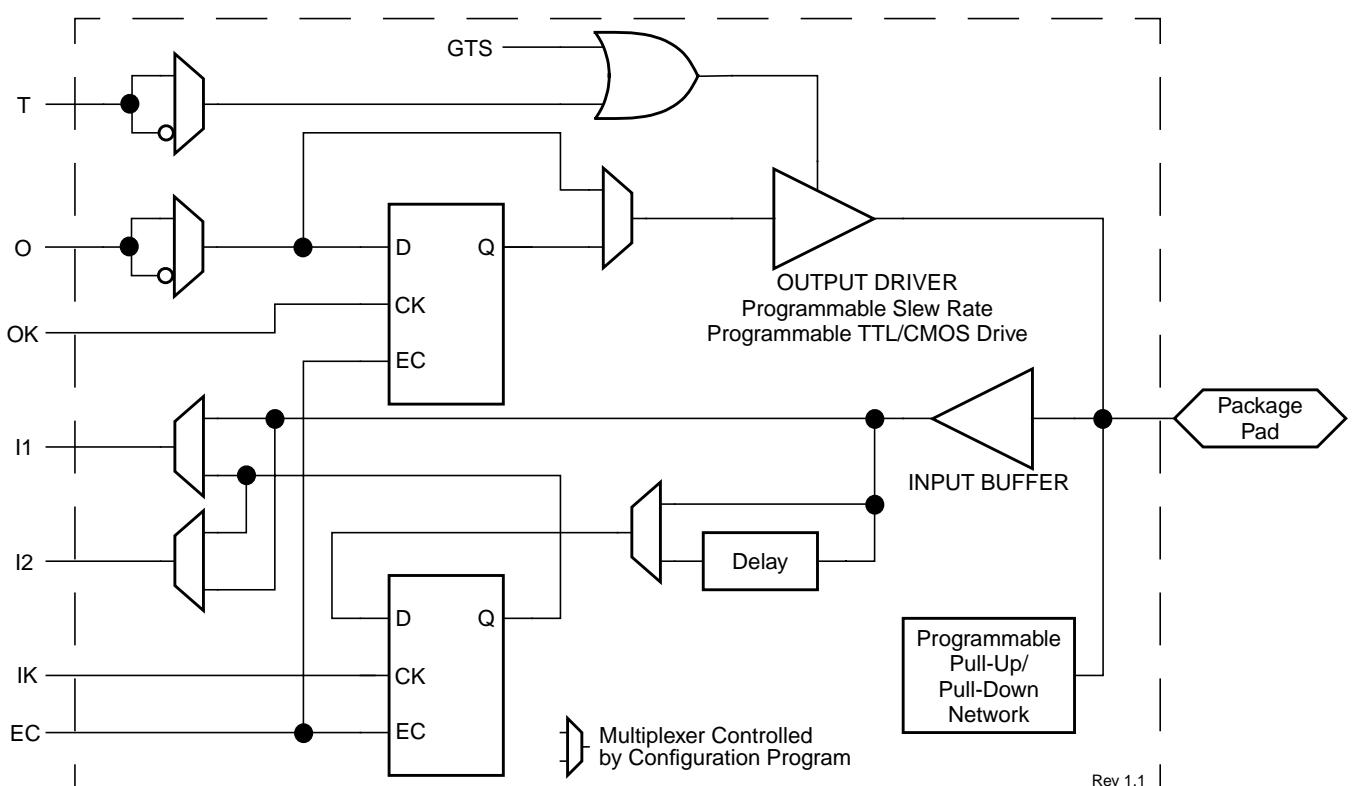
of any 3.3 V device, if the Spartan inputs are in TTL mode. There is a slight input hysteresis of about 300 mV. SpartanXL inputs are TTL compatible and 3.3 V CMOS compatible.

Supported sources for Spartan Series device inputs are shown in [Table 4](#).

SpartanXL I/Os are fully 5V tolerant even though the VCC is 3.3 Volts. This allows 5V signals to directly connect to the SpartanXL inputs without damage, as shown in [Table 4](#). In addition, the 3.3 Volt VCC can be applied before or after 5V signals are applied to the I/Os. This makes the SpartanXL devices immune to power supply sequencing problems.

**Table 4: Supported Sources for Spartan Series Inputs**

Source	Spartan Inputs		SpartanXL Inputs
	5.0 V, TTL	5.0 V, CMOS	3.3 V CMOS
Any device, $V_{CC} = 3.3$ V, CMOS outputs	✓	Unreliable Data	✓
Spartan Series, $V_{CC} = 5$ V, TTL outputs	✓		✓
Any device, $V_{CC} = 5$ V, TTL outputs ( $V_{OH} \leq 3.7$ V)	✓		✓
Any device, $V_{CC} = 5$ V, CMOS outputs	✓	✓	✓ (default mode)



**Figure 5: Simplified Spartan IOB Block Diagram**

**Table 5: I/O Standards Supported by SpartanXL FPGAs**

Signaling Standard	VCC Clamping	Output Drive	V <sub>IH MAX</sub>	V <sub>IH MIN</sub>	V <sub>IL MAX</sub>	V <sub>OH MIN</sub>	V <sub>OL MAX</sub>
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of VCC	30% of VCC	90% of VCC	10% of VCC
LVCMS 3V	OK	12/24 mA	3.6	50% of VCC	30% of VCC	90% of VCC	10% of VCC

### SpartanXL VCC Clamping

SpartanXL FPGAs have an optional clamping diode connected from each I/O to VCC. When enabled they clamp ringing transients back to the 3.3 V supply rail. This clamping action is required in 3.3 V PCI applications. VCC clamping is a global option affecting all I/O pins.

SpartanXL devices are fully 5V TTL I/O compatible if VCC clamping is not enabled. With VCC clamping enabled, the SpartanXL devices will begin to clamp input voltages to one diode voltage drop above VCC. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3 V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

SpartanXL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMS signalling. The various standards are illustrated in [Table 5](#).

### Additional Fast Capture Input Latch (SpartanXL only)

The SpartanXL IOB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active-High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a Transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

### IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in [Table 6](#).

**Table 6: Output Flip-Flop Functionality**

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	<u>—</u> /—	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X  
—/—  
SR  
0\*  
1\*  
Z

Don't care  
Rising edge (clock not inverted)  
Set or Reset value. Reset is default.  
Input is Low or unconnected (default value)  
Input is High or unconnected (default value)  
3-state

### Output Multiplexer/2-Input Function Generator (SpartanXL only)

The output path in the SpartanXL IOB contains an additional multiplexer not available in the Spartan IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad; effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe Driven by a Global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labelled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in [Figure 7](#).

**Figure 7: AND & MUX Symbols in SpartanXL IOB**

### Output Buffer

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see [Figure 5 on page 1-6](#)).

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below Vcc. Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to Vcc. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All SpartanXL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The SpartanXL outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3 V device. (For a detailed discussion of how to interface between 5.0 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.) Supported destinations for Spartan Series device outputs are shown in [Table 7](#).

### Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

**Table 7: Supported Destinations for Spartan Series Outputs**

Destination	SpartanXL Outputs		Spartan Outputs
	3.3 V, CMOS	5.0 V, TTL	5.0 V, CMOS
Any device, Vcc = 3.3 V, CMOS-threshold inputs	√	√	some <sup>1</sup>
Any device, Vcc = 5.0 V, TTL-threshold inputs	√	√	√
Any device, Vcc = 5.0 V, CMOS-threshold inputs	Unreliable Data		√

1. Only if destination device has 5-V tolerant inputs

Spartan Series devices have a feature called “Soft Start-up,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

### Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 kΩ – 100 kΩ ([See “Spartan DC Characteristics Over Operating Conditions” on page 1-34](#)). This high value makes them unsuitable as wired-AND pull-up resistors.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

### Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops ([Figure 6](#)). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

### Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

### Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in [Figure 6](#)), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan Series CLB. It cannot be inverted within the IOB.

## Routing Channel Description

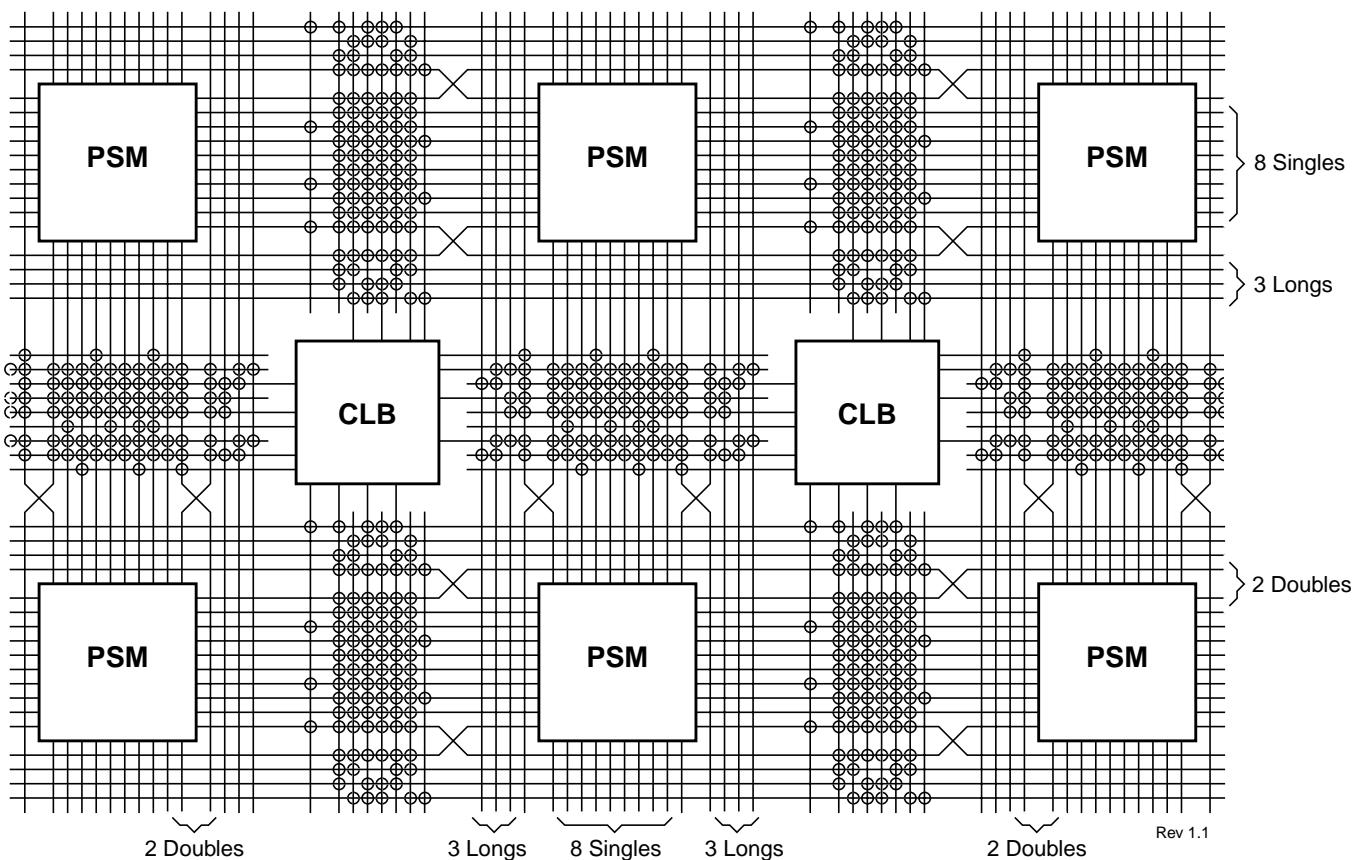
All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan Series devices. **Figure 8** shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the

designer should open a design in the EPIC design editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.



**Figure 8:** Spartan Series CLB Routing Channels and Interface Block Diagram

## CLB Routing Channels

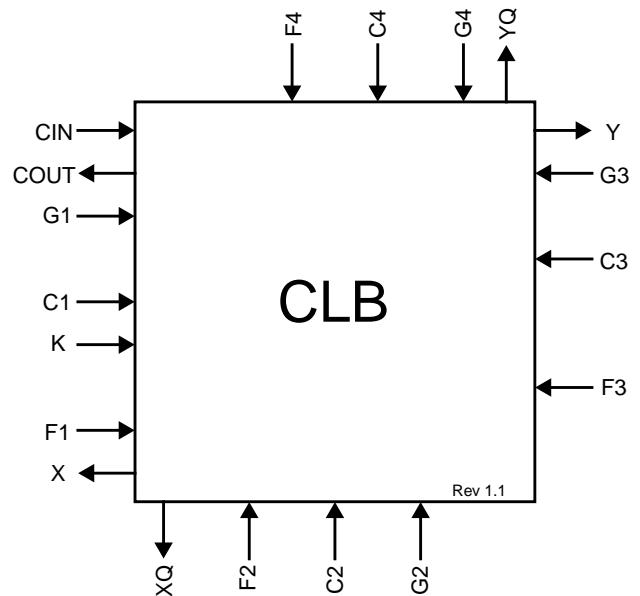
The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). [Figure 8](#) shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.

## CLB Interface

A block diagram of the CLB interface signals is shown in [Figure 9](#). The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as 4 single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.

## Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see [Figure 10](#)).

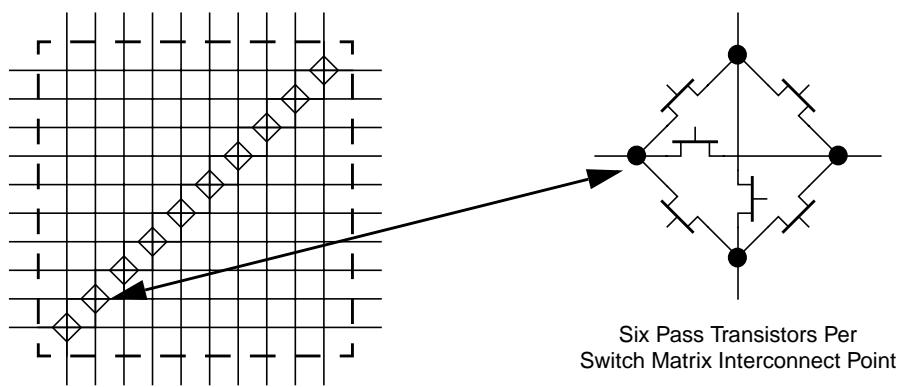


**Figure 9: CLB Interconnect Signals**

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

## Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs.



**Figure 10: Programmable Switch Matrix**

Single-length lines are connected by way of the programmable switch matrices, as shown in [Figure 10](#). Routing connectivity is shown in [Figure 8](#).

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

### Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see [Figure 8](#)).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

### Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan Series longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in [Figure 8](#). The longlines also interface to some 3-state buffers which is described later in “[3-State Long Line Drivers](#)” on [page 1-17](#).

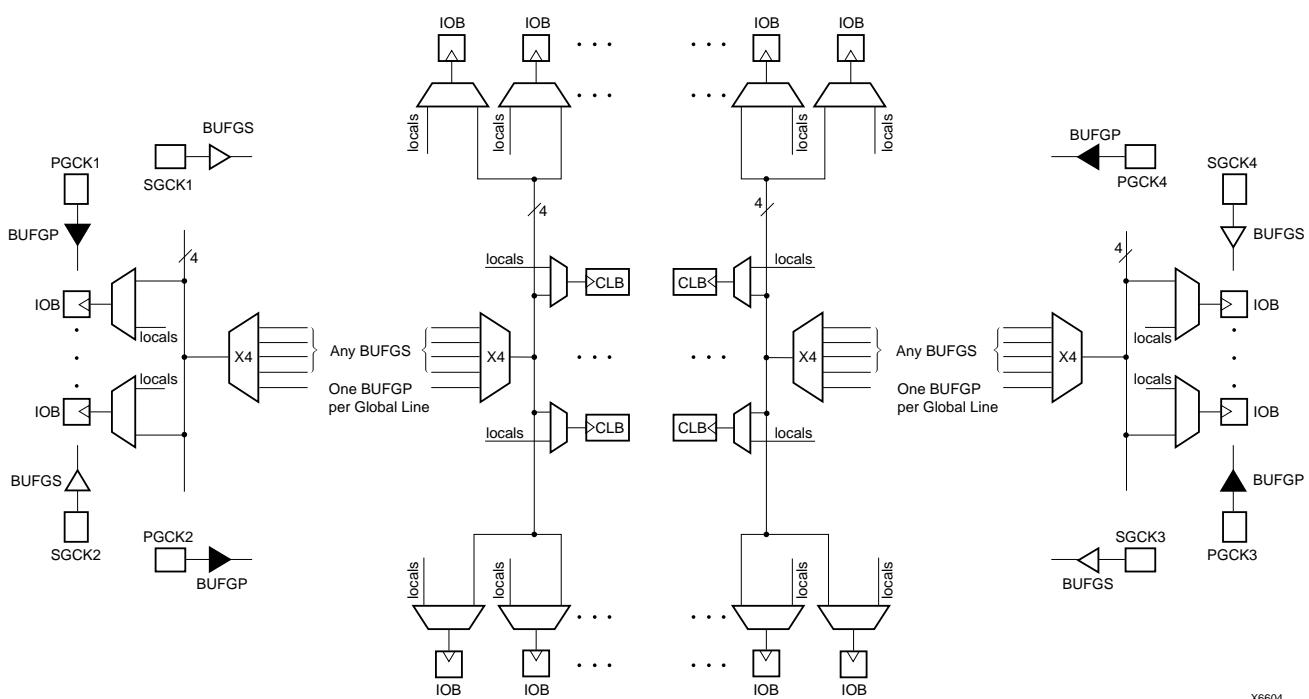
### I/O Routing

Spartan Series devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

### Global Nets and Buffers

The Spartan Series devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in [Figure 11](#). In the 3V SpartanXL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.



X6604

**Figure 11: 5V Spartan Series Global Net Distribution**

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the SpartanXL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The SpartanXL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (SpartanXL global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

## Advanced Features Description

### Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

### Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the Single-Port Mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2 or 32 x 1 RAM array. In the Dual-Port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in [Table 8](#). Any of these possibilities can be individually programmed into a Spartan Series CLB.

- The 16 x 1 Single-Port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 Single-Port configuration combines two 16 x 1 Single Port configurations (each according to the

preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.

- The 32 x 1 Single-Port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The Dual-Port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

**Table 8: CLB Memory Configurations**

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√		

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 Single-Port, the (16 x 1) x 2 Single-Port and the 16 x 1 Dual-Port configurations each use one entire CLB, the 16 x 1 Single-Port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the Dual-Port RAM can transfer twice as much data as the Single-Port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

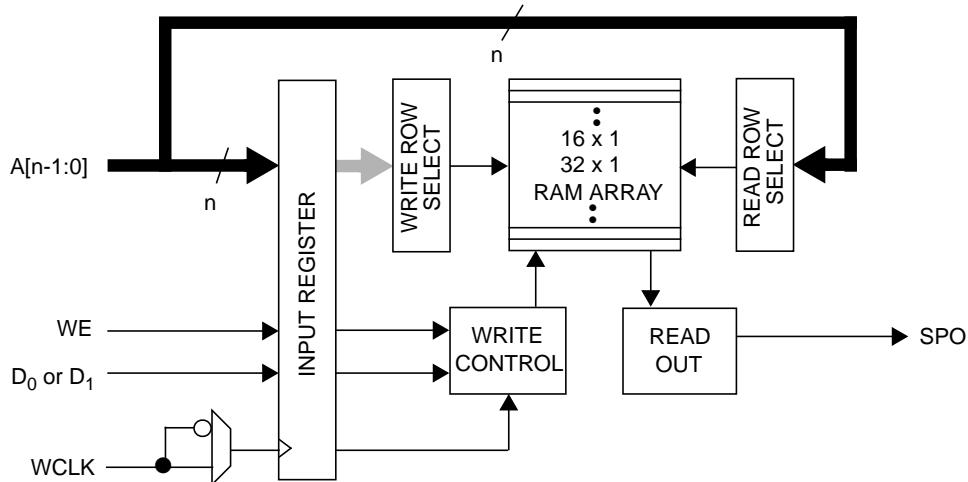
### Single-Port Mode

There are three CLB memory configurations for the Single-Port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in [Figure 12](#).

The Single-Port RAM signals and the CLB signals ([Figure 2 on page 1-3](#)) from which they are originally derived are shown in [Table 9](#).

**Table 9: Single-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN or H <sub>1</sub>
A[3:0]	Address	F <sub>1</sub> -F <sub>4</sub> or G <sub>1</sub> -G <sub>4</sub>
A <sub>4</sub> (32 x 1 only)	Address	H <sub>1</sub>
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F <sub>OUT</sub> or G <sub>OUT</sub>



**Figure 12: Logic Diagram for the Single-Port RAM**

NOTE: 1. The  $(16 \times 1) \times 2$  configuration combines two  $16 \times 1$  Single Port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.  
 2.  $n = 4$  for the  $16 \times 1$  and  $(16 \times 1) \times 2$  configurations.  $n = 5$  for the  $32 \times 1$  configuration.

Writing data to the Single-Port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM's SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

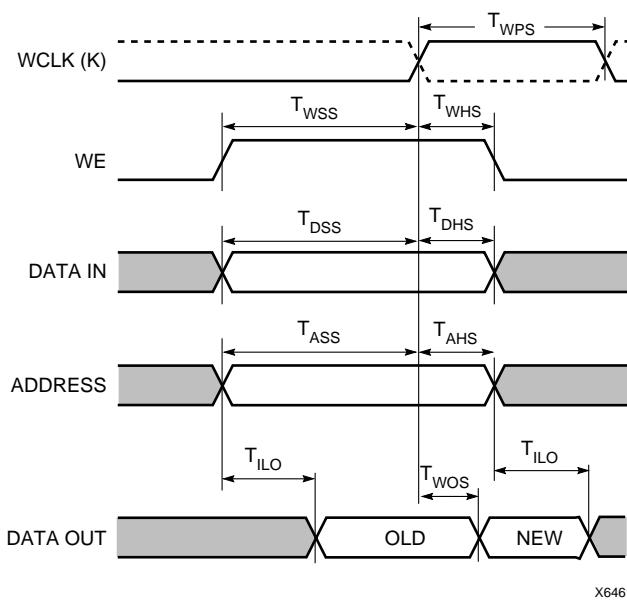
The WE input is active-High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay  $T_{ILO}$ , the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay  $T_{WOS}$ , the new data will appear on SPO.

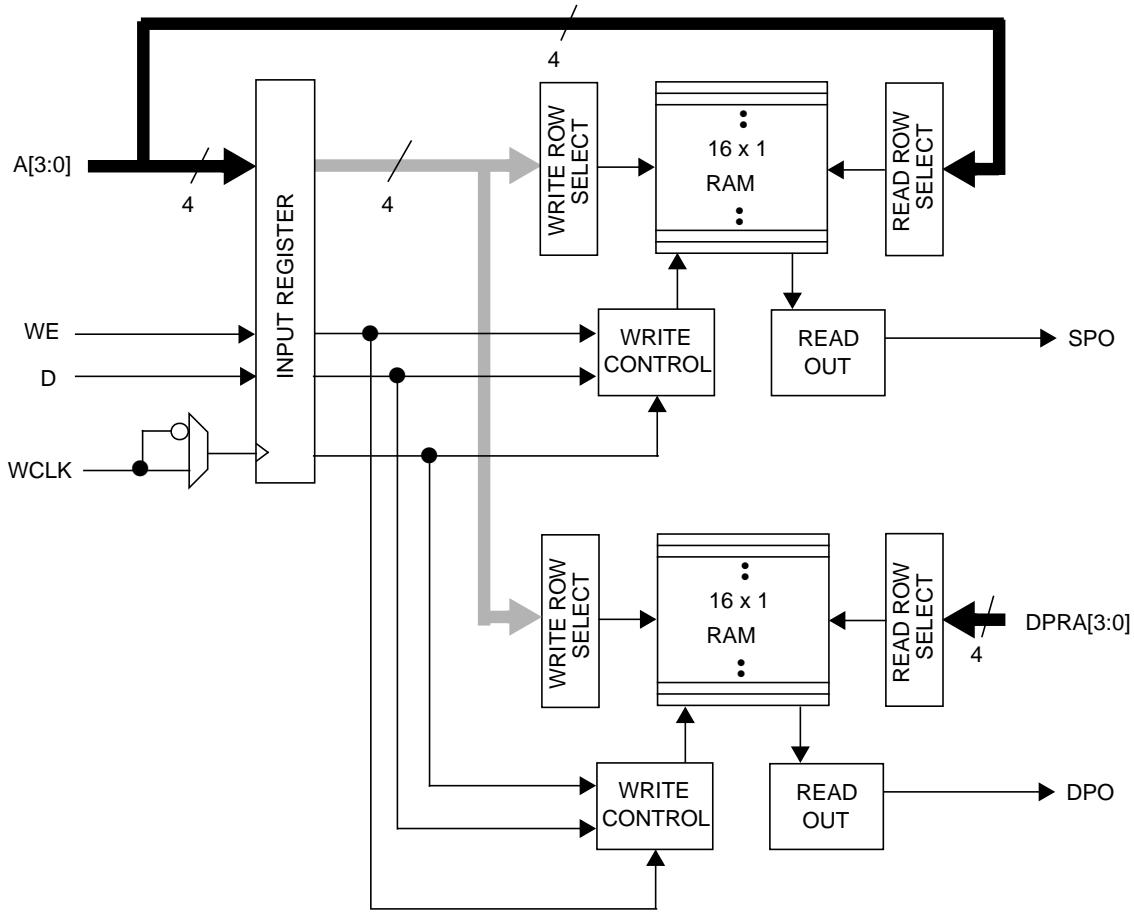
#### Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a  $16 \times 1$  Dual-Port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the  $16 \times 1$  Dual-Port RAM is shown in Figure 14.



**Figure 13: Data Write and Access Timing for RAM**

**Figure 14:** Logic Diagram for the Dual-Port RAM

The Dual-Port RAM signals and the CLB signals from which they are originally derived are shown in [Table 10](#).

**Table 10: Dual-Port RAM Signals**

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F <sub>1</sub> -F <sub>4</sub>
DPRA[3:0]	Read Address for Dual-Port	G <sub>1</sub> -G <sub>4</sub>
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F <sub>OUT</sub>
DPO	Dual Port Out (addressed by DPRA[3:0])	G <sub>OUT</sub>

The RAM16X1D primitive used to instantiate the Dual-Port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 Single-Port RAM array described previously. Single Port Out (SPO) serves as the data output

for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the Dual-Port RAM can provide twice the effective data throughput of a Single-Port RAM alternating read and write operations.

The timing relationships for the Dual-Port RAM mode are shown in [Figure 13](#).

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

## Initializing RAM at FPGA Configuration

Both RAM and ROM implementations of the Spartan Series are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

## More Information on using RAM inside CLBs

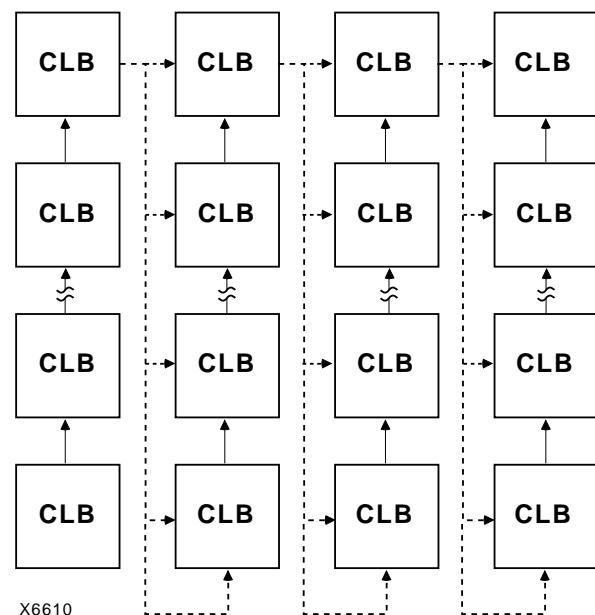
Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "Xilinx Edge-Trig-gered and Dual-Port RAM Capability," "Implementing FIFOs in Xilinx RAM," and "Synchronous and Asynchronous FIFO Designs." All three application notes apply to both the Spartan and the SpartanXL Series.

## Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See [Figure 15](#).)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan Series, speeding up arithmetic and counting functions.



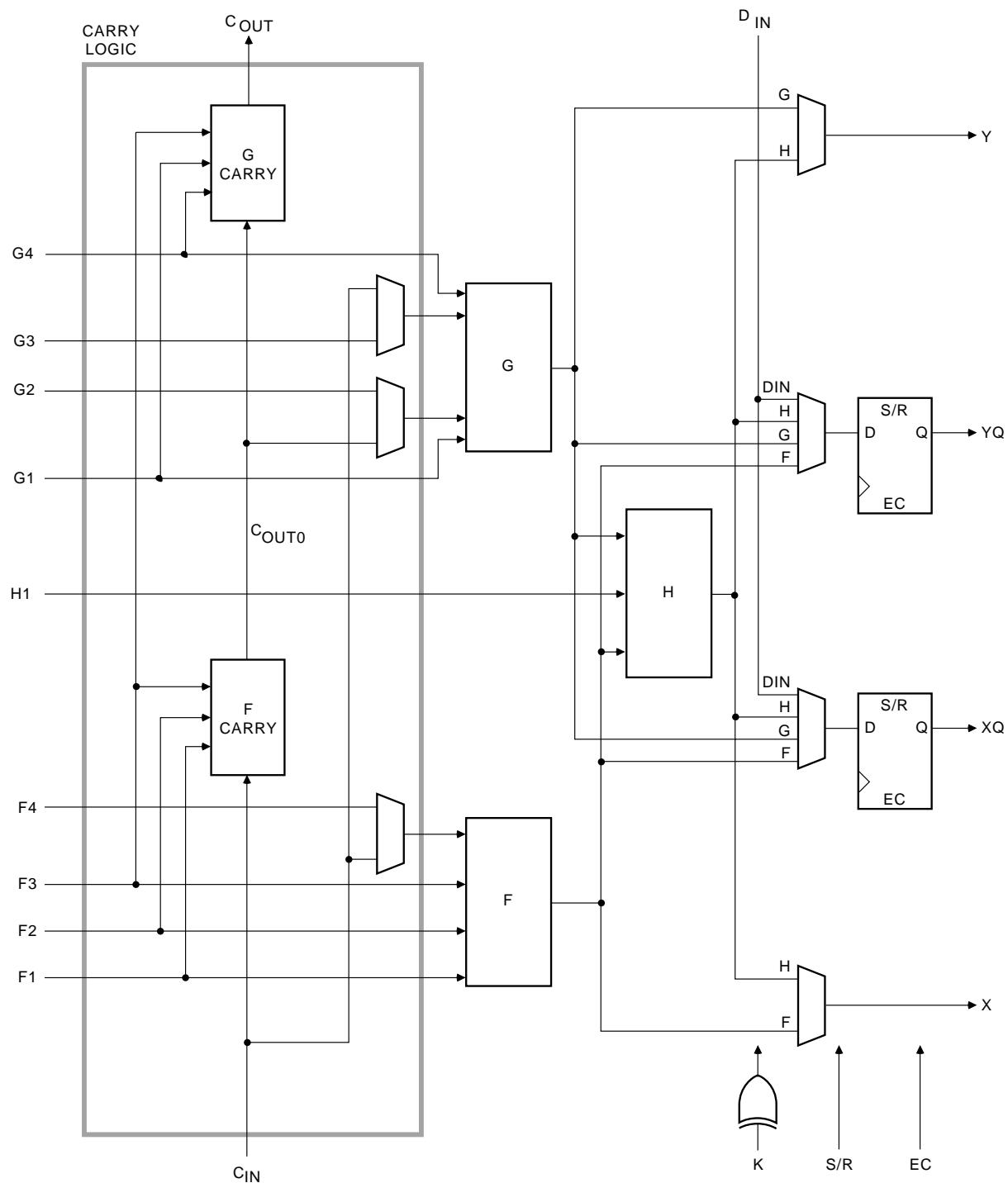
**Figure 15: Available Spartan Carry Propagation Paths**

The carry chain in Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in SpartanXL devices can only run up the column, providing even higher speed.

[Figure 16 on page 1-16](#) shows a Spartan Series CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

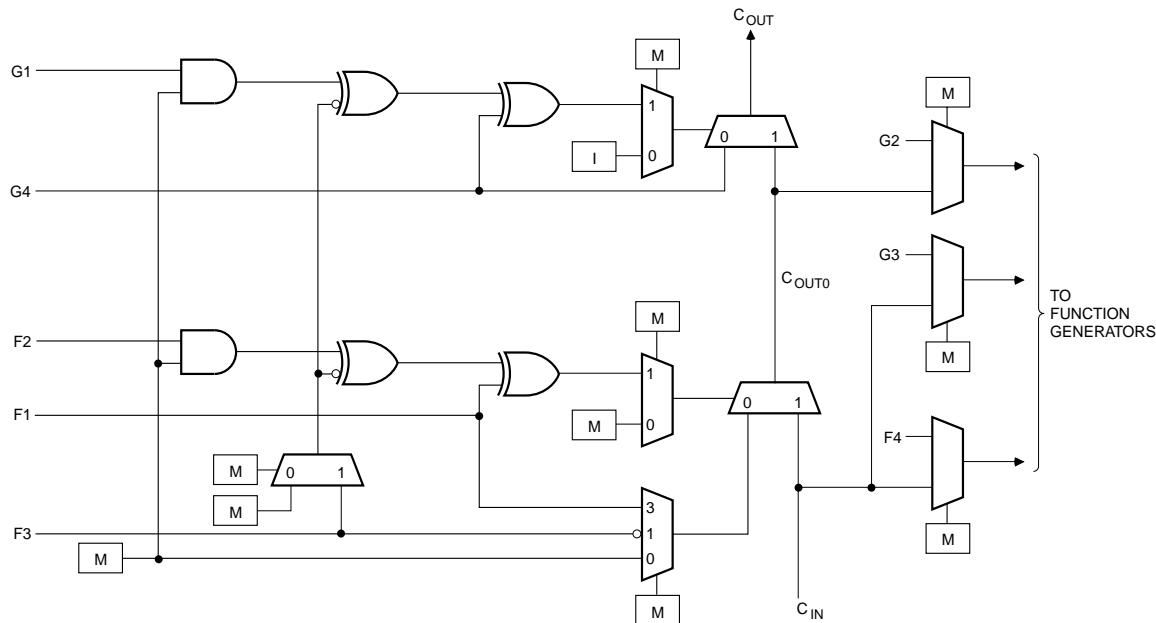
[Figure 17 on page 1-17](#) shows the details of the Spartan carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in [Figure 16](#).

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.



S6699\_01

Figure 16: Fast Carry Logic in Spartan CLB



S2000\_01

**Figure 17: Detail of Spartan Dedicated Carry Logic**

### 3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in [Table 11](#).

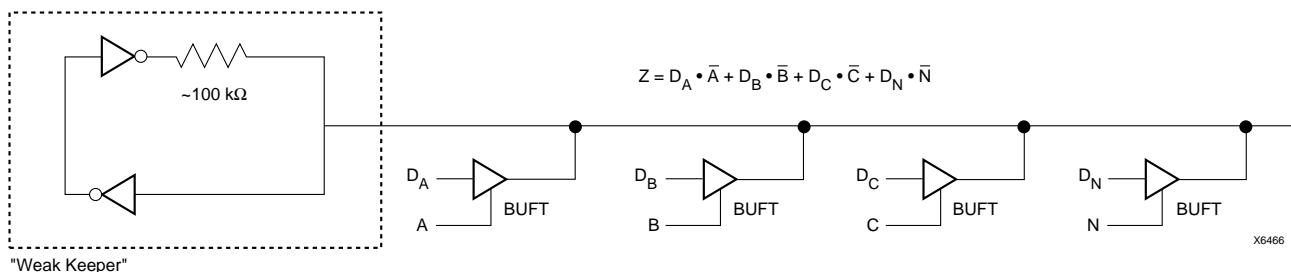
### Three-State Buffer Example

[Figure 18](#) shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active-High 3-state (T) is identical to an active-Low output enable, as shown in [Table 11](#).

**Table 11: Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN



**Figure 18: 3-State Buffers Implement a Multiplexer**

## On-Chip Oscillator

Spartan Series devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, Vcc, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8 MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC symbol is not used in the design.

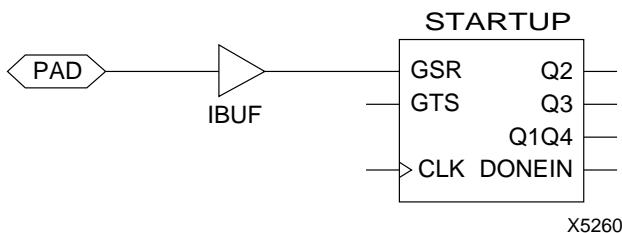
## Global Signals: GSR and GTS

### Global Set/Reset

A separate Global Set/Reset line, as shown in [Figure 3 on page 1-4](#) for the CLB and [Figure 6 on page 1-5](#) for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See [Figure 19](#).) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.



**Figure 19:** Schematic Symbols for Global Set/Reset

### Global 3-State

A separate Global 3-State line (GTS) as shown in [Figure 5 on page 1-6](#) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in [Figure 19](#) for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Alternatively, GTS can be driven from any internal node.

### Boundary Scan

The 'bed of nails' has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan Series implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "Boundary Scan in FPGA Devices."

**Figure 20 on page 1-19** is a diagram of the Spartan Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan Series devices can also be configured through the boundary scan logic. See “[Configuration Through the Boundary Scan Pins](#)” on page 1-30.

### Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

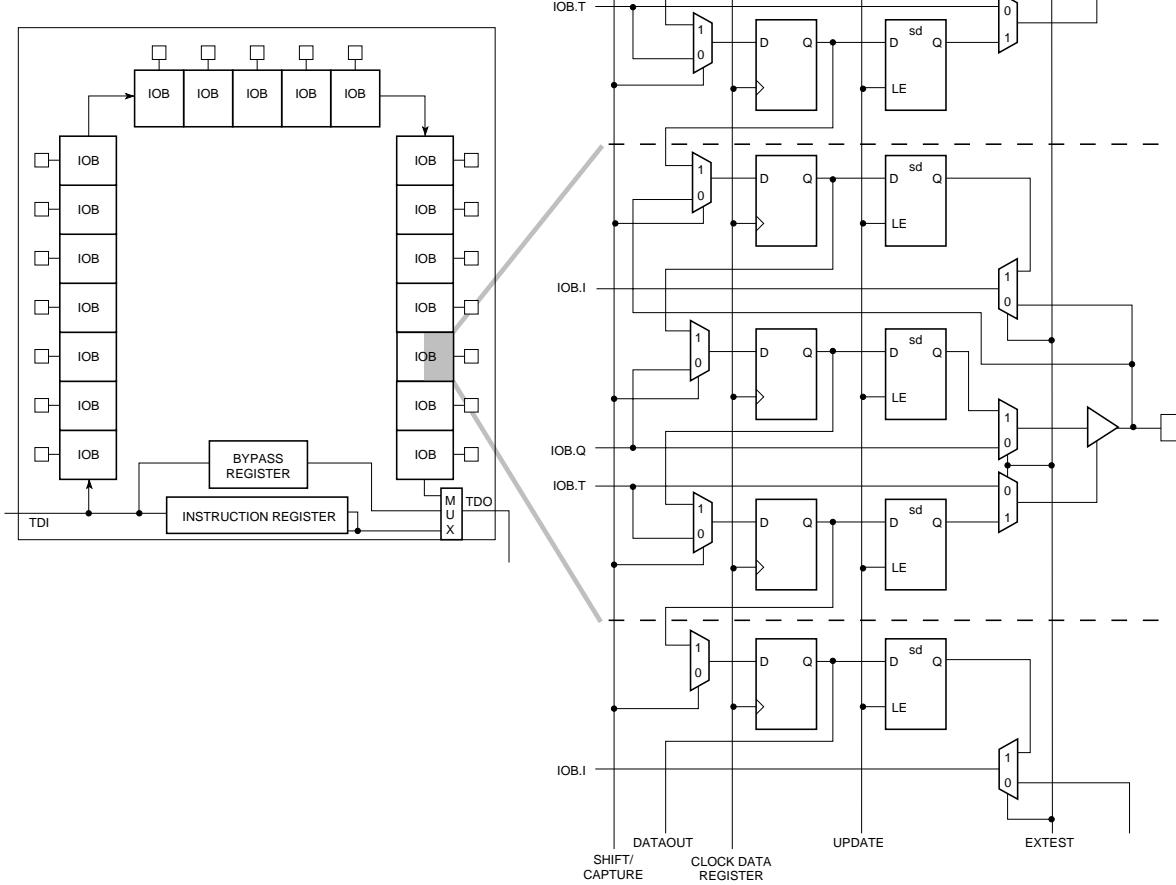
The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

### Instruction Set

The Spartan Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in [Table 12](#).



**Figure 20: Spartan Series Boundary Scan Logic**

**Table 12: Boundary Scan Instructions**

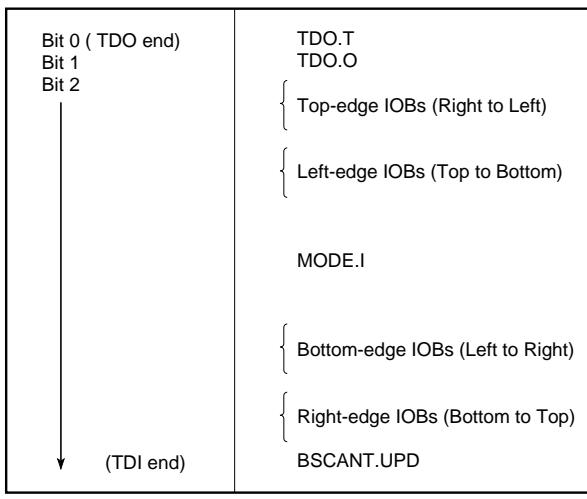
Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

**Bit Sequence**

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in [Figure 21](#). The device-specific pinout tables for the Spartan Series include the boundary scan locations for each IOB pin.

**Figure 21: Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Spartan Series devices are available on the Xilinx web site in the File Download area. Note that the 5V Spartan devices and 3V SpartanXL devices have different BSDL files.

**Including Boundary Scan in a Design**

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in [Figure 22](#).

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

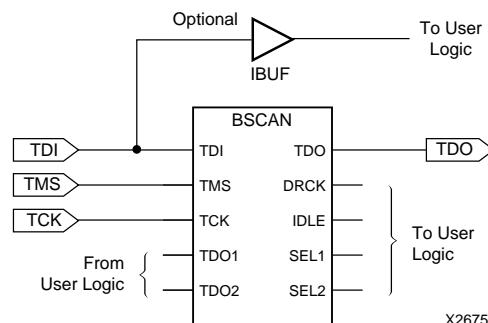
**Avoiding Inadvertent Boundary Scan**

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, “*Boundary Scan in FPGA Devices*.”

**Figure 22: Boundary Scan Schematic Example**

### ***Boundary Scan Enhancements (SpartanXL only)***

SpartanXL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is now supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

## Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

### Configuration Mode Control

5V Spartan Series devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V SpartanXL Series devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See “[Configuration Through the Boundary Scan Pins](#)” on page 1-30).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor of 20 kΩ to 100 kΩ turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in [Table 13](#) and [Table 14](#).

**Table 13: Pin Functions During Configuration (Spartan only)**

CONFIGURATION MODE <MODE Pin>		USER OPERATION
SLAVE SERIAL <High>	MASTER SERIAL <Low>	
MODE (I)	MODE (I)	MODE
HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	I/O
INIT	INIT	I/O
DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes 1. A shaded table cell represents the internal pull-up used before and during configuration.  
 2. (I) represents an input; (O) represents an output.  
 3. INIT is an open-drain output during configuration.

**Table 14: Pin Functions During Configuration (SpartanXL only)**

CONFIGURATION MODE <M1:M0>			USER OPERATION
SLAVE SERIAL <1:1>	MASTER SERIAL <1:0>	EXPRESS <0:X>	
M1(HIGH) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1
M0(HIGH) (I)	M0(LOW) (I)	M0 (I)	M0
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
INIT	INIT	INIT	I/O
DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes 1. A shaded table cell represents the internal pull-up used before and during configuration.  
 2. (I) represents an input; (O) represents an output.  
 3. INIT is an open-drain output during configuration.

## Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

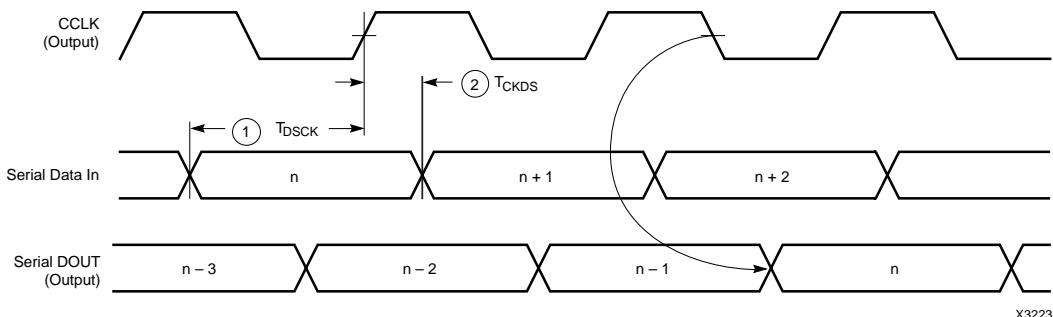
When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the

falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in [Figure 23](#).

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Devices such as XC3000A and XC3100A do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either  $\overline{\text{LDC}}$  or  $\overline{\text{DONE}}$ . Using  $\overline{\text{LDC}}$  avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but  $\overline{\text{LDC}}$  is then restricted to be a permanently High user output after configuration. Using  $\overline{\text{DONE}}$  can also avoid contention on DIN, provided the early  $\overline{\text{DONE}}$  option is invoked.

[Figure 24](#) shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



X3223

	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1	$T_{\text{DSCK}}$	20	ns
	DIN hold	2	$T_{\text{CKDS}}$	0	ns

Notes:

1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

**Figure 23: Master Serial Mode Programming Switching Characteristics**

## Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

[Figure 24](#) shows a full master/slave system. A Spartan Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

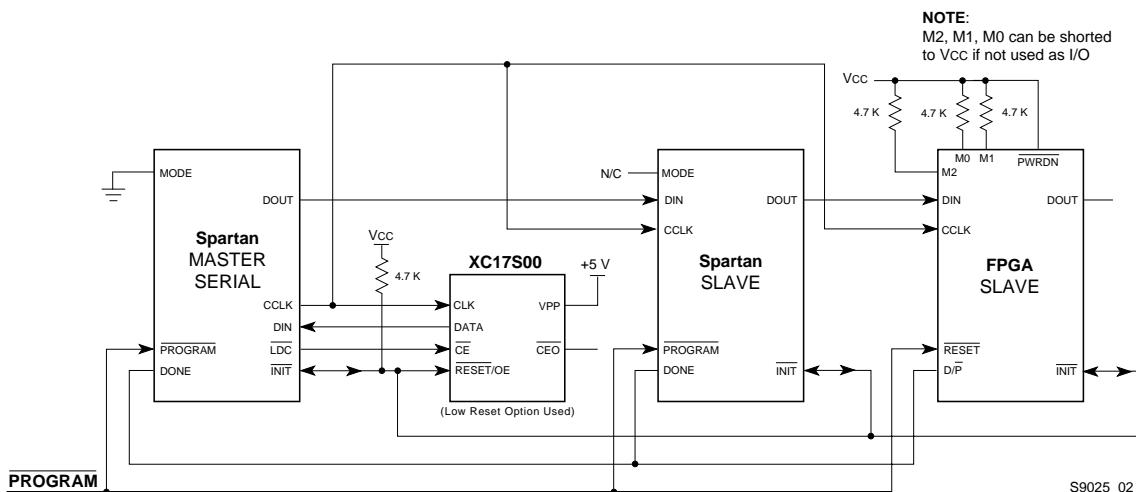
## Serial Daisy Chain

Multiple devices with different configurations can be connected together in a “daisy chain,” and a single combined bitstream used to configure the chain of slave devices.

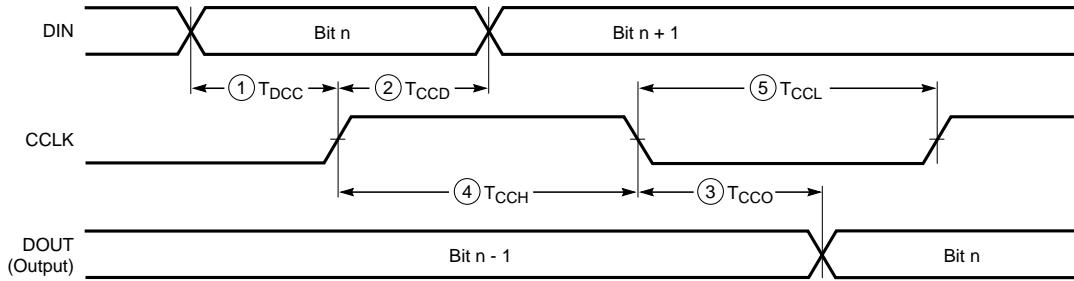
To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in [Figure 24 on page 1-24](#). Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each pass resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.



**Figure 24: Master/Slave Serial Mode Circuit Diagram**



	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1 $T_{DCC}$	20		ns
	DIN hold	2 $T_{CCD}$	0		ns
	DIN to DOUT	3 $T_{cco}$		30	ns
	High time	4 $T_{CCH}$	45		ns
	Low time	5 $T_{CCL}$	45		ns
	Frequency	$F_{cc}$		10	MHz

Note: Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

**Figure 25: Slave Serial Mode Programming Switching Characteristics**

### Express Mode (SpartanXL only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 26). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the BitGen program, which generates the bitstream. The Express mode bitstream is not compatible with the other configuration modes. Express mode is selected by a <0X> on the mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 27).

### Pseudo Daisy Chain

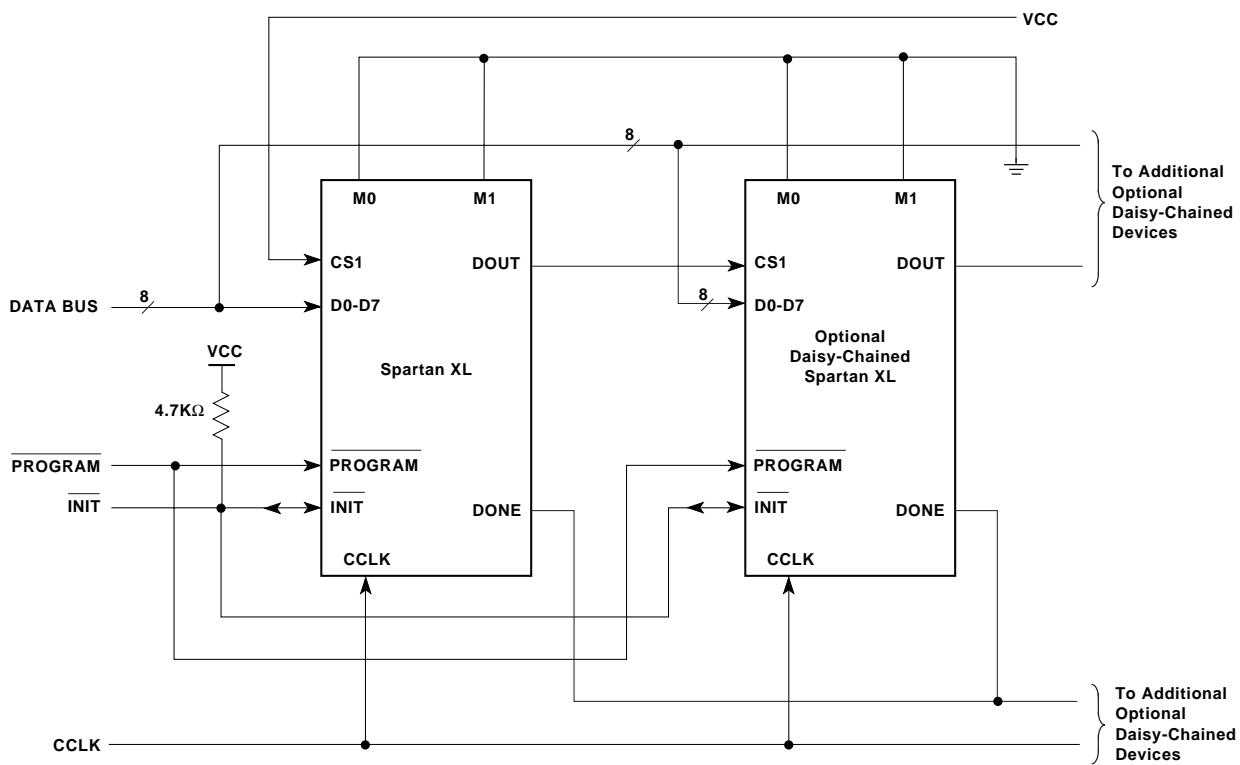
Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. A single combined bitstream is used to configure the chain of Express mode devices. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the

device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). The status pin DOUT is pulled Low two internal-oscillator cycles after INIT is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a BitGen option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All SpartanXL devices in Express mode are synchronized to the DONE pin. User I/O for each device become active after the DONE pin for that device goes High. (The exact timing is determined by BitGen options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured.

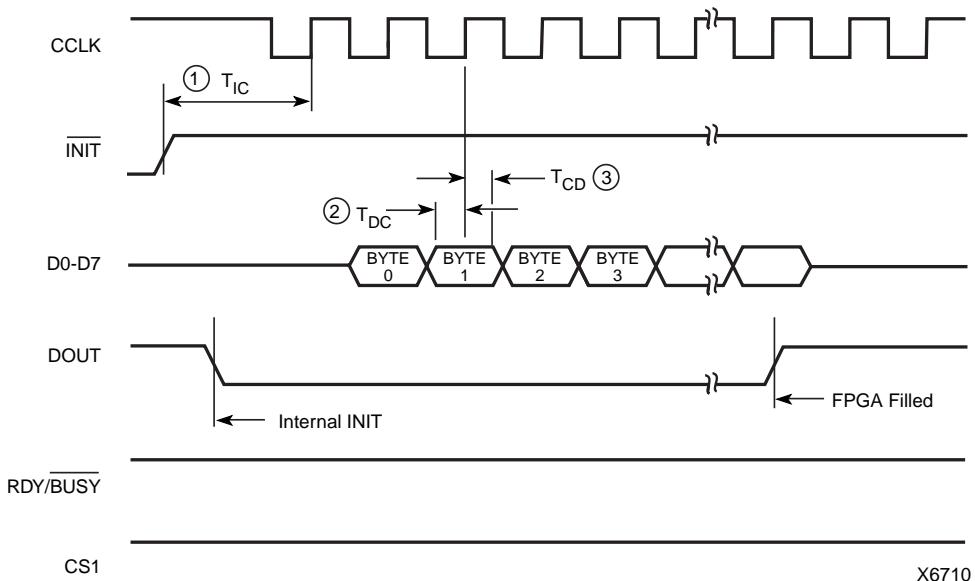
Because only SpartanXL, XC4000XLA/XV, and XC5200 devices support Express mode, only these devices can be used to form an Express mode daisy chain.



X6611\_A

Figure 26: Express Mode Circuit Diagram

	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	$T_{IC}$	5		$\mu s$
	D0 - D7 setup time	$T_{DC}$	20		ns
	D0 - D7 hold time	$T_{CD}$	0		ns
	CCLK High time	$T_{CCH}$	45		ns
	CCLK Low time	$T_{CCL}$	45		ns
	CCLK Frequency	$F_{CC}$	8		MHz
Advance					



Note: If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

**Figure 27: Express Mode Programming Switching Characteristics**

## Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan Series devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan Series devices. The frequency is selected by an option when running the bitstream generation software. Slow mode is the default.

## Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the SpartanXL Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 15. Bit-serial data is read from left to right. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in SpartanXL Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 16). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

**Table 15: Spartan Series Data Stream Formats**

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (SpartanXL only)
Fill Byte	11111111b	11111111b
Preamble Code	0010b	11110010b
Length Count	COUNT(23:0)	FFFFFFh
Fill Bits	1111b	—
Start Field	0b	11010010b
Data Frame	DATA(n-1:0)	DATA(n-1:0)
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	—	FFFFFFFFFFh
Postamble	01111111b	—
Start-Up Bytes	xxh	xxxxxxxxh

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The SpartanXL Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the INIT pin. In Master serial mode, CCLK and address signals continue to operate externally. The user must detect INIT and initialize a new configuration by pulsing the PROGRAM pin Low or cycling Vcc.

### **Cyclic Redundancy Check (CRC) for Configuration and Readback**

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 15. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.

**Table 16: Spartan Program Data**

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
<b>Max System Gates</b>	5,000		10,000		20,000		30,000		40,000	
<b>CLBs (Row x Col.)</b>	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
<b>IOBs</b>	80		112		160		192		224	
<b>Part Number</b>	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
<b>Supply Voltage</b>	5 V	3.3 V								
<b>Bits per Frame</b>	126	127	166	167	226	227	266	267	306	307
<b>Frames</b>	428	429	572	573	788	789	932	933	1,076	1,077
<b>Program Data</b>	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
<b>PROM Size (bits)</b>	53,984	54,544	95,008	95,752	178,144	179,160	247,968	249,168	329,312	330,696
<b>Serial PROM</b>	17S05	17S05XL	17S10	17S10XL	17S20	17S20XL	17S30	17S30XL	17S40	17S40XL

Notes: 1. Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+ 1 for SpartanXL device)

Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for SpartanXL device)

Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits

PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte

2. The user can add more “one” bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra “one” bits, even for extra leading ones at the beginning of the header.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 28. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

## Configuration Sequence

There are four major steps in the Spartan Series power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 29.

### Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic. When Vcc reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable Vcc. When all INIT pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the PROGRAM pin

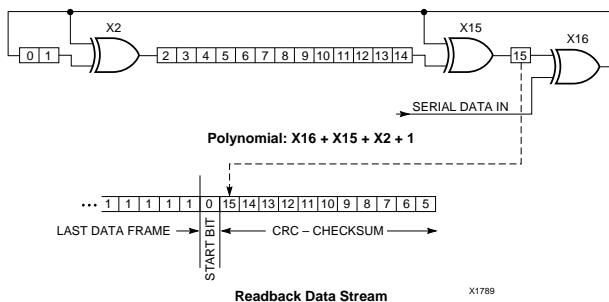


Figure 28: Circuit for Generating CRC-16

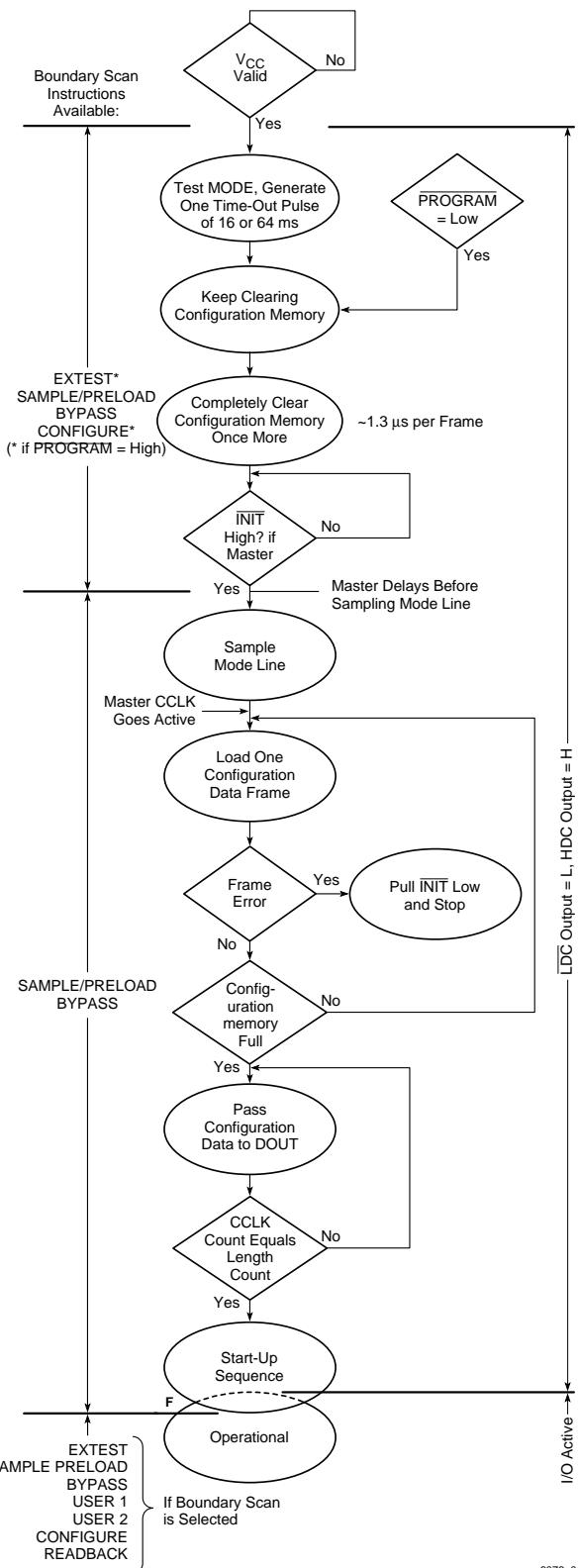


Figure 29: Power-up Configuration Sequence

Low. During this time delay, or as long as the PROGRAM input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the PROGRAM pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the INIT input.

### **Initialization**

During initialization and configuration, user pins HDC, LDC, INIT and DONE provide status outputs for the system interface. The outputs LDC, INIT and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain INIT pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive INIT. Two internal clocks after the INIT pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

### **Configuration**

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In SpartanXL Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain INIT pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In SpartanXL Express mode, when the first device is fully pro-

grammed, DOUT goes High to enable the next device in the chain.

### **Delaying Configuration After Power-Up**

There are two methods of delaying configuration after power-up: put a logic Low on the PROGRAM input, or pull the bidirectional INIT pin Low, using an open-collector (open-drain) driver. (See [Figure 29 on page 1-29](#).)

A Low on the PROGRAM input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as PROGRAM is Low, the FPGA keeps clearing its configuration memory. When PROGRAM goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the PROGRAM input automatically forces a Low on the INIT output. The Spartan Series PROGRAM pin has a permanent weak pull-up.

Using an open-collector or open-drain driver to hold INIT Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When INIT is no longer held Low externally, the device determines its configuration mode by capturing the state of the MODE pin, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that INIT is High.

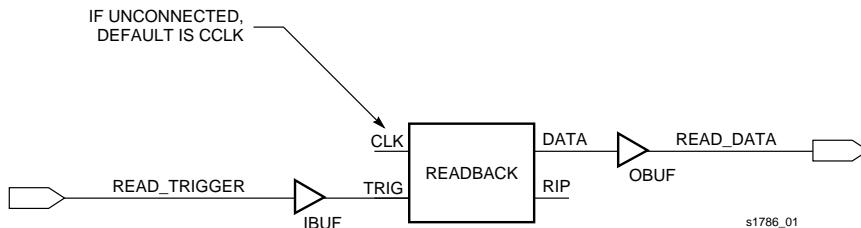
### **Configuration Through the Boundary Scan Pins**

Spartan Series devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.
- Issue the CONFIG command to the TMS input
- Wait for INIT to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and SpartanXL devices.



**Figure 30: Readback Schematic Example**

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Readback of SpartanXL Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in [Figure 30](#).

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

## Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

### Readback Capture

When the Readback Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-

flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

### Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

### Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

### Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts

before frame boundaries. Frame lengths and data formats are listed in [Table 15](#) and [Table 16](#).

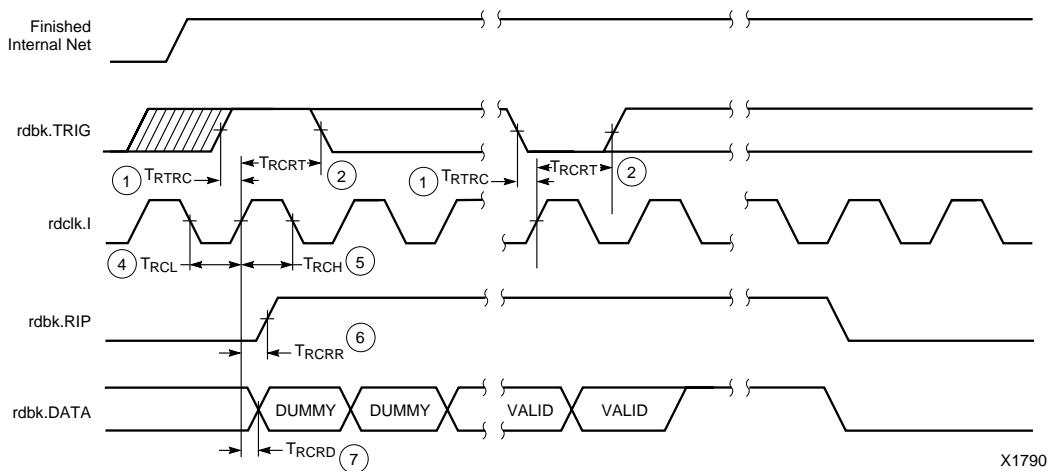
### **Readback with the XChecker Cable**

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the computer screen, acting as a low-cost in-circuit emulator.

### **Spartan Program Readback Switching Characteristic Guidelines**

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



### **Spartan and SpartanXL Readback**

	Description	Symbol	Min	Max	Units	
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	$T_{RTRC}$	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	$T_{RCRT}$	50	-	ns
rdclk.1	rdbk.DATA delay	7	$T_{RCRD}$	-	250	ns
	rdbk.RIP delay	6	$T_{RCRR}$	-	250	ns
	High time	5	$T_{RCH}$	250	500	ns
	Low time	4	$T_{RCL}$	250	500	ns

Note 1: Timing parameters apply to all speed grades.

Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

## Spartan Detailed Specifications

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

### Spartan Absolute Maximum Ratings<sup>1</sup>

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage relative to GND (Note 2, 3)	-0.5 to $V_{CC}$ +0.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 2, 3)	-0.5 to $V_{CC}$ +0.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	Plastic packages +125	°C

- Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- 2: Maximum DC overshoot (above  $V_{CC}$ ) or undershoot (below GND) must be limited to either 0.5 V or 10 mA, whichever is easier to achieve.
- 3: Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

### Spartan Recommended Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_J$ = 0°C to +85°C	Commercial 4.75	5.25	V
	Supply voltage relative to GND, $T_J$ = -40°C to +100°C	Industrial 4.5	5.5	V
$V_{IH}$	High-level input voltage	TTL inputs 2.0	$V_{CC}$	V
		CMOS inputs 70%	100%	$V_{CC}$
$V_{IL}$	Low-level input voltage	TTL inputs 0	0.8	V
		CMOS inputs 0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns

Note 1: At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output Measurement thresholds are: 1.5 V for TTL and 2.5 V for CMOS.

## Spartan DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0\text{mA}$ , $V_{CC}$ min	TTL outputs	2.4		V
	High-level output voltage @ $I_{OH} = -1.0\text{mA}$ , $V_{CC}$ min	CMOS outputs	$V_{CC}-0.5$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0\text{mA}$ , $V_{CC}$ min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
$I_L$	Input or output leakage current		-10	+10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample tested)			10	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ (sample tested)		0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{IN} = 5\text{V}$ (sample tested)		0.02		mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.

Note 2: With no output current loads, no active input pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a Tie option.

## Spartan Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Device	Speed Grade		Units
			-3	-4	
From pad through Primary buffer, to any clock K	$T_{PG}$	XCS05	4.0	2.0	ns
		XCS10	4.3	2.4	ns
		XCS20	5.4	2.8	ns
		XCS30	5.8	3.2	ns
		XCS40	6.4	3.5	ns
From pad through Secondary buffer, to any clock K	$T_{SG}$	XCS05	4.4	2.5	ns
		XCS10	4.7	2.9	ns
		XCS20	5.8	3.3	ns
		XCS30	6.2	3.6	ns
		XCS40	6.7	3.9	ns

Preliminary

## Spartan CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Description	Symbol	Speed Grade		-3		-4		Units
		Min	Max	Min	Max	Min	Max	
<b>Clocks</b>								
Clock High time	$T_{CH}$	4.0		3.0				ns
Clock Low time	$T_{CL}$	4.0		3.0				ns
<b>Combinatorial Delays</b>								
F/G inputs to X/Y outputs	$T_{ILO}$		1.6			1.2		ns
F/G inputs via H to X/Y outputs	$T_{IHO}$		2.7			2.0		ns
C inputs via H1 via H to X/Y outputs	$T_{HH1O}$		2.2			1.7		ns
<b>CLB Fast Carry Logic</b>								
Operand inputs (F1, F2, G1, G4) to $C_{OUT}$	$T_{OPCY}$		2.1			1.7		ns
Add/Subtract input (F3) to $C_{OUT}$	$T_{ASCY}$		3.7			2.8		ns
Initialization inputs (F1, F3) to $C_{OUT}$	$T_{INCY}$		1.4			1.2		ns
$C_{IN}$ through function generators to X/Y outputs	$T_{SUM}$		2.6			2.0		ns
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$		0.6			0.5		ns
<b>Sequential Delays</b>								
Clock K to Flip-Flop outputs Q	$T_{CKO}$		2.8			2.1		ns
<b>Setup Time before Clock K</b>								
F/G inputs	$T_{ICK}$	2.4		1.8				ns
F/G inputs via H	$T_{IHCK}$	3.9		2.9				ns
C inputs via H1 through H	$T_{HH1CK}$	3.3		2.3				ns
C inputs via DIN	$T_{DICK}$	2.0		1.3				ns
C inputs via EC	$T_{ECCK}$	2.6		2.0				ns
C inputs via S/R, going Low (inactive)	$T_{RCK}$	4.0		2.5				ns
<b>Hold Time after Clock K</b>								
All Hold times, all devices		0.0		0.0				ns
<b>Set/Reset Direct</b>								
Width (High)	$T_{RPW}$	4.0		3.0				ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		4.0			3.0		ns
<b>Global Set/Reset</b>								
Minimum GSR Pulse Width	$T_{MRW}$	13.5		11.5				ns
Delay from GSR input to any Q	$T_{MRQ}$	See page 1-40 for $T_{RR}$ values per device.						
<b>Toggle Frequency (MHz)</b> (for export control purposes)	$F_{TOG}$		125			166		MHz
Preliminary								

## Spartan CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-3		-4		Units
	Size	Symbol	Min	Max	Min	Max	
<b>Write Operation</b>							
Address write cycle time (clock K period)	16x2 32x1	T <sub>WC</sub> S T <sub>WCT</sub> S	11.6 11.6		8.0 8.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T <sub>WP</sub> S T <sub>WPT</sub> S	5.8 5.8		4.0 4.0		ns ns
Address setup time before clock K	16x2 32x1	T <sub>A</sub> SS T <sub>A</sub> STS	2.0 2.0		1.5 1.5		ns ns
Address hold time after clock K	16x2 32x1	T <sub>A</sub> HS T <sub>A</sub> HTS	0.0 0.0		0.0 0.0		ns ns
DIN setup time before clock K	16x2 32x1	T <sub>D</sub> SS T <sub>D</sub> STS	2.7 1.7		1.5 1.5		ns ns
DIN hold time after clock K	16x2 32x1	T <sub>D</sub> HS T <sub>D</sub> HTS	0.0 0.0		0.0 0.0		ns ns
WE setup time before clock K	16x2 32x1	T <sub>W</sub> SS T <sub>W</sub> STS	1.6 1.6		1.5 1.5		ns ns
WE hold time after clock K	16x2 32x1	T <sub>W</sub> HS T <sub>W</sub> HTS	0.0 0.0		0.0 0.0		ns ns
Data valid after clock K	16x2 32x1	T <sub>W</sub> OS T <sub>W</sub> OTS		7.9 9.3		6.5 7.0	ns ns
<b>Read Operation</b>							
Address read cycle time	16x2 32x1	T <sub>R</sub> C T <sub>R</sub> CT	2.6 3.8		2.6 3.8		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T <sub>I</sub> LO T <sub>I</sub> HO		1.6 2.7		1.2 2.0	ns ns
Address setup time before clock K	16x2 32x1	T <sub>I</sub> CK T <sub>I</sub> HCK	2.4 3.9		1.8 2.9		ns ns
Preliminary							

Note: Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

## Spartan CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

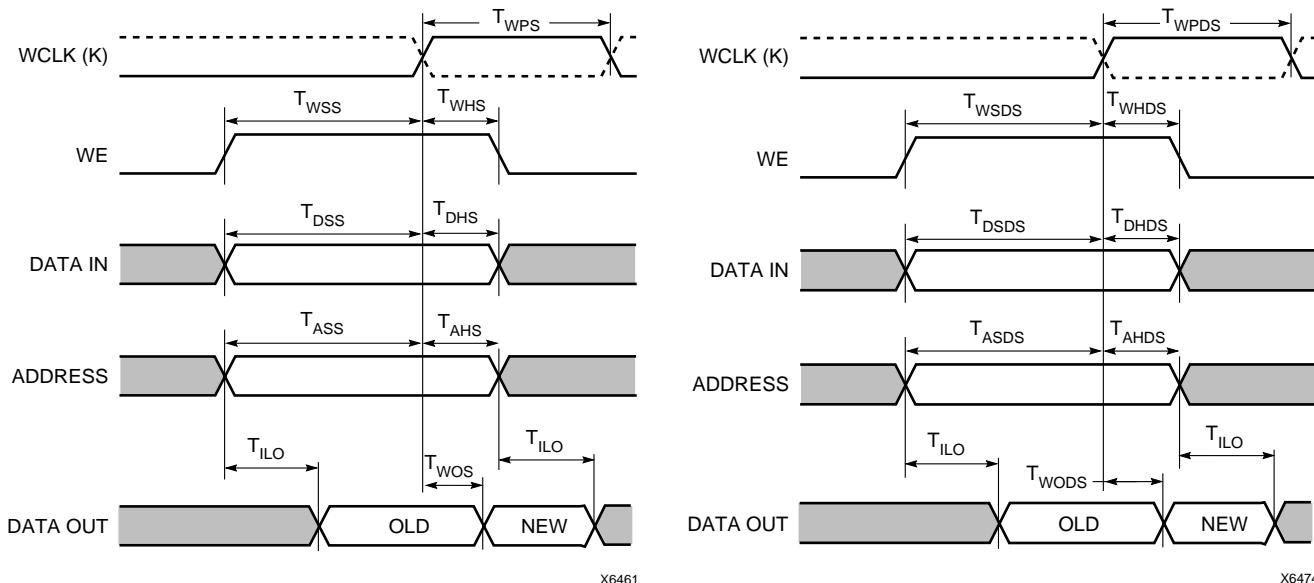
Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Dual Port RAM	Speed Grade		-3		-4		Units
	Size	Symbol	Min	Max	Min	Max	
<b>Write Operation</b>							
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	11.6		8.0		ns
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	5.8		4.0		ns
Address setup time before clock K	16x1	$T_{ASDS}$	2.1		1.5		ns
Address hold time after clock K	16x1	$T_{AHDS}$	0.0		0.0		ns
DIN setup time before clock K	16x1	$T_{DSDS}$	1.6		1.5		ns
DIN hold time after clock K	16x1	$T_{DHDS}$	0.0		0.0		ns
WE setup time before clock K	16x1	$T_{WSDS}$	1.6		1.5		ns
WE hold time after clock K	16x1	$T_{WHDS}$	0.0		0.0		ns
Data valid after clock K	16x1	$T_{WODS}$		7.0		6.5	ns

Preliminary

Note 1: Read Operation Timing for 16x1 dual-port RAM option is identical to 16x2 single-port RAM timing.

## Spartan CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port

Dual Port

## Spartan Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

### Spartan Output Flip-Flop, Clock-to-Out

Speed Grade			-3	-4	Units
Description	Symbol	Device	Max	Max	
Global Primary Clock to TTL Output using OFF					
<b>Fast</b>	T <sub>ICKOF</sub>	XCS05	8.7	5.3	ns
		XCS10	9.1	5.7	ns
		XCS20	9.3	6.1	ns
		XCS30	9.4	6.5	ns
		XCS40	10.2	6.8	ns
<b>Slew-rate limited</b>	T <sub>ICKO</sub>	XCS05	11.5	9.0	ns
		XCS10	12.0	9.4	ns
		XCS20	12.2	9.8	ns
		XCS30	12.8	10.2	ns
		XCS40	12.8	10.5	ns
Global Secondary Clock to TTL Output using OFF					
<b>Fast</b>	T <sub>ICKSOF</sub>	XCS05	9.2	5.8	ns
		XCS10	9.6	6.2	ns
		XCS20	9.8	6.6	ns
		XCS30	9.9	7.0	ns
		XCS40	10.7	7.3	ns
<b>Slew-rate limited</b>	T <sub>ICKSO</sub>	XCS05	12.0	9.5	ns
		XCS10	12.5	9.9	ns
		XCS20	12.7	10.3	ns
		XCS30	13.2	10.7	ns
		XCS40	14.3	11.0	ns
Delay Adder for CMOS Outputs Option					
<b>Fast</b>	T <sub>CMOSOF</sub>	All devices	1.0	0.8	ns
<b>Slew-rate Limited</b>	T <sub>CMOSO</sub>	All devices	2.0	1.5	ns
Preliminary					

OFF = Output Flip-Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load. For different loads, see [Figure 28](#).

### Capacitive Load Factor

[Figure 28](#) shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. [Figure 28](#) is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

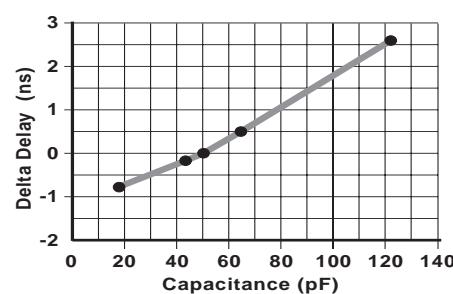


Figure 28: Delay Factor at Various Capacitive Loads

## Spartan Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### Spartan Primary and Secondary Setup and Hold

Speed Grade			-3	-4	Units
Description	Symbol	Device	Min	Min	
Input Setup/Hold Times Using Primary Clock and IFF					
<b>No Delay</b>	$T_{PSUF}/T_{PHF}$	XCS05	1.8 / 2.5	1.2 / 1.7	ns
		XCS10	1.5 / 3.4	1.0 / 2.3	ns
		XCS20	1.2 / 4.0	0.8 / 2.7	ns
		XCS30	0.9 / 4.5	0.6 / 3.0	ns
		XCS40	0.6 / 5.2	0.4 / 3.5	ns
<b>With Delay</b>	$T_{PSU}/T_{PH}$	XCS05	6.0 / 0.0	4.3 / 0.0	ns
		XCS10	6.0 / 0.0	4.3 / 0.0	ns
		XCS20	6.0 / 0.0	4.3 / 0.0	ns
		XCS30	6.0 / 0.0	4.3 / 0.0	ns
		XCS40	6.8 / 0.0	5.3 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
<b>No Delay</b>	$T_{SSUF}/T_{SHF}$	XCS05	1.5 / 3.0	0.9 / 2.2	ns
		XCS10	1.2 / 3.9	0.7 / 2.8	ns
		XCS20	0.9 / 4.5	0.5 / 3.2	ns
		XCS30	0.6 / 5.0	0.3 / 3.5	ns
		XCS40	0.3 / 5.7	0.1 / 4.0	ns
<b>With Delay</b>	$T_{SSU}/T_{SH}$	XCS05	5.7 / 0.0	4.0 / 0.0	ns
		XCS10	5.7 / 0.0	4.0 / 0.0	ns
		XCS20	5.7 / 0.5	4.0 / 0.5	ns
		XCS30	5.7 / 0.5	4.0 / 0.5	ns
		XCS40	6.5 / 0.0	5.0 / 0.0	ns

IFF = Input Flip-Flop or Latch

Preliminary

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

## Spartan IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Symbol	Device	Speed Grade		-3		-4		Units
			Min	Max	Min	Max	Min	Max	
<b>Setup Times - TTL Inputs (Note 1)</b>									
Clock Enable (EC) to Clock (IK), no delay	$T_{ECIK}$	All devices	2.1		1.6				ns
Pad to Clock (IK), no delay	$T_{PICK}$	All devices	2.0		1.5				ns
<b>Hold Times</b>									
Clock Enable (EC) to Clock (IK), no delay	$T_{IKEC}$	All devices	0.9		0.0				ns
All Other Hold Times		All devices	0.0		0.0				ns
<b>Propagation Delays - TTL Inputs (Note 1)</b>									
Pad to I1, I2	$T_{PID}$	All devices		2.0			1.5		ns
Pad to I1, I2 via transparent input latch, no delay	$T_{PLI}$	All devices		3.6			2.8		ns
Clock (IK) to I1, I2 (flip-flop)	$T_{IKRI}$	All devices		2.8			2.7		ns
Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKLI}$	All devices		3.9			3.2		ns
<b>Delay Adder for Input with Delay Option</b>									
$T_{ECIKD} = T_{ECIK} + T_{Delay}$	$T_{Delay}$	XCS05	4.0		3.6				ns
$T_{PICKD} = T_{PICK} + T_{Delay}$		XCS10	4.1		3.7				ns
$T_{PDLI} = T_{PLI} + T_{Delay}$		XCS20	4.2		3.8				ns
		XCS30	5.0		4.5				ns
		XCS40	5.5		5.5				ns
<b>Global Set/Reset</b>									
Minimum GSR Pulse Width	$T_{MRW}$	All devices	13.5		11.5				ns
Delay from GSR input to any Q	$T_{RRI}$	XCS05	11.3		9.0				ns
		XCS10	11.9		9.5				ns
		XCS20	12.5		10.0				ns
		XCS30	13.1		10.5				ns
		XCS40	13.8		11.0				ns
<b>Preliminary</b>									

Note 1: Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.

Note 2: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## Spartan IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Description	Symbol	Device	-3		-4		Units
			Min	Max	Min	Max	
<b>Clocks</b>							
Clock High	$T_{CH}$	All devices	4.0		3.0		ns
Clock Low	$T_{CL}$	All devices	4.0		3.0		ns
<b>Propagation Delays - TTL Outputs (Notes 1, 2)</b>							
Clock (OK) to Pad, fast	$T_{OKPOF}$	All devices		4.5		3.3	ns
Clock (OK) to Pad, slew-rate limited	$T_{OKPOS}$	All devices		7.0		6.9	ns
Output (O) to Pad, fast	$T_{OPF}$	All devices		4.8		3.6	ns
Output (O) to Pad, slew-rate limited	$T_{OPS}$	All devices		7.3		7.2	ns
3-state to Pad hi-Z (slew-rate independent)	$T_{TSHZ}$	All devices		3.8		3.0	ns
3-state to Pad active and valid, fast	$T_{TSONF}$	All devices		7.3		6.0	ns
3-state to Pad active and valid, slew-rate limited	$T_{TSONS}$	All devices		9.8		9.6	ns
<b>Setup and Hold Times</b>							
Output (O) to clock (OK) setup time	$T_{OOK}$	All devices	3.8		2.5		ns
Output (O) to clock (OK) hold time	$T_{OKO}$	All devices	0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	$T_{ECOK}$	All devices	2.7		2.0		ns
Clock Enable (EC) to clock (OK) hold time	$T_{OKEC}$	All devices	0.5		0.0		ns
<b>Global Set/Reset</b>							
Minimum GSR pulse width	$T_{MRW}$	All devices	13.5		11.5		ns
Delay from GSR input to any Pad	$T_{RPO}$	XCS05	15.0		12.0		ns
		XCS10	15.7		12.5		ns
		XCS20	16.2		13.0		ns
		XCS30	16.9		13.5		ns
		XCS40	17.5		14.0		ns

Preliminary

Note 1: Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.

Note 2: Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.

Note 3: Output timing is measured at ~50%  $V_{CC}$  threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.

Note 4: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## SpartanXL Detailed Specifications

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

**Notwithstanding the definition of the above terms, all specifications are subject to change without notice.**

### SpartanXL Absolute Maximum Ratings<sup>1</sup>

Symbol	Description	Value	Units	
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V	
$V_{IN}$	Input voltage relative to GND (Note 2, 3, 4, 5)	5V Tolerant I/O Checked <sup>2, 3</sup>	-0.5 to 5.5	V
		Not 5V Tolerant I/Os <sup>4, 5</sup>	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output (Note 2, 3, 4, 5)	5V Tolerant I/O Checked <sup>2, 3</sup>	-0.5 to 5.5	V
		Not 5V Tolerant I/Os <sup>4, 5</sup>	-0.5 to $V_{CC} + 0.5$	V
$V_{CCt}$	Longest Supply Voltage Rise Time from 1V to 3V	50	ms	
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C	
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C	
$T_J$	Junction temperature	Plastic packages	+125	°C

- Note
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
  - With 5V Tolerant I/Os Selected, the Maximum DC overshoot (above  $V_{CC}$ ) must be limited to either 5.5 V or 10 mA and undershoot (below GND) must be limited to either 0.5 V or 10 mA, whichever is easier to achieve.
  - With 5V Tolerant I/Os Selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
  - Without 5V Tolerant I/Os Selected, the Maximum DC overshoot or undershoot must be limited to either 0.5 V or 10 mA, whichever is easier to achieve.
  - Without 5V Tolerant I/Os Selected, the Maximum AC conditions are as follows; the device pins may undershoot to -2.0 V or overshoot to  $V_{CC} + 2.0$  V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

### SpartanXL Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_J = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$	Industrial	3.0	3.6	V
$V_{IH}$	High-level input voltage		50% of $V_{CC}$	5.5	V
$V_{IL}$	Low-level input voltage		0	30% of $V_{CC}$	V
$T_{IN}$	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.  
Input and output measurement threshold is ~50% of  $V_{CC}$ .

## SpartanXL DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0 \text{ mA}$ , $V_{CC}$ min (LVTTL)	2.4		V
	High-level output voltage @ $I_{OH} = -500 \mu\text{A}$ , (LVC MOS)	90% $V_{CC}$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0 \text{ mA}$ , $V_{CC}$ min (LVTTL) (Note 1)		0.4	V
	Low-level output voltage @ $I_{OL} = 24.0 \text{ mA}$ , $V_{CC}$ min (LVTTL) (Note 2)		0.4	V
	Low-level output voltage @ $I_{OL} = 1500 \mu\text{A}$ , (LVC MOS)		10% $V_{CC}$	V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)	2.5		V
$I_{CC0}$	Quiescent FPGA supply current (Note 3)		5	mA
$I_L$	Input or output leakage current	-10	+10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample tested)		10	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0\text{V}$ (sample tested)	0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.3\text{V}$ (sample tested)	0.02		mA

Note 1: With up to 64 pins simultaneously sinking 12 mA (default mode).

Note 2: With up to 64 pins simultaneously sinking 24mA (with 24 mA option selected).

Note 3: With no output current loads, no active input pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the Tie option.

## SpartanXL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

NOTE: “-5” is a faster speed grade than “-4”. Updated advance speed files are expected in mid-October.

### SpartanXL Output Flip-Flop, Clock-to-Out

Speed Grade			-4	-5	Units
Description	Symbol	Device	Max	Max	
Global Clock to Output using OFF					
<b>Fast</b>	$T_{ICKOF}$	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL			ns ns ns ns ns
<b>Slew-rate limited</b>	$T_{ICKO}$	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL			ns ns ns ns ns
OFF = Output Flip Flop			<b>Advance</b>		

Note 1: Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50%  $V_{CC}$  threshold with 50 pF external capacitive load.

## SpartanXL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

### SpartanXL Setup and Hold

Speed Grade			-4	-5	Units
Description	Symbol	Device	Min	Min	
Input Setup/Hold Times Using Global Clock and IFF					
<b>No Delay</b>	$T_{SUF}/T_{HF}$	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL			ns ns ns ns ns
<b>With Delay</b>	$T_{SU}/T_H$	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL			ns ns ns ns ns
IFF = Input Flip-Flop or Latch			<b>Advance</b>		

Note 3: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

## Pin Descriptions

There are three types of pins in the Spartan Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is

unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net, GTS. See “[Global Signals: GSR and GTS](#)” on page 1-18 for more information.

Device pins for Spartan Series devices are described in [Table 15](#).

**Table 15: Pin Descriptions**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
<b>Permanently Dedicated Pins</b>			
VCC	X	X	Eight or more (depending on package) connections to the nominal +5 V supply voltage (+3.3 V for SpartanXL devices). All must be connected, and each must be decoupled with a 0.01 - 0.1 $\mu$ F capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan Series devices, except during Readback. See “ <a href="#">Violating the Maximum High and Low Time Specification for the Readback Clock</a> ” on page 1-31 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
PROGRAM	I	I	PROGRAM is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases INIT. The PROGRAM pin has a permanent weak pull-up, so it need not be externally pulled up to Vcc.
MODE (Spartan) M0, M1 (SpartanXL)	I	X	The Mode input(s) are sampled after INIT goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.
Don't Connect	X	X	Pins reserved for factory testing and possible future enhancements. Pins must be left floating.
<b>User I/O Pins That Can Have Special Functions</b>			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

**Table 15: Pin Descriptions (Continued)**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
LDC	O	I/O	Low During Configuration (LDC) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin.
INIT	I/O	I/O	Before and during configuration, INIT is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, INIT is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins..
SGCK1 - SGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (SpartanXL)	Weak Pull-up	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (SpartanXL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (SpartanXL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.

**Table 15: Pin Descriptions (Continued)**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In SpartanXL Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
<b>Unrestricted User-Programmable I/O Pins</b>			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

## Device-Specific Pinout Tables

Device-specific tables include all packages for each Spartan and SpartanXL device. They follow the pad locations around the die, and include boundary scan register locations.

### Pin Locations for XCS05 & XCS05XL Devices

XCS05/XL Pad Name	PC84	VQ100	Bndry Scan
VCC	P2	P89	-
I/O	P3	P90	32
I/O	P4	P91	35
I/O	-	P92	38
I/O	-	P93	41
I/O	P5	P94	44
I/O	P6	P95	47
I/O	P7	P96	50
I/O	P8	P97	53
I/O	P9	P98	56
I/O, SGCK1 †, GCK8 ‡‡	P10	P99	59
VCC	P11	P100	-
GND	P12	P1	-
I/O, PGCK1 †, GCK1 ‡‡	P13	P2	62
I/O	P14	P3	65
I/O, TDI	P15	P4	68
I/O, TCK	P16	P5	71
I/O, TMS	P17	P6	74
I/O	P18	P7	77
I/O	-	P8	83
I/O	P19	P9	86
I/O	P20	P10	89
GND	P21	P11	-
VCC	P22	P12	-
I/O	P23	P13	92
I/O	P24	P14	95
I/O	-	P15	98
I/O	P25	P16	104
I/O	P26	P17	107
I/O	P27	P18	110
I/O	-	P19	113
I/O	P28	P20	116

XCS05/XL Pad Name	PC84	VQ100	Bndry Scan
I/O, SGCK2 †, GCK2 ‡‡	P29	P21	119
Don't Connect †, M1 ‡‡	P30	P22	122
GND	P31	P23	-
MODE †, M0 ‡‡	P32	P24	125
VCC	P33	P25	-
Don't Connect	P34	P26	126 †
I/O, PGCK2 †, GCK3 ‡‡	P35	P27	127 ‡
I/O (HDC)	P36	P28	130 ‡
I/O	-	P29	133 ‡
I/O (LDC)	P37	P30	136 ‡
I/O	P38	P31	139 ‡
I/O	P39	P32	142 ‡
I/O	-	P33	145 ‡
I/O	-	P34	148 ‡
I/O	P40	P35	151 ‡
I/O (INIT)	P41	P36	154 ‡
VCC	P42	P37	-
GND	P43	P38	-
I/O	P44	P39	157 ‡
I/O	P45	P40	160 ‡
I/O	-	P41	163 ‡
I/O	-	P42	166 ‡
I/O	P46	P43	169 ‡
I/O	P47	P44	172 ‡
I/O	P48	P45	175 ‡
I/O	P49	P46	178 ‡
I/O	P50	P47	181 ‡
I/O, SGCK3 †, GCK4 ‡‡	P51	P48	184 ‡
GND	P52	P49	-
DONE	P53	P50	-
VCC	P54	P51	-
PROGRAM	P55	P52	-

XCS05/XL Pad Name	PC84	VQ100	Bndry Scan
I/O (D7 ††)	P56	P53	187 ‡
I/O, PGCK3 †, GCK5 ††	P57	P54	190 ‡
I/O (D6 ††)	P58	P55	193 ‡
I/O	-	P56	196 ‡
I/O (D5 ††)	P59	P57	199 ‡
I/O	P60	P58	202 ‡
I/O	-	P59	205 ‡
I/O	-	P60	208 ‡
I/O (D4 ††)	P61	P61	211 ‡
I/O	P62	P62	214 ‡
VCC	P63	P63	-
GND	P64	P64	-
I/O (D3 ††)	P65	P65	217 ‡
I/O	P66	P66	220 ‡
I/O	-	P67	223 ‡
I/O (D2 ††)	P67	P68	229 ‡
I/O	P68	P69	232 ‡
I/O (D1 ††)	P69	P70	235 ‡
I/O	P70	P71	238 ‡
I/O (D0 ††, DIN)	P71	P72	241 ‡
I/O, SGCK4 †, GCK6 †† (DOUT)	P72	P73	244 ‡

XCS05/XL Pad Name	PC84	VQ100	Bndry Scan
CCLK	P73	P74	-
VCC	P74	P75	-
O, TDO	P75	P76	0
GND	P76	P77	-
I/O	P77	P78	2
I/O, PGCK4 †, GCK7 ††	P78	P79	5
I/O (CS1 ††)	P79	P80	8
I/O	P80	P81	11
I/O	P81	P82	14
I/O	P82	P83	17
I/O	-	P84	20
I/O	-	P85	23
I/O	P83	P86	26
I/O	P84	P87	29
GND	P1	P88	-

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† = 5V Spartan only

†† = 3V SpartanXL only

‡ The "Don't Connect" on the XCS05XL is not part of the Boundary Scan chain. For the XCS05XL, subtract 1 from all Boundary Scan numbers from GCK3 on (127 and higher).

## Pin Locations for XCS10 & XCS10XL Devices

XCS10/XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
VCC	P2	P89	P128	-
I/O	P3	P90	P129	44
I/O	P4	P91	P130	47
I/O	-	P92	P131	50
I/O	-	P93	P132	53
I/O	P5	P94	P133	56
I/O	P6	P95	P134	59
I/O	-	-	P135	62
I/O	-	-	P136	65
GND	-	-	P137	-
I/O	P7	P96	P138	68
I/O	P8	P97	P139	71
I/O	-	-	P140	74
I/O	-	-	P141	77
I/O	P9	P98	P142	80
I/O, SGCK1 †, GCK8 ††	P10	P99	P143	83
VCC	P11	P100	P144	-
GND	P12	P1	P1	-
I/O, PGCK1 †, GCK1 ††	P13	P2	P2	86
I/O	P14	P3	P3	89
I/O	-	-	P4	92
I/O	-	-	P5	95
I/O, TDI	P15	P4	P6	98
I/O, TCK	P16	P5	P7	101
GND	-	-	P8	-
I/O	-	-	P9	104
I/O	-	-	P10	107

XCS10/XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
I/O, TMS	P17	P6	P11	110
I/O	P18	P7	P12	113
I/O	-	-	P13	116
I/O	-	P8	P14	119
I/O	P19	P9	P15	122
I/O	P20	P10	P16	125
GND	P21	P11	P17	-
VCC	P22	P12	P18	-
I/O	P23	P13	P19	128
I/O	P24	P14	P20	131
I/O	-	P15	P21	134
I/O	-	-	P22	137
I/O	P25	P16	P23	140
I/O	P26	P17	P24	143
I/O	-	-	P25	146
I/O	-	-	P26	149
GND	-	-	P27	-
I/O	P27	P18	P28	152
I/O	-	P19	P29	155
I/O	-	-	P30	158
I/O	-	-	P31	161
I/O	P28	P20	P32	164
I/O, SGCK2 †, GCK2 ††	P29	P21	P33	167
Don't Connect †, M1 ††	P30	P22	P34	170
GND	P31	P23	P35	-
MODE †, M0 ††	P32	P24	P36	173
VCC	P33	P25	P37	-

XCS10/XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
Don't Connect	P34	P26	P38	174 †
I/O, PGCK2 †, GCK3 ‡‡	P35	P27	P39	175 ‡
I/O (HDC)	P36	P28	P40	178 ‡
I/O	-	-	P41	181 ‡
I/O	-	-	P42	184 ‡
I/O	-	P29	P43	187 ‡
I/O (LDC)	P37	P30	P44	190 ‡
GND	-	-	P45	-
I/O	-	-	P46	193 ‡
I/O	-	-	P47	196 ‡
I/O	P38	P31	P48	199 ‡
I/O	P39	P32	P49	202 ‡
I/O	-	P33	P50	205 ‡
I/O	-	P34	P51	208 ‡
I/O	P40	P35	P52	211 ‡
I/O (INIT)	P41	P36	P53	214 ‡
VCC	P42	P37	P54	-
GND	P43	P38	P55	-
I/O	P44	P39	P56	217 ‡
I/O	P45	P40	P57	220 ‡
I/O	-	P41	P58	223 ‡
I/O	-	P42	P59	226 ‡
I/O	P46	P43	P60	229 ‡
I/O	P47	P44	P61	232 ‡
I/O	-	-	P62	235 ‡
I/O	-	-	P63	238 ‡
GND	-	-	P64	-
I/O	P48	P45	P65	241 ‡
I/O	P49	P46	P66	244 ‡
I/O	-	-	P67	247 ‡
I/O	-	-	P68	250 ‡
I/O	P50	P47	P69	253 ‡
I/O, SGCK3 †, GCK4 ‡‡	P51	P48	P70	256 ‡
GND	P52	P49	P71	-
DONE	P53	P50	P72	-
VCC	P54	P51	P73	-
PROGRAM	P55	P52	P74	-
I/O (D7 ‡‡)	P56	P53	P75	259 ‡
I/O, PGCK3 †, GCK5 ‡‡	P57	P54	P76	262 ‡
I/O	-	-	P77	265 ‡
I/O	-	-	P78	268 ‡
I/O (D6 ‡‡)	P58	P55	P79	271 ‡
I/O	-	P56	P80	274 ‡
GND	-	-	P81	-
I/O	-	-	P82	277 ‡
I/O	-	-	P83	280 ‡
I/O (D5 ‡‡)	P59	P57	P84	283 ‡
I/O	P60	P58	P85	286 ‡
I/O	-	P59	P86	289 ‡
I/O	-	P60	P87	292 ‡
I/O (D4 ‡‡)	P61	P61	P88	295 ‡

XCS10/XL Pad Name	PC84	VQ100	TQ144	Bndry Scan
I/O	P62	P62	P89	298 ‡
VCC	P63	P63	P90	-
GND	P64	P64	P91	-
I/O (D3 ‡‡)	P65	P65	P92	301 ‡
I/O	P66	P66	P93	304 ‡
I/O	-	P67	P94	307 ‡
I/O	-	-	P95	310 ‡
I/O (D2 ‡‡)	P67	P68	P96	313 ‡
I/O	P68	P69	P97	316 ‡
I/O	-	-	P98	319 ‡
I/O	-	-	P99	322 ‡
GND	-	-	P100	-
I/O (D1 ‡‡)	P69	P70	P101	325 ‡
I/O	P70	P71	P102	328 ‡
I/O	-	-	P103	331 ‡
I/O	-	-	P104	334 ‡
I/O (D0 ‡‡, DIN)	P71	P72	P105	337 ‡
I/O, SGCK4 †, GCK6 ‡‡ (DOUT)	P72	P73	P106	340 ‡
CCLK	P73	P74	P107	-
VCC	P74	P75	P108	-
O, TDO	P75	P76	P109	0
GND	P76	P77	P110	-
I/O	P77	P78	P111	2
I/O, PGCK4 †, GCK7 ‡‡	P78	P79	P112	5
I/O	-	-	P113	8
I/O	-	-	P114	11
I/O (CS1 ‡‡)	P79	P80	P115	14
I/O	P80	P81	P116	17
GND	-	-	P118	-
I/O	-	-	P119	20
I/O	-	-	P120	23
I/O	P81	P82	P121	26
I/O	P82	P83	P122	29
I/O	-	P84	P123	32
I/O	-	P85	P124	35
I/O	P83	P86	P125	38
I/O	P84	P87	P126	41
GND	P1	P88	P127	-

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† = 5V Spartan only

‡‡ = 3V SpartanXL only

‡ The “Don’t Connect” on the XCS10XL is not part of the Boundary Scan chain. For the XCS10XL, subtract 1 from all Boundary Scan numbers from GCK3 on (175 and higher).

### Additional XCS10/XL Package Pins

#### TQ144

Not Connected Pins						
P117	-	-	-	-	-	-

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## Pin Locations for XCS20 & XCS20XL Devices

XCS20/XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
VCC	P89	P128	P183	-
I/O	P90	P129	P184	62
I/O	P91	P130	P185	65
I/O	P92	P131	P186	68
I/O	P93	P132	P187	71
I/O	-	-	P188	74
I/O	-	-	P189	77
I/O	P94	P133	P190	80
I/O	P95	P134	P191	83
VCC ††	-	-	P192	-
I/O	-	P135	P193	86
I/O	-	P136	P194	89
GND	-	P137	P195	-
I/O	-	-	P196	92
I/O	-	-	P197	95
I/O	-	-	P198	98
I/O	-	-	P199	101
I/O	P96	P138	P200	104
I/O	P97	P139	P201	107
I/O	-	P140	P204	110
I/O	-	P141	P205	113
I/O	P98	P142	P206	116
I/O, SGCK1 †, GCK8 ††	P99	P143	P207	119
VCC	P100	P144	P208	-
GND	P1	P1	P1	-
I/O, PGCK1 †, GCK1 ††	P2	P2	P2	122
I/O	P3	P3	P3	125
I/O	-	P4	P4	128
I/O	-	P5	P5	131
I/O, TDI	P4	P6	P6	134
I/O, TCK	P5	P7	P7	137
I/O	-	-	P8	140
I/O	-	-	P9	143
I/O	-	-	P10	146
I/O	-	-	P11	149
GND	-	P8	P13	-
I/O	-	P9	P14	152
I/O	-	P10	P15	155
I/O, TMS	P6	P11	P16	158
I/O	P7	P12	P17	161
VCC ††	-	-	P18	-
I/O	-	-	P19	164
I/O	-	-	P20	167
I/O	-	P13	P21	170
I/O	P8	P14	P22	173
I/O	P9	P15	P23	176
I/O	P10	P16	P24	179
GND	P11	P17	P25	-
VCC	P12	P18	P26	-
I/O	P13	P19	P27	182
I/O	P14	P20	P28	185
I/O	P15	P21	P29	188
I/O	-	P22	P30	191

XCS20/XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
I/O	-	-	P31	194
I/O	-	-	P32	197
VCC ††	-	-	P33	-
I/O	P16	P23	P34	200
I/O	P17	P24	P35	203
I/O	-	P25	P36	206
I/O	-	P26	P37	209
GND	-	P27	P38	-
I/O	-	-	P40	212
I/O	-	-	P41	215
I/O	-	-	P42	218
I/O	-	-	P43	221
I/O	P18	P28	P44	224
I/O	P19	P29	P45	227
I/O	-	P30	P46	230
I/O	-	P31	P47	233
I/O	P20	P32	P48	236
I/O, SGCK2 †, GCK2 ††	P21	P33	P49	239
Don't Connect †, M1 ††	P22	P34	P50	242
GND	P23	P35	P51	-
MODE †, M0 ††	P24	P36	P52	245
VCC	P25	P37	P53	-
Don't Connect	P26	P38	P54	246 †
I/O, PGCK2 †, GCK3 ††	P27	P39	P55	247 †
I/O (HDC)	P28	P40	P56	250 †
I/O	-	P41	P57	253 †
I/O	-	P42	P58	256 †
I/O	P29	P43	P59	259 †
I/O (LDC)	P30	P44	P60	262 †
I/O	-	-	P61	265 †
I/O	-	-	P62	268 †
I/O	-	-	P63	271 †
I/O	-	-	P64	274 †
GND	-	P45	P66	-
I/O	-	P46	P67	277 †
I/O	-	P47	P68	280 †
I/O	P31	P48	P69	283 †
I/O	P32	P49	P70	286 †
VCC ††	-	-	P71	-
I/O	-	-	P72	289 †
I/O	-	-	P73	292 †
I/O	P33	P50	P74	295 †
I/O	P34	P51	P75	298 †
I/O	P35	P52	P76	301 †
I/O (INIT)	P36	P53	P77	304 †
VCC	P37	P54	P78	-
GND	P38	P55	P79	-
I/O	P39	P56	P80	307 †
I/O	P40	P57	P81	310 †
I/O	P41	P58	P82	313 †
I/O	P42	P59	P83	316 †
I/O	-	-	P84	319 †
I/O	-	-	P85	322 †

XCS20/XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
VCC ††	-	-	P86	-
I/O	P43	P60	P87	325 ‡
I/O	P44	P61	P88	328 ‡
I/O	-	P62	P89	331 ‡
I/O	-	P63	P90	334 ‡
GND	-	P64	P91	-
I/O	-	-	P93	337 ‡
I/O	-	-	P94	340 ‡
I/O	-	-	P95	343 ‡
I/O	-	-	P96	346 ‡
I/O	P45	P65	P97	349 ‡
I/O	P46	P66	P98	352 ‡
I/O	-	P67	P99	355 ‡
I/O	-	P68	P100	358 ‡
I/O	P47	P69	P101	361 ‡
I/O, SGCK3 †, GCK4 ††	P48	P70	P102	364 ‡
GND	P49	P71	P103	-
DONE	P50	P72	P104	-
VCC	P51	P73	P105	-
PROGRAM	P52	P74	P106	-
I/O (D7 ††)	P53	P75	P107	367 ‡
I/O, PGCK3 †, GCK5 ††	P54	P76	P108	370 ‡
I/O	-	P77	P109	373 ‡
I/O	-	P78	P110	376 ‡
I/O (D6 ††)	P55	P79	P112	379 ‡
I/O	P56	P80	P113	382 ‡
I/O	-	-	P114	385 ‡
I/O	-	-	P115	388 ‡
I/O	-	-	P116	391 ‡
I/O	-	-	P117	394 ‡
GND	-	P81	P118	-
I/O	-	P82	P119	397 ‡
I/O	-	P83	P120	400 ‡
VCC ††	-	-	P121	-
I/O (D5 ††)	P57	P84	P122	403 ‡
I/O	P58	P85	P123	406 ‡
I/O	-	-	P124	409 ‡
I/O	-	-	P125	412 ‡
I/O	P59	P86	P126	415 ‡
I/O	P60	P87	P127	418 ‡
I/O (D4 ††)	P61	P88	P128	421 ‡
I/O	P62	P89	P129	424 ‡
VCC	P63	P90	P130	-
GND	P64	P91	P131	-
I/O (D3 ††)	P65	P92	P132	427 ‡
I/O	P66	P93	P133	430 ‡
I/O	P67	P94	P134	433 ‡
I/O	-	P95	P135	436 ‡
I/O	-	-	P136	439 ‡
I/O	-	-	P137	442 ‡
I/O (D2 ††)	P68	P96	P138	445 ‡
I/O	P69	P97	P139	448 ‡
VCC ††	-	-	P140	-
I/O	-	P98	P141	451 ‡

XCS20/XL Pad Name	VQ100	TQ144	PQ208	Bndry Scan
I/O	-	P99	P142	454 ‡
GND	-	P100	P143	-
I/O	-	-	P145	457 ‡
I/O	-	-	P146	460 ‡
I/O	-	-	P147	463 ‡
I/O	-	-	P148	466 ‡
I/O (D1 ††)	P70	P101	P149	469 ‡
I/O	P71	P102	P150	472 ‡
I/O	-	P103	P151	475 ‡
I/O	-	P104	P152	478 ‡
I/O (D0 ††, DIN)	P72	P105	P153	481 ‡
I/O, SGCK4 †, GCK6 †† (DOUT)	P73	P106	P154	484 ‡
CCLK	P74	P107	P155	-
VCC	P75	P108	P156	-
O, TDO	P76	P109	P157	0
GND	P77	P110	P158	-
I/O	P78	P111	P159	2
I/O, PGCK4 †, GCK7 ††	P79	P112	P160	5
I/O	-	P113	P161	8
I/O	-	P114	P162	11
I/O (CS1 ††)	P80	P115	P163	14
I/O	P81	P116	P164	17
I/O	-	P117	P166	20
I/O	-	-	P167	23
I/O	-	-	P168	26
I/O	-	-	P169	29
GND	-	P118	P170	-
I/O	-	P119	P171	32
I/O	-	P120	P172	35
VCC ††	-	-	P173	-
I/O	P82	P121	P174	38
I/O	P83	P122	P175	41
I/O	-	-	P176	44
I/O	-	-	P177	47
I/O	P84	P123	P178	50
I/O	P85	P124	P179	53
I/O	P86	P125	P180	56
I/O	P87	P126	P181	59
GND	P88	P127	P182	-

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### Additional XCS20/XL Package Pins

#### PQ208

Not Connected Pins					
P12	P18 †	P33 †	P39	P65	P71 †
P86 †	P92	P111	P121 †	P140 †	P144
P165	P173 †	P192 †	P202	P203	-

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† = 5V Spartan only

†† = 3V SpartanXL only

‡ The “Don’t Connect” on the XCS20XL is not part of the Boundary Scan chain. For the XCS20XL, subtract 1 from all Boundary Scan numbers from GCK3 on (247 and higher).

## Pin Locations for XCS30 & XCS30XL Devices

XCS30/XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
VCC	P89	P128	P183	P212	VCC*	-
I/O	P90	P129	P184	P213	C10	74
I/O	P91	P130	P185	P214	D10	77
I/O	P92	P131	P186	P215	A9	80
I/O	P93	P132	P187	P216	B9	83
I/O	-	-	P188	P217	C9	86
I/O	-	-	P189	P218	D9	89
I/O	P94	P133	P190	P220	A8	92
I/O	P95	P134	P191	P221	B8	95
VCC	-	-	P192	P222	VCC*	-
I/O	-	-	-	P223	A6	98
I/O	-	-	-	P224	C7	101
I/O	-	P135	P193	P225	B6	104
I/O	-	P136	P194	P226	A5	107
GND	-	P137	P195	P227	GND*	-
I/O	-	-	P196	P228	C6	110
I/O	-	-	P197	P229	B5	113
I/O	-	-	P198	P230	A4	116
I/O	-	-	P199	P231	C5	119
I/O	P96	P138	P200	P232	B4	122
I/O	P97	P139	P201	P233	A3	125
I/O	-	-	P202	P234	D5	128
I/O	-	-	P203	P235	C4	131
I/O	-	P140	P204	P236	B3	134
I/O	-	P141	P205	P237	B2	137
I/O	P98	P142	P206	P238	A2	140
I/O, SGCK1 †, GCK8 ‡†	P99	P143	P207	P239	C3	143
VCC	P100	P144	P208	P240	VCC*	-
GND	P1	P1	P1	P1	GND*	-
I/O, PGCK1 †, GCK1 ‡†	P2	P2	P2	P2	B1	146
I/O	P3	P3	P3	P3	C2	149
I/O	-	P4	P4	P4	D2	152
I/O	-	P5	P5	P5	D3	155
I/O, TDI	P4	P6	P6	P6	E4	158
I/O, TCK	P5	P7	P7	P7	C1	161
I/O	-	-	P8	P8	D1	164
I/O	-	-	P9	P9	E3	167
I/O	-	-	P10	P10	E2	170
I/O	-	-	P11	P11	E1	173
I/O	-	-	P12	P12	F3	176
I/O	-	-	-	P13	F2	179
GND	-	P8	P13	P14	GND*	-
I/O	-	P9	P14	P15	G3	182
I/O	-	P10	P15	P16	G2	185
I/O, TMS	P6	P11	P16	P17	G1	188
I/O	P7	P12	P17	P18	H3	191
VCC	-	-	P18	P19	VCC*	-
I/O	-	-	-	P20	H2	194
I/O	-	-	-	P21	H1	197
I/O	-	-	P19	P23	J2	200
I/O	-	-	P20	P24	J1	203

XCS30/XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
I/O	-	P13	P21	P25	K2	206
I/O	P8	P14	P22	P26	K3	209
I/O	P9	P15	P23	P27	K1	212
I/O	P10	P16	P24	P28	L1	215
GND	P11	P17	P25	P29	GND*	-
VCC	P12	P18	P26	P30	VCC*	-
I/O	P13	P19	P27	P31	L2	218
I/O	P14	P20	P28	P32	L3	221
I/O	P15	P21	P29	P33	L4	224
I/O	-	P22	P30	P34	M1	227
I/O	-	-	P31	P35	M2	230
I/O	-	-	P32	P36	M3	233
I/O	-	-	-	P38	N1	236
I/O	-	-	-	P39	N2	239
VCC	-	-	P33	P40	VCC*	-
I/O	P16	P23	P34	P41	P1	242
I/O	P17	P24	P35	P42	P2	245
I/O	-	P25	P36	P43	R1	248
I/O	-	P26	P37	P44	P3	251
GND	-	P27	P38	P45	GND*	-
I/O	-	-	-	P46	T1	254
I/O	-	-	P39	P47	R3	257
I/O	-	-	P40	P48	T2	260
I/O	-	-	P41	P49	U1	263
I/O	-	-	P42	P50	T3	266
I/O	-	-	P43	P51	U2	269
I/O	P18	P28	P44	P52	V1	272
I/O	P19	P29	P45	P53	T4	275
I/O	-	P30	P46	P54	U3	278
I/O	-	P31	P47	P55	V2	281
I/O	P20	P32	P48	P56	W1	284
I/O, SGCK2 †, GCK2 ‡†	P21	P33	P49	P57	V3	287
Don't Connect †, M1 ‡†	P22	P34	P50	P58	W2	290
GND	P23	P35	P51	P59	GND*	-
MODE †, M0 ‡†	P24	P36	P52	P60	Y1	293
VCC	P25	P37	P53	P61	VCC*	-
Don't Connect	P26	P38	P54	P62	W3	294 †
I/O, PGCK2 †, GCK3 ‡†	P27	P39	P55	P63	Y2	295 †
I/O (HDC)	P28	P40	P56	P64	W4	298 †
I/O	-	P41	P57	P65	V4	301 †
I/O	-	P42	P58	P66	U5	304 †
I/O	P29	P43	P59	P67	Y3	307 †
I/O (LDC)	P30	P44	P60	P68	Y4	310 †
I/O	-	-	P61	P69	V5	313 †
I/O	-	-	P62	P70	W5	316 †
I/O	-	-	P63	P71	Y5	319 †
I/O	-	-	P64	P72	V6	322 †
I/O	-	-	P65	P73	W6	325 †
I/O	-	-	-	P74	Y6	328 †
GND	-	P45	P66	P75	GND*	-

XCS30/XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
I/O	-	P46	P67	P76	W7	331 ‡
I/O	-	P47	P68	P77	Y7	334 ‡
I/O	P31	P48	P69	P78	V8	337 ‡
I/O	P32	P49	P70	P79	W8	340 ‡
VCC	-	-	P71	P80	VCC*	-
I/O	-	-	P72	P81	Y8	343 ‡
I/O	-	-	P73	P82	U9	346 ‡
I/O	-	-	-	P84	Y9	349 ‡
I/O	-	-	-	P85	W10	352 ‡
I/O	P33	P50	P74	P86	V10	355 ‡
I/O	P34	P51	P75	P87	Y10	358 ‡
I/O	P35	P52	P76	P88	Y11	361 ‡
I/O (INIT)	P36	P53	P77	P89	W11	364 ‡
VCC	P37	P54	P78	P90	VCC*	-
GND	P38	P55	P79	P91	GND*	-
I/O	P39	P56	P80	P92	V11	367 ‡
I/O	P40	P57	P81	P93	U11	370 ‡
I/O	P41	P58	P82	P94	Y12	373 ‡
I/O	P42	P59	P83	P95	W12	376 ‡
I/O	-	-	P84	P96	V12	379 ‡
I/O	-	-	P85	P97	U12	382 ‡
I/O	-	-	-	P99	V13	385 ‡
I/O	-	-	-	P100	Y14	388 ‡
VCC	-	-	P86	P101	VCC*	-
I/O	P43	P60	P87	P102	Y15	391 ‡
I/O	P44	P61	P88	P103	V14	394 ‡
I/O	-	P62	P89	P104	W15	397 ‡
I/O	-	P63	P90	P105	Y16	400 ‡
GND	-	P64	P91	P106	GND*	-
I/O	-	-	-	P107	V15	403 ‡
I/O	-	-	P92	P108	W16	406 ‡
I/O	-	-	P93	P109	Y17	409 ‡
I/O	-	-	P94	P110	V16	412 ‡
I/O	-	-	P95	P111	W17	415 ‡
I/O	-	-	P96	P112	Y18	418 ‡
I/O	P45	P65	P97	P113	U16	421 ‡
I/O	P46	P66	P98	P114	V17	424 ‡
I/O	-	P67	P99	P115	W18	427 ‡
I/O	-	P68	P100	P116	Y19	430 ‡
I/O	P47	P69	P101	P117	V18	433 ‡
I/O, SGCK3 †, GCK4 ‡†	P48	P70	P102	P118	W19	436 ‡
GND	P49	P71	P103	P119	GND*	-
DONE	P50	P72	P104	P120	Y20	-
VCC	P51	P73	P105	P121	VCC*	-
PROGRAM	P52	P74	P106	P122	V19	-
I/O (D7 ‡†)	P53	P75	P107	P123	U19	439 ‡
I/O, PGCK3 †, GCK5 ‡†	P54	P76	P108	P124	U18	442 ‡
I/O	-	P77	P109	P125	T17	445 ‡
I/O	-	P78	P110	P126	V20	448 ‡
I/O	-	-	-	P127	U20	451 ‡
I/O	-	-	P111	P128	T18	454 ‡
I/O (D6 ‡†)	P55	P79	P112	P129	T19	457 ‡
I/O	P56	P80	P113	P130	T20	460 ‡
I/O	-	-	P114	P131	R18	463 ‡

XCS30/XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
I/O	-	-	P115	P132	R19	466 ‡
I/O	-	-	P116	P133	R20	469 ‡
I/O	-	-	P117	P134	P18	472 ‡
GND	-	P81	P118	P135	GND*	-
I/O	-	-	-	P136	P20	475 ‡
I/O	-	-	-	P137	N18	478 ‡
I/O	-	P82	P119	P138	N19	481 ‡
I/O	-	P83	P120	P139	N20	484 ‡
VCC	-	-	P121	P140	VCC*	-
I/O (D5 ‡†)	P57	P84	P122	P141	M17	487 ‡
I/O	P58	P85	P123	P142	M18	490 ‡
I/O	-	-	P124	P144	M20	493 ‡
I/O	-	-	P125	P145	L19	496 ‡
I/O	P59	P86	P126	P146	L18	499 ‡
I/O	P60	P87	P127	P147	L20	502 ‡
I/O (D4 ‡†)	P61	P88	P128	P148	K20	505 ‡
I/O	P62	P89	P129	P149	K19	508 ‡
VCC	P63	P90	P130	P150	VCC*	-
GND	P64	P91	P131	P151	GND*	-
I/O (D3 ‡†)	P65	P92	P132	P152	K18	511 ‡
I/O	P66	P93	P133	P153	K17	514 ‡
I/O	P67	P94	P134	P154	J20	517 ‡
I/O	-	P95	P135	P155	J19	520 ‡
I/O	-	-	P136	P156	J18	523 ‡
I/O	-	-	P137	P157	J17	526 ‡
I/O (D2 ‡†)	P68	P96	P138	P159	H19	529 ‡
I/O	P69	P97	P139	P160	H18	532 ‡
VCC	-	-	P140	P161	VCC*	-
I/O	-	P98	P141	P162	G19	535 ‡
I/O	-	P99	P142	P163	F20	538 ‡
I/O	-	-	P164	G18	541 ‡	
I/O	-	-	P165	F19	544 ‡	
GND	-	P100	P143	P166	GND*	-
I/O	-	-	-	P167	F18	547 ‡
I/O	-	-	P144	P168	E19	550 ‡
I/O	-	-	P145	P169	D20	553 ‡
I/O	-	-	P146	P170	E18	556 ‡
I/O	-	-	P147	P171	D19	559 ‡
I/O	-	-	P148	P172	C20	562 ‡
I/O (D1 ‡†)	P70	P101	P149	P173	E17	565 ‡
I/O	P71	P102	P150	P174	D18	568 ‡
I/O	-	P103	P151	P175	C19	571 ‡
I/O	-	P104	P152	P176	B20	574 ‡
I/O (D0 ‡†, DIN)	P72	P105	P153	P177	C18	577 ‡
I/O, SGCK4 †, GCK6 ‡† (DOUT)	P73	P106	P154	P178	B19	580 ‡
CCLK	P74	P107	P155	P179	A20	-
VCC	P75	P108	P156	P180	VCC*	-
O, TDO	P76	P109	P157	P181	A19	0
GND	P77	P110	P158	P182	GND*	-
I/O	P78	P111	P159	P183	B18	2
I/O, PGCK4 †, GCK7 ‡†	P79	P112	P160	P184	B17	5
I/O	-	P113	P161	P185	C17	8
I/O	-	P114	P162	P186	D16	11
I/O (CS1) ‡†	P80	P115	P163	P187	A18	14

XCS30/XL Pad Name	VQ100	TQ144	PQ208	PQ240	BG256	Bndry Scan
I/O	P81	P116	P164	P188	A17	17
I/O	-	-	P165	P189	C16	20
I/O	-	-	-	P190	B16	23
I/O	-	P117	P166	P191	A16	26
I/O	-	-	P167	P192	C15	29
I/O	-	-	P168	P193	B15	32
I/O	-	-	P169	P194	A15	35
GND	-	P118	P170	P196	GND*	-
I/O	-	P119	P171	P197	B14	38
I/O	-	P120	P172	P198	A14	41
I/O	-	-	-	P199	C13	44
I/O	-	-	-	P200	B13	47
VCC	-	-	P173	P201	VCC*	-
I/O	P82	P121	P174	P202	C12	50
I/O	P83	P122	P175	P203	B12	53
I/O	-	-	P176	P205	A12	56
I/O	-	-	P177	P206	B11	59
I/O	P84	P123	P178	P207	C11	62
I/O	P85	P124	P179	P208	A11	65
I/O	P86	P125	P180	P209	A10	68
I/O	P87	P126	P181	P210	B10	71
GND	P88	P127	P182	P211	GND*	-

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package.

† = 5V Spartan only

†† = 3V SpartanXL only

‡ The "Don't Connect" on the XCS30XL is not part of the Boundary Scan chain. For the XCS30XL, subtract 1 from all Boundary Scan numbers from GCK3 on (295 and higher).

## Additional XCS30/XL Package Pins

### PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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### BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-
Not Connected Pins					
A7	A13	C8	D12	H20	J3
J4	M4	M19	V9	W9	W13
Y13	-	-	-	-	-

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## Pin Locations for XCS40 &amp; XCS40XL Devices

XCS40/XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
VCC	P183	P212	VCC*	-
I/O	P184	P213	C10	86
I/O	P185	P214	D10	89
I/O	P186	P215	A9	92
I/O	P187	P216	B9	95
I/O	P188	P217	C9	98
I/O	P189	P218	D9	101
I/O	P190	P220	A8	104
I/O	P191	P221	B8	107
I/O	-	-	C8	110
I/O	-	-	A7	113
VCC	P192	P222	VCC*	-
I/O	-	P223	A6	116
I/O	-	P224	C7	119
I/O	P193	P225	B6	122
I/O	P194	P226	A5	125
GND	P195	P227	GND*	-
I/O	P196	P228	C6	128
I/O	P197	P229	B5	131
I/O	P198	P230	A4	134
I/O	P199	P231	C5	137
I/O	P200	P232	B4	140
I/O	P201	P233	A3	143
I/O	P202	P234	D5	152
I/O	P203	P235	C4	155
I/O	P204	P236	B3	158
I/O	P205	P237	B2	161
I/O	P206	P238	A2	164
I/O, SGCK1 †, GCK8 ††	P207	P239	C3	167
VCC	P208	P240	VCC*	-
GND	P1	P1	GND*	-
I/O, PGCK1 †, GCK1 ††	P2	P2	B1	170
I/O	P3	P3	C2	173
I/O	P4	P4	D2	176
I/O	P5	P5	D3	179
I/O, TDI	P6	P6	E4	182
I/O, TCK	P7	P7	C1	185
I/O	P8	P8	D1	194
I/O	P9	P9	E3	197
I/O	P10	P10	E2	200
I/O	P11	P11	E1	203
I/O	P12	P12	F3	206
I/O	-	P13	F2	209
GND	P13	P14	GND*	-
I/O	P14	P15	G3	212
I/O	P15	P16	G2	215
I/O, TMS	P16	P17	G1	218
I/O	P17	P18	H3	221
VCC	P18	P19	VCC*	-
I/O	-	P20	H2	224
I/O	-	P21	H1	227

XCS40/XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O	-	-	J4	230
I/O	-	-	J3	233
I/O	P19	P23	J2	236
I/O	P20	P24	J1	239
I/O	P21	P25	K2	242
I/O	P22	P26	K3	245
I/O	P23	P27	K1	248
I/O	P24	P28	L1	251
GND	P25	P29	GND*	-
VCC	P26	P30	VCC*	-
I/O	P27	P31	L2	254
I/O	P28	P32	L3	257
I/O	P29	P33	L4	260
I/O	P30	P34	M1	263
I/O	P31	P35	M2	266
I/O	P32	P36	M3	269
I/O	-	-	M4	272
I/O	-	P38	N1	278
I/O	-	P39	N2	281
VCC	P33	P40	VCC*	-
I/O	P34	P41	P1	284
I/O	P35	P42	P2	287
I/O	P36	P43	R1	290
I/O	P37	P44	P3	293
GND	P38	P45	GND*	-
I/O	-	P46	T1	296
I/O	P39	P47	R3	299
I/O	P40	P48	T2	302
I/O	P41	P49	U1	305
I/O	P42	P50	T3	308
I/O	P43	P51	U2	311
I/O	P44	P52	V1	320
I/O	P45	P53	T4	323
I/O	P46	P54	U3	326
I/O	P47	P55	V2	329
I/O	P48	P56	W1	332
I/O, SGCK2 †, GCK2 ††	P49	P57	V3	335
Don't Connect †, M1 ††	P50	P58	W2	338
GND	P51	P59	GND*	-
MODE †, M0 ††	P52	P60	Y1	341
VCC	P53	P61	VCC*	-
Don't Connect	P54	P62	W3	342†
I/O, PGCK2 †, GCK3 ††	P55	P63	Y2	343‡
I/O (HDC)	P56	P64	W4	346‡
I/O	P57	P65	V4	349‡
I/O	P58	P66	U5	352‡
I/O	P59	P67	Y3	355‡
I/O (LDC)	P60	P68	Y4	358‡
I/O	P61	P69	V5	367‡
I/O	P62	P70	W5	370‡

XCS40/XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O	P63	P71	Y5	373 $\pm$
I/O	P64	P72	V6	376 $\pm$
I/O	P65	P73	W6	379 $\pm$
I/O	-	P74	Y6	382 $\pm$
GND	P66	P75	GND*	-
I/O	P67	P76	W7	385 $\pm$
I/O	P68	P77	Y7	388 $\pm$
I/O	P69	P78	V8	391 $\pm$
I/O	P70	P79	W8	394 $\pm$
VCC	P71	P80	VCC*	-
I/O	P72	P81	Y8	397 $\pm$
I/O	P73	P82	U9	400 $\pm$
I/O	-	-	V9	403 $\pm$
I/O	-	-	W9	406 $\pm$
I/O	-	P84	Y9	409 $\pm$
I/O	-	P85	W10	412 $\pm$
I/O	P74	P86	V10	415 $\pm$
I/O	P75	P87	Y10	418 $\pm$
I/O	P76	P88	Y11	421 $\pm$
I/O (INIT)	P77	P89	W11	424 $\pm$
VCC	P78	P90	VCC*	-
GND	P79	P91	GND*	-
I/O	P80	P92	V11	427 $\pm$
I/O	P81	P93	U11	430 $\pm$
I/O	P82	P94	Y12	433 $\pm$
I/O	P83	P95	W12	436 $\pm$
I/O	P84	P96	V12	439 $\pm$
I/O	P85	P97	U12	442 $\pm$
I/O	-	-	Y13	445 $\pm$
I/O	-	-	W13	448 $\pm$
I/O	-	P99	V13	451 $\pm$
I/O	-	P100	Y14	454 $\pm$
VCC	P86	P101	VCC*	-
I/O	P87	P102	Y15	457 $\pm$
I/O	P88	P103	V14	460 $\pm$
I/O	P89	P104	W15	463 $\pm$
I/O	P90	P105	Y16	466 $\pm$
GND	P91	P106	GND*	-
I/O	-	P107	V15	469 $\pm$
I/O	P92	P108	W16	472 $\pm$
I/O	P93	P109	Y17	475 $\pm$
I/O	P94	P110	V16	478 $\pm$
I/O	P95	P111	W17	481 $\pm$
I/O	P96	P112	Y18	484 $\pm$
I/O	P97	P113	U16	493 $\pm$
I/O	P98	P114	V17	496 $\pm$
I/O	P99	P115	W18	499 $\pm$
I/O	P100	P116	Y19	502 $\pm$
I/O	P101	P117	V18	505 $\pm$
I/O, SGCK3 †, GCK4 ‡	P102	P118	W19	508 $\pm$
GND	P103	P119	GND*	-
DONE	P104	P120	Y20	-
VCC	P105	P121	VCC*	-
PROGRAM	P106	P122	V19	-
I/O (D7 ††)	P107	P123	U19	511 $\pm$

XCS40/XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O, PGCK3 †, GCK5 ‡‡	P108	P124	U18	514 $\pm$
I/O	P109	P125	T17	517 $\pm$
I/O	P110	P126	V20	520 $\pm$
I/O	-	P127	U20	523 $\pm$
I/O	P111	P128	T18	526 $\pm$
I/O (D6 ‡‡)	P112	P129	T19	535 $\pm$
I/O	P113	P130	T20	538 $\pm$
I/O	P114	P131	R18	541 $\pm$
I/O	P115	P132	R19	544 $\pm$
I/O	P116	P133	R20	547 $\pm$
I/O	P117	P134	P18	550 $\pm$
GND	P118	P135	GND*	-
I/O	-	P136	P20	553 $\pm$
I/O	-	P137	N18	556 $\pm$
I/O	P119	P138	N19	559 $\pm$
I/O	P120	P139	N20	562 $\pm$
VCC	P121	P140	VCC*	-
I/O (D5 ‡‡)	P122	P141	M17	565 $\pm$
I/O	P123	P142	M18	568 $\pm$
I/O	-	-	M19	574 $\pm$
I/O	P124	P144	M20	577 $\pm$
I/O	P125	P145	L19	580 $\pm$
I/O	P126	P146	L18	583 $\pm$
I/O	P127	P147	L20	586 $\pm$
I/O (D4 ‡‡)	P128	P148	K20	589 $\pm$
I/O	P129	P149	K19	592 $\pm$
VCC	P130	P150	VCC*	-
GND	P131	P151	GND*	-
I/O (D3 ‡‡)	P132	P152	K18	595 $\pm$
I/O	P133	P153	K17	598 $\pm$
I/O	P134	P154	J20	601 $\pm$
I/O	P135	P155	J19	604 $\pm$
I/O	P136	P156	J18	607 $\pm$
I/O	P137	P157	J17	610 $\pm$
I/O	-	-	H20	613 $\pm$
I/O (D2 ‡‡)	P138	P159	H19	619 $\pm$
I/O	P139	P160	H18	622 $\pm$
VCC	P140	P161	VCC*	-
I/O	P141	P162	G19	625 $\pm$
I/O	P142	P163	F20	628 $\pm$
I/O	-	P164	G18	631 $\pm$
I/O	-	P165	F19	634 $\pm$
GND	P143	P166	GND*	-
I/O	-	P167	F18	637 $\pm$
I/O	P144	P168	E19	640 $\pm$
I/O	P145	P169	D20	643 $\pm$
I/O	P146	P170	E18	646 $\pm$
I/O	P147	P171	D19	649 $\pm$
I/O	P148	P172	C20	652 $\pm$
I/O (D1 ‡‡)	P149	P173	E17	655 $\pm$
I/O	P150	P174	D18	658 $\pm$
I/O	P151	P175	C19	667 $\pm$
I/O	P152	P176	B20	670 $\pm$
I/O (D0 ‡‡, DIN)	P153	P177	C18	673 $\pm$

XCS40/XL Pad Name	PQ208	PQ240	BG256	Bndry Scan
I/O, SGCK4 †, GCK6 †† (DOUT)	P154	P178	B19	676 ‡
CCLK	P155	P179	A20	-
VCC	P156	P180	VCC*	-
O, TDO	P157	P181	A19	0
GND	P158	P182	GND*	-
I/O	P159	P183	B18	2
I/O, PGCK4 †, GCK7 ††	P160	P184	B17	5
I/O	P161	P185	C17	8
I/O	P162	P186	D16	11
I/O (CS1 ††)	P163	P187	A18	14
I/O	P164	P188	A17	17
I/O	P165	P189	C16	26
I/O	-	P190	B16	29
I/O	P166	P191	A16	32
I/O	P167	P192	C15	35
I/O	P168	P193	B15	38
I/O	P169	P194	A15	41
GND	P170	P196	GND*	-
I/O	P171	P197	B14	44
I/O	P172	P198	A14	47
I/O	-	P199	C13	50
I/O	-	P200	B13	53
VCC	P173	P201	VCC*	-
I/O	-	-	A13	56
I/O	-	-	D12	59
I/O	P174	P202	C12	62
I/O	P175	P203	B12	65
I/O	P176	P205	A12	68
I/O	P177	P206	B11	71
I/O	P178	P207	C11	74
I/O	P179	P208	A11	77
I/O	P180	P209	A10	80
I/O	P181	P210	B10	83
GND	P182	P211	GND*	-

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\* Pads labelled GND\* or VCC\* are internally bonded to Ground or VCC planes within the package.

† = 5V Spartan only

†† = 3V SpartanXL only

‡ The "Don't Connect" on the XCS40XL is not part of the Boundary Scan chain. For the XCS40XL, subtract 1 from all Boundary Scan numbers from GCK3 on (343 and higher).

### Additional XCS40/XL Package Pins

#### PQ240

GND Pins					
P22	P37	P83	P98	P143	P158
P204	P219	-	-	-	-
Not Connected Pins					
P195	-	-	-	-	-

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#### BG256

VCC Pins					
C14	D6	D7	D11	D14	D15
E20	F1	F4	F17	G4	G17
K4	L17	P4	P17	P19	R2
R4	R17	U6	U7	U10	U14
U15	V7	W20	-	-	-
GND Pins					
A1	B7	D4	D8	D13	D17
G20	H4	H17	N3	N4	N17
U4	U8	U13	U17	W14	-

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## Product Availability

Table 16 shows the packages and speed grades for Spartan Series devices. Table 17 shows the number of user I/Os available for each device/package combination.

**Table 16: Component Availability Chart for Spartan Series FPGAs**

Device	PINS	84	100	144	208	240	256
	TYPE	Plast. PLCC	Plast. VQFP	Plast. TQFP	Plast. PQFP	Plast. PQFP	Plast. BGA
	CODE	PC84	VQ100	TQ144	PQ208	PQ240	BG256
XCS05	-3	C	C, I				
	-4	C	C				
XCS10	-3	C	C, I	C			
	-4	C	C	C			
XCS20	-3		C	C, I	C, I		
	-4		C	C	C		
XCS30	-3		C	C, I	C, I	C	C
	-4		C	C	C	C	C
XCS40	-3				C, I	C	C
	-4				C	C	C
XCS05XL	-4	C	C, (I)				
	-5	(C)	(C)				
XCS10XL	-4	C	C, (I)	C			
	-5	(C)	(C)	(C)			
XCS20XL	-4		C	C, (I)	C, (I)		
	-5		(C)	(C)	(C)		
XCS30XL	-4		C	C, (I)	C, (I)	C	C
	-5		(C)	(C)	(C)	(C)	(C)
XCS40XL	-4				C, (I)	C	C
	-5				(C)	(C)	(C)

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C = Commercial  $T_J = 0^\circ \text{ to } +85^\circ\text{C}$ I = Industrial  $T_J = -40^\circ\text{C} \text{ to } +100^\circ\text{C}$ 

( ) Parentheses indicate future product plans

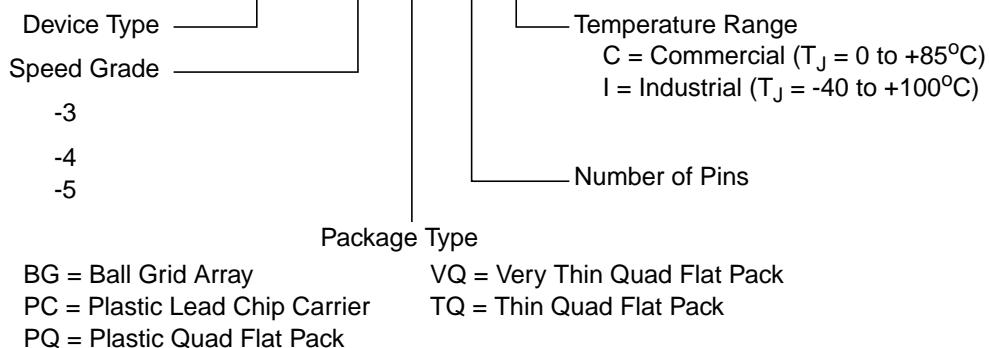
**Table 17: User I/O Chart for Spartan Series FPGAs**

Device	Max I/O	Package Type					
		PC84	VQ100	TQ144	PQ208	PQ240	BG256
XCS05	80	61	77				
XCS10	112	61	77	112			
XCS20	160		77	113	160		
XCS30	192		77	113	169	192	192
XCS40	224				169	193	205
XCS05XL	80	61	77				
XCS10XL	112	61	77	112			
XCS20XL	160		77	113	160		
XCS30XL	192		77	113	169	192	192
XCS40XL	224				169	193	205

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## Ordering Information

### Example: XCS20XL-4 PQ208C



**Table 18: Revisions**

Version	Description
4/2/98	Rev 1.0 (Preliminary) Added timing specifications for 5V devices, updated PQ208 pinout tables, improved description.
5/31/98	Rev 1.1 (Preliminary) Updated all timing specifications.
9/28/98	Rev. 1.2 (Preliminary) Added SpartanXL architecture description, changed speed grades to -4/-5

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April 8, 1998 (Version 5.0)

Product Specification

## Features

- Low-cost, process-optimized, register/latch rich, SRAM based reprogrammable architecture
  - 0.5µm three-layer metal CMOS process technology
  - 256 to 1936 logic cells (3,000 to 23,000 "gates")
  - Price competitive with Gate Arrays
- System Level Features
  - System performance beyond 50 MHz
  - 6 levels of interconnect hierarchy
  - VersaRing™ I/O Interface for pin-locking
  - Dedicated carry logic for high-speed arithmetic functions
  - Cascade chain for wide input functions
  - Built-in IEEE 1149.1 JTAG boundary scan test circuitry on all I/O pins
  - Internal 3-state bussing capability
  - Four dedicated low-skew clock or signal distribution nets
- Versatile I/O and Packaging
  - Innovative VersaRing™ I/O interface provides a high logic cell to I/O ratio, with up to 244 I/O signals
  - Programmable output slew-rate control maximizes performance and reduces noise
  - Zero Flip-Flop hold time for input registers simplifies system timing
  - Independent Output Enables for external bussing
  - Footprint compatibility in common packages within the XC5200 Series and with the XC4000 Series
  - Over 150 device/package combinations, including advanced BGA, TQ, and VQ packaging available

- Fully Supported by XACTstep™ Development System
  - Automatic place and route software
  - Wide selection of PC and Workstation platforms
  - Over 100 3rd-party Alliance interfaces
  - Supported by shrink-wrap Foundation software

## Description

The XC5200 Field-Programmable Gate Array Family is engineered to deliver the lowest cost of any FPGA family. By optimizing the new XC5200 architecture for three-layer metal (TLM) technology and a 0.5-µm CMOS SRAM process, dramatic advances have been made in silicon efficiency. These advances position the XC5200 family as a cost-effective, high-volume alternative to gate arrays.

Building on experiences gained with three previous successful SRAM FPGA families, the XC5200 family brings a robust feature set to high-density programmable logic design. The VersaBlock™ logic module, the VersaRing I/O interface, and a rich hierarchy of interconnect resources combine to enhance design flexibility and reduce time-to-market. Complete support for the XC5200 family is delivered through the familiar XACTstep software environment. The XC5200 family is fully supported on popular workstation and PC platforms. Popular design entry methods are fully supported, including ABEL, schematic capture, VHDL, and Verilog HDL synthesis. Designers utilizing logic synthesis can use their existing tools to design with the XC5200 devices.

Table 2: XC5200 Field-Programmable Gate Array Family Members

Device	XC5202	XC5204	XC5206	XC5210	XC5215
Logic Cells	256	480	784	1,296	1,936
Max Logic Gates	3,000	6,000	10,000	16,000	23,000
Typical Gate Range	2,000 - 3,000	4,000 - 6,000	6,000 - 10,000	10,000 - 16,000	15,000 - 23,000
VersaBlock Array	8 x 8	10 x 12	14 x 14	18 x 18	22 x 22
CLBs	64	120	196	324	484
Flip-Flops	256	480	784	1,296	1,936
I/Os	84	124	148	196	244
TBUFs per Longline	10	14	16	20	24

## XC5200 Family Compared to XC4000 and XC3000 Series

For readers already familiar with the XC4000 and XC3000 FPGA Families, this section describes significant differences between them and the XC5200 family. Unless otherwise indicated, comparisons refer to both XC4000 and XC3000 devices.

### Configurable Logic Block (CLB) Resources

Each XC5200 CLB contains four independent 4-input function generators and four registers, which are configured as four independent Logic Cells™ (LCs). The registers in each XC5200 LC are optionally configurable as edge-triggered D-type flip-flops or as transparent level-sensitive latches.

The XC5200 CLB includes dedicated carry logic that provides fast arithmetic carry capability. The dedicated carry logic may also be used to cascade function generators for implementing wide arithmetic functions.

**XC4000 family:** XC5200 devices have no wide edge decoders. Wide decoders are implemented using cascade logic. Although sacrificing speed for some designs, lack of wide edge decoders reduces the die area and hence cost of the XC5200.

**XC4000 family:** XC5200 dedicated carry logic differs from that of the XC4000 family in that the sum is generated in an additional function generator in the adjacent column. This design reduces XC5200 die size and hence cost for many applications. Note, however, that a loadable up/down counter requires the same number of function generators in both families. XC3000 has no dedicated carry.

**XC4000 family:** XC5200 lookup tables are optimized for cost and hence cannot implement RAM.

### Input/Output Block (IOB) Resources

The XC5200 family maintains footprint compatibility with the XC4000 family, but not with the XC3000 family.

To minimize cost and maximize the number of I/O per Logic Cell, the XC5200 I/O does not include flip-flops or latches.

For high performance paths, the XC5200 family provides direct connections from each IOB to the registers in the adjacent CLB in order to emulate IOB registers.

Each XC5200 I/O Pin provides a programmable delay element to control input set-up time. This element can be used to avoid potential hold-time problems. Each XC5200 I/O Pin is capable of 8-mA source and sink currents.

IEEE 1149.1-type boundary scan is supported in each XC5200 I/O.

**Table 3: Xilinx Field-Programmable Gate Array Families**

Parameter	XC5200	XC4000	XC3000
Function generators per CLB	4	3	2
Logic inputs per CLB	20	9	5
Logic outputs per CLB	12	4	2
Low-skew global buffers	4	8	2
User RAM	no	yes	no
Dedicated decoders	no	yes	no
Cascade chain	yes	no	no
Fast carry logic	yes	yes	no
Internal 3-state drivers	yes	yes	yes
IEEE boundary scan	yes	yes	no
Output slew-rate control	yes	yes	yes

### Routing Resources

The XC5200 family provides a flexible coupling of logic and local routing resources called the VersaBlock. The XC5200 VersaBlock element includes the CLB, a Local Interconnect Matrix (LIM), and direct connects to neighboring VersaBlocks.

The XC5200 provides four global buffers for clocking or high-fanout control signals. Each buffer may be sourced by means of its dedicated pad or from any internal source.

Each XC5200 TBUF can drive up to two horizontal and two vertical Longlines. There are no internal pull-ups for XC5200 Longlines.

### Configuration and Readback

The XC5200 supports a new configuration mode called Express mode, not available in XC4000/E or XC3000 Families.

**XC4000 family:** The XC5200 family provides a global reset but not a global set.

XC5200 devices use a different configuration process than that of the XC3000 family, but use the same process as the XC4000 family.

**XC3000 family:** Although their configuration processes differ, XC5200 devices may be used in daisy chains with XC3000 devices.

**XC3000 family:** The XC5200 PROGRAM pin is a single-function input pin that overrides all other inputs. The program pin does not exist in XC3000.

**XC3000 family:** XC5200 devices support an additional programming mode: Peripheral Synchronous.

**XC3000 family:** The XC5200 family does not support Power-down, but offers a Global 3-state input that does not reset any flip-flops.

**XC3000 family:** The XC5200 family does not provide an on-chip crystal oscillator amplifier, but it does provide an internal oscillator from which a variety of frequencies up to 12 MHz are available.

## Architectural Overview

Figure 2 presents a simplified, conceptual overview of the XC5200 architecture. Similar to conventional FPGAs, the XC5200 family consists of programmable IOBs, programmable logic blocks, and programmable interconnect. Unlike other FPGAs, however, the logic and local routing resources of the XC5200 family are combined in flexible VersaBlocks (Figure 3). General-purpose routing connects to the VersaBlock through the General Routing Matrix (GRM).

## VersaBlock: Abundant Local Routing Plus Versatile Logic

The basic logic element in each VersaBlock structure is the Logic Cell, shown in Figure 4. Each LC contains a 4-input function generator (F), a storage device (FD), and control logic. There are five independent inputs and three outputs to each LC. The independence of the inputs and outputs allows the software to maximize the resource utilization within each LC. Each Logic Cell also contains a direct feedthrough path that does not sacrifice the use of either the function generator or the register; this feature is a first for FPGAs. The storage device is configurable as either a D flip-flop or a latch. The control logic consists of carry logic for fast implementation of arithmetic functions, which can also be configured as a cascade chain allowing decode of very wide input functions.

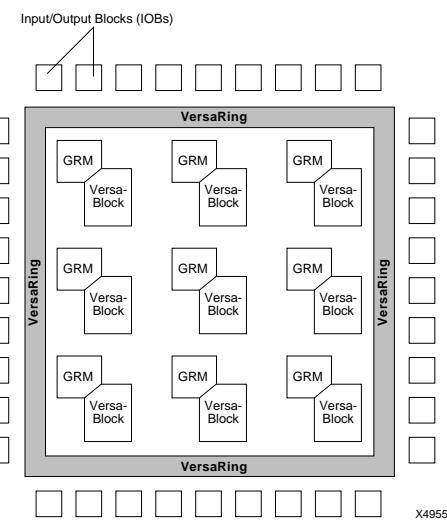


Figure 2: XC5200 Architectural Overview

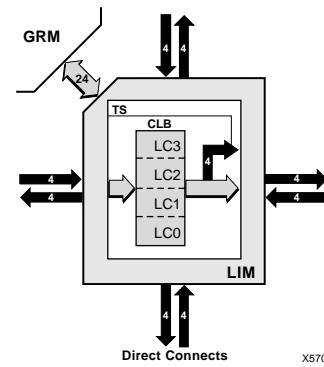


Figure 3: VersaBlock

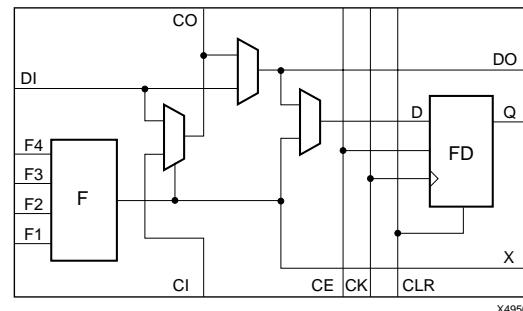
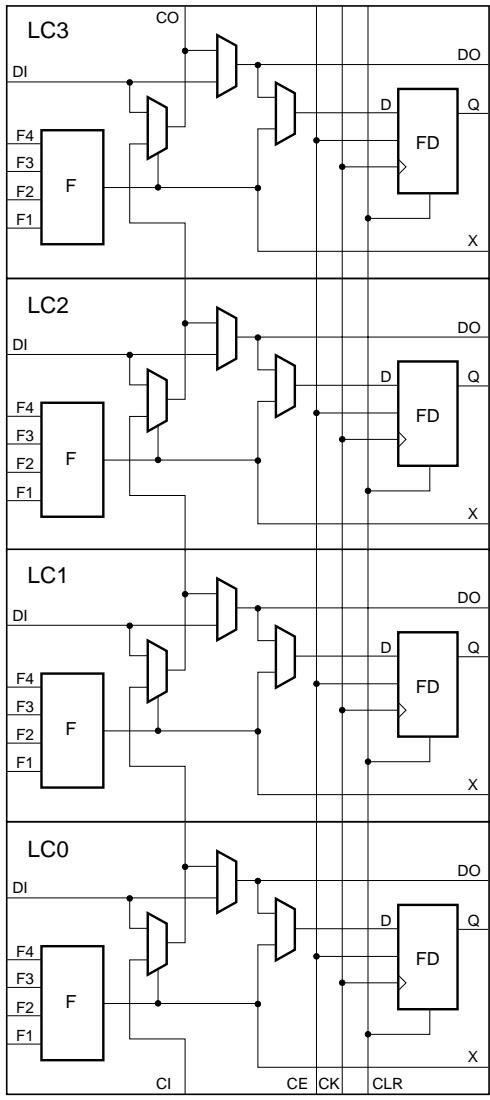


Figure 4: XC5200 Logic Cell (Four LCs per CLB)

The XC5200 CLB consists of four LCs, as shown in [Figure 5](#). Each CLB has 20 independent inputs and 12 independent outputs. The top and bottom pairs of LCs can be configured to implement 5-input functions. The challenge of FPGA implementation software has always been to maximize the usage of logic resources. The XC5200 family addresses this issue by surrounding each CLB with two types of local interconnect — the Local Interconnect Matrix (LIM) and direct connects. These two interconnect resources, combined with the CLB, form the VersaBlock, represented in [Figure 3](#).



**Figure 5: Configurable Logic Block**

The LIM provides 100% connectivity of the inputs and outputs of each LC in a given CLB. The benefit of the LIM is that no general routing resources are required to connect feedback paths within a CLB. The LIM connects to the GRM via 24 bidirectional nodes.

The direct connects allow immediate connections to neighboring CLBs, once again without using any of the general interconnect. These two layers of local routing resource improve the granularity of the architecture, effectively making the XC5200 family a “sea of logic cells.” Each VersaBlock has four 3-state buffers that share a common enable line and directly drive horizontal and vertical Longlines, creating robust on-chip bussing capability. The VersaBlock allows fast, local implementation of logic functions, effectively implementing user designs in a hierarchical fashion. These resources also minimize local routing congestion and improve the efficiency of the general interconnect, which is used for connecting larger groups of logic. It is this combination of both fine-grain and coarse-grain architecture attributes that maximize logic utilization in the XC5200 family. This symmetrical structure takes full advantage of the third metal layer, freeing the placement software to pack user logic optimally with minimal routing restrictions.

## VersaRing I/O Interface

The interface between the IOBs and core logic has been redesigned in the XC5200 family. The IOBs are completely decoupled from the core logic. The XC5200 IOBs contain dedicated boundary-scan logic for added board-level testability, but do not include input or output registers. This approach allows a maximum number of IOBs to be placed around the device, improving the I/O-to-gate ratio and decreasing the cost per I/O. A “freeway” of interconnect cells surrounding the device forms the VersaRing, which provides connections from the IOBs to the internal logic. These incremental routing resources provide abundant connections from each IOB to the nearest VersaBlock, in addition to Longline connections surrounding the device. The VersaRing eliminates the historic trade-off between high logic utilization and pin placement flexibility. These incremental edge resources give users increased flexibility in preassigning (i.e., locking) I/O pins before completing their logic designs. This ability accelerates time-to-market, since PCBs and other system components can be manufactured concurrent with the logic design.

## General Routing Matrix

The GRM is functionally similar to the switch matrices found in other architectures, but it is novel in its tight coupling to the logic resources contained in the VersaBlocks. Advanced simulation tools were used during the development of the XC5200 architecture to determine the optimal level of routing resources required. The XC5200 family contains six levels of interconnect hierarchy — a series of single-length lines, double-length lines, and Longlines all

routed through the GRM. The direct connects, LIM, and logic-cell feedthrough are contained within each Versa-Block. Throughout the XC5200 interconnect, an efficient multiplexing scheme, in combination with three layer metal (TLM), was used to improve the overall efficiency of silicon usage.

## Performance Overview

The XC5200 family has been benchmarked with many designs running synchronous clock rates beyond 66 MHz. The performance of any design depends on the circuit to be implemented, and the delay through the combinatorial and sequential logic elements, plus the delay in the interconnect routing. A rough estimate of timing can be made by assuming 3-6 ns per logic level, which includes direct-connect routing delays, depending on speed grade. More accurate estimations can be made using the information in the Switching Characteristic Guideline section.

## Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

## Detailed Functional Description

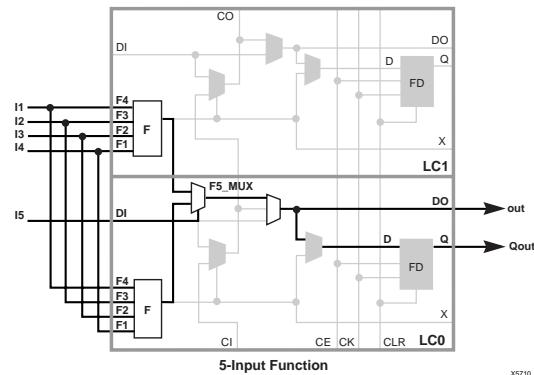
### Configurable Logic Blocks (CLBs)

Figure 5 shows the logic in the XC5200 CLB, which consists of four Logic Cells (LC[3:0]). Each Logic Cell consists of an independent 4-input Lookup Table (LUT), and a D-Type flip-flop or latch with common clock, clock enable, and clear, but individually selectable clock polarity. Additional logic features provided in the CLB are:

- An independent 5-input LUT by combining two 4-input LUTs.
- High-speed carry propagate logic.
- High-speed pattern decoding.
- High-speed direct connection to flip-flop D-inputs.
- Individual selection of either a transparent, level-sensitive latch or a D flip-flop.
- Four 3-state buffers with a shared Output Enable.

### 5-Input Functions

Figure 6 illustrates how the outputs from the LUTs from LC0 and LC1 can be combined with a 2:1 multiplexer (F5\_MUX) to provide a 5-input function. The outputs from the LUTs of LC2 and LC3 can be similarly combined.



**Figure 6: Two LUTs in Parallel Combined to Create a 5-input Function**

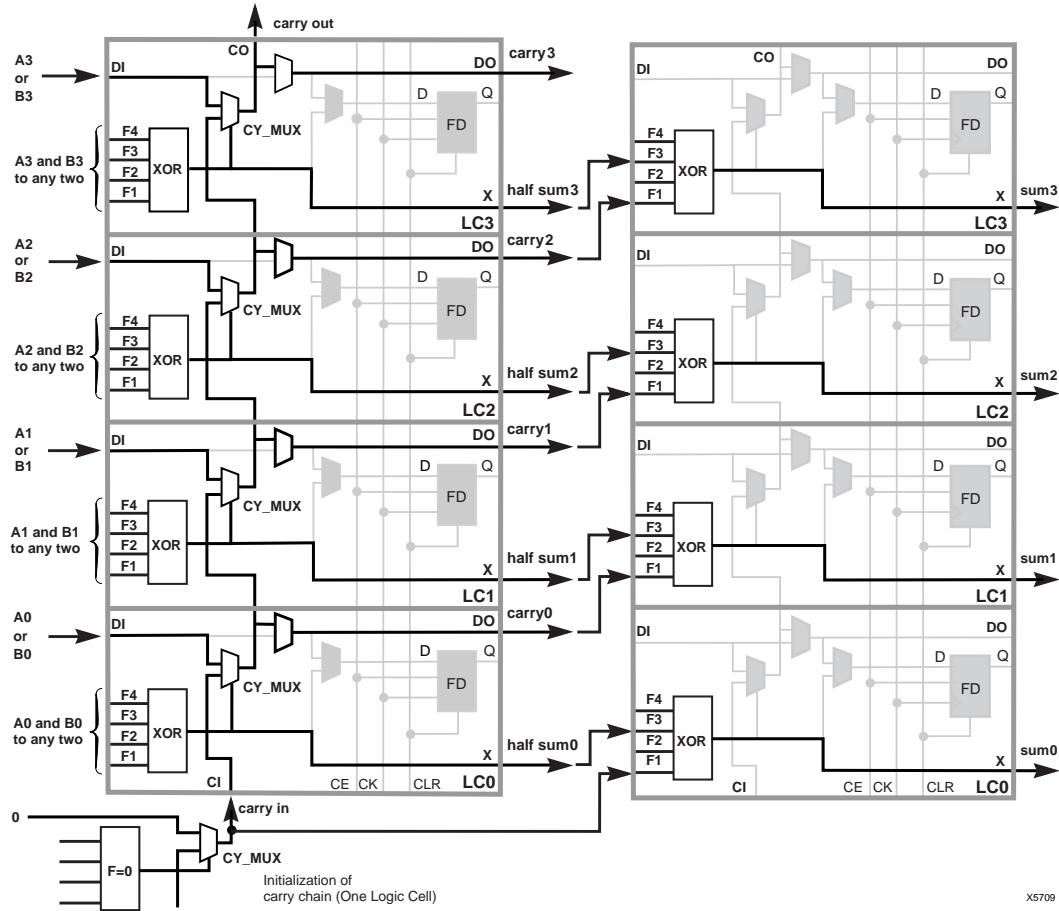


Figure 7: XC5200 CY\_MUX Used for Adder Carry Propagate

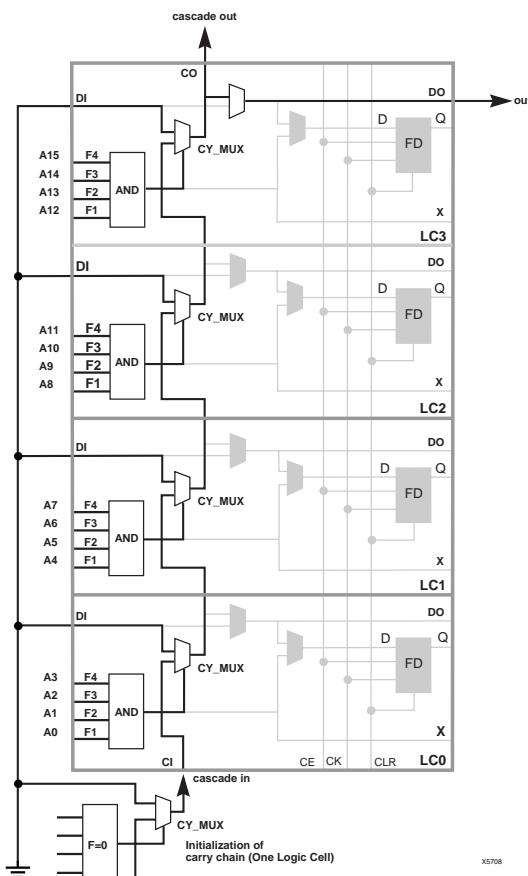
### Carry Function

The XC5200 family supports a carry-logic feature that enhances the performance of arithmetic functions such as counters, adders, etc. A carry multiplexer (CY\_MUX) symbol is used to indicate the XC5200 carry logic. This symbol represents the dedicated 2:1 multiplexer in each LC that performs the one-bit high-speed carry propagate per logic cell (four bits per CLB).

While the carry propagate is performed inside the LC, an adjacent LC must be used to complete the arithmetic function. Figure 7 represents an example of an adder function. The carry propagate is performed on the CLB shown, which also generates the half-sum for the four-bit adder. An adjacent CLB is responsible for XORing the half-sum with the corresponding carry-out. Thus an adder or counter

requires two LCs per bit. Notice that the carry chain requires an initialization stage, which the XC5200 family accomplishes using the carry initialize (CY\_INIT) macro and one additional LC. The carry chain can propagate vertically up a column of CLBs.

The XC5200 library contains a set of Relationally-Placed Macros (RPMs) and arithmetic functions designed to take advantage of the dedicated carry logic. Using and modifying these macros makes it much easier to implement customized RPMs, freeing the designer from the need to become an expert on architectures.



**Figure 8: XC5200 CY\_MUX Used for Decoder Cascade Logic**

## Cascade Function

Each CY\_MUX can be connected to the CY\_MUX in the adjacent LC to provide cascadable decode logic. **Figure 8** illustrates how the 4-input function generators can be configured to take advantage of these four cascaded CY\_MUXes. Note that AND and OR cascading are specific cases of a general decode. In AND cascading all bits are decoded equal to logic one, while in OR cascading all bits are decoded equal to logic zero. The flexibility of the LUT achieves this result. The XC5200 library contains gate macros designed to take advantage of this function.

## CLB Flip-Flops and Latches

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in flip-flops, and connect their outputs to the interconnect network as well. The CLB storage elements can also be configured as latches.

**Table 4: CLB Storage Element Functionality  
(active rising edge is shown)**

Mode	CK	CE	CLR	D	Q
Power-Up or GR	X	X	X	X	0
Flip-Flop	X	X	1	X	0
	/\	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

### Legend:

X	Don't care
/\	Rising edge
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

## Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by the function F, or by the Direct In (DI) block input. The flip-flops or latches drive the Q CLB outputs.

Four fast feed-through paths from DI to DO are available, as shown in **Figure 5**. This bypass is sometimes used by the automated router to repower internal signals. In addition to the storage element (Q) and direct (DO) outputs, there is a combinatorial output (X) that is always sourced by the Lookup Table.

The four edge-triggered D-type flip-flops or level-sensitive latches have common clock (CK) and clock enable (CE) inputs. Any of the clock inputs can also be permanently enabled. Storage element functionality is described in **Table 4**.

## Clock Input

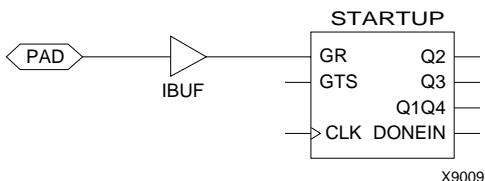
The flip-flops can be triggered on either the rising or falling clock edge. The clock pin is shared by all four storage elements with individual polarity control. Any inverter placed on the clock input is automatically absorbed into the CLB.

## Clock Enable

The clock enable signal (CE) is active High. The CE pin is shared by the four storage elements. If left unconnected for any, the clock enable for that storage element defaults to the active state. CE is not invertible within the CLB.

## Clear

An asynchronous storage element input (CLR) can be used to reset all four flip-flops or latches in the CLB. This input can also be independently disabled for any flip-flop. CLR is active High. It is not invertible within the CLB.

**Figure 9: Schematic Symbols for Global Reset**

### Global Reset

A separate Global Reset line clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GR) does not compete with other routing resources; it uses a dedicated distribution network.

GR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GR pin of the STARTUP symbol. (See [Figure 9](#).) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Reset signal. Alternatively, GR can be driven from any internal node.

### Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC5200 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

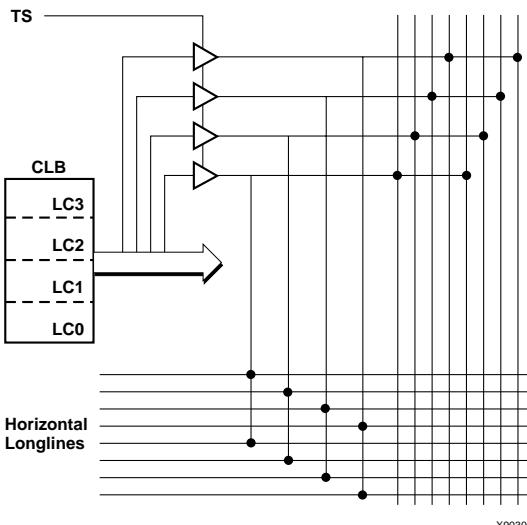
To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol is called LDCE.

In XC5200-Series devices, the flip-flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input CK. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

### Three-State Buffers

The XC5200 family has four dedicated Three-State Buffers (TBUFs, or BUFTs in the schematic library) per CLB (see [Figure 10](#)). The four buffers are individually configurable through four configuration bits to operate as simple non-inverting buffers or in 3-state mode. When in 3-state mode the CLB output enable (TS) control signal drives the enable to all four buffers. Each TBUF can drive up to two horizontal and/or two vertical Longlines. These 3-state buffers can be used to implement multiplexed or bidirectional buses on the horizontal or vertical longlines, saving logic resources.

**Figure 10: XC5200 3-State Buffers**

The 3-state buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in [Table 5](#).

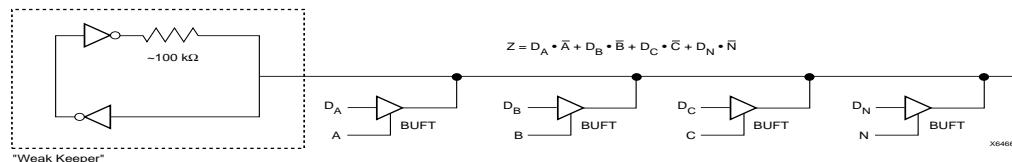
Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array.

The longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver. To ensure the longline goes high when no buffers are on, add an additional BUFT to drive the output High during all of the previously undefined states.

[Figure 11](#) shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

**Table 5: Three-State Buffer Functionality**

IN	T	OUT
X	1	Z
IN	0	IN

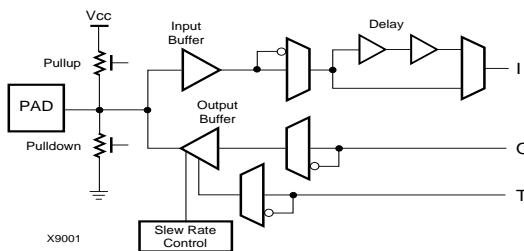


**Figure 11:** 3-State Buffers Implement a Multiplexer

## Input/Output Blocks

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

The I/O block, shown in [Figure 12](#), consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible. The input buffer has globally selected CMOS or TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.



**Figure 12:** XC5200 I/O Block

### IOB Input Signals

The XC5200 inputs can be globally configured for either TTL (1.2V) or CMOS thresholds, using an option in the bit-stream generation software. There is a slight hysteresis of about 300mV.

The inputs of XC5200-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC5200-Series device inputs are shown in [Table 6](#).

**Table 6: Supported Sources for XC5200-Series Device Inputs**

Source	XC5200 Input Mode	
	5 V, TTL	5 V, CMOS
Any device, Vcc = 3.3 V, CMOS outputs	✓	<b>Unreliable Data</b>
Any device, Vcc = 5 V, TTL outputs	✓	
Any device, Vcc = 5 V, CMOS outputs	✓	✓

### Optional Delay Guarantees Zero Hold Time

XC5200 devices do not have storage elements in the IOBs. However, XC5200 IOBs can be efficiently routed to CLB flip-flops or latches to store the I/O signals.

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the CLB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the CLB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the software default.

The XC5200 IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC5200 global clock buffers. (See ["Global Lines" on page 260](#) for a description of the global clock buffers in the XC5200.) For a shorter input register setup time, with non-zero hold, attach a NODELAY attribute or property to the flip-flop or input buffer.

## IOB Output Signals

Output signals can be optionally inverted within the IOB, and pass directly to the pad. As with the inputs, a CLB flip-flop or latch can be used to store the output signal.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The XC5200 devices provide a guaranteed output sink current of 8 mA.

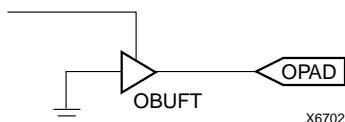
Supported destinations for XC5200-Series device outputs are shown in [Table 7](#). (For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See [Figure 13](#).)

**Table 7: Supported Destinations for XC5200-Series Outputs**

Destination	XC5200 Output Mode
	5 V, CMOS
XC5200 device, $V_{CC}=3.3$ V, CMOS-threshold inputs	✓
Any typical device, $V_{CC} = 3.3$ V, CMOS-threshold inputs	some <sup>1</sup>
Any device, $V_{CC} = 5$ V, TTL-threshold inputs	✓
Any device, $V_{CC} = 5$ V, CMOS-threshold inputs	✓

1. Only if destination device has 5-V tolerant inputs



**Figure 13: Open-Drain Output**

## Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC5200 devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is

200 pF for all package pins between each Power/Ground pin pair. For some XC5200 devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC5200 devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC5200 Series.

XC5200-Series devices have a feature called “Soft Startup,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

## Global Three-State

A separate Global 3-State line (not shown in [Figure 12](#)) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to Global Reset. See [Figure 9 on page 254](#) for details. Alternatively, GTS can be driven from any internal node.

## Other IOB Options

There are a number of other programmable options in the XC5200-Series IOB.

## Pull-up and Pull-down Resistors

Programmable IOB pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is  $20\text{ k}\Omega - 100\text{ k}\Omega$ . This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See [Table 14 on page 288](#) for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

#### JTAG Support

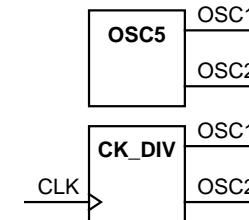
Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, simplifying board-level testing. More information is provided in [“Boundary Scan” on page 262](#).

#### Oscillator

XC5200 devices include an internal oscillator. This oscillator is used to clock the power-on time-out, clear configuration memory, and source CCLK in Master configuration modes. The oscillator runs at a nominal 12 MHz frequency that varies with process, V<sub>cc</sub>, and temperature. The output CCLK frequency is selectable as 1 MHz (default), 6 MHz, or 12 MHz.

The XC5200 oscillator divides the internal 12-MHz clock or a user clock. The user then has the choice of dividing by 4, 16, 64, or 256 for the “OSC1” output and dividing by 2, 8, 32, 128, 1024, 4096, 16384, or 65536 for the “OSC2” output. The division is specified via a “DIVIDE<sub>n</sub>\_BY=x” attribute on the symbol, where n=1 for OSC1, or n=2 for OSC2. These frequencies can vary by as much as -50% or + 50%.

The OSC5 macro is used where an internal oscillator is required. The CK\_DIV macro is applicable when a user clock input is specified (see [Figure 14](#)).



**Figure 14:** XC5200 Oscillator Macros

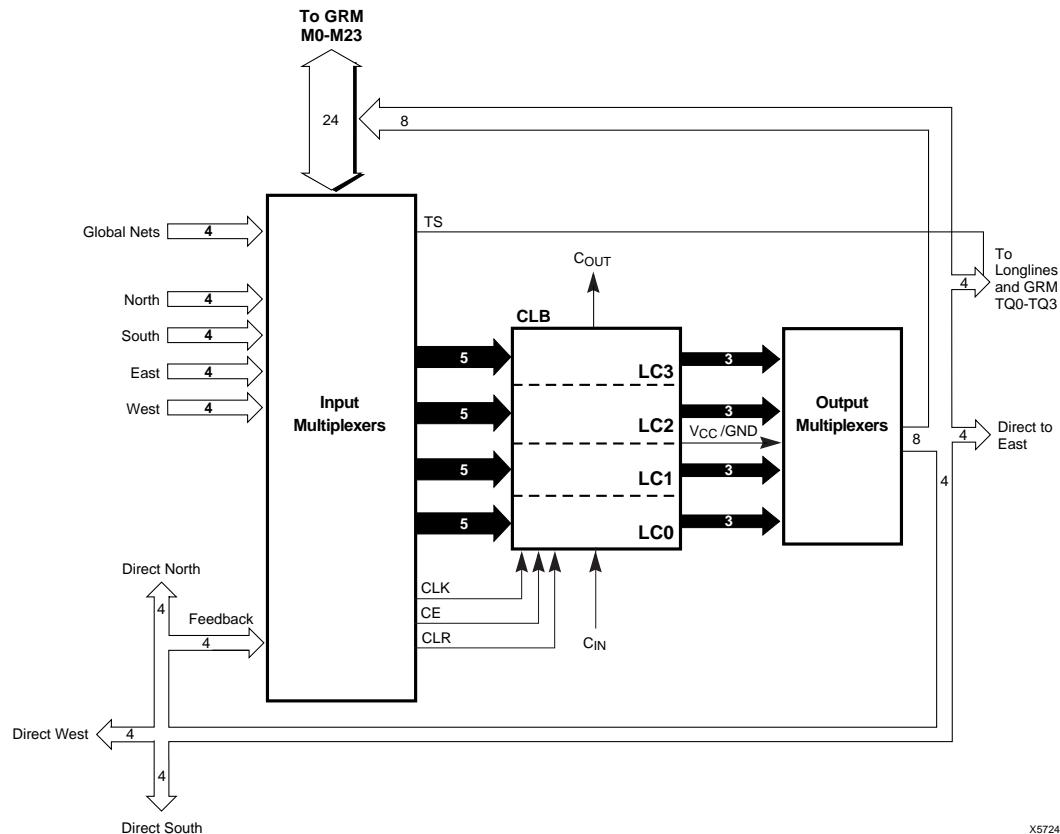
#### VersaBlock Routing

The General Routing Matrix (GRM) connects to the VersaBlock via 24 bidirectional ports (M0-M23). Excluding direct connections, global nets, and 3-statable Longlines, all VersaBlock inputs and outputs connect to the GRM via these 24 ports. Four 3-statable unidirectional signals (TQ0-TQ3) drive out of the VersaBlock directly onto the horizontal and vertical Longlines. Two horizontal global nets and two vertical global nets connect directly to every CLB clock pin; they can connect to other CLB inputs via the GRM. Each CLB also has four unidirectional direct connects to each of its four neighboring CLBs. These direct connects can also feed directly back to the CLB (see [Figure 15](#)).

In addition, each CLB has 16 direct inputs, four direct connections from each of the neighboring CLBs. These direct connections provide high-speed local routing that bypasses the GRM.

#### Local Interconnect Matrix

The Local Interconnect Matrix (LIM) is built from input and output multiplexers. The 13 CLB outputs (12 LC outputs plus a V<sub>cc</sub>/GND signal) connect to the eight VersaBlock outputs via the output multiplexers, which consist of eight fully populated 13-to-1 multiplexers. Of the eight VersaBlock outputs, four signals drive each neighboring CLB directly, and provide a direct feedback path to the input multiplexers. The four remaining multiplexer outputs can drive the GRM through four TBUFs (TQ0-TQ3). All eight multiplexer outputs can connect to the GRM through the bidirectional M0-M23 signals. All eight signals also connect to the input multiplexers and are potential inputs to that CLB.



X5724

**Figure 15: VersaBlock Details**

CLB inputs have several possible sources: the 24 signals from the GRM, 16 direct connections from neighboring VersaBlocks, four signals from global, low-skew buffers, and the four signals from the CLB output multiplexers. Unlike the output multiplexers, the input multiplexers are not fully populated; i.e., only a subset of the available signals can be connected to a given CLB input. The flexibility of LUT input swapping and LUT mapping compensates for this limitation. For example, if a 2-input NAND gate is required, it can be mapped into any of the four LUTs, and use any two of the four inputs to the LUT.

## Direct Connects

The unidirectional direct-connect segments are connected to the logic input/output pins through the CLB input and output multiplexer arrays, and thus bypass the general routing matrix altogether. These lines increase the routing channel utilization, while simultaneously reducing the delay incurred in speed-critical connections.

The direct connects also provide a high-speed path from the edge CLBs to the VersaRing input/output buffers, and thus reduce pin-to-pin set-up time, clock-to-out, and combinational propagation delay. Direct connects from the input buffers to the CLB DI pin (direct flip-flop input) are only available on the left and right edges of the device. CLB look-up table inputs and combinatorial/registered outputs have direct connects to input/output buffers on all four sides.

The direct connects are ideal for developing customized RPM cells. Using direct connects improves the macro performance, and leaves the other routing channels intact for improved routing. Direct connects can also route through a CLB using one of the four cell-feedthrough paths.

## General Routing Matrix

The General Routing Matrix, shown in [Figure 16](#), provides flexible bidirectional connections to the Local Interconnect Matrix through a hierarchy of different-length metal segments in both the horizontal and vertical directions. A pro-

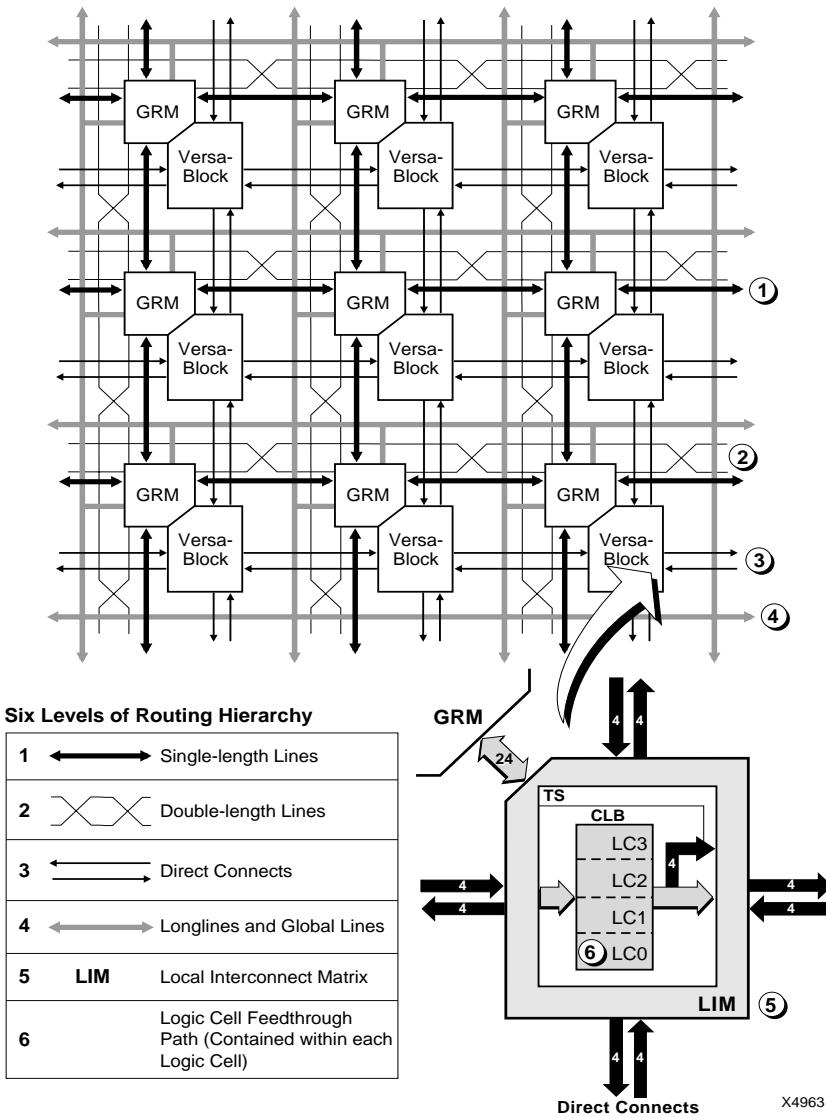


Figure 16: XC5200 Interconnect Structure

grammable interconnect point (PIP) establishes an electrical connection between two wire segments. The PIP, consisting of a pass transistor switch controlled by a memory element, provides bidirectional (in some cases, unidirectional) connection between two adjoining wires. A collection of PIPs inside the General Routing Matrix and in the Local Interconnect Matrix provides connectivity between various types of metal segments. A hierarchy of PIPs and associated routing segments combine to provide a powerful interconnect hierarchy:

- Forty bidirectional single-length segments per CLB

provide ten routing channels to each of the four neighboring CLBs in four directions.

- Sixteen bidirectional double-length segments per CLB provide four routing channels to each of four other (non-neighboring) CLBs in four directions.
- Eight horizontal and eight vertical bidirectional Longline segments span the width and height of the chip, respectively.

Two low-skew horizontal and vertical unidirectional global-line segments span each row and column of the chip, respectively.

## Single- and Double-Length Lines

The single- and double-length bidirectional line segments make up the bulk of the routing channels. The double-length lines hop across every other CLB to reduce the propagation delays in speed-critical nets. Regenerating the signal strength is recommended after traversing three or four such segments. XACTstep place-and-route software automatically connects buffers in the path of the signal as necessary. Single- and double-length lines cannot drive onto Longlines and global lines; Longlines and global lines can, however, drive onto single- and double-length lines. As a general rule, Longline and global-line connections to the general routing matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

### Longlines

Longlines are used for high-fan-out signals, 3-state busses, low-skew nets, and faraway destinations. Row and column splitter PIPs in the middle of the array effectively double the total number of Longlines by electrically dividing them into two separated half-lines. Longlines are driven by the 3-state buffers in each CLB, and are driven by similar buffers at the periphery of the array from the VersaRing I/O Interface.

Bus-oriented designs are easily implemented by using Longlines in conjunction with the 3-state buffers in the CLB and in the VersaRing. Additionally, weak keeper cells at the periphery retain the last valid logic level on the Longlines when all buffers are in 3-state mode.

Longlines connect to the single-length or double-length lines, or to the logic inside the CLB, through the General Routing Matrix. The only manner in which a Longline can be driven is through the four 3-state buffers; therefore, a Longline-to-Longline or single-line-to-Longline connection through PIPs in the General Routing Matrix is not possible. Again, as a general rule, long- and global-line connections to the General Routing Matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

The XC5200 family has no pull-ups on the ends of the Longlines sourced by TBUFs, unlike the XC4000 Series. Consequently, wired functions (i.e., WAND and WORAND) and wide multiplexing functions requiring pull-ups for undefined states (i.e., bus applications) must be implemented in a different way. In the case of the wired functions, the same functionality can be achieved by taking advantage of the carry/cascade logic described above, implementing a wide logic function in place of the wired function. In the case of 3-state bus applications, the user must insure that all states of the multiplexing function are defined. This process is as

simple as adding an additional TBUF to drive the bus High when the previously undefined states are activated.

## Global Lines

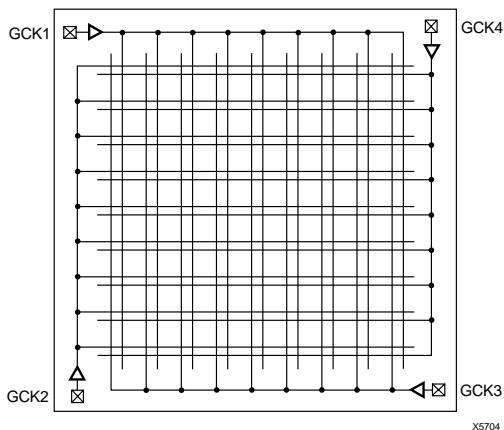
Global buffers in Xilinx FPGAs are special buffers that drive a dedicated routing network called Global Lines, as shown in [Figure 17](#). This network is intended for high-fanout clocks or other control signals, to maximize speed and minimize skewing while distributing the signal to many loads.

The XC5200 family has a total of four global buffers (BUFG symbol in the library), each with its own dedicated routing channel. Two are distributed vertically and two horizontally throughout the FPGA.

The global lines provide direct input only to the CLB clock pins. The global lines also connect to the General Routing Matrix to provide access from these lines to the function generators and other control signals.

Four clock input pads at the corners of the chip, as shown in [Figure 17](#), provide a high-speed, low-skew clock network to each of the four global-line buffers. In addition to the dedicated pad, the global lines can be sourced by internal logic. PIPs from several routing channels within the VersaRing can also be configured to drive the global-line buffers.

Details of all the programmable interconnect for a CLB is shown in [Figure 18](#).



**Figure 17: Global Lines**

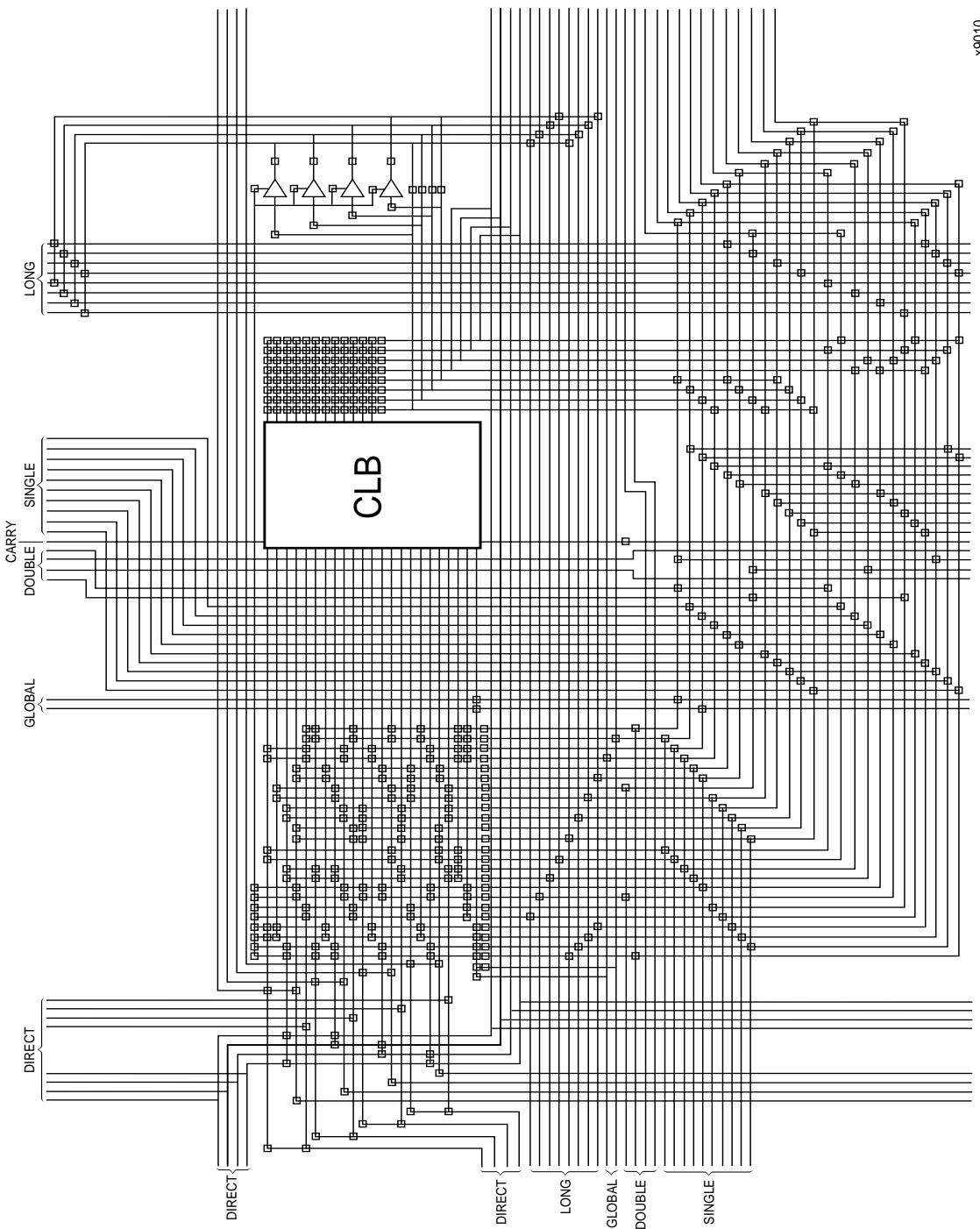
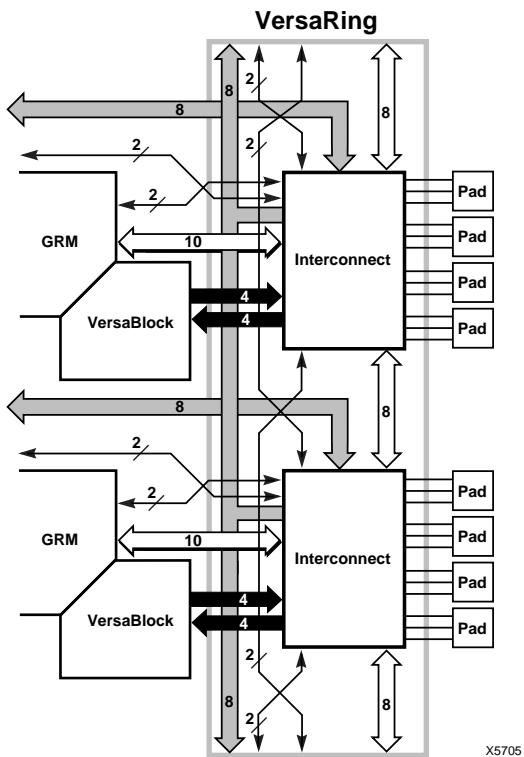


Figure 18: Detail of Programmable Interconnect Associated with XC5200 Series CLB

## VersaRing Input/Output Interface

The VersaRing, shown in [Figure 19](#), is positioned between the core logic and the pad ring; it has all the routing resources of a VersaBlock without the CLB logic. The VersaRing decouples the core logic from the I/O pads. Each VersaRing Cell provides up to four pad-cell connections on one side, and connects directly to the CLB ports on the other side.



**Figure 19:** VersaRing I/O Interface

## Boundary Scan

The “bed of nails” has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE boundary scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP can also support two USERCODE instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability after configuration provides flexibility for interconnect testing.

Also, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This technique partially compensates for the lack of INTEST support.

The user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

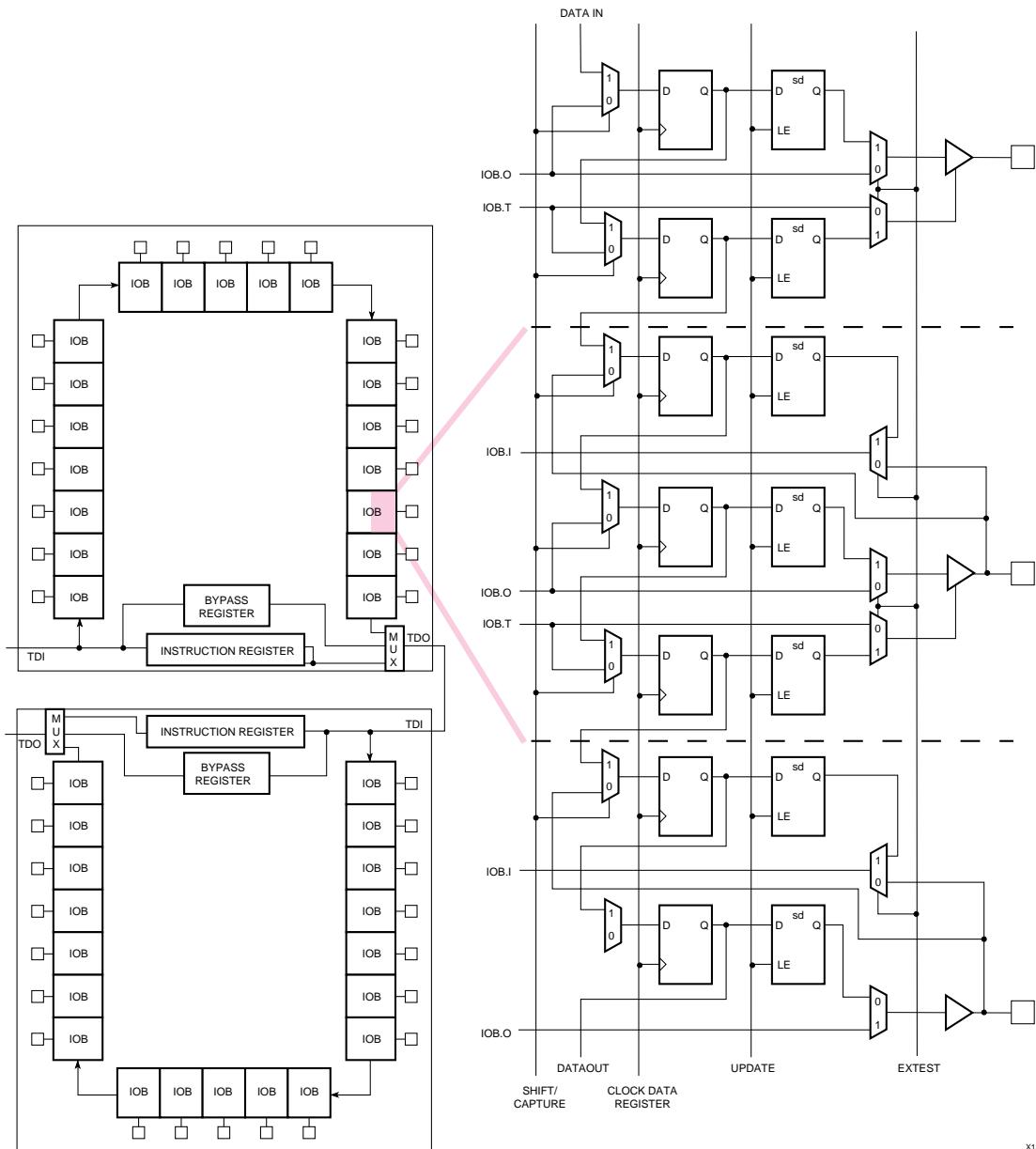
The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: *“Boundary Scan in XC4000 and XC5200 Series devices”*

[Figure 20 on page 263](#) is a diagram of the XC5200-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA device, and to read back the configuration data.

All of the XC4000 boundary-scan modes are supported in the XC5200 family. Three additional outputs for the User-Register are provided (Reset, Update, and Shift), representing the decoding of the corresponding state of the boundary-scan internal state machine.



**Figure 20: XC5200-Series Boundary Scan Logic**

X1523

XC5200-Series devices can also be configured through the boundary scan logic. See XAPP 017 for more information.

## Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-State pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions, USER1 and USER2. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

## Instruction Set

The XC5200-Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in [Table 8](#).

**Table 8: Boundary Scan Instructions**

Instruction I2 I1 I0			Test Selected	TDO Source	I/O Data Source
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	BYPASS	Bypass Register	—

## Bit Sequence

The bit sequence within each IOB is: 3-State, Out, In. The data-register cells for the TAP pins TMS, TCK, and TDI have an OR-gate that permanently disables the output buffer if boundary-scan operation is selected. Consequently, it is impossible for the outputs in IOBs used by TAP inputs to conflict with TAP operation. TAP data is taken directly from the pin, and cannot be overwritten by injected boundary-scan data.

The primary global clock inputs (PGCK1-PGCK4) are taken directly from the pins, and cannot be overwritten with boundary-scan data. However, if necessary, it is possible to drive the clock input from boundary scan. The external clock source is 3-stated, and the clock net is driven with boundary scan data through the output driver in the clock-pad IOB. If the clock-pad IOBs are used for non-clock signals, the data may be overwritten normally.

Pull-up and pull-down resistors remain active during boundary scan. Before and during configuration, all pins are pulled up. After configuration, the choice of internal pull-up or pull-down resistor must be taken into account when designing test vectors to detect open-circuit PC traces.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in [Table 9](#). The device-specific pinout tables for the XC5200 Series include the boundary scan locations for each IOB pin.

**Table 9: Boundary Scan Bit Sequence**

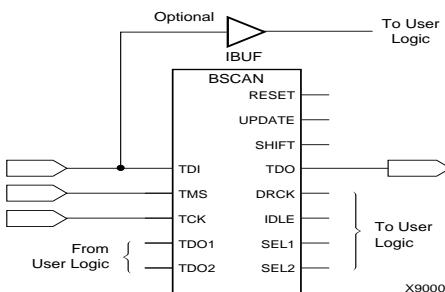
Bit Position	I/O Pad Location
Bit 0 (TDO)	Top-edge I/O pads (right to left)
Bit 1	...
...	Left-edge I/O pads (top to bottom)
...	Bottom-edge I/O pads (left to right)
...	Right-edge I/O pads (bottom to top)
Bit N (TDI)	BSCANT.UPD

BSDL (Boundary Scan Description Language) files for XC5200-Series devices are available on the Xilinx web site in the File Download area.

## Including Boundary Scan

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, include the BSCAN library symbol and connect pad symbols to the TDI, TMS, TCK and TDO pins, as shown in [Figure 21](#).



**Figure 21: Boundary Scan Schematic Example**

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

### Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017, “*Boundary Scan in XC4000 and XC5200 Devices*.“

## Power Distribution

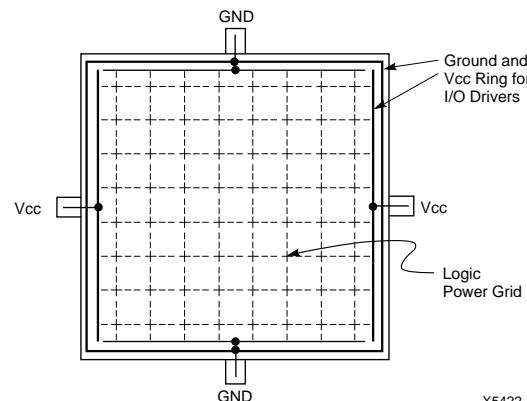
Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in [Figure 22](#). An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1  $\mu$ F capacitor connected near the Vcc and

Ground pins of the package will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 8 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.



**Figure 22: XC5200-Series Power Distribution**

## Pin Descriptions

There are three types of pins in the XC5200-Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated and pulled high with a 20 k $\Omega$  - 100 k $\Omega$  pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 20 k $\Omega$  - 100 k $\Omega$  pull-up resistor.

Device pins for XC5200-Series devices are described in [Table 10](#). Pin functions during configuration for each of the seven configuration modes are summarized in “[Pin Functions During Configuration](#)” on page 288, in the “Configuration Timing” section.

**Table 10: Pin Descriptions**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
<b>Permanently Dedicated Pins</b>			
VCC	I	I	Five or more (depending on package) connections to the nominal +5 V supply voltage. All must be connected, and each must be decoupled with a 0.01 - 0.1 $\mu$ F capacitor to Ground.
GND	I	I	Four or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode, Synchronous Peripheral mode, and Express mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC5200-Series devices, except during Readback. See " <a href="#">Violating the Maximum High and Low Time Specification for the Readback Clock</a> " on page 277 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The exact timing, the clock source for the Low-to-High transition, and the optional pull-up resistor are selected as options in the XACTstep program that creates the configuration bitstream. The resistor is included by default.
PROGRAM	I	I	PROGRAM is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When PROGRAM goes High, the FPGA executes a complete clear cycle, before it goes into a WAIT state and releases INIT. The PROGRAM pin has an optional weak pull-up after configuration.
<b>User I/O Pins That Can Have Special Functions</b>			
RDY/BUSY	O	I/O	During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/BUSY is a user-programmable I/O pin. RDY/BUSY is pulled High with a high-impedance pull-up prior to INIT going High.
RCLK	O	I/O	During Master Parallel configuration, each change on the A0-A17 outputs is preceded by a rising edge on RCLK, a redundant output signal. RCLK is useful for clocked PROMs. It is rarely used during configuration. After configuration, RCLK is a user-programmable I/O pin.
M0, M1, M2	I	I/O	As Mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used. After configuration, M0, M1, and M2 become user-programmable I/O. During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. A pull-down resistor value of 4.7 k $\Omega$ is recommended for other modes.
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output, after configuration is completed. This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

Table 10: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special schematic definitions. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
LDC	O	I/O	Low During Configuration (LDC) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, LDC is a user-programmable I/O pin.
INIT	I/O	I/O	Before and during configuration, INIT is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active-Low open-drain output, INIT is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 50 to 250 μs after INIT has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, INIT is a user-programmable I/O pin.
GCK1 - GCK4	Weak Pull-up	I or I/O	Four Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK4 pins provide the shortest path to the four Global Buffers. Any input pad symbol connected directly to the input of a BUFG symbol is automatically placed on one of these pins.
CS0, CS1, WS, RS	I	I/O	These four inputs are used in Asynchronous Peripheral mode. The chip is selected when CS0 is Low and CS1 is High. While the chip is selected, a Low on Write Strobe (WS) loads the data present on the D0 - D7 inputs into the internal data buffer. A Low on Read Strobe (RS) changes D7 into a status output — High if Ready, Low if Busy — and drives D0 - D6 High. In Express mode, CS1 is used as a serial-enable signal for daisy-chaining. WS and RS should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.
A0 - A17	O	I/O	During Master Parallel configuration, these 18 output pins address the configuration EPROM. After configuration, they are user-programmable I/O pins.
D0 - D7	I	I/O	During Master Parallel, Peripheral, and Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. During Parallel configuration, DIN is the D0 input. After configuration, DIN is a user-programmable I/O pin.
DOUT	O	I/O	During configuration in any mode but Express mode, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK. In Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.

**Table 10: Pin Descriptions (Continued)**

Pin Name	I/O During Config.	I/O After Config.	Pin Description
<b>Unrestricted User-Programmable I/O Pins</b>			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (20 kΩ - 100 kΩ) that defines the logic level as High.

## Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC5200-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT-step development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

### Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary I/O connections. The XACTstep development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC5200-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 4.7 kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

### Configuration Modes

XC5200 devices have seven configuration modes. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode,

**Table 11: Configuration Modes**

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note :\*Peripheral Synchronous can be considered byte-wide Slave Parallel

which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration. The coding for mode selection is shown in [Table 11](#).

Note that the smallest package, VQ64, only supports the Master Serial, Slave Serial, and Express modes. A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in [Table 14 on page 288](#).

### Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configura-

tion data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as 1 MHz (default), 6 MHz, or 12 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +50%.

### **Peripheral Modes**

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

### **Slave Serial Mode**

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

### **Serial Daisy Chain**

Multiple devices with different configurations can be connected together in a “daisy chain,” and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in [Figure 29 on page 278](#). Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. [Figure 26 on page 273](#) shows the start-up timing for an XC5200-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

### **Multi-Family Daisy Chain**

All Xilinx FPGAs of the XC2000, XC3000, XC4000, and XC5200 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. If the chain contains XC5200-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in [Figure 26 on page 273](#). Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of [Figure 26](#). The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC5200-Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

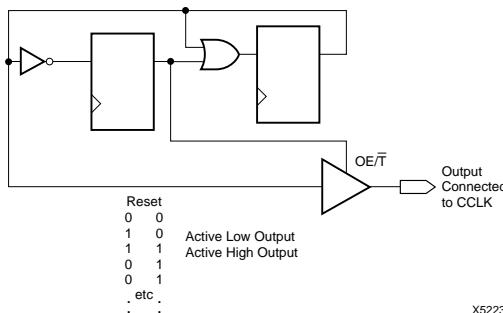
XC5200 devices always have the same number of CCLKs in the power up delay, independent of the configuration mode, unlike the XC3000/XC4000 Series devices. To guarantee all devices in a daisy chain have finished the power-up delay, tie the INIT pins together, as shown in [Figure 28](#).

### **XC3000 Master with an XC5200-Series Slave**

Some designers want to use an XC3000 lead device in peripheral mode and have the I/O pins of the XC5200-Series devices all available for user I/O. [Figure 23](#) provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC5200-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.



**Figure 23: CCLK Generation for XC3000 Master Driving an XC5200-Series Slave**

### Express Mode

Express mode is similar to Slave Serial mode, except the data is presented in parallel format, and is clocked into the target device a byte at a time rather than a bit at a time. The data is loaded in parallel into eight different columns: it is not internally serialized. Eight bits of configuration data are loaded with every CCLK cycle, therefore this configuration mode runs at eight times the data rate of the other six modes. In this mode the XC5200 family is capable of supporting a CCLK frequency of 10 MHz, which is equivalent to an 80 MHz serial rate, because eight bits of configuration data are being loaded per CCLK cycle. An XC5210 in the Express mode, for instance, can be configured in about 2 ms. The Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

In the Express configuration mode, an external signal drives the CCLK input(s). The first byte of parallel configuration data must be available at the D inputs of the FPGA devices a short set-up time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge. See [Figure 39 on page 287](#).

Bitstream generation currently generates a bitstream sufficient to program in all configuration modes except Express. Extra CCLK cycles are necessary to complete the configuration, since in this mode data is read at a rate of eight bits per CCLK cycle instead of one bit per cycle. Normally the entire start-up sequence requires a number of bits that is equal to the number of CCLK cycles needed. An additional five CCLKs (equivalent to 40 extra bits) will guarantee completion of configuration, regardless of the start-up options chosen.

Multiple slave devices with identical configurations can be wired with parallel D0-D7 inputs. In this way, multiple devices can be configured simultaneously.

### Pseudo Daisy Chain

Multiple devices with different configurations can be connected together in a pseudo daisy chain, provided that all of the devices are in Express mode. A single combined bit-stream is used to configure the chain of Express mode devices, but the input data bus must drive D0-D7 of each device. Tie High the CS1 pin of the first device to be configured, or leave it floating in the XC5200 since it has an internal pull-up. Connect the DOUT pin of each FPGA to the CS1 pin of the next device in the chain. The D0-D7 inputs are wired to each device in parallel. The DONE pins are wired together, with one or more internal DONE pull-ups activated. Alternatively, a 4.7 k $\Omega$  external resistor can be used, if desired. (See [Figure 38 on page 286](#).) CCLK pins are tied together.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All devices in Express mode are synchronized to the DONE pin. User I/O for each device become active after the DONE pin for that device goes High. (The exact timing is determined by options to the bitstream generation software.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle.

The status pin DOUT is pulled LOW two internal-oscillator cycles (nominally 1 MHz) after INIT is recognized as High, and remains Low until the device's configuration memory is full. Then DOUT is pulled High to signal the next device in the chain to accept the configuration data on the D7-D0 bus. All devices receive and recognize the six bytes of preamble and length count, irrespective of the level on CS1; but subsequent frame data is accepted only when CS1 is High and the device's configuration memory is not already full.

### Setting CCLK Frequency

For Master modes, CCLK can be generated in one of three frequencies. In the default slow mode, the frequency is nominally 1 MHz. In fast CCLK mode, the frequency is nominally 12 MHz. In medium CCLK mode, the frequency is nominally 6 MHz. The frequency range is -50% to +50%. The frequency is selected by an option when running the bitstream generation software. If an XC5200-Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. Slow mode is the default.

**Table 12: XC5200 Bitstream Format**

Data Type	Value	Occurrences
Fill Byte	11111111	Once per bit-stream
Preamble	11110010	
Length Counter	COUNT(23:0)	
Fill Byte	11111111	
Start Byte	11111110	Once per data frame
Data Frame *	DATA(N-1:0)	
Cyclic Redundancy Check or Constant Field Check	CRC(3:0) or 0110	
Fill Nibble	1111	
Extend Write Cycle	FFFFFF	
Postamble	11111110	Once per device
Fill Bytes (30)	FFFF...FF	
Start-Up Byte	FF	Once per bit-stream

\*Bits per Frame (N) depends on device size, as described for table 11.

## Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes, with the exception of Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode.

The data stream formats are shown in [Table 12](#). Express mode data is shown with D0 at the left and D7 at the right. For all other modes, bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see [Table 13](#)). Each frame begins with a start field and ends with an error check. In all modes except Express mode, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

In Express mode, only non-CRC error checking is supported. In all other modes, a selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the INIT pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect INIT and initialize a new configuration by pulsing the PROGRAM pin Low or cycling Vcc.

**Table 13: Internal Configuration Data Structure**

Device	VersaBlock Array	PROM Size (bits)	Xilinx Serial PROM Needed
XC5202	8 x 8	42,416	XC1765D
XC5204	10 x 12	70,704	XC17128D
XC5206	14 x 14	106,288	XC17128D
XC5210	18 x 18	165,488	XC17256D
XC5215	22 x 22	237,744	XC17256D

Bits per Frame = (34 x number of Rows) + 28 for the top + 28 for the bottom + 4 splitter bits + 8 start bits + 4 error check bits + 4 fill bits \* + 24 extended write bits  
= (34 x number of Rows) + 100

\* In the XC5202 (8 x 8), there are 8 fill bits per frame, not 4  
Number of Frames = (12 x number of Columns) + 7 for the left edge + 8 for the right edge + 1 splitter bit  
= (12 x number of Columns) + 16

Program Data = (Bits per Frame x Number of Frames) + 48 header bits + 8 postamble bits + 240 fill bits + 8 start-up bits  
= (Bits per Frame x Number of Frames) + 304

PROM Size = Program Data

## Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in [Table 12](#). If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in [Figure 24](#). The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not used). Statistically, one error out of 2048 might go undetected.

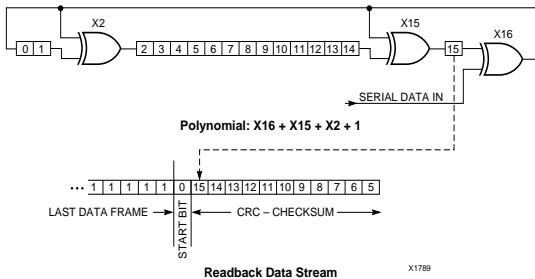


Figure 24: Circuit for Generating CRC-16

## Configuration Sequence

There are four major steps in the XC5200-Series power-up configuration sequence.

- Power-On Time-Out
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 25.

### Power-On Time-Out

An internal power-on reset circuit is triggered when power is applied. When  $V_{CC}$  reaches the voltage at which portions of the FPGA begin to operate (i.e., performs a write-and-read test of a sample pair of configuration memory bits), the programmable I/O buffers are 3-stated with active high-impedance pull-up resistors. A time-out delay — nominally 4 ms — is initiated to allow the power-supply voltage to stabilize. For correct operation the power supply must reach  $V_{CC}(\text{min})$  by the end of the time-out, and must not dip below it thereafter.

There is no distinction between master and slave modes with regard to the time-out delay. Instead, the  $\overline{\text{INIT}}$  line is used to ensure that all daisy-chained devices have completed initialization. Since XC2000 devices do not have this signal, extra care must be taken to guarantee proper operation when daisy-chaining them with XC5200 devices. For proper operation with XC3000 devices, the  $\overline{\text{RESET}}$  signal, which is used in XC3000 to delay configuration, should be connected to  $\overline{\text{INIT}}$ .

If the time-out delay is insufficient, configuration should be delayed by holding the  $\overline{\text{INIT}}$  pin Low until the power supply has reached operating levels.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the  $\overline{\text{PROGRAM}}$  pin Low. During all three phases — Power-on, Initialization, and Configuration —  $\overline{\text{DONE}}$  is held Low;  $\overline{\text{HDC}}$ ,  $\overline{\text{LDC}}$ , and  $\overline{\text{INIT}}$  are active;  $\text{DOUT}$  is driven; and all I/O buffers are disabled.

### Initialization

This phase clears the configuration memory and establishes the configuration mode.

The configuration memory is cleared at the rate of one frame per internal clock cycle (nominally 1 MHz). An open-drain bidirectional signal,  $\overline{\text{INIT}}$ , is released when the configuration memory is completely cleared. The device then tests for the absence of an external active-low level on  $\overline{\text{INIT}}$ . The mode lines are sampled two internal clock cycles later (nominally 2  $\mu\text{s}$ ).

The master device waits an additional 32  $\mu\text{s}$  to 256  $\mu\text{s}$  (nominally 64-128  $\mu\text{s}$ ) to provide adequate time for all of the slave devices to recognize the release of  $\overline{\text{INIT}}$  as well. Then the master device enters the Configuration phase.

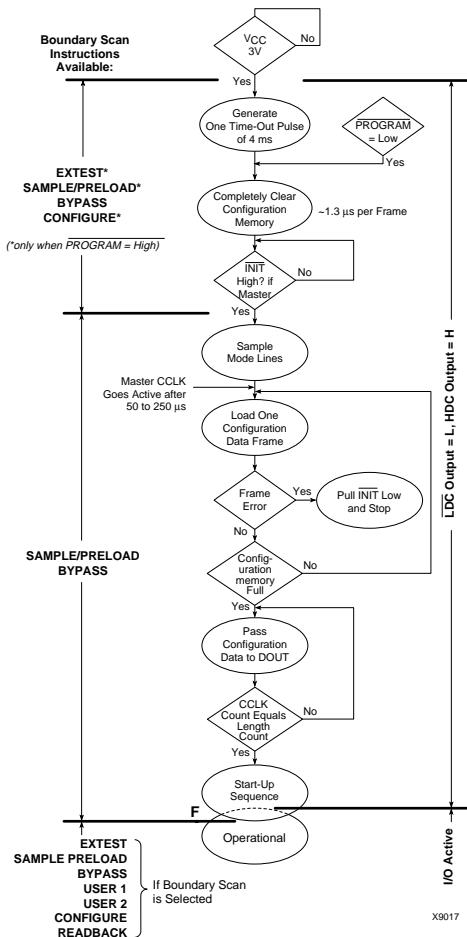
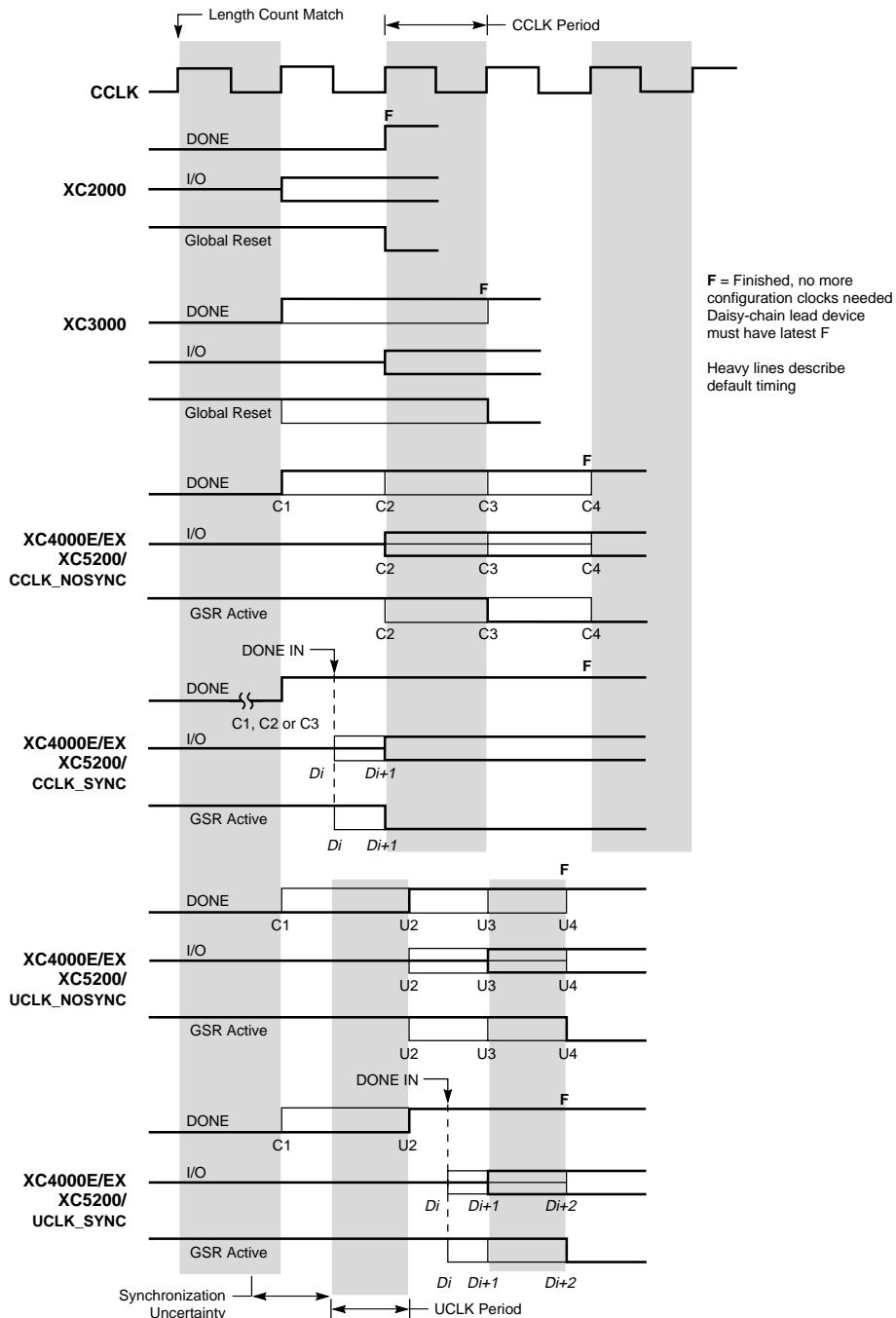


Figure 25: Configuration Sequence



X6700

**Figure 26: Start-up Timing**

## Configuration

The length counter begins counting immediately upon entry into the configuration state. In slave-mode operation it is important to wait at least two cycles of the internal 1-MHz clock oscillator after  $\overline{\text{INIT}}$  is recognized before toggling CCLK and feeding the serial bitstream. Configuration will not begin until the internal configuration logic reset is released, which happens two cycles after  $\overline{\text{INIT}}$  goes High. A master device's configuration is delayed from 32 to 256  $\mu\text{s}$  to ensure proper operation with any slave devices driven by the master device.

The 0010 preamble code, included for all modes except Express mode, indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain  $\overline{\text{INIT}}$  pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device. In Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

### ***Delaying Configuration After Power-Up***

To delay master mode configuration after power-up, pull the bidirectional  $\overline{\text{INIT}}$  pin Low, using an open-collector (open-drain) driver. (See [Figure 13](#).)

Using an open-collector or open-drain driver to hold  $\overline{\text{INIT}}$  Low before the beginning of master mode configuration causes the FPGA to wait after completing the configuration memory clear operation. When  $\overline{\text{INIT}}$  is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250  $\mu\text{s}$  to make sure that any slaves in the optional daisy chain have seen that  $\overline{\text{INIT}}$  is High.

## ***Start-Up***

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset at the right time.

[Figure 26](#) describes start-up timing for the three Xilinx families in detail. Express mode configuration always uses either CCLK\_SYNC or UCLK\_SYNC timing, the other configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

### ***Start-up Timing***

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000/XC5200 Series offers additional flexibility. The three events — DONE going High, the internal Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in [Figure 26](#), but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

XC4000/XC5200 Series offers another start-up clocking option, UCLK\_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK\_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

### Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since INIT went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in **Figure 27**. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDED with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and is selected by either CCLK\_SYNC or UCLK\_SYNC.

When DONE is not used as an input, the operation is called "Start-up Timing Not Synchronous to DONE In," and is selected by either CCLK\_NOSYNC or UCLK\_NOSYNC.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

### Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in **Figure 26** show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

### Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relation-

ship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

### DONE Goes High to Signal End of Configuration

In all configuration modes except Express mode, XC5200-Series devices read the expected length count from the bit-stream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly*.

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [ $2^{24} * \text{CCLK period}$ ] — which is sometimes interpreted as the device not configuring at all.

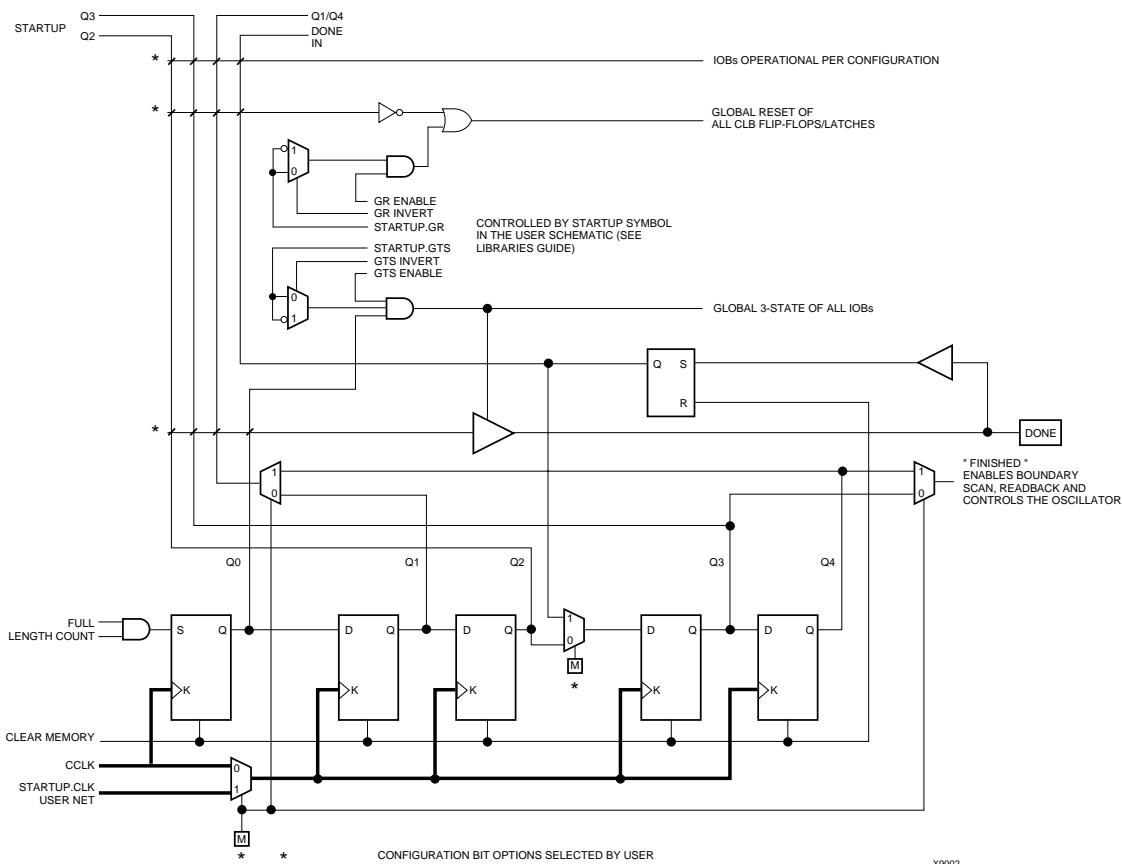
If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

### Release of User I/O After DONE Goes High

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a  $20\text{ k}\Omega - 100\text{ k}\Omega$  pull-up. The delay from DONE High to active user I/O is controlled by an option to the bitstream generation software.

**Figure 27: Start-up Logic**

### **Release of Global Reset After DONE Goes High**

By default, Global Reset (GR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial reset state. The delay from DONE High to GR inactive is controlled by an option to the bitstream generation software.

### **Configuration Complete After DONE Goes High**

Three full CCLK cycles are required after the DONE pin goes High, as shown in [Figure 26 on page 273](#). If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

### **Configuration Through the Boundary Scan Pins**

XC5200-Series devices can be configured through the boundary scan pins.

For detailed information, refer to the Xilinx application note XAPP017, “*Boundary Scan in XC4000 and XC5200 Devices*”.

### **Readback**

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs.

Note that in XC5200-Series devices, configuration data is *not* inverted with respect to configuration as it is in XC2000 and XC3000 families.

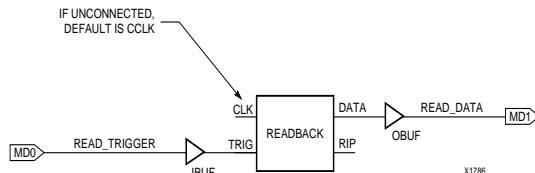
Readback of Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

XC5200-Series Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, place the READBACK library symbol and attach the appropriate pad symbols, as shown in [Figure 28](#).

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.



**Figure 28: Readback Schematic Example**

## Readback Options

Readback options are: Read Capture, Read Abort, and Clock Select. They are set with the bitstream generation software.

### Read Capture

When the Read Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the CLB outputs and the IOB output and input signals. Note that while the bits describing configuration (interconnect and function generators) are *not* inverted, the CLB and IOB output signals *are* inverted.

When the Read Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations.

The readback signals are located in the lower-left corner of the device.

### Read Abort

When the Read Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger.

After an aborted readback, additional clocks (up to one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

### Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If readback must be inhibited for security reasons, the readback control nets are simply not connected.

## Violating the Maximum High and Low Time Specification for the Readback Clock

The readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in [Table 12](#) and [Table 13](#).

### Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the PC or workstation screen, functioning as a low-cost in-circuit emulator.

## Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

### Slave Serial Mode

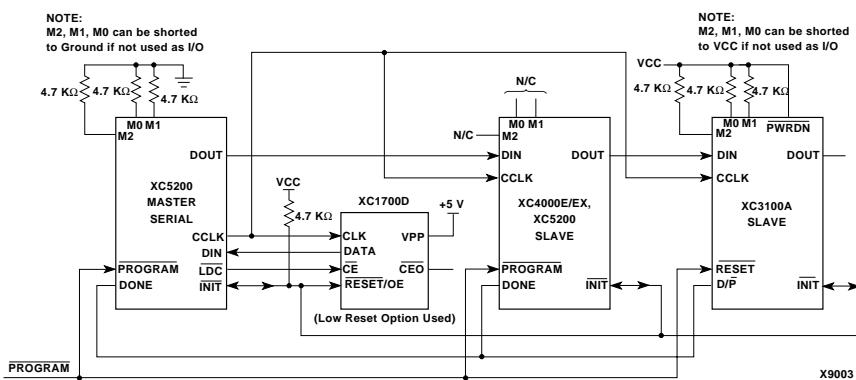
In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

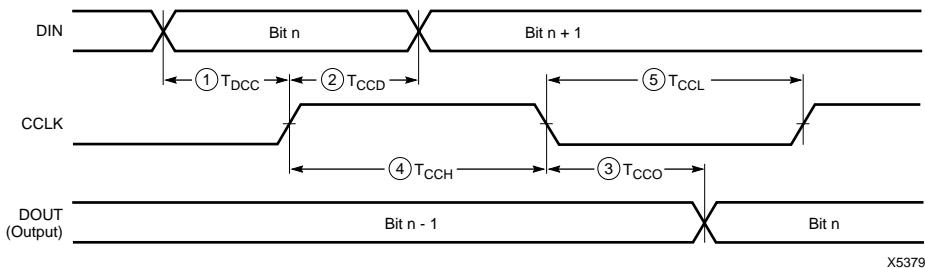
There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 29 shows a full master/slave system. An XC5200-Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.



**Figure 29:** Master/Slave Serial Mode Circuit Diagram



X5379

	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1 $T_{DCC}$	20		ns
	DIN hold	2 $T_{CCD}$	0		ns
	DIN to DOUT	3 $T_{CCO}$		30	ns
	High time	4 $T_{CCH}$	45		ns
	Low time	5 $T_{CCL}$	45		ns
	Frequency	$F_{CC}$		10	MHz

Note: Configuration must be delayed until the INIT pins of all daisy-chained FPGAs are High.

**Figure 30:** Slave Serial Mode Programming Switching Characteristics

## Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

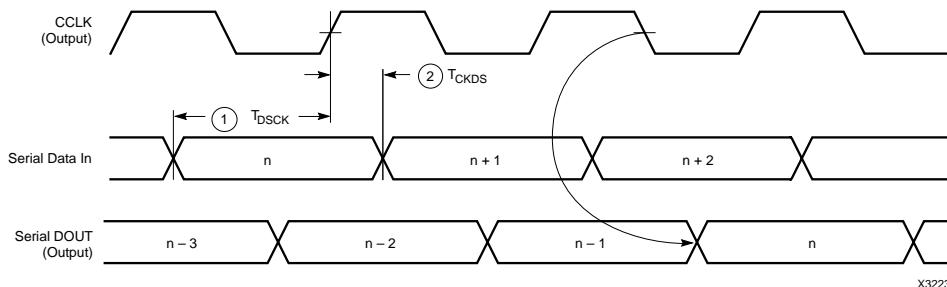
In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of twelve.

The value increases from a nominal 1 MHz, to a nominal 12 MHz. Be sure that the serial PROM and slaves are fast enough to support this data rate. The Medium ConfigRate option changes the frequency to a nominal 6 MHz. XC2000, XC3000/A, and XC3100A devices do not support the Fast or Medium ConfigRate options.

The SPROM CE input can be driven from either  $\overline{\text{LDC}}$  or DONE. Using LDC avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but  $\overline{\text{LDC}}$  is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

[Figure 29 on page 278](#) shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



	Description	Symbol	Min	Max	Units
CCLK	DIN setup	1	$T_{DSCK}$	20	ns
	DIN hold	2	$T_{CKDS}$	0	ns

Notes:

1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until Vcc is valid.
2. Master Serial mode timing is based on testing in slave mode.

**Figure 31: Master Serial Mode Programming Switching Characteristics**

## Master Parallel Modes

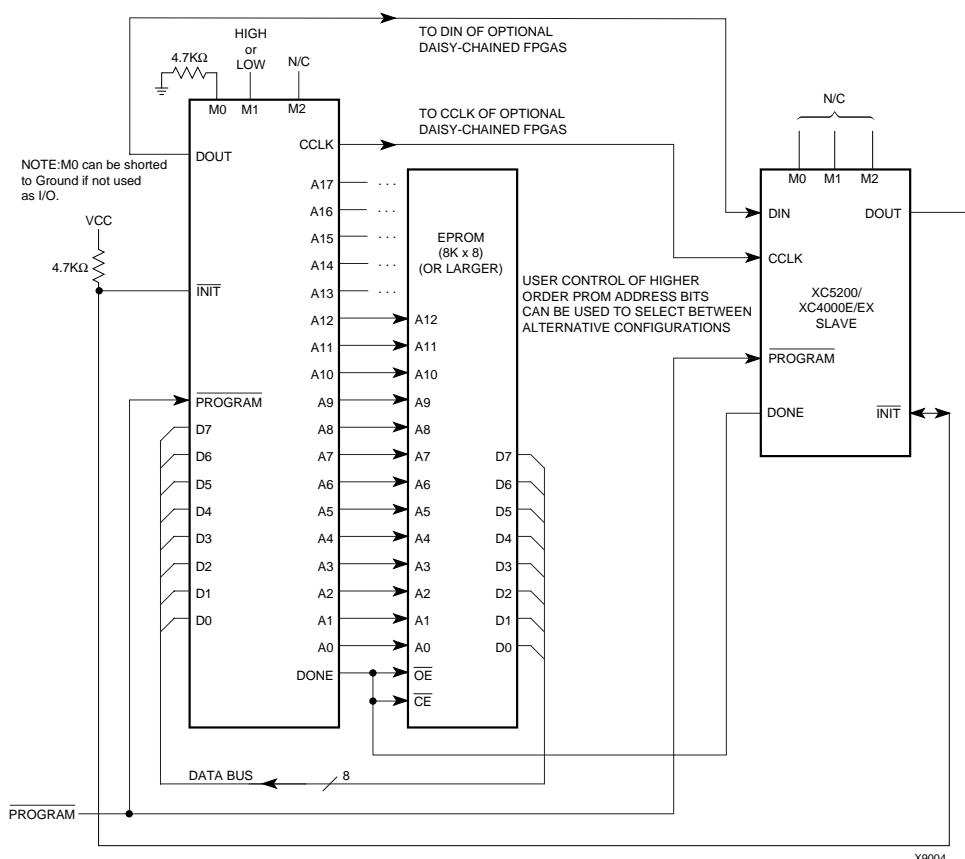
In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

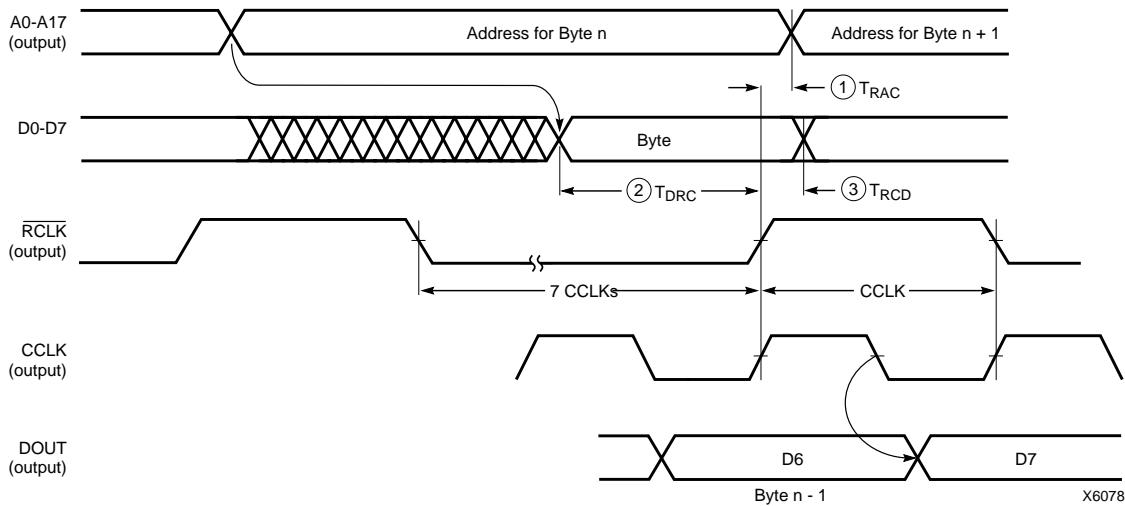
The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at FFFF and decrement.



**Figure 32:** Master Parallel Mode Circuit Diagram



	Description	Symbol	Min	Max	Units
CCLK	Delay to Address valid	1 $T_{RAC}$	0	200	ns
	Data setup time	2 $T_{DRC}$	60		ns
	Data hold time	3 $T_{RCD}$	0		ns

Note: 1. At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms, otherwise delay configuration by pulling  $\overline{\text{PROGRAM}}$  Low until  $V_{CC}$  is Valid.

2. The first Data byte is loaded and CCLK starts at the end of the first  $\overline{\text{RCLK}}$  active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

**Figure 33: Master Parallel Mode Programming Switching Characteristics**

## Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/BUSY output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal

for test purposes. Note that RDY/BUSY is pulled High with a high-impedance pullup prior to INIT going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

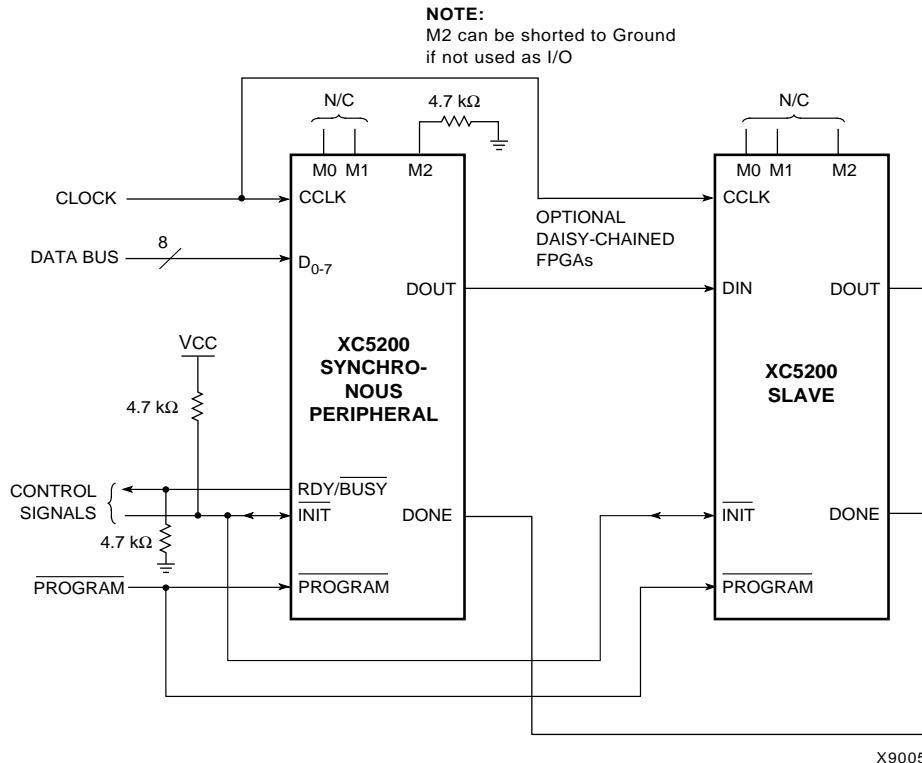
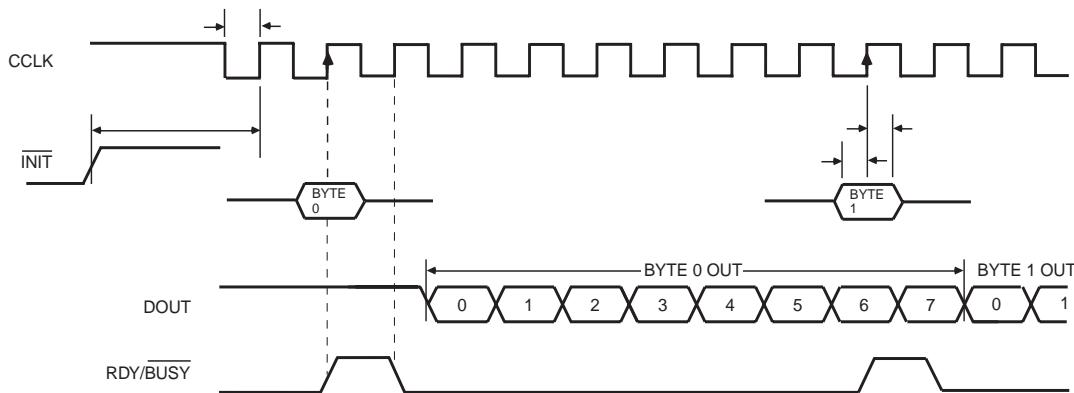


Figure 34: Synchronous Peripheral Mode Circuit Diagram



X6096

	Description	Symbol	Min	Max	Units
CCLK	INIT (High) setup time	1	$T_{IC}$		$\mu s$
	D0 - D7 setup time	2	$T_{DC}$		ns
	D0 - D7 hold time	3	$T_{CD}$		ns
	CCLK High time		$T_{CCH}$		ns
	CCLK Low time		$T_{CCL}$		ns
	CCLK Frequency		$F_{CC}$	8	MHz

- Notes:
- Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes high. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
  - The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
  - The pin name RDY/BUSY is a misnomer. In synchronous peripheral mode this is really an ACKNOWLEDGE signal.
  - Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 35: Synchronous Peripheral Mode Programming Switching Characteristics

## Asynchronous Peripheral Mode

### Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of  $\overline{WS}$  and  $\overline{CS0}$  being Low and  $\overline{RS}$  and  $CS1$  being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/BUSY output from the lead FPGA acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/BUSY output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/BUSY is High again for one CCLK period. Note that RDY/BUSY is pulled High with a high-impedance pull-up prior to INIT going High.

The length of the BUSY signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the BUSY signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the BUSY signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.

The READY/BUSY handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

### Status Read

The logic AND condition of the  $\overline{CS0}$ , CS1 and  $\overline{RS}$  inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in [Figure 26 on page 273](#)).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by the XACTstep software, ensures that these problems never occur.

Although RDY/BUSY is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/BUSY status when RS is Low, WS is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).

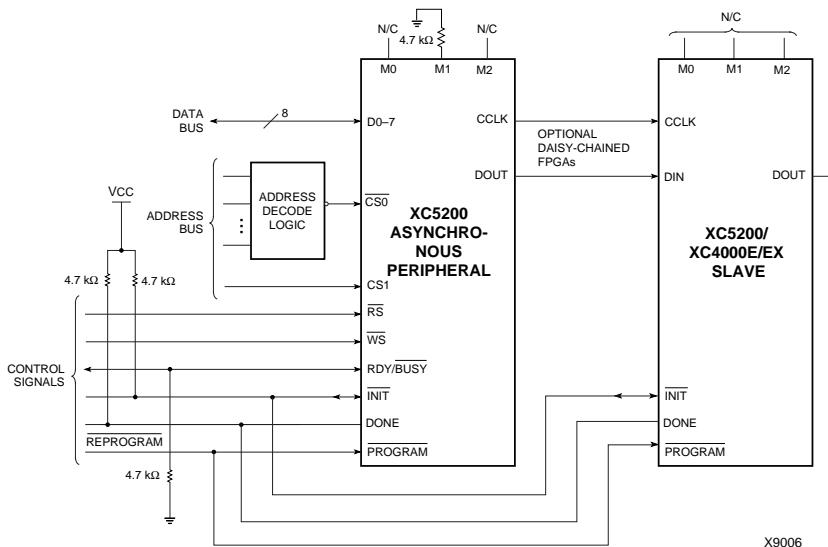
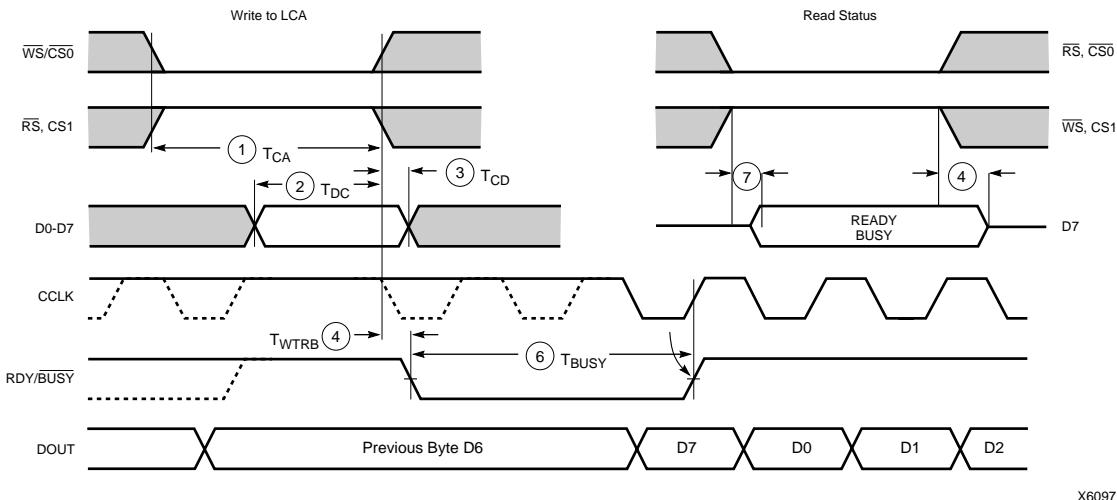


Figure 36: Asynchronous Peripheral Mode Circuit Diagram



X6097

	Description	Symbol	Min	Max	Units
Write	Effective Write time (CS0, WS=Low; RS, CS1=High)	1 T <sub>CA</sub>	100		ns
	DIN setup time	2 T <sub>DC</sub>	60		ns
	DIN hold time	3 T <sub>CD</sub>	0		ns
RDY	RDY/BUSY delay after end of Write or Read	4 T <sub>WTRB</sub>		60	ns
	RDY/BUSY active after beginning of Read	7		60	ns
	RDY/BUSY Low output (Note 4)	6 T <sub>BUSY</sub>	2	9	CCLK periods

- Notes:
- Configuration must be delayed until INIT pins of all daisy-chained FPGAs are high.
  - The time from the end of WS to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of internal timing generator for CCLK.
  - CCLK and DOUT timing is tested in slave mode.
  - T<sub>BUSY</sub> indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T<sub>BUSY</sub> occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T<sub>BUSY</sub> occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of WS. RDY/BUSY will go active within 60 ns after the end of WS. A new write may be asserted immediately after RDY/BUSY goes Low, but write may not be terminated until RDY/BUSY has been High for one CCLK period.

**Figure 37: Asynchronous Peripheral Mode Programming Switching Characteristics**

## Express Mode

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers. A CCLK frequency of 10 MHz is equivalent to an 80 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking.

In Express mode, an external signal drives the CCLK input of the FPGA device. The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge.

Express mode is only supported by the XC4000EX and XC5200 families. It may not be used, therefore, when an XC4000EX or XC5200 device is daisy-chained with devices from other Xilinx families.

If the first device is configured in Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in Express mode. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). Frame data is accepted only when CS1 is High and the device's configu-

ration memory is not already full. The status pin DOUT is pulled Low two internal-oscillator cycles after INIT is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using an option in the bitstream generation software.

XC5200 devices in Express mode are always synchronized to DONE. The device becomes active after DONE goes High. DONE is an open-drain output. With the DONE pins tied together, therefore, the external DONE signal stays low until all devices are configured, then all devices in the daisy chain become active simultaneously. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. XC4000EX devices in the chain should be configured as synchronized to DONE (either CCLK\_SYNC or UCLK\_SYNC), and their DONE pins wired together with those of the XC5200 devices.

Express mode is selected by a <010> on the mode pins (M2, M1, M0).

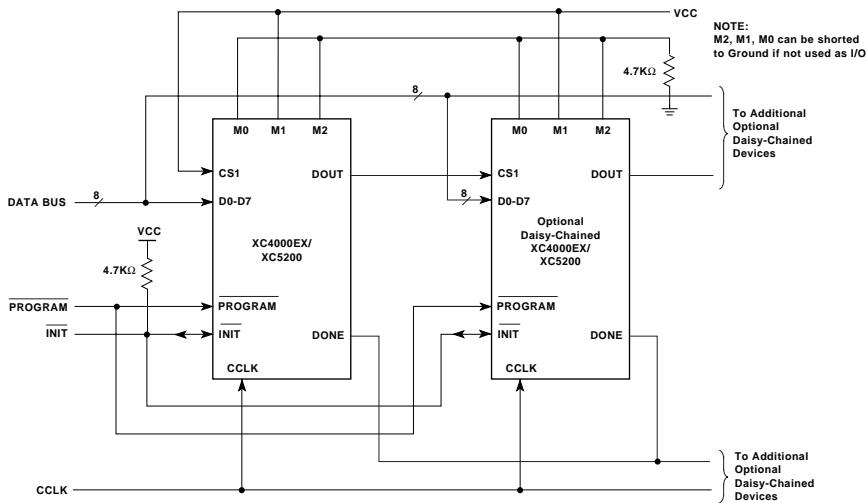
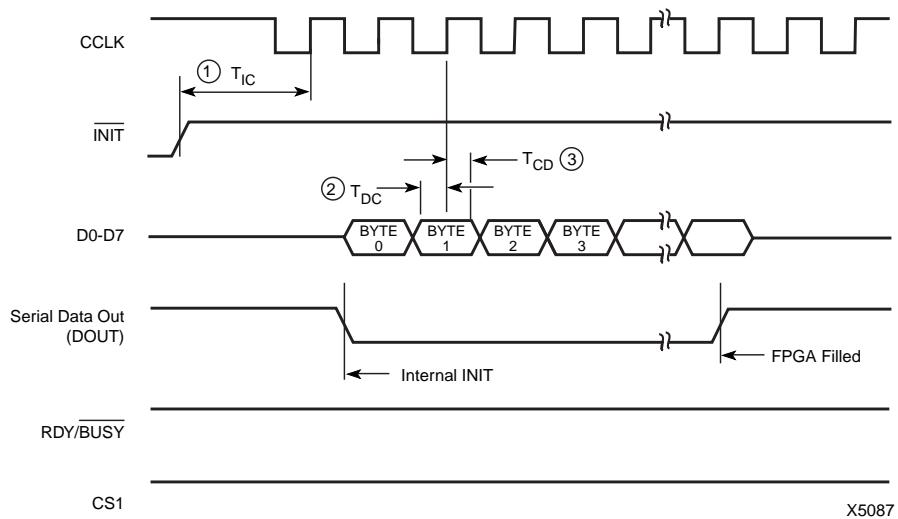


Figure 38: Express Mode Circuit Diagram



X5087

	Description	Symbol	Min	Max	Units
CCLK	INIT (High) Setup time required	1	$T_{IC}$	5	$\mu s$
	DIN Setup time required	2	$T_{DC}$	30	ns
	DIN hold time required	3	$T_{CD}$	0	ns
	CCLK High time		$T_{CCH}$	30	ns
	CCLK Low time		$T_{CCL}$	30	ns
	CCLK frequency		$F_{CC}$	10	MHz

Note: If not driven by the preceding DOUT, CS1 must remain high until the device is fully configured.

**Figure 39: Express Mode Programming Switching Characteristics**

**Table 14. Pin Functions During Configuration**

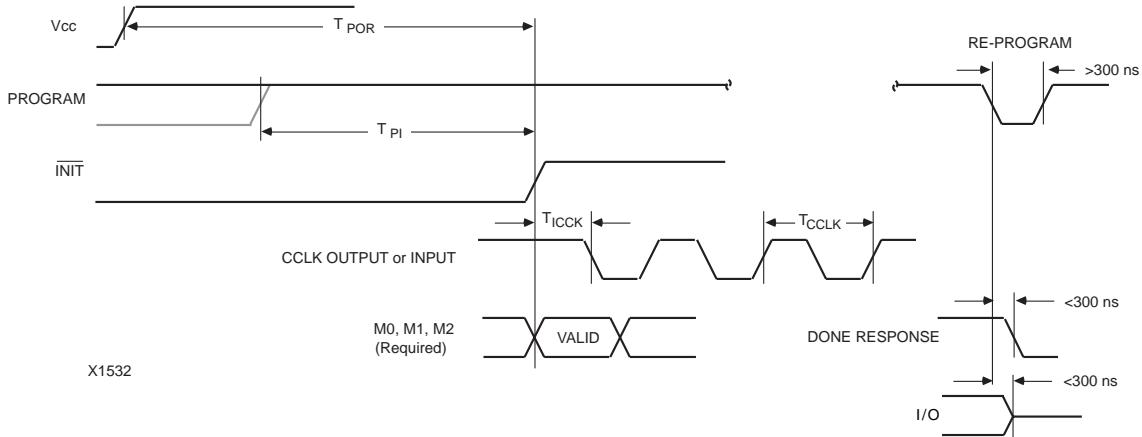
CONFIGURATION MODE: <M2:M1:M0>							USER OPERATION
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	EXPRESS <0:1:0>	
				A16	A16		GCK1-I/O
				A17	A17		I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
							I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	I/O
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	M0 (LOW) (I)	I/O
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	I/O
							GCK2-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	I/O
							I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
							GCK3-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			CSO (I)				I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			RS (I)				I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
			RDY/BUSY	RDY/BUSY	RCLK	RCLK	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	I/O
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-I/O
			WS (I)	A0	A0		I/O
				A1	A1		GCK4-I/O
			CS1 (I)	A2	A2	CS1 (I)	I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		I/O
							ALL OTHERS

Notes 1. A shaded table cell represents a 20-kΩ to 100-kΩ pull-up resistor before and during configuration.

2. (I) represents an input (O) represents an output.

3. INIT is an open-drain output during configuration.

## Configuration Switching Characteristics



## Master Modes

Description	Symbol	Min	Max	Units
Power-On-Reset	$T_{POR}$	2	15	ms
Program Latency	$T_{PI}$	6	70	$\mu\text{s}$ per CLB column
CCLK (output) Delay	$T_{ICCK}$	40	375	$\mu\text{s}$
period (slow)	$T_{CCLK}$	640	3000	ns
period (fast)	$T_{CCLK}$	100	375	ns

## Slave and Peripheral Modes

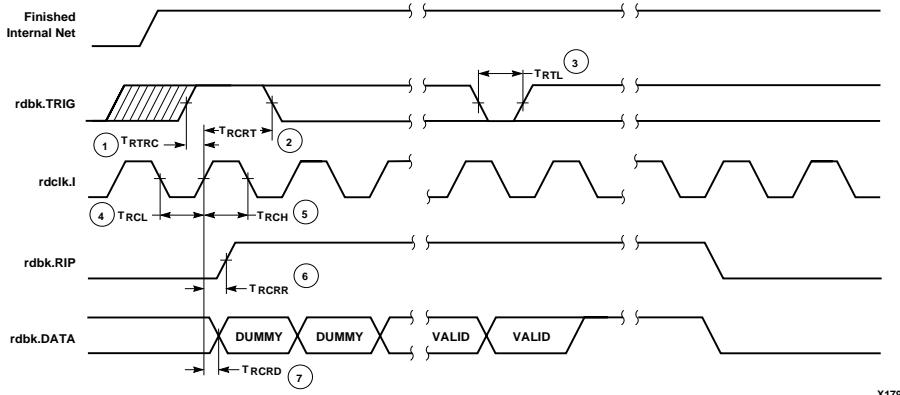
Description	Symbol	Min	Max	Units
Power-On-Reset	$T_{POR}$	2	15	ms
Program Latency	$T_{PI}$	6	70	$\mu\text{s}$ per CLB column
CCLK (input) Delay (required)	$T_{ICCK}$	5		$\mu\text{s}$
period (required)	$T_{CCLK}$	100		ns

**Note:** At power-up,  $V_{CC}$  must rise from 2.0 to  $V_{CC}$  min in less than 15 ms, otherwise delay configuration using PROGRAM until  $V_{CC}$  is valid.

## XC5200 Program Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.



X1790

	Description		Symbol	Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback rdbk.TRIG hold to initiate and abort Readback	1 2	$T_{RTRC}$ $T_{RCRT}$	200 50	- -	ns ns
rdclk.1	rdbk.DATA delay rdbk.RIP delay High time Low time	7 6 5 4	$T_{RCRD}$ $T_{RCRR}$ $T_{RCH}$ $T_{RCL}$	- - 250 250	250 250 500 500	ns ns ns ns

Note 1: Timing parameters apply to all speed grades.

Note 2: rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback

## XC5200 Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.<sup>1</sup>

### XC5200 Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial:0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial:-40°C to 100°C junction	4.5	5.5	V
$V_{IHT}$	High-level input voltage — TTL configuration	2.0	$V_{CC}$	V
$V_{ILT}$	Low-level input voltage — TTL configuration	0	0.8	V
$V_{IHC}$	High-level input voltage — CMOS configuration	70%	100%	$V_{CC}$
$V_{ILC}$	Low-level input voltage — CMOS configuration	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns

### XC5200 DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -8.0$ mA, $V_{CC}$ min	3.86		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 8.0$ mA, $V_{CC}$ max		0.4	V
$I_{CC0}$	Quiescent FPGA supply current (Note 1)		15	mA
$I_{IL}$	Leakage current	-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)		15	pF
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0V$ (sample tested)	0.02	0.30	mA

Note: 1. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a tie option.

### XC5200 Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

## XC5200 Global Buffer Switching Characteristic Guidelines

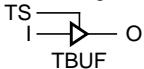
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACTstep timing calculator and used in the simulator.

Speed Grade			-6	-5	-4	-3
Description	Symbol	Device	Max (ns)	Max (ns)	Max (ns)	Max (ns)
<b>Global Signal Distribution</b> From pad through global buffer, to any clock (CK)	T <sub>BUFG</sub>	XC5202	9.1	8.5	8.0	6.9
		XC5204	9.3	8.7	8.2	7.6
		XC5206	9.4	8.8	8.3	7.7
		XC5210	9.4	8.8	8.5	7.7
		XC5215	10.5	9.9	9.8	9.6

PRELIMINARY

## XC5200 Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACTstep timing calculator and used in the simulator.

Speed Grade			-6	-5	-4	-3
Description	Symbol	Device	Max (ns)	Max (ns)	Max (ns)	Max (ns)
TBUF driving a Longline  I to Longline, while TS is Low; i.e., buffer is constantly active	T <sub>IO</sub>	XC5202	6.0	3.8	3.0	2.0
		XC5204	6.4	4.1	3.2	2.3
		XC5206	6.6	4.2	3.3	2.7
		XC5210	6.6	4.2	3.3	2.9
		XC5215	7.3	4.6	3.8	3.2
TS going Low to Longline going from floating High or Low to active Low or High	T <sub>ON</sub>	XC5202	7.8	5.6	4.7	4.0
		XC5204	8.3	5.9	4.9	4.3
		XC5206	8.4	6.0	5.0	4.4
		XC5210	8.4	6.0	5.0	4.4
		XC5215	8.9	6.3	5.3	4.5
TS going High to TBUF going inactive, not driving Longline	T <sub>OFF</sub>	XC52xx	3.0	2.8	2.6	2.4

PRELIMINARY

**Note:** 1. Die-size-dependent parameters are based upon XC5215 characterization. Production specifications will vary with array size.

## XC5200 CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACTstep timing calculator and used in the simulator.

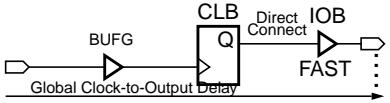
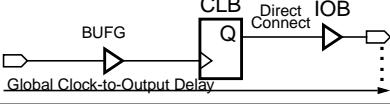
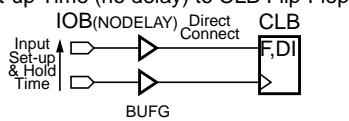
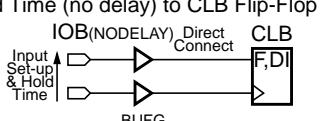
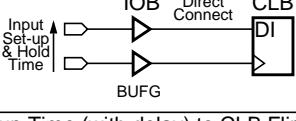
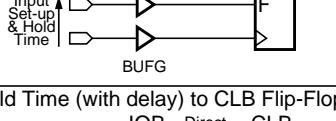
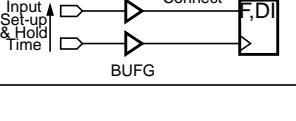
Speed Grade		-6		-5		-4		-3	
Description	Symbol	Min (ns)	Max (ns)						
Combinatorial Delays									
F inputs to X output	$T_{ILO}$		5.6		4.6		3.8		3.0
F inputs via transparent latch to Q	$T_{ITO}$		8.0		6.6		5.4		4.3
DI inputs to DO output (Logic-Cell Feedthrough)	$T_{IDO}$		4.3		3.5		2.8		2.4
F inputs via F5_MUX to DO output	$T_{IMO}$		7.2		5.8		5.0		4.3
Carry Delays									
Incremental delay per bit	$T_{CY}$		0.7		0.6		0.5		0.5
Carry-in overhead from DI	$T_{CYDI}$		1.8		1.6		1.5		1.4
Carry-in overhead from F	$T_{CYL}$		3.7		3.2		2.9		2.4
Carry-out overhead to DO	$T_{CYO}$		4.0		3.2		2.5		2.1
Sequential Delays									
Clock (CK) to out (Q) (Flip-Flop)	$T_{CKO}$		5.8		4.9		4.0		4.0
Gate (Latch enable) going active to out (Q)	$T_{GO}$		9.2		7.4		5.9		5.5
Set-up Time Before Clock (CK)									
F inputs	$T_{ICK}$	2.3		1.8		1.4		1.3	
F inputs via F5_MUX	$T_{MICK}$	3.8		3.0		2.5		2.4	
DI input	$T_{DICK}$	0.8		0.5		0.4		0.4	
CE input	$T_{EICK}$	1.6		1.2		0.9		0.9	
Hold Times After Clock (CK)									
F inputs	$T_{CKI}$	0		0		0		0	
F inputs via F5_MUX	$T_{CKMI}$	0		0		0		0	
DI input	$T_{CKDI}$	0		0		0		0	
CE input	$T_{CKEI}$	0		0		0		0	
Clock Widths									
Clock High Time	$T_{CH}$	6.0		6.0		6.0		6.0	
Clock Low Time	$T_{CL}$	6.0		6.0		6.0		6.0	
Toggle Frequency (MHz) (Note 3)	$F_{TOG}$		83		83		83		83
Reset Delays									
Width (High)	$T_{CLRW}$	6.0		6.0		6.0		6.0	
Delay from CLR to Q (Flip-Flop)	$T_{CLR}$		7.7		6.3		5.1		4.0
Delay from CLR to Q (Latch)	$T_{CLRL}$		6.5		5.2		4.2		3.0
Global Reset Delays									
Width (High)	$T_{GCLRW}$	6.0		6.0		6.0		6.0	
Delay from internal GR to Q	$T_{GCLR}$		14.7		12.1		9.1		8.0

PRELIMINARY

- Note:**
1. The CLB K to Q output delay ( $T_{CKO}$ ) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold-time requirement ( $T_{CKDI}$ ) of any CLB on the same die.
  2. Timing is based upon the XC5215 device. For other devices, see XACTstep Timing Calculator.
  3. Maximum flip-flop toggle rate for export control purposes.

## XC5200 Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the Global Buffer specifications. The XACTstep delay calculator uses this indirect method, and may overestimate because of worst-case assumptions. When there is a discrepancy between these two methods, the values listed below should be used, and the derived values should be considered conservative overestimates.

			Speed Grade	-6	-5	-4	-3
Description	Symbol	Device	Max (ns)	Max (ns)	Max (ns)	Max (ns)	
Global Clock to Output Pad (fast)	$T_{ICKOF}$ (Max)	XC5202	16.9	15.1	10.9	9.8	
		XC5204	17.1	15.3	11.3	9.9	
		XC5206	17.2	15.4	11.9	10.8	
		XC5210	17.2	15.4	12.8	11.2	
		XC5215	19.0	17.0	12.8	11.7	
Global Clock to Output Pad (slew-limited)	$T_{ICKO}$ (Max)	XC5202	21.4	18.7	12.6	11.5	
		XC5204	21.6	18.9	13.3	11.9	
		XC5206	21.7	19.0	13.6	12.5	
		XC5210	21.7	19.0	15.0	12.9	
		XC5215	24.3	21.2	15.0	13.1	
Input Set-up Time (no delay) to CLB Flip-Flop	$T_{PSUF}$ (Min)	XC5202	2.5	2.0	1.9	1.9	
		XC5204	2.3	1.9	1.9	1.9	
		XC5206	2.2	1.9	1.9	1.9	
		XC5210	2.2	1.9	1.9	1.8	
		XC5215	2.0	1.8	1.7	1.7	
Input Hold Time (no delay) to CLB Flip-Flop	$T_{PHF}$ (Min)	XC5202	3.8	3.8	3.5	3.5	
		XC5204	3.9	3.9	3.8	3.6	
		XC5206	4.4	4.4	4.4	4.3	
		XC5210	5.1	5.1	4.9	4.8	
		XC5215	5.8	5.8	5.7	5.6	
Input Set-up Time (with delay) to CLB Flip-Flop DI Input	$T_{PSU}$	XC5202	7.3	6.6	6.6	6.6	
		XC5204	7.3	6.6	6.6	6.6	
		XC5206	7.2	6.5	6.4	6.3	
		XC5210	7.2	6.5	6.0	6.0	
		XC5215	6.8	5.7	5.7	5.7	
Input Set-up Time (with delay) to CLB Flip-Flop F Input	$T_{PSUL}$ (Min)	XC5202	8.8	7.7	7.5	7.5	
		XC5204	8.6	7.5	7.5	7.5	
		XC5206	8.5	7.4	7.4	7.4	
		XC5210	8.5	7.4	7.4	7.3	
		XC5215	8.5	7.4	7.4	7.2	
Input Hold Time (with delay) to CLB Flip-Flop	$T_{PH}$ (Min)	XC52xx	0	0	0	0	
							

PRELIMINARY

- Note:**
- These measurements assume that the CLB flip-flop uses a direct interconnect to or from the IOB. The XACTstep M1 INREG/OUTREG properties, or XACT-Performance, can be used to assure that direct connects are used.  $t_{PSU}$  applies only to the CLB input DI that bypasses the look-up table, which only offers direct connects to IOBs on the left and right edges of the die.  $t_{PSUL}$  applies to the CLB inputs F that feed the look-up table, which offers direct connect to IOBs on all four edges, as do the CLB Q outputs.
  - When testing outputs (fast or slew-limited), half of the outputs on one side of the device are switching.

## XC5200 IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACTstep timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	-3
Description	Symbol	Max (ns)	Max (ns)	Max (ns)	Max (ns)	
<b>Input</b>						
Propagation Delays from CMOS or TTL Levels						
Pad to I (no delay)	$T_{PI}$	5.7	5.0	4.8	3.3	
Pad to I (with delay)	$T_{PID}$	11.4	10.2	10.2	9.5	
<b>Output</b>						
Propagation Delays to CMOS or TTL Levels						
Output (O) to Pad (fast)	$T_{OPF}$	4.6	4.5	4.5	3.5	
Output (O) to Pad (slew-limited)	$T_{OPS}$	9.5	8.4	8.0	5.0	
From clock (CK) to output pad (fast), using direct connect between Q and output (O)	$T_{OKPOF}$	10.1	9.3	8.3	7.5	
From clock (CK) to output pad (slew-limited), using direct connect between Q and output (O)	$T_{OKPOS}$	14.9	13.1	11.8	10.0	
3-state to Pad active (fast)	$T_{TSONF}$	5.6	5.2	4.9	4.6	
3-state to Pad active (slew-limited)	$T_{TSONS}$	10.4	9.0	8.3	6.0	
Internal GTS to Pad active	$T_{GTS}$	17.7	15.9	14.7	13.5	
						PRELIMINARY

- Note:**
1. Timing is measured at pin threshold, with 50-pF external capacitance loads. **Slew-limited** output rise/fall times are approximately two times longer than **fast** output rise/fall times.
  2. Unused and unbonded IOBs are configured by default as inputs with internal pull-up resistors.
  3. Timing is based upon the XC5215 device. For other devices, see XACTstep Timing Calculator.

## XC5200 Boundary Scan (JTAG) Switching Characteristic Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC5200 devices unless otherwise noted.

Speed Grade		-6		-5		-4		-3	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
<b>Setup and Hold</b>									
Input (TDI) to clock (TCK) setup time	$T_{TDITCK}$	30.0		30.0		30.0		30.0	
Input (TDI) to clock (TCK) hold time	$T_{TCKTDI}$	0		0		0		0	
Input (TMS) to clock (TCK) setup time	$T_{TMSTCK}$	15.0		15.0		15.0		15.0	
Input (TMS) to clock (TCK) hold time	$T_{TCKTMS}$	0		0		0		0	
<b>Propagation Delay</b>									
Clock (TCK) to Pad (TDO)	$T_{TCKPO}$		30.0		30.0		30.0		30.0
<b>Clock</b>									
Clock (TCK) High	$T_{TCKH}$	30.0		30.0		30.0		30.0	
Clock (TCK) Low	$T_{TCKL}$	30.0		30.0		30.0		30.0	
$F_{MAX}$ (MHz)	$F_{MAX}$		10.0		10.0		10.0		10.0
ADVANCE									

Note 1: Input pad setup and hold times are specified with respect to the internal clock.

## Device-Specific Pinout Tables

Device-specific tables include all packages for each XC5200-Series device. They follow the pad locations around the die, and include boundary scan register locations.

### Pin Locations for XC5202 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

<b>Pin</b>	<b>Description</b>	<b>VQ64*</b>	<b>PC84</b>	<b>PQ100</b>	<b>VQ100</b>	<b>TQ144</b>	<b>PG156</b>	<b>Boundary Scan Order</b>
	VCC	-	2	92	89	128	H3	-
1.	I/O (A8)	57	3	93	90	129	H1	51
2.	I/O (A9)	58	4	94	91	130	G1	54
3.	I/O	-	-	95	92	131	G2	57
4.	I/O	-	-	96	93	132	G3	63
5.	I/O (A10)	-	5	97	94	133	F1	66
6.	I/O (A11)	59	6	98	95	134	F2	69
	GND	-	-	-	-	137	F3	-
7.	I/O (A12)	60	7	99	96	138	E3	78
8.	I/O (A13)	61	8	100	97	139	C1	81
9.	I/O (A14)	62	9	1	98	142	B1	90
10.	I/O (A15)	63	10	2	99	143	B2	93
	VCC	64	11	3	100	144	C3	-
	GND	-	12	4	1	1	C4	-
11.	GCK1 (A16, I/O)	1	13	5	2	2	B3	102
12.	I/O (A17)	2	14	6	3	3	A1	105
13.	I/O (TDI)	3	15	7	4	6	B4	111
14.	I/O (TCK)	4	16	8	5	7	A3	114
	GND	-	-	-	-	8	C6	-
15.	I/O (TMS)	5	17	9	6	11	A5	117
16.	I/O	6	18	10	7	12	C7	123
17.	I/O	-	-	-	-	13	B7	126
18.	I/O	-	-	11	8	14	A6	129
19.	I/O	-	19	12	9	15	A7	135
20.	I/O	7	20	13	10	16	A8	138
	GND	8	21	14	11	17	C8	-
	VCC	9	22	15	12	18	B8	-
21.	I/O	-	23	16	13	19	C9	141
22.	I/O	10	24	17	14	20	B9	147
23.	I/O	-	-	18	15	21	A9	150
24.	I/O	-	-	-	-	22	B10	153
25.	I/O	-	25	19	16	23	C10	159
26.	I/O	11	26	20	17	24	A10	162
	GND	-	-	-	-	27	C11	-
27.	I/O	12	27	21	18	28	B12	165
28.	I/O	-	-	22	19	29	A13	171
29.	I/O	13	28	23	20	32	B13	174
30.	I/O	14	29	24	21	33	B14	177
31.	M1 (I/O)	15	30	25	22	34	A15	186
	GND	-	31	26	23	35	C13	-
32.	M0 (I/O)	16	32	27	24	36	A16	189
	VCC	-	33	28	25	37	C14	-
33.	M2 (I/O)	17	34	29	26	38	B15	192
34.	GCK2 (I/O)	18	35	30	27	39	B16	195

<b>Pin</b>	<b>Description</b>	<b>VQ64*</b>	<b>PC84</b>	<b>PQ100</b>	<b>VQ100</b>	<b>TQ144</b>	<b>PG156</b>	<b>Boundary Scan Order</b>
35.	I/O (HDC)	19	36	31	28	40	D14	204
36.	I/O	-	-	32	29	43	E14	207
37.	I/O (LDC)	20	37	33	30	44	C16	210
	GND	-	-	-	-	45	F14	-
38.	I/O	-	38	34	31	48	F16	216
39.	I/O	21	39	35	32	49	G14	219
40.	I/O	-	-	36	33	50	G15	222
41.	I/O	-	-	37	34	51	G16	228
42.	I/O	22	40	38	35	52	H16	231
43.	I/O (ERR, INIT)	23	41	39	36	53	H15	234
	VCC	24	42	40	37	54	H14	-
	GND	25	43	41	38	55	J14	-
44.	I/O	26	44	42	39	56	J15	240
45.	I/O	27	45	43	40	57	J16	243
46.	I/O	-	-	44	41	58	K16	246
47.	I/O	-	-	45	42	59	K15	252
48.	I/O	28	46	46	43	60	K14	255
49.	I/O	29	47	47	44	61	L16	258
	GND	-	-	-	-	64	L14	-
50.	I/O	-	48	48	45	65	P16	264
51.	I/O	30	49	49	46	66	M14	267
52.	I/O	-	50	50	47	69	N14	276
53.	I/O	31	51	51	48	70	R16	279
	GND	-	52	52	49	71	P14	-
	DONE	32	53	53	50	72	R15	-
	VCC	33	54	54	51	73	P13	-
	PROG	34	55	55	52	74	R14	-
54.	I/O (D7)	35	56	56	53	75	T16	288
55.	GCK3 (I/O)	36	57	57	54	76	T15	291
56.	I/O (D6)	37	58	58	55	79	T14	300
57.	I/O	-	-	59	56	80	T13	303
	GND	-	-	-	-	81	P11	-
58.	I/O (D5)	38	59	60	57	84	T10	306
59.	I/O (CS0)	-	60	61	58	85	P10	312
60.	I/O	-	-	62	59	86	R10	315
61.	I/O	-	-	63	60	87	T9	318
62.	I/O (D4)	39	61	64	61	88	R9	324
63.	I/O	-	62	65	62	89	P9	327
	VCC	40	63	66	63	90	R8	-
	GND	41	64	67	64	91	P8	-
64.	I/O (D3)	42	65	68	65	92	T8	336
65.	I/O (RS)	43	66	69	66	93	T7	339
66.	I/O	-	-	70	67	94	T6	342
67.	I/O	-	-	-	-	95	R7	348
68.	I/O (D2)	44	67	71	68	96	P7	351
69.	I/O	-	68	72	69	97	T5	360
	GND	-	-	-	-	100	P6	-
70.	I/O (D1)	45	69	73	70	101	T3	363
71.	I/O (RCLK-BUSY/RDY)	-	70	74	71	102	P5	366
72.	I/O (D0, DIN)	46	71	75	72	105	P4	372
73.	I/O (DOUT)	47	72	76	73	106	T2	375

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	CCLK	48	73	77	74	107	R2	-
	VCC	-	74	78	75	108	P3	-
74.	I/O (TDO)	49	75	79	76	109	T1	0
	GND	-	76	80	77	110	N3	-
75.	I/O (A0, $\overline{WS}$ )	50	77	81	78	111	R1	9
76.	GCK4 (A1, I/O)	51	78	82	79	112	P2	15
77.	I/O (A2, CS1)	52	79	83	80	115	P1	18
78.	I/O (A3)	-	80	84	81	116	N1	21
	GND	-	-	-	-	118	L3	-
79.	I/O (A4)	-	81	85	82	121	K3	27
80.	I/O (A5)	53	82	86	83	122	K2	30
81.	I/O	-	-	87	84	123	K1	33
82.	I/O	-	-	88	85	124	J1	39
83.	I/O (A6)	54	83	89	86	125	J2	42
84.	I/O (A7)	55	84	90	87	126	J3	45
	GND	56	1	91	88	127	H2	-

\* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

### Additional No Connect (N.C.) Connections on TQ144 Package

TQ144					
135	9	41	67	98	117
136	10	42	68	99	119
140	25	46	77	103	120
141	26	47	78	104	
4	30	62	82	113	
5	31	63	83	114	

**Notes:** Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

### Pin Locations for XC5204 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
	VCC		2	92	89	128	H3	142	-
1.	I/O (A8)		3	93	90	129	H1	143	78
2.	I/O (A9)		4	94	91	130	G1	144	81
3.	I/O		-	95	92	131	G2	145	87
4.	I/O		-	96	93	132	G3	146	90
5.	I/O (A10)		5	97	94	133	F1	147	93
6.	I/O (A11)		6	98	95	134	F2	148	99
7.	I/O		-	-	-	135	E1	149	102
8.	I/O		-	-	-	136	E2	150	105
	GND		-	-	-	137	F3	151	-
9.	I/O		-	-	-	-	D1	152	111
10.	I/O		-	-	-	-	D2	153	114
11.	I/O (A12)		7	99	96	138	E3	154	117
12.	I/O (A13)		8	100	97	139	C1	155	123
13.	I/O		-	-	-	140	C2	156	126

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
14.	I/O		-	-	-	141	D3	157	129
15.	I/O (A14)		9	1	98	142	B1	158	138
16.	I/O (A15)		10	2	99	143	B2	159	141
	VCC		11	3	100	144	C3	160	-
	GND		12	4	1	1	C4	1	-
17.	GCK1 (A16, I/O)		13	5	2	2	B3	2	150
18.	I/O (A17)		14	6	3	3	A1	3	153
19.	I/O		-	-	-	4	A2	4	159
20.	I/O		-	-	-	5	C5	5	162
21.	I/O (TDI)		15	7	4	6	B4	6	165
22.	I/O (TCK)		16	8	5	7	A3	7	171
	GND		-	-	-	8	C6	10	-
23.	I/O		-	-	-	9	B5	11	174
24.	I/O		-	-	-	10	B6	12	177
25.	I/O (TMS)		17	9	6	11	A5	13	180
26.	I/O		18	10	7	12	C7	14	183
27.	I/O		-	-	-	13	B7	15	186
28.	I/O		-	11	8	14	A6	16	189
29.	I/O		19	12	9	15	A7	17	195
30.	I/O		20	13	10	16	A8	18	198
	GND		21	14	11	17	C8	19	-
	VCC		22	15	12	18	B8	20	-
31.	I/O		23	16	13	19	C9	21	201
32.	I/O		24	17	14	20	B9	22	207
33.	I/O		-	18	15	21	A9	23	210
34.	I/O		-	-	-	22	B10	24	213
35.	I/O		25	19	16	23	C10	25	219
36.	I/O		26	20	17	24	A10	26	222
37.	I/O		-	-	-	25	A11	27	225
38.	I/O		-	-	-	26	B11	28	231
	GND		-	-	-	27	C11	29	-
39.	I/O		27	21	18	28	B12	32	234
40.	I/O		-	22	19	29	A13	33	237
41.	I/O		-	-	-	30	A14	34	240
42.	I/O		-	-	-	31	C12	35	243
43.	I/O		28	23	20	32	B13	36	246
44.	I/O		29	24	21	33	B14	37	249
45.	M1 (I/O)		30	25	22	34	A15	38	258
	GND		31	26	23	35	C13	39	-
46.	M0 (I/O)		32	27	24	36	A16	40	261
	VCC		33	28	25	37	C14	41	-
47.	M2 (I/O)		34	29	26	38	B15	42	264
48.	GCK2 (I/O)		35	30	27	39	B16	43	267
49.	I/O (HDC)		36	31	28	40	D14	44	276
50.	I/O		-	-	-	41	C15	45	279
51.	I/O		-	-	-	42	D15	46	282
52.	I/O		-	32	29	43	E14	47	288
53.	I/O (LDC)		37	33	30	44	C16	48	291
54.	I/O		-	-	-	-	E15	49	294
55.	I/O		-	-	-	-	D16	50	300
	GND		-	-	-	45	F14	51	-
56.	I/O		-	-	-	46	F15	52	303

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
57.	I/O		-	-	-	47	E16	53	306
58.	I/O		38	34	31	48	F16	54	312
59.	I/O		39	35	32	49	G14	55	315
60.	I/O		-	36	33	50	G15	56	318
61.	I/O		-	37	34	51	G16	57	324
62.	I/O		40	38	35	52	H16	58	327
63.	I/O ( $\overline{\text{ERR}}$ , $\overline{\text{INIT}}$ )		41	39	36	53	H15	59	330
	VCC		42	40	37	54	H14	60	-
	GND		43	41	38	55	J14	61	-
64.	I/O		44	42	39	56	J15	62	336
65.	I/O		45	43	40	57	J16	63	339
66.	I/O		-	44	41	58	K16	64	348
67.	I/O		-	45	42	59	K15	65	351
68.	I/O		46	46	43	60	K14	66	354
69.	I/O		47	47	44	61	L16	67	360
70.	I/O		-	-	-	62	M16	68	363
71.	I/O		-	-	-	63	L15	69	366
	GND		-	-	-	64	L14	70	-
72.	I/O		-	-	-	-	N16	71	372
73.	I/O		-	-	-	-	M15	72	375
74.	I/O		48	48	45	65	P16	73	378
75.	I/O		49	49	46	66	M14	74	384
76.	I/O		-	-	-	67	N15	75	387
77.	I/O		-	-	-	68	P15	76	390
78.	I/O		50	50	47	69	N14	77	396
79.	I/O		51	51	48	70	R16	78	399
	GND		52	52	49	71	P14	79	-
	DONE		53	53	50	72	R15	80	-
	VCC		54	54	51	73	P13	81	-
	PROG		55	55	52	74	R14	82	-
80.	I/O (D7)		56	56	53	75	T16	83	408
81.	GCK3 (I/O)		57	57	54	76	T15	84	411
82.	I/O		-	-	-	77	R13	85	420
83.	I/O		-	-	-	78	P12	86	423
84.	I/O (D6)		58	58	55	79	T14	87	426
85.	I/O		-	59	56	80	T13	88	432
	GND		-	-	-	81	P11	91	-
86.	I/O		-	-	-	82	R11	92	435
87.	I/O		-	-	-	83	T11	93	438
88.	I/O (D5)		59	60	57	84	T10	94	444
89.	I/O ( $\overline{\text{CS0}}$ )		60	61	58	85	P10	95	447
90.	I/O		-	62	59	86	R10	96	450
91.	I/O		-	63	60	87	T9	97	456
92.	I/O (D4)		61	64	61	88	R9	98	459
93.	I/O		62	65	62	89	P9	99	462
	VCC		63	66	63	90	R8	100	-
	GND		64	67	64	91	P8	101	-
94.	I/O (D3)		65	68	65	92	T8	102	468
95.	I/O ( $\overline{\text{RS}}$ )		66	69	66	93	T7	103	471
96.	I/O		-	70	67	94	T6	104	474
97.	I/O		-	-	-	95	R7	105	480
98.	I/O (D2)		67	71	68	96	P7	106	483

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
99.	I/O		68	72	69	97	T5	107	486
100.	I/O		-	-	-	98	R6	108	492
101.	I/O		-	-	-	99	T4	109	495
	GND		-	-	-	100	P6	110	-
102.	I/O (D1)		69	73	70	101	T3	113	498
103.	I/O (RCLK-BUSY/ RDY)		70	74	71	102	P5	114	504
104.	I/O		-	-	-	103	R4	115	507
105.	I/O		-	-	-	104	R3	116	510
106.	I/O (D0, DIN)		71	75	72	105	P4	117	516
107.	I/O (DOUT)		72	76	73	106	T2	118	519
	CCLK		73	77	74	107	R2	119	-
	VCC		74	78	75	108	P3	120	-
108.	I/O (TDO)		75	79	76	109	T1	121	0
	GND		76	80	77	110	N3	122	-
109.	I/O (A0, $\overline{WS}$ )		77	81	78	111	R1	123	9
110.	GCK4 (A1, I/O)		78	82	79	112	P2	124	15
111.	I/O		-	-	-	113	N2	125	18
112.	I/O		-	-	-	114	M3	126	21
113.	I/O (A2, CS1)		79	83	80	115	P1	127	27
114.	I/O (A3)		80	84	81	116	N1	128	30
115.	I/O		-	-	-	117	M2	129	33
116.	I/O		-	-	-	-	M1	130	39
	GND		-	-	-	118	L3	131	-
117.	I/O		-	-	-	119	L2	132	42
118.	I/O		-	-	-	120	L1	133	45
119.	I/O (A4)		81	85	82	121	K3	134	51
120.	I/O (A5)		82	86	83	122	K2	135	54
121.	I/O		-	87	84	123	K1	137	57
122.	I/O		-	88	85	124	J1	138	63
123.	I/O (A6)		83	89	86	125	J2	139	66
124.	I/O (A7)		84	90	87	126	J3	140	69
	GND		1	91	88	127	H2	141	-

**Additional No Connect (N.C.) Connections for PQ160 Package**

PQ160				
8	30	89	111	136
9	31	90	112	

**Notes:** Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

## Pin Locations for XC5206 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	VCC	2	92	89	128	142	155	J4	183	-
1.	I/O (A8)	3	93	90	129	143	156	J3	184	87
2.	I/O (A9)	4	94	91	130	144	157	J2	185	90
3.	I/O	-	95	92	131	145	158	J1	186	93
4.	I/O	-	96	93	132	146	159	H1	187	99
5.	I/O	-	-	-	-	-	160	H2	188	102
6.	I/O	-	-	-	-	-	161	H3	189	105
7.	I/O (A10)	5	97	94	133	147	162	G1	190	111
8.	I/O (A11)	6	98	95	134	148	163	G2	191	114
9.	I/O	-	-	-	135	149	164	F1	192	117
10.	I/O	-	-	-	136	150	165	E1	193	123
	GND	-	-	-	137	151	166	G3	194	-
11.	I/O	-	-	-	-	152	168	C1	197	126
12.	I/O	-	-	-	-	153	169	E2	198	129
13.	I/O (A12)	7	99	96	138	154	170	F3	199	138
14.	I/O (A13)	8	100	97	139	155	171	D2	200	141
15.	I/O	-	-	-	140	156	172	B1	201	150
16.	I/O	-	-	-	141	157	173	E3	202	153
17.	I/O (A14)	9	1	98	142	158	174	C2	203	162
18.	I/O (A15)	10	2	99	143	159	175	B2	204	165
	VCC	11	3	100	144	160	176	D3	205	-
	GND	12	4	1	1	1	1	D4	2	-
19.	GCK1 (A16, I/O)	13	5	2	2	2	2	C3	4	174
20.	I/O (A17)	14	6	3	3	3	3	C4	5	177
21.	I/O	-	-	-	4	4	4	B3	6	183
22.	I/O	-	-	-	5	5	5	C5	7	186
23.	I/O (TDI)	15	7	4	6	6	6	A2	8	189
24.	I/O (TCK)	16	8	5	7	7	7	B4	9	195
25.	I/O	-	-	-	-	8	8	C6	10	198
26.	I/O	-	-	-	-	9	9	A3	11	201
	GND	-	-	-	8	10	10	C7	14	-
27.	I/O	-	-	-	9	11	11	A4	15	207
28.	I/O	-	-	-	10	12	12	A5	16	210
29.	I/O (TMS)	17	9	6	11	13	13	B7	17	213
30.	I/O	18	10	7	12	14	14	A6	18	219
31.	I/O	-	-	-	-	-	15	C8	19	222
32.	I/O	-	-	-	-	-	16	A7	20	225
33.	I/O	-	-	-	13	15	17	B8	21	234
34.	I/O	-	11	8	14	16	18	A8	22	237
35.	I/O	19	12	9	15	17	19	B9	23	246
36.	I/O	20	13	10	16	18	20	C9	24	249
	GND	21	14	11	17	19	21	D9	25	-
	VCC	22	15	12	18	20	22	D10	26	-
37.	I/O	23	16	13	19	21	23	C10	27	255
38.	I/O	24	17	14	20	22	24	B10	28	258
39.	I/O	-	18	15	21	23	25	A9	29	261
40.	I/O	-	-	-	22	24	26	A10	30	267
41.	I/O	-	-	-	-	-	27	A11	31	270

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O ( <u>ERR</u> , <u>INIT</u> )	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
86.	I/O	-	-	-	-	71	79	T18	93	459

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
87.	I/O	-	-	-	-	72	80	P17	94	468
88.	I/O	48	48	45	65	73	81	N16	95	471
89.	I/O	49	49	46	66	74	82	T17	96	480
90.	I/O	-	-	-	67	75	83	R17	97	483
91.	I/O	-	-	-	68	76	84	P16	98	486
92.	I/O	50	50	47	69	77	85	U18	99	492
93.	I/O	51	51	48	70	78	86	T16	100	495
	GND	52	52	49	71	79	87	R16	101	-
	DONE	53	53	50	72	80	88	U17	103	-
	VCC	54	54	51	73	81	89	R15	106	-
	PROG	55	55	52	74	82	90	V18	108	-
94.	I/O (D7)	56	56	53	75	83	91	T15	109	504
95.	GCK3 (I/O)	57	57	54	76	84	92	U16	110	507
96.	I/O	-	-	-	77	85	93	T14	111	516
97.	I/O	-	-	-	78	86	94	U15	112	519
98.	I/O (D6)	58	58	55	79	87	95	V17	113	522
99.	I/O	-	59	56	80	88	96	V16	114	528
100.	I/O	-	-	-	-	89	97	T13	115	531
101.	I/O	-	-	-	-	90	98	U14	116	534
	GND	-	-	-	81	91	99	T12	119	-
102.	I/O	-	-	-	82	92	100	U13	120	540
103.	I/O	-	-	-	83	93	101	V13	121	543
104.	I/O (D5)	59	60	57	84	94	102	U12	122	552
105.	I/O (CS0)	60	61	58	85	95	103	V12	123	555
106.	I/O	-	-	-	-	-	104	T11	124	558
107.	I/O	-	-	-	-	-	105	U11	125	564
108.	I/O	-	62	59	86	96	106	V11	126	567
109.	I/O	-	63	60	87	97	107	V10	127	570
110.	I/O (D4)	61	64	61	88	98	108	U10	128	576
111.	I/O	62	65	62	89	99	109	T10	129	579
	VCC	63	66	63	90	100	110	R10	130	-
	GND	64	67	64	91	101	111	R9	131	-
112.	I/O (D3)	65	68	65	92	102	112	T9	132	588
113.	I/O (RS)	66	69	66	93	103	113	U9	133	591
114.	I/O	-	70	67	94	104	114	V9	134	600
115.	I/O	-	-	-	95	105	115	V8	135	603
116.	I/O	-	-	-	-	-	116	U8	136	612
117.	I/O	-	-	-	-	-	117	T8	137	615
118.	I/O (D2)	67	71	68	96	106	118	V7	138	618
119.	I/O	68	72	69	97	107	119	U7	139	624
120.	I/O	-	-	-	98	108	120	V6	140	627
121.	I/O	-	-	-	99	109	121	U6	141	630
	GND	-	-	-	100	110	122	T7	142	-
122.	I/O	-	-	-	-	111	123	U5	145	636
123.	I/O	-	-	-	-	112	124	T6	146	639
124.	I/O (D1)	69	73	70	101	113	125	V3	147	642
125.	I/O (RCLK-BUSY/RDY)	70	74	71	102	114	126	V2	148	648
126.	I/O	-	-	-	103	115	127	U4	149	651
127.	I/O	-	-	-	104	116	128	T5	150	654
128.	I/O (D0, DIN)	71	75	72	105	117	129	U3	151	660
129.	I/O (DOUT)	72	76	73	106	118	130	T4	152	663

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	CCLK	73	77	74	107	119	131	V1	153	-
	VCC	74	78	75	108	120	132	R4	154	-
130.	I/O (TDO)	75	79	76	109	121	133	U2	159	-
	GND	76	80	77	110	122	134	R3	160	-
131.	I/O (A0, $\overline{WS}$ )	77	81	78	111	123	135	T3	161	9
132.	GCK4 (A1, I/O)	78	82	79	112	124	136	U1	162	15
133.	I/O	-	-	-	113	125	137	P3	163	18
134.	I/O	-	-	-	114	126	138	R2	164	21
135.	I/O (A2, CS1)	79	83	80	115	127	139	T2	165	27
136.	I/O (A3)	80	84	81	116	128	140	N3	166	30
137.	I/O	-	-	-	117	129	141	P2	167	33
138.	I/O	-	-	-	-	130	142	T1	168	42
	GND	-	-	-	118	131	143	M3	171	-
139.	I/O	-	-	-	119	132	144	P1	172	45
140.	I/O	-	-	-	120	133	145	N1	173	51
141.	I/O (A4)	81	85	82	121	134	146	M2	174	54
142.	I/O (A5)	82	86	83	122	135	147	M1	175	57
143.	I/O	-	-	-	-	-	148	L3	176	63
144.	I/O	-	-	-	-	136	149	L2	177	66
145.	I/O	-	87	84	123	137	150	L1	178	69
146.	I/O	-	88	85	124	138	151	K1	179	75
147.	I/O (A6)	83	89	86	125	139	152	K2	180	78
148.	I/O (A7)	84	90	87	126	140	153	K3	181	81
	GND	1	91	88	127	141	154	K4	182	-

### Additional No Connect (N.C.) Connections for PQ208 and TQ176 Packages

PQ208							TQ176
195	1	39	65	104	144	169	167
196	3	51	66	107	155	170	
206	12	52	91	117	156		
207	13	53	92	118	157		
208	38	54	102	143	158		

**Notes:** Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

### Pin Locations for XC5210 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	VCC	2	128	142	155	183	J4	VCC*	212	-
1.	I/O (A8)	3	129	143	156	184	J3	E8	213	111
2.	I/O (A9)	4	130	144	157	185	J2	B7	214	114
3.	I/O	-	131	145	158	186	J1	A7	215	117
4.	I/O	-	132	146	159	187	H1	C7	216	123
5.	I/O	-	-	-	160	188	H2	D7	217	126
6.	I/O	-	-	-	161	189	H3	E7	218	129

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
7.	I/O (A10)	5	133	147	162	190	G1	A6	220	135
8.	I/O (A11)	6	134	148	163	191	G2	B6	221	138
	VCC	-	-	-	-	-	-	VCC*	222	-
9.	I/O	-	-	-	-	-	H4	C6	223	141
10.	I/O	-	-	-	-	-	G4	F7	224	150
11.	I/O	-	135	149	164	192	F1	A5	225	153
12.	I/O	-	136	150	165	193	E1	B5	226	162
	GND	-	137	151	166	194	G3	GND*	227	-
13.	I/O	-	-	-	-	195	F2	D6	228	165
14.	I/O	-	-	-	167	196	D1	C5	229	171
15.	I/O	-	-	152	168	197	C1	A4	230	174
16.	I/O	-	-	153	169	198	E2	E6	231	177
17.	I/O (A12)	7	138	154	170	199	F3	B4	232	183
18.	I/O (A13)	8	139	155	171	200	D2	D5	233	186
19.	I/O	-	-	-	-	-	F4	A3	234	189
20.	I/O	-	-	-	-	-	E4	C4	235	195
21.	I/O	-	140	156	172	201	B1	B3	236	198
22.	I/O	-	141	157	173	202	E3	F6	237	201
23.	I/O (A14)	9	142	158	174	203	C2	A2	238	210
24.	I/O (A15)	10	143	159	175	204	B2	C3	239	213
	VCC	11	144	160	176	205	D3	VCC*	240	-
	GND	12	1	1	1	2	D4	GND*	1	-
25.	GCK1 (A16, I/O)	13	2	2	2	4	C3	D4	2	222
26.	I/O (A17)	14	3	3	3	5	C4	B1	3	225
27.	I/O	-	4	4	4	6	B3	C2	4	231
28.	I/O	-	5	5	5	7	C5	E5	5	234
29.	I/O (TDI)	15	6	6	6	8	A2	D3	6	237
30.	I/O (TCK)	16	7	7	7	9	B4	C1	7	243
31.	I/O	-	-	8	8	10	C6	D2	8	246
32.	I/O	-	-	9	9	11	A3	G6	9	249
33.	I/O	-	-	-	-	12	B5	E4	10	255
34.	I/O	-	-	-	-	13	B6	D1	11	258
35.	I/O	-	-	-	-	-	D5	E3	12	261
36.	I/O	-	-	-	-	-	D6	E2	13	267
	GND	-	8	10	10	14	C7	GND*	14	-
37.	I/O	-	9	11	11	15	A4	F5	15	270
38.	I/O	-	10	12	12	16	A5	E1	16	273
39.	I/O (TMS)	17	11	13	13	17	B7	F4	17	279
40.	I/O	18	12	14	14	18	A6	F3	18	282
	VCC	-	-	-	-	-	-	VCC*	19	-
41.	I/O	-	-	-	-	-	D7	F2	20	285
42.	I/O	-	-	-	-	-	D8	F1	21	291
43.	I/O	-	-	-	15	19	C8	G4	23	294
44.	I/O	-	-	-	16	20	A7	G3	24	297
45.	I/O	-	13	15	17	21	B8	G2	25	306
46.	I/O	-	14	16	18	22	A8	G1	26	309
47.	I/O	19	15	17	19	23	B9	G5	27	318
48.	I/O	20	16	18	20	24	C9	H3	28	321
	GND	21	17	19	21	25	D9	GND*	29	-
	VCC	22	18	20	22	26	D10	VCC*	30	-
49.	I/O	23	19	21	23	27	C10	H4	31	327

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
50.	I/O	24	20	22	24	28	B10	H5	32	330
51.	I/O	-	21	23	25	29	A9	J2	33	333
52.	I/O	-	22	24	26	30	A10	J1	34	339
53.	I/O	-	-	-	27	31	A11	J3	35	342
54.	I/O	-	-	-	28	32	C11	J4	36	345
55.	I/O	-	-	-	-	-	D11	J5	38	351
56.	I/O	-	-	-	-	-	D12	K1	39	354
	VCC	-	-	-	-	-	-	VCC*	40	-
57.	I/O	25	23	25	29	33	B11	K2	41	357
58.	I/O	26	24	26	30	34	A12	K3	42	363
59.	I/O	-	25	27	31	35	B12	J6	43	366
60.	I/O	-	26	28	32	36	A13	L1	44	369
	GND	-	27	29	33	37	C12	GND*	45	-
61.	I/O	-	-	-	-	-	D13	L2	46	375
62.	I/O	-	-	-	-	-	D14	K4	47	378
63.	I/O	-	-	-	-	38	B13	L3	48	381
64.	I/O	-	-	-	-	39	A14	M1	49	387
65.	I/O	-	-	30	34	40	A15	K5	50	390
66.	I/O	-	-	31	35	41	C13	M2	51	393
67.	I/O	27	28	32	36	42	B14	L4	52	399
68.	I/O	-	29	33	37	43	A16	N1	53	402
69.	I/O	-	30	34	38	44	B15	M3	54	405
70.	I/O	-	31	35	39	45	C14	N2	55	411
71.	I/O	28	32	36	40	46	A17	K6	56	414
72.	I/O	29	33	37	41	47	B16	P1	57	417
73.	M1 (I/O)	30	34	38	42	48	C15	N3	58	426
	GND	31	35	39	43	49	D15	GND*	59	-
74.	M0 (I/O)	32	36	40	44	50	A18	P2	60	429
	VCC	33	37	41	45	55	D16	VCC*	61	-
75.	M2 (I/O)	34	38	42	46	56	C16	M4	62	432
76.	GCK2 (I/O)	35	39	43	47	57	B17	R2	63	435
77.	I/O (HDC)	36	40	44	48	58	E16	P3	64	444
78.	I/O	-	41	45	49	59	C17	L5	65	447
79.	I/O	-	42	46	50	60	D17	N4	66	450
80.	I/O	-	43	47	51	61	B18	R3	67	456
81.	I/O (LDC)	37	44	48	52	62	E17	P4	68	459
82.	I/O	-	-	49	53	63	F16	K7	69	462
83.	I/O	-	-	50	54	64	C18	M5	70	468
84.	I/O	-	-	-	-	65	D18	R4	71	471
85.	I/O	-	-	-	-	66	F17	N5	72	474
86.	I/O	-	-	-	-	-	E15	P5	73	480
87.	I/O	-	-	-	-	-	F15	L6	74	483
	GND	-	45	51	55	67	G16	GND*	75	-
88.	I/O	-	46	52	56	68	E18	R5	76	486
89.	I/O	-	47	53	57	69	F18	M6	77	492
90.	I/O	38	48	54	58	70	G17	N6	78	495
91.	I/O	39	49	55	59	71	G18	P6	79	504
	VCC	-	-	-	-	-	-	VCC*	80	-
92.	I/O	-	-	-	60	72	H16	R6	81	507
93.	I/O	-	-	-	61	73	H17	M7	82	510
94.	I/O	-	-	-	-	-	G15	N7	84	516

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
95.	I/O	-	-	-	-	-	H15	P7	85	519
96.	I/O	-	50	56	62	74	H18	R7	86	522
97.	I/O	-	51	57	63	75	J18	L7	87	528
98.	I/O	40	52	58	64	76	J17	N8	88	531
99.	I/O (ERR, INIT)	41	53	59	65	77	J16	P8	89	534
	VCC	42	54	60	66	78	J15	VCC*	90	-
	GND	43	55	61	67	79	K15	GND*	91	-
100.	I/O	44	56	62	68	80	K16	L8	92	540
101.	I/O	45	57	63	69	81	K17	P9	93	543
102.	I/O	-	58	64	70	82	K18	R9	94	546
103.	I/O	-	59	65	71	83	L18	N9	95	552
104.	I/O	-	-	-	72	84	L17	M9	96	555
105.	I/O	-	-	-	73	85	L16	L9	97	558
106.	I/O	-	-	-	-	-	L15	R10	99	564
107.	I/O	-	-	-	-	-	M15	P10	100	567
	VCC	-	-	-	-	-	-	VCC*	101	-
108.	I/O	46	60	66	74	86	M18	N10	102	570
109.	I/O	47	61	67	75	87	M17	K9	103	576
110.	I/O	-	62	68	76	88	N18	R11	104	579
111.	I/O	-	63	69	77	89	P18	P11	105	588
	GND	-	64	70	78	90	M16	GND*	106	-
112.	I/O	-	-	-	-	-	N15	M10	107	591
113.	I/O	-	-	-	-	-	P15	N11	108	600
114.	I/O	-	-	-	-	91	N17	R12	109	603
115.	I/O	-	-	-	-	92	R18	L10	110	606
116.	I/O	-	-	71	79	93	T18	P12	111	612
117.	I/O	-	-	72	80	94	P17	M11	112	615
118.	I/O	48	65	73	81	95	N16	R13	113	618
119.	I/O	49	66	74	82	96	T17	N12	114	624
120.	I/O	-	67	75	83	97	R17	P13	115	627
121.	I/O	-	68	76	84	98	P16	K10	116	630
122.	I/O	50	69	77	85	99	U18	R14	117	636
123.	I/O	51	70	78	86	100	T16	N13	118	639
	GND	52	71	79	87	101	R16	GND*	119	-
	DONE	53	72	80	88	103	U17	P14	120	-
	VCC	54	73	81	89	106	R15	VCC*	121	-
	PROG	55	74	82	90	108	V18	M12	122	-
124.	I/O (D7)	56	75	83	91	109	T15	P15	123	648
125.	GCK3 (I/O)	57	76	84	92	110	U16	N14	124	651
126.	I/O	-	77	85	93	111	T14	L11	125	660
127.	I/O	-	78	86	94	112	U15	M13	126	663
128.	I/O	-	-	-	-	-	R14	N15	127	666
129.	I/O	-	-	-	-	-	R13	M14	128	672
130.	I/O (D6)	58	79	87	95	113	V17	J10	129	675
131.	I/O	-	80	88	96	114	V16	L12	130	678
132.	I/O	-	-	89	97	115	T13	M15	131	684
133.	I/O	-	-	90	98	116	U14	L13	132	687
134.	I/O	-	-	-	-	117	V15	L14	133	690
135.	I/O	-	-	-	-	118	V14	K11	134	696
	GND	-	81	91	99	119	T12	GND*	135	-
136.	I/O	-	-	-	-	-	R12	L15	136	699

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
137.	I/O	-	-	-	-	-	R11	K12	137	708
138.	I/O	-	82	92	100	120	U13	K13	138	711
139.	I/O	-	83	93	101	121	V13	K14	139	714
	VCC	-	-	-	-	-	-	VCC*	140	-
140.	I/O (D5)	59	84	94	102	122	U12	K15	141	720
141.	I/O (CS0)	60	85	95	103	123	V12	J12	142	723
142.	I/O	-	-	-	104	124	T11	J13	144	726
143.	I/O	-	-	-	105	125	U11	J14	145	732
144.	I/O	-	86	96	106	126	V11	J15	146	735
145.	I/O	-	87	97	107	127	V10	J11	147	738
146.	I/O (D4)	61	88	98	108	128	U10	H13	148	744
147.	I/O	62	89	99	109	129	T10	H14	149	747
	VCC	63	90	100	110	130	R10	VCC*	150	-
	GND	64	91	101	111	131	R9	GND*	151	-
148.	I/O (D3)	65	92	102	112	132	T9	H12	152	756
149.	I/O (RS)	66	93	103	113	133	U9	H11	153	759
150.	I/O	-	94	104	114	134	V9	G14	154	768
151.	I/O	-	95	105	115	135	V8	G15	155	771
152.	I/O	-	-	-	116	136	U8	G13	156	780
153.	I/O	-	-	-	117	137	T8	G12	157	783
154.	I/O (D2)	67	96	106	118	138	V7	G11	159	786
155.	I/O	68	97	107	119	139	U7	F15	160	792
	VCC	-	-	-	-	-	-	VCC*	161	-
156.	I/O	-	98	108	120	140	V6	F14	162	795
157.	I/O	-	99	109	121	141	U6	F13	163	798
158.	I/O	-	-	-	-	-	R8	G10	164	804
159.	I/O	-	-	-	-	-	R7	E15	165	807
	GND	-	100	110	122	142	T7	GND*	166	-
160.	I/O	-	-	-	-	-	R6	E14	167	810
161.	I/O	-	-	-	-	-	R5	F12	168	816
162.	I/O	-	-	-	-	143	V5	E13	169	819
163.	I/O	-	-	-	-	144	V4	D15	170	822
164.	I/O	-	-	111	123	145	U5	F11	171	828
165.	I/O	-	-	112	124	146	T6	D14	172	831
166.	I/O (D1)	69	101	113	125	147	V3	E12	173	834
167.	I/O (RCLK-BUSY/RDY)	70	102	114	126	148	V2	C15	174	840
168.	I/O	-	103	115	127	149	U4	D13	175	843
169.	I/O	-	104	116	128	150	T5	C14	176	846
170.	I/O (D0, DIN)	71	105	117	129	151	U3	F10	177	855
171.	I/O (DOUT)	72	106	118	130	152	T4	B15	178	858
	CCLK	73	107	119	131	153	V1	C13	179	-
	VCC	74	108	120	132	154	R4	VCC*	180	-
172.	I/O (TDO)	75	109	121	133	159	U2	A15	181	-
	GND	76	110	122	134	160	R3	GND*	182	-
173.	I/O (A0, $\bar{WS}$ )	77	111	123	135	161	T3	A14	183	9
174.	GCK4 (A1, I/O)	78	112	124	136	162	U1	B13	184	15
175.	I/O	-	113	125	137	163	P3	E11	185	18
176.	I/O	-	114	126	138	164	R2	C12	186	21
177.	I/O (CS1, A2)	79	115	127	139	165	T2	A13	187	27
178.	I/O (A3)	80	116	128	140	166	N3	B12	188	30
179.	I/O	-	-	-	-	-	P4	F9	189	33

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
180.	I/O	-	-	-	-	-	N4	D11	190	39
181.	I/O	-	117	129	141	167	P2	A12	191	42
182.	I/O	-	-	130	142	168	T1	C11	192	45
183.	I/O	-	-	-	-	169	R1	B11	193	51
184.	I/O	-	-	-	-	170	N2	E10	194	54
	-	-	-	-	-	-	-	GND*	-	-
	GND	-	118	131	143	171	M3	-	196	-
185.	I/O	-	119	132	144	172	P1	A11	197	57
186.	I/O	-	120	133	145	173	N1	D10	198	66
187.	I/O	-	-	-	-	-	M4	C10	199	69
188.	I/O	-	-	-	-	-	L4	B10	200	75
	VCC	-	-	-	-	-	-	VCC*	201	-
189.	I/O (A4)	81	121	134	146	174	M2	A10	202	78
190.	I/O (A5)	82	122	135	147	175	M1	D9	203	81
191.	I/O	-	-	-	148	176	L3	C9	205	87
192.	I/O	-	-	136	149	177	L2	B9	206	90
193.	I/O	-	123	137	150	178	L1	A9	207	93
194.	I/O	-	124	138	151	179	K1	E9	208	99
195.	I/O (A6)	83	125	139	152	180	K2	C8	209	102
196.	I/O (A7)	84	126	140	153	181	K3	B8	210	105
	GND	1	127	141	154	182	K4	GND*	211	-

### Additional No Connect (N.C.) Connections for PQ208 and PQ240 Packages

PQ208				PQ240			
1	53	107	158	22	143	219	
3	54	155	206	37	158		
51	102	156	207	83	195		
52	104	157	208	98	204		

**Notes:** \* Pins labeled VCC\* are internally bonded to a VCC plane within the BG225 package. The external pins are: B2, D8, H15, R8, B14, R1, H1, and R15.

Pins labeled GND\* are internally bonded to a ground plane within the BG225 package. The external pins are: A1, D12, G7, G9, H6, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8.

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

### Pin Locations for XC5215 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
	VCC	142	183	212	K1	38	VCC*	VCC*	-
1.	I/O (A8)	143	184	213	K2	37	E8	D14	138
2.	I/O (A9)	144	185	214	K3	36	B7	C14	141
3.	I/O	145	186	215	K5	35	A7	A15	147
4.	I/O	146	187	216	K4	34	C7	B15	150
5.	I/O	-	188	217	J1	33	D7	C15	153
6.	I/O	-	189	218	J2	32	E7	D15	159
7.	I/O (A10)	147	190	220	H1	31	A6	A16	162

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
8.	I/O (A11)	148	191	221	J3	30	B6	B16	165
9.	I/O	-	-	-	H2	27	-	C17	171
10.	I/O	-	-	-	G1	26	-	B18	174
	VCC	-	-	222	E1	25	VCC*	VCC*	-
11.	I/O	-	-	223	H3	23	C6	C18	177
12.	I/O	-	-	224	G2	22	F7	D17	183
13.	I/O	149	192	225	H4	21	A5	A20	186
14.	I/O	150	193	226	F2	20	B5	B19	189
	GND	151	194	227	F1	19	GND*	GND*	-
15.	I/O	-	-	-	H5	18	-	C19	195
16.	I/O	-	-	-	G3	17	-	D18	198
17.	I/O	-	195	228	D1	16	D6	A21	201
18.	I/O	-	196	229	G4	15	C5	B20	207
19.	I/O	152	197	230	E2	14	A4	C20	210
20.	I/O	153	198	231	F3	13	E6	B21	213
21.	I/O (A12)	154	199	232	G5	12	B4	B22	219
22.	I/O (A13)	155	200	233	C1	10	D5	C21	222
23.	I/O	-	-	-	F4	9	-	D20	225
24.	I/O	-	-	-	E3	8	-	A23	234
25.	I/O	-	-	234	D2	7	A3	D21	237
26.	I/O	-	-	235	C2	6	C4	C22	243
27.	I/O	156	201	236	F5	5	B3	B24	246
28.	I/O	157	202	237	E4	4	F6	C23	249
29.	I/O (A14)	158	203	238	D3	3	A2	D22	258
30.	I/O (A15)	159	204	239	C3	2	C3	C24	261
	VCC	160	205	240	A2	1	VCC*	VCC*	-
	GND	1	2	1	B1	304	GND*	GND*	-
31.	GCK1 (A16, I/O)	2	4	2	D4	303	D4	D23	270
32.	I/O (A17)	3	5	3	B2	302	B1	C25	273
33.	I/O	4	6	4	B3	301	C2	D24	279
34.	I/O	5	7	5	E6	300	E5	E23	282
35.	I/O (TDI)	6	8	6	D5	299	D3	C26	285
36.	I/O (TCK)	7	9	7	C4	298	C1	E24	294
37.	I/O	-	-	-	A3	297	-	F24	297
38.	I/O	-	-	-	D6	296	-	E25	303
39.	I/O	8	10	8	E7	295	D2	D26	306
40.	I/O	9	11	9	B4	294	G6	G24	309
41.	I/O	-	12	10	C5	293	E4	F25	315
42.	I/O	-	13	11	A4	292	D1	F26	318
43.	I/O	-	-	12	D7	291	E3	H23	321
44.	I/O	-	-	13	C6	290	E2	H24	327
45.	I/O	-	-	-	E8	289	-	G25	330
46.	I/O	-	-	-	B5	288	-	G26	333
	GND	10	14	14	A5	287	GND*	GND*	-
47.	I/O	11	15	15	B6	286	F5	J23	339
48.	I/O	12	16	16	D8	285	E1	J24	342
49.	I/O (TMS)	13	17	17	C7	284	F4	H25	345
50.	I/O	14	18	18	B7	283	F3	K23	351
	VCC	-	-	19	A6	282	VCC*	VCC*	-
51.	I/O	-	-	20	C8	280	F2	L24	354
52.	I/O	-	-	21	E9	279	F1	K25	357
53.	I/O	-	-	-	B8	276	-	L25	363

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
54.	I/O	-	-	-	A8	275	-	L26	366
55.	I/O	-	19	23	C9	274	G4	M23	369
56.	I/O	-	20	24	B9	273	G3	M24	375
57.	I/O	15	21	25	E10	272	G2	M25	378
58.	I/O	16	22	26	A9	271	G1	M26	381
59.	I/O	17	23	27	D10	270	G5	N24	390
60.	I/O	18	24	28	C10	269	H3	N25	393
	GND	19	25	29	A10	268	GND*	GND*	-
	VCC	20	26	30	A11	267	VCC*	VCC*	-
61.	I/O	21	27	31	B10	266	H4	N26	399
62.	I/O	22	28	32	B11	265	H5	P25	402
63.	I/O	23	29	33	C11	264	J2	P23	405
64.	I/O	24	30	34	E11	263	J1	P24	411
65.	I/O	-	31	35	D11	262	J3	R26	414
66.	I/O	-	32	36	A12	261	J4	R25	417
67.	I/O	-	-	-	B12	260	-	R24	423
68.	I/O	-	-	-	A13	259	-	R23	426
69.	I/O	-	-	38	E12	256	J5	T26	429
70.	I/O	-	-	39	B13	255	K1	T25	435
	VCC	-	-	40	A16	253	VCC*	VCC*	-
71.	I/O	25	33	41	A14	252	K2	U24	438
72.	I/O	26	34	42	C13	251	K3	V25	441
73.	I/O	27	35	43	B14	250	J6	V24	447
74.	I/O	28	36	44	D13	249	L1	U23	450
	GND	29	37	45	A15	248	GND*	GND*	-
75.	I/O	-	-	-	B15	247	-	Y26	453
76.	I/O	-	-	-	E13	246	-	W25	459
77.	I/O	-	-	46	C14	245	L2	W24	462
78.	I/O	-	-	47	A17	244	K4	V23	465
79.	I/O	-	38	48	D14	243	L3	AA26	471
80.	I/O	-	39	49	B16	242	M1	Y25	474
81.	I/O	30	40	50	C15	241	K5	Y24	477
82.	I/O	31	41	51	E14	240	M2	AA25	483
83.	I/O	-	-	-	A18	239	-	AB25	486
84.	I/O	-	-	-	D15	238	-	AA24	489
85.	I/O	32	42	52	C16	237	L4	Y23	495
86.	I/O	33	43	53	B17	236	N1	AC26	498
87.	I/O	34	44	54	B18	235	M3	AA23	501
88.	I/O	35	45	55	E15	234	N2	AB24	507
89.	I/O	36	46	56	D16	233	K6	AD25	510
90.	I/O	37	47	57	C17	232	P1	AC24	513
91.	M1 (I/O)	38	48	58	A20	231	N3	AB23	522
	GND	39	49	59	A19	230	GND*	GND*	-
92.	M0 (I/O)	40	50	60	C18	229	P2	AD24	525
	VCC	41	55	61	B20	228	VCC*	VCC*	-
93.	M2 (I/O)	42	56	62	D17	227	M4	AC23	528
94.	GCK2 (I/O)	43	57	63	B19	226	R2	AE24	531
95.	I/O (HDC)	44	58	64	C19	225	P3	AD23	540
96.	I/O	45	59	65	F16	224	L5	AC22	543
97.	I/O	46	60	66	E17	223	N4	AF24	546
98.	I/O	47	61	67	D18	222	R3	AD22	552
99.	I/O (LDC)	48	62	68	C20	221	P4	AE23	555

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
100.	I/O	-	-	-	F17	220	-	AE22	558
101.	I/O	-	-	-	G16	219	-	AF23	564
102.	I/O	49	63	69	D19	218	K7	AD20	567
103.	I/O	50	64	70	E18	217	M5	AE21	570
104.	I/O	-	65	71	D20	216	R4	AF21	576
105.	I/O	-	66	72	G17	215	N5	AC19	579
106.	I/O	-	-	73	F18	214	P5	AD19	582
107.	I/O	-	-	74	H16	213	L6	AE20	588
108.	I/O	-	-	-	E19	212	-	AF20	591
109.	I/O	-	-	-	F19	211	-	AC18	594
	GND	51	67	75	E20	210	GND*	GND*	-
110.	I/O	52	68	76	H17	209	R5	AD18	600
111.	I/O	53	69	77	G18	208	M6	AE19	603
112.	I/O	54	70	78	G19	207	N6	AC17	606
113.	I/O	55	71	79	H18	206	P6	AD17	612
	VCC	-	-	80	F20	204	VCC*	VCC*	-
114.	I/O	-	72	81	J16	203	R6	AE17	615
115.	I/O	-	73	82	G20	202	M7	AE16	618
116.	I/O	-	-	-	H20	199	-	AF16	624
117.	I/O	-	-	-	J18	198	-	AC15	627
118.	I/O	-	-	84	J19	197	N7	AD15	630
119.	I/O	-	-	85	K16	196	P7	AE15	636
120.	I/O	56	74	86	J20	195	R7	AF15	639
121.	I/O	57	75	87	K17	194	L7	AD14	642
122.	I/O	58	76	88	K18	193	N8	AE14	648
123.	I/O (ERR, INIT)	59	77	89	K19	192	P8	AF14	651
	VCC	60	78	90	L20	191	VCC*	VCC*	-
	GND	61	79	91	K20	190	GND*	GND*	-
124.	I/O	62	80	92	L19	189	L8	AE13	660
125.	I/O	63	81	93	L18	188	P9	AC13	663
126.	I/O	64	82	94	L16	187	R9	AD13	672
127.	I/O	65	83	95	L17	186	N9	AF12	675
128.	I/O	-	84	96	M20	185	M9	AE12	678
129.	I/O	-	85	97	M19	184	L9	AD12	684
130.	I/O	-	-	-	N20	183	-	AC12	687
131.	I/O	-	-	-	M18	182	-	AF11	690
132.	I/O	-	-	99	N19	179	R10	AE11	696
133.	I/O	-	-	100	P20	178	P10	AD11	699
	VCC	-	-	101	T20	177	VCC*	VCC*	-
134.	I/O	66	86	102	N18	175	N10	AE9	702
135.	I/O	67	87	103	P19	174	K9	AD9	708
136.	I/O	68	88	104	N17	173	R11	AC10	711
137.	I/O	69	89	105	R19	172	P11	AF7	714
	GND	70	90	106	R20	171	GND*	GND*	-
138.	I/O	-	-	-	N16	170	-	AE8	720
139.	I/O	-	-	-	P18	169	-	AD8	723
140.	I/O	-	-	107	U20	168	M10	AC9	726
141.	I/O	-	-	108	P17	167	N11	AF6	732
142.	I/O	-	91	109	T19	166	R12	AE7	735
143.	I/O	-	92	110	R18	165	L10	AD7	738
144.	I/O	71	93	111	P16	164	P12	AE6	744
145.	I/O	72	94	112	V20	163	M11	AE5	747

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
146.	I/O	-	-	-	R17	162	-	AD6	750
147.	I/O	-	-	-	T18	161	-	AC7	756
148.	I/O	73	95	113	U19	160	R13	AF4	759
149.	I/O	74	96	114	V19	159	N12	AF3	768
150.	I/O	75	97	115	R16	158	P13	AD5	771
151.	I/O	76	98	116	T17	157	K10	AE3	774
152.	I/O	77	99	117	U18	156	R14	AD4	780
153.	I/O	78	100	118	X20	155	N13	AC5	783
	GND	79	101	119	W20	154	GND*	GND*	-
	DONE	80	103	120	V18	153	P14	AD3	-
	VCC	81	106	121	X19	152	VCC*	VCC*	-
	PROG	82	108	122	U17	151	M12	AC4	-
154.	I/O (D7)	83	109	123	W19	150	P15	AD2	792
155.	GCK3 (I/O)	84	110	124	W18	149	N14	AC3	795
156.	I/O	85	111	125	T15	148	L11	AB4	804
157.	I/O	86	112	126	U16	147	M13	AD1	807
158.	I/O	-	-	127	V17	146	N15	AA4	810
159.	I/O	-	-	128	X18	145	M14	AA3	816
160.	I/O	-	-	-	U15	144	-	AB2	819
161.	I/O	-	-	-	T14	143	-	AC1	828
162.	I/O (D6)	87	113	129	W17	142	J10	Y3	831
163.	I/O	88	114	130	V16	141	L12	AA2	834
164.	I/O	89	115	131	X17	140	M15	AA1	840
165.	I/O	90	116	132	U14	139	L13	W4	843
166.	I/O	-	117	133	V15	138	L14	W3	846
167.	I/O	-	118	134	T13	137	K11	Y2	852
168.	I/O	-	-	-	W16	136	-	Y1	855
169.	I/O	-	-	-	W15	135	-	V4	858
	GND	91	119	135	X16	134	GND*	GND*	-
170.	I/O	-	-	136	U13	133	L15	V3	864
171.	I/O	-	-	137	V14	132	K12	W2	867
172.	I/O	92	120	138	W14	131	K13	U4	870
173.	I/O	93	121	139	V13	130	K14	U3	876
	VCC	-	-	140	X15	129	VCC*	VCC*	-
174.	I/O (D5)	94	122	141	T12	127	K15	V2	879
175.	I/O (CS0)	95	123	142	X14	126	J12	V1	882
176.	I/O	-	-	-	X13	123	-	T1	888
177.	I/O	-	-	-	V12	122	-	R4	891
178.	I/O	-	124	144	W12	121	J13	R3	894
179.	I/O	-	125	145	T11	120	J14	R2	900
180.	I/O	96	126	146	X12	119	J15	R1	903
181.	I/O	97	127	147	U11	118	J11	P3	906
182.	I/O (D4)	98	128	148	V11	117	H13	P2	912
183.	I/O	99	129	149	W11	116	H14	P1	915
	VCC	100	130	150	X10	115	VCC*	VCC*	-
	GND	101	131	151	X11	114	GND*	GND*	-
184.	I/O (D3)	102	132	152	W10	113	H12	N2	924
185.	I/O ( $\bar{RS}$ )	103	133	153	V10	112	H11	N4	927
186.	I/O	104	134	154	T10	111	G14	N3	936
187.	I/O	105	135	155	U10	110	G15	M1	939
188.	I/O	-	136	156	X9	109	G13	M2	942
189.	I/O	-	137	157	W9	108	G12	M3	948

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
190.	I/O	-	-	-	X8	107	-	M4	951
191.	I/O	-	-	-	V9	106	-	L1	954
192.	I/O (D2)	106	138	159	W8	103	G11	J1	960
193.	I/O	107	139	160	X7	102	F15	K3	963
	VCC	-	-	161	X5	101	VCC*	VCC*	
194.	I/O	108	140	162	V8	99	F14	J2	966
195.	I/O	109	141	163	W7	98	F13	J3	972
196.	I/O	-	-	164	U8	97	G10	K4	975
197.	I/O	-	-	165	W6	96	E15	G1	978
	GND	110	142	166	X6	95	GND*	GND*	
198.	I/O	-	-	-	T8	94	-	H2	984
199.	I/O	-	-	-	V7	93	-	H3	987
200.	I/O	-	-	167	X4	92	E14	J4	990
201.	I/O	-	-	168	U7	91	F12	F1	996
202.	I/O	-	143	169	W5	90	E13	G2	999
203.	I/O	-	144	170	V6	89	D15	G3	1002
204.	I/O	111	145	171	T7	88	F11	F2	1008
205.	I/O	112	146	172	X3	87	D14	E2	1011
206.	I/O (D1)	113	147	173	U6	86	E12	F3	1014
207.	I/O (RCLK-BUSY/RDY)	114	148	174	V5	85	C15	G4	1020
208.	I/O	-	-	-	W4	84	-	D2	1023
209.	I/O	-	-	-	W3	83	-	F4	1032
210.	I/O	115	149	175	T6	82	D13	E3	1035
211.	I/O	116	150	176	U5	81	C14	C2	1038
212.	I/O (D0, DIN)	117	151	177	V4	80	F10	D3	1044
213.	I/O (DOUT)	118	152	178	X1	79	B15	E4	1047
	CCLK	119	153	179	V3	78	C13	C3	-
	VCC	120	154	180	W1	77	VCC*	VCC*	-
214.	I/O (TDO)	121	159	181	U4	76	A15	D4	0
	GND	122	160	182	X2	75	GND*	GND*	-
215.	I/O (A0, WS)	123	161	183	W2	74	A14	B3	9
216.	GCK4 (A1, I/O)	124	162	184	V2	73	B13	C4	15
217.	I/O	125	163	185	R5	72	E11	D5	18
218.	I/O	126	164	186	T4	71	C12	A3	21
219.	I/O (A2, CS1)	127	165	187	U3	70	A13	D6	27
220.	I/O (A3)	128	166	188	V1	69	B12	C6	30
221.	I/O	-	-	-	R4	68	-	B5	33
222.	I/O	-	-	-	P5	67	-	A4	39
223.	I/O	-	-	189	U2	66	F9	C7	42
224.	I/O	-	-	190	T3	65	D11	B6	45
225.	I/O	129	167	191	U1	64	A12	A6	51
226.	I/O	130	168	192	P4	63	C11	D8	54
227.	I/O	-	169	193	R3	62	B11	B7	57
228.	I/O	-	170	194	N5	61	E10	A7	63
229.	I/O	-	-	195	T2	60	-	D9	66
230.	I/O	-	-	-	R2	59	-	C9	69
	GND	131	171	196	T1	58	GND*	GND*	-
231.	I/O	132	172	197	N4	57	A11	B8	75
232.	I/O	133	173	198	P3	56	D10	D10	78
233.	I/O	-	-	199	P2	55	C10	C10	81
234.	I/O	-	-	200	N3	54	B10	B9	87
	VCC	-	-	201	R1	52	VCC*	VCC*	-

Pin	Description	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
235.	I/O	-	-	-	M5	51	-	B11	90
236.	I/O	-	-	-	P1	50	-	A11	93
237.	I/O (A4)	134	174	202	N1	47	A10	D12	99
238.	I/O (A5)	135	175	203	M3	46	D9	C12	102
239.	I/O	-	176	205	M2	45	C9	B12	105
240.	I/O	136	177	206	L5	44	B9	A12	111
241.	I/O	137	178	207	M1	43	A9	C13	114
242.	I/O	138	179	208	L4	42	E9	B13	117
243.	I/O (A6)	139	180	209	L3	41	C8	A13	126
244.	I/O (A7)	140	181	210	L2	40	B8	B14	129
	GND	141	182	211	L1	39	GND*	GND*	-

### Additional No Connect (N.C.) Connections for HQ208, HQ240, and HQ304 Packages

HQ208		HQ240	HQ304		
206	102	219	29	254	124
207	104	22	28	205	105
208	105	37	24	201	104
1	107	83	11	200	100
3	155	98	281	181	53
51	156	143	278	180	49
52	157	158	277	176	48
53	158	204	258	128	-
54	-	-	257	125	-

**Notes:** \* Pins labeled VCC\* are internally bonded to a VCC plane within the BG225 and BG352 packages. The external pins for the BG225 are: B2, D8, H15, R8, B14, R1, H1, and R15. The external pins for the BG352 are: A10, A17, B2, B25, D13, D19, D7, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC14, AC20, AC8, AE2, AE25, AF10, and AF17.

Pins labeled GND\* are internally bonded to a ground plane within the BG225 and BG352 packages. The external pins for the BG225 are: A1, D12, G7, G9, H6, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8. The external pins for the BG352 are: A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF13, AF19, AF2, AF22, AF25, AF26, AF5, AF8.

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

## Product Availability

	PINS	64	84	100	100	144	156	160	176	191									
	TYPE	Plast. VQFP	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	Ceram. PGA	Plast. PQFP	Plast. TQFP	Ceram. PGA	High-Perf. QFP	208	208	223	240	240	299	304	352
	CODE	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304	BG352
XC5202	-6	Cl	Cl	Cl	Cl	Cl													
	-5	C(I)	C(I)	C(I)	C(I)	C(I)													
	-4	C	C	C	C	C													
	-3	C	C	C	C	C													
XC5204	-6	Cl	Cl	Cl	Cl	Cl													
	-5	Cl	Cl	Cl	Cl	Cl													
	-4	C	C	C	C	C													
	-3	C	C	C	C	C													
XC5206	-6	Cl	Cl	Cl	Cl		Cl	Cl	Cl		Cl								
	-5	Cl	Cl	Cl	Cl		Cl	Cl	Cl		Cl								
	-4	C	C	C	C		C	C	C		C								
	-3	C	C	C	C		C	C	C		C								
XC5210	-6	Cl			Cl		Cl	Cl			Cl	Cl	Cl		Cl				
	-5	Cl			Cl		Cl	Cl			Cl	Cl	Cl		Cl				
	-4	C			C		C	C			C	C	C		C				
	-3	C			C		C	C			C	C	C		C				
XC5215	-6						Cl			Cl			Cl	Cl		Cl	Cl	Cl	
	-5						C(I)			C(I)			C(I)	C(I)		C(I)	C(I)	C(I)	
	-4						C			C			C	C					
	-3						C			C			C	C					

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C = Commercial  $T_J = 0^\circ\text{C}$  to  $+85^\circ\text{C}$ I= Industrial  $T_J = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ 

\* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

( ) Parentheses indicate future product plans

## User I/O Per Package

Device	Max I/O	Package Type																	
		VQ64	PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	HQ304	BG352
XC5202	84	52	65	81	81	84	84												
XC5204	124		65	81	81	117	124	124											
XC5206	148		65	81	81	117		133	148	148			148						
XC5210	196		65			117		133	149			164	196	196		196			
XC5215	244						133				164		196	197		244	244	244	

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## Ordering Information

Example: **XC5210-6PQ208C**

Device Type

Speed Grade



Temperature Range

Number of Pins

Package Type

**XC3000 Series Field Programmable Gate Arrays (XC3000A/L, XC3100A/L)**

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# XC3000 Series

## Field Programmable Gate Arrays

### (XC3000A/L, XC3100A/L)

November 20, 1997 (Version 3.0)

#### Product Description

## Features

- Complete line of four related Field Programmable Gate Array product families
  - XC3000A, XC3000L, XC3100A, XC3100L
- Ideal for a wide range of custom VLSI design tasks
  - Replaces TTL, MSI, and other PLD logic
  - Integrates complete sub-systems into a single package
  - Avoids the NRE, time delay, and risk of conventional masked gate arrays
- High-performance CMOS static memory technology
  - Guaranteed toggle rates of 70 to 370 MHz, logic delays from 9 to 1.5 ns
  - System clock speeds over 85 MHz
  - Low quiescent and active power consumption
- Flexible FPGA architecture
  - Compatible arrays ranging from 1,000 to 7,500 gate complexity
  - Extensive register, combinatorial, and I/O capabilities
  - High fan-out signal distribution, low-skew clock nets
  - Internal 3-state bus capabilities
  - TTL or CMOS input thresholds
  - On-chip crystal oscillator amplifier
- Unlimited reprogrammability
  - Easy design iteration
  - In-system logic changes
- Extensive packaging options
  - Over 20 different packages
  - Plastic and ceramic surface-mount and pin-grid-array packages
  - Thin and Very Thin Quad Flat Pack (TQFP and VQFP) options
- Ready for volume production
  - Standard, off-the-shelf product availability
  - 100% factory pre-tested devices
  - Excellent reliability record
- Complete XACTstep Development System

- Schematic capture, automatic place and route
- Logic and timing simulation
- Interactive design editor for design optimization
- Timing calculator
- Interfaces to popular design environments like Viewlogic, Cadence, Mentor Graphics, and others

## Additional XC3100A Features

- Ultra-high-speed FPGA family with six members
  - 50-85 MHz system clock rates
  - 190 to 370 MHz guaranteed flip-flop toggle rates
  - 1.55 to 4.1 ns logic delays
- High-end additional family member in the 22 X 22 CLB array-size XC3195A device
- 8 mA output sink current and 8 mA source current
- Maximum power-down and quiescent current is 5 mA
- 100% architecture and pin-out compatible with other XC3000 families
- Software and bitstream compatible with the XC3000, XC3000A, and XC3000L families
- PCI compliant (-2, -1, -09 speed grade in plastic quad flat pack (PQFP) packaging).

XC3100A combines the features of the XC3000A and XC3100 families:

- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

## Low-Voltage Versions Available

- Low-voltage devices function at 3.0 - 3.6 V
- XC3000L - Low-voltage versions of XC3000A devices
- XC3100L - Low-voltage versions of XC3100A devices

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020A, 3020L, 3120A	1,500	1,000 - 1,500	64	8 x 8	64	256	16	14,779
XC3030A, 3030L, 3130A	2,000	1,500 - 2,000	100	10 x 10	80	360	20	22,176
XC3042A, 3042L, 3142A, 3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3064A, 3064L, 3164A	4,500	3,500 - 4,500	224	16 x 14	120	688	32	46,064
XC3090A, 3090L, 3190A, 3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160
XC3195A	7,500	6,500 - 7,500	484	22 x 22	176	1,320	44	94,984

## Introduction

XC3000-Series Field Programmable Gate Arrays (FPGAs) provide a group of high-performance, high-density, digital integrated circuits. Their regular, extendable, flexible, user-programmable array architecture is composed of a configuration program store plus three types of configurable elements: a perimeter of I/O Blocks (IOBs), a core array of Configurable Logic Bocks (CLBs) and resources for interconnection. The general structure of an FPGA is shown in [Figure 2](#). The XACTstep development system provides schematic capture and auto place-and-route for design entry. Logic and timing simulation, and in-circuit emulation are available as design verification alternatives. The design editor is used for interactive design optimization, and to compile the data pattern that represents the configuration program.

The FPGA user logic functions and interconnections are determined by the configuration program data stored in internal static memory cells. The program can be loaded in any of several modes to accommodate various system requirements. The program data resides externally in an EEPROM, EPROM or ROM on the application circuit board, or on a floppy disk or hard disk. On-chip initialization logic provides for optional automatic loading of program data at power-up. The companion XC17XX Serial Configuration PROMs provide a very simple serial configuration program storage in a one-time programmable package.

The XC3000 Field Programmable Gate Array families provide a variety of logic capacities, package styles, temperature ranges and speed grades.

## XC3000 Series Overview

There are now four distinct family groupings within the XC3000 Series of FPGA devices, with emphasis on those listed below:

- XC3000A Family
- XC3000L Family
- XC3100A Family
- XC3100L Family

All four families share a common architecture, development software, design and programming methodology, and also common package pin-outs. An extensive Product Description covers these common aspects.

Detailed parametric information for the XC3000A, XC3000L, XC3100A, and XC3100L product families is then provided. (The XC3000 and XC3100 families are not recommended for new designs, and their individual product specifications are not included in this book.)

Here is a simple overview of those XC3000 products currently emphasized:

- **XC3000A Family** — The XC3000A is an enhanced version of the basic XC3000 family, featuring additional interconnect resources and other user-friendly enhancements. The ease-of-use of the XC3000A family makes it the obvious choice for all new designs that do not require the speed of the XC3100A or the 3-V operation of the XC3000L.
- **XC3000L Family** — The XC3000L is identical in architecture and features to the XC3000A family, but operates at a nominal supply voltage of 3.3 V. The XC3000L is the right solution for battery-operated and low-power applications.
- **XC3100A Family** — The XC3100A is a performance-optimized relative of the XC3000A family. While both families are bitstream and footprint compatible, the XC3100A family extends toggle rates to 370 MHz and in-system performance to over 80 MHz. The XC3100A family also offers one additional array size, the XC3195A. The XC3100A is best suited for designs that require the highest clock speed or the shortest net delays.
- **XC3100L Family** — The XC3100L is identical in architectures and features to the XC3100A family, but operates at a nominal supply voltage of 3.3V.

[Figure 1](#) illustrates the relationships between the families. Compared to the original XC3000 family, XC3000A offers additional functionality and, coming soon, increased speed. The XC3000L family offers the same additional functionality, but reduced speed due to its lower supply voltage of 3.3 V. The XC3100A family offers substantially higher speed and higher density with the XC3195A.

## New XC3000 Series Compared to Original XC3000 Family

For readers already familiar with the original XC3000 family of FPGAs, the major new features in the XC3000A, XC3000L, XC3100A, and XC3100L families are listed in this section.

All of these new families are upward-compatible extensions of the original XC3000 FPGA architecture. Any bitstream used to configure an XC3000 device will configure the corresponding XC3000A, XC3000L, XC3100A, or XC3100L device exactly the same way.

The XC3100A and XC3100L FPGA architectures are upward-compatible extensions of the XC3000A and XC3000L architectures. Any bitstream used to configure an XC3000A or XC3000L device will configure the corresponding XC3100A or XC3100L device exactly the same way.

## ***Improvements in the XC3000A and XC3000L Families***

The XC3000A and XC3000L families offer the following enhancements over the popular XC3000 family:

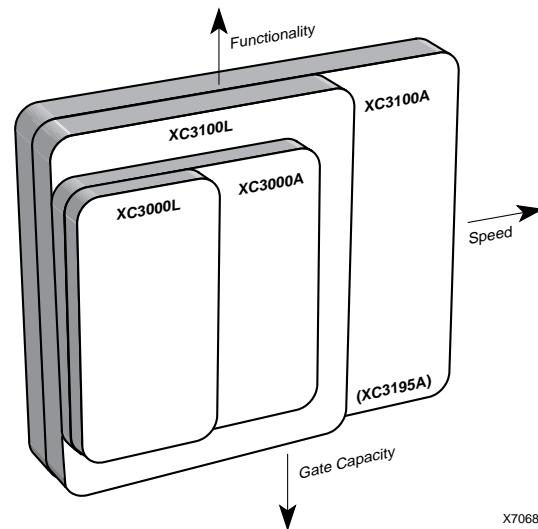
The XC3000A and XC3000L families has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A and XC3000L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

## ***Improvements in the XC3100A and XC3100L Families***

Based on a more advanced CMOS process, the XC3100A and XC3100L families are architecturally-identical, performance-optimized relatives of the XC3000A and XC3000A families. While all families are footprint compatible, the XC3100A family extends achievable system performance beyond 85 MHz.



**Figure 1: XC3000 FPGA Families**

X7068

## Detailed Functional Description

The perimeter of configurable Input/Output Blocks (IOBs) provides a programmable interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks, carrying logic signals among blocks, analogous to printed circuit board traces connecting MSI/SSI packages.

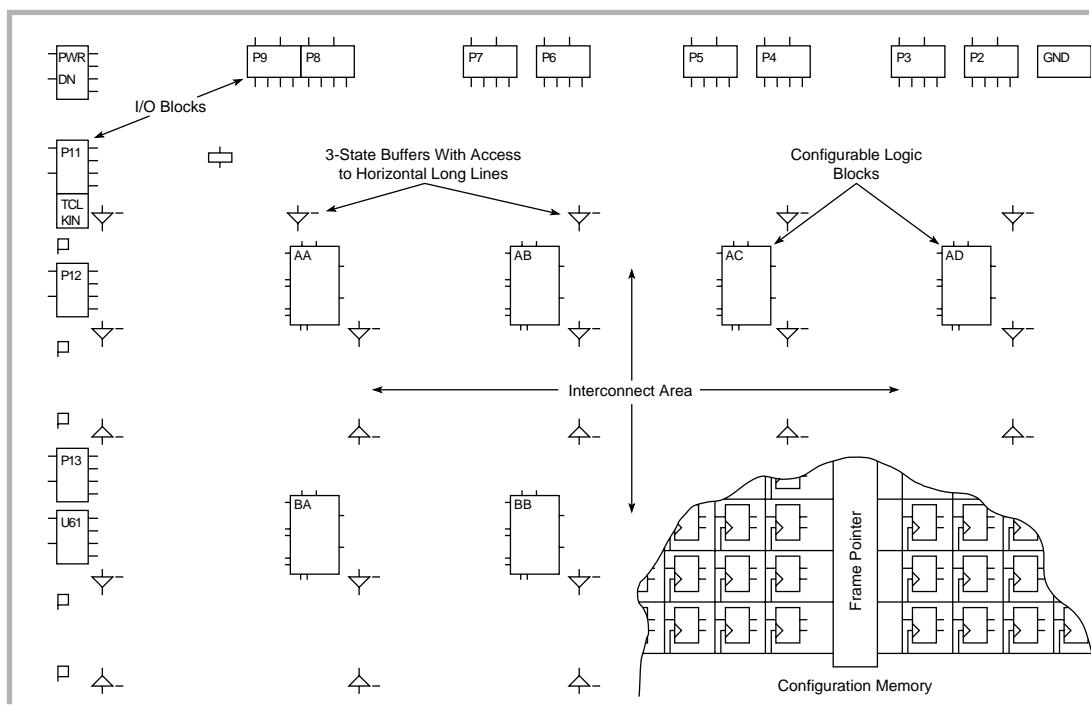
The block logic functions are implemented by programmed look-up tables. Functional options are implemented by program-controlled multiplexers. Interconnecting networks between blocks are implemented with metal segments joined by program-controlled pass transistors.

These FPGA functions are established by a configuration program which is loaded into an internal, distributed array of configuration memory cells. The configuration program is loaded into the device at power-up and may be reloaded on command. The FPGA includes logic and control signals to implement automatic or passive configuration. Program

data may be either bit serial or byte parallel. The XACT<sup>step</sup> development system generates the configuration program bitstream used to configure the device. The memory loading process is independent of the user logic functions.

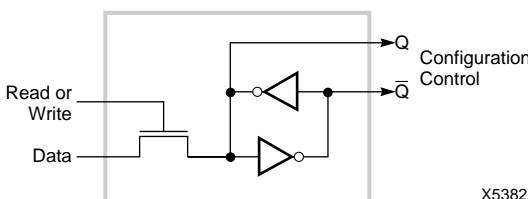
## Configuration Memory

The static memory cell used for the configuration memory in the Field Programmable Gate Array has been designed specifically for high reliability and noise immunity. Integrity of the device configuration memory based on this design is assured even under adverse conditions. As shown in **Figure 3**, the basic memory cell consists of two CMOS inverters plus a pass transistor used for writing and reading cell data. The cell is only written during configuration and only read during readback. During normal operation, the cell provides continuous control and the pass transistor is off and does not affect cell stability. This is quite different from the operation of conventional memory devices, in which the cells are frequently read and rewritten.



**Figure 2: Field Programmable Gate Array Structure.**

It consists of a perimeter of programmable I/O blocks, a core of configurable logic blocks and their interconnect resources. These are all controlled by the distributed array of configuration program memory cells.



**Figure 3: Static Configuration Memory Cell.**

It is loaded with one bit of configuration program and controls one program selection in the Field Programmable Gate Array.

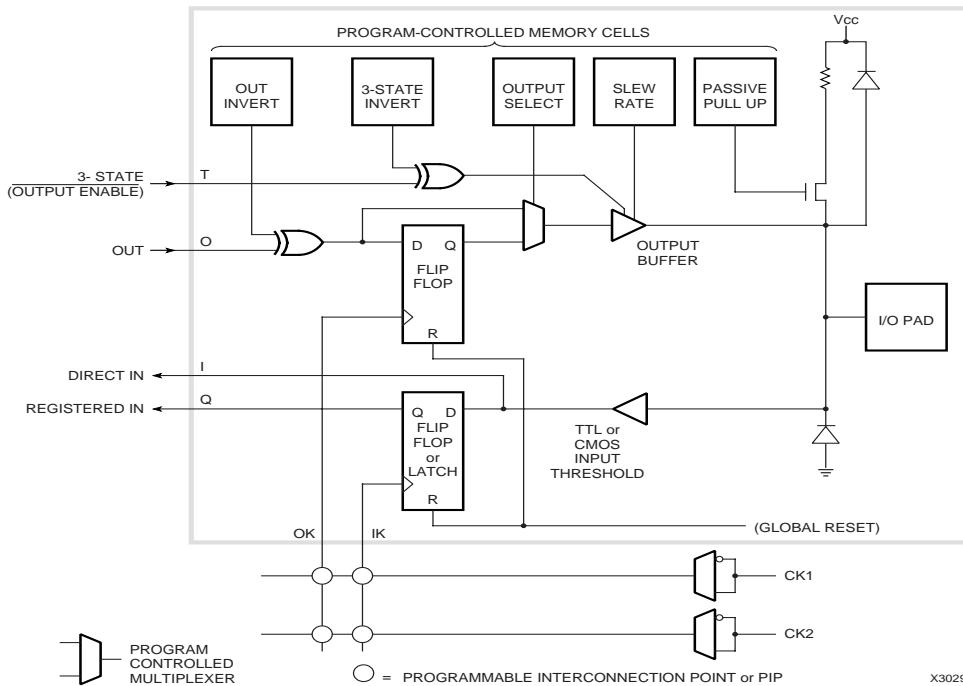
The memory cell outputs  $Q$  and  $\bar{Q}$  use ground and  $V_{CC}$  levels and provide continuous, direct control. The additional capacitive load together with the absence of address decoding and sense amplifiers provide high stability to the cell. Due to the structure of the configuration memory cells, they are not affected by extreme power-supply excursions or very high levels of alpha particle radiation. In reliability

testing, no soft errors have been observed even in the presence of very high doses of alpha radiation.

The method of loading the configuration data is selectable. Two methods use serial data, while three use byte-wide data. The internal configuration logic utilizes framing information, embedded in the program data by the XACTstep development system, to direct memory-cell loading. The serial-data framing and length-count preamble provide programming compatibility for mixes of various FPGA device devices in a synchronous, serial, daisy-chain fashion.

## I/O Block

Each user-configurable IOB shown in Figure 4, provides an interface between the external package pin of the device and the internal user logic. Each IOB includes both registered and direct input paths. Each IOB provides a programmable 3-state output buffer, which may be driven by a registered or direct output signal. Configuration options allow each IOB an inversion, a controlled slew rate and a high impedance pull-up. Each input circuit also provides input clamping diodes to provide electrostatic protection, and circuits to inhibit latch-up produced by input currents.



**Figure 4: Input/Output Block.**

Each IOB includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active Low Latch Enable (Latch transparent) signal and vice versa. Passive pull-up can only be enabled on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

The input-buffer portion of each IOB provides threshold detection to translate external signals applied to the package pin to internal logic levels. The global input-buffer threshold of the IOBs can be programmed to be compatible with either TTL or CMOS levels. The buffered input signal drives the data input of a storage element, which may be configured as either a flip-flop or a latch. The clocking polarity (rising/falling edge-triggered flip-flop, High/Low transparent latch) is programmable for each of the two clock lines on each of the four die edges. Note that a clock line driving a *rising* edge-triggered flip-flop makes any latch driven by the same line on the same edge Low-level transparent and vice versa (*falling* edge, *High* transparent). All Xilinx primitives in the supported schematic-entry packages, however, are positive edge-triggered flip-flops or High transparent latches. When one clock line must drive flip-flops as well as latches, it is necessary to compensate for the difference in clocking polarities with an additional inverter either in the flip-flop clock input or the latch-enable input. I/O storage elements are reset during configuration or by the active-Low chip RESET input. Both direct input (from IOB pin I) and registered input (from IOB pin Q) signals are available for interconnect.

For reliable operation, inputs should have transition times of less than 100 ns and should not be left floating. Floating CMOS input-pin circuits might be at threshold and produce oscillations. This can produce additional power dissipation and system noise. A typical hysteresis of about 300 mV reduces sensitivity to input noise. Each user IOB includes a programmable high-impedance pull-up resistor, which may be selected by the program to provide a constant High for otherwise undriven package pins. Although the Field Programmable Gate Array provides circuitry to provide input protection for electrostatic discharge, normal CMOS handling precautions should be observed.

Flip-flop loop delays for the IOB and logic-block flip-flops are short, providing good performance under asynchronous clock and data conditions. Short loop delays minimize the probability of a metastable condition that can result from assertion of the clock during data transitions. Because of the short-loop-delay characteristic in the Field Programmable Gate Array, the IOB flip-flops can be used to synchronize external signals applied to the device. Once synchronized in the IOB, the signals can be used internally without further consideration of their clock relative timing, except as it applies to the internal logic and routing-path delays.

IOB output buffers provide CMOS-compatible 4-mA source-or-sink drive for high fan-out CMOS or TTL-compatible signal levels (8 mA in the XC3100A family). The network driving IOB pin O becomes the registered or direct data source for the output buffer. The 3-state control signal (IOB) pin T can control output activity. An open-drain output may be obtained by using the same signal for driving the

output and 3-state signal nets so that the buffer output is enabled only for a Low.

Configuration program bits for each IOB control features such as optional output register, logic signal inversion, and 3-state and slew-rate control of the output.

The program-controlled memory cells of [Figure 4](#) control the following options.

- Logic inversion of the output is controlled by one configuration program bit per IOB.
- Logic 3-state control of each IOB output buffer is determined by the states of configuration program bits that turn the buffer on, or off, or select the output buffer 3-state control interconnection (IOB pin T). When this IOB output control signal is High, a logic one, the buffer is disabled and the package pin is high impedance. When this IOB output control signal is Low, a logic zero, the buffer is enabled and the package pin is active. Inversion of the buffer 3-state control-logic sense (output enable) is controlled by an additional configuration program bit.
- Direct or registered output is selectable for each IOB. The register uses a positive-edge, clocked flip-flop. The clock source may be supplied (IOB pin OK) by either of two metal lines available along each die edge. Each of these lines is driven by an invertible buffer.
- Increased output transition speed can be selected to improve critical timing. Slower transitions reduce capacitive-load peak currents of non-critical outputs and minimize system noise.
- An internal high-impedance pull-up resistor (active by default) prevents unconnected inputs from floating.

Unlike the original XC3000 series, the XC3000A, XC3000L, XC3100A, and XC3100L families include the Soft Startup feature. When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature avoids potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is determined by the individual configuration option.

### **Summary of I/O Options**

- Inputs
  - Direct
  - Flip-flop/latch
  - CMOS/TTL threshold (chip inputs)
  - Pull-up resistor/open circuit
- Outputs
  - Direct/registered
  - Inverted/not
  - 3-state/on/off
  - Full speed/slew limited
  - 3-state/output enable (inverse)

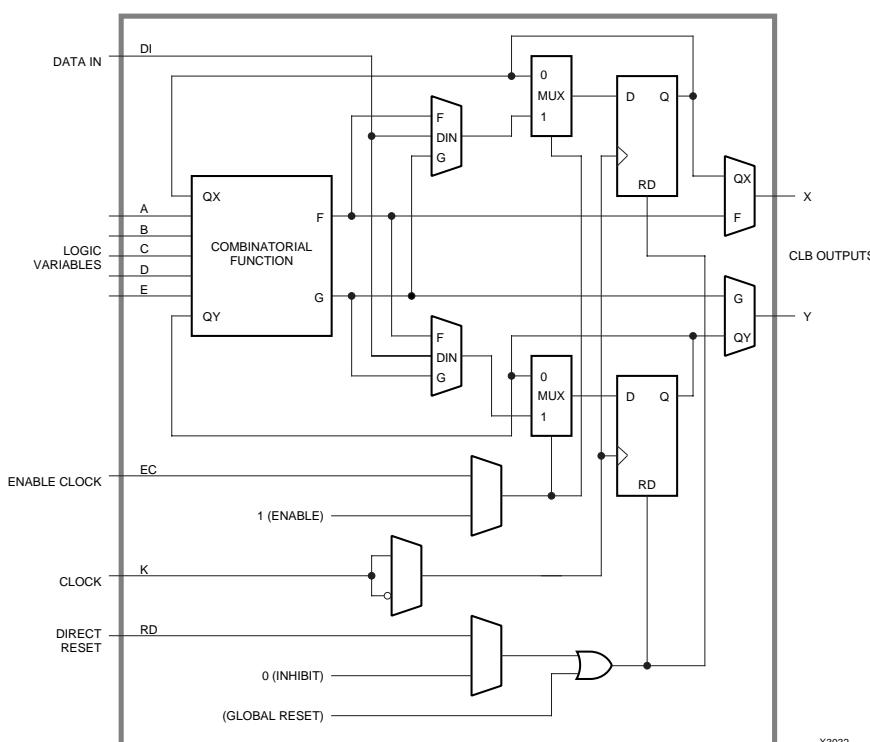
## Configurable Logic Block

The array of CLBs provides the functional elements from which the user's logic is constructed. The logic blocks are arranged in a matrix within the perimeter of IOBs. For example, the XC3020A has 64 such blocks arranged in 8 rows and 8 columns. The XACTstep development system is used to compile the configuration data which is to be loaded into the internal configuration memory to define the operation and interconnection of each block. User definition of CLBs and their interconnecting networks may be done by automatic translation from a schematic-capture logic diagram or optionally by installing library or user macros.

Each CLB has a combinatorial logic section, two flip-flops, and an internal control section. See **Figure 5**. There are: five logic inputs (A, B, C, D and E); a common clock input (K); an asynchronous direct RESET input (RD); and an enable clock (EC). All may be driven from the interconnect

resources adjacent to the blocks. Each CLB also has two outputs (X and Y) which may drive interconnect networks.

Data input for either flip-flop within a CLB is supplied from the function F or G outputs of the combinatorial logic, or the block input, DI. Both flip-flops in each CLB share the asynchronous RD which, when enabled and High, is dominant over clocked inputs. All flip-flops are reset by the active-Low chip input, RESET, or during the configuration process. The flip-flops share the enable clock (EC) which, when Low, recirculates the flip-flops' present states and inhibits response to the data-in or combinatorial function inputs on a CLB. The user may enable these control inputs and select their sources. The user may also select the clock net input (K), as well as its active sense within each CLB. This programmable inversion eliminates the need to route both phases of a clock signal throughout the device. Flexible routing allows use of common or individual CLB clocking.



X3032

**Figure 5: Configurable Logic Block.**

Each CLB includes a combinatorial logic section, two flip-flops and a program memory controlled multiplexer selection of function. It has the following:

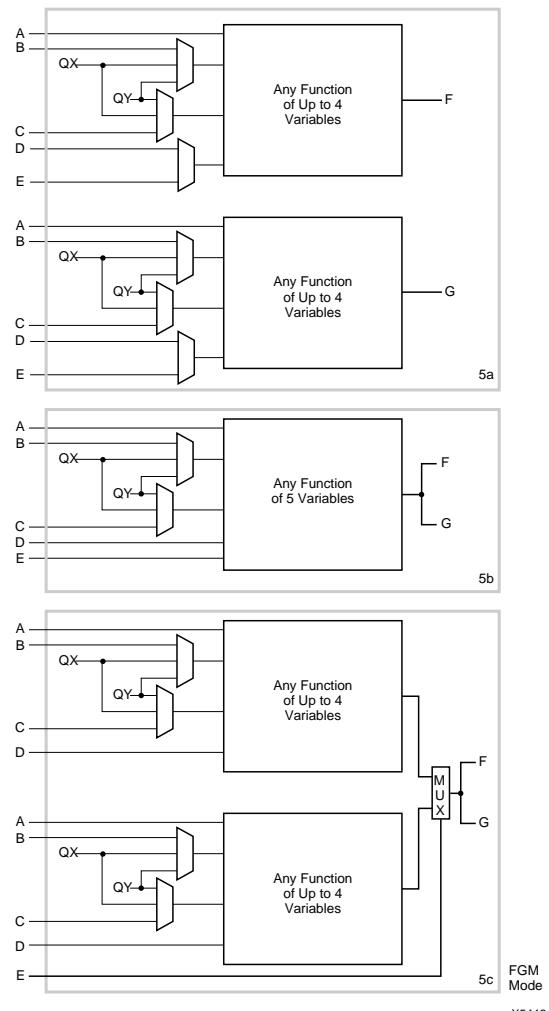
- five logic variable inputs A, B, C, D, and E
- a direct data in DI
- an enable clock EC
- a clock (invertible) K
- an asynchronous direct RESET RD
- two outputs X and Y

The combinatorial-logic portion of the CLB uses a 32 by 1 look-up table to implement Boolean functions. Variables selected from the five logic inputs and two internal block flip-flops are used as table address inputs. The combinatorial propagation delay through the network is independent of the logic function generated and is spike free for single input variable changes. This technique can generate two independent logic functions of up to four variables each as shown in Figure 6a, or a single function of five variables as shown in Figure 6b, or some functions of seven variables as shown in Figure 6c. Figure 7 shows a modulo-8 binary counter with parallel enable. It uses one CLB of each type. The partial functions of six or seven variables are implemented using the input variable (E) to dynamically select between two functions of four different variables. For the two functions of four variables each, the independent results (F and G) may be used as data inputs to either flip-flop or either logic block output. For the single function of five variables and merged functions of six or seven variables, the F and G outputs are identical. Symmetry of the F and G functions and the flip-flops allows the interchange of CLB outputs to optimize routing efficiencies of the networks interconnecting the CLBs and IOBs.

## Programmable Interconnect

Programmable-interconnection resources in the Field Programmable Gate Array provide routing paths to connect inputs and outputs of the IOBs and CLBs into logic networks. Interconnections between blocks are composed of a two-layer grid of metal segments. Specially designed pass transistors, each controlled by a configuration bit, form programmable interconnect points (PIPs) and switching matrices used to implement the necessary connections between selected metal segments and block pins. Figure 8 is an example of a routed net. The XACTstep development system provides automatic routing of these interconnections. Interactive routing (Editnet) is also available for design optimization. The inputs of the CLBs or IOBs are multiplexers which can be programmed to select an input network from the adjacent interconnect segments. ***Since the switch connections to block inputs are unidirectional, as are block outputs, they are usable only for block input connection and not for routing.*** Figure 9 illustrates routing access to logic block input variables, control inputs and block outputs. Three types of metal resources are provided to accommodate various network interconnect requirements.

- General Purpose Interconnect
- Direct Connection
- Longlines (multiplexed busses and wide AND gates

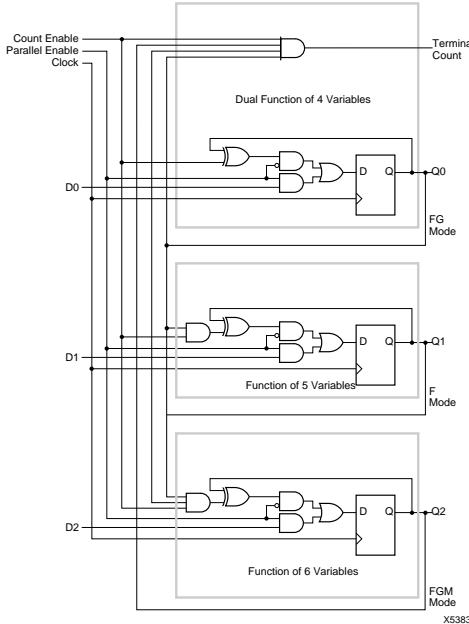


**Figure 6: Combinational Logic Options**

**6a.** Combinatorial Logic Option FG generates two functions of four variables each. One variable, A, must be common to both functions. The second and third variable can be any choice of B, C, QX and QY. The fourth variable can be any choice of D or E.

**6b.** Combinatorial Logic Option F generates any function of five variables: A, D, E and two choices out of B, C, QX, QY.

**6c.** Combinatorial Logic Option FGM allows variable E to select between two functions of four variables: Both have common inputs A and D and any choice out of B, C, QX and QY for the remaining two variables. Option 3 can then implement some functions of six or seven variables.



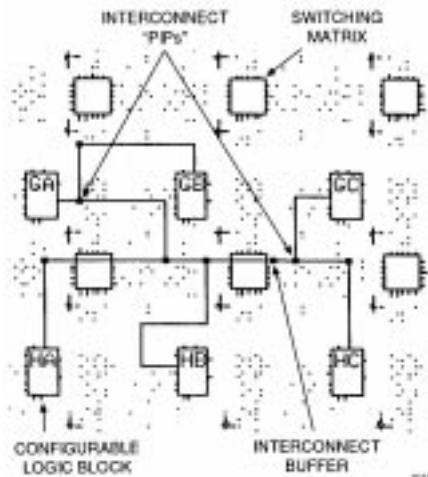
**Figure 7: C8BCP Macro.**

The C8BCP macro (modulo-8 binary counter with parallel enable and clock enable) uses one combinatorial logic block of each option.

### General Purpose Interconnect

General purpose interconnect, as shown in [Figure 10](#), consists of a grid of five horizontal and five vertical metal segments located between the rows and columns of logic and IOBs. Each segment is the height or width of a logic block. Switching matrices join the ends of these segments and allow programmed interconnections between the metal grid segments of adjoining rows and columns. The switches of an unprogrammed device are all non-conducting. The connections through the switch matrix may be established by the automatic routing or by using Editnet to select the desired pairs of matrix pins to be connected or disconnected. The legitimate switching matrix combinations for each pin are indicated in [Figure 11](#) and may be highlighted by the use of the Show-Matrix command in the XACT Design Editor.

Special buffers within the general interconnect areas provide periodic signal isolation and restoration for improved performance of lengthy nets. The interconnect buffers are available to propagate signals in either direction on a given general interconnect segment. These bidirectional (bidi) buffers are found adjacent to the switching matrices, above

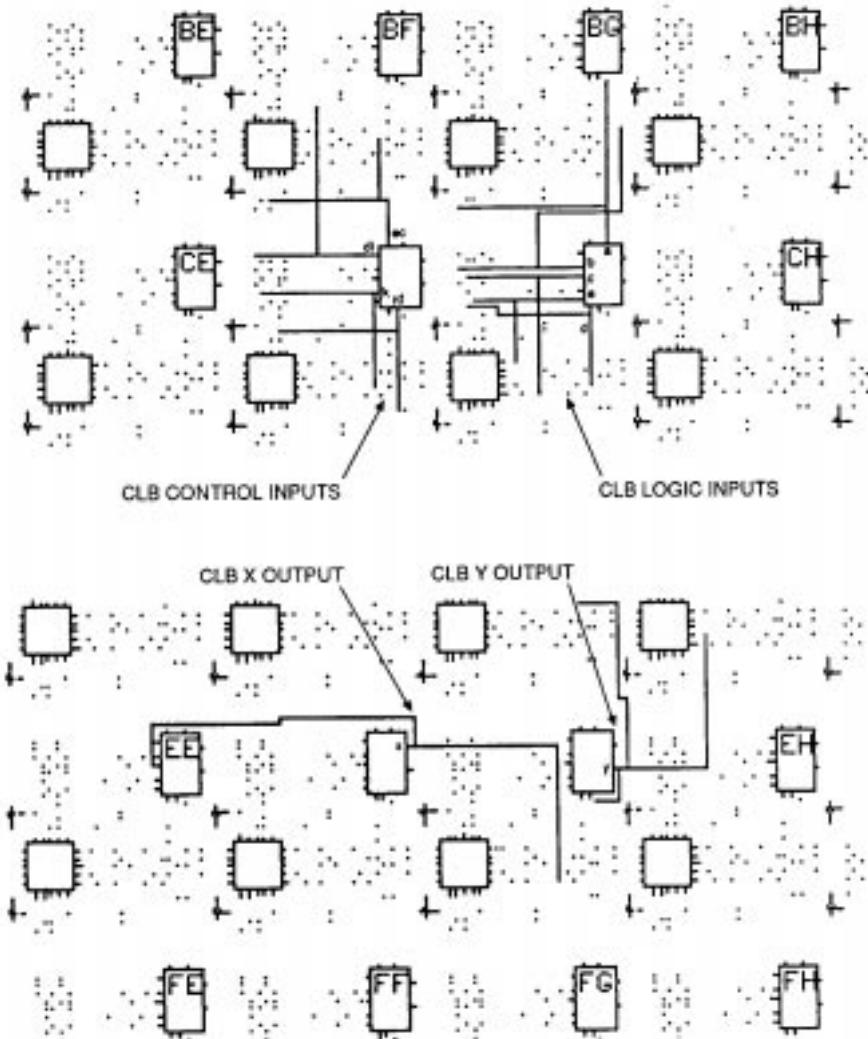


**Figure 8: An XACT Design Editor view of routing resources used to form a typical interconnection network from CLB GA.**

and to the right and may be highlighted by the use of the Show BIDI command in the XACT Design Editor. The other PIPs adjacent to the matrices are accessed to or from Long-lines. The development system automatically defines the buffer direction based on the location of the interconnection network source. The delay calculator of the XACTstep development system automatically calculates and displays the block, interconnect and buffer delays for any paths selected. Generation of the simulation netlist with a worst-case delay model is provided by an XACT option.

### Direct Interconnect

Direct interconnect, shown in [Figure 12](#), provides the most efficient implementation of networks between adjacent CLBs or I/O Blocks. Signals routed from block to block using the direct interconnect exhibit minimum interconnect propagation and use no general interconnect resources. For each CLB, the X output may be connected directly to the B input of the CLB immediately to its right and to the C input of the CLB to its left. The Y output can use direct interconnect to drive the D input of the block immediately above and the A input of the block below. Direct interconnect should be used to maximize the speed of high-performance portions of logic. Where logic blocks are adjacent to IOBs, direct connect is provided alternately to the IOB inputs (I) and outputs (O) on all four edges of the die. The right edge provides additional direct connects from CLB outputs to adjacent IOBs. Direct interconnections of IOBs with CLBs are shown in [Figure 13](#).



**Figure 9: XACT Design Editor** Locations of interconnect access, CLB control inputs, logic inputs and outputs. The dot pattern represents the available programmable interconnection points (PIPs).

Some of the interconnect PIPs are directional. This is indicated on the XACT Design Editor status line:

ND is a nondirectional interconnection.

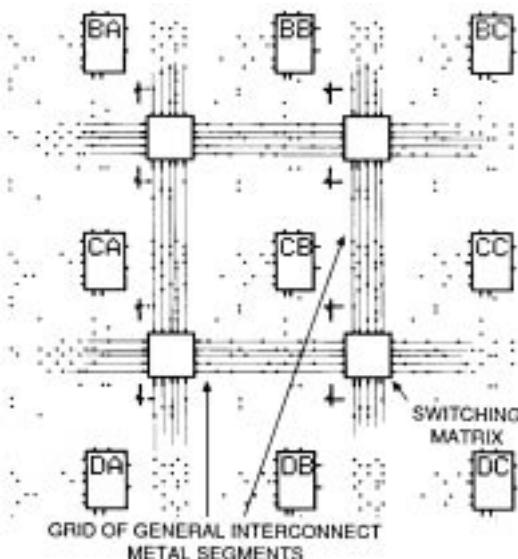
D:H->V is a PIP that drives from a horizontal to a vertical line.

D:V->H is a PIP that drives from a vertical to a horizontal line.

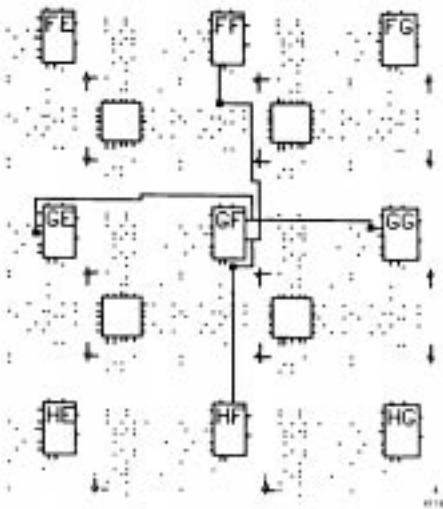
D:C->T is a "T" PIP that drives from a cross of a T to the tail.

D:CW is a corner PIP that drives in the clockwise direction.

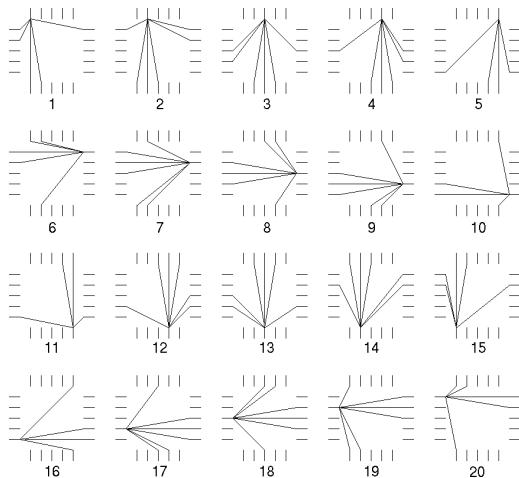
P0 indicates the PIP is non-conducting, P1 is on.



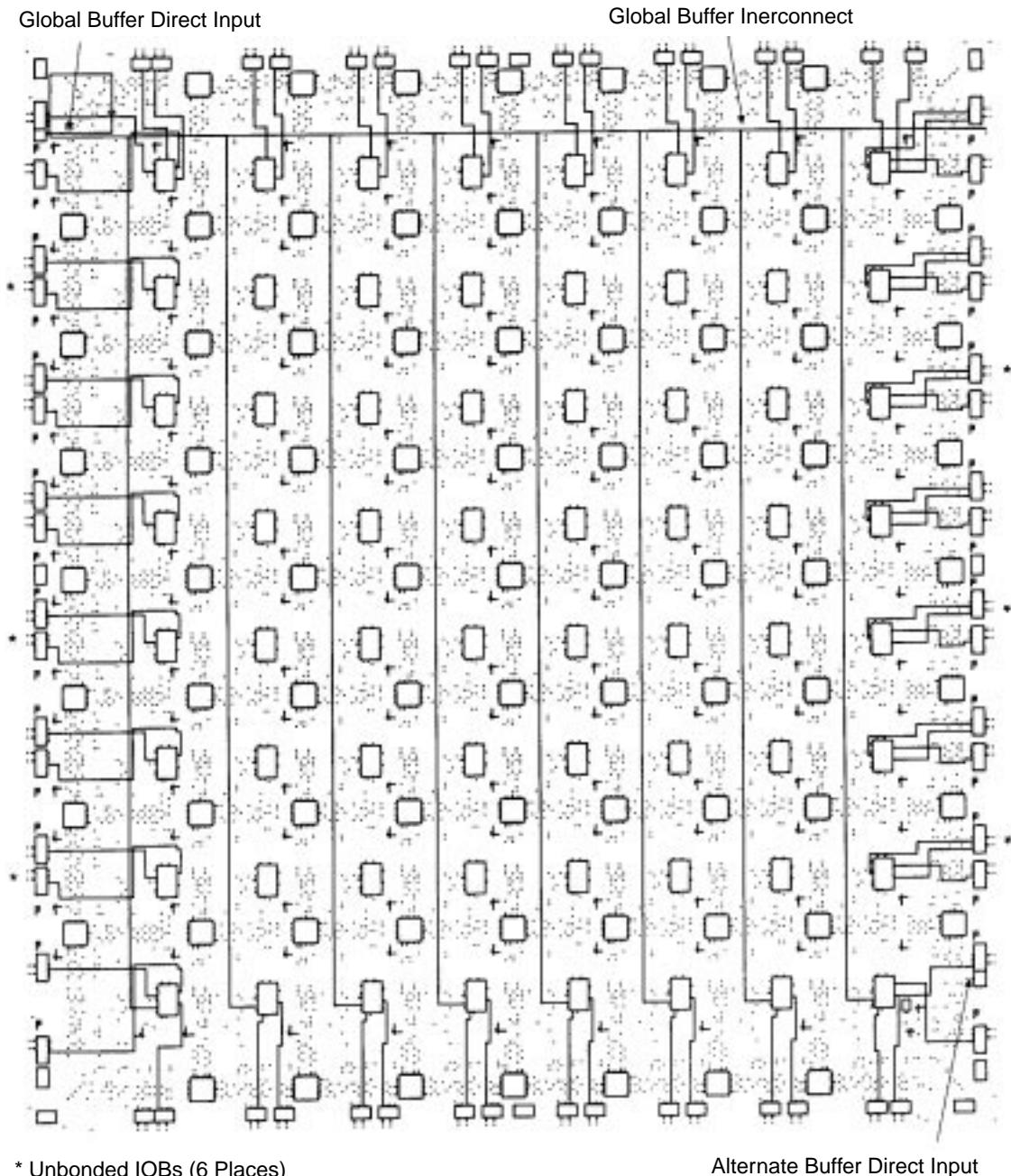
**Figure 10: FPGA General-Purpose Interconnect.**  
Composed of a grid of metal segments that may be interconnected through switch matrices to form networks for CLB and IOB inputs and outputs.



**Figure 12: CLB X and Y Outputs.**  
The X and Y outputs of each CLB have single contact, direct access to inputs of adjacent CLBs



**Figure 11: Switch Matrix Interconnection Options for Each Pin.**  
Switch matrices on the edges are different. Use Show Matrix menu option in the XACT Design Editor.



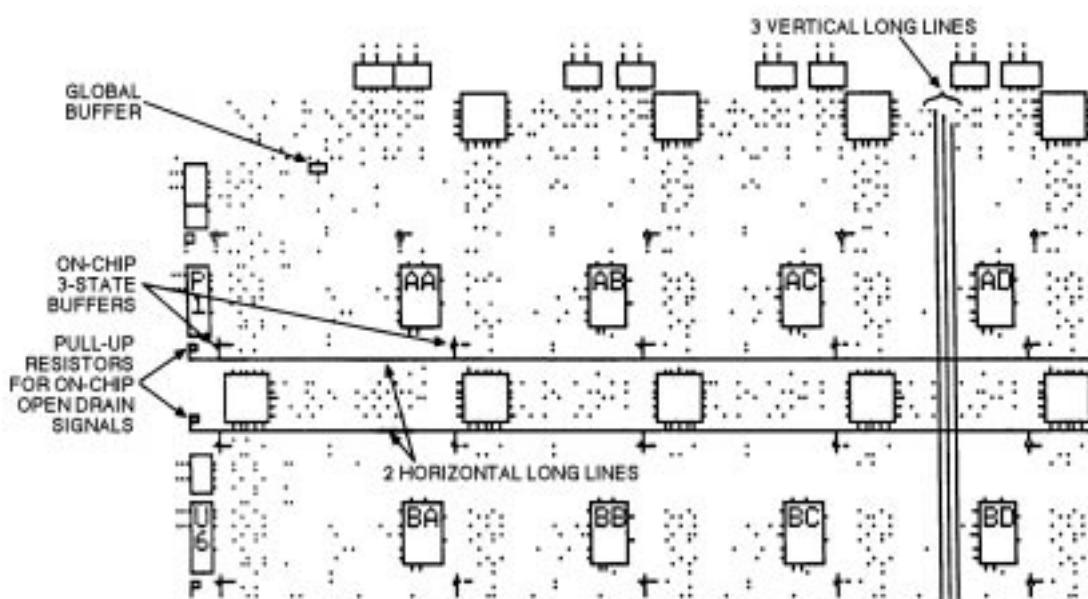
**Figure 13: XC3020A Die-Edge IOBs.** The XC3020A die-edge IOBs are provided with direct access to adjacent CLBs.

## Longlines

The Longlines bypass the switch matrices and are intended primarily for signals that must travel a long distance, or must have minimum skew among multiple destinations. Longlines, shown in [Figure 14](#), run vertically and horizontally the height or width of the interconnect area. Each interconnection column has three vertical Longlines, and each interconnection row has two horizontal Longlines. Two additional Longlines are located adjacent to the outer sets of switching matrices. In devices larger than the XC3020A/L and XC3120A FPGAs, two vertical Longlines in each col-

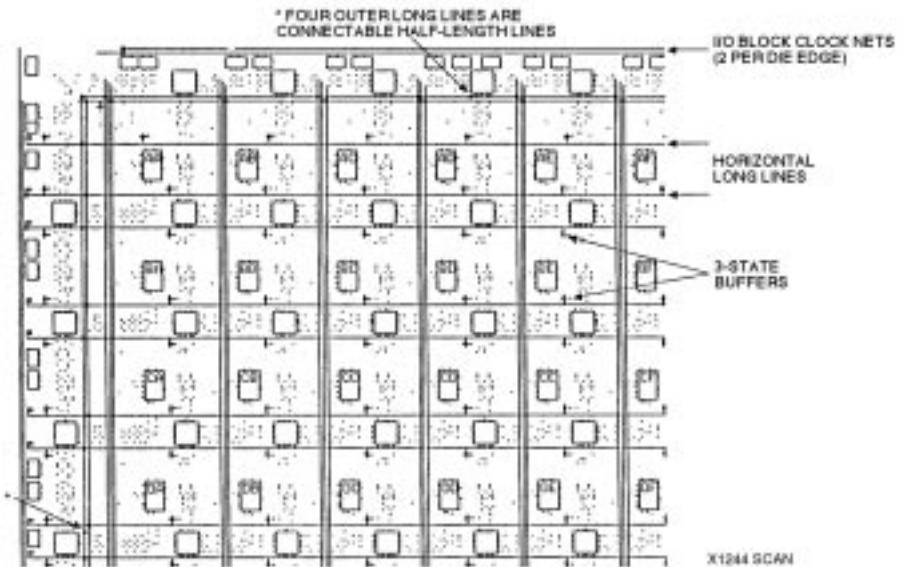
umn are connectable half-length lines. On the XC3020A/L and XC3120A FPGAs, only the outer Longlines are connectable half-length lines.

Longlines can be driven by a logic block or IOB output on a column-by-column basis. This capability provides a common low skew control or clock line within each column of logic blocks. Interconnections of these Longlines are shown in [Figure 15](#). Isolation buffers are provided at each input to a Longline and are enabled automatically by the development system when a connection is made.

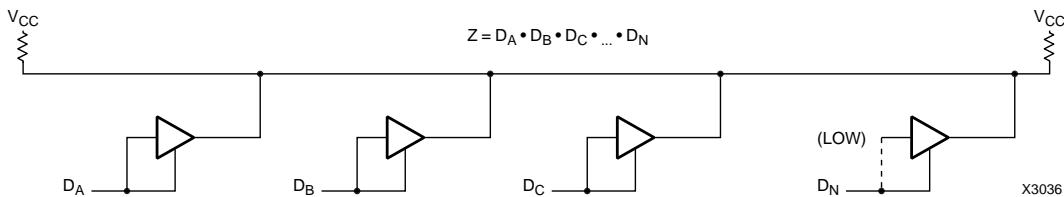


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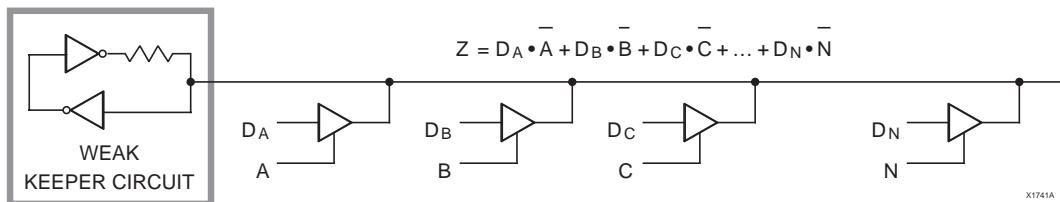
**Figure 14: Horizontal and Vertical Longlines.** These Longlines provide high fan-out, low-skew signal distribution in each row and column. The global buffer in the upper left die corner drives a common line throughout the FPGA.



**Figure 15: Programmable Interconnection of Longlines.** This is provided at the edges of the routing area. Three-state buffers allow the use of horizontal Longlines to form on-chip wired AND and multiplexed buses. The left two non-clock vertical Longlines per column (except XC3020A) and the outer perimeter Longlines may be programmed as connectable half-length lines.



**Figure 16: 3-State Buffers Implement a Wired-AND Function.** When all the buffer 3-state lines are High, (high impedance), the pull-up resistor(s) provide the High output. The buffer inputs are driven by the control signals or a Low.



**Figure 17: 3-State Buffers Implement a Multiplexer.** The selection is accomplished by the buffer 3-state signal.

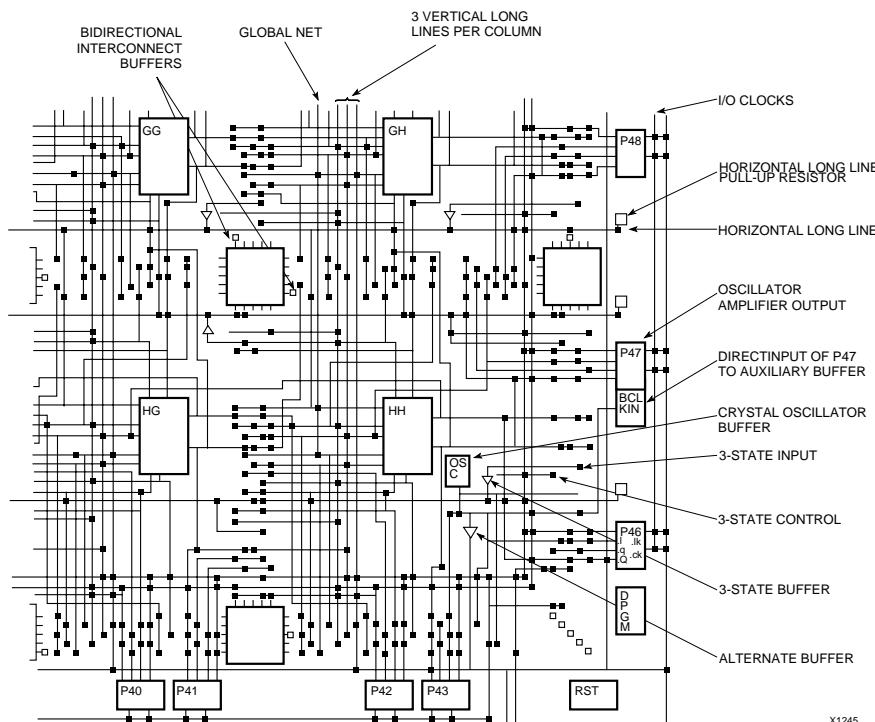
A buffer in the upper left corner of the FPGA chip drives a global net which is available to all K inputs of logic blocks. Using the global buffer for a clock signal provides a skew-free, high fan-out, synchronized clock for use at any or all of the IOBs and CLBs. Configuration bits for the K input to each logic block can select this global line or another routing resource as the clock source for its flip-flops. This net may also be programmed to drive the die edge clock lines for IOB use. An enhanced speed, CMOS threshold, direct access to this buffer is available at the second pad from the top of the left die edge.

A buffer in the lower right corner of the array drives a horizontal Longline that can drive programmed connections to a vertical Longline in each interconnection column. This alternate buffer also has low skew and high fan-out. The network formed by this alternate buffer's Longlines can be selected to drive the K inputs of the CLBs. CMOS threshold, high speed access to this buffer is available from the third pad from the bottom of the right die edge.

### Internal Busses

A pair of 3-state buffers, located adjacent to each CLB, permits logic to drive the horizontal Longlines. Logic operation

of the 3-state buffer controls allows them to implement wide multiplexing functions. Any 3-state buffer input can be selected as drive for the horizontal long-line bus by applying a Low logic level on its 3-state control line. See [Figure 16](#). The user is required to avoid contention which can result from multiple drivers with opposing logic levels. Control of the 3-state input by the same signal that drives the buffer input, creates an open-drain wired-AND function. A logic High on both buffer inputs creates a high impedance, which represents no contention. A logic Low enables the buffer to drive the Longline Low. See [Figure 17](#). Pull-up resistors are available at each end of the Longline to provide a High output when all connected buffers are non-conducting. This forms fast, wide gating functions. When data drives the inputs, and separate signals drive the 3-state control lines, these buffers form multiplexers (3-state buses). In this case, care must be used to prevent contention through multiple active buffers of conflicting levels on a common line. Each horizontal Longline is also driven by a weak keeper circuit that prevents undefined floating levels by maintaining the previous logic level when the line is not driven by an active buffer or a pull-up resistor. [Figure 18](#) shows 3-state buffers, Longlines and pull-up resistors.



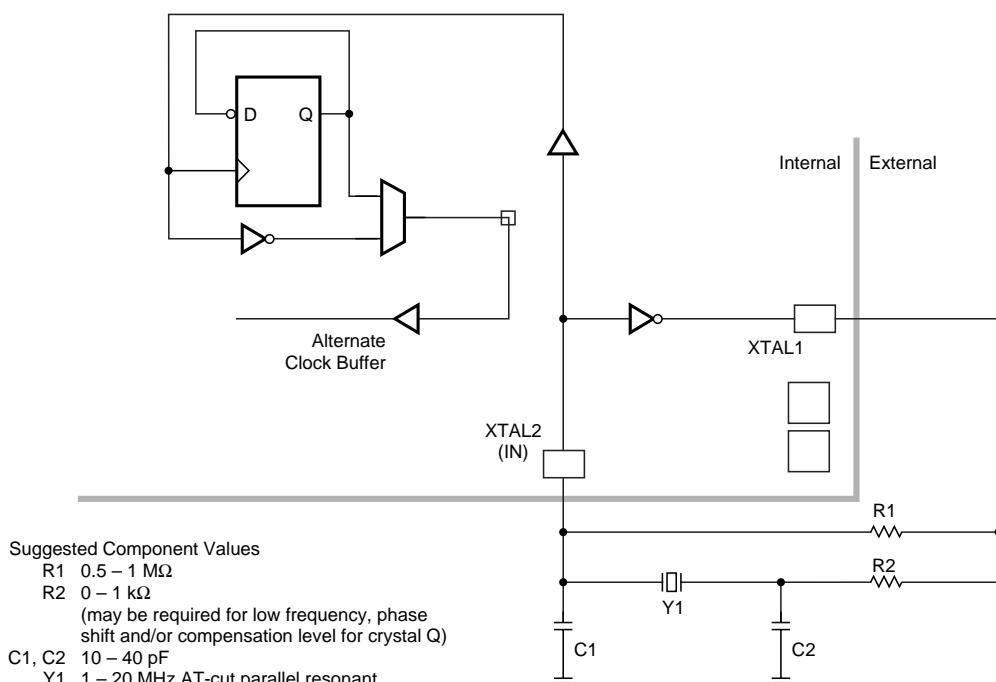
**Figure 18:** XACT Design Editor.

An extra large view of possible interconnections in the lower right corner of the XC3020A.

## Crystal Oscillator

Figure 18 also shows the location of an internal high speed inverting amplifier that may be used to implement an on-chip crystal oscillator. It is associated with the auxiliary buffer in the lower right corner of the die. When the oscillator is configured by MakeBits and connected as a signal source, two special user IOBs are also configured to connect the oscillator amplifier with external crystal oscillator components as shown in Figure 19. A divide by two option is available to assure symmetry. The oscillator circuit becomes active early in the configuration process to allow the oscillator to stabilize. Actual internal connection is delayed until completion of configuration. In Figure 19 the feedback resistor R1, between the output and input, biases the amplifier at threshold. The inversion of the amplifier, together with the R-C networks and an AT-cut series resonant crystal, produce the 360-degree phase shift of the

Pierce oscillator. A series resistor R2 may be included to add to the amplifier output impedance when needed for phase-shift control, crystal resistance matching, or to limit the amplifier input swing to control clipping at large amplitudes. Excess feedback voltage may be corrected by the ratio of C2/C1. The amplifier is designed to be used from 1 MHz to about one-half the specified CLB toggle frequency. Use at frequencies below 1 MHz may require individual characterization with respect to a series resistance. Crystal oscillators above 20 MHz generally require a crystal which operates in a third overtone mode, where the fundamental frequency must be suppressed by an inductor across C2, turning this parallel resonant circuit to double the fundamental crystal frequency, i.e., 2/3 of the desired third harmonic frequency network. When the oscillator inverter is not used, these IOBs and their package pins are available for general user I/O.



	44 PIN	68 PIN	84 PIN		100 PIN		132 PIN	160 PIN	164 PIN	175 PIN	176 PIN	208 PIN
	PLCC	PLCC	PLCC	PGA	CQFP	PQFP	PGA	PQFP	CQFP	PGA	TQFP	PQFP
XTAL 1 (OUT)	30	47	57	J11	67	82	P13	82	105	T14	91	110
XTAL 2 (IN)	26	43	53	L11	61	76	M13	76	99	P15	85	100

X7064

**Figure 19: Crystal Oscillator Inverter.** When activated in the MakeBits program and by selecting an output network for its buffer, the crystal oscillator inverter uses two unconfigured package pins and external components to implement an oscillator. An optional divide-by-two mode is available to assure symmetry.

# Configuration

## Initialization Phase

An internal power-on-reset circuit is triggered when power is applied. When  $V_{CC}$  reaches the voltage at which portions of the FPGA device begin to operate (nominally 2.5 to 3 V), the programmable I/O output buffers are 3-stated and a high-impedance pull-up resistor is provided for the user I/O pins. A time-out delay is initiated to allow the power supply voltage to stabilize. During this time the power-down mode is inhibited. The Initialization state time-out (about 11 to 33 ms) is determined by a 14-bit counter driven by a self-generated internal timer. This nominal 1-MHz timer is subject to variations with process, temperature and power supply. As shown in [Table 1](#), five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

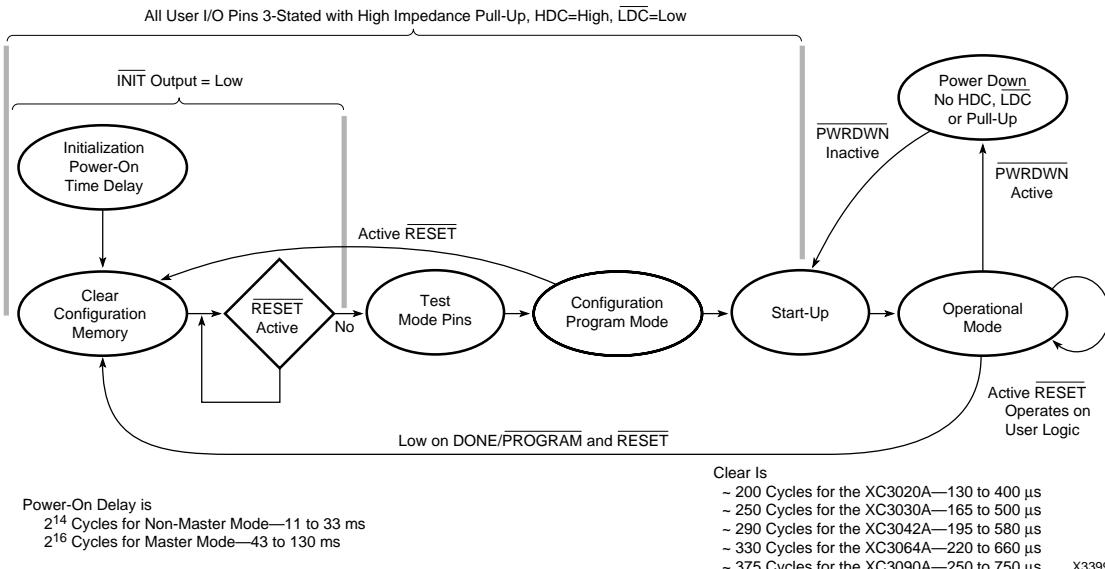
**Table 1: Configuration Mode Choices**

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

In Master configuration modes, the device becomes the source of the Configuration Clock (CCLK). The beginning of configuration of devices using Peripheral or Slave modes must be delayed long enough for their initialization to be completed. An FPGA with mode lines selecting a Master configuration mode extends its initialization state using four times the delay (43 to 130 ms) to assure that all daisy-chained slave devices, which it may be driving, will be ready even if the master is very fast, and the slave(s) very slow. [Figure 20](#) shows the state sequences. At the end of Initialization, the device enters the Clear state where it clears the configuration memory. The active Low, open-drain initialization signal  $\overline{INIT}$  indicates when the Initialization and Clear states are complete. The FPGA tests for the absence of an external active Low  $\overline{RESET}$  before it makes a final sample of the mode lines and enters the Configuration state. An external wired-AND of one or more  $\overline{INIT}$  pins can be used to control configuration by the assertion of the active-Low  $\overline{RESET}$  of a master mode device or to signal a processor that the FPGAs are not yet initialized.

If a configuration has begun, a re-assertion of  $\overline{RESET}$  for a minimum of three internal timer cycles will be recognized and the FPGA will initiate an abort, returning to the Clear state to clear the partially loaded configuration memory words. The FPGA will then resample  $\overline{RESET}$  and the mode lines before re-entering the Configuration state.

During configuration, the XC3000A, XC3000L, XC3100A, and XC3100L devices check the bit-stream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls  $\overline{INIT}$  Low.



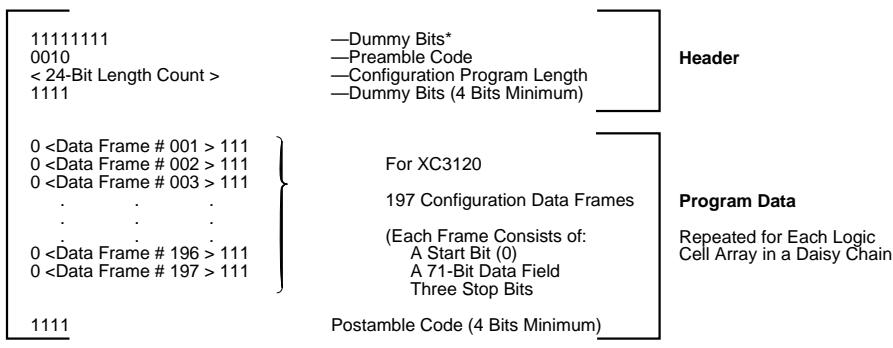
**Figure 20: A State Diagram of the Configuration Process for Power-up and Reprogram.**

A re-program is initiated when a configured XC3000 series device senses a High-to-Low transition and subsequent >6 µs Low level on the DONE/PROG package pin, or, if this pin is externally held permanently Low, a High-to-Low transition and subsequent >6 µs Low time on the RESET package pin.

The device returns to the Clear state where the configuration memory is cleared and mode lines re-sampled, as for an aborted configuration. The complete configuration program is cleared and loaded during each configuration program cycle.

Length count control allows a system of multiple Field Programmable Gate Arrays, of assorted sizes, to begin operation in a synchronized fashion. The configuration program

generated by the MakePROM program of the XACTstep development system begins with a preamble of 111111110010 followed by a 24-bit length count representing the total number of configuration clocks needed to complete loading of the configuration program(s). The data framing is shown in Figure 21. All FPGAs connected in series read and shift preamble and length count in on positive and out on negative configuration clock edges. A device which has received the preamble and length count then presents a High Data Out until it has intercepted the appropriate number of data frames. When the configuration program memory of an FPGA is full and the length count does not yet compare, the device shifts any additional data through, as it did for preamble and length count. When the FGA configuration memory is full and the length count



\*The LCA Device Requires Four Dummy Bits Min; XACT Software Generates Eight Dummy Bits

X5300

Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including 1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

**Figure 21: Internal Configuration Data Structure for an FPGA.** This shows the preamble, length count and data frames generated by the XACTstep Development System.

The Length Count produced by the MakeBits program = [(40-bit preamble + sum of program data + 1 per daisy chain device) rounded up to multiple of 8] – (2 ≤ K ≤ 4) where K is a function of DONE and RESET timing selected. An additional 8 is added if roundup increment is less than K. K additional clocks are needed to complete start-up after length count is reached.

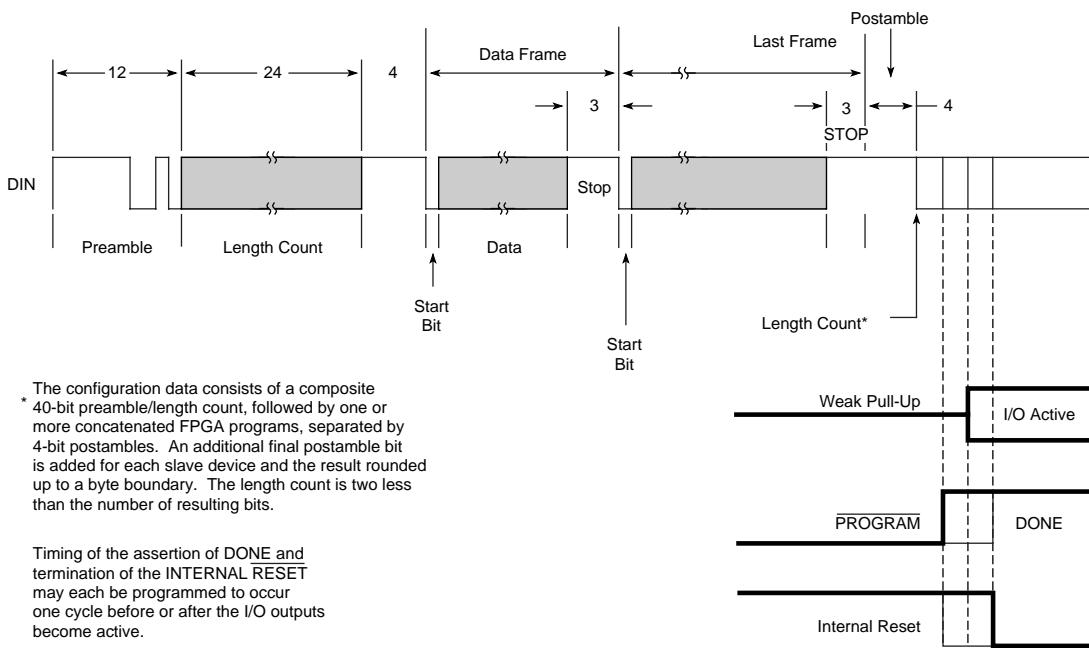
compares, the device will execute a synchronous start-up sequence and become operational. See [Figure 22](#). Two CCLK cycles after the completion of loading configuration data, the user I/O pins are enabled as configured. As selected in MakeBits, the internal user-logic RESET is released either one clock cycle before or after the I/O pins become active. A similar timing selection is programmable for the DONE/PROG output signal. DONE/PROG may also be programmed to be an open drain or include a pull-up resistor to accommodate wired ANDing. The High During Configuration (HDC) and Low During Configuration (LDC) are two user I/O pins which are driven active while an FPGA is in its Initialization, Clear or Configure states. They and DONE/PROG provide signals for control of external logic signals such as RESET, bus enable or PROM enable during configuration. For parallel Master configuration modes, these signals provide PROM enable control and allow the data pins to be shared with user logic signals.

User I/O inputs can be programmed to be either TTL or CMOS compatible thresholds. At power-up, all inputs have TTL thresholds and can change to CMOS thresholds at the completion of configuration if the user has selected CMOS thresholds. The threshold of PWRDWN and the direct clock inputs are fixed at a CMOS level.

If the crystal oscillator is used, it will begin operation before configuration is complete to allow time for stabilization before it is connected to the internal circuitry.

## Configuration Data

Configuration data to define the function and interconnection within a Field Programmable Gate Array is loaded from an external storage at power-up and after a re-program signal. Several methods of automatic and controlled loading of the required data are available. Logic levels applied to mode selection pins at the start of configuration time determine the method to be used. See [Table 1](#). The data may be either bit-serial or byte-parallel, depending on the configuration mode. The different FPGAs have different sizes and numbers of data frames. To maintain compatibility between various device types, the Xilinx product families use compatible configuration formats. For the XC3020A, configuration requires 14779 bits for each device, arranged in 197 data frames. An additional 40 bits are used in the header. See [Figure 22](#). The specific data format for each device is produced by the MakeBits command of the development system and one or more of these files can then be combined and appended to a length count preamble and be transformed into a PROM format file by the MakePROM command of the XACTstep development system. A compatibility exception precludes the use of an XC2000-series device as the master for XC3000-series devices if their DONE or RESET are programmed to occur after their outputs become active. The Tie Option of the MakeBits program defines output levels of unused blocks of a design and connects these to unused routing resources. This prevents indeterminate levels that might produce parasitic



**Figure 22: Configuration and Start-up of One or More FPGAs.**

supply currents. If unused blocks are not sufficient to complete the tie, the Flagnet command of EditLCA can be used to indicate nets which must not be used to drive the remaining unused routing, as that might affect timing of user nets. Norestore will retain the results of tie for timing analysis with Querynet before Restore returns the design to the untied condition. Tie can be omitted for quick breadboard iterations where a few additional millamps of I<sub>cc</sub> are acceptable.

The configuration bitstream begins with eight High preamble bits, a 4-bit preamble code and a 24-bit length count. When configuration is initiated, a counter in the FPGA is set to zero and begins to count the total number of configuration clock cycles applied to the device. As each configuration data frame is supplied to the device, it is internally assembled into a data word, which is then loaded in parallel into one word of the internal configuration memory array. The configuration loading process is complete when the current length count equals the loaded length count and the required configuration program data frames have been written. Internal user flip-flops are held Reset during configuration.

Two user-programmable pins are defined in the unconfigured Field Programmable Gate Array. High During Configuration (HDC) and Low During Configuration (LDC) as well as DONE/PROG may be used as external control signals during configuration. In Master mode configurations it is convenient to use LDC as an active-Low EPROM Chip Enable. After the last configuration data bit is loaded and the length count compares, the user I/O pins become active. Options in the MakeBits program allow timing choices of one clock earlier or later for the timing of the end of the internal logic RESET and the assertion of the DONE signal. The open-drain DONE/PROG output can be AND-tied with multiple devices and used as an active-High READY, an active-Low PROM enable or a RESET to other portions of the system. The state diagram of Figure 20 illustrates the configuration process.

## Configuration Modes

### Master Mode

In Master mode, the FPGA automatically loads configuration data from an external memory device. There are three Master modes that use the internal timing source to supply the configuration clock (CCLK) to time the incoming data. Master Serial mode uses serial configuration data supplied to Data-in (DIN) from a synchronous serial source such as the Xilinx Serial Configuration PROM shown in Figure 23. Master Parallel Low and High modes automatically use parallel data supplied to the D0–D7 pins in response to the 16-bit address generated by the FPGA. Figure 25 shows an example of the parallel Master mode connections required. The HEX starting address is 0000 and increments for Master Low mode and it is FFFF and decrements

for Master High mode. These two modes provide address compatibility with microprocessors which begin execution from opposite ends of memory.

### Peripheral Mode

Peripheral mode provides a simplified interface through which the device may be loaded byte-wide, as a processor peripheral. Figure 27 shows the peripheral mode connections. Processor write cycles are decoded from the common assertion of the active low Write Strobe (WS), and two active low and one active high Chip Selects (CS0, CS1, CS2). The FPGA generates a configuration clock from the internal timing generator and serializes the parallel input data for internal framing or for succeeding slaves on Data Out (DOUT). A output High on READY/BUSY pin indicates the completion of loading for each byte when the input register is ready for a new byte. As with Master modes, Peripheral mode may also be used as a lead device for a daisy-chain of slave devices.

### Slave Serial Mode

Slave Serial mode provides a simple interface for loading the Field Programmable Gate Array configuration as shown in Figure 29. Serial data is supplied in conjunction with a synchronizing input clock. Most Slave mode applications are in daisy-chain configurations in which the data input is driven from the previous FPGA's data out, while the clock is supplied by a lead device in Master or Peripheral mode. Data may also be supplied by a processor or other special circuits.

### Daisy Chain

The XACTstep development system is used to create a composite configuration for selected FPGAs including: a preamble, a length count for the total bitstream, multiple concatenated data programs and a postamble plus an additional fill bit per device in the serial chain. After loading and passing-on the preamble and length count to a possible daisy-chain, a lead device will load its configuration data frames while providing a High DOUT to possible down-stream devices as shown in Figure 25. Loading continues while the lead device has received its configuration program and the current length count has not reached the full value. The additional data is passed through the lead device and appears on the Data Out (DOUT) pin in serial form. The lead device also generates the Configuration Clock (CCLK) to synchronize the serial output data and data in of down-stream FPGAs. Data is read in on DIN of slave devices by the positive edge of CCLK and shifted out the DOUT on the negative edge of CCLK. A parallel Master mode device uses its internal timing generator to produce an internal CCLK of 8 times its EPROM address rate, while a Peripheral mode device produces a burst of 8 CCLKs for each chip select and write-strobe cycle. The internal timing generator continues to operate for general timing and synchronization of inputs in all modes.

## Special Configuration Functions

The configuration data includes control over several special functions in addition to the normal user logic functions and interconnect.

- Input thresholds
- Readback disable
- DONE pull-up resistor
- DONE timing
- RESET timing
- Oscillator frequency divided by two

Each of these functions is controlled by configuration data bits which are selected as part of the normal *XACTstep* development system bitstream generation process.

### **Input Thresholds**

Prior to the completion of configuration all FPGA input thresholds are TTL compatible. Upon completion of configuration, the input thresholds become either TTL or CMOS compatible as programmed. The use of the TTL threshold option requires some additional supply current for threshold shifting. The exception is the threshold of the PWRDWN input and direct clocks which always have a CMOS input. Prior to the completion of configuration the user I/O pins each have a high impedance pull-up. The configuration program can be used to enable the IOB pull-up resistors in the Operational mode to act either as an input load or to avoid a floating input on an otherwise unused pin.

### **Readback**

The contents of a Field Programmable Gate Array may be read back if it has been programmed with a bitstream in which the Readback option has been enabled. Readback may be used for verification of configuration and as a method of determining the state of internal logic nodes during debugging. There are three options in generating the configuration bitstream.

- “Never” inhibits the Readback capability.
- “One-time,” inhibits Readback after one Readback has been executed to verify the configuration.
- “On-command” allows unrestricted use of Readback.

Readback is accomplished without the use of any of the user I/O pins; only M0, M1 and CCLK are used. The initiation of Readback is produced by a Low to High transition of the M0/RTRIG (Read Trigger) pin. The CCLK input must then be driven by external logic to read back the configuration data. The first three Low-to-High CCLK transitions clock out dummy data. The subsequent Low-to-High CCLK transitions shift the data frame information out on the M1/RDATA (Read Data) pin. Note that the logic polarity is always inverted, a zero in configuration becomes a one in Readback, and vice versa. Note also that each Readback frame has one Start bit (read back as a one) but, unlike in configuration, each Readback frame has only one Stop bit (read back as a zero). The third leading dummy bit men-

tioned above can be considered the Start bit of the first frame. All data frames must be read back to complete the process and return the Mode Select and CCLK pins to their normal functions.

Readback data includes the current state of each CLB flip-flop, each input flip-flop or latch, and each device pad. These data are imbedded into unused configuration bit positions during Readback. This state information is used by the *XACTstep* development system In-Circuit Verifier to provide visibility into the internal operation of the logic while the system is operating. To readback a uniform time-sample of all storage elements, it may be necessary to inhibit the system clock.

### **Reprogram**

To initiate a re-programming cycle, the dual-function pin DONE/PROG must be given a High-to-Low transition. To reduce sensitivity to noise, the input signal is filtered for two cycles of the FPGA internal timing generator. When reprogram begins, the user-programmable I/O output buffers are disabled and high-impedance pull-ups are provided for the package pins. The device returns to the Clear state and clears the configuration memory before it indicates ‘initialized’. Since this Clear operation uses chip-individual internal timing, the master might complete the Clear operation and then start configuration before the slave has completed the Clear operation. To avoid this problem, the slave INIT pins must be AND-wired and used to force a RESET on the master (see [Figure 25](#)). Reprogram control is often implemented using an external open-collector driver which pulls DONE/PROG Low. Once a stable request is recognized, the DONE/PROG pin is held Low until the new configuration has been completed. Even if the re-program request is externally held Low beyond the configuration period, the FPGA will begin operation upon completion of configuration.

### **DONE Pull-up**

DONE/PROG is an open-drain I/O pin that indicates the FPGA is in the operational state. An optional internal pull-up resistor can be enabled by the user of the *XACT* development system when MakeBits is executed. The DONE/PROG pins of multiple FPGAs in a daisy-chain may be connected together to indicate all are DONE or to direct them all to reprogram.

### **DONE Timing**

The timing of the DONE status signal can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This facilitates control of external functions such as a PROM enable or holding a system in a wait state.

## RESET Timing

As with DONE timing, the timing of the release of the internal reset can be controlled by a selection in the MakeBits program to occur either a CCLK cycle before, or after, the outputs going active. See [Figure 22](#). This reset keeps all user programmable flip-flops and latches in a zero state during configuration.

## Crystal Oscillator Division

A selection in the MakeBits program allows the user to incorporate a dedicated divide-by-two flip-flop between the crystal oscillator and the alternate clock line. This guarantees a symmetrical clock signal. Although the frequency stability of a crystal oscillator is very good, the symmetry of its waveform can be affected by bias or feedback drive.

## Bitstream Error Checking

**Bitstream error checking** protects against erroneous configuration.

Each Xilinx FPGA bitstream consists of a 40-bit preamble, followed by a device-specific number of data frames. The number of bits per frame is also device-specific; however, each frame ends with three stop bits (111) followed by a start bit for the next frame (0).

All devices in all XC3000 families start reading in a new frame when they find the first 0 after the end of the previous frame. XC3000 device does not check for the correct stop bits, but XC3000A/XC3100A/XC3000L and XC3100L devices check that the last three bits of any frame are actually 111.

Under normal circumstances, all these FPGAs behave the same way; however, if the bitstream is corrupted, an XC3000 device will always start a new frame as soon as it finds the first 0 after the end of the previous frame, even if the data is completely wrong or out-of-sync. Given sufficient zeros in the data stream, the device will also go Done,

but with incorrect configuration and the possibility of internal contention.

An XC3000A/XC3100A/XC3000L/XC3100L device starts any new frame only if the three preceding bits are all ones. If this check fails, it pulls INIT Low and stops the internal configuration, although the Master CCLK keeps running. The user must then start a new configuration by applying a >6 µs Low level on RESET.

This simple check does not protect against random bit errors, but it offers almost 100 percent protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, or PC-board level defects, such as broken lines or solder-bridges.

## Reset Spike Protection

A separate modification slows down the RESET input before configuration by using a two-stage shift register driven from the internal clock. It tolerates submicrosecond High spikes on RESET before configuration. The XC3000 master can be connected like an XC4000 master, but with its RESET input used instead of INIT. (On XC3000, INIT is output only).

## Soft Start-up

After configuration, the outputs of all FPGAs in a daisy-chain become active simultaneously, as a result of the same CCLK edge. In the original XC3000/3100 devices, each output becomes active in either fast or slew-rate limited mode, depending on the way it is configured. This can lead to large ground-bounce signals. In XC3000A/XC3000L/XC3100A/XC3100L devices, all outputs become active first in slew-rate limited mode, reducing the ground bounce. After this soft start-up, each individual output slew rate is again controlled by the respective configuration bit.

## Configuration Timing

This section describes the configuration modes in detail.

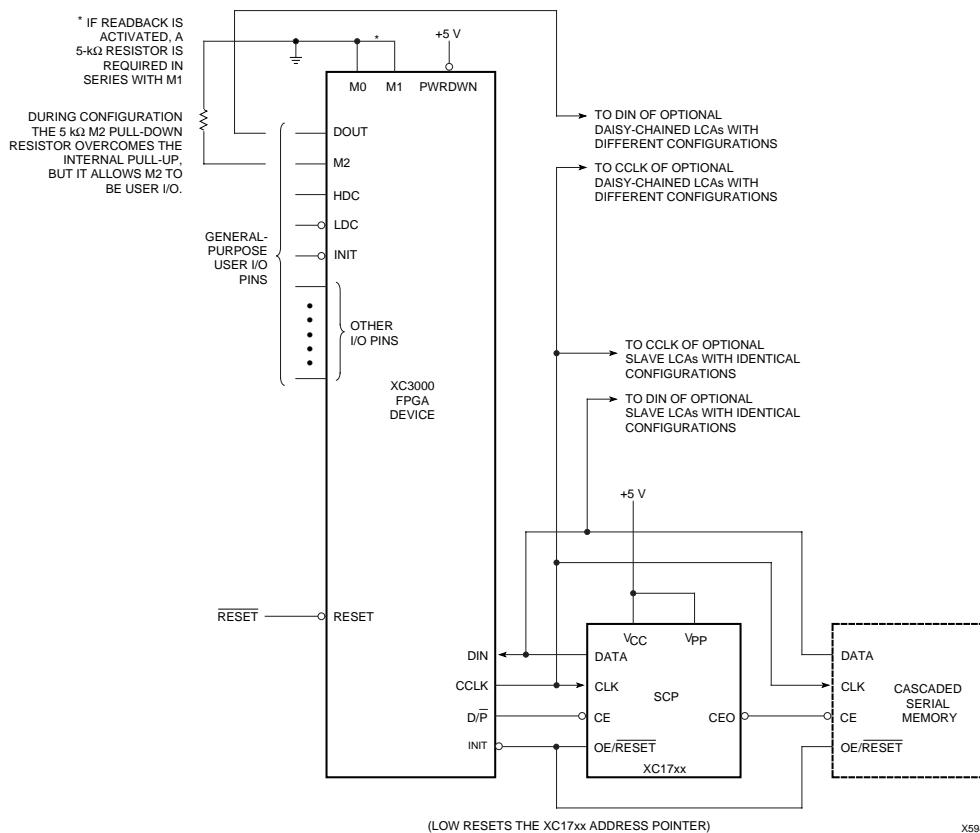
### Master Serial Mode

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

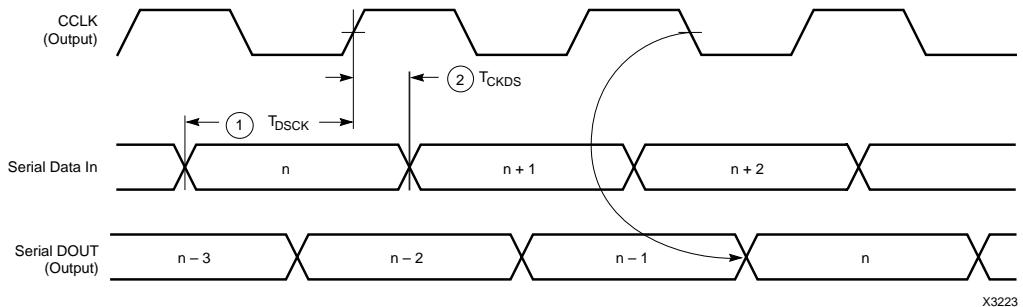
The lead FPGA then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that

DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.

The SPROM CE input can be driven from either LDC or DONE. Using LDC avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but LDC is then restricted to be a permanently High user output. Using DONE also avoids contention on DIN, provided the early DONE option is invoked.



**Figure 23: Master Serial Mode Circuit Diagram**



X3223

	Description	Symbol	Min	Max	Units
CCLK	Data In setup	1 $T_{DSCK}$	60		ns
	Data In hold	2 $C_{KDS}$	0		ns

- Notes:
- At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$  may require >6- $\mu$ s High level on RESET, followed by a >6- $\mu$ s Low level on RESET and D/P after  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L).
  - Configuration can be controlled by holding RESET Low with or until after the INIT of all daisy-chain slave-mode devices is High.
  - Master-serial-mode timing is based on slave-mode testing.

**Figure 24: Master Serial Mode Programming Switching Characteristics**

## Master Parallel Mode

In Master Parallel mode, the lead FPGA directly addresses an industry-standard byte-wide EPROM and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an inter-

nal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data, and also changes the EPROM address, until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next device in the daisy chain accepts data on the subsequent rising CCLK edge.

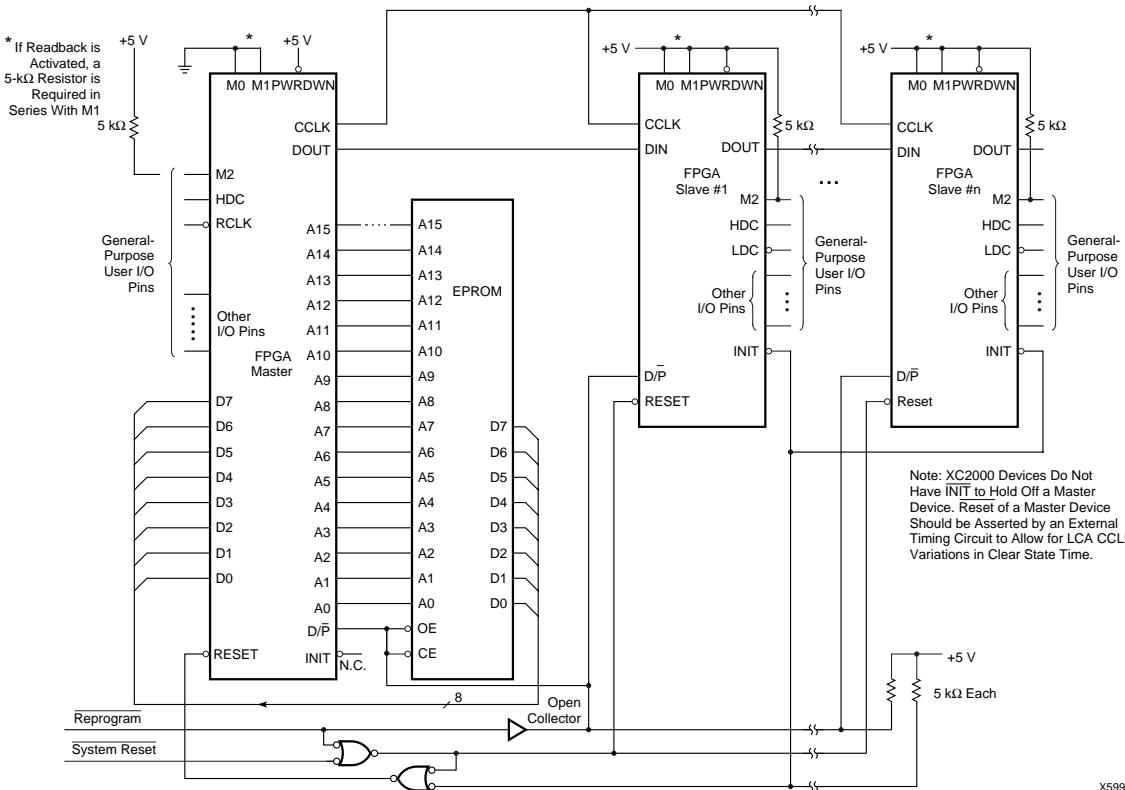
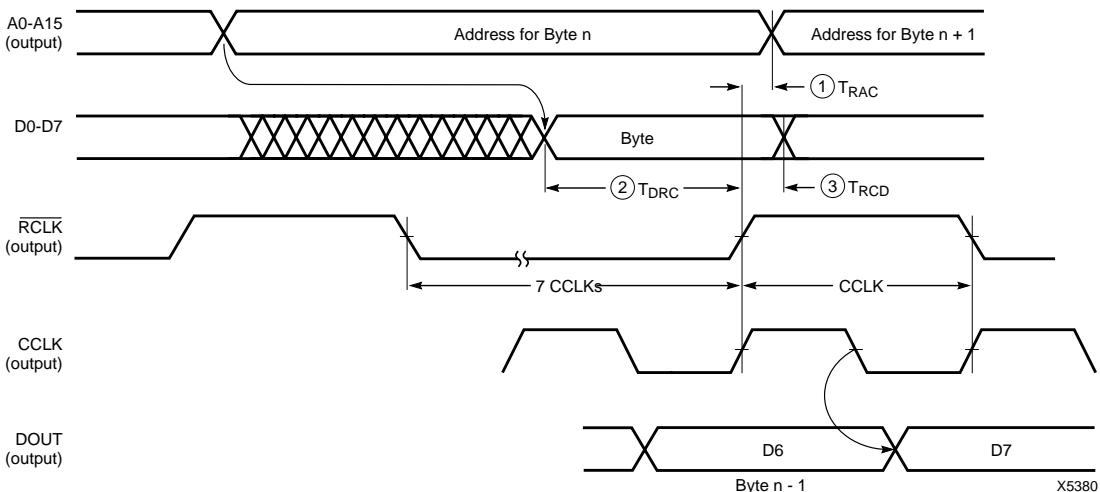


Figure 25: Master Parallel Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
RCLK	To address valid	1	$T_{RAC}$	0	200	ns
	To data setup	2	$T_{DRC}$	60		ns
	To data hold	3	$T_{RCD}$	0		ns
	RCLK High		$T_{RCH}$	600		ns
	RCLK Low		$T_{RCL}$	4.0		$\mu s$

Notes:

- At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding  $\overline{RESET}$  Low until  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$  may require a >6- $\mu s$  High level on  $\overline{RESET}$ , followed by a >6- $\mu s$  Low level on  $\overline{RESET}$  and D/P after  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L).
- Configuration can be controlled by holding  $\overline{RESET}$  Low with or until after the  $\overline{INIT}$  of all daisy-chain slave-mode devices is High.

*This timing diagram shows that the EPROM requirements are extremely relaxed:  
EPROM access time can be longer than 4000 ns. EPROM data output has no hold time requirements.*

**Figure 26: Master Parallel Mode Programming Switching Characteristics**

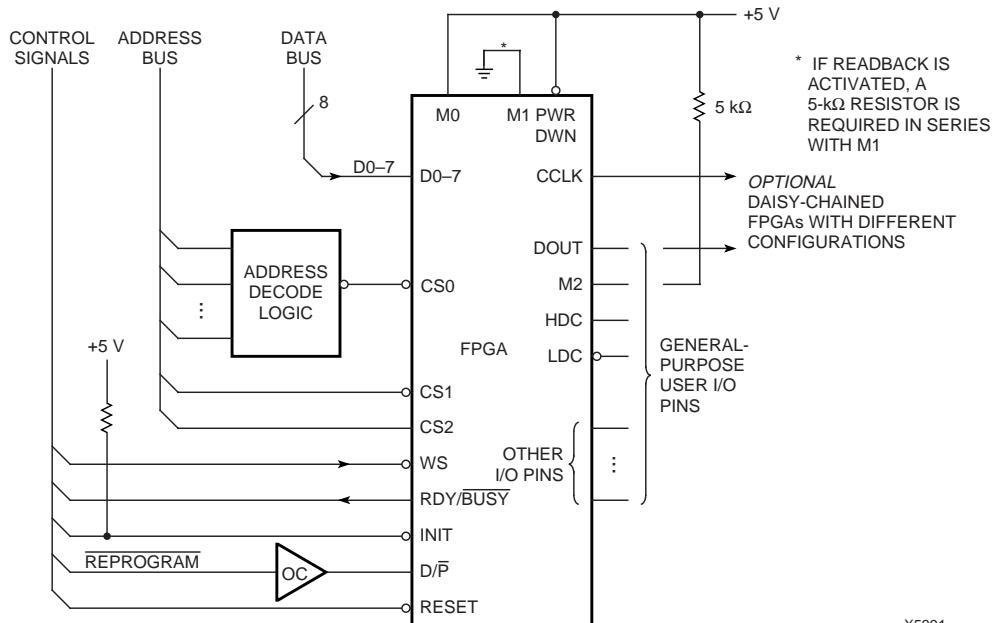
## Peripheral Mode

Peripheral mode uses the trailing edge of the logic AND condition of the  $\overline{CS_0}$ ,  $\overline{CS_1}$ , CS2, and WS inputs to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead FPGA presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The Ready/Busy output from the lead device acts as a handshake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again

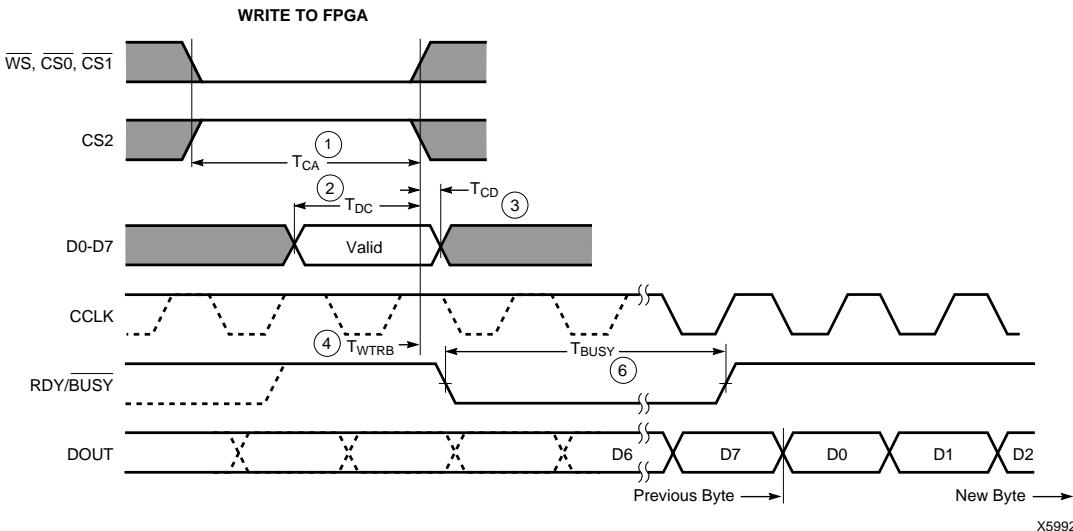
when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the BUSY signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the BUSY signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the BUSY signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered.



X5991

**Figure 27:** Peripheral Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
WRITE	Effective Write time required (Assertion of $\overline{CS0}$ , $\overline{CS1}$ , $\overline{CS2}$ , $\overline{WS}$ )	1	$T_{CA}$	100		ns
	DIN Setup time required	2	$T_{DC}$	60		ns
	DIN Hold time required	3	$T_{CD}$	0		ns
RDY	RDY/BUSY delay after end of $\overline{WS}$	4	$T_{TWTRB}$		60	ns
	Earliest next $\overline{WS}$ after end of BUSY	5	$T_{TRBWT}$	0		ns
	BUSY Low time generated	6	$T_{BUSY}$	2.5	9	CCLK periods

- Notes:
- At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$  may require a >6- $\mu$ s High level on RESET, followed by a >6- $\mu$ s Low level on RESET and D/P after  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L).
  - Configuration must be delayed until the INIT of all FPGAs is High.
  - Time from end of WS to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
  - CCLK and DOUT timing is tested in slave mode.
  - $T_{BUSY}$  indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest  $T_{BUSY}$  occurs when a byte is loaded into an empty parallel-to-serial converter. The longest  $T_{BUSY}$  occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

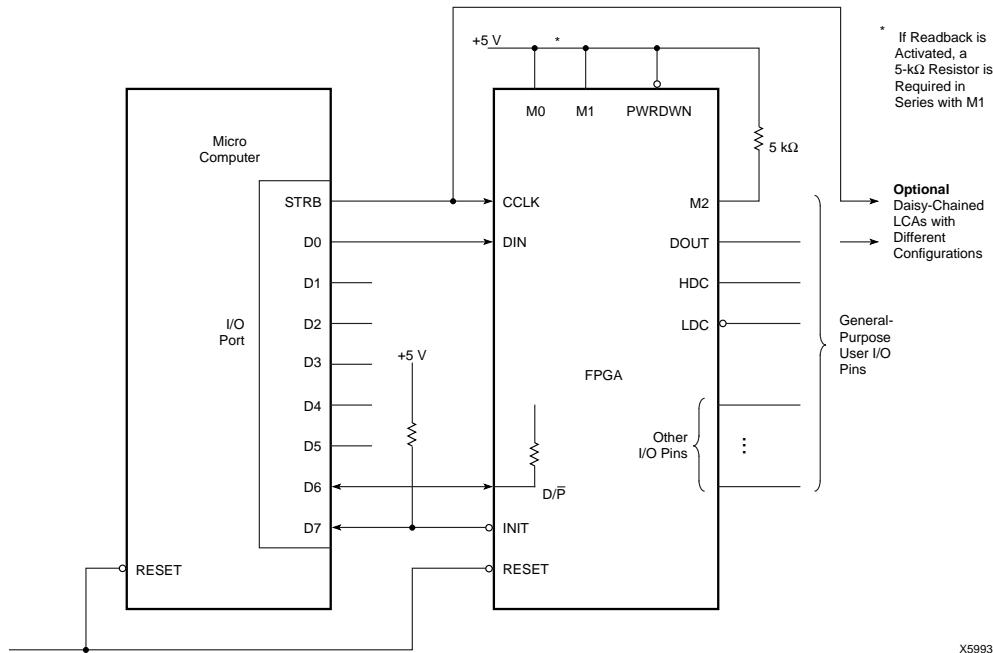
**Note:** This timing diagram shows very relaxed requirements: Data need not be held beyond the rising edge of  $\overline{WS}$ .  $\overline{BUSY}$  will go active within 60 ns after the end of  $\overline{WS}$ .  $\overline{BUSY}$  will stay active for several microseconds.  $\overline{WS}$  may be asserted immediately after the end of  $\overline{BUSY}$ .

**Figure 28: Peripheral Mode Programming Switching Characteristics**

## Slave Serial Mode

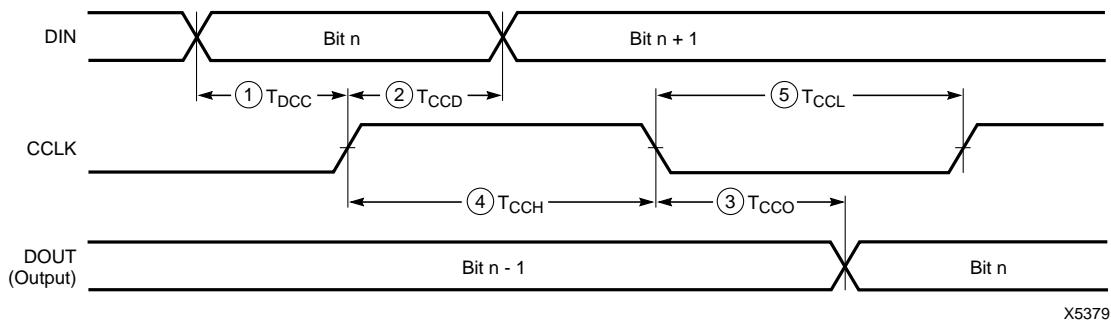
In Slave Serial mode, an external signal drives the CCLK input(s) of the FPGA(s). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short set-up time before each rising CCLK edge. The lead device then presents the preamble data (and all data that over-

flows the lead device) on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next device in the daisy-chain accepts data on the subsequent rising CCLK edge.



X5993

**Figure 29: Slave Serial Mode Circuit Diagram**



X5379

	Description		Symbol	Min	Max	Units
CCLK	To DOUT	3	$T_{CCO}$		100	ns
	DIN setup	1	$T_{DCC}$	60		ns
	DIN hold	2	$T_{CCD}$	0		ns
	High time	4	$T_{CCH}$	0.05		$\mu s$
	Low time (Note 1)	5	$T_{CCL}$	0.05	5.0	$\mu s$
	Frequency		$F_{CC}$		10	MHz

Notes:

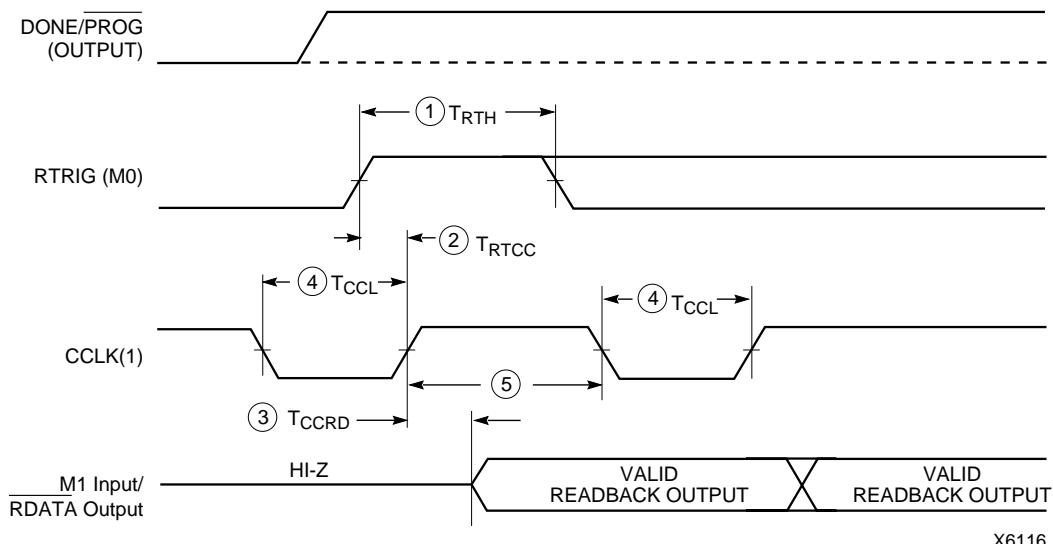
1. The max limit of CCLK Low time is caused by dynamic circuitry inside the FPGA.

2. Configuration must be delayed until the INIT of all FPGAs is High.

3. At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$  may require a >6- $\mu s$  High level on RESET, followed by a >6- $\mu s$  Low level on RESET and D/P after  $V_{CC}$  has reached 4.0 V (2.5 V for the XC3000L).

**Figure 30: Slave Serial Mode Programming Switching Characteristics**

## Program Readback Switching Characteristics



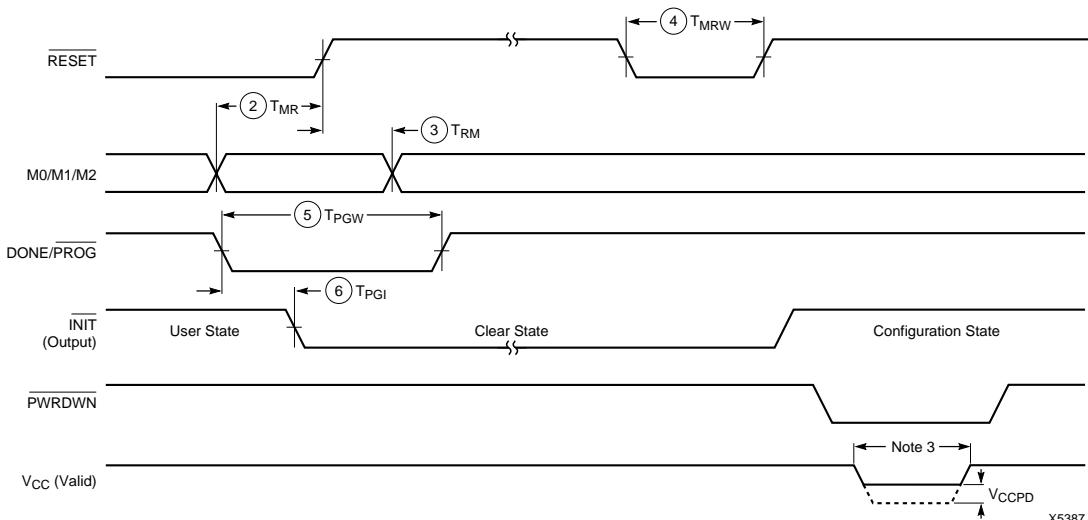
X6116

	Description	Symbol	Min	Max	Units
RTRIG	RTRIG High	1 $T_{RTH}$	250		ns
CCLK	RTRIG setup RDATA delay High time Low time	2 $T_{RTCC}$ 3 $T_{CCRD}$ 4 $T_{CCHR}$ 5 $T_{CCLR}$	200 100 0.5 0.5		ns ns $\mu$ s $\mu$ s

Notes:

1. During Readback, CCLK frequency may not exceed 1 MHz.
2. RTRIG (M0 positive transition) shall not be done until after one clock following active I/O pins.
3. Readback should not be initiated until configuration is complete.
4.  $T_{CCLR}$  is 5  $\mu$ s min to 15  $\mu$ s max for XC3000L.

## General XC3000 Series Switching Characteristics



	Description	Symbol		Min	Max	Units
RESET (2)	M0, M1, M2 setup time required	2	$T_{MR}$	1		μs
	M0, M1, M2 hold time required	3	$T_{RM}$	4.5		μs
	RESET Width (Low) req. for Abort	4	$T_{MRW}$	6		μs
DONE/PROG	Width (Low) required for Re-config.	5	$T_{PGW}$	6		μs
	INIT response after D/P is pulled Low	6	$T_{PGI}$		7	μs
PWRDWN (3)	Power Down $V_{CC}$	$V_{CCPD}$		2.3		V

Notes:

- At power-up,  $V_{CC}$  must rise from 2.0 V to  $V_{CC}$  min in less than 25 ms. If this is not possible, configuration can be delayed by holding RESET Low until  $V_{CC}$  has reached 4.0 V (2.5 V for XC3000L). A very long  $V_{CC}$  rise time of >100 ms, or a non-monotonically rising  $V_{CC}$ , may require a >1-μs High level on RESET, followed by a >6-μs Low level on RESET and D/P after  $V_{CC}$  has reached 4.0 V (2.5 V for XC3000L).
- RESET timing relative to valid mode lines (M0, M1, M2) is relevant when RESET is used to delay configuration. The specified hold time is caused by a shift-register filter slowing down the response to RESET during configuration.
- PWRDWN transitions must occur while  $V_{CC} > 4.0$  V (2.5 V for XC3000L).

## Device Performance

The XC3000 families of FPGAs can achieve very high performance. This is the result of

- A sub-micron manufacturing process, developed and continuously being enhanced for the production of state-of-the-art CMOS SRAMs.
- Careful optimization of transistor geometries, circuit design, and lay-out, based on years of experience with the XC3000 family.
- A look-up table based, coarse-grained architecture that can collapse multiple-layer combinatorial logic into a single function generator. One CLB can implement up to four layers of conventional logic in as little as 1.5 ns.

Actual system performance is determined by the timing of critical paths, including the delay through the combinatorial and sequential logic elements within CLBs and IOBs, plus the delay in the interconnect routing. The AC-timing specifications state the worst-case timing parameters for the various logic resources available in the XC3000-families architecture. [Figure 31](#) shows a variety of elements involved in determining system performance.

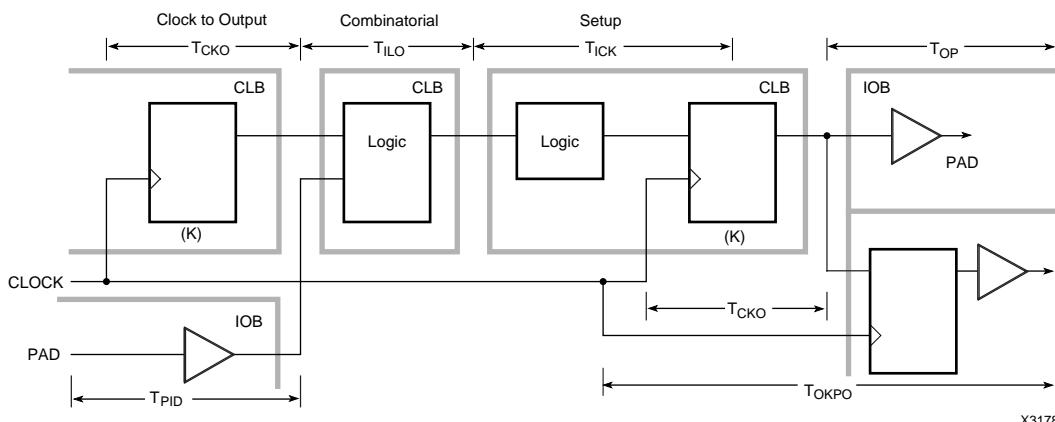
Logic block performance is expressed as the propagation time from the interconnect point at the input to the output of the block in the interconnect area. Since combinatorial logic is implemented with a memory lookup table within a CLB, the combinatorial delay through the CLB, called  $T_{ILO}$ , is always the same, regardless of the function being implemented. For the combinatorial logic function driving the data input of the storage element, the critical timing is data set-up relative to the clock edge provided to the flip-flop element. The delay from the clock source to the output of the logic block is critical in the timing signals pro-

duced by storage elements. Loading of a logic-block output is limited only by the resulting propagation delay of the larger interconnect network. Speed performance of the logic block is a function of supply voltage and temperature. See [Figure 32](#).

Interconnect performance depends on the routing resources used to implement the signal path. Direct interconnects to the neighboring CLB provide an extremely fast path. Local interconnects go through switch matrices (magic boxes) and suffer an RC delay, equal to the resistance of the pass transistor multiplied by the capacitance of the driven metal line. Longlines carry the signal across the length or breadth of the chip with only one access delay. Generous on-chip signal buffering makes performance relatively insensitive to signal fan-out; increasing fan-out from 1 to 8 changes the CLB delay by only 10%. Clocks can be distributed with two low-skew clock distribution networks.

The tools in the XACTstep Development System used to place and route a design in an XC3000 FPGA automatically calculate the actual maximum worst-case delays along each signal path. This timing information can be back-annotated to the design's netlist for use in timing simulation or examined with X-Delay, a static timing analyzer.

Actual system performance is applications dependent. The maximum clock rate that can be used in a system is determined by the critical path delays within that system. These delays are combinations of incremental logic and routing delays, and vary from design to design. In a synchronous system, the maximum clock rate depends on the number of combinatorial logic layers between re-synchronizing flip-flops. [Figure 33](#) shows the achievable clock rate as a function of the number of CLB layers.



**Figure 31: Primary Block Speed Factors.** Actual timing is a function of various block factors combined with routing factors. Overall performance can be evaluated with XDelay timing calculator or by an optional simulation.

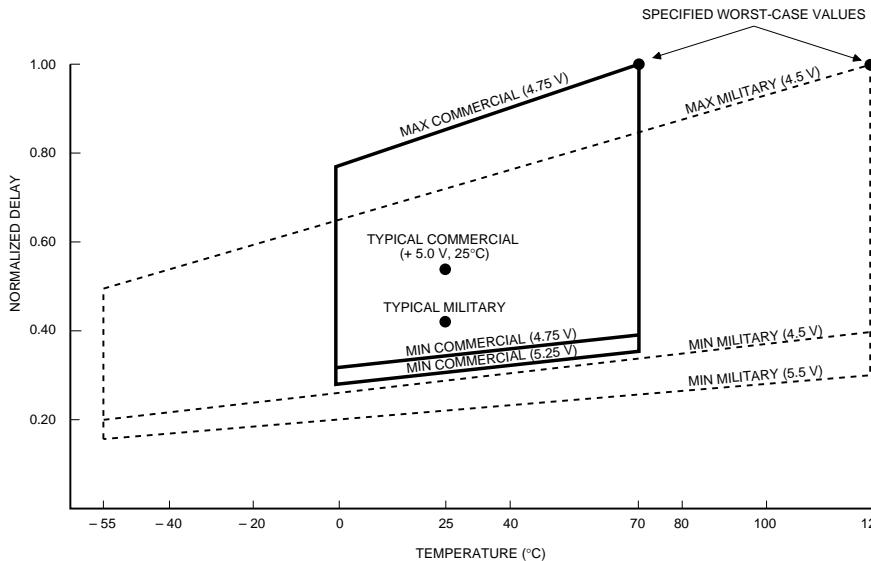


Figure 32: Relative Delay as a Function of Temperature, Supply Voltage and Processing Variations

X6094

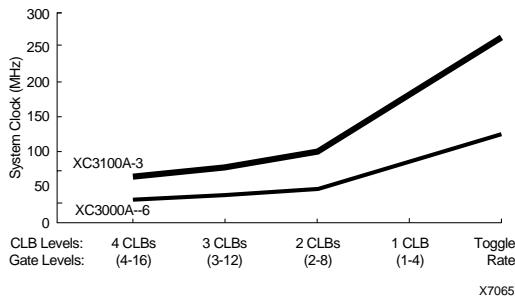


Figure 33: Clock Rate as a Function of Logic Complexity (Number of Combinational Levels between Flip-Flops)

## Power

### Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated  $V_{CC}$  and ground ring surrounding the logic array provides power to the I/O drivers. An independent matrix of  $V_{CC}$  and groundlines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a  $0.1\text{-}\mu\text{F}$  capacitor connected near the  $V_{CC}$  and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 4- or 8-mA loads under worst-case conditions may be capable of driving as much as 25 to 30 times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise.

## Dynamic Power Consumption

	XC3042A	XC3042L	XC3142A	
One CLB driving three local interconnects	0.25	0.17	0.25	mW per MHz
One global clock buffer and clock line	2.25	1.40	1.70	mW per MHz
One device output with a 50 pF load	1.25	1.25	1.25	mW per MHz

## Power Consumption

The Field Programmable Gate Array exhibits the low power consumption characteristic of CMOS ICs. For any design, the configuration option of TTL chip input threshold requires power for the threshold reference. The power required by the static memory cells that hold the configuration data is very low and may be maintained in a power-down mode.

Typically, most of power dissipation is produced by external capacitive loads on the output buffers. This load and frequency dependent power is 25  $\mu\text{W}/\text{pF}/\text{MHz}$  per output. Another component of I/O power is the external dc loading on all output pins.

Internal power dissipation is a function of the number and size of the nodes, and the frequency at which they change. In an FPGA, the fraction of nodes changing on a given clock is typically low (10-20%). For example, in a long binary counter, the total activity of all counter flip-flops is equivalent to that of only two CLB outputs toggling at the clock frequency. Typical global clock-buffer power is between 2.0 mW/MHz for the XC3020A and 3.5 mW/MHz for the XC3090A. The internal capacitive load is more a function of interconnect than fan-out. With a typical load of three general interconnect segments, each CLB output requires about 0.25 mW per MHz of its output frequency.

Because the control storage of the FPGA is CMOS static memory, its cells require a very low standby current for data retention. In some systems, this low data retention current characteristic can be used as a method of preserving configurations in the event of a primary power loss. The FPGA

has built in powerdown logic which, when activated, will disable normal operation of the device and retain only the configuration data. All internal operation is suspended and output buffers are placed in their high-impedance state with no pull-ups. Different from the XC3000 family which can be powered down to a current consumption of a few microamps, the XC3100A draws 5 mA, even in power-down. This makes power-down operation less meaningful. In contrast,  $I_{CCPD}$  for the XC3000L is only 10  $\mu\text{A}$ .

To force the FPGA into the Powerdown state, the user must pull the  $\overline{\text{PWRDWN}}$  pin Low and continue to supply a retention voltage to the  $V_{CC}$  pins. When normal power is restored,  $V_{CC}$  is elevated to its normal operating voltage and  $\overline{\text{PWRDWN}}$  is returned to a High. The FPGA resumes operation with the same internal sequence that occurs at the conclusion of configuration. Internal-I/O and logic-block storage elements will be reset, the outputs will become enabled and the  $\text{DONE}/\overline{\text{PROG}}$  pin will be released.

When  $V_{CC}$  is shut down or disconnected, some power might unintentionally be supplied from an incoming signal driving an I/O pin. The conventional electrostatic input protection is implemented with diodes to the supply and ground. A positive voltage applied to an input (or output) will cause the positive protection diode to conduct and drive the  $V_{CC}$  connection. This condition can produce invalid power conditions and should be avoided. A large series resistor might be used to limit the current or a bipolar buffer may be used to isolate the input signal.

## Pin Descriptions

### Permanently Dedicated Pins

#### V<sub>CC</sub>

Two to eight (depending on package type) connections to the positive V supply voltage. All must be connected.

#### GND

Two to eight (depending on package type) connections to ground. All must be connected.

#### PWRDWN

A Low on this CMOS-compatible input stops all internal activity, but retains configuration. All flip-flops and latches are reset, all outputs are 3-stated, and all inputs are interpreted as High, independent of their actual level. When PWRDWN returns High, the FPGA becomes operational with DONE Low for two cycles of the internal 1-MHz clock. Before and during configuration, PWRDWN must be High. If not used, PWRDWN must be tied to V<sub>CC</sub>.

#### RESET

This is an active Low input which has three functions.

Prior to the start of configuration, a Low input will delay the start of the configuration process. An internal circuit senses the application of power and begins a minimal time-out cycle. When the time-out and  $\overline{\text{RESET}}$  are complete, the levels of the M lines are sampled and configuration begins.

If  $\overline{\text{RESET}}$  is asserted during a configuration, the FPGA is re-initialized and restarts the configuration at the termination of  $\overline{\text{RESET}}$ .

If  $\overline{\text{RESET}}$  is asserted after configuration is complete, it provides a global asynchronous  $\overline{\text{RESET}}$  of all IOB and CLB storage elements of the FPGA.

#### CCLK

During configuration, Configuration Clock is an output of an FPGA in Master mode or Peripheral mode, but an input in Slave mode. During Readback, CCLK is a clock input for shifting configuration data out of the FPGA.

CCLK drives dynamic circuitry inside the FPGA. The Low time may, therefore, not exceed a few microseconds. When used as an input, CCLK must be “parked High”. An internal pull-up resistor maintains High when the pin is not being driven.

#### DONE/PROG (D/P)

DONE is an open-drain output, configurable with or without an internal pull-up resistor of 2 to 8 k $\Omega$ . At the completion of configuration, the FPGA circuitry becomes active in a synchronous order; DONE is programmed to go active High one cycle either before or after the outputs go active.

Once configuration is done, a High-to-Low transition of this pin will cause an initialization of the FPGA and start a reconfiguration.

#### M0/RTRIG

As Mode 0, this input is sampled on power-on to determine the power-on delay (2<sup>14</sup> cycles if M0 is High, 2<sup>16</sup> cycles if M0 is Low). Before the start of configuration, this input is again sampled together with M1, M2 to determine the configuration mode to be used.

A Low-to-High input transition, after configuration is complete, acts as a Read Trigger and initiates a Readback of configuration and storage-element data clocked by CCLK. By selecting the appropriate Readback option when generating the bitstream, this operation may be limited to a single Readback, or be inhibited altogether.

#### M1/RDATA

As Mode 1, this input and M0, M2 are sampled before the start of configuration to establish the configuration mode to be used. If Readback is never used, M1 can be tied directly to ground or V<sub>CC</sub>. If Readback is ever used, M1 must use a 5-k $\Omega$  resistor to ground or V<sub>CC</sub>, to accommodate the RDATA output.

As an active-Low Read Data, after configuration is complete, this pin is the output of the Readback data.

### User I/O Pins That Can Have Special Functions

#### M2

During configuration, this input has a weak pull-up resistor. Together with M0 and M1, it is sampled before the start of configuration to establish the configuration mode to be used. After configuration, this pin is a user-programmable I/O pin.

#### HDC

During configuration, this output is held at a High level to indicate that configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin.

#### LDC

During Configuration, this output is held at a Low level to indicate that the configuration is not yet complete. After configuration, this pin is a user-programmable I/O pin. LDC is particularly useful in Master mode as a Low enable for an EPROM, but it must then be programmed as a High after configuration.

#### INIT

This is an active Low open-drain output with a weak pull-up and is held Low during the power stabilization and internal clearing of the configuration memory. It can be used to indicate status to a configuring microprocessor or, as a wired

AND of several slave mode devices, a hold-off signal for a master mode device. After configuration this pin becomes a user-programmable I/O pin.

#### **BCLKIN**

This is a direct CMOS level input to the alternate clock buffer (Auxiliary Buffer) in the lower right corner.

#### **XTL1**

This user I/O pin can be used to operate as the output of an amplifier driving an external crystal and bias circuitry.

#### **XTL2**

This user I/O pin can be used as the input of an amplifier connected to an external crystal and bias circuitry. The I/O Block is left unconfigured. The oscillator configuration is activated by routing a net from the oscillator buffer symbol output and by the MakeBits program.

#### **CS0, CS1, CS2, WS**

These four inputs represent a set of signals, three active Low and one active High, that are used to control configuration-data entry in the Peripheral mode. Simultaneous assertion of all four inputs generates a Write to the internal data buffer. The removal of any assertion clocks in the D0-D7 data. In Master-Parallel mode, WS and CS2 are the A0 and A1 outputs. After configuration, these pins are user-programmable I/O pins.

#### **RDY/BUSY**

During Peripheral Parallel mode configuration this pin indicates when the chip is ready for another byte of data to be written to it. After configuration is complete, this pin becomes a user-programmable I/O pin.

#### **RCLK**

During Master Parallel mode configuration, each change on the A0-15 outputs is preceded by a rising edge on RCLK, a redundant output signal. After configuration is complete, this pin becomes a user-programmable I/O pin.

#### **D0-D7**

This set of eight pins represents the parallel configuration byte for the parallel Master and Peripheral modes. After configuration is complete, they are user-programmed I/O pins.

#### **A0-A15**

During Master Parallel mode, these 16 pins present an address output for a configuration EPROM. After configuration, they are user-programmable I/O pins.

#### **DIN**

During Slave or Master Serial configuration, this pin is used as a serial-data input. In the Master or Peripheral configuration, this is the Data 0 input. After configuration is complete, this pin becomes a user-programmed I/O pin.

#### **DOUT**

During configuration this pin is used to output serial-configuration data to the DIN pin of a daisy-chained slave. After configuration is complete, this pin becomes a user-programmed I/O pin.

#### **TCLKIN**

This is a direct CMOS-level input to the global clock buffer. This pin can also be configured as a user programmable I/O pin. However, since TCLKIN is the preferred input to the global clock net, and the global clock net should be used as the primary clock source, this pin is usually the clock input to the chip.

### **Unrestricted User I/O Pins**

#### **I/O**

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. All unrestricted I/O pins, plus the special pins mentioned on the following page, have a weak pull-up resistor of 50 kΩ to 100 kΩ that becomes active as soon as the device powers up, and stays active until the end of configuration.

**Note:** Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.

## Pin Functions During Configuration

Configuration Mode <M2:M1:M0>					***		**									****							
SLAVE SERIAL <1:1:1>	MASTER-SERIAL <0:0:0>	PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	44 PLCC	64 VQFP	68 PLCC	84 PGA	84 PQFP	100 TQFP	132 PGA	144 TQFP	160 PQFP	175 PGA	176 TQFP	208 PQFP	223 PGA	User Function					
POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	POWER DWN (I)	7	17	10	12	B2	29	26	A1	1	159	B2	1	3	B2					
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	16	31	25	31	J2	52	49	B13	36	40	B14	45	48	C16	RDATA				
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	17	32	26	32	L1	54	51	A14	38	42	B15	47	50	B17	RTRIG (I)				
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	18	33	27	33	K2	56	53	C13	40	44	C15	49	56	A17	I/O				
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	19	34	28	34	K3	57	54	B14	41	45	E14	50	57	A18	I/O				
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	20	36	30	36	L3	59	56	D14	45	49	D16	54	61	E16	I/O				
INIT*	INIT*	INIT*	INIT*	INIT*	22	40	34	42	K6	65	62	G14	53	59	H15	65	77	J16	I/O				
GND	GND	GND	GND	GND	23	41	35	43	J6	66	63	H12	55	61	J14	67	79	K15	GND				
					26	47	43	53	L11	76	73	M13	69	76	P15	85	100	V18	XTL2 OR I/O				
RESET (I)	RESET (I)	RESET (I)	RESET (I)	RESET (I)	27	48	44	54	K10	78	75	P14	71	78	R15	87	102	U17	RESET (I)				
DONE	DONE	DONE	DONE	DONE	28	49	45	55	J10	80	77	N13	73	80	R14	89	107	V17	PROGRAM (I)				
					DATA 7 (I)	DATA 7 (I)	DATA 7 (I)			50	46	56	K11	81	78	M12	74	81	N13	90	109	T16	I/O
					30	51	47	57	J11	82	79	P13	75	82	T14	91	110	U16	XTL1 OR I/O				
					DATA 6 (I)	DATA 6 (I)	DATA 6 (I)			52	48	58	H10	83	80	N11	78	86	P12	96	115	U15	I/O
					DATA 5 (I)	DATA 5 (I)	DATA 5 (I)			53	49	60	F10	87	84	M9	84	92	T11	102	122	U12	I/O
					CS0 (I)					54	50	61	G10	88	85	N9	85	93	R10	103	123	V11	I/O
					DATA 4 (I)	DATA 4 (I)	DATA 4 (I)			55	51	62	G11	89	86	N8	88	96	R9	108	128	U10	I/O
					DATA 3 (I)	DATA 3 (I)	DATA 3 (I)			57	53	65	F11	92	89	N7	92	102	P8	112	132	T9	I/O
					CS1 (I)					58	54	66	E11	93	90	P6	93	103	R8	113	133	U9	I/O
					DATA 2 (I)	DATA 2 (I)	DATA 2 (I)			59	55	67	E10	94	91	M6	96	106	R7	118	138	V8	I/O
					DATA 1 (I)	DATA 1 (I)	DATA 1 (I)			60	56	70	D10	98	95	M5	102	114	R5	124	145	U5	I/O
					RDY/BUSY					61	57	71	C11	99	96	N4	103	115	P5	125	146	U4	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	38	62	58	72	B11	100	97	N2	106	119	R3	130	151	U3	I/O				
DOUT	DOUT	DOUT	DOUT	DOUT	39	63	59	73	C10	1	98	M3	107	120	N4	131	152	V2	I/O				
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (O)	40	64	60	74	A11	2	99	P1	108	121	R2	132	153	U2	CCLK (I)				
					WS (I)	A0	A0			1	61	75	B10	5	2	M2	111	124	P2	135	161	T3	I/O
					CS2 (I)	A1	A1			2	62	76	B9	6	3	N1	112	125	M3	136	162	V1	I/O
						A2	A2			3	63	77	A10	8	5	L2	115	128	P1	140	165	R2	I/O
						A3	A3			4	64	78	A9	9	6	L1	116	129	N1	141	166	T1	I/O
						A15	A15			65	81	B6	12	9	K1	119	132	M1	146	172	N2	5	
						A4	A4			5	66	82	B7	13	10	J2	120	133	L2	147	173	M4	I/O
						A14	A14			6	67	83	A7	14	11	H1	123	136	K2	150	178	L4	I/O
						A5	A5			7	68	84	C7	15	12	H2	124	137	K1	151	179	L2	I/O
						A13	A13			9	2	2	A6	17	14	G2	128	141	H2	156	184	K3	I/O
						A6	A6			10	3	3	A5	18	15	G1	129	142	H1	157	185	J1	I/O
						A12	A12			11	4	4	B5	19	16	F2	133	147	F2	164	192	G1	I/O
						A7	A7			12	5	5	C5	20	17	E1	134	148	E1	165	193	G4	I/O
						A11	A11			13	6	8	A3	23	20	D1	137	151	D1	169	199	F4	I/O
						A8	A8			14	7	9	A2	24	21	D2	138	152	C1	170	200	E2	I/O
						A10	A10			15	8	10	B3	25	22	B1	141	155	E3	173	203	E3	I/O
						A9	A9			16	9	11	A1	26	26	C2	142	156	C2	174	204	B1	I/O
																		All Others					
													X	X	X	X						XC3x20A etc.	
													X	X	X	X						XC3x30A etc.	
													X**			X	X					XC3x42A etc.	
													X**			X	X	X	X	X	X	XC3x64A etc.	
													X**			X	X	X	X	X	X	XC3x90A etc.	
																						XC3195A	

Notes:

Generic I/O pins are not shown.

For a detailed description of the configuration modes, see page 343 through page 352.

For pinout details, see page 383 through page 394.

Represents a 50-kΩ to 100-kΩ pull-up before and during configuration.

INIT is an open drain output during configuration.

Represents an input.

Pin assignment for the XC3064A/XC3090A and XC3195A differ from those shown.

Peripheral mode and master parallel mode are not supported in the PC44 package.

Pin assignments for the XC3195A PQ208 differ from those shown.

Pin assignments of PGA Footprint PLCC sockets and PGA packages are not identical.

The information on this page is provided as a convenient summary. For detailed pin descriptions, see the preceding two pages.

**Note:** Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50-kW to 100-kW pull-up resistor.

## XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3000A Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
$V_{IHT}$	High-level input voltage — TTL configuration	2.0	$V_{CC}$	V
$V_{ILT}$	Low-level input voltage — TTL configuration	0	0.8	V
$V_{IHC}$	High-level input voltage — CMOS configuration	70%	100%	$V_{CC}$
$V_{ILC}$	Low-level input voltage — CMOS configuration	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns

**Note:** At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

### XC3000A DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)	Commercial	3.86	V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)		0.40	V
$V_{OH}$	High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)	Industrial	3.76	V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)		0.40	V
$V_{CCPD}$	Power-down supply voltage (PWRDWN must be Low)	2.30		V
$I_{CCPD}$	Power-down supply current ( $V_{CC(MAX)}$ @ $T_{MAX}$ )	3020A	100	$\mu A$
		3030A	160	$\mu A$
		3042A	240	$\mu A$
		3064A	340	$\mu A$
		3090A	500	$\mu A$
$I_{CCO}$	Quiescent FPGA supply current in addition to $I_{CCPD}$ Chip thresholds programmed as CMOS levels Chip thresholds programmed as TTL levels		500	$\mu A$
			10	$\mu A$
$I_{IL}$	Input Leakage Current	-10	+10	$\mu A$
$C_{IN}$	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		10	pF
			15	pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		16	pF
			20	pF
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)	0.02	0.17	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low		3.4	mA

**Notes:** 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at  $V_{CC}$  or GND, and the FPGA device configured with a MakeBits tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per  $V_{CC}$  pin. The number of ground pins varies from the XC3020A to the XC3090A.

**XC3000A Absolute Maximum Ratings**

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
$T_J$	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

**XC3000A Global Buffer Switching Characteristics Guidelines**

Description	Symbol	Speed Grade		Units
		-7	-6	
Global and Alternate Clock Distribution <sup>1</sup> Either: <b>Normal</b> IOB input pad through clock buffer to any CLB or IOB clock input Or: <b>Fast</b> (CMOS only) input pad through clock buffer to any CLB or IOB clock input	$T_{PID}$	7.5	7.0	ns
	$T_{PIDC}$	6.0	5.7	ns
<b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup> I to L.L. while T is Low (buffer active) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \downarrow$ to L.L. active and valid with pair of pull-up resistors $T \uparrow$ to L.L. High with single pull-up resistor $T \uparrow$ to L.L. High with pair of pull-up resistors	$T_{IO}$ $T_{ON}$ $T_{ON}$ $T_{PUS}$ $T_{PUF}$	4.5 9.0 11.0 16.0 10.0	4.0 8.0 10.0 14.0 8.0	ns ns ns ns ns
<b>BIDI</b> Bidirectional buffer delay	$T_{BIDI}$	1.7	1.5	ns

**Note:** 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

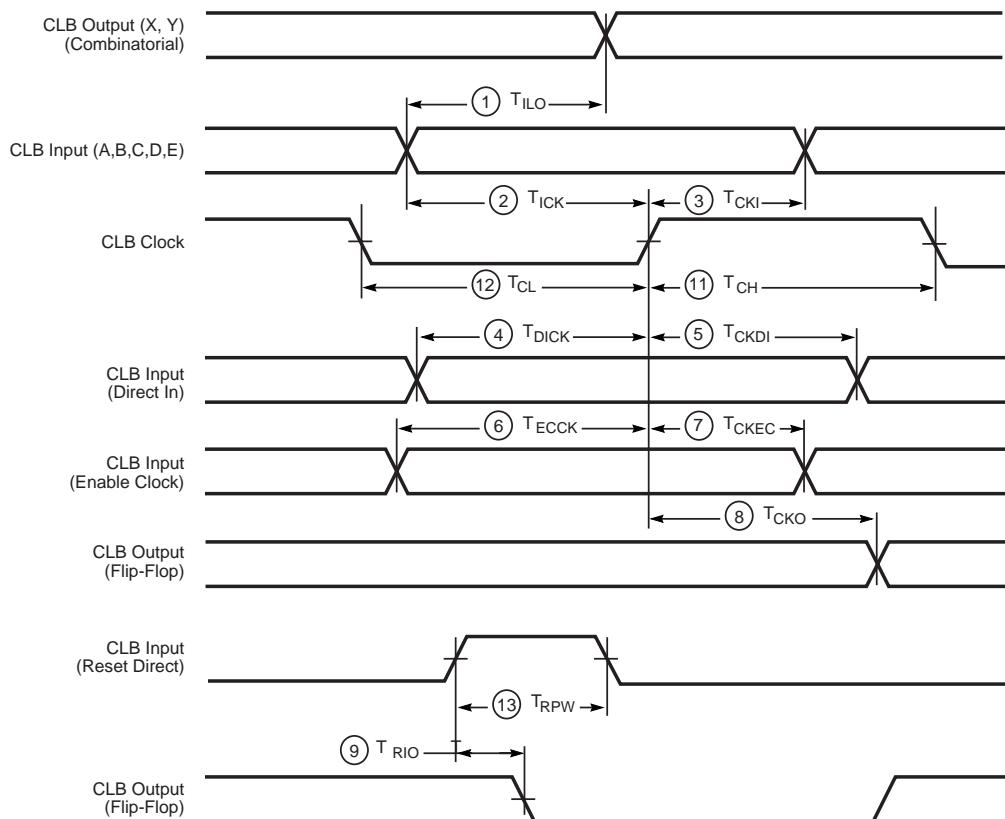
## XC3000A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-7		-6		
Description		Symbol		Min	Max	Min	Max	Units
Combinatorial Delay Logic Variables	A, B, C, D, E, to outputs X or Y FG Mode F and FGM Mode	1	$T_{ILO}$		5.1 5.6		4.1 4.6	ns ns
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y FG Mode F and FGM Mode		8	$T_{CKO}$		4.5		4.0	ns
			$T_{QLO}$		9.5 10.0		8.0 8.5	ns ns
Set-up time before clock K Logic Variables	A, B, C, D, E FG Mode F and FGM Mode	2	$T_{ICK}$	4.5 5.0		3.5 4.0		ns ns
Data In Enable Clock	DI EC	4 6	$T_{DICK}$ $T_{ECKK}$	4.0 4.5		3.0 4.0		ns ns
Hold Time after clock K Logic Variables	A, B, C, D, E	3	$T_{CKI}$	0		0		ns
Data In Enable Clock	DI <sup>2</sup> EC	5 7	$T_{CKDI}$ $T_{CKEC}$	1.0 2.0		1.0 2.0		ns ns
Clock Clock High time Clock Low time Max. flip-flop toggle rate		11 12	$T_{CH}$ $T_{CL}$ $F_{CLK}$	4.0 4.0 113.0		3.5 3.5 135.0		ns ns MHz
Reset Direct (RD) RD width delay from RD to outputs X or Y		13 9	$T_{RPW}$ $T_{RIO}$	6.0	6.0	5.0	5.0	ns ns
Global Reset ( $\overline{\text{RESET}}$ Pad) <sup>1</sup> $\overline{\text{RESET}}$ width (Low) delay from $\overline{\text{RESET}}$ pad to outputs X or Y			$T_{MRW}$ $T_{MRQ}$	16.0	19.0	14.0	17.0	ns ns

**Notes:** 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

2. The CLB K to Q output delay ( $T_{CKO}$ , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement ( $T_{CKDI}$ , #5) of any CLB on the same die.

**XC3000A CLB Switching Characteristics Guidelines (continued)**

X5424

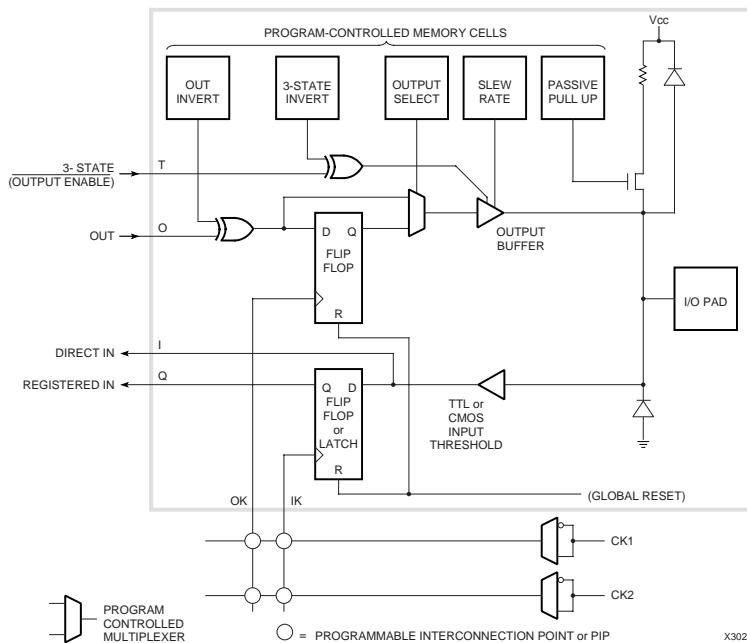
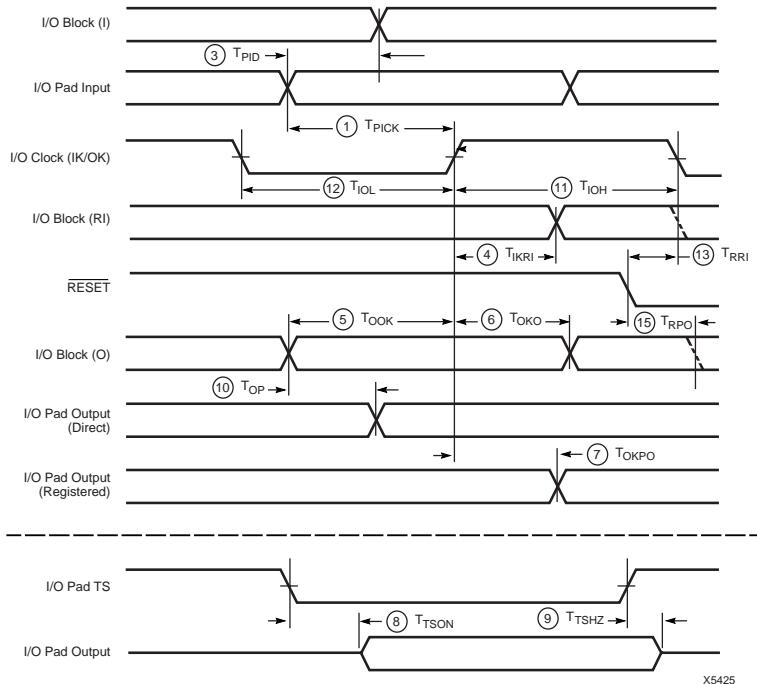
## XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-7		-6		
Description	Symbol	Min	Max	Min	Max	Units
Propagation Delays (Input)						
Pad to Direct In (I)	T <sub>PID</sub>		4.0		3.0	ns
Pad to Registered In (Q) with latch transparent	T <sub>PTG</sub>		15.0		14.0	ns
Clock (IK) to Registered In (Q)	T <sub>IKRI</sub>		3.0		2.5	ns
Set-up Time (Input)						
Pad to Clock (IK) set-up time	T <sub>PICK</sub>	14.0		12.0		ns
Propagation Delays (Output)						
Clock (OK) to Pad (fast)	T <sub>OKPO</sub>		8.0		7.0	ns
same (slew rate limited)	T <sub>OKPO</sub>		18.0		15.0	ns
Output (O) to Pad (fast)	T <sub>OPF</sub>		6.0		5.0	ns
same (slew-rate limited)	T <sub>OPS</sub>		16.0		13.0	ns
3-state to Pad begin hi-Z (fast)	T <sub>TSHZ</sub>		10.0		9.0	ns
same (slew-rate limited)	T <sub>TSHZ</sub>		20.0		12.0	ns
3-state to Pad active and valid (fast)	T <sub>TSON</sub>		11.0		10.0	ns
same (slew -rate limited)	T <sub>TSON</sub>		21.0		18.0	ns
Set-up and Hold Times (Output)						
Output (O) to clock (OK) set-up time	T <sub>OOK</sub>	8.0		7.0		ns
Output (O) to clock (OK) hold time	T <sub>OKO</sub>	0		0		ns
Clock						
Clock High time	T <sub>IOH</sub>	4.0		3.5		ns
Clock Low time	T <sub>IOL</sub>	4.0		3.5		ns
Max. flip-flop toggle rate	F <sub>CLK</sub>	113.0		135.0		MHz
Global Reset Delays (based on XC3042A)						
RESET Pad to Registered In (Q)	T <sub>RR</sub>		24.0		23.0	ns
RESET Pad to output pad (fast)	T <sub>RPO</sub>		33.0		29.0	ns
(slew-rate limited)	T <sub>RPO</sub>		43.0		37.0	ns

- Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
  4. T<sub>PID</sub>, T<sub>PTG</sub>, and T<sub>PICK</sub> are 3 ns higher for XTL2 when the pin is configured as a user input.

## XC3000A IOB Switching Characteristics Guidelines (continued)



## XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3000L Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
$V_{IH}$	High-level input voltage — TTL configuration	2.0	$V_{CC}+0.3$	V
$V_{IL}$	Low-level input voltage — TTL configuration	-0.3	0.8	V
$T_{IN}$	Input signal transition time		250	ns

- Notes:**
- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
  - Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 6.0 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V  $V_{CC}$  range.

### XC3000L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)	2.40		V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)		0.40	V
$V_{OH}$	High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)	$V_{CC} - 0.2$		V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)		0.2	V
$V_{CCPD}$	Power-down supply voltage (PWRDWN must be Low)	2.30		V
$I_{CCPD}$	Power-down supply current ( $V_{CC(MAX)}$ @ $T_{MAX}$ )		10	µA
$I_{CCO}$	Quiescent FPGA supply current in addition to $I_{CCPD}$ <sup>1</sup> Chip thresholds programmed as CMOS levels		20	µA
$I_{IL}$	Input Leakage Current	-10	+10	µA
$C_{IN}$	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2		15 20	pF pF
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)	0.02	0.17	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low		2.50	mA

- Notes:**
- With no output current loads, no active input or Longline pull-up resistors, all package pins at  $V_{CC}$  or GND, and the FPGA device configured with a MakeBits tie option.  $I_{CCO}$  is in addition to  $I_{CCPD}$ .
  - Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per  $V_{CC}$  pin. The number of ground pins varies from the XC3020L to the XC3090L.

## XC3000L Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
$T_J$	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## XC3000L Global Buffer Switching Characteristics Guidelines

Description	Speed Grade	-8	
	Symbol	Max	Units
Global and Alternate Clock Distribution <sup>1</sup> Either: <b>Normal</b> IOB input pad through clock buffer to any CLB or IOB clock input Or: <b>Fast</b> (CMOS only) input pad through clock buffer to any CLB or IOB clock input	$T_{PID}$	9.0	ns
	$T_{PIDC}$	7.0	ns
<b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup> I to L.L. while T is Low (buffer active) $T_{\downarrow}$ to L.L. active and valid with single pull-up resistor $T_{\uparrow}$ to L.L. High with single pull-up resistor	$T_{IO}$ $T_{ON}$ $T_{PUS}$	5.0 12.0 24.0	ns ns ns
<b>BIDI</b> Bidirectional buffer delay	$T_{BIDI}$	2.0	ns

1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

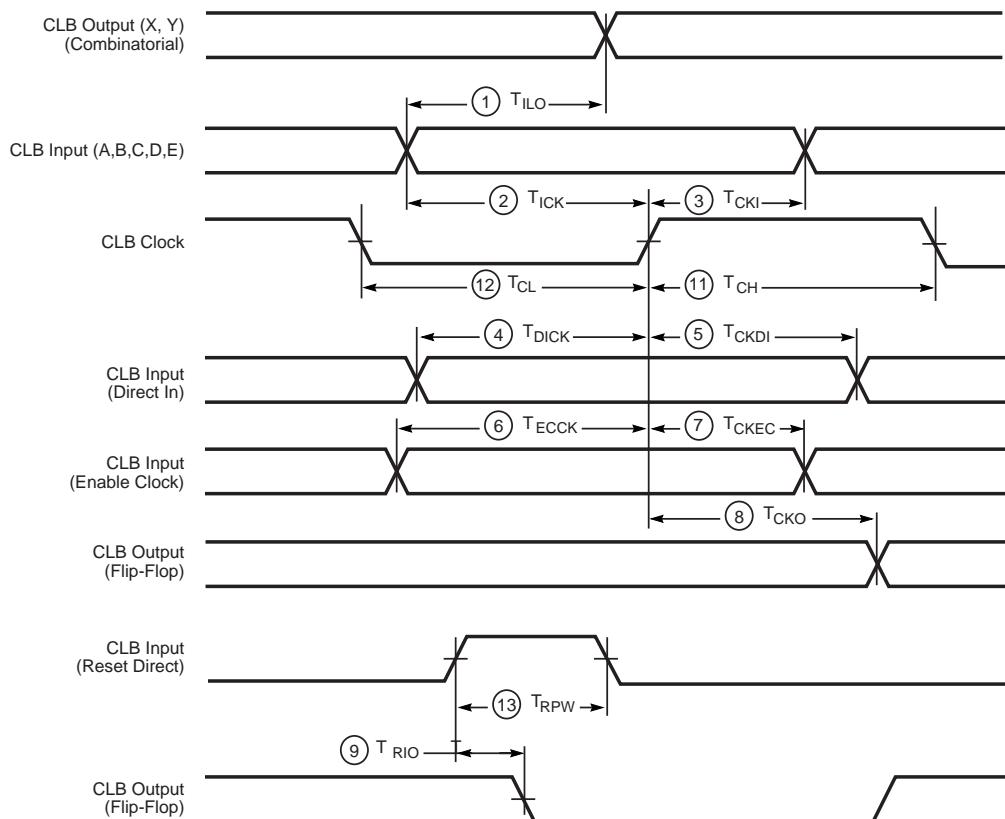
## XC3000L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade		-8	
Description		Symbol	Min	Max	Units
Combinatorial Delay					
Logic Variables	A, B, C, D, E, to outputs X or Y FG Mode F and FGM Mode	1	T <sub>ILO</sub>	6.7 7.5	ns ns
Sequential delay					
Clock k to outputs X or Y		8	T <sub>CKO</sub>	7.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y			T <sub>QLO</sub>	14.0 14.8	ns ns
FG Mode					
F and FGM Mode					
Set-up time before clock K					
Logic Variables	A, B, C, D, E FG Mode F and FGM Mode	2	T <sub>ICK</sub>	5.0 5.8	ns ns
Data In	DI	4	T <sub>DICK</sub>	5.0	ns
Enable Clock	EC	6	T <sub>ECCK</sub>	6.0	ns
Hold Time after clock K					
Logic Variables	A, B, C, D, E	3	T <sub>CKI</sub>	0	ns
Data In	DI <sup>2</sup>	5	T <sub>CKDI</sub>	2.0	ns
Enable Clock	EC	7	T <sub>CKEC</sub>	2.0	ns
Clock					
Clock High time		11	T <sub>CH</sub>	5.0	ns
Clock Low time		12	T <sub>CL</sub>	5.0	ns
Max. flip-flop toggle rate			F <sub>CLK</sub>	80.0	MHz
Reset Direct (RD)					
RD width		13	T <sub>RPW</sub>	7.0	ns
delay from RD to outputs X or Y		9	T <sub>RIO</sub>	7.0	ns
Global Reset (RESET Pad) <sup>1</sup>					
RESET width (Low)			T <sub>MRW</sub>	16.0	ns
delay from RESET pad to outputs X or Y			T <sub>MRQ</sub>	23.0	ns

**Notes:** 1. Timing is based on the XC3042L, for other devices see XACT timing calculator.

2. The CLB K to Q output delay (T<sub>CKO</sub>, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T<sub>CKDI</sub>, #5) of any CLB on the same die.

**XC3000L CLB Switching Characteristics Guidelines (continued)**

X5424

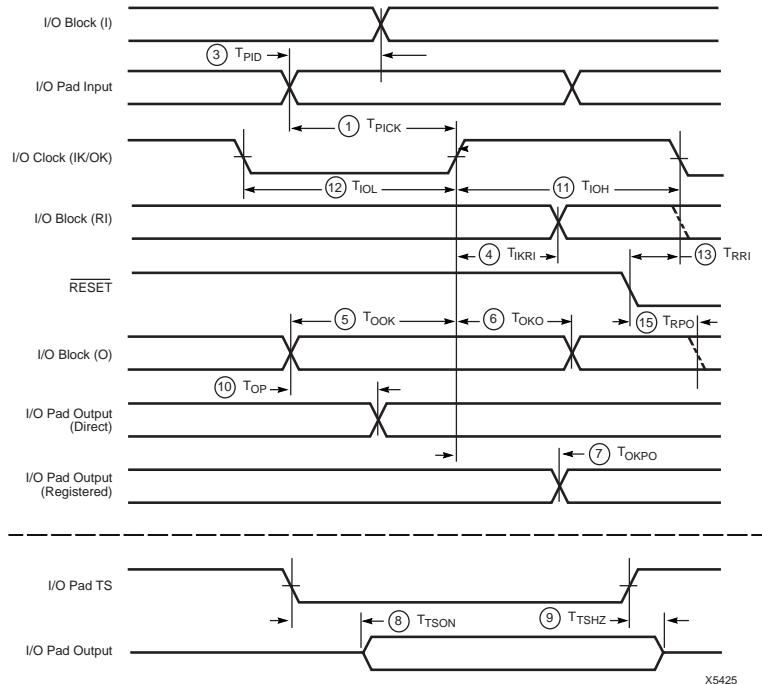
## XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

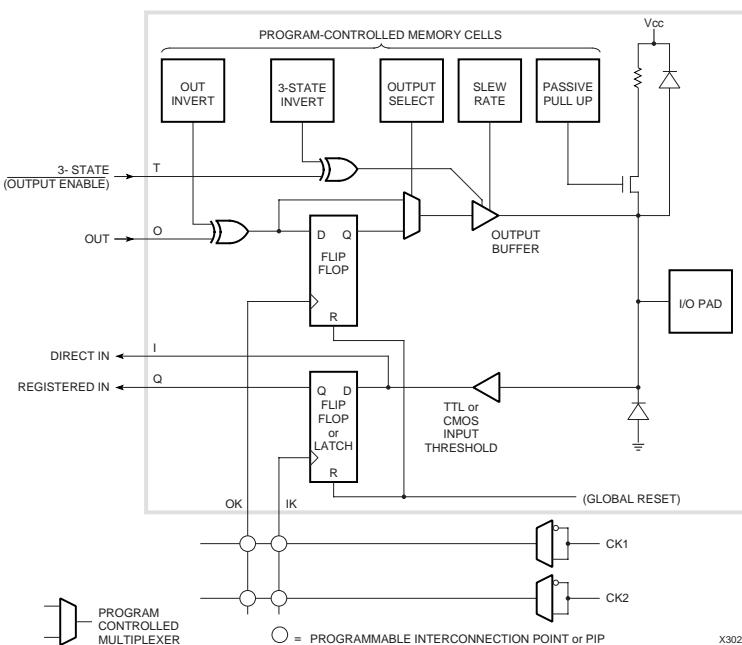
Description	Symbol	Speed Grade		-8	Units
		Min	Max		
Propagation Delays (Input)					
Pad to Direct In (I)	$T_{PID}$	3		5.0	ns
Pad to Registered In (Q) with latch transparent	$T_{PTG}$			24.0	ns
Clock (IK) to Registered In (Q)	$T_{IKRI}$	4		6.0	ns
Set-up Time (Input)					
Pad to Clock (IK) set-up time	$T_{PICK}$	1	22.0		ns
Propagation Delays (Output)					
Clock (OK) to Pad (fast)	$T_{OKPO}$	7		12.0	ns
same (slew rate limited)	$T_{OKPO}$	7		28.0	ns
Output (O) to Pad (fast)	$T_{OPF}$	10		9.0	ns
same (slew-rate limited)	$T_{OPS}$	10		25.0	ns
3-state to Pad begin hi-Z (fast)	$T_{TSHZ}$	9		12.0	ns
same (slew-rate limited)	$T_{TSHZ}$	9		28.0	ns
3-state to Pad active and valid (fast)	$T_{TSON}$	8		16.0	ns
same (slew -rate limited)	$T_{TSON}$	8		32.0	ns
Set-up and Hold Times (Output)					
Output (O) to clock (OK) set-up time	$T_{OOK}$	5		12.0	ns
Output (O) to clock (OK) hold time	$T_{OKO}$	6	0		ns
Clock					
Clock High time	$T_{IOH}$	11		5.0	ns
Clock Low time	$T_{IOL}$	12		5.0	ns
Max. flip-flop toggle rate	$F_{CLK}$		80.0		MHz
Global Reset Delays (based on XC3042A)					
RESET Pad to Registered In (Q)	$T_{RRI}$	13		25.0	ns
RESET Pad to output pad (fast)	$T_{RPO}$	15		35.0	ns
(slew-rate limited)	$T_{RPO}$	15		51.0	ns

- Notes:**
- Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  - Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  - Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
  - $T_{PID}$ ,  $T_{PTG}$ , and  $T_{PICK}$  are 3 ns higher for XTL2 when the pin is configured as a user input.

## XC3000L IOB Switching Characteristics Guidelines (continued)



X5425



X3029

## XC3100A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3100A Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.25	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
$V_{IHT}$	High-level input voltage — TTL configuration	2.0	$V_{CC}$	V
$V_{ILT}$	Low-level input voltage — TTL configuration	0	0.8	V
$V_{IHC}$	High-level input voltage — CMOS configuration	70%	100%	$V_{CC}$
$V_{ILC}$	Low-level input voltage — CMOS configuration	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns

**Note:** At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

### XC3100A DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage (@ $I_{OH} = -8.0$ mA, $V_{CC}$ min)	Commercial	3.86	V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 8.0$ mA, $V_{CC}$ min)		0.40	V
$V_{OH}$	High-level output voltage (@ $I_{OH} = -8.0$ mA, $V_{CC}$ min)	Industrial	3.76	V
$V_{OL}$	Low-level output voltage (@ $I_{OL} = 8.0$ mA, $V_{CC}$ min)		0.40	V
$V_{CCPD}$	Power-down supply voltage (PWRDWN must be Low)	2.30		V
$I_{CCO}$	Quiescent LCA supply current in addition to $I_{CCPD}$ <sup>1</sup>			
	Chip thresholds programmed as CMOS levels		8	mA
$I_{IL}$	Chip thresholds programmed as TTL levels		14	mA
	Input Leakage Current	-10	+10	µA
$C_{IN}$	Input capacitance, all packages except PGA175 (sample tested)			
	All Pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF
	Input capacitance, PGA 175 (sample tested)		15	pF
	All Pins except XTL1 and XTL2		20	pF
	XTL1 and XTL2			
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)	0.02	0.17	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low	0.20	2.80	mA

**Notes:** 1. With no output current loads, no active input or Longline pull-up resistors, all package pins at  $V_{CC}$  or GND, and the LCA device configured with a MakeBits tie option.

2. Total continuous output sink current may not exceed 100 mA per ground pin. The number of ground pins varies from two for the XC3120A in the PC84 package, to eight for the XC3195A in the PQ208 or PG223 package.

## XC3100A Absolute Maximum Ratings

Symbol	Description			Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0		V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$		V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$		V
$T_{STG}$	Storage temperature (ambient)	-65 to +150		°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260		°C
$T_J$	Junction temperature plastic	+125		°C
	Junction temperature ceramic	+150		°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## XC3100A Global Buffer Switching Characteristics Guidelines

Description	Symbol	Speed Grade		-5	-4	-3	-2	-1	-09	Units
		Max	Max	Max	Max	Max	Max	Max	Max	
<b>Global and Alternate Clock Distribution<sup>1</sup></b> Either: <b>Normal</b> IOB input pad through clock buffer to any CLB or IOB clock input Or: <b>Fast</b> (CMOS only) input pad through clock buffer to any CLB or IOB clock input	$T_{PID}$	6.8	6.5	5.6	4.7	4.3	3.9	3.1	ns	
	$T_{PIDC}$	5.4	5.1	4.3	3.7	3.5	3.1	ns		
<b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup> I to L.L. while T is Low (buffer active) (XC3100) (XC3100A) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \downarrow$ to L.L. active and valid with pair of pull-up resistors $T \uparrow$ to L.L. High with single pull-up resistor $T \uparrow$ to L.L. High with pair of pull-up resistors	$T_{IO}$	4.1	3.7	3.1					ns	
	$T_{IO}$	3.6	3.6	3.1	3.1	2.9	2.1	ns		
	$T_{ON}$	5.6	5.0	4.2	4.2	4.0	3.1	ns		
	$T_{ON}$	7.1	6.5	5.7	5.7	5.5	4.6	ns		
	$T_{PUS}$	15.6	13.5	11.4	11.4	10.4	8.9	ns		
	$T_{PUF}$	12.0	10.5	8.8	8.1	7.1	5.9	ns		
<b>BIDI</b> Bidirectional buffer delay	$T_{BIDI}$	1.4	1.2	1.0	0.9	0.85	0.75	ns		
									Prelim	

**Note:** 1. Timing is based on the XC3142A, for other devices see XACT timing calculator.

The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid design option for XC3100A devices.

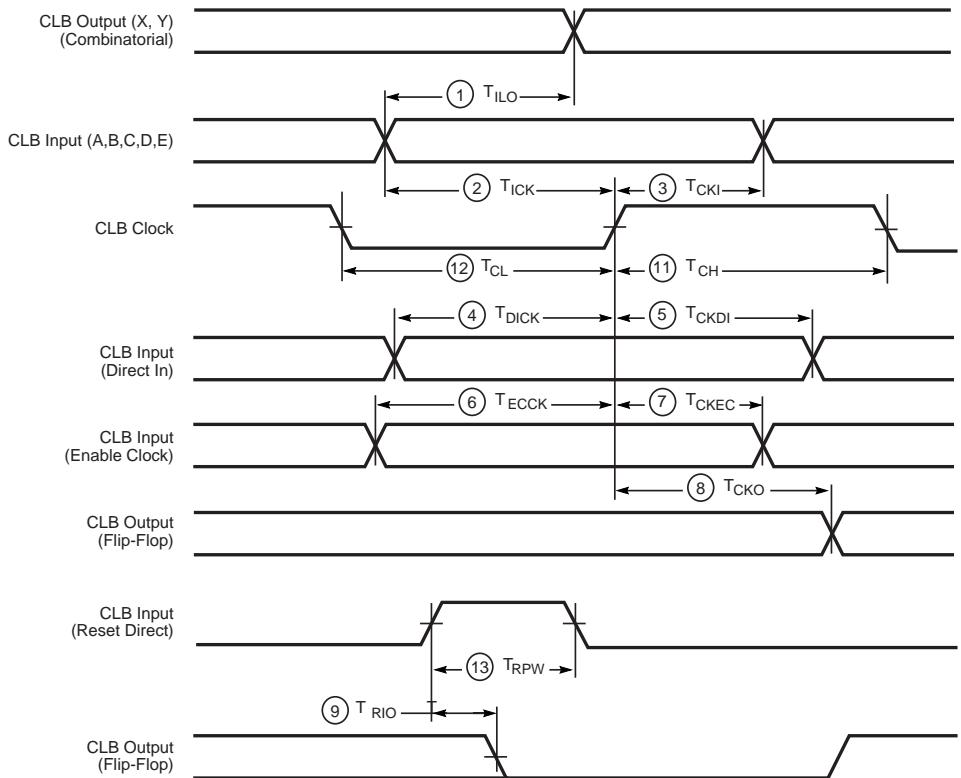
## XC3100A CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-5		-4		-3		-2		-1		-09		Units	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y	1 T <sub>ILO</sub>			4.1		3.3		2.7		2.2		1.75		1.5 ns	
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y	8 T <sub>CKO</sub> T <sub>QLO</sub>			3.1		2.5		2.1		1.7		1.4		1.25 ns	
Set-up time before clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC Reset Direct inactive RD	2 T <sub>ICK</sub> 4 T <sub>DICK</sub> 6 T <sub>ECCK</sub>	3.1 2.0 3.8 1.0		2.5 1.6 3.2 1.0		2.1 1.4 2.7 1.0		1.8 1.3 2.5 1.0		1.7 1.2 2.3 1.0		1.5 1.0 2.05 1.0		ns	
Hold Time after clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC	3 T <sub>CKI</sub> 5 T <sub>CKDI</sub> 7 T <sub>CKEC</sub>	0 1.0 1.0		0 1.0 0.8		0 0.9 0.7		0 0.9 0.7		0 0.8 0.6		0 0.7 0.55		ns ns ns	
Clock Clock High time Clock Low time Max. flip-flop toggle rate	11 T <sub>CH</sub> 12 T <sub>CL</sub> F <sub>CLK</sub>	2.4 2.4 188		2.0 2.0 227		1.6 1.6 270		1.3 1.3 323		1.3 1.3 323		1.3 1.3 370		ns ns MHz	
Reset Direct (RD) RD width delay from RD to outputs X or Y	13 T <sub>RPW</sub> 9 T <sub>TRIO</sub>	3.8		4.4	3.2		3.7	2.7		3.1	2.3	2.7	2.3	2.05 2.15	ns ns
Global Reset (RESET Pad) <sup>1</sup> RESET width (Low) (XC3142A) delay from RESET pad to outputs X or Y	T <sub>MRW</sub> T <sub>MRQ</sub>	14.0		17.0	14.0	14.0		12.0	12.0	12.0	12.0	12.0	12.0	12.0 12.0	ns ns

Prelim

- Notes:**
1. The CLB K to Q output delay (T<sub>CKO</sub>, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T<sub>CKDI</sub>, #5) of any CLB on the same die.
  2. T<sub>ILO</sub>, T<sub>QLO</sub> and T<sub>ICK</sub> are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100A family increases by 0.50 ns (-5), 0.42 ns (-4) and 0.35 ns (-3), 0.35 ns (-2), 0.30 ns (-1), and 0.30 ns (-09).

**XC3100A CLB Switching Characteristics Guidelines (continued)**

X5424

## XC3100A IOB Switching Characteristics Guidelines

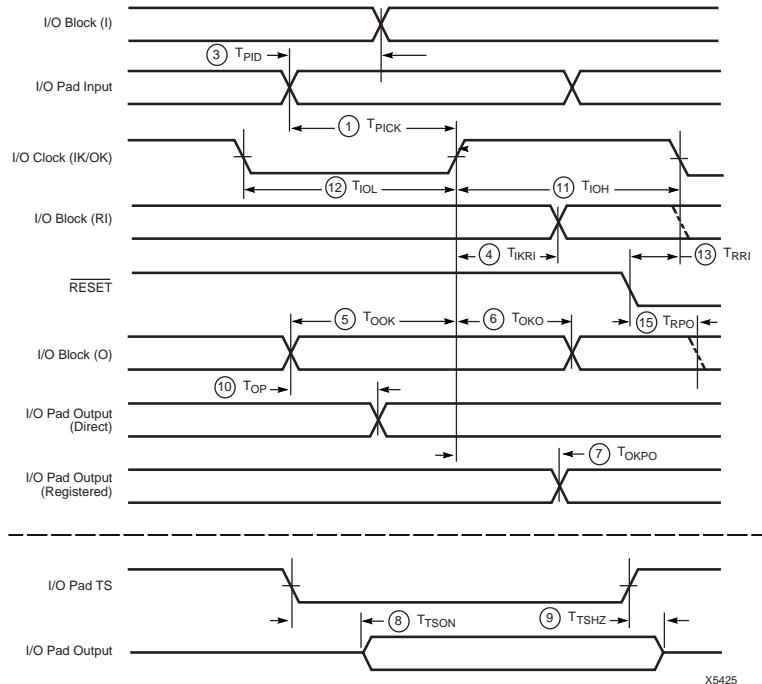
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-5		-4		-3		-2		-1		-09		Units
Description	Symbol	Min	Max											
Propagation Delays (Input)														
Pad to Direct In (I)	3 T <sub>PID</sub>			2.8		2.5		2.2		2.0		1.7		1.55 ns
Pad to Registered In (Q) with latch transparent (XC3100A)	4 T <sub>PTG</sub>			14.0		12.0		11.0		11.0		10.0		9.2 ns
Clock (IK) to Registered In (Q)	T <sub>IKRI</sub>	2.8		2.5		2.2		1.9		1.7		1.55		ns
Set-up Time (Input)														
Pad to Clock (IK) set-up time	1 T <sub>PICK</sub>	10.9		10.6		9.4		8.9		8.0		7.2		ns
XC3120A, XC3130A		11.0		10.7		9.5		9.0		8.1		7.3		ns
XC3142A		11.2		11.0		9.7		9.2		8.3		7.5		ns
XC3164A		11.5		11.2		9.9		9.4		8.5		7.7		ns
XC3190A		12.0		11.6		10.3		9.8		8.9		8.1		ns
XC3195A														
Propagation Delays (Output)														
Clock (OK) to Pad (fast)	7 T <sub>OKPO</sub>			5.5		5.0		4.4		3.7		3.4		3.3 ns
same (slew rate limited)	7 T <sub>OKPO</sub>			14.0		12.0		10.0		9.7		8.4		6.9 ns
Output (O) to Pad (fast)	10 T <sub>OPF</sub>			4.1		3.7		3.3		3.0		3.0		2.9 ns
same (slew-rate limited)														
(XC3100A)														
3-state to Pad	10 T <sub>OPS</sub>			12.1		11.0		9.0		8.7		8.0		6.5 ns
begin hi-Z (fast)	9 T <sub>TSHZ</sub>			6.9		6.2		5.5		5.0		4.5		4.05 ns
same (slew-rate limited)	9 T <sub>TSHZ</sub>			6.9		6.2		5.5		5.0		4.5		4.05 ns
3-state to Pad	8 T <sub>TS0N</sub>			10.0		10.0		9.0		8.5		6.5		5.0 ns
active and valid (fast) (XC3100A)				18.0		17.0		15.0		14.2		11.5		8.6 ns
same (slew-rate limited)	8 T <sub>TS0N</sub>													
Set-up and Hold Times (Output)														
Output (O) to clock (OK) set-up time	5 T <sub>OOK</sub>	5.0		4.5										ns
(XC3100A)	6 T <sub>OKO</sub>	0		0										ns
Output (O) to clock (OK) hold time														
Clock														
Clock High time	11 T <sub>IOH</sub>			2.4		2.0		1.6		1.3		1.3		ns
Clock Low time	12 T <sub>IOL</sub>			2.4		2.0		1.6		1.3		1.3		ns
Max. flip-flop toggle rate	F <sub>CLK</sub>	188		227		270		323		323		370		MHz
Global Reset Delays														
RESET Pad to Registered In (Q)	13 T <sub>RRI</sub>			18.0		15.0		13.0		13.0		13.0		14.4 ns
(XC3142A)				29.5		25.5		21.0		21.0		21.0		ns
(XC3190A)				32.0		27.0		23.0		23.0		22.0		ns
RESET Pad to output pad (fast)	15 T <sub>RP0</sub>			24.0		20.0		17.0		17.0		17.0		17.0 ns
(slew-rate limited)	15 T <sub>RP0</sub>													

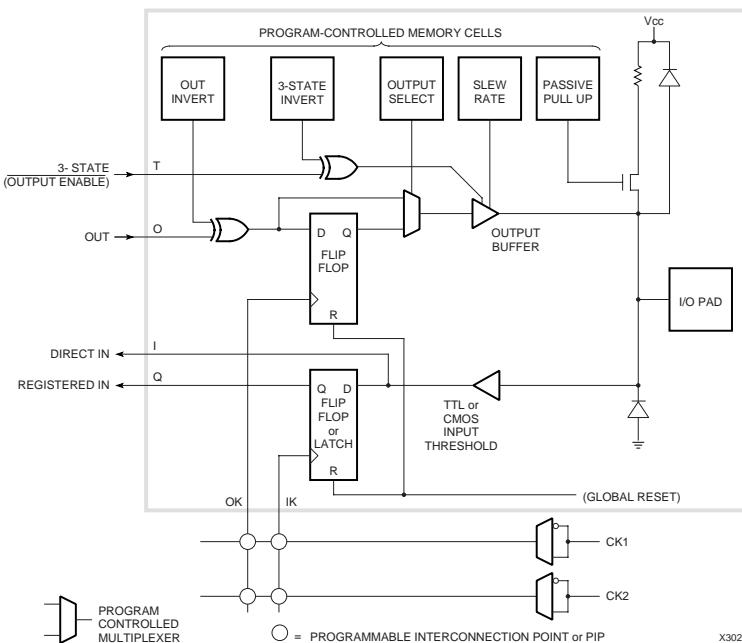
Preliminary

- Notes:**
- Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see page XAPP024. Typical slew rate limited output rise/fall times are approximately four times longer.
  - Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  - Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
  - T<sub>PID</sub>, T<sub>PTG</sub>, and T<sub>PICK</sub> are 3 ns higher for XTL2 when the pin is configured as a user input.

## XC3100A IOB Switching Characteristics Guidelines (continued)



X5425



X3029

## XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
$V_{IH}$	High-level input voltage	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Low-level input voltage	-0.3	0.8	V
$T_{IN}$	Input signal transition time		250	ns

- Notes:**
- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
  - Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V  $V_{CC}$  range.

### XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)	2.4		V
	High-level output voltage (@ $I_{OH} = -100.0$ $\mu$ A, $V_{CC}$ min)	$V_{CC} - 0.2$		V
$V_{OL}$	Low-level output voltage (@ $I_{OH} = 4.0$ mA, $V_{CC}$ min)		0.40	V
	Low-level output voltage (@ $I_{OH} = +100.0$ $\mu$ A, $V_{CC}$ min)		0.2	V
$V_{CCPD}$	Power-down supply voltage (PWRDWN must be Low)	2.30		V
$I_{CC0}$	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels <sup>1</sup>		1.5	mA
$I_{IL}$	Input Leakage Current	-10	+10	$\mu$ A
$C_{IN}$	Input capacitance, all packages except PGA175 (sample tested)			
	All pins except XTL1 and XTL2		10	pF
	XTL1 and XTL2		15	pF
	Input capacitance, PGA175 (sample tested)			
	All pins except XTL1 and XTL2		15	pF
	XTL1 and XTL2		20	pF
$I_{RIN}$	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)	0.02	0.17	mA
$I_{RLL}$	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

- Notes:**
- With no output current loads, no active input or long line pull-up resistors, all package pins at  $V_{CC}$  or GND, and the FPGA configured with a MakeBits tie option.
  - Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per  $V_{CC}$  pin. The number of ground pins varies from the XC3142L to the XC3190L.

## XC3100L Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
$T_J$	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## XC3100L Global Buffer Switching Characteristics Guidelines

Description	Symbol	Speed Grade		Units
		-3	-2	
<b>Global and Alternate Clock Distribution<sup>1</sup></b> Either: <b>Normal</b> IOB input pad through clock buffer to any CLB or IOB clock input Or: <b>Fast</b> (CMOS only) input pad through clock buffer to any CLB or IOB clock input	$T_{PID}$	5.6	4.7	ns
	$T_{PIDC}$	4.3	3.7	ns
<b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup> I to L.L. while T is Low (buffer active) $T \downarrow$ to L.L. active and valid with single pull-up resistor $T \uparrow$ to L.L. High with single pull-up resistor	$T_{IO}$ $T_{ON}$ $T_{PUS}$	3.1 4.2 11.4	3.1 4.2 11.4	ns ns ns
<b>BIDI</b> Bidirectional buffer delay	$T_{BIDI}$	1.0	0.9	ns
		Advance		

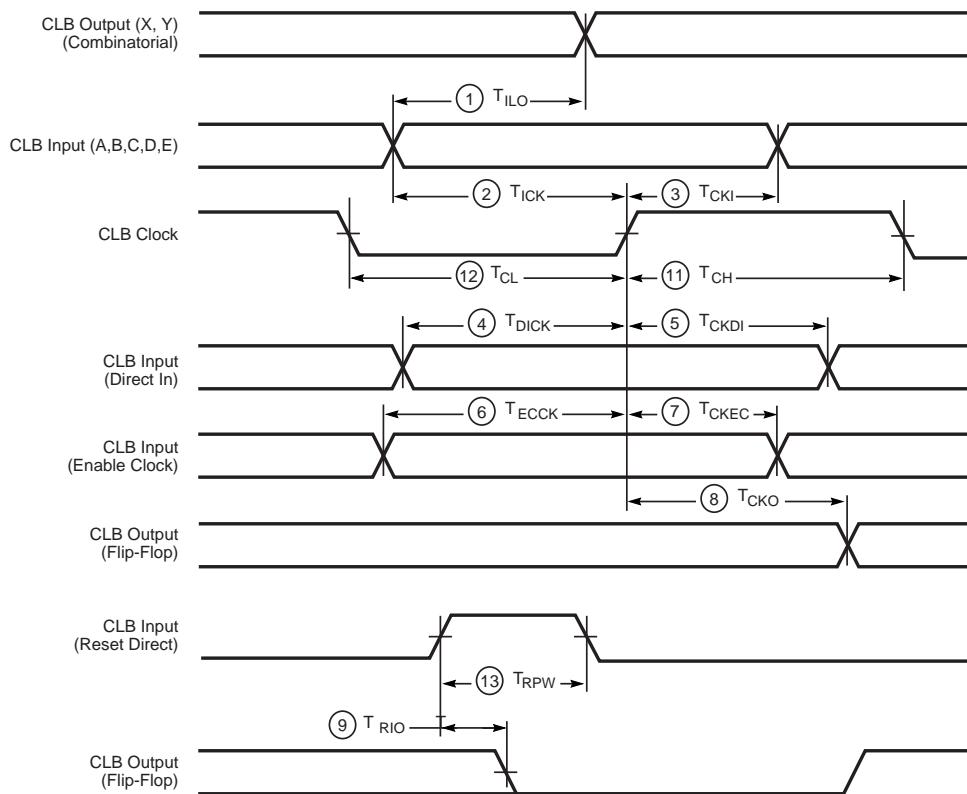
**Notes:** 1. Timing is based on the XC3142L, for other devices see XACT timing calculator.  
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

## XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-3	-2			
Description	Symbol		Min	Max	Min	Max	Units
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y	1	$T_{ILO}$		2.7		2.2	ns
Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y	8	$T_{CKO}$		2.1		1.7	ns
		$T_{QLO}$		4.3		3.5	ns
Set-up time before clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC Reset Direct Inactive RD	2 4 6	$T_{ICK}$ $T_{DICK}$ $T_{ECCK}$	2.1 1.4 2.7 1.0		1.8 1.3 2.5 1.0		ns ns ns ns
Hold Time after clock K Logic Variables A, B, C, D, E Data In DI Enable Clock EC	3 5 7	$T_{CKI}$ $T_{CKDI}$ $T_{CKEC}$	0 0.9 0.7		0 0.9 0.7		ns ns ns
Clock Clock High time Clock Low time Max. flip-flop toggle rate	11 12	$T_{CH}$ $T_{CL}$ $F_{CLK}$	1.6 1.6 270		1.3 1.3 325		ns ns MHz
Reset Direct (RD) RD width delay from RD to outputs X or Y	13 9	$T_{RPW}$ $T_{RIO}$	2.7	3.1	2.3	2.7	ns ns
Global Reset (RESET Pad) RESET width (Low) (XC3142L) delay from RESET pad to outputs X or Y		$T_{MRW}$ $T_{MRQ}$	12.0	12.0	12.0	12.0	ns ns
<b>Advance</b>							

- Notes:
1. The CLB K to Q delay ( $T_{CKO}$ , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement ( $T_{CKDI}$ , #5) of any CLB on the same die.
  2.  $T_{ILO}$ ,  $T_{QLO}$  and  $T_{ICK}$  are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

**XC3100L CLB Switching Characteristics Guidelines (continued)**

X5424

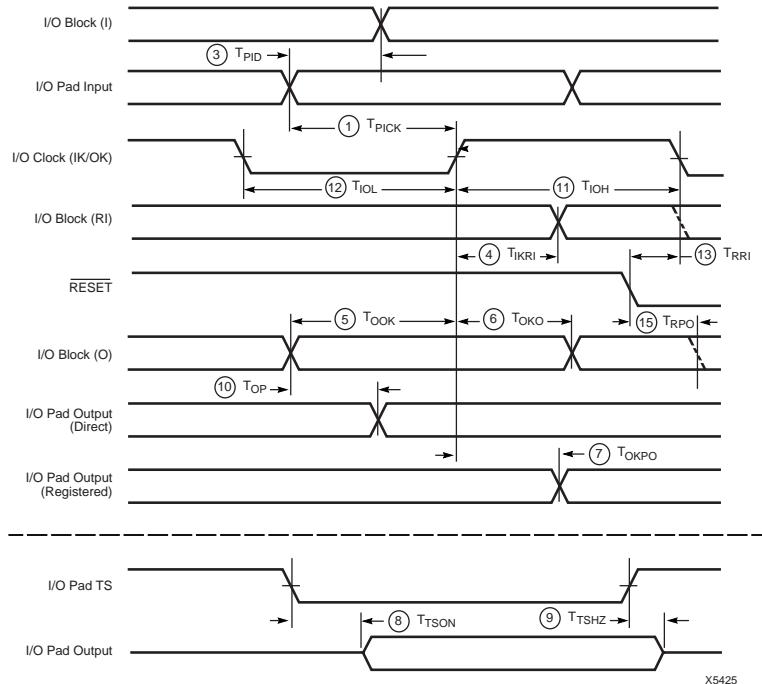
## XC3100L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

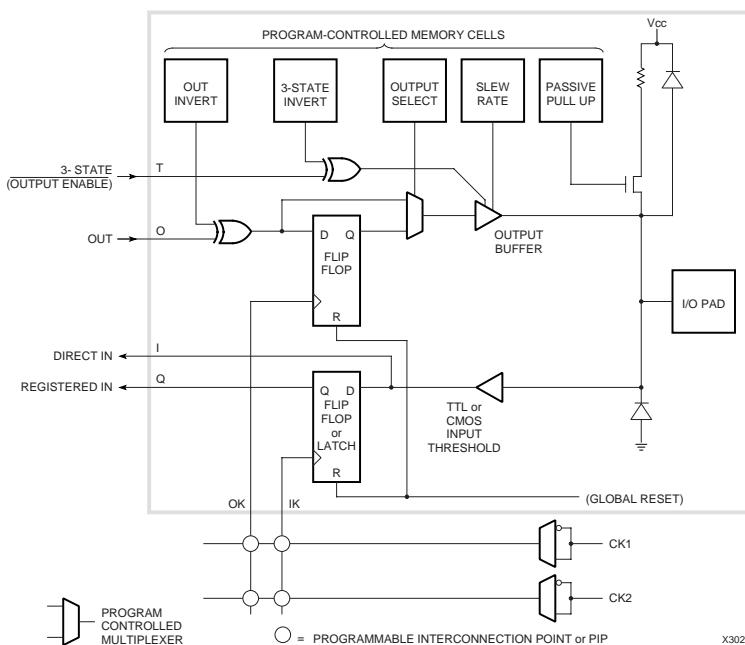
Speed Grade			-3	-2			
Description	Symbol		Min	Max	Min	Max	Units
Propagation Delays (Input)							
Pad to Direct In (I)	3	T <sub>PID</sub>		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		T <sub>PTG</sub>		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	T <sub>IKRI</sub>		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T <sub>PICK</sub>					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	T <sub>OKPO</sub>	T <sub>OK</sub>	4.4		4.0	ns
same (slew rate limited)	7	T <sub>PO</sub>		10.0		9.7	ns
Output (O) to Pad (fast)	10	T <sub>OPF</sub>		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	T <sub>OPF</sub>		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	T <sub>TSHZ</sub>		5.5		5.0	ns
same (slew-rate limited)	9	T <sub>TSHZ</sub>		5.5		5.0	ns
3-state to Pad active and valid(fast)(XC3100L)	8	T <sub>TS0N</sub>		9.0		8.5	ns
same (slew -rate limited)	8	T <sub>TS0N</sub>		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	T <sub>OOK</sub>		4.0		3.6	ns
Output (O) to clock (OK) hold time	6	T <sub>OKO</sub>		0		0	ns
Clock							
Clock High time	11	T <sub>I0H</sub>		1.6		1.3	ns
Clock Low time	12	T <sub>I0L</sub>		1.6		1.3	ns
Export Control Maximum flip-flop toggle rate		F <sub>TOG</sub>		270		325	MHz
Global Reset Delays							
RESET Pad to Registered In (Q) (XC3142L) (XC3190L)	13	T <sub>RRI</sub>		16.0		16.0	ns
RESET Pad to output pad (fast) (slew-rate limited)	15	T <sub>RPO</sub>		21.0		21.0	ns
	15	T <sub>RPO</sub>		17.0		17.0	ns
				23.0		23.0	ns
<b>Advance</b>							

- Notes:**
- Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  - Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  - Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

## XC3100L IOB Switching Characteristics Guidelines (continued)



X5425



X3029

## XC3000 Series Pin Assignments

Xilinx offers the six different array sizes in the XC3000 families in a variety of surface-mount and through-hole package types, with pin counts from 44 to 223.

Each chip is offered in several package types to accommodate the available PC board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without the need for PC board changes.

Note that there is no perfect match between the number of bonding pads on the chip and the number of pins on a package. In some cases, the chip has more pads than there are pins on the package, as indicated by the information ("unused" pads) below the line in the following table. The IOBs of the unconnected pads can still be used as storage elements if the specified propagation delays and set-up times are acceptable.

In other cases, the chip has fewer pads than there are pins on the package; therefore, some package pins are not connected (n.c.), as shown above the line in the following table.

### XC3000 Series 44-Pin PLCC Pinouts

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	GND
2	I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	PWRDWN
8	TCLKIN-I/O
9	I/O
10	I/O
11	I/O
12	VCC
13	I/O
14	I/O
15	I/O
16	M1-RDATA
17	M0-RTRIG
18	M2-I/O
19	HDC-I/O
20	LDC-I/O
21	I/O
22	INIT-I/O

Pin No.	XC3030A
23	GND
24	I/O
25	I/O
26	XTL2(IN)-I/O
27	RESET
28	DONE-PGM
29	I/O
30	XTL1(OUT)-BCLK-I/O
31	I/O
32	I/O
33	I/O
34	VCC
35	I/O
36	I/O
37	I/O
38	DIN-I/O
39	DOUT-I/O
40	CCLK
41	I/O
42	I/O
43	I/O
44	I/O

Peripheral mode and Master Parallel mode are not supported in the PC44 package

**XC3000 Series 64-Pin Plastic VQFP Pinouts**

XC3000A, XC3000L, and XC3100A families have identical pinouts

Pin No.	XC3030A
1	A0-WS-I/O
2	A1-CS2-I/O
3	A2-I/O
4	A3-I/O
5	A4-I/O
6	A14-I/O
7	A5-I/O
8	<b>GND</b>
9	A13-I/O
10	A6-I/O
11	A12-I/O
12	A7-I/O
13	A11-I/O
14	A8-I/O
15	A10-I/O
16	A9-I/O
17	PWRDN
18	TCLKIN-I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	<b>VCC</b>
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG

Pin No.	XC3030A
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	$\overline{\text{INIT}}$ -I/O
41	<b>GND</b>
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	XTAL2(IN)-I/O
48	$\overline{\text{RESET}}$
49	DONE-PG
50	D7-I/O
51	XTAL1(OUT)-BCLKIN-I/O
52	D6-I/O
53	D5-I/O
54	$\overline{\text{CS0}}$ -I/O
55	D4-I/O
56	VCC
57	D3-I/O
58	$\overline{\text{CS1}}$ -I/O
59	D2-I/O
60	D1-I/O
61	RDY/BUSY-RCLK-I/O
62	D0-DIN-I/O
63	DOUT-I/O
64	CCLK

## XC3000 Series 68-Pin PLCC, 84-Pin PLCC and PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA
XC3030A	XC3020A			
10	10	PWRDN	12	B2
11	11	TCLKIN-I/O	13	C2
12	—	I/O*	14	B1
13	12	I/O	15	C1
14	13	I/O	16	D2
—	—	I/O	17	D1
15	14	I/O	18	E3
16	15	I/O	19	E2
—	16	I/O	20	E1
17	17	I/O	21	F2
18	18	VCC	22	F3
19	19	I/O	23	G3
—	—	I/O	24	G1
20	20	I/O	25	G2
—	21	I/O	26	F1
21	22	I/O	27	H1
22	—	I/O	28	H2
23	23	I/O	29	J1
24	24	I/O	30	K1
25	25	M1-RDATA	31	J2
26	26	M0-RTRIG	32	L1
27	27	M2-I/O	33	K2
28	28	HDC-I/O	34	K3
29	29	I/O	35	L2
30	30	LD <sup>C</sup> -I/O	36	L3
—	31	I/O	37	K4
—	—	I/O*	38	L4
31	32	I/O	39	J5
32	33	I/O	40	K5
33	—	I/O*	41	L5
34	34	INIT-I/O	42	K6
35	35	GND	43	J6
36	36	I/O	44	J7
37	37	I/O	45	L7
38	38	I/O	46	K7
39	39	I/O	47	L6
—	40	I/O	48	L8
—	41	I/O	49	K8
40	—	I/O*	50	L9
41	—	I/O*	51	L10
42	42	I/O	52	K9
43	43	XTL2(IN)-I/O	53	L11

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC	84 PGA
XC3030A	XC3020A			
44	44	RESET	54	K10
45	45	DONE-PG	55	J10
46	46	D7-I/O	56	K11
47	47	XTL1(OUT)-BCLKIN-I/O	57	J11
48	48	D6-I/O	58	H10
—	—	I/O	59	H11
49	49	D5-I/O	60	F10
50	50	CS0-I/O	61	G10
51	51	D4-I/O	62	G11
—	—	I/O	63	G9
52	52	VCC	64	F9
53	53	D3-I/O	65	F11
54	54	CS1-I/O	66	E11
55	55	D2-I/O	67	E10
—	—	I/O	68	E9
—	—	I/O*	69	D11
56	56	D1-I/O	70	D10
57	57	RDY/BUSY-RCLK-I/O	71	C11
58	58	D0-DIN-I/O	72	B11
59	59	DOUT-I/O	73	C10
60	60	CCLK	74	A11
61	61	A0-WS-I/O	75	B10
62	62	A1-CS2-I/O	76	B9
63	63	A2-I/O	77	A10
64	64	A3-I/O	78	A9
—	—	I/O*	79	B8
—	—	I/O*	80	A8
65	65	A15-I/O	81	B6
66	66	A4-I/O	82	B7
67	67	A14-I/O	83	A7
68	68	A5-I/O	84	C7
1	1	GND	1	C6
2	2	A13-I/O	2	A6
3	3	A6-I/O	3	A5
4	4	A12-I/O	4	B5
5	5	A7-I/O	5	C5
—	—	I/O*	6	A4
—	—	I/O*	7	B4
6	6	A11-I/O	8	A3
7	7	A8-I/O	9	A2
8	8	A10-I/O	10	B3
9	9	A9-I/O	11	A1

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

This table describes the pinouts of three different chips in three different packages. The pin-description column lists 84 of the 118 pads on the XC3042A (and 84 of the 98 pads on the XC3030A) that are connected to the 84 package pins. Ten pads, indicated by an asterisk, do not exist on the XC3020A, which has 74 pads; therefore the corresponding pins on the 84-pin packages have no connections to an XC3020A. Six pads on the XC3020A and 16 pads on the XC3030A, indicated by a dash (—) in the 68 PLCC column, have no connection to the 68 PLCC, but are connected to the 84-pin packages.

**XC3064A/XC3090A/XC3195A 84-Pin PLCC Pinouts**

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PLCC Pin Number	XC3064A, XC3090A, XC3195A
12	PWRDN
13	TCLKIN-I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	GND*
22	VCC
23	I/O
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	M1-RDATA
32	M0-RTRIG
33	M2-I/O
34	HDC-I/O
35	I/O
36	LDC-I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	INIT/I/O*
42	VCC*
43	GND
44	I/O
45	I/O
46	I/O
47	I/O
48	I/O
49	I/O
50	I/O
51	I/O
52	I/O
53	XTL2(IN)-I/O

PLCC Pin Number	XC3064A, XC3090A, XC3195A
54	RESET
55	DONE- $\overline{PG}$
56	D7-I/O
57	XTL1(OUT)-BCLKIN-I/O
58	D6-I/O
59	I/O
60	D5-I/O
61	$\overline{CS0}$ -I/O
62	D4-I/O
63	I/O
64	VCC
65	GND*
66	D3-I/O*
67	$\overline{CS1}$ -I/O*
68	D2-I/O*
69	I/O
70	D1-I/O
71	RDY/BUSY-RCLK-I/O
72	D0-DIN-I/O
73	DOUT-I/O
74	CCLK
75	A0- $\overline{WS}$ -I/O
76	A1-CS2-I/O
77	A2-I/O
78	A3-I/O
79	I/O
80	I/O
81	A15-I/O
82	A4-I/O
83	A14-I/O
84	A5-I/O
1	GND
2	VCC*
3	A13-I/O*
4	A6-I/O*
5	A12-I/O*
6	A7-I/O*
7	I/O
8	A11-I/O
9	A8-I/O
10	A10-I/O
11	A9-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

\* In the PC84 package, XC3064A, XC3090A and XC3195A have additional VCC and GND pins and thus a different pin definition than XC3020A/XC3030A/XC3042A.

## XC3000 Series 100-Pin QFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin No.		XC3020A		Pin No.		XC3020A		Pin No.		XC3020A		
CQFP	PQFP	TQFP	VQFP	CQFP	PQFP	TQFP	VQFP	CQFP	PQFP	TQFP	VQFP	
1	16	13		GND	35	50	47	I/O*	69	84	81	I/O*
2	17	14		A13-I/O	36	51	48	I/O*	70	85	82	I/O*
3	18	15		A6-I/O	37	52	49	M1-RD	71	86	83	I/O
4	19	16		A12-I/O	38	53	50	GND*	72	87	84	D5-I/O
5	20	17		A7-I/O	39	54	51	MO-RT	73	88	85	CS0-I/O
6	21	18		I/O*	40	55	52	VCC*	74	89	86	D4-I/O
7	22	19		I/O*	41	56	53	M2-I/O	75	90	87	I/O
8	23	20		A11-I/O	42	57	54	HDC-I/O	76	91	88	VCC
9	24	21		A8-I/O	43	58	55	I/O	77	92	89	D3-I/O
10	25	22		A10-I/O	44	59	56	LDC-I/O	78	93	90	CS1-I/O
11	26	23		A9-I/O	45	60	57	I/O*	79	94	91	D2-I/O
12	27	24		VCC*	46	61	58	I/O*	80	95	92	I/O
13	28	25		GND*	47	62	59	I/O	81	96	93	I/O*
14	29	26		PWRDN	48	63	60	I/O	82	97	94	I/O*
15	30	27		TCLKIN-I/O	49	64	61	I/O	83	98	95	D1-I/O
16	31	28		I/O**	50	65	62	INIT-I/O	84	99	96	RDY/BUSY-RCLK-I/O
17	32	29		I/O*	51	66	63	GND	85	100	97	DO-DIN-I/O
18	33	30		I/O*	52	67	64	I/O	86	1	98	DOUT-I/O
19	34	31		I/O	53	68	65	I/O	87	2	99	CCLK
20	35	32		I/O	54	69	66	I/O	88	3	100	VCC*
21	36	33		I/O	55	70	67	I/O	89	4	1	GND*
22	37	34		I/O	56	71	68	I/O	90	5	2	AO-W\$-I/O
23	38	35		I/O	57	72	69	I/O	91	6	3	A1-CS2-I/O
24	39	36		I/O	58	73	70	I/O	92	7	4	I/O**
25	40	37		I/O	59	74	71	I/O*	93	8	5	A2-I/O
26	41	38		VCC	60	75	72	I/O*	94	9	6	A3-I/O
27	42	39		I/O	61	76	73	XTL2-I/O	95	10	7	I/O*
28	43	40		I/O	62	77	74	GND*	96	11	8	I/O*
29	44	41		I/O	63	78	75	RESET	97	12	9	A15-I/O
30	45	42		I/O	64	79	76	VCC*	98	13	10	A4-I/O
31	46	43		I/O	65	80	77	DONE- $\bar{PG}$	99	14	11	A14-I/O
32	47	44		I/O	66	81	78	D7-I/O	100	15	12	A5-I/O
33	48	45		I/O	67	82	79	BCLKIN-XTL1-I/O				
34	49	46		I/O	68	83	80	D6-I/O				

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

\* This table describes the pinouts of three different chips in three different packages. The pin-description column lists 100 of the 118 pads on the XC3042A that are connected to the 100 package pins. Two pads, indicated by double asterisks, do not exist on the XC3030A, which has 98 pads; therefore the corresponding pins have no connections. Twenty-six pads, indicated by single or double asterisks, do not exist on the XC3020A, which has 74 pads; therefore, the corresponding pins have no connections. (See table on [page 383](#).)

**XC3000 Series 132-Pin Ceramic and Plastic PGA Pinouts**

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

<b>PGA Pin Number</b>	<b>XC3042A XC3064A</b>						
C4	GND	B13	M1- <u>RD</u>	P14	<u>RESET</u>	M3	DOUT-I/O
A1	PWRDN	C11	GND	M11	VCC	P1	CCLK
C3	I/O-TCLKIN	A14	M0-RT	N13	<u>DONE-PG</u>	M4	VCC
B2	I/O	D12	VCC	M12	D7-I/O	L3	GND
B3	I/O	C13	M2-I/O	P13	XTL1-I/O-BCLKIN	M2	A0-WS-I/O
A2	I/O*	B14	HDC-I/O	N12	I/O	N1	A1-CS2-I/O
B4	I/O	C14	I/O	P12	I/O	M1	I/O
C5	I/O	E12	I/O	N11	D6-I/O	K3	I/O
A3	I/O*	D13	I/O	M10	I/O	L2	A2-I/O
A4	I/O	D14	<u>LDC</u> -I/O	P11	I/O*	L1	A3-I/O
B5	I/O	E13	I/O*	N10	I/O	K2	I/O
C6	I/O	F12	I/O	P10	I/O	J3	I/O
A5	I/O	E14	I/O	M9	D5-I/O	K1	A15-I/O
B6	I/O	F13	I/O	N9	<u>CS0</u> -I/O	J2	A4-I/O
A6	I/O	F14	I/O	P9	I/O*	J1	I/O*
B7	I/O	G13	I/O	P8	I/O*	H1	A14-I/O
C7	GND	G14	<u>INIT</u> -I/O	N8	D4-I/O	H2	A5-I/O
C8	VCC	G12	VCC	P7	I/O	H3	GND
A7	I/O	H12	GND	M8	VCC	G3	VCC
B8	I/O	H14	I/O	M7	GND	G2	A13-I/O
A8	I/O	H13	I/O	N7	D3-I/O	G1	A6-I/O
A9	I/O	J14	I/O	P6	<u>CS1</u> -I/O	F1	I/O*
B9	I/O	J13	I/O	N6	I/O*	F2	A12-I/O
C9	I/O	K14	I/O	P5	I/O*	E1	A7-I/O
A10	I/O	J12	I/O	M6	D2-I/O	F3	I/O
B10	I/O	K13	I/O	N5	I/O	E2	I/O
A11	I/O*	L14	I/O*	P4	I/O	D1	A11-I/O
C10	I/O	L13	I/O	P3	I/O	D2	A8-I/O
B11	I/O	K12	I/O	M5	D1-I/O	E3	I/O
A12	I/O*	M14	I/O	N4	RDY/BUSY-RCLK-I/O	C1	I/O
B12	I/O	N14	I/O	P2	I/O	B1	A10-I/O
A13	I/O*	M13	XTL2(IN)-I/O	N3	I/O	C2	A9-I/O
C12	I/O	L12	GND	N2	D0-DIN-I/O	D3	VCC

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

\*Indicates unconnected package pins (14) for the XC3042A.

## XC3000 Series 144-Pin Plastic TQFP Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A	Pin Number	XC3042A XC3064A XC3090A
1	PWRDN	49	I/O	97	I/O
2	I/O-TCLKIN	50	I/O*	98	I/O
3	I/O*	51	I/O	99	I/O*
4	I/O	52	I/O	100	I/O
5	I/O	53	INIT-I/O	101	I/O*
6	I/O*	54	VCC	102	D1-I/O
7	I/O	55	GND	103	RDY/BUSY-RCLK-I/O
8	I/O	56	I/O	104	I/O
9	I/O*	57	I/O	105	I/O
10	I/O	58	I/O	106	D0-DIN-I/O
11	I/O	59	I/O	107	DOUT-I/O
12	I/O	60	I/O	108	CCLK
13	I/O	61	I/O	109	VCC
14	I/O	62	I/O	110	GND
15	I/O*	63	I/O*	111	A0-WSI/O
16	I/O	64	I/O*	112	A1-CS2-I/O
17	I/O	65	I/O	113	I/O
18	GND	66	I/O	114	I/O
19	VCC	67	I/O	115	A2-I/O
20	I/O	68	I/O	116	A3-I/O
21	I/O	69	XTL2(IN)-I/O	117	I/O
22	I/O	70	GND	118	I/O
23	I/O	71	RESET	119	A15-I/O
24	I/O	72	VCC	120	A4-I/O
25	I/O	73	DONE-PG	121	I/O*
26	I/O	74	D7-I/O	122	I/O*
27	I/O	75	XTL1(OUT)-BCLKIN-I/O	123	A14-I/O
28	I/O*	76	I/O	124	A5-I/O
29	I/O	77	I/O	125	I/O (XC3090 only)
30	I/O	78	D6-I/O	126	GND
31	I/O*	79	I/O	127	VCC
32	I/O*	80	I/O*	128	A13-I/O
33	I/O	81	I/O	129	A6-I/O
34	I/O*	82	I/O	130	I/O*
35	I/O	83	I/O*	131	I/O (XC3090 only)
36	M1-RD	84	D5-I/O	132	I/O*
37	GND	85	CS0-I/O	133	A12-I/O
38	MO-RT	86	I/O*	134	A7-I/O
39	VCC	87	I/O*	135	I/O
40	M2-I/O	88	D4-I/O	136	I/O
41	HDC-I/O	89	I/O	137	A11-I/O
42	I/O	90	VCC	138	A8-I/O
43	I/O	91	GND	139	I/O
44	I/O	92	D3-I/O	140	I/O
45	LDC-I/O	93	CS1-I/O	141	A10-I/O
46	I/O*	94	I/O*	142	A9-I/O
47	I/O	95	I/O*	143	VCC
48	I/O	96	D2-I/O	144	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

\* Indicates unconnected package pins (24) for the XC3042A.

**XC3000 Series 160-Pin PQFP Pinouts**

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PQFP Pin Number	XC3064A, XC3090A, XC3195A						
1	I/O*	41	GND	81	D7-I/O	121	CCLK
2	I/O*	42	M0-RTRIG	82	XTL1-I/O-BCLKIN	122	VCC
3	I/O*	43	VCC	83	I/O*	123	GND
4	I/O	44	M2-I/O	84	I/O	124	A0-W <sub>S</sub> -I/O
5	I/O	45	HDC-I/O	85	I/O	125	A1-CS2-I/O
6	I/O	46	I/O	86	D6-I/O	126	I/O
7	I/O	47	I/O	87	I/O	127	I/O
8	I/O	48	I/O	88	I/O	128	A2-I/O
9	I/O	49	LDC-I/O	89	I/O	129	A3-I/O
10	I/O	50	I/O*	90	I/O	130	I/O
11	I/O	51	I/O*	91	I/O	131	I/O
12	I/O	52	I/O	92	D5-I/O	132	A15-I/O
13	I/O	53	I/O	93	CS0-I/O	133	A4-I/O
14	I/O	54	I/O	94	I/O*	134	I/O
15	I/O	55	I/O	95	I/O*	135	I/O
16	I/O	56	I/O	96	I/O	136	A14-I/O
17	I/O	57	I/O	97	I/O	137	A5-I/O
18	I/O	58	I/O	98	D4-I/O	138	I/O*
19	GND	59	INIT-I/O	99	I/O	139	GND
20	VCC	60	VCC	100	VCC	140	VCC
21	I/O*	61	GND	101	GND	141	A13-I/O
22	I/O	62	I/O	102	D3-I/O	142	A6-I/O
23	I/O	63	I/O	103	CS1-I/O	143	I/O*
24	I/O	64	I/O	104	I/O	144	I/O*
25	I/O	65	I/O	105	I/O	145	I/O
26	I/O	66	I/O	106	I/O*	146	I/O
27	I/O	67	I/O	107	I/O*	147	A12-I/O
28	I/O	68	I/O	108	D2-I/O	148	A7-I/O
29	I/O	69	I/O	109	I/O	149	I/O
30	I/O	70	I/O	110	I/O	150	I/O
31	I/O	71	I/O	111	I/O	151	A11-I/O
32	I/O	72	I/O	112	I/O	152	A8-I/O
33	I/O	73	I/O	113	I/O	153	I/O
34	I/O	74	I/O	114	D1-I/O	154	I/O
35	I/O	75	I/O*	115	RDY/BUSY-RCLK-I/O	155	A10-I/O
36	I/O	76	XTL2-I/O	116	I/O	156	A9-I/O
37	I/O	77	GND	117	I/O	157	VCC
38	I/O*	78	RESET	118	I/O*	158	GND
39	I/O*	79	VCC	119	D0-DIN-I/O	159	PWRDW <sub>N</sub>
40	M1-RDATA	80	DONE/PG	120	DOUT-I/O	160	TCLKIN-I/O

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed IOBs are default slew-rate limited.

\*Indicates unconnected package pins (18) for the XC3064A.

## XC3000 Series 175-Pin Ceramic and Plastic PGA Pinouts

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

PGA Pin Number	XC3090A, XC3195A
B2	PWRDN
D4	TCLKIN-I/O
B3	I/O
C4	I/O
B4	I/O
A4	I/O
D5	I/O
C5	I/O
B5	I/O
A5	I/O
C6	I/O
D6	I/O
B6	I/O
A6	I/O
B7	I/O
C7	I/O
D7	I/O
A7	I/O
A8	I/O
B8	I/O
C8	I/O
D8	GND
D9	VCC
C9	I/O
B9	I/O
A9	I/O
A10	I/O
D10	I/O
C10	I/O
B10	I/O
A11	I/O
B11	I/O
D11	I/O
C11	I/O
A12	I/O
B12	I/O
C12	I/O
D12	I/O
A13	I/O
B13	I/O
C13	I/O
A14	I/O

PGA Pin Number	XC3090A, XC3195A
D13	I/O
B14	M1-RDATA
C14	GND
B15	M0-RTRIG
D14	VCC
C15	M2-I/O
E14	HDC-I/O
B16	I/O
D15	I/O
C16	I/O
D16	<u>LDC</u> -I/O
F14	I/O
E15	I/O
E16	I/O
F15	I/O
F16	I/O
G14	I/O
G15	I/O
G16	I/O
H16	I/O
H15	<u>INIT</u> -I/O
H14	VCC
J14	GND
J15	I/O
J16	I/O
K16	I/O
K15	I/O
K14	I/O
L16	I/O
L15	I/O
M16	I/O
M15	I/O
L14	I/O
N16	I/O
P16	I/O
N15	I/O
R16	I/O
M14	I/O
P15	XTL2(IN)-I/O
N14	GND
R15	<u>RESET</u>
P14	VCC

PGA Pin Number	XC3090A, XC3195A
R14	DONE- <u>PG</u>
N13	D7-I/O
T14	XTL1(OUT)-BCLKIN-I/O
P13	I/O
R13	I/O
T13	I/O
N12	I/O
P12	D6-I/O
R12	I/O
T12	I/O
P11	I/O
N11	I/O
R11	I/O
T11	D5-I/O
R10	<u>CS0</u> -I/O
P10	I/O
N10	I/O
T10	I/O
T9	I/O
R9	D4-I/O
P9	I/O
N9	VCC
N8	GND
P8	D3-I/O
R8	<u>CS1</u> -I/O
T8	I/O
T7	I/O
N7	I/O
P7	I/O
R7	D2-I/O
T6	I/O
R6	I/O
N6	I/O
P6	I/O
T5	I/O
R5	D1-I/O
P5	RDY/BUSY-RCLK-I/O
N5	I/O
T4	I/O
R4	I/O
P4	I/O
R3	D0-DIN-I/O

PGA Pin Number	XC3090A, XC3195A
N4	DOUT-I/O
R2	CCLK
P3	VCC
N3	GND
P2	A0-W <u>S</u> -I/O
M3	A1-CS2-I/O
R1	I/O
N2	I/O
P1	A2-I/O
N1	A3-I/O
L3	I/O
M2	I/O
M1	A15-I/O
L2	A4-I/O
L1	I/O
K3	I/O
K2	A14-I/O
K1	A5-I/O
J1	I/O
J2	I/O
J3	GND
H3	VCC
H2	A13-I/O
H1	A6-I/O
G1	I/O
G2	I/O
G3	I/O
F1	I/O
F2	A12-I/O
E1	A7-I/O
E2	I/O
F3	I/O
D1	A11-I/O
C1	A8-I/O
D2	I/O
B1	I/O
E3	A10-I/O
C2	A9-I/O
D3	VCC
C3	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

Pins A2, A3, A15, A16, T1, T2, T3, T15 and T16 are not connected. Pin A1 does not exist.

**XC3000 Series 176-Pin TQFP Pinouts**

XC3000A, XC3000L, XC3100A, and XC3100L families have identical pinouts

Pin Number	XC3090A
1	PWRDWN
2	TCLKIN-I/O
3	I/O
4	I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	I/O
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	GND
23	VCC
24	I/O
25	I/O
26	I/O
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	I/O
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	-

Pin Number	XC3090A
45	M1-RDATA
46	GND
47	M0-RTRIG
48	VCC
49	M2-I/O
50	HDC-I/O
51	I/O
52	I/O
53	I/O
54	LDC-I/O
55	-
56	I/O
57	I/O
58	I/O
59	I/O
60	I/O
61	I/O
62	I/O
63	I/O
64	I/O
65	INIT-I/O
66	VCC
67	GND
68	I/O
69	I/O
70	I/O
71	I/O
72	I/O
73	I/O
74	I/O
75	I/O
76	I/O
77	I/O
78	I/O
79	I/O
80	I/O
81	I/O
82	-
83	-
84	I/O
85	XTAL2(IN)-I/O
86	GND
87	RESET
88	VCC

Pin Number	XC3090A
89	DONE-PG
90	D7-I/O
91	XTAL1(OUT)-BCLKIN-I/O
92	I/O
93	I/O
94	I/O
95	I/O
96	D6-I/O
97	I/O
98	I/O
99	I/O
100	I/O
101	I/O
102	D5-I/O
103	CS0-I/O
104	I/O
105	I/O
106	I/O
107	I/O
108	D4-I/O
109	I/O
110	VCC
111	GND
112	D3-I/O
113	CS1-I/O
114	I/O
115	I/O
116	I/O
117	I/O
118	D2-I/O
119	I/O
120	I/O
121	I/O
122	I/O
123	I/O
124	D1-I/O
125	RDY/BUSY-RCLK-I/O
126	I/O
127	I/O
128	I/O
129	I/O
130	D0-DIN-I/O
131	DOUT-I/O
132	CCLK

Pin Number	XC3090A
133	VCC
134	GND
135	A0-WS-I/O
136	A1-CS2-I/O
137	-
138	I/O
139	I/O
140	A2-I/O
141	A3-I/O
142	-
143	-
144	I/O
145	I/O
146	A15-I/O
147	A4-I/O
148	I/O
149	I/O
150	A14-I/O
151	A5-I/O
152	I/O
153	I/O
154	GND
155	VCC
156	A13-I/O
157	A6-I/O
158	I/O
159	I/O
160	-
161	-
162	I/O
163	I/O
164	A12-I/O
165	A7-I/O
166	I/O
167	I/O
168	-
169	A11-I/O
170	A8-I/O
171	I/O
172	I/O
173	A10-I/O
174	A9-I/O
175	VCC
176	GND

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

## XC3000 Series 208-Pin PQFP Pinouts

XC3000A, and XC3000L families have identical pinouts

Pin Number	XC3090A
1	-
2	GND
3	PWRDN
4	TCLKIN-I/O
5	I/O
6	I/O
7	I/O
8	I/O
9	I/O
10	I/O
11	I/O
12	I/O
13	I/O
14	I/O
15	-
16	I/O
17	I/O
18	I/O
19	I/O
20	I/O
21	I/O
22	I/O
23	I/O
24	I/O
25	GND
26	VCC
27	I/O
28	I/O
29	I/O
30	I/O
31	I/O
32	I/O
33	I/O
34	I/O
35	I/O
36	I/O
37	-
38	I/O
39	I/O
40	I/O
41	I/O
42	I/O
43	I/O
44	I/O
45	I/O
46	I/O
47	I/O
48	M1-RDATA
49	GND
50	M0-RTRIG
51	-
52	-

Pin Number	XC3090A
53	-
54	-
55	VCC
56	M2-I/O
57	HDC-I/O
58	I/O
59	I/O
60	I/O
61	LDC-I/O
62	I/O
63	I/O
64	-
65	-
66	-
67	-
68	I/O
69	I/O
70	I/O
71	I/O
72	-
73	-
74	I/O
75	I/O
76	I/O
77	INIT-I/O
78	VCC
79	GND
80	I/O
81	I/O
82	I/O
83	-
84	-
85	I/O
86	I/O
87	I/O
88	I/O
89	I/O
90	-
91	-
92	-
93	I/O
94	I/O
95	I/O
96	I/O
97	I/O
98	I/O
99	I/O
100	XTL2-I/O
101	GND
102	RESET
103	-
104	-

Pin Number	XC3090A
105	-
106	VCC
107	D/P
108	-
109	D7-I/O
110	XTL1-BCLKIN-I/O
111	I/O
112	I/O
113	I/O
114	I/O
115	D6-I/O
116	I/O
117	I/O
118	I/O
119	-
120	I/O
121	I/O
122	D5-I/O
123	CS0-I/O
124	I/O
125	I/O
126	I/O
127	I/O
128	D4-I/O
129	I/O
130	VCC
131	GND
132	D3-I/O
133	CS1-I/O
134	I/O
135	I/O
136	I/O
137	I/O
138	D2-I/O
139	I/O
140	I/O
141	I/O
142	-
143	I/O
144	I/O
145	D1-I/O
146	RDY/BUSY-RCLK-I/O
147	I/O
148	I/O
149	I/O
150	I/O
151	DIN-D0-I/O
152	DOUT-I/O
153	CCLK
154	VCC
155	-
156	-

Pin Number	XC3090A
157	-
158	-
159	-
160	GND
161	WS-A0-I/O
162	CS2-A1-I/O
163	I/O
164	I/O
165	A2-I/O
166	A3-I/O
167	I/O
168	I/O
169	-
170	-
171	-
172	A15-I/O
173	A4-I/O
174	I/O
175	I/O
176	-
177	-
178	A14-I/O
179	A5-I/O
180	I/O
181	I/O
182	GND
183	VCC
184	A13-I/O
185	A6-I/O
186	I/O
187	I/O
188	-
189	-
190	I/O
191	I/O
192	A12-I/O
193	A7-I/O
194	-
195	-
196	-
197	I/O
198	I/O
199	A11-I/O
200	A8-I/O
201	I/O
202	I/O
203	A10-I/O
204	A9-I/O
205	VCC
206	-
207	-
208	-

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

\*In PQ208, XC3090A and XC3195A have different pinouts.

**XC3195A PQ208 and PG223 Pinouts**

Pin Description	PG223	PQ208
A9-I/O	B1	206
A10-I/O	E3	205
I/O	E4	204
I/O	C2	203
I/O	C1	202
I/O	D2	201
A8-I/O	E2	200
A11-I/O	F4	199
I/O	F3	198
I/O	D1	197
I/O	F2	196
I/O	G2	194
A7-I/O	G4	193
A12-I/O	G1	192
I/O	H2	191
I/O	H3	190
I/O	H1	189
I/O	H4	188
I/O	J3	187
I/O	J2	186
A6-I/O	J1	185
A13-I/O	K3	184
VCC	J4	183
GND	K4	182
I/O	K2	181
I/O	K1	180
A5-I/O	L2	179
A14-I/O	L4	178
I/O	L3	177
I/O	L1	176
I/O	M1	175
I/O	M2	174
A4-I/O	M4	173
A15-I/O	N2	172
I/O	N3	171
I/O	P2	169
I/O	R1	168
I/O	N4	167
A3-I/O	T1	166
A2-I/O	R2	165
I/O	P3	164
I/O	T2	163
I/O	P4	162
I/O	U1	161
A1-CS2-I/O	V1	160
A0-W\$-I/O	T3	159
GND	R3	158
VCC	R4	157
CCLK	U2	156
DOUT-I/O	V2	155

Pin Description	PG223	PQ208
D0-DIN-I/O	U3	154
I/O	V3	153
I/O	R5	152
I/O	T4	151
I/O	V4	150
RDY/BUSY-RCLK-I/O	U4	149
D1-I/O	U5	148
I/O	R6	147
I/O	T5	146
I/O	U6	145
I/O	T6	144
I/O	V7	141
I/O	R7	140
I/O	U7	139
D2-I/O	V8	138
I/O	U8	137
I/O	T8	136
I/O	R8	135
I/O	V9	134
CS1-I/O	U9	133
D3-I/O	T9	132
GND	R9	131
VCC	R10	130
I/O	T10	129
D4-I/O	U10	128
I/O	V10	127
I/O	R11	126
I/O	T11	125
I/O	U11	124
CS0-I/O	V11	123
D5-I/O	U12	122
I/O	R12	121
I/O	V12	120
I/O	T13	119
I/O	U13	118
I/O	T14	117
I/O	R13	116
I/O	U14	115
D6-I/O	U15	114
I/O	V15	113
I/O	T15	112
I/O	R14	111
I/O	V16	110
XTLX1(OUT)BCLKN-I/O	U16	109
D7-I/O	T16	108
D/P	V17	107
VCC	R15	106
RESET	U17	105
GND	R16	104
XTL2(IN)-I/O	V18	103

Pin Description	PG223	PQ208
I/O	U18	102
I/O	P15	101
I/O	T17	100
I/O	T18	99
I/O	P16	98
I/O	R17	97
I/O	N15	96
I/O	R18	95
I/O	P17	94
I/O	N17	93
I/O	N16	92
I/O	M15	89
I/O	M18	88
I/O	M17	87
I/O	L18	86
I/O	L17	85
I/O	L15	84
I/O	L16	83
I/O	K18	82
I/O	K17	81
I/O	K16	80
GND	K15	79
VCC	J15	78
INIT	J16	77
I/O	J17	76
I/O	J18	75
I/O	H16	74
I/O	H15	73
I/O	H17	72
I/O	H18	71
I/O	G17	70
I/O	G18	69
I/O	G15	68
I/O	F16	67
I/O	F17	66
I/O	E17	63
I/O	C18	62
I/O	F15	61
I/O	D17	60
LDC-I/O	E16	59
I/O	C17	58
I/O	B18	57
I/O	E15	56
HDC-I/O	A18	55
M2-I/O	A17	54
VCC	D16	53
M0-RTIG	B17	52
GND	D15	51
M1/RDATA	C16	50
I/O	B16	49

Pin Description	PG223	PQ208
I/O	A16	48
I/O	D14	47
I/O	C15	46
I/O	B15	45
I/O	A15	44
I/O	C14	43
I/O	D13	42
I/O	B14	41
I/O	C13	40
I/O	B13	39
I/O	B12	38
I/O	D12	37
I/O	A12	36
I/O	B11	35
I/O	C11	34
I/O	A11	33
I/O	D11	32
I/O	A10	31
I/O	B10	30
I/O	C10	29
I/O	C9	28
VCC	D10	27
GND	D9	26
I/O	B9	25
I/O	A9	24
I/O	C8	23
I/O	D8	22
I/O	B8	21
I/O	A8	20
I/O	B7	19
I/O	A7	18
I/O	D7	17
I/O	B6	14
I/O	C6	13
I/O	B5	12
I/O	A4	11
I/O	D6	10
I/O	C5	9
I/O	B4	8
I/O	B3	7
I/O	C4	6
I/O	D5	5
I/O	C3	4
I/O	A3	3
TCLKIN-I/O	A2	2
PWRDN	B2	1
GND	D4	208
VCC	D3	207

Unprogrammed IOBs have a default pull-up. This prevents an undefined pad level for unbonded or unused IOBs. Programmed outputs are default slew-rate limited.

In the PQ208 package, pins 15, 16, 64, 65, 90, 91, 142, 143, 170 and 195 are not connected.

In the PG223 package, the following pins are not connected: A5, A6, A13, A14, D18, E1, E18, F1, F18, N1, N18, P1, P18, V5, V6, V13, and V14.

\*In PQ208, XC3090A and XC3195A have different pinouts.

## Product Availability

Pins		44	64	68	84		100					132			144	160	164	175			176	208	223
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast.P QFP	Plast. TQFP	Plast. VQFP	Top- Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Top- Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA			
Code		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223			
XC3020A	-7			CI	CI	CI	CI																
	-6			C	C	C	C																
XC3030A	-7	CI	CI	CI	CI	CI	CI		CI														
	-6	C	C	C	C	C	C		C														
XC3042A	-7			CI	CI	CI		CI			CI	CI	CI										
	-6			C	C	C		C			C	C	C										
XC3064A	-7			CI							CI	CI	CI	CI									
	-6			C						C	C	C	C										
XC3090A	-7			CI									CI	CI			CI	CI	CI	CI			
	-6			C									C	C		C	C	C	C				
XC3020L	-8			CI																			
XC3030L	-8		CI		CI				CI														
XC3042L	-8			CI				CI					CI										
XC3064L	-8			CI									CI										
XC3090L	-8			CI								CI						CI					
XC3120A	-5			CI	CI	CI	CI																
	-4			CI	CI	CI	CI																
	-3			CI	CI	CI	CI																
	-2			CI	CI	CI	CI																
	-1			C	C	C	C																
	-09			C	C	C	C																
XC3130A	-5	CI	CI	CI	CI	CI	CI		CI														
	-4	CI	CI	CI	CI	CI	CI		CI														
	-3	CI	CI	CI	CI	CI	CI		CI														
	-2	CI	CI	CI	CI	CI	CI		CI														
	-1	C	C	C	C	C	C		C														
	-09	C	C	C	C	C	C		C														
XC3142A	-5			CI	CIMB	CI		C	MB	C	CIMB	CI											
	-4			CI	CI	CI		C		C	CI	CI											
	-3			CI	CI	CI		CI		CI	CI	CI											
	-2			CI	CI	CI		CI		CI	CI	CI											
	-1			C	C	C		C		C	C	C											
	-09			C	C	C		C		C	C	C											
XC3164A	-5			CI					CI	CI	CI	CI											
	-4			CI					CI	CI	CI	CI											
	-3			CI					CI	CI	CI	CI											
	-2			CI					CI	CI	CI	CI											
	-1			C					C	C	C	C											
	-09			C					C	C	C	C				C	C	C	C				
XC3190A	-5			CI									CI	CI	MB	CI	CIMB	CI	CI				
	-4			CI									CI	CI		CI	CI	CI	CI				
	-3			CI									CI	CI		CI	CI	CI	CI				
	-2			CI									CI	CI		CI	CI	CI	CI				
	-1			C									C	C		C	C	C	C				
	-09			C									C	C		C	C	C	C				
XC3195A	-5			CI											CI	MB	CI	CIMB	CI	CIMB			
	-4			CI											CI		CI	CI	CI	CI			
	-3			CI											CI	CI		CI	CI	CI			
	-2			CI											CI	CI	CI	CI	CI	CI			
	-1			C											C	C	C	C	C	C			
	-09			C											C	C	C	C	C	C			

Pins		44	64	68	84	100				132			144	160	164	175			176	208	223
Type		Plast. PLCC	Plast. VQFP	Plast. PLCC	Plast. PLCC	Cer. PGA	Plast.P QFP	Plast. TQFP	Plast. VQFP	Top-Brazed CQFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Plast.-Brazed COFP	Plast. PGA	Cer. PGA	Plast. TQFP	Plast. PQFP	Cer. PGA	
Code	PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223		
XC3142L	-3*			C			C					C									
	-2*			C			C					C									
XC3190L	-3*			C								C					C				
	-2*			C								C					C				

Notes: \* Advance Information

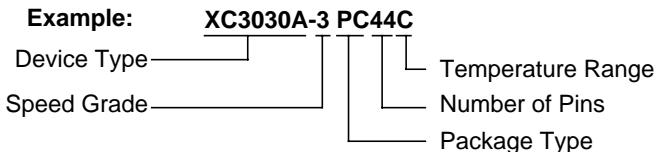
C = Commercial,  $T_J = 0^\circ \text{ to } +85^\circ\text{C}$   
M=Military Temp,  $T_C = -55^\circ \text{ to } +125^\circ\text{C}$ I = Industrial,  $T_J = -40^\circ \text{ to } +100^\circ\text{C}$   
B = MIL-STD-883C Class B

### Number of Available I/O Pins

	Max I/O	Number of Package Pins																			
		44	64	68	84	100	120	132	144	156	160	164	175	176	191	196	208	223	240		
XC3020A/XC3120A	64																				
XC3030A/XC3130A	80	34	54	58	64	64															
XC3042A/XC3142A	96		58	74	80	82		96	96												
XC3064A/XC3164A	120			74	70	74		110	120	120	120										
XC3090A/XC3190A	144			70	70	70		138	144	144	144	144					144	176	176		
XC3195A	176			70				138	144	144	144	144									

X7067

### Ordering Information



- 1 Introduction**
- 2 Development System Products and CORE Solutions Products**
- 3 CPLD Products**
- 4 FPGA Products**
- 5 SPROM Products**
- 6 3V Products**
- 7 HardWire FpgASIC Products**
- 8 High-Reliability and QML Military Products**
- 9 Programming Support**
- 10 Packages and Thermal Characteristics**
- 11 Testing, Quality, and Reliability**
- 12 Technical Support and Services**
- 13 Product Technical Information**

September 8, 1998 (Version 2.1)

Product Specification

## Features

- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports XC4000EX/XL/XLA/XV fast configuration mode (15.0 MHz)
- Low-power CMOS Floating Gate process
- XC1704L, XC1702L, XC1701L, XQ1701L and the XC17512L are 3.3 V devices
- XC1701 is a 5 V device only
- Available in compact plastic packages: 8-pin PDIP, 20-pin SOIC, 20-pin PLCC, and 44-pin VQFP.
- QPRO™ parts available in 44-pin ceramic LCC and 20-pin SOIC.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

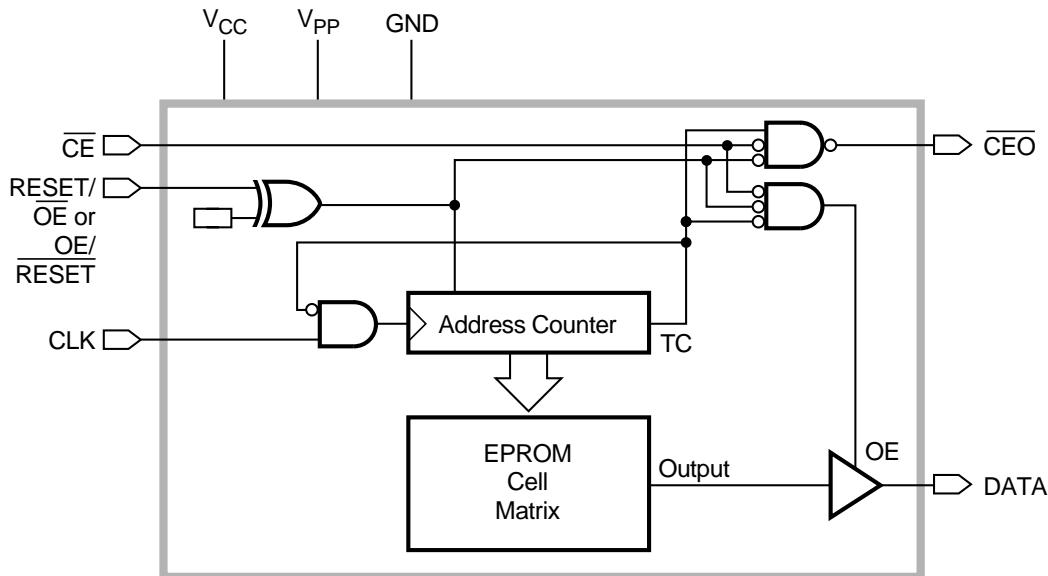
## Description

The XC1704L, XC1702L, XC1701L, and the XC17512L are Xilinx's 3.3V series of high density serial configuration PROMs (SPROMs). Included within this family are the XC1701 (5V) and the XQ1701L (3.3V) SPROMs to provide an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the  $\overline{CEO}$  output to drive the  $\overline{CE}$  input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.



X3185

**Figure 1: Simplified Block Diagram (does not show programming circuit)**

## Pin Description

### DATA

Data output, 3-stated when either  $\overline{CE}$  or  $\overline{OE}$  are inactive. During programming, the DATA pin is I/O. Note that  $\overline{OE}$  can be programmed to be either active High or active Low.

### CLK

Each rising edge on the CLK input increments the internal address counter, if both  $\overline{CE}$  and  $\overline{OE}$  are active.

### RESET/OE

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/ $\overline{OE}$  or OE/ $\overline{RESET}$ . To avoid confusion, this document describes the pin as RESET/ $\overline{OE}$ , although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low RESET, because it can be driven by the FPGA's INIT pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 Programmer. Third-party programmers have different methods to invert this pin.

### $\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low- $I_{CC}$  standby mode.

### CEO

Chip Enable output, to be connected to the  $\overline{CE}$  input of the next SPROM in the daisy chain. This output is Low when the  $\overline{CE}$  and  $\overline{OE}$  inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, CEO will follow  $\overline{CE}$  as long as  $\overline{OE}$  is active. When  $\overline{OE}$  goes inactive, CEO stays High until the PROM is reset. Note that OE can be programmed to be either active High or active Low.

### $V_{PP}$

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to  $V_{CC}$ . Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

### $V_{CC}$ and GND

Positive supply and ground pins.

## Serial PROM Pinouts

Pin Name	8-Pin PDIP	20-Pin SOIC	20-Pin PLCC	44-Pin VQFP	44-Pin LCC
DATA	1	1	2	40	2
CLK	2	3	4	43	5
RESET/OE (OE/RESET)	3	8	6	13	19
$\overline{CE}$	4	10	8	15	21
GND	5	11	10	18 & 41	24 & 3
CEO	6	13	14	21	27
$V_{PP}$	7	18	17	35	41
$V_{CC}$	8	20	20	38	44

## Capacity

Devices	Configuration Bits
XC1704L	4,194,304
XC1702L	2,097,152
XC1701L	1,048,576
XC1701	1,048,576
XC17512L	524,288

## Number of Configuration Bits, Including Header for Xilinx FPGAs and Compatible SPROMs.

Device	Configuration Bits	SPROM
XC4010XL	283,424	XC17512L
XC4013XL/XLA	393,632	XC17512L
XC4020E	329,312	XC1701
XC4020XL/XLA	521,880	XC17512L
XC4025E	422,176	XC1701
XC4028XL/XLA	668,184	XC1701L
XC4028EX	668,184	XC1701
XC4036EX	832,528	XC1701
XC4036XL/XLA	832,528	XC1701L
XC4044XL/XLA	1,014,928	XC1701L
XC4052XL/XLA	1,215,368	XC1702L
XC4062XL/XLA	1,433,864	XC1702L
XC4085XL/XLA	1,924,992	XC1702L
XC40110XV	2,686,136	XC1704L
XC40150XV	3,373,448	XC1704L
XC40200XV	4,551,056	XC1704L + XC17512L
XC40250XV	5,433,888	XC1704L + XC1702L

## Controlling Serial PROMs

Connecting the FPGA device with the SPROM.

- The DATA output(s) of the of the SPROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the SPROM(s).
- The CEO output of a SPROM drives the CE input of the next SPROM in a daisy chain (if any).
- The RESET/OE input of all SPROMs is best driven by the INIT output of the lead FPGA device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V<sub>CC</sub> glitch. Other methods – such as driving RESET/OE from LDC or system reset – assume the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.
- The SPROM CE input can be driven from either the LDC or DONE pins. Using LDC avoids potential contention on the DIN pin.
- The CE input of the lead (or only) SPROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, LDC can be used to drive CE, but must then be unconditionally High during user operation. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

## FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx SPROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the SPROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the SPROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA

families take care of this automatically with an on-chip default pull-up resistor.

## Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a SPROM, the OE pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the OE pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

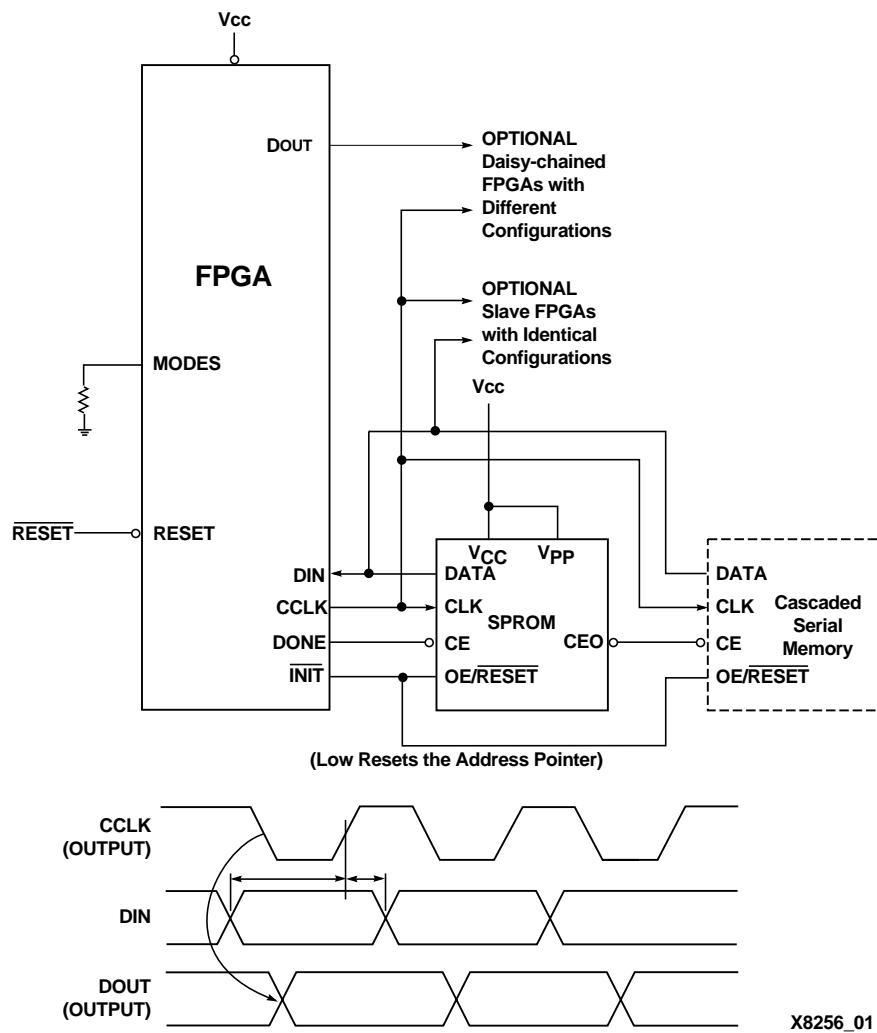
This method fails if a user applies RESET during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the Serial PROM does not reset its address counter, since it never saw a High level on its OE input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2<sup>24</sup>) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

## Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SPROMs provide additional memory. After the last bit from the first SPROM is read, the next clock signal to the SPROM asserts its CEO output Low and disables its DATA line. The second SPROM recognizes the Low level on its CE input and enables its DATA output. See [Figure 2](#).

After configuration is complete, the address counters of all cascaded SPROMs are reset if the FPGA RESET pin goes Low, assuming the SPROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.



**Figure 2: Master Serial Mode.** The one-time-programmable SPROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGA. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

## Standby Mode

The PROM enters a low-power standby mode whenever  $\overline{CE}$  is asserted High. The output remains in a high impedance state regardless of the state of the  $\overline{OE}$  input.

## Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

**Table 1: Truth Table for XC1700 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	$I_{cc}$
Inactive	Low	if address $\leq$ TC: increment if address $>$ TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

**Notes:** 1. The XC1700 RESET input has programmable polarity  
 2. TC = Terminal Count = highest address value. TC+1 = address 0.

**IMPORTANT:** Always tie the  $V_{PP}$  pin to  $V_{CC}$  in your application. Never leave  $V_{PP}$  floating.

## XC1701

### Absolute Maximum Ratings

Symbol	Description		Units
V <sub>CC</sub>	Supply voltage relative to GND	-0.5 to +7.0	V
V <sub>PP</sub>	Supply voltage relative to GND	-0.5 to +12.5	V
V <sub>IN</sub>	Input voltage relative to GND	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>TS</sub>	Voltage applied to 3-state output	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage temperature (ambient)	-65 to +150	°C
T <sub>SOL</sub>	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Operating Conditions

Symbol	Description		Min	Max	Units
V <sub>CC</sub>	Commercial	Supply voltage relative to GND (T <sub>A</sub> = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T <sub>A</sub> = -40°C to +85°C)	4.50	5.50	V

**Note:** During normal read operation V<sub>PP</sub> **must** be connect to V<sub>CC</sub>

### DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V <sub>IH</sub>	High-level input voltage		2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage		0	0.8	V
V <sub>OH</sub>	High-level output voltage (I <sub>OH</sub> = -4 mA)	Commercial	3.86		V
V <sub>OL</sub>	Low-level output voltage (I <sub>OL</sub> = +4 mA)			0.32	V
V <sub>OH</sub>	High-level output voltage (I <sub>OH</sub> = -4 mA)	Industrial	3.76		V
V <sub>OL</sub>	Low-level output voltage (I <sub>OL</sub> = +4 mA)			0.37	V
I <sub>CCA</sub>	Supply current, active mode (at maximum frequency)			10.0	mA
I <sub>CCS</sub>	Supply current, standby mode			100.0	µA
I <sub>L</sub>	Input or output leakage current		-10.0	10.0	µA
C <sub>IN</sub>	Input Capacitance (V <sub>IN</sub> = GND, f = 1.0 MHZ)			10.0	pF
C <sub>OUT</sub>	Output Capacitance (V <sub>IN</sub> = GND, f = 1.0 MHZ)			10.0	pF

## XC1704L, XC1702L, XC1701L, XQ1701L, & XC17512L

### Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +4.0	V
$V_{PP}$	Supply voltage relative to GND	-0.5 to +12.5	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Operating Conditions

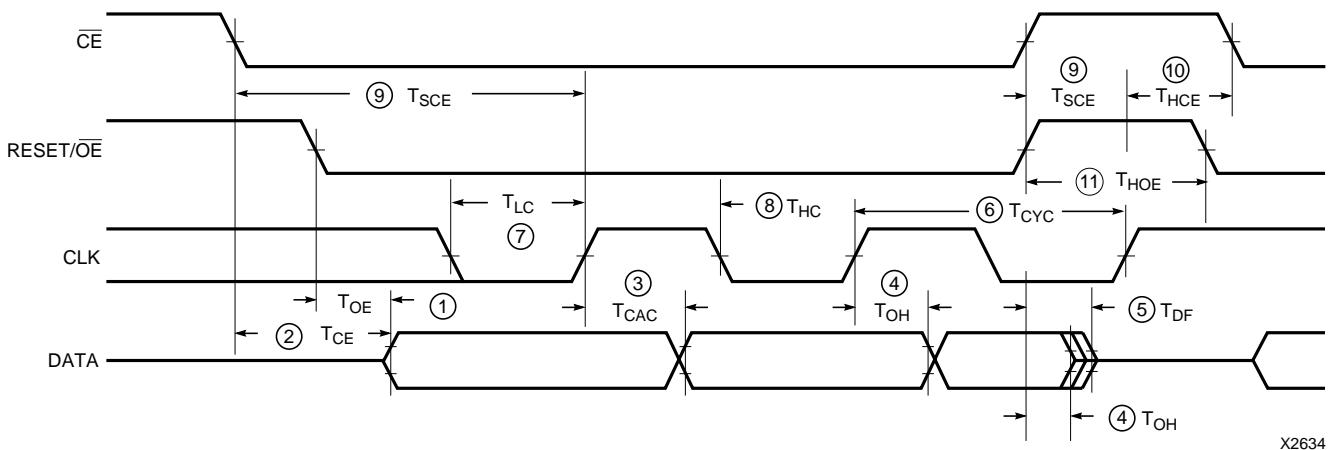
Symbol	Description		Min	Max	Units
$V_{CC}$	Commercial	Supply voltage relative to GND ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	3.0	3.6	V
	Industrial	Supply voltage relative to GND ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	3.0	3.6	V
	Military	Supply voltage relative to GND Ceramic Package ( $T_C = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )	3.0	3.6	V
		Supply voltage relative to GND Plastic Package ( $T_J = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )	3.0	3.6	V

**Note:** During normal read operation  $V_{PP}$  **must** be connected to  $V_{CC}$

### DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
$V_{IH}$	High-level input voltage	2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -3 \text{ mA}$ )	2.4		V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +3 \text{ mA}$ )		0.4	V
$I_{CCA}$	Supply current, active mode (at maximum frequency)		10.0	mA
$I_{CCS}$	Supply current, standby mode		50.0	$\mu\text{A}$
$I_L$	Input or output leakage current	-10.0	10.0	$\mu\text{A}$
$C_{IN}$	Input Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0 \text{ MHZ}$ )		10.0	pF
$C_{OUT}$	Output Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0 \text{ MHZ}$ )		10.0	pF

## AC Characteristics Over Operating Condition



Symbol	Description	XC1701		XC1704L, XC1702L, XC1701L, XQ1701L & XC17512L		Units
		Min	Max	Min	Max	
1   T <sub>OE</sub>	OE to Data Delay		25		30	ns
2   T <sub>CE</sub>	CE to Data Delay		45		45	ns
3   T <sub>CAC</sub>	CLK to Data Delay		45		45	ns
4   T <sub>OH</sub>	Data Hold From CE, OE, or CLK	0		0		ns
5   T <sub>DF</sub>	CE or OE to Data Float Delay <sup>2</sup>		50		50	ns
6   T <sub>CYC</sub>	Clock Periods	67		67		ns
7   T <sub>LC</sub>	CLK Low Time <sup>3</sup>	20		25		ns
8   T <sub>HC</sub>	CLK High Time <sup>3</sup>	20		25		ns
9   T <sub>SCE</sub>	CE Setup Time to CLK (to guarantee proper counting)	20		25		ns
10   T <sub>HCE</sub>	CE Hold Time to CLK (to guarantee proper counting)	0		0		ns
11   T <sub>HOE</sub>	OE Hold Time (guarantees counters are reset)	20		25		ns

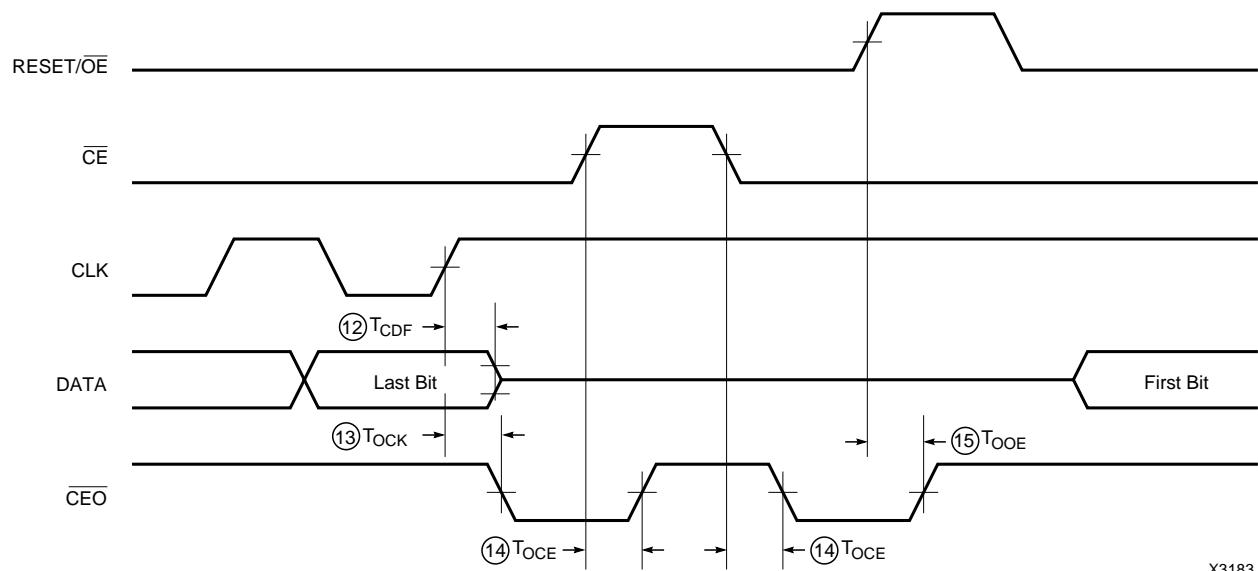
**Notes:** 1. AC test load = 50 pF

2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.

3. Guaranteed by design, not tested.

4. All AC parameters are measured with  $V_{IL} = 0.0$  V and  $V_{IH} = 3.0$  V.

## AC Characteristics Over Operating Condition When Cascading



X3183

Symbol	Description	Min	Max	Units
12	T <sub>CDF</sub> CLK to Data Float Delay <sup>2,3</sup>		50	ns
13	T <sub>OCK</sub> CLK to CEO Delay <sup>3</sup>		30	ns
14	T <sub>OCE</sub> CE to CEO Delay <sup>3</sup>		35	ns
15	T <sub>OEE</sub> RESET/OE to CEO Delay <sup>3</sup>		30	ns

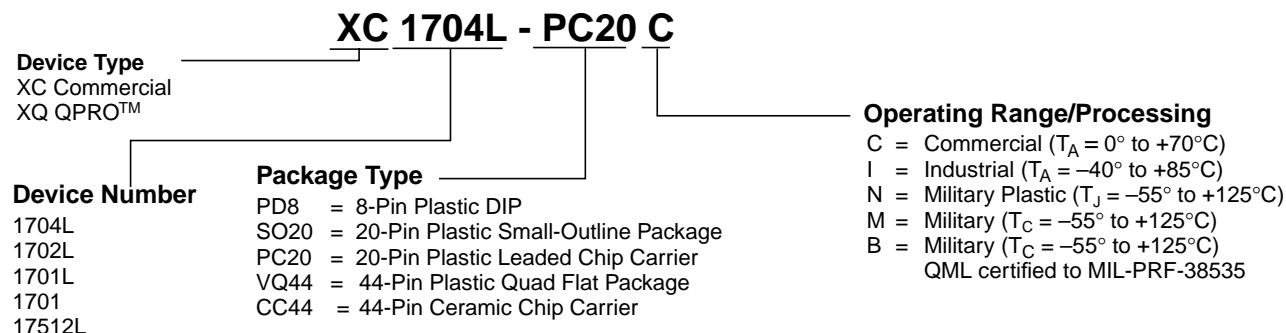
**Notes:** 1. AC test load = 50 pF

2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.

3. Guaranteed by design, not tested.

4. All AC parameters are measured with V<sub>IL</sub> = 0.0 V and V<sub>IH</sub> = 3.0 V.

## Ordering Information

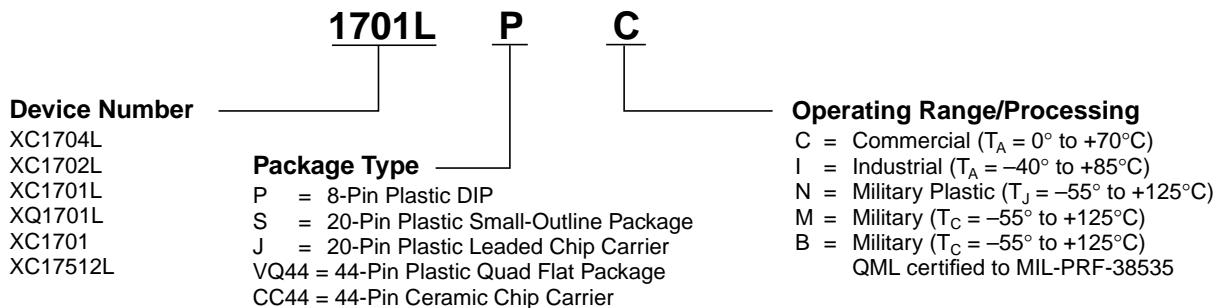


## Valid Ordering Combinations

XC1704LVQ44C	XC1702LVQ44C	XC1701LPD8C XC1701LSO20C XC1701LPC20C	XC1701PD8C XC1701SO20C XC1701PC20C	XC17512LPD8C XC17512LSO20C XC17512LPC20C
XC1704LVQ44I	XC1702LVQ44I	XC1701LPD8I XC1701LSO20I XC1701PC20I	XC1701PD8I XC1701SO20I XC1701PC20I	XC17512LPD8I XC17512LSO20I XC17512LPC20I
		XQ1701LCC44M XQ1701LCC44B XQ1701LS020N		

## Marking Information

Due to the small size of the commercial serial PROM packages, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. The XQ CC44 packages are marked as ordered. Device marking on the commercial and military plastic packages is as follows:



## Revision Control

Date	Revision
7/14/98	Major revisions to include the XC1704L, XC1702L, and the XQ1701L devices, packages and operating conditions. Also revised the timing specifications on page 5-8.
9/8/98	Revised the marking information on page 5-10 for the VQ44. Updated the DC characteristics on page 5-7. Added references to the XC4000XLA and XC4000XV families in table on 5-2, figure 2 on 5-4.

## Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports the XC4000EX/XL/XLA/XV fast configuration mode (15.0 MHz)
- Low-power CMOS floating gate process
- Available in 5 V and 3.3 V versions
- Available in compact plastic 8-pin DIP, 8-pin SOIC, 8-pin VOIC, or 20-pin PLCC packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

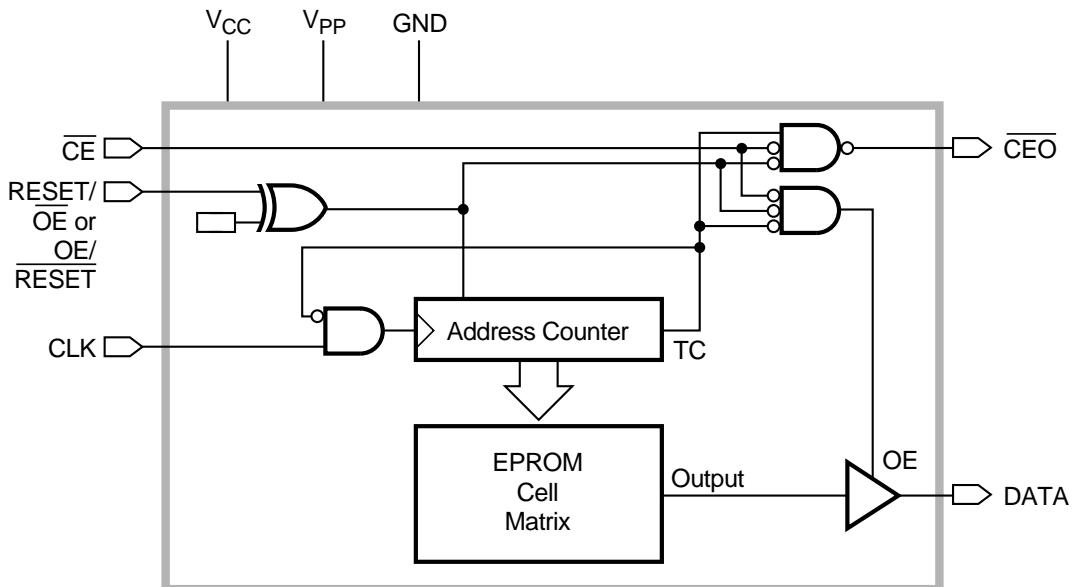
## Description

The XC1700 family of serial configuration PROMs (SPROMs) provides an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the  $\overline{CEO}$  output to drive the  $\overline{CE}$  input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the FPGA design file into a standard HEX format which is then transferred to most commercial PROM programmers.



X3185

**Figure 1: Simplified Block Diagram (does not show programming circuit)**

## Pin Description

### DATA

Data output, 3-stated when either  $\overline{CE}$  or  $\overline{OE}$  are inactive. During programming, the DATA pin is I/O. Note that  $\overline{OE}$  can be programmed to be either active High or active Low.

### CLK

Each rising edge on the CLK input increments the internal address counter, if both  $\overline{CE}$  and  $\overline{OE}$  are active.

### RESET/ $\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/ $\overline{OE}$  or OE/ $\overline{RESET}$ . To avoid confusion, this document describes the pin as RESET/ $\overline{OE}$ , although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low RESET, because it can be driven by the FPGA's INIT pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.

### $\overline{CE}$

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low- $I_{CC}$  standby mode.

### CEO

Chip Enable output, to be connected to the  $\overline{CE}$  input of the next SPROM in the daisy chain. This output is Low when the  $\overline{CE}$  and  $\overline{OE}$  inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. In other words: when the PROM has been read, CEO will follow  $\overline{CE}$  as long as  $\overline{OE}$  is active. When  $\overline{OE}$  goes inactive, CEO stays High until the PROM is reset. Note that  $\overline{OE}$  can be programmed to be either active High or active Low.

### $V_{PP}$

Programming voltage. No overshoot above the specified max voltage is permitted on this pin. For normal read operation, this pin *must* be connected to  $V_{CC}$ . Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging. *Do not leave VPP floating!*

### $V_{CC}$ and GND

$V_{CC}$  is positive supply pin and GND is ground pin.

## Serial PROM Pinouts

Pin Name	8-Pin	20-Pin
DATA	1	2
CLK	2	4
RESET/ $\overline{OE}$ (OE/RESET)	3	6
$\overline{CE}$	4	8
GND	5	10
CEO	6	14
$V_{PP}$	7	17
$V_{CC}$	8	20

## Capacity

Device	Configuration Bits
XC1736E	36,288
XC1765E or EL	65,536
XC17128E or EL	131,072
XC17256E or EL	262,144
XC17512L	524,288
XC1701 or L	1,048,576
XC1702L	2,097,152
XC1704L	4,194,304

**Note:** The XC17512L and larger SPROMs are specified in a separate datasheet.

## Number of Configuration Bits, Including Header for Xilinx FPGAs and Compatible SPROMs

Device	Configuration Bits	SPROM
XC4003E	53,984	XC17128E <sup>1</sup>
XC4005E	95,008	XC17128E
XC4006E	119,840	XC17128E
XC4008E	147,552	XC17256E
XC4010E	178,144	XC17256E
XC4013E	247,968	XC17256E
XC4020E	329,312	XC1701
XC4025E	422,176	XC1701
XC4002XL	61,100	XC17128EL <sup>1</sup>
XC4005XL	151,960	XC17256EL
XC4010XL	283,424	XC17512L
XC4013XL/XLA	393,632	XC17512L
XC4020XL/XLA	521,880	XC17512L
XC4028XL/XLA	668,184	XC1701L
XC4028EX	668,184	XC1701
XC4036EX/XL/XLA	832,528	XC1701L
XC4036EX	832,528	XC1701
XC4044XL/XLA	1,014,928	XC1701L
XC4052XL/XLA	1,215,368	XC1702L
XC4062XL/XLA	1,433,864	XC1702L
XC4085XL/XLA	1,924,992	XC1702L
XC40110XV	2,686,136	XC1704L
XC40150XV	3,373,448	XC1704L
XC40200XV	4,551,056	XC1704L + XC17512L
XC40250XV	5,433,888	XC1704L+ XC1702L
XC5202	42,416	XC1765E
XC5204	70,704	XC17128E
XC5206	106,288	XC17128E
XC5210	165,488	XC17256E
XC5215	237,744	XC17256E

**Note:** 1. The suggested SPROM is determined by compatibility with the higher configuration frequency of the Xilinx FPGA CCLK. Designers using the default slow configuration frequency (CCLK) can use the XC1765E or XC1765EL for the noted FPGA devices.

## Controlling Serial PROMs

Connecting the FPGA device with the SPROM.

- The DATA output(s) of the SPROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the SPROM(s).
- The CEO output of a SPROM drives the  $\overline{CE}$  input of the next SPROM in a daisy chain (if any).
- The RESET/OE input of all SPROMs is best driven by the INIT output of the lead FPGA device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a  $V_{CC}$  glitch. Other methods – such as driving RESET/OE from LDC or system reset – assume the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This may not be a safe assumption.
- The SPROM  $\overline{CE}$  input can be driven from either the LDC or DONE pins. Using  $\overline{LDC}$  avoids potential contention on the DIN pin.
- The CE input of the lead (or only) SPROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise,  $\overline{LDC}$  can be used to drive  $\overline{CE}$ , but must then be unconditionally High during user operation.  $\overline{CE}$  can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

## FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx SPROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low ( $M0=0$ ,  $M1=0$ ,  $M2=0$ ). Data is read from the SPROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the SPROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. Xilinx FPGAs take care of this automatically with an on-chip default pull-up resistor.

## Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a SPROM, the  $\overline{OE}$  pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the  $\overline{OE}$  pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies  $\overline{RESET}$  during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the SPROM does not reset its address counter, since it never saw a High level on its  $\overline{OE}$  input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is

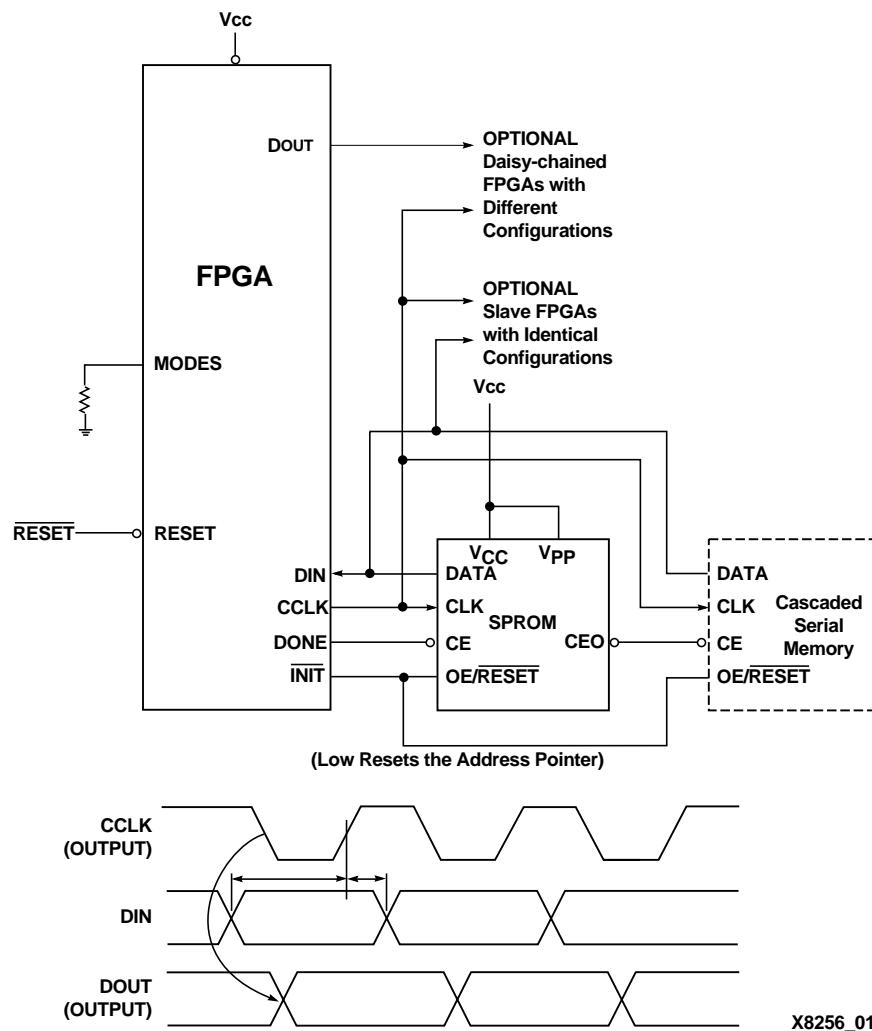
the master, it issues the necessary number of CCLK pulses, up to 16 million ( $2^{24}$ ) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

## Cascading Serial Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded SPROMs provide additional memory. After the last bit from the first SPROM is read, the next clock signal to the SPROM asserts its  $\overline{CEO}$  output Low and disables its DATA line. The second SPROM recognizes the Low level on its  $\overline{CE}$  input and enables its DATA output. See [Figure 2](#).

After configuration is complete, the address counters of all cascaded SPROMs are reset if the FPGA  $\overline{RESET}$  pin goes Low, assuming the SPROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.



**Figure 2: Master Serial Mode.** The one-time-programmable SPROM supports automatic loading of configuration programs. Multiple devices can be cascaded to support additional FPGA. An early DONE inhibits the SPROM data output one CCLK cycle before the FPGA I/Os become active.

## Standby Mode

The SPROM enters a low-power standby mode whenever  $\overline{CE}$  is asserted High. The output remains in a high impedance state regardless of the state of the  $\overline{OE}$  input.

## Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

**Table 1: Truth Table for XC1700 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET	CE		DATA	CEO	$I_{cc}$
Inactive	Low	if address $\leq$ TC: increment if address $>$ TC: don't change	active 3-state	High Low	active reduced
Active	Low	Held reset	3-state	High	active
Inactive	High	Not changing	3-state	High	standby
Active	High	Held reset	3-state	High	standby

**Notes:** 1. The XC1700 RESET input has programmable polarity  
2. TC = Terminal Count = highest address value. TC+1 = address 0.

**Important:** Always tie the  $V_{PP}$  pin to  $V_{CC}$  in your application. Never leave  $V_{PP}$  floating.

## XC1736E, XC1765E, XC17128E and XC17256E

### Absolute Maximum Ratings

Symbol	Description		Units
V <sub>CC</sub>	Supply voltage relative to GND	-0.5 to +7.0	V
V <sub>PP</sub>	Supply voltage relative to GND	-0.5 to +12.5	V
V <sub>IN</sub>	Input voltage relative to GND	-0.5 to V <sub>CC</sub> +0.5	V
V <sub>TS</sub>	Voltage applied to 3-state output	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>STG</sub>	Storage temperature (ambient)	-65 to +150	°C
T <sub>SOL</sub>	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Operating Conditions

Symbol	Description		Min	Max	Units
V <sub>CC</sub>	Commercial	Supply voltage relative to GND (T <sub>A</sub> = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T <sub>A</sub> = -40°C to +85°C)	4.50	5.50	V

**Note:** During normal read operation V<sub>PP</sub> **must** be connected to V<sub>CC</sub>

### DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V <sub>IH</sub>	High-level input voltage		2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage		0	0.8	V
V <sub>OH</sub>	High-level output voltage (I <sub>OH</sub> = -4 mA)	Commercial	3.86		V
V <sub>OL</sub>	Low-level output voltage (I <sub>OL</sub> = +4 mA)			0.32	V
V <sub>OH</sub>	High-level output voltage (I <sub>OH</sub> = -4 mA)	Industrial	3.76		V
V <sub>OL</sub>	Low-level output voltage (I <sub>OL</sub> = +4 mA)			0.37	V
I <sub>CCA</sub>	Supply current, active mode (at maximum frequency)			10.0	mA
I <sub>CCS</sub>	Supply current, standby mode			50.0	µA
I <sub>L</sub>	Input or output leakage current		-10.0	10.0	µA
C <sub>IN</sub>	Input Capacitance (V <sub>IN</sub> = GND, f = 1.0MHz)			10.0	pF
C <sub>OUT</sub>	Output Capacitance (V <sub>IN</sub> = GND, f = 1.0MHz)			10.0	pF

## XC1765EL, XC17128EL and XC17256EL

### Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +4.0	V
$V_{PP}$	Supply voltage relative to GND	-0.5 to +12.5	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Operating Conditions

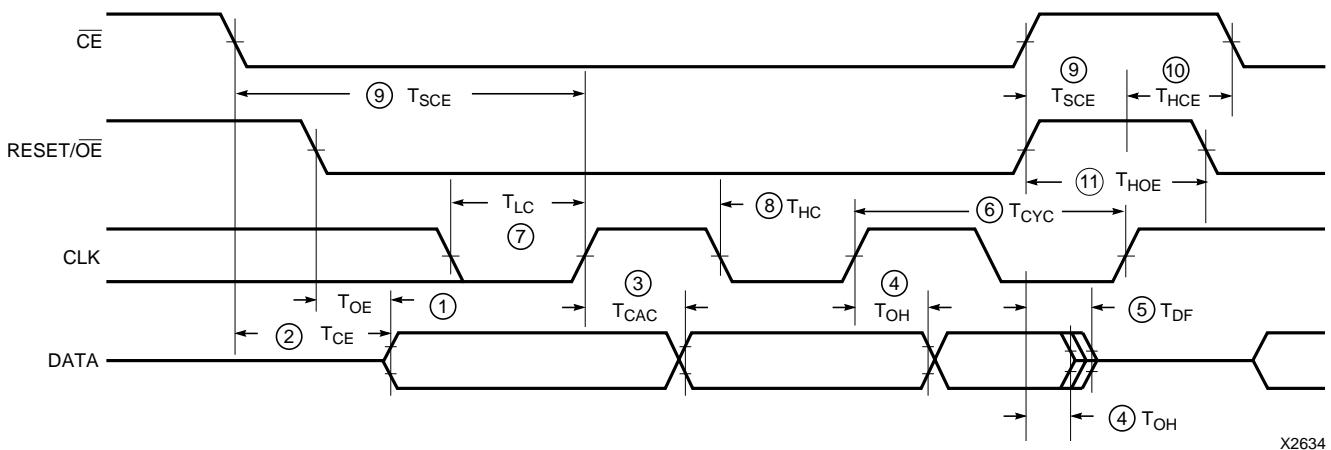
Symbol	Description		Min	Max	Units
$V_{CC}$	Commercial	Supply voltage relative to GND ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	3.0	3.6	V
	Industrial	Supply voltage relative to GND ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	3.0	3.6	V

**Note:** During normal read operation  $V_{PP}$  **must** be connected to  $V_{CC}$

### DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
$V_{IH}$	High-level input voltage	2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -3 \text{ mA}$ )	2.4		V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +3 \text{ mA}$ )		0.4	V
$I_{CCA}$	Supply current, active mode (at maximum frequency)		5.0	mA
$I_{CCS}$	Supply current, standby mode		50.0	$\mu\text{A}$
$I_L$	Input or output leakage current	-10.0	10.0	$\mu\text{A}$
$C_{IN}$	Input Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0\text{MHz}$ )		10.0	pF
$C_{OUT}$	Output Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0\text{MHz}$ )		10.0	pF

## AC Characteristics Over Operating Condition



Symbol	Description	XC1736E XC1765E		XC1765EL		XC17128E XC17256E		XC17128EL XC17256EL		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
1	T <sub>OE</sub>	$\overline{OE}$ to Data Delay		45		45		25		30 ns
2	T <sub>CCE</sub>	$\overline{CE}$ to Data Delay		60		60		45		45 ns
3	T <sub>CAC</sub>	CLK to Data Delay		80		200		45		45 ns
4	T <sub>OH</sub>	Data Hold From $\overline{CE}$ , $\overline{OE}$ , or CLK <sup>3</sup>		0	0		0	0		ns
5	T <sub>DF</sub>	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay <sup>2 &amp; 3</sup>		50		50		50		50 ns
6	T <sub>CYC</sub>	Clock Periods		100	400		67	67		ns
7	T <sub>LC</sub>	CLK Low Time <sup>3</sup>		50	100		20	25		ns
8	T <sub>HC</sub>	CLK High Time <sup>3</sup>		50	100		20	25		ns
9	T <sub>SCE</sub>	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)		25	40		20	25		ns
10	T <sub>HCE</sub>	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)		0	0		0	0		ns
11	T <sub>HOE</sub>	$\overline{OE}$ Hold Time (guarantees counters are reset)		100	100		20	25		ns

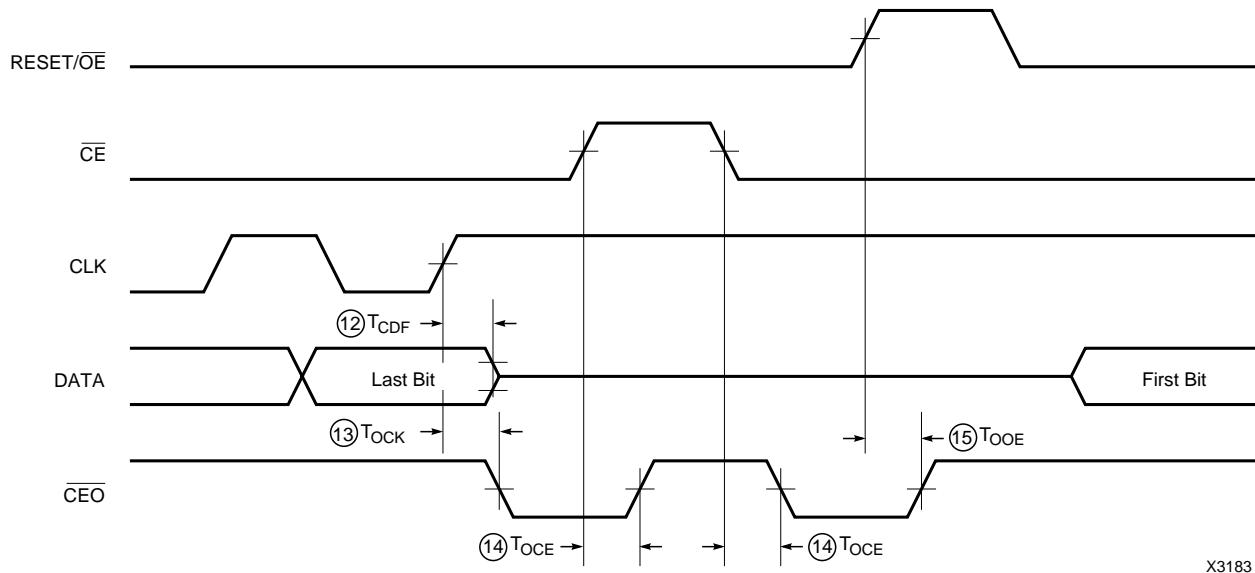
**Notes:** 1. AC test load = 50 pF

2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.

3. Guaranteed by design, not tested.

4. All AC parameters are measured with  $V_{IL} = 0.0$  V and  $V_{IH} = 3.0$  V.

## AC Characteristics Over Operating Condition When Cascading



Symbol	Description	Min	Max	Units
12 T <sub>CDF</sub>	CLK to Data Float Delay <sup>2,3</sup>		50	ns
13 T <sub>OCK</sub>	CLK to $\overline{\text{CEO}}$ Delay <sup>3</sup>		30	ns
14 T <sub>OCE</sub>	CE to $\overline{\text{CEO}}$ Delay <sup>3</sup>		35	ns
15 T <sub>OOE</sub>	RESET/OE to $\overline{\text{CEO}}$ Delay <sup>3</sup>		30	ns

**Notes:** 1. AC test load = 50 pF

2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.

3. Guaranteed by design, not tested.

4. All AC parameters are measured with  $V_{IL} = 0.0$  V and  $V_{IH} = 3.0$  V.

## Ordering Information

**XC17256E VO8 C**

Device Number \_\_\_\_\_

XC1736E  
XC1765E  
XC1765EL  
XC17128E  
XC17128EL  
XC17256E  
XC17256EL

Package Type \_\_\_\_\_

PD8 = 8-Pin Plastic DIP  
SO8 = 8-Pin Plastic Small-Outline Package  
VO8 = 8-Pin Plastic Small-Outline Thin Package  
PC20 = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

## Valid Ordering Combinations

XC17128EPD8C	XC17256EPD8C	XC1736EPD8C	XC1765EPD8C	XC1701PD8C	XC1702LVQ44C
XC17128EVO8C	XC17256EVO8C	XC1736ESO8C	XC1765ESO8C	XC1701PC20C	XC1704LVQ44C
XC17128EPC20C	XC17256EPC20C	XC1736EVO8C	XC1765EVO8C	XC1701SO20C	XC1702LVQ44I
XC17128EPD8I	XC17256EPD8I	XC1736EPC20C	XC1765EPC20C	XC1701PD8I	XC1704LVQ44I
XC17128EVO8I	XC17256EVO8I	XC1736EPD8I	XC1765EPD8I	XC1701PC20I	XQ1701LCC44M
XC17128EPC20I	XC17256EPC20I	XC1736ESO8I	XC1765ESO8I	XC1701SO20I	XQ1701LCC44B
		XC1736EVO8I	XC1765EVO8I		XQ1701LS020N
		XC1736EPC20I	XC1765EPC20I		
XC17128ELPD8C	XC17256ELPD8C		XC1765ELPD8C	XC1701LPD8C	XC17512LPD8C
XC17128ELVO8C	XC17256ELVO8C		XC1765ELSO8C	XC1701LPC20C	XC17512LPC20C
XC17128ELPC20C	XC17256ELPC20C		XC1765ELVO8C	XC1701LSO20C	XC17512LSO20C
XC17128ELPD8I	XC17256ELPD8I		XC1765ELPC20C	XC1701LPD8I	XC17512LPD8I
XC17128ELVO8I	XC17256ELVO8I		XC1765ELPD8I	XC1701LPC20I	XC17512LPC20I
XC17128ELPC20I	XC17256ELPC20I		XC1765ELSO8I	XC1701LSO20I	XC17512LSO20I
			XC1765ELVO8I		
			XC1765ELPC20I		

## Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

**17256E V C**

Device Number \_\_\_\_\_

XC1736E  
XC1765E  
XC1765X  
XC17128E  
XC17128X  
XC17256E  
XC17256X

Package Type \_\_\_\_\_

P = 8-Pin Plastic DIP  
S = 8-Pin Plastic Small-Outline Package  
V = 8-Pin Plastic Small-Outline Thin Package  
J = 20-Pin Plastic Leaded Chip Carrier

Operating Range/Processing

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

**Note:** When marking the device number on the EL parts, an X is used in place of an EL.

## Revision Control

Date	Revision
7/14/98	Revised $I_{CCS}$ on pages 5-17 & 5-18; revised $V_{CC}$ specifications for $T_A$ on pages 5-17 & 5-18; revised $V_{CC}$ on page 5-18; revised Note 2 on page 5-19 and 5-20; clarified title on page 5-20; added $T_A$ to operating range specifications on page 5-21.
9/8/98	Revised the references to FPGA's to include the XC4000XLA and XC4000XV families.
9/30/98	Updated Valid Ordering Combinations on page 11 to include high density products.

September 8, 1998 (Version 1.2)

Product Specification

## Introduction

The Spartan™ family of Serial Configuration PROMs (SPROM) provides an easy-to-use, cost-effective method for storing Spartan device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the Spartan device DIN pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When a Spartan device is in Slave Serial mode, the SPROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

## Spartan SPROM Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Spartan FPGA devices
- Simple interface to the Spartan device requires only one user I/O pin
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- Available in 5 V and 3.3 V versions
- Available in compact plastic 8-pin DIP, 8-pin VOIC, or 20-pin SOIC (XC17S40 only) packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Spartan FPGA	Configuration Bits	Compatible Spartan SPROM
XCS05	53,984	XC17S05
XCS05XL	54,544	XC17S05XL
XCS10	95,008	XC17S10
XCS10XL	95,752	XC17S10XL
XCS20	178,144	XC17S20
XCS20XL	179,160	XC17S20XL
XCS30	247,968	XC17S30
XCS30XL	249,168	XC17S30XL
XCS40	329,312	XC17S40
XCS40XL	330,696	XC17S40XL

## Pin Description

Table 1: Spartan PROM Pinouts

Pin Name	8-Pin PDIP & VOIC	20-Pin SOIC	Pin Description
DATA	1	1	Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/ $\overline{OE}$ ( $\overline{OE}/\overline{RESET}$ )	3	8	<p>When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/<math>\overline{OE}</math> or <math>\overline{OE}/\overline{RESET}</math>. To avoid confusion, this document describes the pin as RESET/<math>\overline{OE}</math>, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low <math>\overline{RESET}</math>, because it can be driven by the FPGA's INIT pin.</p> <p>The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.</p>
$\overline{CE}$	4	10	When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low- $I_{CC}$ standby mode.
GND	5	11	GND is the ground connection.
$V_{CC}$	7, 8	18, 20	The $V_{CC}$ pins are to be connected to the positive voltage supply.

## Controlling Serial PROMs

Connecting the Spartan device with the SPROM:

- The DATA output of the SPROM drives the DIN input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the SPROM.
- The RESET/OE input of the SPROM is driven by the INIT output of the Spartan device. This connection assures that the SPROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V<sub>CC</sub> glitch. Other methods – such as driving RESET/OE from LDC or system reset – assume that the SPROM internal power-on-reset is always in step with the FPGA's internal power-on-reset, which may not be a safe assumption.
- The CE input of the SPROM is driven by the DONE output of the Spartan device, provided that DONE is not permanently grounded. Otherwise, LDC can be used to drive CE, but must then be unconditionally High during user operation. CE can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

## FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device MODE pin. In Master Serial mode, the Spartan device automatically loads the configuration program from an external memory. The Spartan SPROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the MODE pin is Low. Data is read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

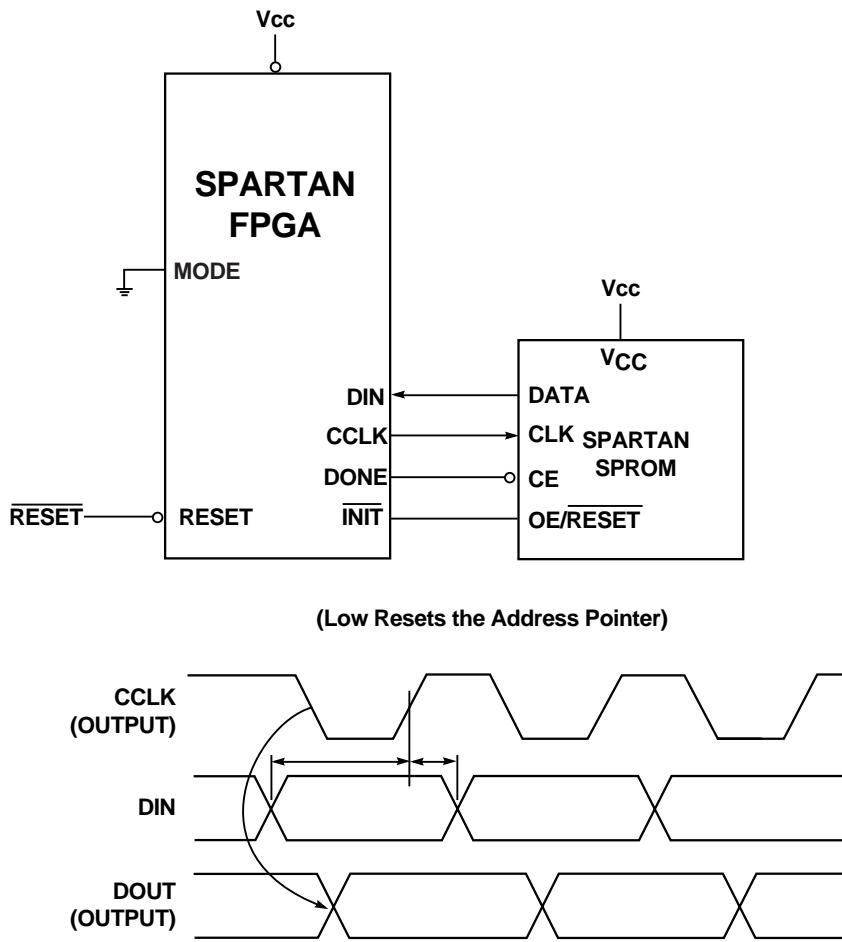
Master Serial mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure the Spartan device. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan family takes care of this automatically with an on-chip default pull-up resistor.

## Programming the FPGA With Counters Unchanged Upon Completion

When multiple-configurations for a single Spartan device are stored in a Serial Configuration PROM, the OE pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the OE pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies RESET during the Spartan device configuration process. The Spartan device aborts the configuration and then restarts a new configuration, as intended, but the SPROM does not reset its address counter, since it never saw a High level on its OE input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the Spartan device is the Master, it issues the necessary number of CCLK pulses, up to 16 million ( $2^{24}$ ) and DONE goes High. However, the Spartan device configuration will be completely wrong, with potential contentions inside the Spartan device and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.



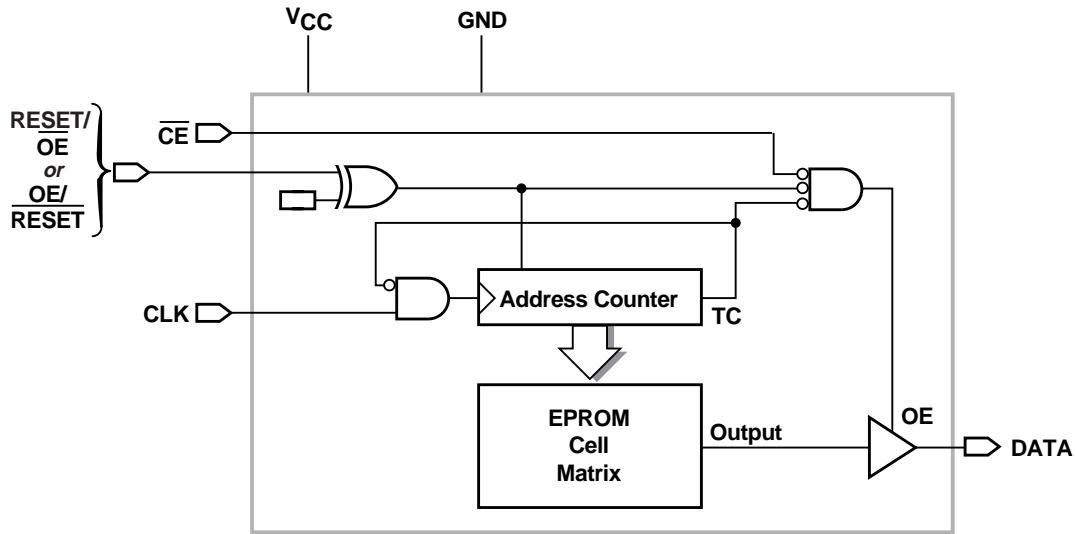
**Figure 1: Master Serial Mode.** The one-time-programmable Spartan SPROM supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.

## Standby Mode

The SPROM enters a low-power standby mode whenever  $\overline{CE}$  is asserted High. The output remains in a high impedance state regardless of the state of the  $\overline{OE}$  input.

## Programming the Spartan Family Serial PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.



X8473\_01

**Figure 2: Simplified Block Diagram (does not show programming circuit)**

**Important:** Always tie the two  $V_{CC}$  pins together in your application.

**Table 2: Truth Table for XC17S00 Control Inputs**

Control Inputs		Internal Address	Outputs	
RESET	CE		DATA	$I_{cc}$
Inactive	Low	if address $\leq$ TC: increment if address $>$ TC: don't change	active 3-state	active reduced
Active	Low	Held reset	3-state	active
Inactive	High	Not changing	3-state	standby
Active	High	Held reset	3-state	standby

**Notes:** 1. The XC17S00 RESET input has programmable polarity  
2. TC = Terminal Count = highest address value. TC+1 = address 0.

**XC17S05, XC17S10, XC17S20, XC17S30, XC17S40****Absolute Maximum Ratings**

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

**Operating Conditions**

Symbol	Description	Min	Max	Units
$V_{CC}$	Commercial Supply voltage relative to GND ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	4.75	5.25	V
	Industrial Supply voltage relative to GND ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	4.50	5.50	V

**Note:** During normal read operation both  $V_{CC}$  pins must be connected together.

**DC Characteristics Over Operating Condition**

Symbol	Description		Min	Max	Units
$V_{IH}$	High-level input voltage		2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage		0	0.8	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -4 \text{ mA}$ )	Commercial	3.86		V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +4 \text{ mA}$ )			0.32	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -4 \text{ mA}$ )	Industrial	3.76		V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +4 \text{ mA}$ )			0.37	V
$I_{CCA}$	Supply current, active mode (at maximum frequency)			10.0	mA
$I_{CCS}$	Supply current, standby mode	XC17S05, XC17S10, XC17S20, XC17S30		50.0	μA
		XC17S40		100.0	μA
$I_L$	Input or output leakage current		-10.0	10.0	μA
$C_{IN}$	Input Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0 \text{ MHz}$ )			10.0	pF
$C_{OUT}$	Output Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0 \text{ MHz}$ )			10.0	pF

## XC17S05XL, XC17S10XL, XC17S20XL, XC17S30XL, XC17S40XL

### Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +4.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### Operating Conditions

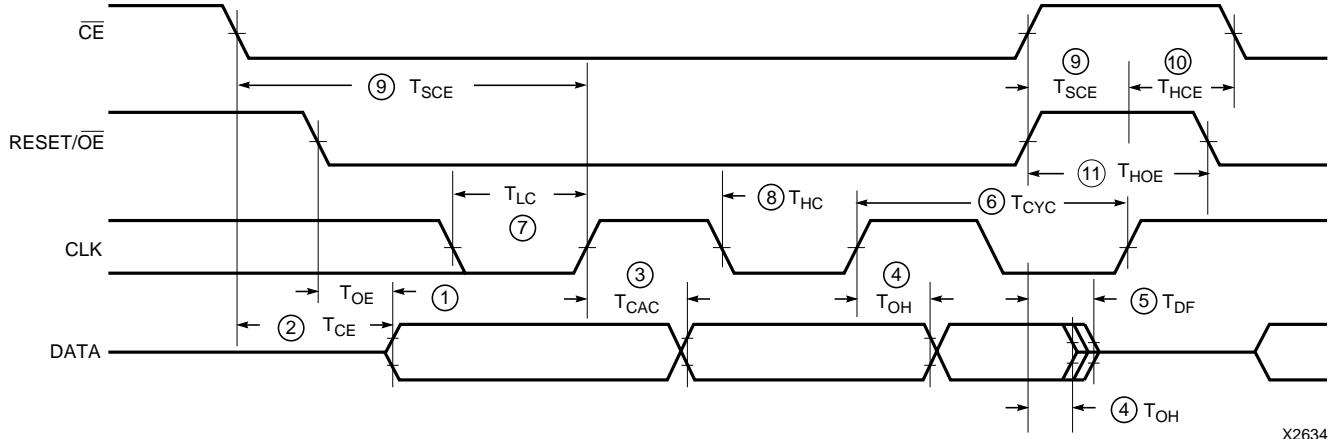
Symbol	Description	Min	Max	Units
$V_{CC}$	Commercial Supply voltage relative to GND ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )	3.0	3.6	V
	Industrial Supply voltage relative to GND ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )	3.0	3.6	V

**Note:** During normal read operation both  $V_{CC}$  pins must be connected together.

### DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
$V_{IH}$	High-level input voltage	2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -3 \text{ mA}$ )	2.4		V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +3 \text{ mA}$ )		0.4	V
$I_{CCA}$	Supply current, active mode (at maximum frequency)		5.0	mA
$I_{CCS}$	Supply current, standby mode		50.0	μA
$I_L$	Input or output leakage current	-10.0	10.0	μA
$C_{IN}$	Input Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0\text{MHz}$ )		10.0	pF
$C_{OUT}$	Output Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0\text{MHz}$ )		10.0	pF

## AC Characteristics Over Operating Condition



X2634

Symbol	Description	Min	Max	Units
1 T <sub>OE</sub>	OE to Data Delay		45	ns
2 T <sub>CE</sub>	CE to Data Delay		60	ns
3 T <sub>CAC</sub>	CLK to Data Delay		80	ns
4 T <sub>OH</sub>	Data Hold From CE, OE, or CLK <sup>2 &amp; 3</sup>	0		ns
5 T <sub>DF</sub>	CE or OE to Data Float Delay <sup>2 &amp; 3</sup>		50	ns
6 T <sub>CYC</sub>	Clock Periods (T <sub>CCLK</sub> on FPGA)	100		ns
7 T <sub>LC</sub>	CLK Low Time <sup>3</sup>	50		ns
8 T <sub>HC</sub>	CLK High Time <sup>3</sup>	50		ns
9 T <sub>SCE</sub>	CE Setup Time to CLK (to guarantee proper counting)	25		ns
10 T <sub>HCE</sub>	CE Hold Time to CLK (to guarantee proper counting)	0		ns
11 T <sub>HOE</sub>	OE Hold Time (guarantees counters are reset)	25		ns

**Notes:** 1. AC test load = 50 pF

2. Float delays are measured with 5 pF AC loads. Transition is measured at +/- 200mV from steady state active levels.

3. Guaranteed by design, not tested.

4. All AC parameters are measured with V<sub>IL</sub> = 0.0 V and V<sub>IH</sub> = 3.0 V.

## Ordering Information

**XC17S20XL VO8 C**

**Device Number**

XC17S05  
XC17S05XL  
XC17S10  
XC17S10XL  
XC17S20  
XC17S20XL  
XC17S30  
XC17S30XL  
XC17S40  
XC17S40XL

**Package Type**

PD8 = 8-Pin Plastic DIP  
VO8 = 8-Pin Plastic Small-Outline Thin Package  
SO20 = 20-Pin Plastic Small-Outline Package

**Operating Range/Processing**

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

## Valid Ordering Combinations

XC17S05PD8C	XC17S10PD8C	XC17S20PD8C	XC17S30PD8C	XC17S40PDC
XC17S05VO8C	XC17S10VO8C	XC17S20VO8C	XC17S30VO8C	XC17S40SO20C
XC17S05PD8I	XC17S10PD8I	XC17S20PD8I	XC17S30PD8I	XC17S40PD8I
XC17S05VO8I	XC17S10VO8I	XC17S20VO8I	XC17S30VO8I	XC17S40SO20I
XC17S05XLPD8C	XC17S10XLPD8C	XC17S20XLPD8C	XC17S30XLPD8C	XC17S40XLPD8C
XC17S05XLVO8C	XC17S10XLVO8C	XC17S20XLVO8C	XC17S30XLVO8C	XC17S40XLSO20C
XC17S05XLPD8I	XC17S10XLPD8I	XC17S20XLPD8I	XC17S30XLPD8I	XC17S40XLPD8I
XC17S05XLVO8I	XC17S10XLVO8I	XC17S20XLVO8I	XC17S30XLVO8I	XC17S40XLSO20I

## Marking Information

Due to the small size of the serial PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.

**17S20L V C**

**Device Number**

XC17S05  
XC17S05L  
XC17S10  
XC17S10L  
XC17S20  
XC17S20L  
XC17S30  
XC17S30L  
XC17S40  
XC17S40L

**Package Type**

P = 8-Pin Plastic DIP  
V = 8-Pin Plastic Small-Outline Thin Package  
S = 20-Pin Plastic Small-Outline Package

**Operating Range/Processing**

C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )  
I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

**Note:** When marking the device number on the XL parts, an L is used in place of an XL.

## Revision Control

Date	Revision
7/14/98	Cosmetic edits for pages 5-24, 5-25, 5-28 & 5-29.
9/8/98	Clarified the SPARTAN FPGA & PROM interface by removing references to CEO pin. Removed the ESD notation in Absolute Maximum table since it is now included in Xilinx's Reliability Monitor Report.

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- 2 Development System Products and CORE Solutions Products**
- 3 CPLD Products**
- 4 FPGA Products**
- 5 SPROM Products**
- 6 3V Products**
- 7 HardWire FpgASIC Products**
- 8 High-Reliability and QML Military Products**
- 9 Programming Support**
- 10 Packages and Thermal Characteristics**
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- 12 Technical Support and Services**
- 13 Product Technical Information**



## 3V Products

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November 20, 1997 (Version 2.1)

The use of advanced deep-submicron IC fabrication processes is resulting in rapidly increasing density and performance for programmable logic devices, as evidenced by the XC4000XL FPGA family. However, as device geometries shrink below 0.5 microns, the smallest transistors cannot withstand 5 volts without damage. Thus, the largest and fastest new devices are based on lower supply voltages, such as the 3.3 V standard.

To reap the benefits of advanced process technology - including increased performance, increased density, lower power consumption, and lower price - many programmable logic users are making the transition from the 5.0 V standard to lower voltages. This transition affects not only the supply voltage, but also I/O signaling levels. Xilinx is taking an active lead in working with programmable logic users to plan an orderly transition from one voltage standard to the next.

Xilinx introduced the Zero+™ product line, the industry's first 3.3 V FPGAs, in 1993. Since then, the number of 3.3 V product offerings has increased dramatically. For example, the new XC4000XL FPGA family, featuring the industry's highest-capacity high-performance FPGAs, is based on the 3.3 V standard.

However, many other system components remain available in 5.0 V versions only. Thus, mixed-voltage systems (i.e., systems employing a mix of 5.0 V and 3.3 V components) are likely to be the rule rather than the exception in the immediate future. Xilinx products have been designed with this in mind (see **Table 1**). 5.0 V input tolerance has been designed into many Xilinx 3.3 V devices; these devices accept 5.0 V signals on all I/Os and can drive TTL levels into any 5.0 V device, eliminating any interface issues. Many Xilinx 5.0 V components can directly interface with 3.3 V devices. Future devices will feature multi-voltage I/Os capable of interfacing between a variety of I/O standards.

All Xilinx device inputs maintain their excellent protection against Electro-Static Discharge (ESD), even in mixed-voltage applications.

The following is a brief description of Xilinx devices suitable for use in 3.3 V and mixed 3.3/5.0 V systems. Complete data sheets for the products mentioned below can be found in Chapters 3 and 4 of this Data Book. 3.3 V versions of the Serial PROM devices also are available (see Chapter 6).

### FPGAs

#### 3.3 V FPGAs with On-Chip RAM: XC4000XL and Spartan-XL

The XC4000XL family is the broadest and highest-capacity 3.3 V FPGA product line in the industry, with ten devices ranging from 465 to 7,448 logic cells (about 5,000 to 85,000 logic gates). The Spartan Series of high-performance, low-cost FPGAs offers five devices ranging from 238 to 1,862 logic cells. The XC4000XL and Spartan-XL devices meet the specifications of 3.3 V PCI applications. See Chapter 4 for complete product descriptions.

#### 3.3 V FPGAs Without On-Chip RAM: XC3100L

The two members of the XC3100L FPGA family are fast 3.3 V FPGAs. See Chapter 4 for complete product descriptions.

#### 3.3 V Zero+ Family of Ultra-Low Power FPGAs: XC3000L

The XC3000L FPGA devices have quiescent supply currents below 1 mA, with some below 50 µA. See Chapter 4 for complete product descriptions.

#### 5.0 V FPGAs for Mixed-Voltage Systems: XC4000E/EX and Spartan Series

The 5.0 V XC4000E/EX and Spartan FPGA families feature a unique output structure that makes them suitable for mixed-voltage system applications. When configured in TTL mode, the XC4000E/EX and Spartan devices can be directly mixed with 3.3 V devices, as described below. See Chapter 4 for complete product descriptions.

### CPLDs

#### 5.0 V CPLDs for Mixed-Voltage Systems: XC9500

Xilinx CPLDs are an excellent fit for mixed-voltage systems. The Input/Output (I/O) ring can be powered by either a 5.0 V  $V_{CCIO}$  or a 3.3 V  $V_{CCIO}$ . Independent of the  $V_{CCIO}$  voltage level, the inputs can accept 5.0 V and 3.3 V inputs. The rail-to-rail output level is defined by  $V_{CCIO}$ . These single-chip solutions function extremely well in mixed-voltage systems without any performance penalty. See Chapter 3 for complete product descriptions.

**Table 1: Supply Voltage Options**

	<b>Device Family</b>	<b>Availability</b>	<b>Accepts 3.3 V Device Outputs<sup>1</sup></b>	<b>Drives 3.3 V Device Inputs</b>	<b>Key Features</b>
<b>Single Supply <math>V_{CC} = 5.0\text{ V}</math></b>	XC3000A	Now	Yes	With limiting resistor	Low quiescent current
	XC3100A	Now	Yes	With limiting resistor	High performance
	XC4000E/EX	Now	Yes	Yes	Highest density and performance
	Spartan	Now	Yes	Yes	High performance, low cost
	XC5200	Now	Yes	With limiting resistor	Most cost-effective
	XC9500	Now	Yes	With limiting resistor	5.0 V in-system-programmable, pin locking
<b>Single Supply <math>V_{CC} = 3.3\text{ V}</math></b>	<b>Device Family</b>	<b>Availability</b>	<b>Accepts 5.0 V Device Outputs</b>	<b>Drives 5.0 V Device Inputs</b>	<b>Key Features</b>
	XC3000L	Now	With limiting resistor	Yes	Very low powerdown & quiescent current
	XC3100L	Now	With limiting resistor	Yes	High performance
	XC4000XL	Now	Yes	Yes	Highest Density & performance
	Spartan-XL	3Q98	Yes	Yes	Cost-effective, high performance
<b>Dual Supply <math>V_{CC} = 5.0\text{ V}</math> <math>V_{CCIO} = 3.3\text{ V}</math></b>	<b>Device Family</b>	<b>Availability</b>	<b>Accepts 5.0 V Device Outputs</b>	<b>Drives 5.0 V Device Inputs</b>	<b>Key Features</b>
	XC9500	Now	Yes	Yes	Mixed-voltage system capable

Notes: 1. Device Inputs must be configured for TTL thresholds.

## Interfacing Between 5.0 V and 3.3 V Devices

Today, many designs must accommodate both 3.3 V and 5 V components on the same board. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

### 3.3 V Devices Driving Inputs on 5.0 V Devices

The lowest output High voltage ( $V_{OH}$ ) of the 3.3 V device must exceed the  $V_{IH}$  requirements of the 5.0 V device. Minimum  $V_{OH}$  for all Xilinx 3.3 V devices is 2.4 V, well above the 2.0 V minimum High level for TTL signaling. (This includes the XC3000L, XC3100L, XC4000XL, and Spartan-XL FPGA families and the XC9500 CPLD family when  $V_{CCIO} = 3.3\text{V}$ .) Thus, all Xilinx 3.3 V devices can drive inputs to devices with TTL-compatible input thresholds, including all 5.0 V Xilinx devices. (Note: Some Xilinx 5.0 V devices can be programmed for TTL or CMOS input thresholds; these devices must be configured for TTL-compatible inputs to be directly driven from a 3.3 V device.)

### 5.0 V Devices Driving Inputs on 3.3 V Devices

The highest 5.0 V device output voltage must not force excessive current into the input of the 3.3 V device. The input structures of Xilinx 3.3 V FPGAs include input protection circuits. These protection circuits in the XC3000L and XC3100L devices are designed for 3.3 V inputs. However,

the protection circuits in the XC4000XL and Spartan-XL devices are designed to withstand 5.0 V inputs.

Most 5.0 V devices have complementary CMOS outputs where  $V_{OH}$  can reach the 5.0 V rail. (All Xilinx 5.0 V FPGAs and CPLDs, except the XC4000E/EX and Spartan series devices in default TTL mode, have complementary CMOS outputs. The XC4000E/EX and Spartan devices can be set to CMOS outputs with the design software.) When driving XC3000L and XC3100L inputs (and most other 3.3 V devices) from such a 5.0 V device, the input current must be limited by a series resistor of no less than  $150\Omega$ . This guarantees an input current below 10 mA, flowing through the ESD input protection diode backwards into the 3.3 V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3 V supply voltage above its 3.6 V maximum whenever a large number of active High inputs drive the 3.3 V device, potentially causing the 3.3 V supply current to reverse direction. The 3.3 V  $V_{CC}$  power should be on before driving the device inputs from a 5.0 V device.

The I/O structures of the XC4000XL and Spartan-XL FPGAs have been designed to tolerate being driven to a 5.0 V rail by a low-impedance source. These 3.3 V FPGAs can be directly driven by 5.0 V devices with either TTL or CMOS outputs. Power supply sequencing is not a problem; the inputs can be driven to 5.0 V either before or after the 3.3 V  $V_{CC}$  power is supplied without risking damage to the devices.

In mixed voltage systems, the XC9500 CPLD family can be driven directly by 5.0 V inputs when set up for 3.3 V I/O

operation (i.e.,  $V_{CCIO} = 3.3$  V). The input protection circuits in these CPLDs are always connected to the 5.0 V  $V_{CC}$  power line, allowing them to tolerate 5.0 V inputs without the need for current-limiting resistors.

If the 5.0 V device has “totem-pole” n-channel-only outputs (as in the default setting of the XC4000E/EX and Spartan FPGA series),  $V_{OH}$  is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5.0 V supply does not exceed 5.25 V (as described in detail in the following section). Thus, the XC4000E/EX and Spartan FPGAs can directly drive any 3.3 V device without the need for current-limiting resistors.

## Using the XC4000E/EX and Spartan FPGAs in Mixed-Voltage Systems

As a default option, all XC4000E/EX and Spartan devices have a TTL-like input threshold (compatible with 3.3 V output levels) and an n-channel-only “totem-pole” or TTL-like output structure, with an n-channel transistor pulling the output to a  $V_{OH}$  level that is one threshold below  $V_{CC}$ .

At a nominal 5.0 V  $V_{CC}$ , the unloaded output High voltage  $V_{OH}$  is less than 3.7 V. When applied to the input of a device with a nominal 3.3 V  $V_{CC}$ , there is no additional input current, and the input level does not violate the conventional specification that prohibits input voltages more than 0.5 V above  $V_{CC}$ . See [Figure 1](#).

If both 5.0 V and 3.3 V supply voltages track reasonably between their maximum and minimum values, there will never be any additional input current in excess of 1 mA at any commercial or industrial operating temperature.

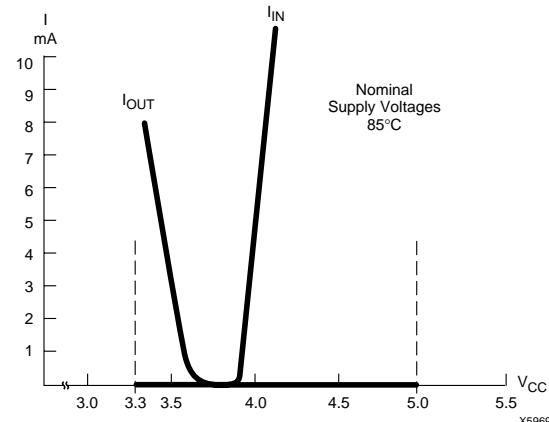
A worst-case analysis of the interface might assume the (unrealistic) condition where the 5.0 V supply is at its maximum value (5.25 V for commercial applications), while the 3.3 V supply is at its minimum value of 3.0 V. Under these conditions, the interface violates the conventional specification, and drives current into the input of the 3.3 V device, as shown in [Figure 2](#). However, as explained below, this interface is reliable.

For protection against electro-static discharge (ESD), most CMOS inputs and I/O pins usually have a diode between the pin and the nearest  $V_{CC}$  connection. This diode prevents the input from going substantially more positive than  $V_{CC}$ , which might destroy the input transistor by rupturing its gate oxide. At room temperature, this ESD protection diode conducts negligible current at  $< 0.6$  V forward bias, and conducts  $\sim 1$  mA at  $\sim 0.7$  V forward bias, typical for any silicon junction diode. These voltages have a predictable negative temperature coefficient of  $-2$  mV per degree C. At 85 degrees C, these voltages are, therefore, 120 mV lower.

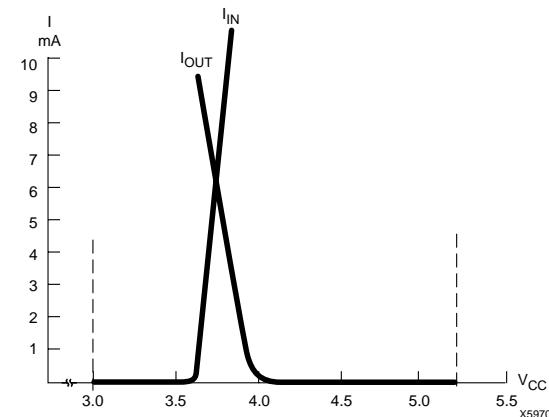
[Figure 1](#) superimposes the output characteristic of the XC4000E/EX and Spartan, and the input current character-

istic of a typical 3.3 V device input. Both supply voltages are at their nominal value, but the die temperatures are at their worst-case value of 85 degrees C, and worst-case processing is assumed.

[Figure 2](#) shows the same curves, but with 5.25 V and 3.0 V  $V_{CC}$  respectively. The intersection of the two curves defines the worst-case operating point of 3.8 V and 6 mA. That means that the XC4000E/Spartan output drives 6 mA into the forward-biased ESD protection diode, raising the input voltage 0.8 V above 3.0 V, the assumed lowest value of the nominally 3.3 V supply voltage.



**Figure 1:** XC4000E/Spartan Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Nominal Voltage (5.0 V and 3.3 V)



**Figure 2:** XC4000E/Spartan Output in “TTL-Mode” driving 3.3 V Device Input with Both Supplies at Extreme Values (5.25 V and 3.0 V)

Although this input condition is not covered by the conventional specification, it does not cause any harm and does not affect reliability. ESD protection diodes are designed to conduct hundreds of mA, and the absolute value of the input voltage with respect to ground will never exceed 3.9 V. If the input pin is part of an I/O structure, there is a theoretical possibility of causing latch-up, but all reputable IC manufacturers design their circuits such that latch-up does not occur below 100 mA of input current per pin.

The system designer must estimate the sum of all maximum input currents, and calculate the impact of this current flowing backwards towards the 3.3 V supply. But even if the total 3.3 V supply current goes to zero,  $V_{CC}$  for the 3.3 V device is still limited to < 3.6 V (the highest output voltage of the 5 V device minus the forward voltage drop of the ESD diode).

## Conclusion

5 V XC4000E/EX and Spartan devices can be freely mixed with 3.3 V devices, without any current or voltage limiting interface resistors, if the following conditions are met:

- The 5.0 V XC4000E/EX and Spartan devices are in their default "TTL mode" with respect to input thresholds and output levels.
- The upper limit on the 5 V  $V_{CC}$  is 5.25 V and the lower limit on the 3.3 V supply is 3.0 V, as per standard commercial specifications.
- For industrial operating conditions with higher  $V_{CC}$  max, the user must make sure that the absolute difference between the two supply voltages does not exceed 2.20 V. Specifically, if the nominally 5 V  $V_{CC}$  is at its max value of 5.50 V, the nominally 3.3 V  $V_{CC}$  must not be lower than 3.30 V.

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## Introduction

When a system incorporating Xilinx FPGA's moves to high volume production, HardWire FpgASIC products should be the first consideration for cost reduction. HardWire products are the only devices developed specifically for Xilinx FPGA's which provide 100% pin compatible replacements. The HardWire conversion flow coupled with the HardWire test methodology provides a no risk path for customers to achieve dramatic cost reductions. Using Xilinx FPGA's and HardWire technology provides the customer with a single source for systems, software and silicon. This combination provides the fastest method for prototype development and production of systems based on leading edge programmable logic technology. Each HardWire product family is developed to match the performance and features of specific Xilinx FPGA's including the popular XC2xxx, XC3xxx, XC4xxx and XC5xxx series families. The newest family of HardWire FpgASIC's are designed to provide a cost reduced device incorporating the latest features of Xilinx FPGA's including E, EX and XL technology.

## Technology Overview

Xilinx Hardwire ASIC products are FPGA specific ASIC's (FpgASIC's). They are a family of devices ranging from 1.0 $\mu$  single mask mapped ASIC's to state-of-the-art sea-of-gates 0.5 $\mu$  and 0.35 $\mu$  multi-mask ASIC devices. The HardWire product families have been developed to match the performance and features of each generation of Xilinx FPGA's.

The HardWire flow is the simplest method for cost reducing an FPGA based system. The Xilinx "Design Once" methodology offers Xilinx customers the advantages of developing prototypes, building pre-production and initial production volumes using Xilinx FPGAs. Once the design is stable and cost reduction is critical, customers can convert the FPGA to a HardWire device developed especially for the features and performance of that FPGA.

The turnkey conversion process allows production quality HardWire prototypes to be developed in half the time of traditional gate arrays. The HardWire methodology provides this without using customers' engineering resources. HardWire FpgASIC's provide a cost - effective alternative to gate arrays.

Xilinx HardWire product families use a combination of industry standard and Xilinx patented test generation methods to achieve the most complete fault coverage possible. This testing strategy allows Xilinx to offer a cost reduction

path that is 100% guaranteed to perform in the user's application.

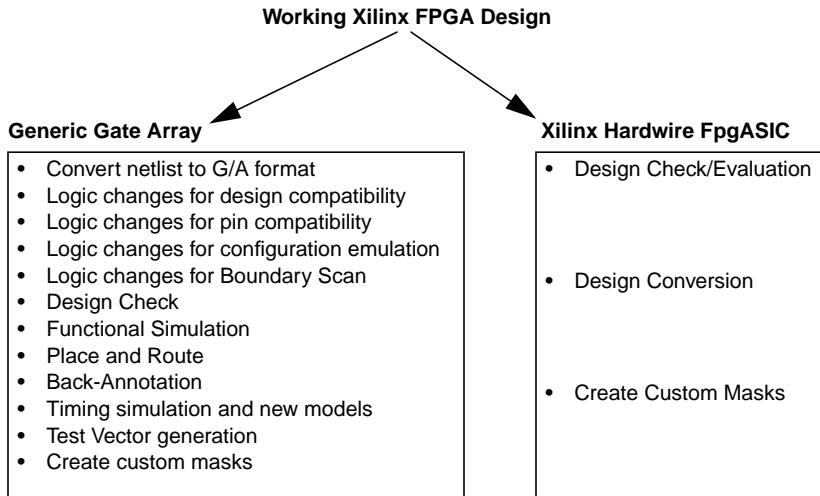
## Advantages of the Xilinx HardWire Methodology

Converting a device from programmable logic to a HardWire FpgASIC has many advantages over standard gate array redesign. The most important is that HardWire devices are developed using a fully turnkey process. No additional customer engineering is required to convert the programmable logic design into a fully tested, completely verified HardWire device. This ease of conversion is available only from Xilinx. HardWire devices are developed using the actual physical database previously created and verified in the process of developing the FPGA design. The HardWire conversion methodology preserves all the attributes of the original physical database file. If the design is mapped to a third party library at the schematic level for conversion to another technology, the design must be verified and prototyped. Third party implementations will change the placement and routing, thereby changing the design's performance characteristics. This means the new device must be re-verified and re-tested in the system to be certain that the performance and functionality still meet the applications requirements. A comparison of the activities required to convert a HardWire FpgASIC versus a generic gate array is shown in [Figure 1](#).

## Re-verifying the Design

In conventional gate array conversion (redesign), the design must be re-verified after the schematic is translated or recaptured. The process of re-verifying a design is rigorous and time consuming. Functional simulation vectors need to be created, and the device must be exhaustively simulated before and after place and route. A suitable test methodology must be considered and implemented. All this is usually done by the customer, at the customers' expense and risk.

In contrast, no additional effort is required when converting to a HardWire FpgASIC. The HardWire design is self-verifying because the actual FPGA database files are used for the conversion. This makes the HardWire conversion process the only guaranteed, fully turnkey FpgASIC conversion.



**Figure 1: Steps Involved in Converting a PLD Design to a Gate Array as Compared to a HardWire FpgASIC**

## Fault Coverage and Test Vectors

All designs need to be testable. In a traditional gate array, the designer is required to build in testability and generate test vectors to verify chip performance by exercising as much of the device circuitry as possible. Most designers strive for greater than 90% fault coverage. However, they often settle for significantly less because the iterative process is time consuming and increases exponentially as fault coverage is increased. A third party conversion from a Xilinx FPGA to a generic gate array or other similar technology will require test vector generation. Typically, the original designers create test vectors, since they are most familiar with the FPGA's design. This method misuses valuable design resources and reverses the value of the decision to use programmable logic for their ease of design and time-to-market advantage. Another method is to contract with the conversion or gate array vendor to create the test vectors. This method is both expensive and time consuming. In some cases, conversion or gate array vendors will accept a design without test vectors, but the customer accepts the liability of determining whether the resulting device is production worthy. In today's competitive market, most projects can not afford the risk of possible re-spins if the design doesn't work.

Converting from a Xilinx FPGA to a HardWire FpgASIC requires no test vector generation by the customer. HardWire devices use a combination of industry standard and Xilinx patented test generation methods to achieve the most complete fault coverage possible. Xilinx guarantees greater than 95% fault coverage for most designs. All HardWire FpgASIC's are tested using a full scan test methodology. The HardWire conversion and test methodology provides a cost reduction path that is guaranteed to work in the customer's application.

## Packaging and Silicon Considerations

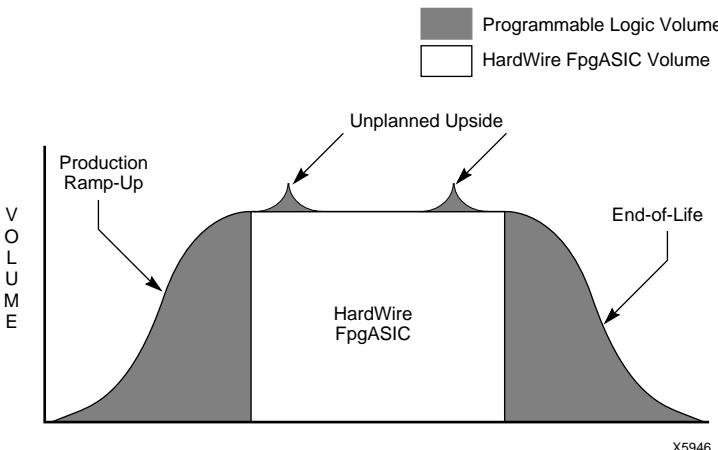
All of the physical attributes of HardWire FpgASIC's are virtually identical to the Xilinx FPGA. HardWire devices are manufactured in the same fabrication facilities used by Xilinx for the production of FPGA's. The same design rules, IC process, as well as packaging, assembly, and test facilities are used. This allows a significant reduction in the time and cost associated with qualifying HardWire devices.

Converting from a Xilinx programmable logic device to any third party device means a change in silicon, packaging, assembly and test. Each of these changes adds an element of risk into the qualification process.

## Support for the entire Product Life Cycle

Figure 2 shows the typical life cycle of a high-volume product. It illustrates the optimal way of using the programmable and HardWire devices. During development, prototyping and initial production cycles, the programmable device is the best choice. As the system moves into higher volume production and no additional modifications are being made to the design, a HardWire FpgASIC can be used in place of the original programmable logic device.

Since the HardWire device and the programmable logic device are functionally and physically identical, production can be switched back to the programmable device if the situation warrants. For example, if the demand for the customer's product increases dramatically, production can be increased immediately by full-filling the additional demand with programmable devices. The change can be made immediately since there is virtually no lead-time for an off-



**Figure 2: Typical High Volume Product Life Cycle**

the-shelf programmable device. Production can also be switched to the programmable device as the product ends its life cycle and volume decreases. This eliminates the need for end-of-life buys and the risk of obsolescence.

Furthermore, designs implemented with multiple static RAM based programmable devices can be cost reduced incrementally, converting one or more of the programmable devices to a HardWire FpgASIC with the balance remaining as FPGAs. As each FPGA is converted to a HardWire device, the user benefits by having a lower cost for that device. This also allows the user to maintain the ease of use of off-the-shelf programmable logic in the other sockets. When all of the devices are converted, the storage element (PROM) can be removed, giving even further cost reductions. This flexibility is unique to Xilinx, and allows customers to achieve cost reduction quickly with minimal effort.

## HardWire Design/ Production Interface

Figure 3 illustrates how the design, development and production activities for both Programmable Logic devices and HardWire FpgASCs are sequenced. Notice that by using the Xilinx "Design Once" methodology, no additional customer activity is needed to develop the HardWire FpgASIC. If design simulation is done in the programmable logic device during development, special HardWire speed files may be also be used for design verification. This allows Xilinx to perform a very simple design check procedure prior to generating the HardWire device. After the design check is complete the HardWire prototypes can be manufactured. The customer then performs in-system verification of the prototypes. Once this verification is complete the HardWire FpgASIC can be released to production. Since the func-

tionality of the FPGA and HardWire device are identical, virtually no customer engineering resources are needed to move from the programmable to the HardWire devices or vice versa. By comparison, using a traditional gate array to reproduce functions implemented in the FPGA would require extensive simulation and test development.

## Design Submittal Process

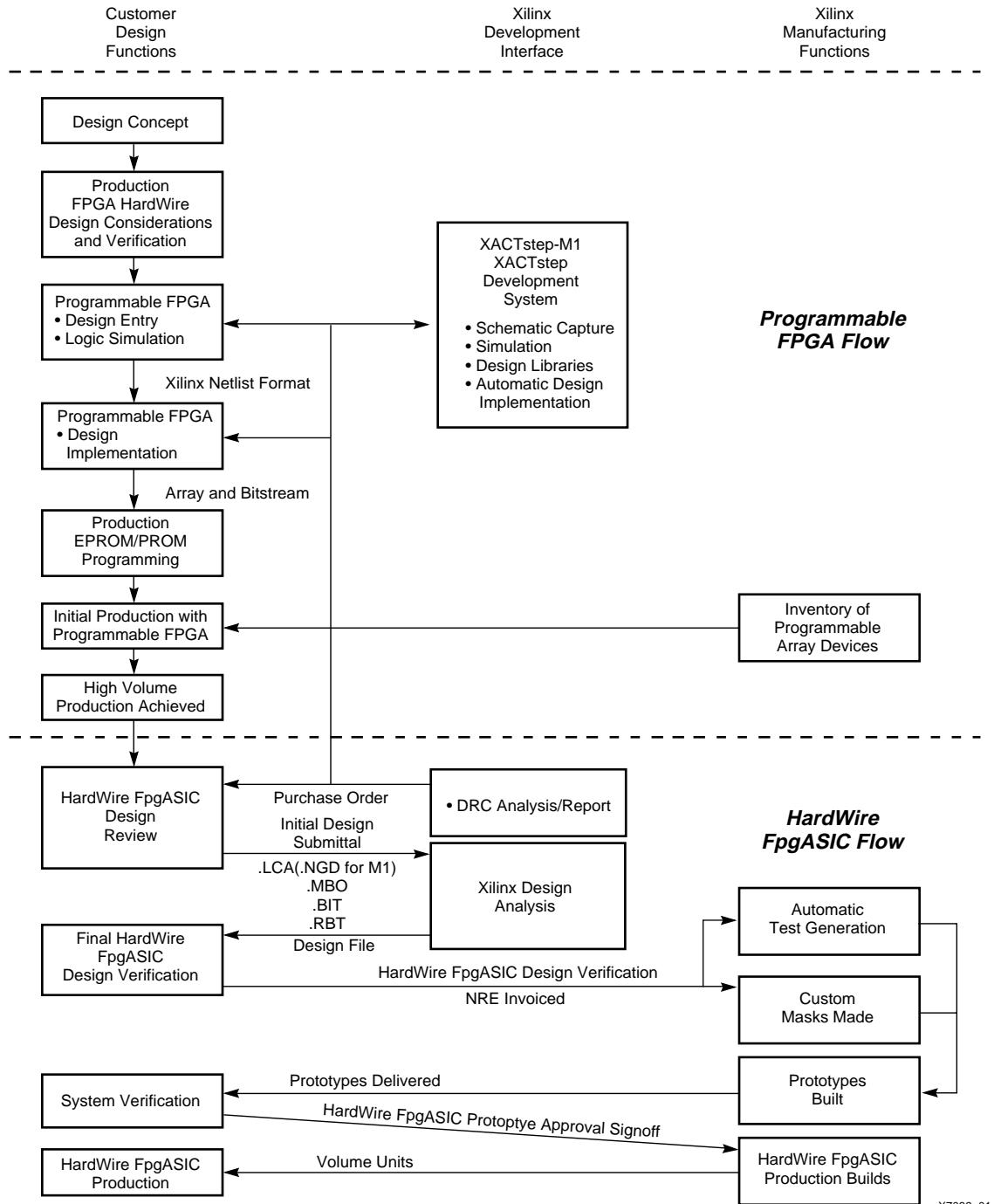
Once the complete design submittal kit is received the HardWire conversion process takes from 3 to 8 weeks. The conversion time will vary with the addition of features such as Select-RAM, Configuration Emulation and JTAG. A complete design submittal kit contains the following:

1. Files: .LCA (or .NGD for M1 designs), .MBO, and .BIT files on disk.
2. Hard copy of a board level schematic showing how the FPGA interfaces with other components on the board (if possible).
3. A detailed explanation of any special requirements for the conversion.
4. A design submittal form and NRE PO.

All forms can be found in the HardWire data book and on the Xilinx web page under HardWire products.

## Summary of the Conversion Process

The HardWire FpgASIC conversion process is the simplest way to cost reduce systems designed using FPGAs. The customer is involved in tracking and approving milestones. Xilinx handles the day-to-day activities of converting the design to a HardWire device. Once Xilinx receives a complete design submittal kit the conversion process begins.



X7089\_01

**Figure 3: Programmable/HardWire Design/Production Interface**

**Table 1: HardWire Products**

Device Family	Speed Grade	Features Supported	Hardwire FpgASIC Family	Notes
XC2xxx	All	All	XC2318	1
XC3xxx	All	All	XC33xx	1
XC4xxx	-4 and slower	No E features	XC43xx	1
XC4xxxE/EX/XL	-3 and slower	E, EX, XL	XC44xx	
XC4xxxE/EX/XL	-3 and faster	E, EX, XL	XH3xx	
XC5xxx	All	Non XL	XC54xx	

Note 1: Some devices require re-routing before conversion. Refer to the HardWire Data Book

Xilinx first reviews the design to determine any items that could impact the performance of the HardWire device. A conversion evaluation report is sent to the customer. After the report has been reviewed and the customer is satisfied, conversion begins. At the completion of the conversion a Design Verification Report and Design Verification Form (DVF) are sent to the customer. Once the DVF is completed the HardWire files are sent to the mask shop for prototyping. If any custom markings are required they must be submitted to Xilinx with the Design Verification Form (DVF). Prototypes are produced, tested and shipped to the customer for in-system testing. The customer signs the prototype approval form and returns it to Xilinx. Production can begin.

## HardWire Product Families

Each HardWire product family is developed to support the features, density and performance of a specific generation of Xilinx FPGA's. See [Table 1](#) for product family details. For designs developed using Xilinx XC2xxx, XC3xxx or XC4xxx (no E features) FPGA's, the XC23xx, XC33xx and 43xx product families provide a fast and simple cost reduction path. For designs developed using Xilinx XC4xxx (E, EX and XL) and XC5xxx FPGA's, the XC44xx and XC54xx product families provide the most effective technology, cost and performance. For customers using fast, dense Xilinx XC4xxxE, EX and XL or XC5xxx FPGA's the XH3 product family provides the most efficient and cost effective solution available. Most HardWire FpgASIC's are available in 3.3v versions. All HardWire devices support commercial and industrial temperature ranges.

## Xilinx HardWire Product Descriptions

### XC23xx, XC33xx and XC43xx Product Description

The initial HardWire product family was developed to match the performance of Xilinx XC2xxx, XC3xxx and slower XC4xxx family FPGA's. This family is still in production today. In standard programmable logic, the functions and interconnections are determined by configuration data stored in memory cells. In the first generation HardWire

technology, the memory cells and programmable interconnect logic they control are replaced by metal connections. All other circuitry in the resulting HardWire device is identical to the corresponding FPGA internal circuitry. The resulting HardWire FpgASIC is a semi-custom device manufactured to provide a specific function, yet it is completely compatible with the FPGA. This product family is the fastest and most simple method of converting first generation Xilinx FPGA's. For more details on XC23xx, XC33xx and XC43xx products please see the Xilinx HardWire Data Book.

### XC23xx, XC33xx and XC43xx Summary

#### Features

- Designed for conversion of XC2xxx, XC3xxx and XC4xxx (no E features) FPGA's.
- Single Mask
- Direct Mapped - Turnkey conversion from FPGA device.
- On-chip scan path test latches.
- Fully pin-for-pin compatible.

#### Benefits

- Simple and efficient conversion process.
- Very fast conversion completion time.
- Conversion success rate over 95%.
- No customer developed test vectors needed, 99% fault coverage.
- Drop-in replacement for Xilinx FPGA's.

### XC44xxE/EX/XL and XC54xx Product Description

The second generation HardWire FpgASIC product family was developed to match the performance, density and features of Xilinx XC4xxxE, EX, XL and XC5xxx family of FPGA's. This HardWire FpgASIC product family supports all the features of Xilinx second generation FPGA's. This includes -3 speed grades, Configuration Emulation (CE), JTAG and Select-RAM. The XC44xx and XC54xx product family follows a more traditional sea-of-gates approach to mapping used CLBs of the FPGA. The used memory cells and programmable interconnect logic of the FPGA are mapped into a corresponding area of a traditional gate

array base. The FPGA's unused CLBs are not mapped into the resulting HardWire device. The HardWire device uses the smallest base array possible while maintaining the performance and functionality of the corresponding FPGA. These devices support most 3.3 volt and 5 volt FPGAs. The feature sizes of the arrays used in the XC44xx and XC54xx product family ( $1.0\mu$  through  $.45\mu$ ) are highly competitive with traditional gate arrays. The wide range of base array feature sizes available allows Xilinx to provide a HardWire device with the smallest possible die size. The same guaranteed turnkey conversion methodology is used. XC44xx and XC54xx devices provide the most cost-effective method for converting XC4xxxE, XC4xxxEX, XC4xxxXL and XC52xx FPGA's to a low cost HardWire FpgASIC.

## XC44xx/E/EX/XL and XC54XX Summary

### Features

- Designed for conversion of XC4xxxE, EX, XL and XC5xxx FPGAs.
- Only used CLBs are mapped.
- Multiple mask, state-of-the-art, gate array process.
- On-chip scan path test latches.
- Fully pin-for-pin compatible.
- Smallest possible die size.

### Benefits

- All Xilinx FPGA features supported, including CE, JTAG and Select-RAM.
- Smallest possible die size used to achieve the lowest possible cost.
- Technology feature size matched to performance requirements.
- No customer developed test vectors needed. Greater than 95% fault coverage (design dependent).
- Drop in replacement for Xilinx FPGAs.

## XH3 Product Description

The third generation HardWire FpgASIC product family, known as XH3, was developed to match the density, performance and features of the fastest, most fully featured Xilinx XC4xxxEX, XL and XC5xxx family of FPGAs. Initial XH3 products are based on  $0.5\mu$ , 5-volt process technology, followed by  $0.35\mu$ , 3.3-volt XH3L technology. XH3 technology was developed specifically for Xilinx FPGA conversions. It uses a dense sea-of-gates CMOS gate array technology. At  $0.5\mu$  and  $0.35\mu$ , the process geometry is small enough that die sizes are driven by pad count and not gate count.

Important features used in Xilinx FPGAs such as Configuration Emulation, JTAG, and Select-RAM are easily implemented in XH3 technology. The control logic for Configuration Emulation, Power on Reset (POR), Oscillators and full JTAG are built into the XH3 base array. These features can usually be implemented with no additional silicon overhead. RAM blocks are incorporated with maxi-

mum efficiency. The XH3 architecture implements Select-RAM 30% more efficiently than generic gate arrays.

In generic gate array methodologies, features such as Configuration Emulation, JTAG and Select-RAM usually require additional silicon area. The result is a larger, more expensive die and changes to the FPGA netlist throughout the conversion process. In many cases implementing Xilinx Select-RAM in a third party gate array may require substantially more gates than the Xilinx XH3 device. XH3 devices incorporate these features without silicon overhead or changes to the netlist.

## XH3 Summary

### Features

- Designed for conversion of XC4xxxE, EX, XL and XC5xxx FPGAs.
- Xilinx FPGA features built in to the base array.
- Multiple Mask, state-of-the-art  $0.5\mu$  and  $0.35\mu$  process technology.
- Pad counts and gate counts available for the densest FPGA devices.
- On chip scan path test latches.
- Fully pin for pin compatible.
- Package flexibility available.

### Benefits

- All Xilinx FPGA features supported, including CE, JTAG and Select-RAM.
- Patented, turnkey conversion flow.
- Pads and package required determine device used.
- No customer developed test vectors needed. Greater than 95% fault coverage (design dependent).
- Drop in replacement for Xilinx FPGAs.
- Conversions to smaller packages available.

## HardWire Summary

Xilinx Hardwire ASIC products are FPGA specific ASIC's (FpgASIC's). They are a family of devices ranging from  $1.0\mu$  single mask mapped ASIC's to state-of-the-art sea-of-gates  $0.5\mu$  and  $0.35\mu$  multi-mask ASIC devices. The HardWire flow is the most simple method of cost reduction for FPGA based systems. They are developed using the FPGA's design files. This guarantees the HardWire FpgASIC will be functionally equivalent to the FPGA. No customer generated test vectors are required with HardWire. Each HardWire device is tested using a combination of industry standard and Xilinx patented test methods in a full scan methodology. The full scan test methodology provides greater than 95% fault coverage depending on the design. HardWire prototypes can be developed in half the time of traditional gate array prototypes. HardWire process technologies, conversion methods and testing procedures provide the most cost - effective alternative to traditional gate arrays.



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March 16, 1998 (version 1.2)

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Xilinx is the world's leading supplier of High-Reliability Programmable Logic Devices (Hi-REL PLDs) to the aerospace, military, defense electronics, and related markets. These devices are being used in a wide variety of programs, including applications such as electronic warfare, missile guidance and targeting, RADAR/SONAR, communications, signal processing, aerospace and avionics.

## QML Certification Part of Overall Quality Platform

Being certified to MIL-PRF-38535 QML (Qualified Manufacturer List), complemented by ISO-9000 Certification, results in an overall product quality platform that truly makes Xilinx a world-class supplier of programmable logic. Designers can confidently design with Xilinx for Hi-Rel systems knowing there is unsurpassed quality and reliability, and long-term commitment to the Hi-Rel market.

## Unmatched Hi-Rel Product Offering

Xilinx offers a wide variety of devices, delivering the fastest and biggest Hi-Rel devices available. Products up to 62,000 gates are available today, with even higher densities to come. Xilinx offers multiple product families to allow you to select the right device to meet your design requirements.

This broad range of devices is available in a wide variety of speed and package options. Both military temperature and full MIL-PRF-38535 QML/SMD versions are available as standard, off-the-shelf products, in through-hole and surface mount packages.

**Table 1: High Density and High Performance Products**

Family	Devices	Features
XC4000/E/XL	XC4003A XC4005/E XC4010/E XC4013/E XC4025E	Highest Density/Most Features Family <ul style="list-style-type: none"><li>• 3,000-25,000+ gates</li><li>• Up to 256 user-definable I/Os</li><li>• Extensive system features include on-chip user RAM, built-in 1149.1 test support and fast carry logic</li></ul>
	XC4036XL XC4062XL	Most Advanced Family <ul style="list-style-type: none"><li>• 62,000 + gates, 3.3 V, 5V-compatible I/O</li></ul>
XC3100A	XC3142A XC3190A XC3195A	Highest Performance Family <ul style="list-style-type: none"><li>• 2,500-7,500 gates</li><li>• Up to 144 user-definable I/Os</li></ul>

## Committed to the Hi-Rel Market

Xilinx understands that you need to be able to count on your Hi-Rel supplier. Xilinx is committed to our customers and the Hi-Rel market for the long-term, and we are continually expanding our Hi-Rel support and product portfolio. The unique capabilities of the Xilinx FPGA solution provide increased design flexibility, field-upgradability and system feature integration, while eliminating the NREs, lead-time and inventory problems of custom logic and gate arrays. Now more than ever, Xilinx is your Hi-Rel logic solution.

## Die Products

Xilinx also provides select products in die form. Working with our partner, Chip Supply of Orlando, Florida, many Xilinx products are available in die form, providing all the advantages of Xilinx FPGAs to designers of hybrids and multi-chip modules. For more information about Xilinx die products, contact the nearest Xilinx Sales office or Sales Representative, or Chip Supply direct at (407)298-7100.

## Xilinx Hi-Rel Products

**Table 1** summarizes Xilinx high density and high performance product offerings. The following pages contain a complete listing of current Xilinx QML/SMD (Standard Microcircuit Drawings) devices and "B" grade equivalents. Architectural descriptions for these FPGA products can be found in Chapter 4. For additional information, contact the nearest Xilinx Sales Office or Sales Representative.

**Table 2: Xilinx SMD (Standard Microcircuit Drawing)****XC1700 Products**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9471701MPA	XC1765DDD8B		DD8	TOP
5962-9561701MPA	XC17256DDD8B		DD8	TOP

**XC2000 Products\***

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8863803XC	XC2018-50PG84B	-50	PG84	TOP
5962-8863804XC	XC2018-70PG84B	-70	PG84	TOP
5962-8863805XC	XC2018-100PG84B	-100	PG84	TOP

\* Do Not Use for New Designs. (Products being obsoleted).

**XC3000 Products**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8994801MXC	XC3020-50PG84B	-50	PG84	TOP
5962-8994802MXC	XC3020-70PG84B	-70	PG84	TOP
5962-8994803MXC	XC3020-100PG84B	-100	PG84	TOP
5962-8994801MNC	XC3020-50CB100B	-50	CB100	BASE
5962-8994802MNC	XC3020-70CB100B	-70	CB100	BASE
5962-8994803MNC	XC3020-100CB100B	-100	CB100	BASE
5962-8994801MMC	XC3020-50CB100B	-50	CB100	LID
5962-8994802MMC	XC3020-70CB100B	-70	CB100	LID
5962-8994803MMC	XC3020-100CB100B	-100	CB100	LID
5962-8994801MYA*	XC3020-50CQ100B	-50	CQ100	BASE
5962-8994802MYA*	XC3020-70CQ100B	-70	CQ100	BASE
5962-8994803MYA*	XC3020-100CQ100B	-100	CQ100	BASE
5962-8994801MTA*	XC3020-50CQ100B	-50	CQ100	LID
5962-8994802MTA*	XC3020-70CQ100B	-70	CQ100	LID
5962-8994803MTA*	XC3020-100CQ100B	-100	CQ100	LID

\* Do Not Use for New Designs (package is obsolete). Use "CB" Package Instead.

**XC3000 Products (continued)**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8971301MXC	XC3042-50PG84B	-50	PG84	TOP
5962-8971302MXC	XC3042-70PG84B	-70	PG84	TOP
5962-8971303MXC	XC3042-100PG84B	-100	PG84	TOP
5962-8971301MZC	XC3042-50PG132B	-50	PG132	TOP
5962-8971302MZC	XC3042-70PG132B	-70	PG132	TOP
5962-8971303MZC	XC3042-100PG132B	-100	PG132	TOP
5962-8971301M9C	XC3042-50CB100B	-50	CB100	BASE
5962-8971302M9C	XC3042-70CB100B	-70	CB100	BASE
5962-8971303M9C	XC3042-100CB100B	-100	CB100	BASE
5962-8971301MMC	XC3042-50CB100B	-50	CB100	LID
5962-8971302MMC	XC3042-70CB100B	-70	CB100	LID
5962-8971303MMC	XC3042-100CB100B	-100	CB100	LID
5962-8971301MYA*	XC3042-50CQ100B	-50	CQ100	BASE
5962-8971302MYA*	XC3042-70CQ100B	-70	CQ100	BASE
5962-8971303MYA*	XC3042-100CQ100B	-100	CQ100	BASE
5962-8971301MNA*	XC3042-50CQ100B	-50	CQ100	LID
5962-8971302MNA*	XC3042-70CQ100B	-70	CQ100	LID
5962-8971303MNA*	XC3042-100CQ100B	-100	CQ100	LID

\* Do Not Use for New Designs (package is obsolete). Use "CB" Package Instead.

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-8982301MXC	XC3090-50PG175B	-50	PG175	TOP
5962-8982302MXC	XC3090-70PG175B	-70	PG175	TOP
5962-8982303MXC	XC3090-100PG175B	-100	PG175	TOP
5962-8982301MZC	XC3090-50CB164B	-50	CB164	BASE
5962-8982302MZC	XC3090-70CB164B	-70	CB164	BASE
5962-8982303MZC	XC3090-100CB164B	-100	CB164	BASE
5962-8982301MTC	XC3090-50CB164B	-50	CB164	LID
5962-8982302MTC	XC3090-70CB164B	-70	CB164	LID
5962-8982303MTC	XC3090-100CB164B	-100	CB164	LID
5962-8982301MYA*	XC3090-50CQ164B	-50	CQ164	BASE
5962-8982302MYA*	XC3090-70CQ164B	-70	CQ164	BASE
5962-8982303MYA*	XC3090-100CQ164B	-100	CQ164	BASE
5962-8982301MUA*	XC3090-50CQ164B	-50	CQ164	LID
5962-8982302MUA*	XC3090-70CQ164B	-70	CQ164	LID
5962-8982303MUA*	XC3090-100CQ164B	-100	CQ164	LID

\* Package OBSOLETE. Use "CB" Package Instead.

**XC3100A Products**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9561001MXC	XC3142A-5PG84B	-5	PG84	TOP
5962-9561002MXC	XC3142A-4PG84B	-4	PG84	TOP
5962-9561001MUC	XC3142A-5PG132B	-5	PG132	TOP
5962-9561002MUC	XC3142A-4PG132B	-4	PG132	TOP
5962-9561001MYC	XC3142A-5CB100B	-5	CB100	BASE
5962-9561002MYC	XC3142A-4CB100B	-4	CB100	BASE
5962-9561001MZC	XC3142A-5CB100B	-5	CB100	LID
5962-9561002MZC	XC3142A-4CB100B	-4	CB100	LID
5962-9561101MXC	XC3190A-5PG175B	-5	PG175	TOP
5962-9561102MXC	XC3190A-4PG175B	-4	PG175	TOP
5962-9561101MYC	XC3190A-5CB164B	-5	CB164	BASE
5962-9561102MYC	XC3190A-4CB164B	-4	CB164	BASE
5962-9561101MZC	XC3190A-5CB164B	-5	CB164	LID
5962-9561102MZC	XC3190A-4CB164B	-4	CB164	LID
5962-9561201MXC	XC3195A-5PG175B	-5	PG175	TOP
5962-9561202MXC	XC3195A-4PG175B	-4	PG175	TOP
5962-9561201MYC	XC3195A-5CB164B	-5	CB164	BASE
5962-9561202MYC	XC3195A-4CB164B	-4	CB164	BASE
5962-9561201MZC	XC3195A-5CB164B	-5	CB164	LID
5962-9561202MZC	XC3195A-4CB164B	-4	CB164	LID

**XC4000 Products**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9471201MXC	XC4003A-10PG120B	-10	PG120	TOP
5962-9471202MXC	XC4003A-6PG120B	-6	PG120	TOP
5962-9471201MYC	XC4003A-10CB100B	-10	CB100	BASE
5962-9471202MYC	XC4003A-6CB100B	-6	CB100	BASE
5962-9471201MZC	XC4003A-10CB100B	-10	CB100	LID
5962-9471202MZC	XC4003A-6CB100B	-6	CB100	LID
5962-9225201MXC	XC4005-10PG156B	-10	PG156	TOP
5962-9225202MXC	XC4005-6PG156B	-6	PG156	TOP
5962-9225203MXC	XC4005-5PG156B	-5	PG156	TOP
5962-9225201MYC	XC4005-10CB164B	-10	CB164	LID
5962-9225202MYC	XC4005-6CB164B	-6	CB164	LID
5962-9225203MYC	XC4005-5CB164B	-5	CB164	LID
5962-9225201MZC	XC4005-10CB164B	-10	CB164	BASE
5962-9225202MZC	XC4005-6CB164B	-6	CB164	BASE
5962-9225203MZC	XC4005-5CB164B	-5	CB164	BASE

**XC4000 Products (continued)**

SMD Number	Equivalent "B" Grade P/N	Speed	Package	Mark Loc
5962-9752201QXC	XC4005E-4PG156B	-4	PG156	TOP
5962-9752201QYC	XC4005E-4CB164B	-4	CB164	BASE
5962-9752201QZC	XC4005E-4CB164B	-4	CB164	LID
5962-9230501M XC	XC4010-10PG191B	-10	PG191	TOP
5962-9230502M XC	XC4010-6PG191B	-6	PG191	TOP
5962-9230503M XC	XC4010-5PG191B	-5	PG191	TOP
5962-9230501MYC	XC4010-10CB196B	-10	CB196	BASE
5962-9230502MYC	XC4010-6CB196B	-6	CB196	BASE
5962-9230503MYC	XC4010-5CB196B	-5	CB196	BASE
5962-9230501MZC	XC4010-10CB196B	-10	CB196	LID
5962-9230502MZC	XC4010-6CB196B	-6	CB196	LID
5962-9230503MZC	XC4010-5CB196B	-5	CB196	LID
5962-9752301QXC	XC4010E-4PG191B	-4	PG191	TOP
5962-9752301QYC	XC4010E-4CB196B	-4	CB196	BASE
5962-9752301QZC	XC4010E-4CB196B	-4	CB196	LID
5962-9473001M XC	XC4013-10PG223B	-10	PG223	TOP
5962-9473002M XC	XC4013-6PG223B	-6	PG223	TOP
5962-9473001MYC	XC4013-10CB228B	-10	CB228	BASE
5962-9473002MYC	XC4013-6CB228B	-6	CB228	BASE
5962-9473001MZC	XC4013-10CB228B	-10	CB228	LID
5962-9473002MZC	XC4013-6CB228B	-6	CB228	LID
5962-9752401QXC	XC4013E-4PG223B	-4	PG223	TOP
5962-9752401QYC	XC4013E-4CB228B	-4	CB228	BASE
5962-9752401QZC	XC4013E-4CB228B	-4	CB228	LID
5962-9752501QXC	XC4025E-4PG299B	-4	PG299	TOP
5962-9752501QYC	XC4025E-4CB228B	-4	CB228	BASE
5962-9752501QZC	XC4025E-4CB228B	-4	CB228	LID

**Table 3: Revision History**

Version	Description
1/98, doc version 1.1	High-Reliability and QML Military Products, correct erroneous information page 2 "XC3000 Products", delete last page, table - "Mil-PRF-3853 QML, Xilinx M Grade and Plastic Commercial Flows"



## QPRO™ XQR4000XL Radiation Hardened Field Programmable Gate Arrays

October 5, 1998 (Version 1.0)

Preliminary Product Specification

### XQR4000XL Series Features

- Radiation Hardened FPGAs for space and satellite applications
- Guaranteed Total Ionizing Dose
- Latch-up Immune
- Low Soft Upset Rate
- Guaranteed to meet full electrical specifications over - 55°C to +125°C
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features

- IEEE 1149.1-compatible boundary scan logic support
- Individually programmable output slew rate
- Programmable input pull-up or pull-down resistors
- 12-mA sink current per output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity - over 130,000 usable gates
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- Advanced 0.35 $\mu$  process
- Processed on Xilinx's QML Line

Table 1: XQR4000X Series Radiation Hardened Field Programmable Gate Arrays

Device	Logic Cells	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQR4013XL	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	CB228
XQR4036XL	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	CB228
XQR4062XL	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	CB228

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

## Radiation Specifications

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose		60K	RAD(Si)
SEL	Single Event Latch-up LET> 100 MeV CM <sup>2</sup> /mg. @ +125°C		0	
SEU	Single Event Upset Galactic p+ (Note 1)		2.43E-8	Upsets/ Bit-Day
SEU	Single Event Upset Galactic Heavy Ion (Note 1)		9.54E-8	Upsets/ Bit-Day
SEU	Single Event Upset Trapped p+ (Note 1)		2.50E-7	Upsets/ Bit-Day
SEU	Single Event Upset Galactic p+ (Note 2)		5.62E-8	Upsets/ Bit-Day
SEU	Single Event Upset Galactic Heavy Ion (Note 2)		2.43E-7	Upsets/ Bit-Day

Note 1: 680 Km LEO, 98° Inclination, 100 Mil Al Shielding

Note 2: 35,000 Km GEO, 0° Inclination, 100 Mil Al Shielding

Note 3: Simulations done using Space Radiation Version 2.5 code from Severn Communication Corp.

## XQR4000XL Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered final.

All specifications subject to change without notice.

### Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family a.c. supplements available on the Xilinx WEBLINX at <http://www.xilinx.com>.

## Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$V_{CCT}$	Longest Supply Voltage Rise Time from 1 V to 3V	50	ms
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	+150	°C

Note 1: Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions

Symbol	Description	Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_C = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	3.0	3.6	V
$V_{IH}$	High-level input voltage	50% of $V_{CC}$	5.5	V
$V_{IL}$	Low-level input voltage	0	30% of $V_{CC}$	V
$T_{IN}$	Input signal transition time		250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output measurement threshold is ~50% of  $V_{CC}$ .

## XQR4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0 \text{ mA}$ , $V_{CC}$ min (LVTTL)	2.4		V
	High-level output voltage @ $I_{OH} = -500 \mu\text{A}$ , (LVCMOS)	90% $V_{CC}$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0 \text{ mA}$ , $V_{CC}$ min (LVTTL) (Note 1)		0.4	V
	Low-level output voltage @ $I_{OL} = 1500 \mu\text{A}$ , (LVCMOS)		10% $V_{CC}$	V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)	2.5		V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)		20	mA
$I_L$	Input or output leakage current	-10	+10	$\mu\text{A}$
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0 \text{ V}$ (sample tested)	0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6 \text{ V}$ (sample tested)	0.02	0.15	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low	0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

## XQR4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the

Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>	<b>-3</b>	<b>Units</b>
				<b>Max</b>	
From pad through Global Low Skew buffer, to any clock K	T <sub>GLS</sub>	XQR4013XL XQR4036XL XQR4062XL	3.6 4.8 6.3	ns ns ns	
From pad through Global Early buffer, to any IOB clockK. Values are for BUFGE #s 1, 2, 5 and 6. Add 1 - 2 ns for BUFGE #s 3, 4, 7 and 8 and for all CLB clock Ks driven from any of the 8 BUFGEs, or consult TRCE.	T <sub>GE</sub>	XQR4013XL XQR4036XL XQR4062XL	2.4 3.1 4.9	ns ns ns	

## XQR4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQR4000XL devices and expressed in nanoseconds unless otherwise noted.

Speed Grade		-3		Units
Description	Symbol	Min	Max	
<b>Combinatorial Delays</b>				
F/G inputs to X/Y outputs	$T_{ILO}$		1.6	ns
F/G inputs via H' to X/Y outputs	$T_{IHO}$		2.7	ns
F/G inputs via transparent latch to Q outputs	$T_{ITO}$		2.9	ns
C inputs via SR/H0 via H to X/Y outputs	$T_{HH0O}$		2.5	ns
C inputs via H1 via H to X/Y outputs	$T_{HH1O}$		2.4	ns
C inputs via DIN/H2 via H to X/Y outputs	$T_{HH2O}$		2.5	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	$T_{CBYP}$		1.5	ns
<b>CLB Fast Carry Logic</b>				
Operand inputs (F1, F2, G1, G4) to $C_{OUT}$	$T_{OPCY}$		2.7	ns
Add/Subtract input (F3) to $C_{OUT}$	$T_{ASCY}$		3.3	ns
Initialization inputs (F1, F3) to $C_{OUT}$	$T_{INCY}$		2.0	ns
$C_{IN}$ through function generators to X/Y outputs	$T_{SUM}$		2.8	ns
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$		0.26	ns
Carry Net Delay, $C_{OUT}$ to $C_{IN}$	$T_{NET}$		0.32	ns
<b>Sequential Delays</b>				
Clock K to Flip-Flop outputs Q	$T_{CKO}$		2.1	ns
Clock K to Latch outputs Q	$T_{CKLO}$		2.1	ns
<b>Setup Time before Clock K</b>				
F/G inputs	$T_{ICK}$	1.3		ns
F/G inputs via H	$T_{IHCK}$	2.3		ns
C inputs via H0 through H	$T_{HH0CK}$	2.0		ns
C inputs via H1 through H	$T_{HH1CK}$	1.9		ns
C inputs via H2 through H	$T_{HH2CK}$	2.0		ns
C inputs via DIN	$T_{DICK}$	0.9		ns
C inputs via EC	$T_{ECK}$	1.0		ns
C inputs via S/R, going Low (inactive)	$T_{RCK}$	0.6		ns
$C_{IN}$ input via F/G	$T_{CCK}$	2.3		ns
$C_{IN}$ input via F/G and H	$T_{CHCK}$	3.4		ns
<b>Hold Time after Clock K</b>				
F/G inputs	$T_{CKI}$	0		ns
F/G inputs via H	$T_{CKIH}$	0		ns
C inputs via SR/H0 through H	$T_{CKHH0}$	0		ns
C inputs via H1 through H	$T_{CKHH1}$	0		ns
C inputs via DIN/H2 through H	$T_{CKHH2}$	0		ns
C inputs via DIN/H2	$T_{CKDI}$	0		ns
C inputs via EC	$T_{CKEC}$	0		ns
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		ns
<b>Clock</b>				
Clock High time	$T_{CH}$	3.0		ns
Clock Low time	$T_{CL}$	3.0		ns
<b>Set/Reset Direct</b>				
Width (High)	$T_{RPW}$	3.0		ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		3.7	ns
<b>Global Set/Reset</b>				
Minimum GSR Pulse Width	$T_{MRW}$		19.8	ns
Delay from GSR input to any Q	$T_{MRQ}$	See page 14 for $T_{RRI}$ values per device.		
<b>Toggle Frequency (MHz)</b> (for export control)	$F_{TOG}$		166	MHz

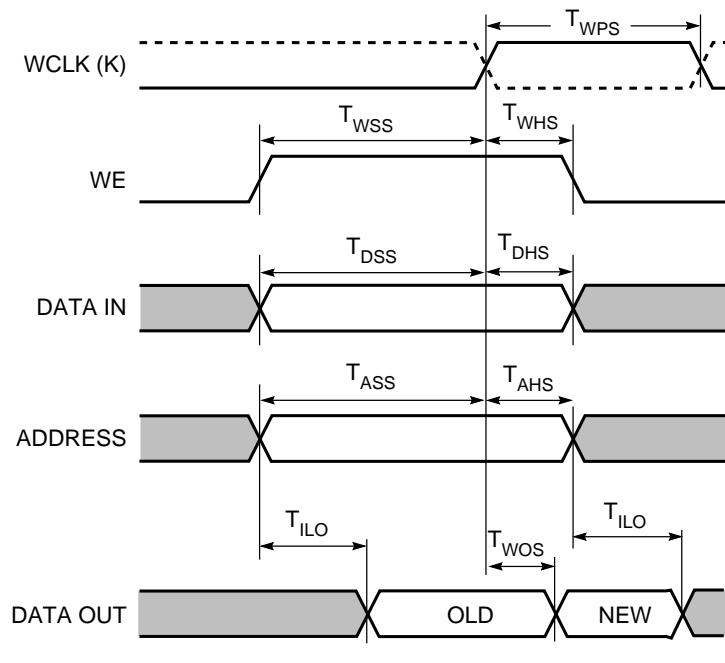
## XQR4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQR4000XL devices and are expressed in nanoseconds unless otherwise noted.

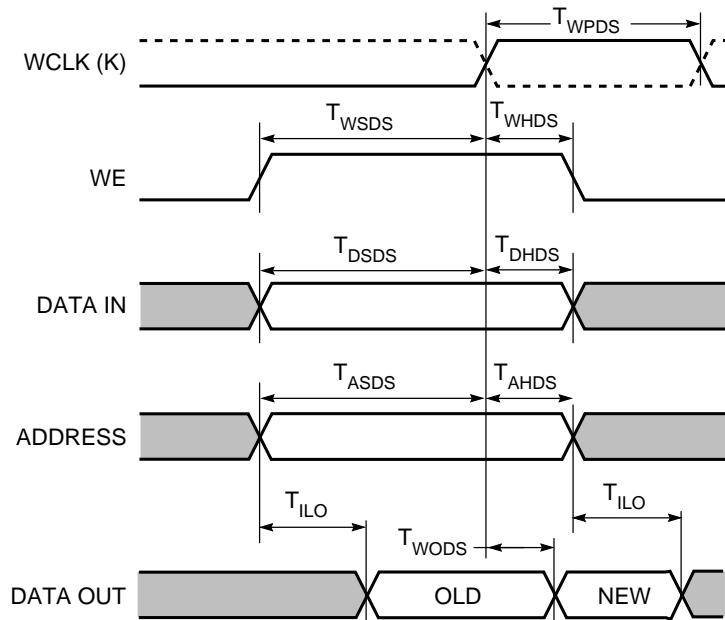
<b>Single Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCTS}$	9.0 9.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPPTS}$	4.5 4.5		ns ns
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.2 2.2		ns ns
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHTS}$	0 0		ns ns
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	2.0 2.5		ns ns
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHTS}$	0 0		ns ns
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.0 1.8		ns ns
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHTS}$	0 0		ns ns
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$		6.8 8.1	ns ns
<b>Read Operation</b>					
Address read cycle time	16x2 32x1	$T_{RC}$ $T_{RCT}$	4.5 6.5		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	$T_{ILO}$ $T_{IHO}$		1.6 2.7	ns ns
Address setup time before clock K	16x2 32x1	$T_{ICK}$ $T_{IHCK}$	1.3 2.3		ns ns

Dual Port RAM	Speed Grade		-3		Units
	Size	Symbol	Min	Max	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x1	T <sub>WCDS</sub>	9.0		ns
Clock K pulse width (active edge)	16x1	T <sub>WPDS</sub>	4.5		ns
Address setup time before clock K	16x1	T <sub>ASDS</sub>	2.5		ns
Address hold time after clock K	16x1	T <sub>AHDS</sub>	0		ns
DIN setup time before clock K	16x1	T <sub>DSDS</sub>	2.5		ns
DIN hold time after clock K	16x1	T <sub>DHDS</sub>	0		ns
WE setup time before clock K	16x1	T <sub>WSDS</sub>	1.8		ns
WE hold time after clock K	16x1	T <sub>WHDS</sub>	0		ns
Data valid after clock K	16x1	T <sub>WODS</sub>		7.8	ns

Note 1: Timing for 16 x 1 RAM option is identical to 16 x 2 RAM.

**XQR4000XL CLB RAM Synchronous (Edge-Triggered) Write Timing**

X6461

**XQR4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing**

X6474

## XQR4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XQR4000XL Output Flip-Flop, Clock to Out

Description	Symbol	Device	Speed Grade	-3	Units
				Max	
Global Low Skew Clock to Output using OFF	$T_{ICKOF}$	XQR4013XL XQR4036XL XQR4062XL	8.6 9.8 11.3	ns ns ns	
Global Early Clock to Output using OFF Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	$T_{ICKEOF}$	XQR4013XL XQR4036XL XQR4062XL	7.4 8.1 9.9	ns ns ns	
For output SLOW option add	$T_{SLOW}$	All Devices	3.0	ns	

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50%  $V_{CC}$  threshold with 50 pF external capacitive load. For different loads, see graph below.

### XQR4000XL Output Mux, Clock to Out

Description	Symbol	Device	Speed Grade	-3	Units
				Max	
Global Low Skew Clock to Output using OFF	$T_{ICKOF}$	XQR4013XL XQR4036XL XQR4062XL	8.8 10.0 11.4	ns ns ns	
Global Early Clock to Output using OFF. Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	$T_{ICKEOF}$	XQR4013XL XQR4036XL XQR4062XL	7.6 8.2 10.0	ns ns ns	
For output SLOW option add	$T_{SLOW}$	All Devices	3.0	ns	

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50%  $V_{CC}$  threshold with 50 pF external capacitive load. For different loads, see graph below.

## Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

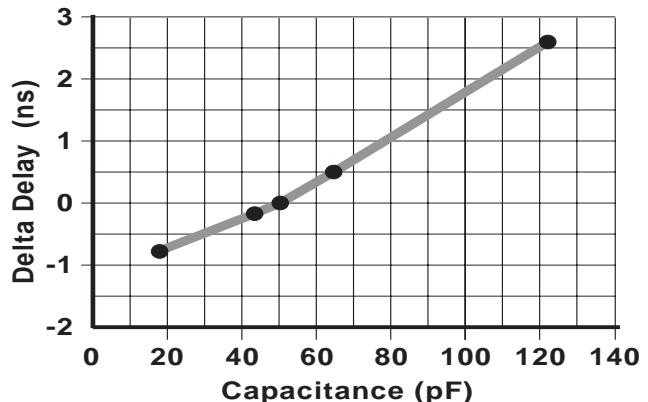


Figure 1: Delay Factor at Various Capacitive Loads

X8257

## XQR4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XQR4000XL Global Low Skew Clock, Set-Up and Hold

Description	Symbol	Device	Speed Grade	-3	Units
				Min	
Input Setup and Hold Times Using Global Low Skew Clock and IFF					
<b>No Delay</b>	$T_{PSN}/T_{PHN}$	XQR4013XL XQR4036XL XQR4062XL	1.2 / 3.2 1.2 / 5.5 1.2 / 7.0	ns ns ns	
<b>Partial Delay</b>	$T_{PSP}/T_{PHP}$	XQR4013XL XQR4036XL XQR4062XL	6.1 / 0.0 6.4 / 1.0 6.7 / 1.2	ns ns ns	
<b>Full Delay</b>	$T_{PSD}/T_{PHD}$	XQR4013XL XQR4036XL XQR4062XL	6.4 / 0.0 6.6 / 0.0 6.8 / 0.0	ns ns ns	

IFF = Input Flip-Flop or Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

Note 2: The XQ4013XL, XQ4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XQR4000XL BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Speed Grade			-3
Description	Symbol	Device	Min
Input Setup and Hold Times			
<b>No Delay</b>			
Global Early Clock and IFF	$T_{PSEN}/T_{PHEN}$	XQR4013XL	1.2 / 4.7
Global Early Clock and FCL	$T_{PFSEN}/T_{PFHEN}$	XQR4036XL	1.2 / 6.7
		XQR4062XL	1.2 / 8.4
<b>Partial Delay</b>			
Global Early Clock and IFF	$T_{PSEP}/T_{PHEP}$	XQR4013XL	5.4 / 0.0
Global Early Clock and FCL	$T_{PFSEP}/T_{PFHEP}$	XQR4036XL	6.4 / 0.8
		XQR4062XL	8.4 / 1.5
<b>Full Delay</b>			
Global Early Clock and IFF	$T_{PSED}/T_{PHED}$	XQR4013XL	12.0 / 0.0
		XQR4036XL	13.8 / 0.0
		XQR4062XL	13.1 / 0.0

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

## XQR4000XL BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-3
Description	Symbol	Device	Min
Input Setup and Hold Times			
<b>No Delay</b>			
Global Early Clock and IFF	$T_{PSEN}/T_{PHEN}$	XQR4013XL	1.2 / 4.7
Global Early Clock and FCL	$T_{PFSEN}/T_{PFHEN}$	XQR4036XL	1.2 / 6.7
		XQR4062XL	1.2 / 8.4
<b>Partial Delay</b>			
Global Early Clock and IFF	$T_{PSEP}/T_{PHEP}$	XQR4013XL	6.4 / 0.0
Global Early Clock and FCL	$T_{PFSEP}/T_{PFHEP}$	XQR4036XL	7.0 / 0.0
		XQR4062XL	9.0 / 0.8
<b>Full Delay</b>			
Global Early Clock and IFF	$T_{PSED}/T_{PHED}$	XQR4013XL	10.0 / 0.0
		XQR4036XL	12.2 / 0.0
		XQR4062XL	13.1 / 0.0

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

## XQR4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

<b>Description</b>	<b>Speed Grade</b>		<b>-3</b>	<b>Units</b>
	<b>Symbol</b>	<b>Device</b>	<b>Min</b>	
<b>Clocks</b>				
Clock Enable (EC) to Clock (IK)	$T_{ECIK}$	All devices	0.3	ns
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	$T_{OKIK}$	All devices	1.7	ns
<b>Setup Times</b>				
Pad to Clock (IK), no delay	$T_{PICK}$	All devices	1.7	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	$T_{PICKF}$	All devices	2.3	ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{POCK}$	All devices	0.7	ns
<b>Hold Times</b>				
All Hold Times		All devices	0	ns
<b>Global Set/Reset</b>				
Minimum GSR Pulse Width	$T_{MRW}$	All devices	19.8	ns
Delay from GSR input to any Q	$T_{RRI}$	XQR4013XL	15.9	ns
		XQR4036XL	22.5	ns
		XQR4062XL	29.1	ns
<b>Propagation Delays</b>				
Pad to I1, I2	$T_{PID}$	All devices	1.6	ns
Pad to I1, I2 via transparent input latch, no delay	$T_{PLI}$	All devices	2.6	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	$T_{PFLI}$	All devices	3.1	ns
Clock (IK) to I1, I2 (flip-flop)	$T_{IKRI}$	All devices	1.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKLI}$	All devices	1.9	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	$T_{OKLI}$	All devices	3.6	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

## XQR4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

Description	Symbol	-3		Units
		Min	Max	
<b>Clocks</b>				
Clock High	$T_{CH}$	3.0		ns
Clock Low	$T_{CL}$	3.0		ns
<b>Propagation Delays</b>				
Clock (OK) to Pad	$T_{OKPOF}$		5.0	ns
Output (O) to Pad	$T_{OPF}$		4.1	ns
3-state to Pad hi-Z (slew-rate independent)	$T_{TSHZ}$		4.4	ns
3-state to Pad active and valid	$T_{TSONF}$		4.1	ns
Output (O) to Pad via Fast Output MUX	$T_{OFPF}$		5.5	ns
Select (OK) to Pad via Fast MUX	$T_{OKPPF}$		5.1	ns
<b>Setup and Hold Times</b>				
Output (O) to clock (OK) setup time	$T_{OOK}$	0.5		ns
Output (O) to clock (OK) hold time	$T_{OKO}$	0.0		ns
Clock Enable (EC) to clock (OK) setup time	$T_{ECOK}$	0.0		ns
Clock Enable (EC) to clock (OK) hold time	$T_{OKEC}$	0.3		ns
<b>Global Set/Reset</b>				
Minimum GSR pulse width	$T_{MRW}$	19.8		ns
Delay from GSR input to any Pad	$T_{RPO}$			
XQR4013XL		20.5		ns
XQR4036XL		27.1		ns
XQR4062XL		33.7		ns
<b>Slew Rate Adjustment</b>				
For output SLOW option add	$T_{SLOW}$		3.0	ns

Note 1: Output timing is measured at ~50%  $V_{CC}$  threshold, with 50 pF external capacitive loads.

## Pinouts

### CB228 Package for XQR4013XL/4036XL/ 4062XL

PIN_NAME	CB228
VSS	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
VSS	P14
IO	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
VSS	P27
VCC	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
VCC	P37
IO	P38
IO	P39
IO	P40
IO	P41
VSS	P42
IO	P43

PIN_NAME	CB228
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
VSS	P56
M0	P57
VCC	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
VSS	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
VCC	P85
VSS	P86
IO	P87
IO	P88
IO	P89

<b>PIN_NAME</b>	<b>CB228</b>
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
VCC	P95
IO	P96
IO	P97
IO	P98
IO	P99
VSS	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
VSS	P113
DONE	P114
VCC	P115
/PROG	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
VSS	P129
IO	P130
IO	P131
IO	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136
IO	P137

<b>PIN_NAME</b>	<b>CB228</b>
IO	P138
IO	P139
D4_IO	P140
IO	P141
VCC	P142
VSS	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
VCC	P152
IO	P153
IO	P154
IO	P155
IO	P156
VSS	P157
IO	P158
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
VCC	P171
TDO	P172
VSS	P173
A0_WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184
IO	P185

PIN_NAME	CB228
VSS	P186
IO	P187
IO	P188
IO	P189
IO	P190
VCC	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198
A7_IO	P199
VSS	P200
VCC	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
VCC	P210
IO	P211
IO	P212
IO	P213
IO	P214
VSS	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
VCC	P228

## Ordering Information

**XQR 4062XL -3 CB 228 M**

QPRO™ Radiation Hardened

Device Type  
XQR4062XL  
XQR4036XL  
XQR4013XL

Speed Grade

Temperature Range  
M = Military Ceramic ( $T_C = -55^{\circ}\text{C}$  to  
 $+125^{\circ}\text{C}$ )

Number of Pins

Package Type  
CB = Top Brazed Ceramic Quad Flat Pack



# QPRO™ XQ4000XL Series QML

## High-Reliability Field Programmable Gate Arrays

May 19, 1998 (Version 1.0)

### XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
  - XQ4013XL 5962-98513
  - XQ4036XL 5962-98510
  - XQ4062XL 5962-98511
- For more information contact the Defense Supply Center Columbus (DSCC) <http://www.dscc.dla.mil/v/va/smd/smdsrch.html>
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 50 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA Sink Current Per XQ4000XL Output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XQ4000E
  - almost twice the routing capacity for high-density designs

- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- 0.35µ SRAM process

### Introduction

XQ4000X Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000X Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

**Table 1: XQ4000X Series High Reliability Field Programmable Gate Arrays**

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Packages
XQ4013XL	2432	13,000	18,432	10,000-30,000	24x24	576	1,536	192	PG223, CB228, PQ240, BG256
XQ4036XL	3078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	PG411, CB228, HQ240, BG352
XQ4062XL	5472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	PG475, CB228, HQ240, BG432

5/11/98

\* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

## XQ4000XL Switching Characteristics

### Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered final.

All specifications subject to change without notice.

### Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family a.c. supplements available on the Xilinx WEBLINK at <http://www.xilinx.com>.

### Absolute Maximum Ratings

Symbol	Description		Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to 4.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to 5.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to 5.5	V
$V_{CCT}$	Longest Supply Voltage Rise Time from 1 V to 3V	50	ms
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	Ceramic packages	+150
		Plastic packages	+125

Note 1: Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{CC}$	Supply voltage relative to GND, $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Plastic	3.0	3.6	V
	Supply voltage relative to GND, $T_C = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Ceramic	3.0	3.6	V
$V_{IH}$	High-level input voltage		50% of $V_{CC}$	5.5	V
$V_{IL}$	Low-level input voltage		0	30% of $V_{CC}$	V
$T_{IN}$	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per  $^{\circ}\text{C}$ .

Note 2: Input and output measurement threshold is ~50% of  $V_{CC}$ .

## XQ4000XL DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0 \text{ mA}$ , $V_{CC}$ min (LVTTL)		2.4		V
	High-level output voltage @ $I_{OH} = -500 \mu\text{A}$ , (LVCMS)		90% $V_{CC}$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0 \text{ mA}$ , $V_{CC}$ min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ $I_{OL} = 1500 \mu\text{A}$ , (LVCMS)			10% $V_{CC}$	V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)			5	mA
$I_L$	Input or output leakage current		-10	+10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample tested)	BGA, PQ, HQ, packages		10	pF
		PGA packages		16	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0 \text{ V}$ (sample tested)		0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 3.6 \text{ V}$ (sample tested)		0.02	0.15	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

## XQ4000XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

<b>Description</b>	<b>Symbol</b>	<b>Speed Grade</b>	<b>-3</b>	<b>Units</b>
		<b>Device</b>	<b>Max</b>	
From pad through Global Low Skew buffer, to any clock K	T <sub>GLS</sub>	XQ4013XL XQ4036XL XQ4062XL	3.6 4.8 6.3	ns ns ns
From pad through Global Early buffer, to any IOB clockK. Values are for BUFGE #s 1, 2, 5 and 6. Add 1 - 2 ns for BUFGE #s 3, 4, 7 and 8 and for all CLB clock Ks driven from any of the 8 BUFGEs, or consult TRCE.	T <sub>GE</sub>	XQ4013XL XQ4036XL XQ4062XL	2.4 3.1 4.9	ns ns ns

## XQ4000XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and expressed in nanoseconds unless otherwise noted.

Speed Grade		-3		Units
Description	Symbol	Min	Max	
<b>Combinatorial Delays</b>				
F/G inputs to X/Y outputs	$T_{ILO}$		1.6	ns
F/G inputs via H' to X/Y outputs	$T_{IHO}$		2.7	ns
F/G inputs via transparent latch to Q outputs	$T_{ITO}$		2.9	ns
C inputs via SR/H0 via H to X/Y outputs	$T_{HH0O}$		2.5	ns
C inputs via H1 via H to X/Y outputs	$T_{HH1O}$		2.4	ns
C inputs via DIN/H2 via H to X/Y outputs	$T_{HH2O}$		2.5	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	$T_{CBYP}$		1.5	ns
<b>CLB Fast Carry Logic</b>				
Operand inputs (F1, F2, G1, G4) to $C_{OUT}$	$T_{OPCY}$		2.7	ns
Add/Subtract input (F3) to $C_{OUT}$	$T_{ASCY}$		3.3	ns
Initialization inputs (F1, F3) to $C_{OUT}$	$T_{INCY}$		2.0	ns
$C_{IN}$ through function generators to X/Y outputs	$T_{SUM}$		2.8	ns
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$		0.26	ns
Carry Net Delay, $C_{OUT}$ to $C_{IN}$	$T_{NET}$		0.32	ns
<b>Sequential Delays</b>				
Clock K to Flip-Flop outputs Q	$T_{CKO}$		2.1	ns
Clock K to Latch outputs Q	$T_{CKLO}$		2.1	ns
<b>Setup Time before Clock K</b>				
F/G inputs	$T_{ICK}$	1.1		ns
F/G inputs via H	$T_{IHCK}$	2.2		ns
C inputs via H0 through H	$T_{HH0CK}$	2.0		ns
C inputs via H1 through H	$T_{HH1CK}$	1.9		ns
C inputs via H2 through H	$T_{HH2CK}$	2.0		ns
C inputs via DIN	$T_{DICK}$	0.9		ns
C inputs via EC	$T_{ECK}$	1.0		ns
C inputs via S/R, going Low (inactive)	$T_{RCK}$	0.6		ns
$C_{IN}$ input via F/G	$T_{CCK}$	2.3		ns
$C_{IN}$ input via F/G and H	$T_{CHCK}$	3.4		ns
<b>Hold Time after Clock K</b>				
F/G inputs	$T_{CKI}$	0		ns
F/G inputs via H	$T_{CKIH}$	0		ns
C inputs via SR/H0 through H	$T_{CKHH0}$	0		ns
C inputs via H1 through H	$T_{CKHH1}$	0		ns
C inputs via DIN/H2 through H	$T_{CKHH2}$	0		ns
C inputs via DIN/H2	$T_{CKDI}$	0		ns
C inputs via EC	$T_{CKEC}$	0		ns
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		ns
<b>Clock</b>				
Clock High time	$T_{CH}$	3.0		ns
Clock Low time	$T_{CL}$	3.0		ns
<b>Set/Reset Direct</b>				
Width (High)	$T_{RPW}$	3.0		ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		3.7	ns
<b>Global Set/Reset</b>				
Minimum GSR Pulse Width	$T_{MRW}$		19.8	ns
Delay from GSR input to any Q	$T_{MRQ}$	See page13 for $T_{RR}$ values per device.		
<b>Toggle Frequency (MHz)</b> (for export control)	$F_{TOG}$		166	MHz

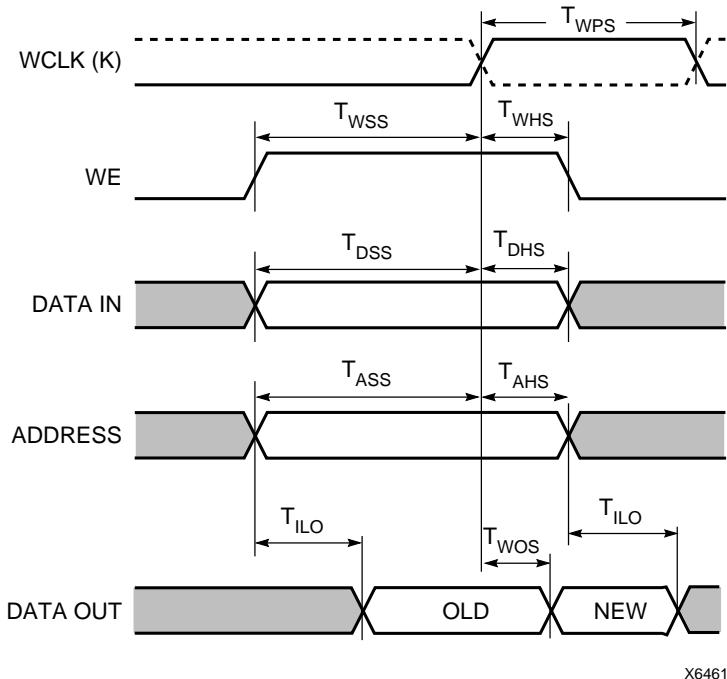
## XQ4000XL RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000XL devices and are expressed in nanoseconds unless otherwise noted.

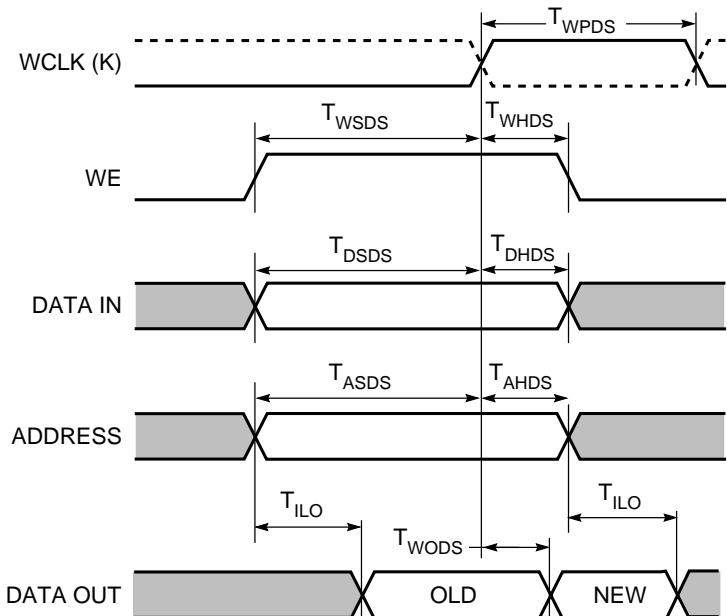
<b>Single Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x2 32x1	T <sub>WCS</sub> T <sub>WCSTS</sub>	9.0 9.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T <sub>WPS</sub> T <sub>WPPTS</sub>	4.5 4.5		ns ns
Address setup time before clock K	16x2 32x1	T <sub>ASS</sub> T <sub>ASTS</sub>	2.2 2.2		ns ns
Address hold time after clock K	16x2 32x1	T <sub>AHS</sub> T <sub>AHTS</sub>	0 0		ns ns
DIN setup time before clock K	16x2 32x1	T <sub>DSS</sub> T <sub>DSTS</sub>	2.0 2.5		ns ns
DIN hold time after clock K	16x2 32x1	T <sub>DHS</sub> T <sub>DHTS</sub>	0 0		ns ns
WE setup time before clock K	16x2 32x1	T <sub>WSS</sub> T <sub>WSTS</sub>	2.0 1.8		ns ns
WE hold time after clock K	16x2 32x1	T <sub>WHS</sub> T <sub>WHTS</sub>	0 0		ns ns
Data valid after clock K	16x2 32x1	T <sub>WOS</sub> T <sub>WOTS</sub>		6.8 8.1	ns ns
<b>Read Operation</b>					
Address read cycle time	16x2 32x1	T <sub>RC</sub> T <sub>RCT</sub>	4.5 6.5		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T <sub>ILO</sub> T <sub>IHO</sub>		1.6 2.7	ns ns
Address setup time before clock K	16x2 32x1	T <sub>ICK</sub> T <sub>IHKCK</sub>	1.3 2.3		ns ns

<b>Dual Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x1	T <sub>WCDS</sub>	9.0		ns
Clock K pulse width (active edge)	16x1	T <sub>WPDS</sub>	4.5		ns
Address setup time before clock K	16x1	T <sub>ASDS</sub>	2.5		ns
Address hold time after clock K	16x1	T <sub>AHDS</sub>	0		ns
DIN setup time before clock K	16x1	T <sub>DSDS</sub>	2.5		ns
DIN hold time after clock K	16x1	T <sub>DHDS</sub>	0		ns
WE setup time before clock K	16x1	T <sub>WSDS</sub>	1.8		ns
WE hold time after clock K	16x1	T <sub>WHDS</sub>	0		ns
Data valid after clock K	16x1	T <sub>WODS</sub>		7.8	ns

Note 1: Timing for 16 x1 RAM option is identical to 16 x 2 RAM.

**XQ4000XL CLB RAM Synchronous (Edge-Triggered) Write Timing**

X6461

**XQ4000XL CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing**

X6474

## XQ4000XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XQ4000XL Output Flip-Flop, Clock to Out

		Speed Grade	-3	Units
Description	Symbol	Device	Max	
Global Low Skew Clock to Output using OFF	T <sub>ICKOF</sub>	XQ4013XL XQ4036XL XQ4062XL	8.6 9.8 11.3	ns ns ns
Global Early Clock to Output using OFF Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	T <sub>ICKEOF</sub>	XQ4013XL XQ4036XL XQ4062XL	7.4 8.1 9.9	ns ns ns
For output SLOW option add	T <sub>SLOW</sub>	All Devices	3.0	ns

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load. For different loads, see graph below.

### XQ4000XL Output Mux, Clock to Out

		Speed Grade	-3	Units
Description	Symbol	Device	Max	
Global Low Skew Clock to Output using OFF	T <sub>ICKOF</sub>	XQ4013XL XQ4036XL XQ4062XL	8.8 10.0 11.4	ns ns ns
Global Early Clock to Output using OFF. Values are for BUFGE #s 3, 4, 7, and 8. Add 1.4 ns for BUFGE #s 1, 2, 5, and 6.	T <sub>ICKEOF</sub>	XQ4013XL XQ4036XL XQ4062XL	7.6 8.2 10.0	ns ns ns
For output SLOW option add	T <sub>SLOW</sub>	All Devices	3.0	ns

OFF = Output Flip Flop

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50% V<sub>CC</sub> threshold with 50 pF external capacitive load. For different loads, see graph below.

## Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

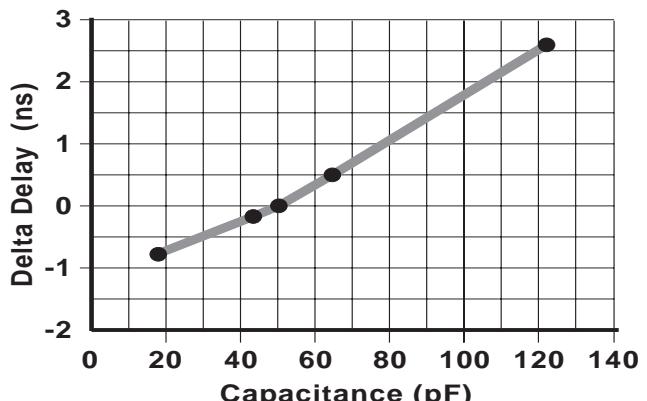


Figure 1: Delay Factor at Various Capacitive Loads

X8257

## XQ4000XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

### XQ4000XL Global Low Skew Clock, Set-Up and Hold

Description	Symbol	Device	Speed Grade	-3	Units
				Min	
Input Setup and Hold Times Using Global Low Skew Clock and IFF					
<b>No Delay</b>	$T_{PSN}/T_{PHN}$	XQ4013XL XQ4036XL XQ4062XL	1.2 / 3.2 1.2 / 5.5 1.2 / 7.0	ns ns ns	
<b>Partial Delay</b>	$T_{PSP}/T_{PHP}$	XQ4013XL XQ4036XL XQ4062XL	6.1 / 0.0 6.4 / 1.0 6.7 / 1.2	ns ns ns	
<b>Full Delay</b>	$T_{PSD}/T_{PHD}$	XQ4013XL XQ4036XL XQ4062XL	6.4 / 0.0 6.6 / 0.0 6.8 / 0.0	ns ns ns	

IFF = Input Flip-Flop or Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

Note 2: The XQ4013XL, XQ4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XQ4000XL BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

			<b>Speed Grade</b>	<b>-3</b>
<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Min</b>	
Input Setup and Hold Times				
<b>No Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEN}/T_{PHEN}$	XQ4013XL	1.2 / 4.7	
	$T_{PFSEN}/T_{PFHEN}$	XQ4036XL	1.2 / 6.7	
		XQ4062XL	1.2 / 8.4	
<b>Partial Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEP}/T_{PHEP}$	XQ4013XL	5.4 / 0.0	
	$T_{PFSEP}/T_{PFHEP}$	XQ4036XL	6.4 / 0.8	
		XQ4062XL	8.4 / 1.5	
<b>Full Delay</b> Global Early Clock and IFF	$T_{PSED}/T_{PHED}$	XQ4013XL	12.0 / 0.0	
		XQ4036XL	13.8 / 0.0	
		XQ4062XL	13.1 / 0.0	

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

Note 2: The XQ4013XL, XQ4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XQ4000XL BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

			<b>Speed Grade</b>	<b>-3</b>
<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Min</b>	
Input Setup and Hold Times				
<b>No Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEN}/T_{PHEN}$	XQ4013XL	1.2 / 4.7	
	$T_{PFSEN}/T_{PFHEN}$	XQ4036XL	1.2 / 6.7	
		XQ4062XL	1.2 / 8.4	
<b>Partial Delay</b> Global Early Clock and IFF Global Early Clock and FCL	$T_{PSEP}/T_{PHEP}$	XQ4013XL	6.4 / 0.0	
	$T_{PFSEP}/T_{PFHEP}$	XQ4036XL	7.0 / 0.0	
		XQ4062XL	9.0 / 0.8	
<b>Full Delay</b> Global Early Clock and IFF	$T_{PSED}/T_{PHED}$	XQ4013XL	10.0 / 0.0	
		XQ4036XL	12.2 / 0.0	
		XQ4062XL	13.1 / 0.0	

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

Note 2: The XQ4013XL, XQ4036XL, and 4062XL have significantly faster partial and full delay setup times than other devices.

## XQ4000XL IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

<b>Description</b>	<b>Speed Grade</b>		<b>-3</b>	<b>Units</b>
	<b>Symbol</b>	<b>Device</b>	<b>Min</b>	
<b>Clocks</b>				
Clock Enable (EC) to Clock (IK)	$T_{ECIK}$	All devices	0.3	ns
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	$T_{OKIK}$	All devices	1.7	ns
<b>Setup Times</b>				
Pad to Clock (IK), no delay	$T_{PICK}$	All devices	1.7	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	$T_{PICKF}$	All devices	2.3	ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{POCK}$	All devices	0.7	ns
<b>Hold Times</b>				
All Hold Times		All devices	0	ns
<b>Global Set/Reset</b>				
Minimum GSR Pulse Width	$T_{MRW}$	All devices	19.8	ns
Delay from GSR input to any Q	$T_{RRI}$	XQ4013XL	15.9	ns
		XQ4036XL	22.5	ns
		XQ4062XL	29.1	ns
<b>Propagation Delays</b>				
Pad to I1, I2	$T_{PID}$	All devices	1.6	ns
Pad to I1, I2 via transparent input latch, no delay	$T_{PLI}$	All devices	2.6	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	$T_{PFLI}$	All devices	3.1	ns
Clock (IK) to I1, I2 (flip-flop)	$T_{IKRI}$	All devices	1.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKLI}$	All devices	1.9	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	$T_{OKLI}$	All devices	3.6	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

## XQ4000XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

		<b>-3</b>		<b>Units</b>
<b>Description</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	
<b>Clocks</b>				
Clock High	$T_{CH}$	3.0		ns
Clock Low	$T_{CL}$	3.0		ns
<b>Propagation Delays</b>				
Clock (OK) to Pad	$T_{OKPOF}$		5.0	ns
Output (O) to Pad	$T_{OPF}$		4.1	ns
3-state to Pad hi-Z (slew-rate independent)	$T_{TSHZ}$		4.4	ns
3-state to Pad active and valid	$T_{TSONF}$		4.1	ns
Output (O) to Pad via Fast Output MUX	$T_{OFPF}$		5.5	ns
Select (OK) to Pad via Fast MUX	$T_{OKFPF}$		5.1	ns
<b>Setup and Hold Times</b>				
Output (O) to clock (OK) setup time	$T_{OOK}$	0.5		ns
Output (O) to clock (OK) hold time	$T_{OKO}$	0.0		ns
Clock Enable (EC) to clock (OK) setup time	$T_{ECOK}$	0.0		ns
Clock Enable (EC) to clock (OK) hold time	$T_{OKEC}$	0.3		ns
<b>Global Set/Reset</b>				
Minimum GSR pulse width	$T_{MRW}$	19.8		ns
Delay from GSR input to any Pad	$T_{RPO}$			
XQ4013XL		20.5		ns
XQ4036XL		27.1		ns
XQ4062XL		33.7		ns
<b>Slew Rate Adjustment</b>				
For output SLOW option add	$T_{SLOW}$		3.0	ns

Note 1: Output timing is measured at ~50%  $V_{CC}$  threshold, with 50 pF external capacitive loads.

## Pinouts

### CB228 Package for XQ4013XL/4036XL/ 4062XL

PIN_NAME	CB228
VTT	
VSS	P1
BUFGP_TL_A16_GCK1_IO	P2
A17_IO	P3
IO	P4
IO	P5
TDI_IO	P6
TCK_IO	P7
IO	P8
IO	P9
IO	P10
IO	P11
IO	P12
IO	P13
VSS	P14
IO_FCLK1	P15
IO	P16
TMS_IO	P17
IO	P18
IO	P19
IO	P20
IO	P21
IO	P22
IO	P23
IO	P24
IO	P25
IO	P26
VSS	P27
VCC	P28
IO	P29
IO	P30
IO	P31
IO	P32
IO	P33
IO	P34
IO	P35
IO	P36
VCC	P37
IO	P38
IO	P39
IO	P40
IO_FCLK2	P41
VSS	P42

PIN_NAME	CB228
IO	P43
IO	P44
IO	P45
IO	P46
IO	P47
IO	P48
IO	P49
IO	P50
IO	P51
IO	P52
IO	P53
BUFGS_BL_GCK2_IO	P54
M1	P55
VSS	P56
M0	P57
VCC	P58
M2	P59
BUFGP_BL_GCK3_IO	P60
HDC_IO	P61
IO	P62
IO	P63
IO	P64
LDC_IO	P65
IO	P66
IO	P67
IO	P68
IO	P69
IO	P70
IO	P71
VSS	P72
IO	P73
IO	P74
IO	P75
IO	P76
IO	P77
IO	P78
IO	P79
IO	P80
IO	P81
IO	P82
IO	P83
/ERR_INIT_IO	P84
VCC	P85
VSS	P86
IO	P87
IO	P88

PIN_NAME	CB228
IO	P89
IO	P90
IO	P91
IO	P92
IO	P93
IO	P94
VCC	P95
IO	P96
IO	P97
IO	P98
IO	P99
VSS	P100
IO	P101
IO	P102
IO	P103
IO	P104
IO	P105
IO	P106
IO	P107
IO	P108
IO	P109
IO	P110
IO	P111
BUFGS_BR_GCK4_IO	P112
VSS	P113
DONE	P114
VCC	P115
/PROG	P116
D7_IO	P117
BUFGP_BR_GCK5_IO	P118
IO	P119
IO	P120
IO	P121
IO	P122
D6_IO	P123
IO	P124
IO	P125
IO	P126
IO	P127
IO	P128
VSS	P129
IO	P130
IO	P131
IO_FCLK3	P132
IO	P133
D5_IO	P134
/CS0_IO	P135
IO	P136

PIN_NAME	CB228
IO	P137
IO	P138
IO	P139
D4_IO	P140
IO	P141
VCC	P142
VSS	P143
D3_IO	P144
/RS_IO	P145
IO	P146
IO	P147
IO	P148
IO	P149
D2_IO	P150
IO	P151
VCC	P152
IO	P153
IO_FCLK4	P154
IO	P155
IO	P156
VSS	P157
IO	P158
IO	P159
IO	P160
IO	P161
IO	P162
IO	P163
D1_IO	P164
BUSY_/RDY_RCLK_IO	P165
IO	P166
IO	P167
D0_DIN_IO	P168
BUFGS_TR_GCK6_DOUT_IO	P169
CCLK	P170
VCC	P171
TDO	P172
VSS	P173
A0_/WS_IO	P174
BUFGP_TR_GCK7_A1_IO	P175
IO	P176
IO	P177
CSI_A2_IO	P178
A3_IO	P179
IO	P180
IO	P181
IO	P182
IO	P183
IO	P184

PIN_NAME	CB228
IO	P185
VSS	P186
IO	P187
IO	P188
IO	P189
IO	P190
VCC	P191
A4_IO	P192
A5_IO	P193
IO	P194
IO	P195
A21_IO	P196
A20_IO	P197
A6_IO	P198
A7_IO	P199
VSS	P200
VCC	P201
A8_IO	P202
A9_IO	P203
A19_IO	P204
A18_IO	P205
IO	P206
IO	P207
A10_IO	P208
A11_IO	P209
VCC	P210
IO	P211
IO	P212
IO	P213
IO	P214
VSS	P215
IO	P216
IO	P217
IO	P218
IO	P219
A12_IO	P220
A13_IO	P221
IO	P222
IO	P223
IO	P224
IO	P225
A14_IO	P226
BUFGS_TL_GCK8_A15_IO	P227
VCC	P228

## Ordering Information

### XQ 4062XL-3 PG 475 M

MIL-PRF-38535  
(QML) Processed

Device Type  
XQ4062XL  
XQ4036XL  
XQ4013XL

Speed Grade

Temperature Range

M = Military Ceramic ( $T_C = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )

N = Military Plastic ( $T_J = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )

Number of Pins

#### Package Type

CB = Top Brazed Ceramic Quad Flat Pack

PG = Ceramic Pin Grid Array

PQ/HQ = Plastic Quad Flat Back

BG = Plastic Ball Grid Array



# QPRO™ XQ4000E/EX QML High-Reliability Field Programmable Gate Arrays

May 19, 1998 (Version 2.1)

Product Specification

## XQ4000E/EX High-Reliability Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XQ4000E/EX output

- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E -3 for plastic packages only
  - -4 for ceramic packages only
  - XQ4028EX -4 for all packages

## More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This datasheet contains pinout tables for XQ4010E only. Refer to Xilinx 1998 Databook for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)

Table 1: XQ4000E/EX Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1024	2560	96	256	PG299, CB228, HQ240, BG352

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

## XQ4000E/EX Switching Characteristics

### XQ4000E/EX Absolute Maximum Ratings

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to $V_{CC}$ +0.5	V
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to $V_{CC}$ +0.5	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
$T_J$	Junction temperature	Ceramic packages	+150
		Plastic packages	+125

- Note 1: Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to  $V_{CC}$  + 2.0 V, provided this over- or undershoot lasts less than 20 ns.
- Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

### XQ4000E/EX Recommended Operating Conditions

Symbol	Description	Min	Max	Units	
$V_{CC}$	Supply voltage relative to GND, $T_C = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Ceramic packages	4.5	5.5	V
$V_{CC}$	Supply voltage relative to GND, $T_J = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	Plastic packages	4.5	5.5	V
$V_{IH}$	High-level input voltage	TTL inputs	2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage	TTL inputs	0	0.8	V
$T_{IN}$	Input signal transition time		250	ns	

- Note 1: At case temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per  $^{\circ}\text{C}$ .
- Note 2: Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.
- Note 3: All specifications are subject to change without notice.

## XQ4000E/EX DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0\text{mA}$ , $V_{CC}$ min	TTL outputs	2.4		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0\text{mA}$ , $V_{CC}$ min (Note 1)	TTL outputs		0.4	V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)			50	mA
$I_L$	Input or output leakage current		-10	+10	$\mu\text{A}$
$C_{IN}$	Input capacitance (sample tested)			16	pF
$I_{RIN^*}$	Pad pull-up (when selected) @ $V_{IN} = 0\text{V}$ (sample tested)		-0.02	-0.25	mA
$I_{RLL^*}$	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the development system Tie option.

\* Characterized Only.

## XQ4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Description	Symbol	Device	Speed Grade	-3*	-4**	Units
			Max	Max		
From pad through Primary buffer, to any clock K	$T_{PG}$	XQ4005E		7.0		ns
		XQ4010E	6.3	11.0		ns
		XQ4013E	6.8	11.5		ns
		XQ4025E		12.5		ns
From pad through Secondary buffer, to any clock K	$T_{SG}$	XQ4005E		7.5		ns
		XQ4010E	6.8	11.5		ns
		XQ4013E	7.3	12.0		ns
		XQ4025E		13.0		ns

\* For plastic package options only.

\*\* For ceramic package options only.

## XQ4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>	<b>-3</b>	<b>-4</b>	<b>Units</b>
				<b>Max</b>	<b>Max</b>	
<b>TBUF driving a Horizontal Longline (LL):</b>						
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	$T_{IO1}$	XQ4005E XQ4010E XQ4013E XQ4025E	6.4 7.2	5.0 8.0 9.0 11.0	ns ns ns ns	
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	$T_{IO2}$	XQ4005E XQ4010E XQ4013E XQ4025E	6.9 7.7	6.0 10.5 11.0 12.0	ns ns ns ns	
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	$T_{ON}$	XQ4005E XQ4010E XQ4013E XQ4025E	7.3 7.5	7.0 8.5 8.7 11.0	ns ns ns ns	
T going High to TBUF going inactive, not driving LL	$T_{OFF}$	XQ4005E XQ4010E XQ4013E XQ4025E		1.8 3.0 3.5 4.0	ns ns ns ns	
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	$T_{PUS}$	XQ4005E XQ4010E XQ4013E XQ4025E	22 26	23.0 29.0 32.0 42.0	ns ns ns ns	
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	$T_{PUF}$	XQ4005E XQ4010E XQ4013E XQ4025E	11 13	10.0 13.5 15.0 18.0	ns ns ns ns	

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

## XQ4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>	<b>-3</b>	<b>-4</b>	<b>Units</b>
			<b>Max</b>	<b>Max</b>		
Full length, both pull-ups, inputs from IOB I-pins	$T_{WAF}$	XQ4005E		9.5		ns
		XQ4010E	9.0	15.0		ns
		XQ4013E	11.0	16.0		ns
		XQ4025E		18.0		ns
Full length, both pull-ups, inputs from internal logic	$T_{WAFL}$	XQ4005E		12.5		ns
		XQ4010E	11.0	18.0		ns
		XQ4013E	13.0	19.0		ns
		XQ4025E		21.0		ns
Half length, one pull-up, inputs from IOB I-pins	$T_{WAO}$	XQ4005E		10.5		ns
		XQ4010E	10.0	16.0		ns
		XQ4013E	12.0	17.0		ns
		XQ4025E		19.0		ns
Half length, one pull-up, inputs from internal logic	$T_{WAOL}$	XQ4005E		12.5		ns
		XQ4010E	12.0	18.0		ns
		XQ4013E	14.0	19.0		ns
		XQ4025E		21.0		ns

Note 1: These delays are specified from the decoder input to the decoder output.

Note 2: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

## XQ4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

Speed Grade		-3		-4		Units	
Description	Symbol	Min	Max	Min	Max		
<b>Combinatorial Delays</b>							
F/G inputs to X/Y outputs	$T_{ILO}$		3.1		3.9	ns	
F/G inputs via H to X/Y outputs	$T_{IHO}$		5.5		5.9	ns	
C inputs via H to X/Y outputs	$T_{HH1O}$		4.7		4.9	ns	
<b>CLB Fast Carry Logic</b>							
Operand inputs (F1, F2, G1, G4) to COUT	$T_{OPCY}$		2.6		4.4	ns	
Add/Subtract input (F3) to COUT	$T_{ASCY}$		4.4		6.8	ns	
Initialization inputs (F1, F3) to COUT	$T_{INCY}$		1.7		2.9	ns	
CIN through function generators to X/Y outputs	$T_{SUM}$		4.4		5.0	ns	
CIN to COUT, bypass function generators	$T_{BYP}$		0.7		1.0	ns	
<b>Sequential Delays</b>							
Clock K to outputs Q	$T_{CKO}$				5.0	ns	
<b>Setup Time before Clock K</b>							
F/G inputs	$T_{ICK}$	3.0		4.0		ns	
F/G inputs via H	$T_{IHCK}$	4.6		6.1		ns	
C inputs via H1 through H	$T_{HH1CK}$	4.1		5.0		ns	
C inputs via H2 through H	$T_{HH2CK}$	3.8		4.8		ns	
C inputs via DIN	$T_{DICK}$	2.4		3.0		ns	
C inputs via EC	$T_{ECK}$	3.0		4.0		ns	
C inputs via S/R, going Low (inactive)	$T_{RCK}$	4.0		4.2		ns	

## XQ4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the static timing analyzer and used in the simulator.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XQ4000E/EX devices unless otherwise noted.

<b>Description</b>	<b>Symbol</b>	<b>Device</b>	<b>Speed Grade</b>		<b>-3</b>		<b>-4</b>		<b>Units</b>
			<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
<b>Hold Time after Clock K</b>									
F/G inputs	$T_{CKI}$		0		0				ns
F/G inputs via H	$T_{CKIH}$		0		0				ns
C inputs via H1 through H	$T_{CKHH1}$		0		0				ns
C inputs via DIN	$T_{CKDI}$		0		0				ns
C inputs via EC	$T_{CKEC}$		0		0				ns
C inputs via SR, going Low (inactive)	$T_{CKR}$		0		0				ns
<b>Clock</b>									
Clock High time	$T_{CH}$		4.0		4.5				ns
Clock Low time	$T_{CL}$		4.0		4.5				ns
<b>Set/Reset Direct</b>									
Width (High)	$T_{RPW}$		4.0		5.5				ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		4.0		6.5				ns
<b>Master Set/Reset</b>									
Width (High or Low)	$T_{MRW}$	4005E 4010E 4013E 4025E	11.5 11.5		13.0 55.0 70.0 112.0				ns ns ns ns
Delay from Global Set/Reset net to Q	$T_{MRQ}$	4005E 4010E 4013E 4025E		18.7 18.7		23.0 60.0 77.0 134.0			ns ns ns ns

## XQ4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

<b>Single Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>-4</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>							
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCSTS}$	14.4 14.4		15.0 15.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPPTS}$	7.2 7.2		7.5 7.5	1 ms 1 ms	ns ns
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.4 2.4		2.8 2.8		ns ns
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHTS}$	0 0		0 0		ns ns
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	3.2 1.9		3.5 2.5		ns ns
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHHTS}$	0 0		0 0		ns ns
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.0 2.0		2.2 2.2		ns ns
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHHTS}$	0 0		0 0		ns ns
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$	8.8 10.3			10.3 11.6	ns ns

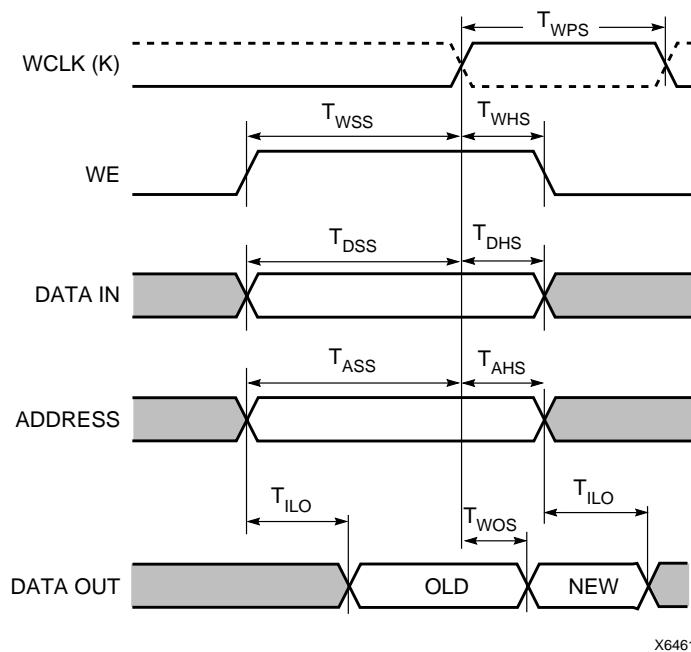
Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

<b>Dual-Port RAM</b>	<b>Speed Grade</b>		<b>-3</b>		<b>-4</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>							
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	14.4		15.0		ns
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	7.2		7.5	1 ms	ns
Address setup time before clock K	16x1	$T_{ASDS}$	2.5		2.8		ns
Address hold time after clock K	16x1	$T_{AHDS}$	0		0		ns
DIN setup time before clock K	16x1	$T_{DSDS}$	1.9		2.2		ns
DIN hold time after clock K	16x1	$T_{DHDS}$	0		0		ns
WE setup time before clock K	16x1	$T_{WSDS}$	2.0		2.2		ns
WE hold time after clock K	16x1	$T_{WHDS}$	0		0.3		ns
Data valid after clock K	16x1	$T_{WODS}$		7.8		10.0	ns

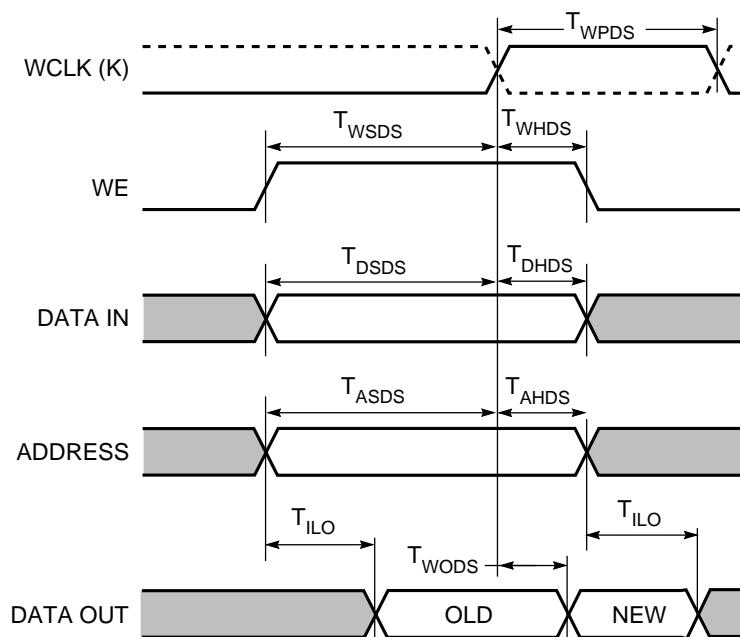
Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

## XQ4000E CLB RAM Synchronous (Edge-Triggered) Write Timing



X6461

## XQ4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



X6474

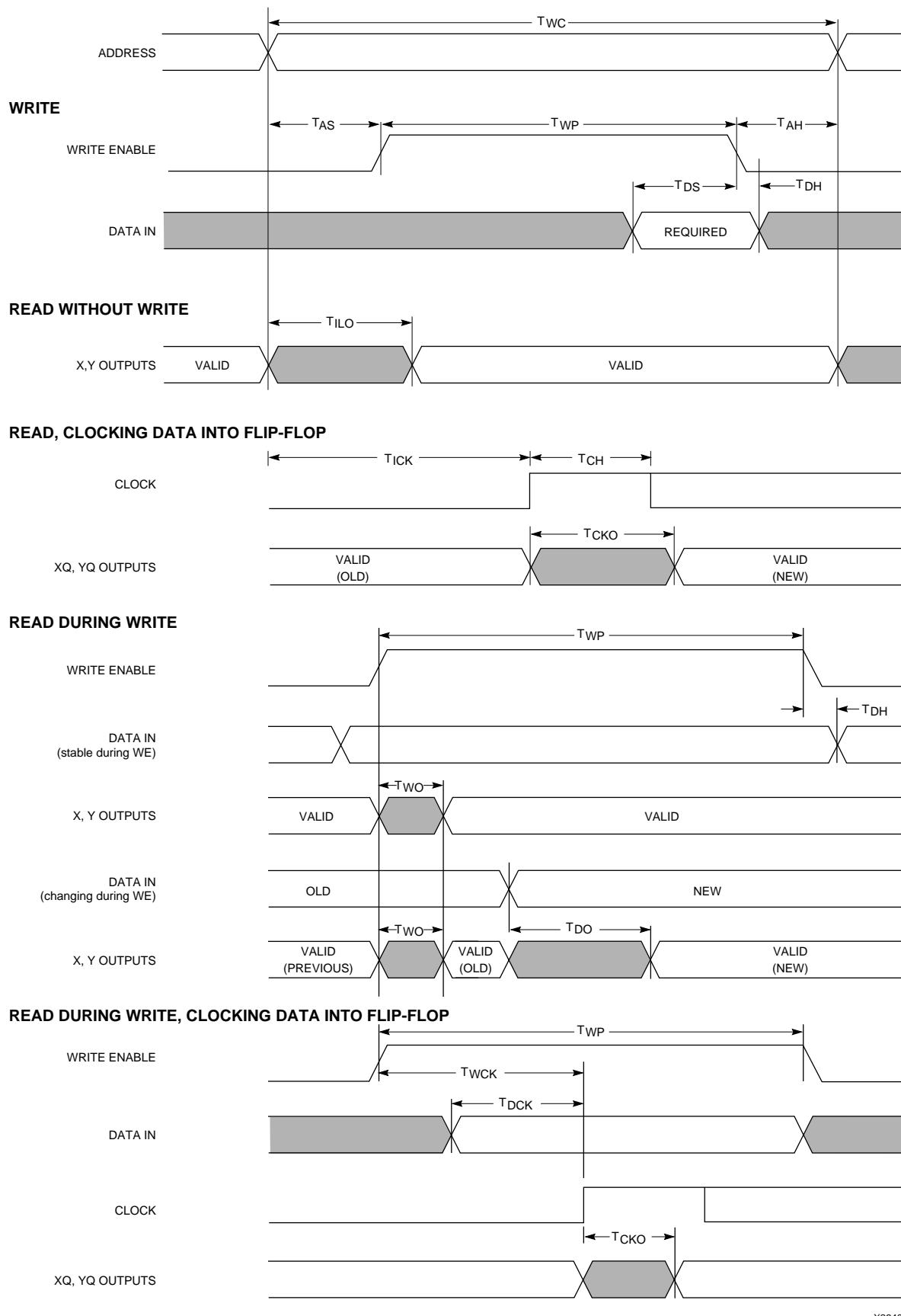
## XQ4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

Speed Grade			-3		-4		Units
Description	Size	Symbol	Min	Max		Max	
<b>Write Operation</b>							
Address write cycle time	16x2 32x1	$T_{WC}$ $T_{WCT}$	8.0 8.0		8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	$T_{WP}$ $T_{WPT}$	4.0 4.0		4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	$T_{AS}$ $T_{AST}$	2.0 2.0		2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	$T_{AH}$ $T_{AHT}$	2.0 2.0		2.5 2.0		ns ns
DIN setup time before end of WE	16x2 32x1	$T_{DS}$ $T_{DST}$	2.2 2.2		4.0 5.0		ns ns
DIN hold time after end of WE	16x2 32x1	$T_{DH}$ $T_{DHT}$	2.0 2.0		2.0 2.0		ns ns
<b>Read Operation</b>							
Address read cycle time	16x2 32x1	$T_{RC}$ $T_{RCT}$	3.1 5.5		4.5 6.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	$T_{ILO}$ $T_{IHO}$		3.1 5.5		3.9 5.9	ns ns
<b>Read Operation, Clocking Data into Flip-Flop</b>							
Address setup time before clock K	16x2 32x1	$T_{ICK}$ $T_{IHCK}$	3.0 4.6		4.0 6.1		ns ns
<b>Read During Write</b>							
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	$T_{WO}$ $T_{WOT}$		6.0 7.3		10.0 12.0	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	$T_{DO}$ $T_{DOT}$		6.6 7.6		9.0 11.0	ns ns
<b>Read During Write, Clocking Data into Flip-Flop</b>							
WE setup time before clock K	16x2 32x1	$T_{WCK}$ $T_{WCKT}$	6.0 6.8		8.0 9.6		ns ns
Data setup time before clock K	16x2 32x1	$T_{DCK}$ $T_{DCKT}$	5.2 6.2		7.0 8.0		ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

## XQ4000E CLB Level-Sensitive RAM Timing Characteristics



X2640

## XQ4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E/EX devices unless otherwise noted.

Description	Symbol	Device	Speed Grade	-3	-4	Units
Global Clock to Output (fast) using OFF	$T_{ICKOF}$ (Max)	XQ4005E XQ4010E XQ4013E XQ4025E		10.9 11.0	14.0 16.0 16.5 17.0	ns ns ns ns
Global Clock to Output (slew-limited) using OFF	$T_{ICKO}$ (Max)	XQ4005E XQ4010E XQ4013E XQ4025E		14.9 15.0	18.0 20.0 20.5 21.0	ns ns ns ns
Input Setup Time, using IFF (no delay)	$T_{PSUF}$ (Min)	XQ4005E XQ4010E XQ4013E XQ4025E		0.2 0	2.0 1.9 1.6 1.5	ns ns ns ns
Input Hold Time, using IFF (no delay)	$T_{PHF}$ (Min)	XQ4005E XQ4010E XQ4013E XQ4025E		5.5 6.5	4.6 6.0 7.0 8.0	ns ns ns ns
Input Setup Time, using IFF (with delay)	$T_{PSU}$ (Min)	XQ4005E XQ4010E XQ4013E XQ4025E		7.0 7.0	8.5 8.5 8.5 9.5	ns ns ns ns ns ns ns
Input Hold Time, using IFF (with delay)	$T_{PH}$ (Min)	XQ4005E XQ4010E XQ4013E XQ4025E		0 0	0 0 0 0	ns ns ns ns

OFF = Output Flip-Flop

IFF = Input Flip-Flop or Latch

## XQ4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade		-3		-4		Units
Description	Symbol	Device	Min	Max	Min	Max		
<b>Propagation Delays (TTL Inputs)</b>								
Pad to I1, I2 Pad to I1, I2 via transparent latch, no delay with delay	$T_{PID}$ $T_{PLI}$ $T_{PDLI}$	All devices All devices XQ4005E XQ4010E XQ4013E XQ4025E		2.5 10.8 11.2		3.0 6.0 12.0 12.2 12.6 15.0	ns ns ns ns ns ns	
<b>Propagation Delays</b>								
Clock (IK) to I1, I2 (flip-flop) Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKRI}$ $T_{IKLI}$	All devices All devices		2.8 4.0		6.8 7.3	ns ns	
<b>Hold Times (Note 1)</b>								
Pad to Clock (IK), no delay with delay	$T_{IKPI}$ $T_{IKPID}$	All devices All devices	0 0		0 0		ns ns	

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## XQ4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

		Speed Grade		-3		-4		Units
Description	Symbol	Device	Min	Max	Min	Max		
<b>Setup Times (TTL Inputs)</b>								
Pad to Clock (IK), no delay with delay	$T_{PICK}$ $T_{PICKD}$	All devices XQ4005E XQ4010E XQ4013E XQ4025E	2.6 9.8 10.2		4.0 10.9 11.3 11.8 14.0			ns ns ns ns ns ns ns ns ns
<b>(TTL or CMOS)</b>								
Clock Enable (EC) to Clock (IK), no delay with delay	$T_{ECIK}$ $T_{ECIKD}$	All devices XQ4005E XQ4010E XQ4013E XQ4025E	2.5 9.7 10.1		3.5 10.4 10.7 11.1 14.0			ns ns ns ns ns
<b>Global Set/Reset (Note 3)</b>								
Delay from GSR net through Q to I1, I2 GSR width GSR inactive to first active Clock (IK) edge	$T_{RRI}$ $T_{MRW}$ $T_{RPO}$	XQ4005E XQ4010E XQ4013E XQ4025E XQ4005E XQ4010E XQ4013E XQ4025E XQ4005E XQ4010E XQ4013E XQ4025E		7.8 7.8 13.0 11.5 55.0 11.5 70.0 112.0 11.8 11.8		12.0 21.0 23.0 29.0 ns ns ns ns ns ns ns ns 15.0 20.3 22.0 28.0		ns ns ns ns ns ns ns ns ns ns ns ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XQ4005E. For other devices see the static timing analyzer.

## XQ4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

Description	Symbol	Speed Grade		-3		-4		Units
		Min	Max	Min	Max	Min	Max	
<b>Propagation Delays (TTL Output Levels)</b>								
Clock (OK) to Pad, fast slew-rate limited	$T_{OKPOF}$		6.5		7.5		ns	
Output (O) to Pad, fast slew-rate limited	$T_{OKPOS}$		9.5		11.5		ns	
3-state to Pad hi-Z (slew-rate independent)	$T_{OPF}$		5.5		8.0		ns	
3-state to Pad active and valid, fast slew-rate limited	$T_{OPS}$		8.6		12.0		ns	
	$T_{TSHZ}$		4.2		10.0		ns	
	$T_{TSOFF}$		8.1		10.0		ns	
	$T_{TSONS}$		11.1		13.7		ns	

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XQ4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

## XQ4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000E/EX devices unless otherwise noted.

Description	Symbol	Device	Speed Grade		-3		-4		Units
			Min	Max	Min	Max	Min	Max	
<b>Setup and Hold</b>									
Output (O) to clock (OK) setup time	$T_{OOK}$		4.6		5.0				ns
Output (O) to clock (OK) hold time	$T_{OKO}$		0		0				ns
<b>Clock</b>									
Clock High	$T_{CH}$		4.0		4.5				ns
Clock Low	$T_{CL}$		4.0		4.5				ns

- Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XQ4000 Data" section of the Programmable Logic Data Book.
- Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
- Note 3: Timing is based on the XQ4005E. For other devices see the static timing analyzer.

# XQ4028EX Switching Characteristics

## Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

**All specifications subject to change without notice.**

## XQ4028EX Absolute Maximum Ratings

Symbol	Description	Value	Units	
$V_{CC}$	Supply voltage relative to GND	-0.5 to +7.0	V	
$V_{IN}$	Input voltage relative to GND (Note 1)	-0.5 to $V_{CC} + 0.5$	V	
$V_{TS}$	Voltage applied to 3-state output (Note 1)	-0.5 to $V_{CC} + 0.5$	V	
$V_{CCT}$	Longest Supply Voltage Rise Time from 1 V to 4 V	50	ms	
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C	
$T_{SOL}$	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C	
$T_J$	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to  $V_{CC} + 2.0$  V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## XQ4028EX Recommended Operating Conditions

Symbol	Description	Min	Max	Units	
$V_{CC}$	Supply voltage relative to GND, $T_C = -55$ °C to +125°C	Ceramic Packages	4.5	5.5	V
	Supply voltage relative to GND, $T_J = -55$ °C to +125°C	Plastic Packages	4.5	5.5	V
$V_{IH}$	High-level input voltage	TTL inputs	2.0	$V_{CC}$	V
		CMOS inputs	70%	100%	$V_{CC}$
$V_{IL}$	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	$V_{CC}$
$T_{IN}$	Input signal transition time		250	ns	

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

Note 2: Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V.

Note 3: All timing parameters are specified for Commercial temperature range only.

## XQ4028EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
$V_{OH}$	High-level output voltage @ $I_{OH} = -4.0$ mA, $V_{CC}$ min	TTL outputs	2.4		V
	High-level output voltage @ $I_{OH} = -1.0$ mA	CMOS outputs	$V_{CC}-0.5$		V
$V_{OL}$	Low-level output voltage @ $I_{OL} = 12.0$ mA, $V_{CC}$ min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
$V_{DR}$	Data Retention Supply Voltage (below which configuration data may be lost)		3.0		V
$I_{CC0}$	Quiescent FPGA supply current (Note 2)			25	mA
$I_L$	Input or output leakage current		-10	+10	$\mu$ A
$C_{IN}$	Input capacitance (sample tested)	Plastic packages		10	pF
		Ceramic packages		16	pF
$I_{RPU}$	Pad pull-up (when selected) @ $V_{in} = 0$ V (sample tested)		0.02	0.25	mA
$I_{RPD}$	Pad pull-down (when selected) @ $V_{in} = 5.5$ V (sample tested)		0.02	0.25	mA
$I_{RLL}$	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND.

## XQ4028EX Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Description	Speed Grade	-4	Units
From pad through Global Low Skew buffer, to any clock K	$T_{GLS}$	9.2	ns
From pad through Global Early buffer, to any clock K in same quadrant	$T_{GE}$	5.7	ns

## XQ4028EX Longline and Wide Decoder Timing Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted. Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

### XQ4028EX Horizontal Longline Switching Characteristic Guidelines

	Speed Grade	-4	Units
Description	Symbol	Max	
<b>TBUF driving a Horizontal Longline</b>			
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	$T_{IO1}$	13.7	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	$T_{ON}$	14.7	ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	$T_{PU2}$		ns ns
<b>TBUF driving Half a Horizontal Longline</b>			
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	$T_{HIO1}$	6.3	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	$T_{HON}$	7.2	ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	$T_{HPU4}$		ns

Note 1: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the static timing analyzer to determine the delay for each destination.

### XQ4028EX Wide Decoder Switching Characteristic Guidelines

	Speed Grade	-4	Units
Description	Symbol	Max	
Full length, two pull-ups, inputs from IOB I-pins	$T_{WAF2}$		ns ns
Full length, two pull-ups, inputs from internal logic	$T_{WAF2L}$		ns ns
Half length, two pull-ups, inputs from IOB I-pins	$T_{WAO2}$		ns ns
Half length, two pull-ups, inputs from internal logic	$T_{WAO2L}$		ns ns

Note 1: These delays are specified from the decoder input to the decoder output.

## XQ4028EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

	Speed Grade	-4		Units
Description	Symbol	Min	Max	
<b>Combinatorial Delays</b>				
F/G inputs to X/Y outputs	$T_{ILO}$		2.2	ns
F/G inputs via H' to X/Y outputs	$T_{IHO}$		3.8	ns
F/G inputs via transparent latch to Q outputs	$T_{ITO}$		3.2	ns
C inputs via SR/H0 via H' to X/Y outputs	$T_{HH0O}$		3.6	ns
C inputs via H1 via H' to X/Y outputs	$T_{HH1O}$		3.0	ns
C inputs via DIN/H2 via H' to X/Y outputs	$T_{HH2O}$		3.6	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	$T_{CBYP}$		2.0	ns
<b>CLB Fast Carry Logic</b>				
Operand inputs (F1, F2, G1, G4) to COUT	$T_{OPCY}$		2.5	ns
Add/Subtract input (F3) to COUT	$T_{ASCY}$		4.1	ns
Initialization inputs (F1, F3) to COUT	$T_{INCY}$		1.9	ns
CIN through function generators to X/Y outputs	$T_{SUM}$		3.0	ns
$C_{IN}$ to $C_{OUT}$ , bypass function generators	$T_{BYP}$		0.60	ns
Carry Net Delay, $C_{OUT}$ to $C_{IN}$	$T_{NET}$		0.18	ns
<b>Sequential Delays</b>				
Clock K to Flip-Flop outputs Q	$T_{CKO}$		2.2	ns
Clock K to Latch outputs Q	$T_{CKLO}$		2.2	ns
<b>Setup Time before Clock K</b>				
F/G inputs	$T_{ICK}$	1.3		ns
F/G inputs via H'	$T_{IHCK}$	3.0		ns
C inputs via H0 through H'	$T_{HH0CK}$	2.8		ns
C inputs via H1 through H'	$T_{HH1CK}$	2.2		ns
C inputs via H2 through H'	$T_{HH2CK}$	2.8		ns
C inputs via DIN	$T_{DICK}$	1.2		ns
C inputs via EC	$T_{ECCK}$	1.2		ns
C inputs via S/R, going Low (inactive)	$T_{RCK}$	0.8		ns
CIN input via F'/G'	$T_{CCK}$	2.2		ns
CIN input via F'/G' and H'	$T_{CHCK}$	3.9		ns
<b>Hold Time after Clock K</b>				
F/G inputs	$T_{CKI}$	0		ns
F/G inputs via H'	$T_{CKIH}$	0		ns
C inputs via SR/H0 through H'	$T_{CKHH0}$	0		ns
C inputs via H1 through H'	$T_{CKHH1}$	0		ns
C inputs via DIN/H2 through H'	$T_{CKHH2}$	0		ns
C inputs via DIN/H2	$T_{CKDI}$	0		ns
C inputs via EC	$T_{CKEC}$	0		ns
C inputs via SR, going Low (inactive)	$T_{CKR}$	0		ns
<b>Clock</b>				
Clock High time	$T_{CH}$	3.5		ns
Clock Low time	$T_{CL}$	3.5		ns
<b>Set/Reset Direct</b>				
Width (High)	$T_{RPW}$	3.5		ns
Delay from C inputs via S/R, going High to Q	$T_{RIO}$		4.5	ns

Description	Speed Grade		-4		Units
	Symbol	Min	Max		
<b>Global Set/Reset</b>					
Minimum GSR Pulse Width	$T_{MRW}$		13.0	ns	
Delay from GSR input to any Q (XQ4028EX)	$T_{MRQ}$		22.8	ns	
Delay from GSR input to any Q (XQ4036EX)	$T_{MRQ}$		24.0	ns	
<b>Toggle Frequency</b> ) (for export control purposes)	$F_{TOG}$		143	MHz	

## XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Single Port RAM	Speed Grade		-4		Units
	Size	Symbol	Min	Max	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x2 32x1	$T_{WCS}$ $T_{WCTS}$	11.0 11.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	$T_{WPS}$ $T_{WPPTS}$	5.5 5.5		ns ns
Address setup time before clock K	16x2 32x1	$T_{ASS}$ $T_{ASTS}$	2.7 2.6		ns ns
Address hold time after clock K	16x2 32x1	$T_{AHS}$ $T_{AHTS}$	0 0		ns ns
DIN setup time before clock K	16x2 32x1	$T_{DSS}$ $T_{DSTS}$	2.4 2.9		ns ns
DIN hold time after clock K	16x2 32x1	$T_{DHS}$ $T_{DHTS}$	0 0		ns ns
WE setup time before clock K	16x2 32x1	$T_{WSS}$ $T_{WSTS}$	2.3 2.1		ns ns
WE hold time after clock K	16x2 32x1	$T_{WHS}$ $T_{WHTS}$	0 0		ns ns
Data valid after clock K	16x2 32x1	$T_{WOS}$ $T_{WOTS}$		8.2 10.1	ns ns

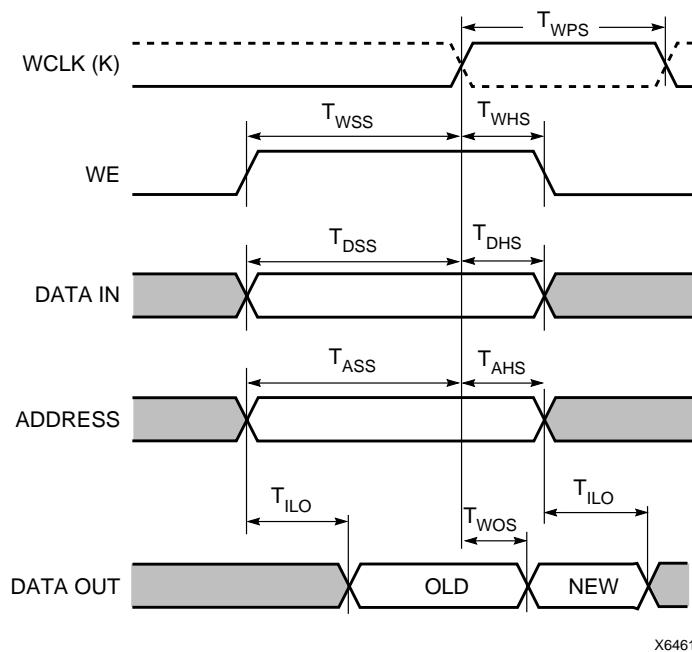
Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

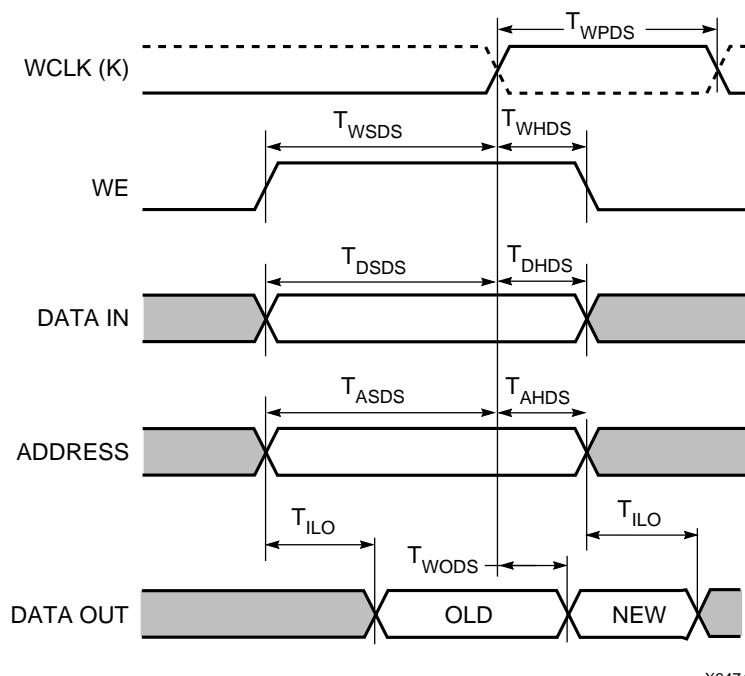
<b>Dual-Port RAM</b>	<b>Speed Grade</b>		<b>-4</b>		<b>Units</b>
	<b>Size</b>	<b>Symbol</b>	<b>Min</b>	<b>Max</b>	
<b>Write Operation</b>					
Address write cycle time (clock K period)	16x1	$T_{WCDS}$	11.0		ns
Clock K pulse width (active edge)	16x1	$T_{WPDS}$	5.5		ns
Address setup time before clock K	16x1	$T_{ASDS}$	3.1		ns
Address hold time after clock K	16x1	$T_{AHDS}$	0		ns
DIN setup time before clock K	16x1	$T_{DSDS}$	2.9		ns
DIN hold time after clock K	16x1	$T_{DHDS}$	0		ns
WE setup time before clock K	16x1	$T_{WSDS}$	2.1		ns
WE hold time after clock K	16x1	$T_{WHDS}$	0		ns
Data valid after clock K	16x1	$T_{WODS}$		9.4	ns

Note 1: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

## XQ4000EX CLB RAM Synchronous (Edge-Triggered) Write Timing



## XQ4000EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



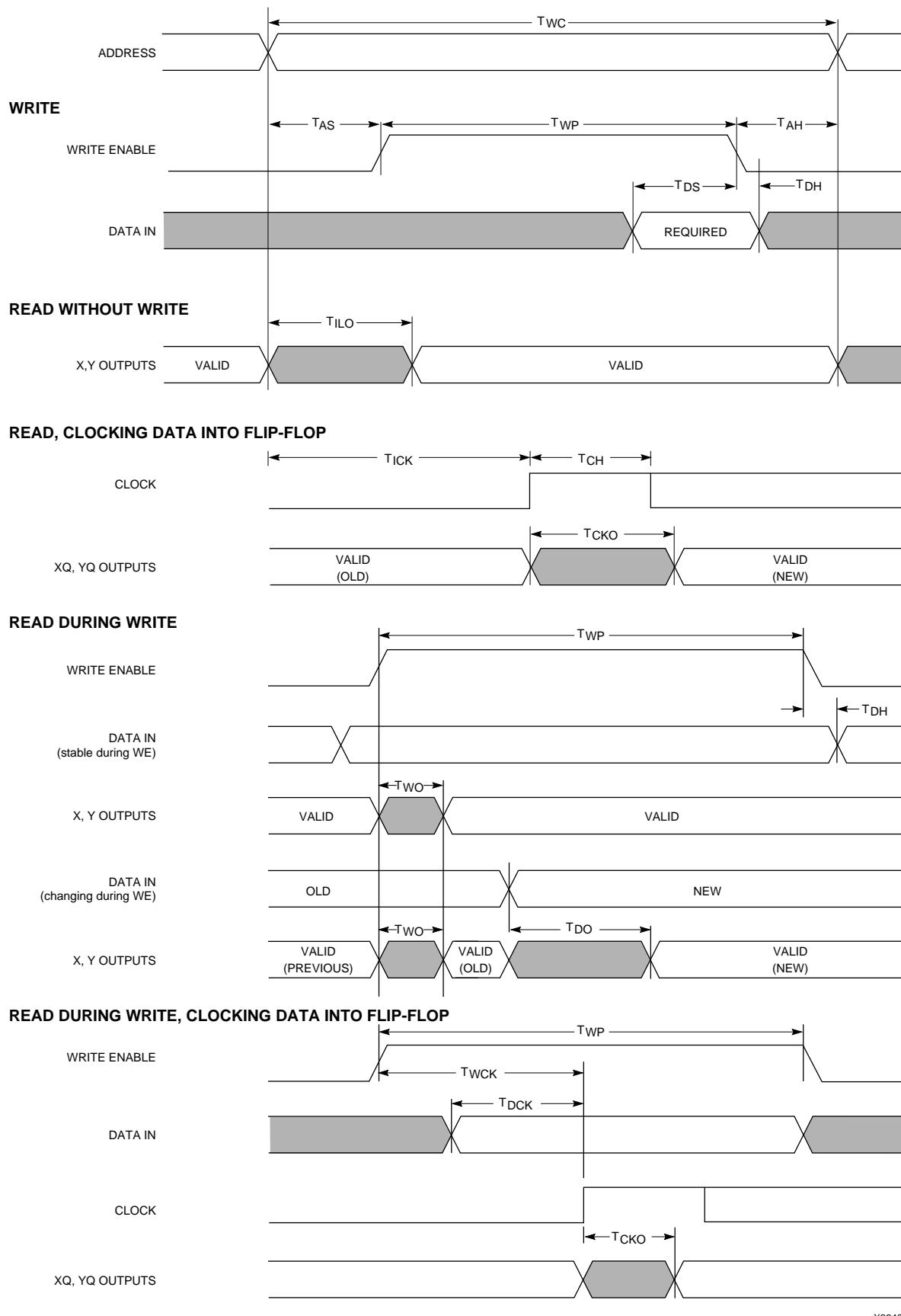
## XQ4028EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Speed Grade			-4		Units
Description	Size	Symbol	Min	Max	
<b>Write Operation</b>					
Address write cycle time	16x2 32x1	$T_{WC}$ $T_{WCT}$	10.6 10.6		ns ns
Write Enable pulse width (High)	16x2 32x1	$T_{WP}$ $T_{WPT}$	5.3 5.3		ns ns
Address setup time before WE	16x2 32x1	$T_{AS}$ $T_{AST}$	2.8 2.9		ns ns
Address hold time after end of WE	16x2 32x1	$T_{AH}$ $T_{AHT}$	1.7 1.7		ns ns
DIN setup time before end of WE	16x2 32x1	$T_{DS}$ $T_{DST}$	1.1 1.1		ns ns
DIN hold time after end of WE	16x2 32x1	$T_{DH}$ $T_{DHT}$	6.6 6.6		ns ns
<b>Read Operation</b>					
Address read cycle time	16x2 32x1	$T_{RC}$ $T_{RCT}$	4.5 6.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	$T_{ILO}$ $T_{IHO}$		2.2 3.8	ns ns
<b>Read Operation, Clocking Data into Flip-Flop</b>					
Address setup time before clock K	16x2 32x1	$T_{ICK}$ $T_{IHCK}$	1.5 3.2		ns ns
<b>Read During Write</b>					
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	$T_{WO}$ $T_{WOT}$		6.5 7.4	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	$T_{DO}$ $T_{DOT}$		7.7 8.2	ns ns
<b>Read During Write, Clocking Data into Flip-Flop</b>					
WE setup time before clock K	16x2 32x1	$T_{WCK}$ $T_{WCKT}$	7.1 9.2		ns ns
Data setup time before clock K	16x2 32x1	$T_{DCK}$ $T_{DCKT}$	5.9 8.4		ns ns

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

## XQ4028EXX CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



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## XQ4028EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted.

### XQ4028EX Output Flip-Flop, Clock to Out

Speed Grade		-4	Units
Description	Symbol	Max	
Global Low Skew Clock to TTL Output (fast) using OFF	$T_{ICKOF}$	16.6	ns
Global Early Clock to TTL Output (fast) using OFF	$T_{ICKEOF}$	13.1	ns

OFF = Output Flip Flop

### XQ4028EX Output MUX, Clock to Out

Speed Grade		-4	Units
Description	Symbol	Max	
Global Low Skew Clock to TTL Output (fast) using OMUX	$T_{PFPF}$	15.9	ns
Global Early Clock to TTL Output (fast) using OMUX	$T_{PEFPF}$	12.4	ns

OMUX = Output MUX

Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at TTL threshold with 50 pF external capacitive load.

Note 3: Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

### XQ4028EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

Speed Grade		-4	Units
Description	Symbol	Max	
For TTL output FAST add	$T_{TTLOF}$	0	ns
For TTL output SLOW add	$T_{TTLO}$	2.9	ns
For CMOS FAST output add	$T_{CMOSOF}$	1.0	ns
For CMOS SLOW output add	$T_{CMOSO}$	3.6	ns

## XQ4028EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted.

### XQ4028EX Global Low Skew Clock, Set-Up and Hold

Description	Speed Grade		-4 Min	Units
	Symbol			
Input Setup Time, using Global Low Skew clock and IFF (full delay)	$T_{PSD}$		8.0	ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	$T_{PHD}$		0	ns

IFF = Flip-Flop or Latch

### XQ4028EX Global Early Clock, Set-Up and Hold for IFF

Description	Speed Grade		-4 Min	Units
	Symbol			
Input Setup Time, using Global Early clock and IFF (partial delay)	$T_{PSEP}$		6.5	ns
Input Hold Time, using Global Early clock and IFF (partial delay)	$T_{PHEP}$		0	ns

IFF = Flip-Flop or Latch

Note 1: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

### XQ4028EX Global Early Clock, Set-Up and Hold for FCL

Description	Speed Grade		-4 Min	Units
	Symbol			
Input Setup Time, using Global Early clock and FCL (partial delay)	$T_{PFSEP}$		3.4	ns
Input Hold Time, using Global Early clock and FCL (partial delay)	$T_{PFHEP}$		0	ns

FCL = Fast Capture Latch

Note 1: For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 27.

Set-up time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time

Note 2: Under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Note 3: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

### XQ4028EX Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

Description	Speed Grade		-4 Max	Units
	Symbol			
For TTL input add	$T_{TTLI}$		0	ns
For CMOS input add	$T_{CMOSI}$		0.3	ns

## XQ4028EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

<b>Description</b>	<b>Speed Grade</b>	-4	<b>Units</b>
	<b>Symbol</b>	<b>Min</b>	
Clocks			
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	$T_{OKIK}$	3.2	ns
<b>Propagation Delays</b>		<b>Max</b>	
Pad to I1, I2	$T_{PID}$	2.2	ns
Pad to I1, I2 via transparent input latch, no delay	$T_{PLI}$	3.8	ns
Pad to I1, I2 via transparent input latch, partial delay	$T_{PPLI}$	13.3	ns
Pad to I1, I2 via transparent input latch, full delay	$T_{PDLI}$	18.2	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	$T_{PFLI}$	5.3	ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	$T_{PPFLI}$	13.6	ns
<b>Propagation Delays</b>			
Clock (IK) to I1, I2 (flip-flop)	$T_{IKRI}$	3.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	$T_{IKLI}$	3.2	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	$T_{OKLI}$	6.2	ns
<b>Global Set/Reset</b>			
Minimum GSR Pulse Width	$T_{MRW}$	13.0	ns
Delay from GSR input to any Q	$T_{RRI}$	22.8	ns

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

Note 1: For CMOS input levels, see the “XQ4028EX Input Threshold Adjustments” on page 27.

Note 2: For set-up and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 27.

## XQ4028EX IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Description	Speed Grade	-4	Units
	Symbol	Min	
<b>Setup Times</b>			
Pad to Clock (IK), no delay	$T_{PICK}$	2.5	ns
Pad to Clock (IK), partial delay	$T_{PICKP}$	10.8	ns
Pad to Clock (IK), full delay	$T_{PICKD}$	15.7	ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	$T_{PICKF}$	3.9	ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	$T_{PICKFP}$	12.3	ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{POCK}$	0.8	ns
Pad to Fast Capture Latch Enable (OK), partial delay	$T_{POCKP}$	9.1	ns
<b>Setup Times (TTL or CMOS Inputs)</b>			
Clock Enable (EC) to Clock (IK)	$T_{ECKI}$	0.3	ns
<b>Hold Times</b>			
Pad to Clock (IK), no delay	$T_{IKPI}$	0	ns
partial delay	$T_{IKPIP}$	0	ns
full delay	$T_{IKPID}$	0	ns
Pad to Clock (IK) via transparent Fast Capture Latch, no delay	$T_{IKFPI}$	0	ns
partial delay	$T_{IKFPIP}$	0	ns
full delay	$T_{IKFPID}$	0	ns
Clock Enable (EC) to Clock (IK), no delay	$T_{IKEC}$	0	ns
partial delay	$T_{IKECP}$	0	ns
full delay	$T_{IKECD}$	0	ns
Pad to Fast Capture Latch Enable (OK), no delay	$T_{OKPI}$	0	ns
partial delay	$T_{OKPIP}$	0	ns

Note 1: For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 27.

Note 2: For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 27.

## XQ4028EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000EX devices unless otherwise noted.

Speed Grade		-4			Units
Description	Symbol	Min	Max	Max	
<b>Propagation Delays</b>					
Clock (OK) to Pad	$T_{OKPOF}$		7.4	6.0	ns
Output (O) to Pad	$T_{OPF}$		6.2	5.0	ns
3-state to Pad hi-Z (slew-rate independent)	$T_{TSHZ}$		4.9	4.1	ns
3-state to Pad active and valid	$T_{TSONF}$		6.2	5.0	ns
Output MUX Select (OK) to Pad	$T_{OKFPF}$		6.7	5.4	ns
Fast Path Output MUX Input (EC) to Pad	$T_{CEFPF}$		6.2	5.0	ns
Slowest Path Output MUX Input (O) to Pad	$T_{OFPF}$		7.3	5.9	ns
<b>Setup and Hold Times</b>					
Output (O) to clock (OK) setup time	$T_{OOK}$	0.6			ns
Output (O) to clock (OK) hold time	$T_{OKO}$	0			ns
Clock Enable (EC) to clock (OK) setup	$T_{ECOK}$	0			ns
Clock Enable (EC) to clock (OK) hold	$T_{OKEC}$	0			ns
<b>Clock</b>					
Clock High	$T_{CH}$	3.5			ns
Clock Low	$T_{CL}$	3.5			ns
<b>Global Set/Reset</b>					
Minimum GSR pulse width	$T_{MRW}$	13.0			ns
Delay from GSR input to any Pad (XQ4028EX)	$T_{RPO}$	30.2			ns
Delay from GSR input to any Pad (XQ4036EX)	$T_{RPO}$	31.4			ns

Note 1: Output timing is measured at TTL threshold, with 35pF external capacitive loads.

Note 2: For CMOS output levels, see the "XQ4028EX Output Level and Slew Rate Adjustments" on page 26.

## CB191/196 Package for XQ4010E

Pin Description	PG191	CB196	Bound Scan
GND	D4	P1	-
PGCK1_(A16*I/O)	C3	P2	122
I/O_(A17)	C4	P3	125
I/O	B3	P4	128
-	-	P5*	-
I/O	C5	P6	131
I/O_(TDI)	A2	P7	134
I/O_(TCK)	B4	P8	137
I/O	C6	P9	140
I/O	A3	P10	143
I/O	B5	P11	146
I/O	B6	P12	149
GND	C7	P13	-
I/O	A4	P14	152
I/O	A5	P15	155
I/O_(TMS)	B7	P16	158
I/O	A6	P17	161
I/O	C8	P18	164
I/O	A7	P19	167
I/O	B8	P20	170
I/O	A8	P21	173
I/O	B9	P22	176
I/O	C9	P23	179
GND	D9	P24	-
VCC	D10	P25	-
I/O	C10	P26	182
I/O	B10	P27	185
I/O	A9	P28	-
I/O	A10	P29	191
I/O	A11	P30	194
I/O	C11	P31	197
I/O	B11	P32	200
I/O	A12	P33	203
I/O	B12	P34	206
I/O	A13	P35	209
GND	C12	P36	-
I/O	B13	P37	212
I/O	A14	P38	215
I/O	A15	P39	218
I/O	C13	P40	221

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	B14	P41	224
I/O	A16	P42	227
I/O	B15	P43	230
I/O	C14	P44	233
I/O	A17	P45	236
SCGK2_(I/O)	B16	P46	239
M1	C15	P47	242
GND	D15	P48	
M0	A18	P49	245**
VCC	D16	P50	-
M2	C16	P51	246**
PGCK2_(I/O)	B17	P52	247
I/O_(HDC)	E16	P53	250
-	-	P54*	-
I/O	C17	P55	253
I/O	D17	P56	256
I/O	B18	P57	259
I/O_(LDC)	E17	P58	262
I/O	F16	P59	265
I/O	C18	P60	268
I/O	D18	P61	271
I/O	F17	P62	274
GND	G16	P63	-
I/O	E18	P64	277
I/O	F18	P65	280
I/O	G17	P66	283
I/O	G18	P67	286
I/O	H16	P68	286
I/O	H17	P69	291
I/O	H18	P70	295
I/O	J18	P71	298
I/O	J17	P72	301
I/O_(/ERR_/_INIT)	J16	P73	304
VCC	J15	P74	-
GND	K15	P75	-
I/O	K16	P76	307
I/O	K17	P77	310
I/O	K18	P78	313
I/O	L18	P79	316
I/O	L17	P80	319
I/O	L16	P81	322

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

<b>Pin Description</b>	<b>PG191</b>	<b>CB196</b>	<b>Bound Scan</b>
I/O	M18	P82	325
I/O	M17	P83	328
I/O	N18	P84	331
I/O	P18	P85	334
GND	M16	P86	-
I/O	N17	P87	337
I/O	R18	P88	340
I/O	T18	P89	343
I/O	P17	P90	349
I/O	N16	P91	349
I/O	T17	P92	352
I/O	R17	P93	355
I/O	P16	P94	358
I/O	U18	P95	361
SGCK3_(I/O)	T16	P96	364
GND	R16	P97	-
DONE	U17	P98	-
VCC	R15	P99	-
/PROG	V18	P100	-
I/O_(D7)	T15	P101	367
PGCK3_(I/O)	U16	P102	370
-	-	P103*	-
I/O	T14	P104	376
I/O	U15	P105	376
I/O_(D6)	V17	P106	379
I/O	V16	P107	382
I/O	T13	P108	385
I/O	U14	P109	388
I/O	V15	P110	391
I/O	V14	P111	394
GND	T12	P112	-
I/O	U13	P113	397
I/O	V13	P114	400
I/O_(D5)	U12	P115	403
I/O_(CS0)	V12	P116	406
I/O	T11	P117	409
I/O	U11	P118	412
I/O	V11	P119	415
I/O	V1	P120	418
I/O_(D4)	U10	P121	421
I/O	T10	P122	424

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

<b>Pin Description</b>	<b>PG191</b>	<b>CB196</b>	<b>Bound Scan</b>
VCC	R10	P123	-
GND	R9	P124	-
I/O_(D3)	T9	P125	427
I/O_(RS)	U9	P126	430
I/O	V9	P127	433
I/O	V8	P128	436
I/O	U8	P129	439
I/O	T8	P130	442
I/O_(D2)	V7	P131	445
I/O	U7	P132	448
I/O	V6	P133	451
I/O	U6	P134	454
GND	T7	P135	-
I/O	V5	P136	457
I/O	V4	P137	460
I/O	U5	P138	463
I/O	T6	T139	446
I/O_(D1)	V3	P140	469
I/O_(RCLK-/BUSY/RDY)	V2	P141	472
I/O	U4	P142	475
I/O	T5	P143	478
I/O_(D0*_DIN)	U3	P144	481
SGCK4_(DOUT*_I/O)	T4	P145	484
CCLK	V1	P146	-
VCC	R4	P147	-
TDO	U2	P148	-
GND	R3	P149	-
I/O_(A0*_WS)	T3	P150	2
PGCK4_(I/O*_A1)	U1	P151	5
-	-	P152*	-
I/O	P3	P153	8
I/O	R2	P154	11
I/O_(CS1*_A2)	T2	P155	14
I/O_(A3)	N3	P156	17
I/O	P2	P157	20
I/O	T1	P158	23
I/O	R1	P159	26
I/O	N2	P160	29
GND	M3	P161	-
I/O	P1	P162	32
I/O	N1	P163	35

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O_(A4)	M2	P164	38
I/O_(A5)	M1	P165	41
I/O	L3	P166	44
I/O	L2	P167	47
I/O	L1	P168	50
I/O	K1	P169	53
I/O_(A6)	K2	P170	56
I/O_(A7)	K3	P171	59
GND	K4	P172	-
VCC	J4	P173	-
I/O_(A8)	J3	P174	62
I/O_(A9)	J2	P175	65
I/O	J1	P176	68
I/O	H1	P177	71
I/O	H2	P178	74
I/O	H3	P179	77
I/O_(A10)	G1	P180	80
I/O_(A11)	G2	P181	83
I/O	F1	P182	86
I/O	E1	P183	89

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
GND	G3	P184	-
I/O	F2	P185	92
I/O	D1	P186	96
I/O	C1	P187	98
I/O	E2	P188	101
I/O_(A12)	F3	P189	104
I/O_(A13)	D2	P190	107
-	-	P192*	-
I/O	E3	P193	113
I/O_(A14)	C2	P194	116
SGCK1(A15*I/O)	B2	P195	119
VCC	D3	P196	-

\* Indicates unconnected package pins.

\*\* Contributes only one bit (.I) to the boundary scan register.

Boundary Scan Blt 0 = TD0.T

Boundary Scan Bit 1 = TD0.0

Boundary Scan Bit 487 = BSCAN.UPD

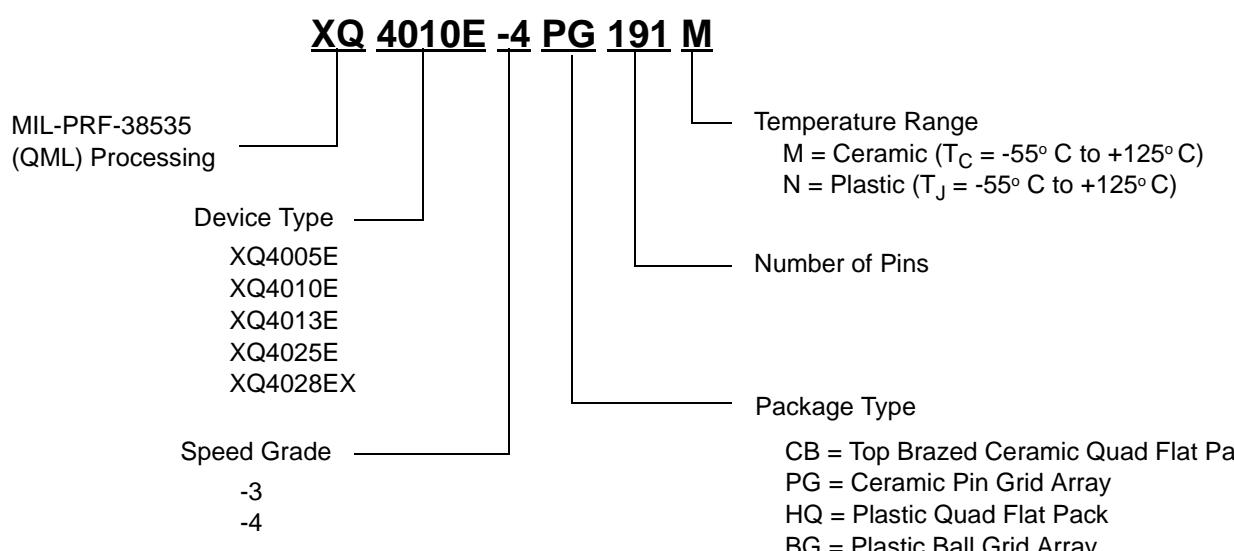
## Additional XQ4010E Package Pins

### CB196

N.C. Pins			
P5	P54	P103	P152
P192	-	-	-

Note: Information current as of 8/14/97.

## Example Ordering Information





- 1 Introduction**
- 2 Development System Products and CORE Solutions Products**
- 3 CPLD Products**
- 4 FPGA Products**
- 5 SPROM Products**
- 6 3V Products**
- 7 HardWire FpgASIC Products**
- 8 High-Reliability and QML Military Products**
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September 8, 1998 (Version 1.4)

Product Specification

## Device and Package Support

- XC1700 Serial PROMs
- XC9500 & XC9500XL CPLDs
- Supports all Xilinx package types

## Programmer Accessories

- Universal power supply
- Power cord options for US/Asia, UK, European and Japanese standards.
- Serial download cable and adapters
- Users manual
- Programmer interface software
- Vacuum handling tool

## Interface Software and System Requirements

The programmer software operates on a variety of different platforms. **Table 1** indicates the minimum system requirements for each. In all cases, a CD-ROM drive and an RS-232 serial port are required. A mouse is recommended.

## Programmer Functional Specifications

- Device programming, erasing and verification
- CPLD security control
- Serial PROM reset polarity control
- Checksum calculation and comparison
- Blank check and signature ID tests
- Master device upload
- File transfer and comparison
- Self check and auto calibration

## Programming Socket Adapters

- Supports all package styles: PLCC, PQFP, TQFP, VQFP, HQFP, BGA, SOIC, VOIC, PGA, CSP and DIP

## Electrical Requirements and Physical Specifications

- Operating voltage: 100-250 VAC, 50-60 Hz
- Power consumption: 1.0 Amp
- Dimensions: 6" x 7.75" x 2"
- Weight: 1 lb.
- Safety standards: approved by UL, CSA, TUV, CE

## New Programming Algorithm Support

The new programmer algorithms are available via the Xilinx WEB site:

- To access programmer software from the Xilinx WEB site, go to [www.xilinx.com](http://www.xilinx.com). The URL for the index of HW-130 software can be found at:  
[www.xilinx.com/techdocs/htm\\_index/sw\\_programmer.htm](http://www.xilinx.com/techdocs/htm_index/sw_programmer.htm)

**Table 1: Interface Software and System Requirements**

Requirements	Windows 95	Windows 98	Windows NT	Sun OS	Solaris	HP9000/700	IBM RS6000
Memory Needed	8MB	16MB	16MB	—	—	—	—
Hard Disk Space	2MB	2MB	2MB	6MB	6MB	6MB	6MB
System Software	4.00 or greater	4.10 or greater	3.1 or greater	SunOS 4.1.3 or greater	SunOS 5.3 or greater, (Solaris 2.3 or greater)	HP-UX A09.05 or greater	AIX 3.2.5 or greater

## Adapter Selection Table

Product Family	Package Types	Adapter P/N
XC9500/XL	PLCC 44	HW-133-PC44
XC9500	VQFP 44	HW-133-VQ44
XC9500/XL	CSP 48	HW-133-CS48
XC9500/XL	VQFP 64	HW-133-VQ64
XC9500	PLCC 84	HW-133-PC84
XC9500	PQFP 100	HW-133-PQ100
XC9500/XL	TQFP 100	HW-133-TQ100
XC9500XL	TQFP 144	HW-133-TQ144
XC9500 <sup>1</sup>	PQFP 160	HW-133-PQ160
XC9500/XL	HQFP 208	HW-133-HQ208
XC9500/XL	BGA 352	HW-133-BG352
XC1700 & XC17S00	DIP 8	HW-137-DIP8
XC1700 & XC17S00	PLCC 20/SO 8/VO 8	HW-137-PC20/SO8
XC1700 & XC17S00	SO 20	HW-137-SO20
XC1700	CLCC 44/VQFP 44	HW-137-LCC44/VQ44
Calibration Adapter		HW-130-CAL

1) Xilinx has manufactured two versions of the HW-133-PQ160 adapter. The current and correct adapter for programming XC9500 devices has "CPLD" written on the front label, at the top left side, under the Xilinx logo.

## Revision Control

Date	Revision
6/13/98	Added Windows 98 system requirements, added HW-137-LCC44/VQ44 to Adapter selection table.
9/8/98	Removed DOS and Windows 3.1 support. Removed the obsolete XC7200/7300 product families. Added package adapters for the XC9500/XL series in CSP 48, VQFP 64, and TQFP 144 packages.



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## Packages and Thermal Characteristics

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November 20, 1997 (Version 2.0)

## Package Information

### Inches vs. Millimeters

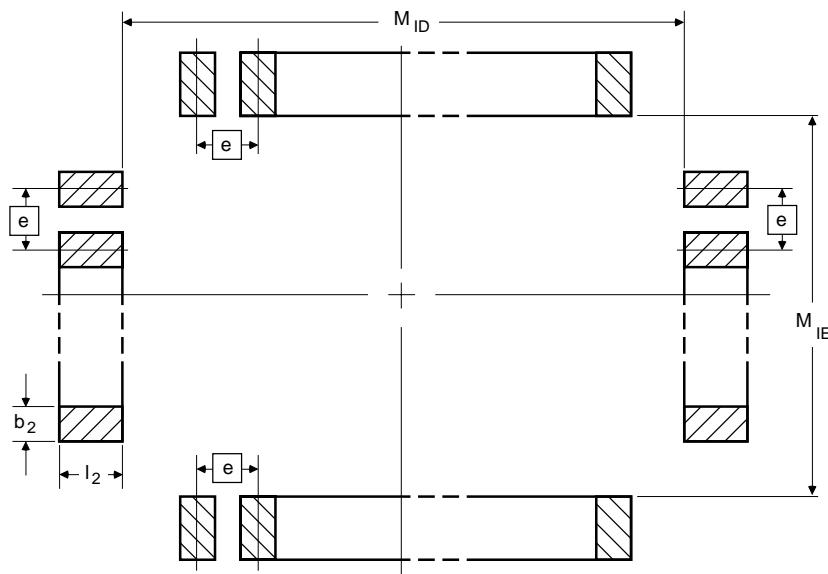
The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These

packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See [Table 1](#) for package dimensions.)

### EIA Standard Board Layout of Soldered Pads for QFP Devices



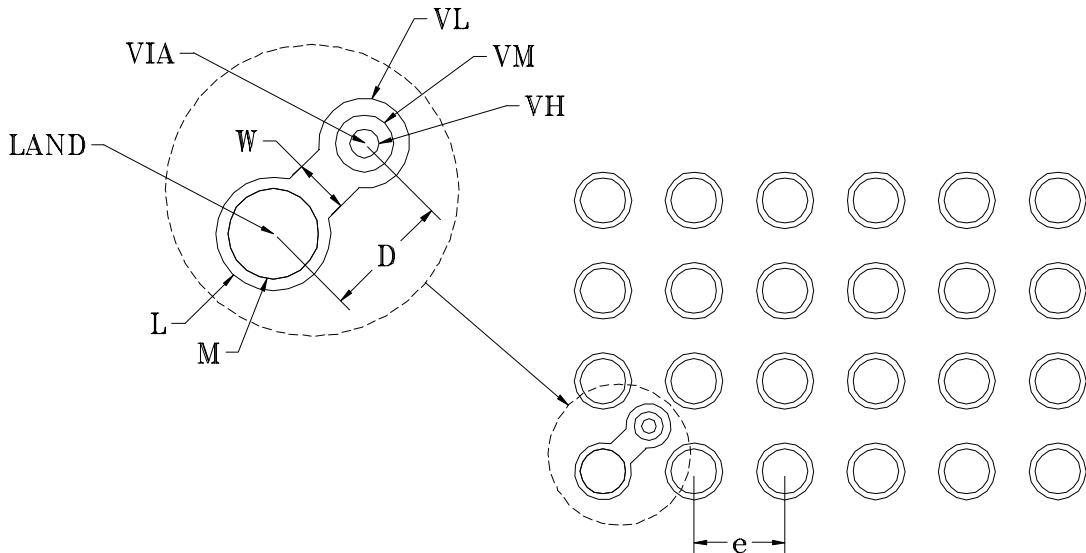
**Table 1: Dimensions for Xilinx Quad Flat Packs<sup>1</sup>**

Dim.	VQ44	VQ64	PQ100	HQ160 PQ160	HQ208 PQ208	VQ100 TQ100	TQ144	TQ176	HQ240 PQ240	HQ304
$M_{ID}$	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
$M_{IE}$	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
$e$	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
$b_2$	0.4 - 0.6	0.3 - 0.4	0.3 - 0.5	0.3 - 0.5	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4
$l_2$	1.60	1.60	1.80 <sup>2</sup>	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes: 1. Dimensions in millimeters  
 2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

## Suggested Board Layout of Soldered Pads for BGA

TYPICAL DOG BONE  
VIA ARRANGEMENT



	BG225	BG256	BG352	BG432	BG560
Solder Land (L) diameter	0.89	0.79	0.79	0.79	0.79
Opening in Solder Mask (M) diameter	0.65	0.58	0.58	0.58	0.58
Solder (Ball) Land Pitch (e)	1.5	1.27	1.27	1.27	1.27
Land Width between Via and Land (D)	0.3	0.3	0.3	0.3	0.3
Distance between Via and Land (D)	1.06	0.9	0.9	0.9	0.9
Via Land (VL) diameter	0.65	0.65	0.65	0.65	0.65
Solder Mask Opening on Via (VM) diameter	0.4	0.4	0.4	0.4	0.4
Through Hole (VH), plated diameter	0.3	0.3	0.3	0.3	0.3
Pad Array	Full	Periphery	Periphery	Periphery	Periphery
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33
Periphery rows	-	4	4	4	5

Notes:

1. Dimensions in millimeters.
2. 6 x 4 matrix for illustration only, one land pad shown with via connection.
3. Reference J-STD-013, use 'dog-bone' design via connection to land pad.

## Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

## Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100- and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

## Thermal Management

Modern high speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages

are chosen to handle 'typical' designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

## Package Thermal Characterization Methods & Conditions

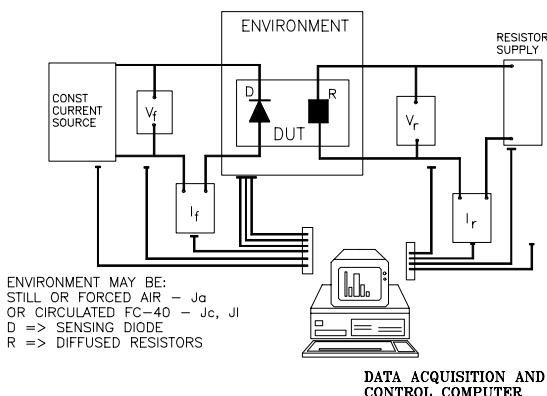
### Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power ( $P_d$ ) is applied. Power ( $P_d$ ) is applied to the device through diffused resistors on the same thermal die. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the set-up is within 6%.

### Definition of Terms

- $T_J$  Junction Temperature — the maximum temperature on the die, expressed in °C (degree Celsius)
- $T_A$  Ambient Temperature — expressed in °C.
- $T_C$  The temperature of the package body taken at a defined location on the body. This is taken at the primary heat flow path on the package and represents the hottest part on the package — expressed in °C.
- $T_i$  The isothermal fluid temperature when junction to case temperature is taken — expressed in °C.
- $P_d$  The total device power dissipation — expressed in watts.

## Junction-to-Reference General Setup



**Figure 1: Thermal Measurement Set-Up (Schematic for Junction to Reference)**

## Junction-to-Case Measurement — $\Theta_{JC}$

$\Theta_{JC}$  is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded.  $Pd$  is then applied. Case temperature ( $T_C$ ) is measured at the primary heat-flow path of the particular package. Junction temperature ( $T_J$ ) is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/Pd$$

The junction-to-isothermal-fluid measurement ( $\Theta_{JI}$ ) is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_l)/Pd$$

The latter data is considered as the ideal  $\Theta_{JA}$  data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heatsinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the  $\Theta_{JI}$  data is not published. The thermal lab keeps such data for package comparisons.

## Junction-to-Ambient Measurement — $\Theta_{JA}$

$\Theta_{JA}$  is measured on FR4 based PC boards measuring 4.5" x 6.0" x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with 2 signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has 2 internal copper planes (one power, one ground) and 2 signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as  $\Theta_{JC}$  measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/Pd$$

The setup described herein lends itself to the application of various airflow velocities from 0 - 800 Linear Feet per Minute (LFM), i.e., 0 - 4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

## Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration,  $\Theta_{JA}$ ,  $\Theta_{JC}$ , fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. [Table 2](#) shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

**Table 2: Summary of Thermal Resistance for Packages**

PKG-CODE	$\Theta_{JA}$ still air (Max)	$\Theta_{JA}$ still air (Typ)	$\Theta_{JA}$ still air (Min)	$\Theta_{JA}$ 250 LFM (Typ)	$\Theta_{JA}$ 500 LFM (Typ)	$\Theta_{JA}$ 750 LFM (Typ)	$\Theta_{JC}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BG225	37	30	24	19	17	16	3.3	Various
BG256	32	29	24	19	17	16	3.2	4L/2P-SMT
BG352	14	12	10	8	7	6	0.8	4L/2P-SMT
BG432	13	11	9	8	6	6	0.8	4L/2P-SMT
BG560	10	9	8	7	6	5	0.8	Estimated
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
DD8	114	109	97	90	73	60	8.2	Socketed
HQ160	14	14	14	10	8	7	1.0	4L/2P-SMT
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
HT144	-	10.9	-	7.3	5.7	5.0	0.9	4L/2P-SMT
HT176	-	16.0	-	-	-	-	2.0	Estimated
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT
PD8	82	79	73	60	54	50	22.2	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Socketed
PG475	14	13	12	9	8	7	1.2	Socketed
PG559	-	12.00	-	-	-	-	-	Estimated
PP132	35	34	33	23	18	17	6.0	Socketed
PP175	29	29	28	19	15	13	2.5	Socketed
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated

**Table 2: Summary of Thermal Resistance for Packages (Continued)**

PKG-CODE	$\Theta_{JA}$ still air (Max)	$\Theta_{JA}$ still air (Typ)	$\Theta_{JA}$ still air (Min)	$\Theta_{JA}$ 250 LFM (Typ)	$\Theta_{JA}$ 500 LFM (Typ)	$\Theta_{JA}$ 750 LFM (Typ)	$\Theta_{JC}$ (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT

Notes: 1. Maximum, typical and minimum numbers are based on numbers for all the devices in the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.  
 2. Package configurations and drawings are in the package section of the data book.  
 3. 2L/OP - SMT: the data is from a surface mount type I board -- no internal planes on the board.  
 4. 4L/2P - SMT: the data is from a 4 layer SMT board incorporating 2 internal planes. Socketed data is taken in socket.  
 5. Air flow is given Linear Feet per Minute (LFM). 500 LFM = 2.5 Meters per Second

## Application of Thermal Resistance Data

Thermal resistance data gauges the IC package thermal performance.  $\Theta_{JC}$  measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior.  $\Theta_{JC}$  strongly depends on the package's heat conductivity, architecture and geometrical considerations.

$\Theta_{JA}$  measures the total package thermal resistance including  $\Theta_{JC}$ .  $\Theta_{JA}$  depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a  $\Theta_{JA}$  value 20% higher than the same package mounted on a 4 layer board with power and ground planes.

By specifying a few constraints, devices are ensured to operate within the intended temperature range. This also ensures device reliability and functionality. The system ambient temperature needs to be specified. A maximum  $T_J$  also needs to be established for the system. The following inequality will hold.

$$T_J(\max) > \Theta_{JA} * P_d + T_A$$

The following two examples illustrates the use of this inequality.

**Table 3: Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

Dev Name	Package	$\Theta_{JA}$ still air	$\Theta_{JA}$ (250 LFM)	$\Theta_{JA}$ (500 LFM)	$\Theta_{JA}$ (750 LFM)	$\Theta_{JC}$	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/OP
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4 Layer Board data

Notes: Possible Solutions to meet the module requirements of 100°C :

- 1a.Using the standard PQ240;  $T_J = 55 + (23.7 \times 2.50) ==> 114.25 ^\circ C$ .
- 1b.Using standard PQ240 with 250LFM forced air  $T_J = 55 + (17.5 \times 2.50) ==> 98.75 ^\circ C$
- 2a.Using standard HQ240  $T_J = 55 + (12.5 \times 2.50) ==> 86.25 ^\circ C$
- 2b.Using HQ240 with 250 LFM forced air  $T_J = 55 + (8.6 \times 2.50) ==> 76.5 ^\circ C$

### Example 1:

The manufacturer's goal is  $T_J$  (max) < 100°C

A module is designed for a  $T_A = 45^\circ C$  max.

A XC3042 in a PLCC 84 has a  $\Theta_{JA} = 32^\circ C/watt$ .

Given a XC3042 with a logic design with a rated power  $P_d$  of 0.75watt.

With this information, the maximum die temperature can be calculated as:

$$T_J = 45 + (32 \times .75) ==> 69^\circ C.$$

The system manufacturer's goal of  $T_J < 100^\circ C$  is met.

### Example 2:

A module has a  $T_A = 55^\circ C$  max.

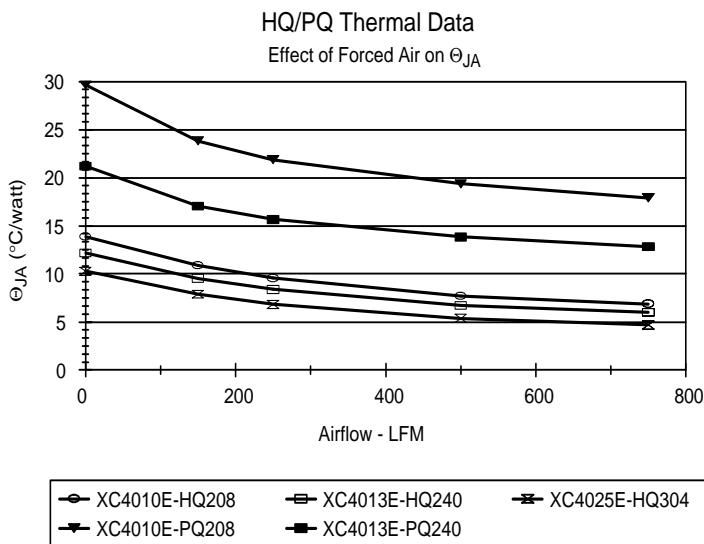
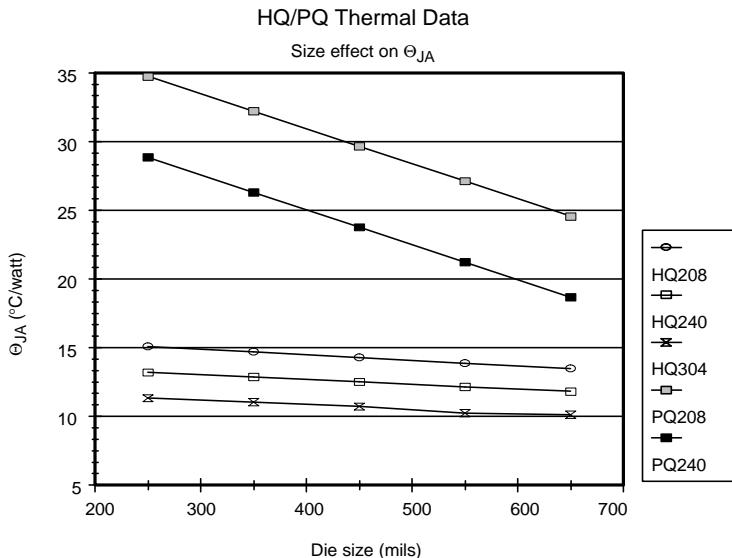
The Xilinx XC4013E is in a PQ240 package (HQ240 is also considered).

A XC4013E, in an example logic design, has a rated power of 2.50 watts. The module manufacturers goal is  $T_J(\max.) < 100^\circ C$ .

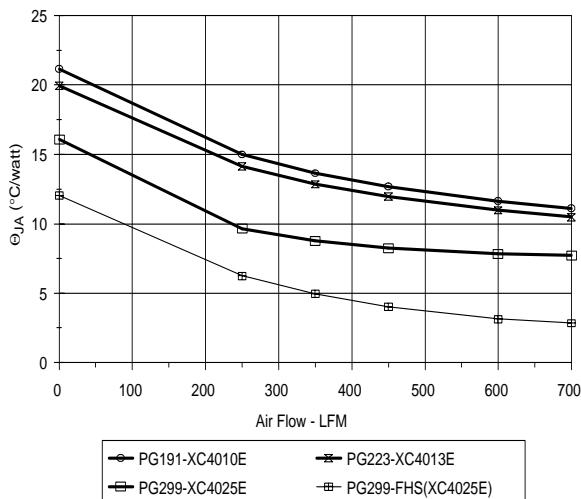
Table 3 shows the package and thermal enhancement combinations required to meet the goal of  $T_J < 100^\circ C$ .

For all solutions, the junction temperature is calculated as:  $T_J = \text{Power} \times \Theta_{JA} + T_A$ . All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements -- such as forced air cooling, heat sinking, etc. may be necessary to meet the  $T_J(\text{max})$  conditions set.

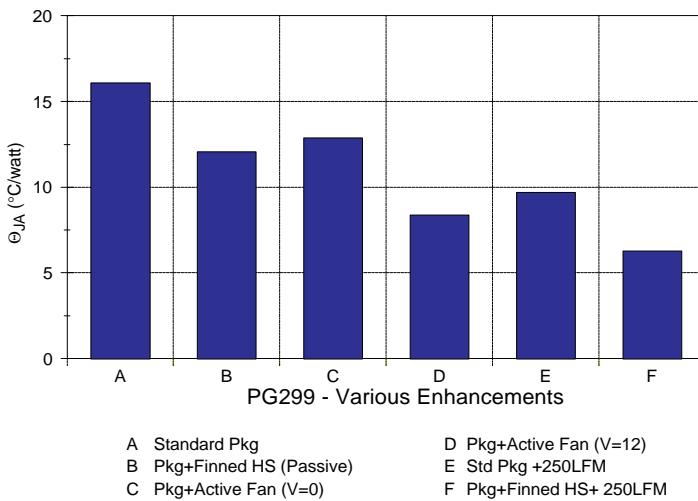
## PQ/HQ Thermal Data Comparison

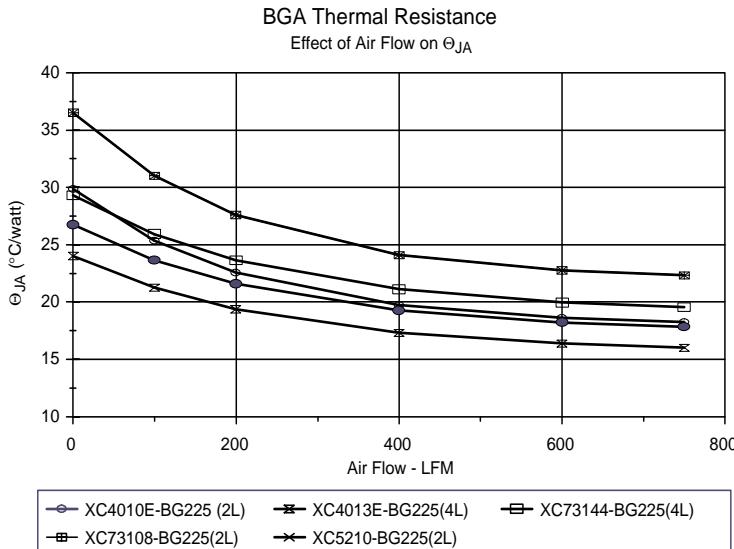


**PGA 299 Thermal Resistance**  
Effect of Air Flow on  $\Theta_{JA}$



**PG299 Thermal Resistance**  
Effects of Active & Passive Heat sinks





## Some Power Management Options

FPGA devices are usually not the dominating power consumers in a system, and do not have a big impact on power supply designs. There are obvious exceptions. When the actual or estimated power dissipation appears to be more than the specification of the chosen package, some options can be considered. Details on the engineering designs and analysis of some of these suggested considerations may be obtained from the references listed at the end of the section. The options include:

- A Xilinx low power (L) version of the circuit in the same package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated. For more information, contact the Xilinx Hotline group.
- Explore thermally enhanced package options available for the same device. As illustrated above, the HQ240 package has a thermal impedance of about 50% of the equivalent PQ240. Besides, the 240 lead, the 208 lead and the 304 lead Quad packages have equivalent heatsink enhanced versions. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink enhanced packages. Most of the high gate count devices above the XC4013 level come either exclusively in heat enhanced packages or have these packages as options. If the use of a standard PQ appears to be a handicap in this respect, a move to the

equivalent HQ package if available may resolve the issue. The heat enhanced packages are pin to pin compatible and they use the same board layout.

- The use of forced air is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200 -- 300 LFM) can reduce junction to ambient thermal resistance by 30%.
- If space will allow, the use of finned external heatsinks can be effective. If implemented with forced air as well, the benefit can be a 40% to 50% reduction. The HQ304, all cavity down PGAs, and the BG352 with exposed heatsink lend themselves to the application of external heatsinks for further heat removal efficiency.
- Outside the package itself, the board on which the package sits can have a significant impact. Board designs may be implemented to take advantage of this. Heat flows to the outside of a board mounted package and is sunk into the board to radiate. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package. Some of the heatsink packages with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal.

## References

### Forced Air Cooling Application Engineering

COMAIR ROTRON  
2675 Custom House Court  
San Ysidro, CA 92173  
1-619-661-6688

### Heatsink Application Engineering

The following facilities provide heatsink solutions for industry standard packages.

**AAVID Thermal Technologies**  
1 Kool Path  
Box 400  
Laconia, NH 03247-0400  
1-603-528-3400

### Thermalloy, Inc.

2021 W. Valley View Lane  
Box 810839  
Dallas, TX 75381-0839  
1-214-243-4321

### Wakefield Engineering, Inc.

60 Audubon Road  
Wakefield MA 01880-1255  
1-617-245-5900

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

## Package Electrical Characterization

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

## Theoretical Background

There are three major electrical parameters which are used to describe the package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC & RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. The lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are:  $I = C * dv/dt$ . Current

spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires:  $V = L * di/dt$ . The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

## Analytical Formulas for Lead Inductance

### 1. Rectangular Leadframe/Trace (straight)

$$L_{self} = 5I \left[ \ln\left(\frac{2I}{w+t}\right) + \frac{1}{2} \right] \text{ nH}$$

(no ground)

$$L_{self} = 5I \left[ \ln\left(\frac{8h}{w+t}\right) + \left(\frac{w+t}{4h}\right) \right] \text{ nH}$$

(above ground)

$I$  = lead/trace length

$w$  = lead/trace width

$t$  = lead/trace thickness

$h$  = ground height

unit = inches

## 2. Bondwire (gold wire)

$$L_{\text{wire}} = 5I \left[ \ln\left(\frac{2I}{r}\right) - \frac{3}{4} \right] \text{ nH}$$

I = wire length

r = wire radius

unit = inches

## General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

### Package & Fixture Preparation

Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self & mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e. QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self & mutual) measurements are finished units with all internal leads floating. The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides small ground loop to minimize ground inductance of the fixture.

### Inductance & Capacitance Measurement Procedure

For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and

parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead/bondwire and returns by the path of the low-impedance ground. On the adjacent "quiet" lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture. For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the "bulk" capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

### Inductance & Capacitance Model Extraction

All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

## Data Acquisition and Package Electrical Database

Xilinx acquires electrical parasitic data only on the longest and the shortest lead/traces of the package. This provides the best and the worst case for each package type (defined by package design, lead/ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes.

The average of these samples is then kept as the official measured parasitic data of that package type in the database.

## Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BG225	MOLDED BGA 27 mm FULL MATRIX	MO-151-CAL	OBG0001	2.2
BG256	MOLDED BGA 27 mm SQ	MO-151-CAL	OBG0011	2.2
BG352	SUPERBGA - 35 X 35 mm PERIPHERAL	MO-151-BAR	OBG0008	7.1
BG432	SUPERBGA - 40 X 40 mm PERIPHERAL	MO-151-BAU	OBG0009	9.1
BG560	SUPERBGA - 42.5 X 42.5 mm SQ	MO-192-BAV	OBG0010	11.5
CB100	NCTB TOP BRAZE 3K VER	MO-113-AD <sup>3</sup>	OCQ0008	10.8
CB100	NCTB TOP BRAZE 4K VER	MO-113-AD <sup>3</sup>	OCQ0006	10.8
CB164	NCTB TOP BRAZE 3K VER	MO-113-AA-AD <sup>3</sup>	OCQ0003	11.5
CB164	NCTB TOP BRAZE 4K VER	MO-113-AA-AD <sup>3</sup>	OCQ0007	11.5
CB196	NCTB TOP BRAZE 4K VER	MO-113-AB-AD <sup>3</sup>	OCQ0005	15.3
CB228	NCTB TOP BRAZE 4K VER	MO-113-AD <sup>3</sup>	OCQ0012	17.6
DD8	.300 CERDIP PACKAGE	MO-036-AA	OPD0005	1.1
HQ160	METRIC 28 28 -.65 mm 1.6H/S DIE UP	MO-108-DDI	OPQ0021	10.8
HQ208	METRIC 28 X 28 - H/S DIE UP	MO-143-FA1	OPQ0020	10.8
HQ240	METRIC QFP 32 32 - H/S DIE UP	MO-143-GA	OPQ0019	15.0
HQ304	METRIC QFP 40 40-H/S DIE DOWN	MO-143-JA	OPQ0014	26.2
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP .300 STANDARD	MO-001-AA	OPD0002	0.5
PG84	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0003	7.2
PG120	CERAMIC PGA 13 X 13 MATRIX	MO-067-AE	OPG0012	11.5
PG132	CERAMIC PGA 14 X 14 MATRIX	MO-067-AF	OPG0004	11.8
PG156	CERAMIC PGA 16 X 16 MATRIX	MO-067-AH	OPG0007	17.1
PG175	CERAMIC PGA 16 X 16 STD VER.	MO-067-AH	OPG0009	17.7
PG191	CERAMIC PGA 18 X 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	CERAMIC PGA 18 X 18 TYPE	MO-067-AK	OPG0016	26.0
PG299	CERAMIC PGA 20 X 20 HEATSINK	MO-067-AK	OPG0022	37.5
PG299	CERAMIC PGA 20 X 20 TYPE	MO-067-AK	OPG0015	29.8
PG411	CERAMIC PGA 39 X 39 STAGGER	MO-128-AM	OPG0019	36.7
PG475	CERAMIC PGA 41 X 41 STAGGER	MO-128-AM	OPG0023	39.5
PG559	CERAMIC PGA 43 x 43	MO-128	OPG0025	44.50
PP132	PLASTIC PGA 14 X 14 MATRIX	MO-83-AF	OPG0001	8.1
PP175	PLASTIC PGA 16 X 16 BURIED	MO-83-AH	OPG0006	11.1
PQ100	EIAJ 14 X 20 QFP - 1.60	MO-108-CC1	OPQ0013	1.6
PQ160	EIAJ 28 X 28 .65 mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 X 28 .5 mm 1.30	MO-143-FA1	OPQ0003	5.3
PQ240	EIAJ 32 X 32 .5 mm	MO-143-GA	OPQ0010	7.1
SO8	VERSION 1 - .150/55MIL	MO-150	OPD0006	0.1
TQ100	THIN QFP 1.4 mm thick	MS-026-BDE	OPQ0004	0.7
TQ144	THIN QFP 1.4 mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	THIN QFP 1.4 mm thick	MS-026-BGA	OPQ0008	1.9

## Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
VO8	THIN SOIC-II	N/A	OPD0007	0.1
VQ44	THIN QFP 1.0 thick	MS-026-ACB	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
VQ100	THIN QFP 1.0 thick	MS-026-AED	OPQ0012	0.6

Notes: 1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.  
 2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.  
 3. Tie-bar details are specific to Xilinx package. Lead width minimum is 0.056".

## Xilinx Thermally Enhanced Packaging

### The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ160	28x28	3.40	10.8	DOWN	MO-108-DD1	OPQ0021
HQ208	28x28	3.40	10.0	DOWN	MO-143-FA	OPQ0020
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014

### Overview

Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

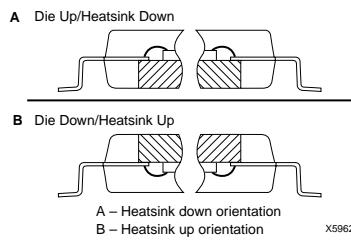
- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

### Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240 pin count level or below are offered with the heatsink at the bottom of the

package. This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.

- At the 304 pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.



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### Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

	HQ (gm)	PQ (gm)
160 Pin	10.8	5.8
208 Pin	10.8	5.3
240 Pin	15.0	7.1
304 Pin	26.2	N/A

## Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Still Air Data Comparison		
	HQ $\Theta_{JA}$ (°C/Watt)	PQ $\Theta_{JA}$ (°C/watt)
160 Pin	13.5-14.5	20.5-38.5
208 Pin	14-15	26-35
240 Pin	12-13	19-28
304 Pin	10-11	N/A

Note:  $\Theta_{JC}$  is typically between 1 and 2 °C/Watt for HQ and MQ Packages. For PQ's, it is between 2 and 7 °C/Watt.

Data Comparison at Airflow - 250 LFM		
	HQ $\Theta_{JA}$ (°C/watt)	PQ $\Theta_{JA}$ (°C/watt)
160 Pin	9-10	15-28.5
208 Pin	9-10	14-26
240 Pin	8-9	11-21
304 Pin	6.5-8	N/A

## Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated → Heatsink metal is Grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material - Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd. Same as PQ - EME7304LC
- Packed in the same JEDEC trays

## Moisture Sensitivity of PSMCs

### Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contami-

nants to the die surface and increasing the potential for early device failure.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details -- materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112. Test Method A112 "Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices".

Available through Global Engineering Documents  
Phone: USA and Canada 800-854-7179, International 1-303-792-2181

- IPC Standard IPC-SM-786A "Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs".

Available through IPC  
Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established 6 levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in [Table 4](#). Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In [Table 4](#), the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

**Table 4: Package Moisture Sensitivity Levels per J-STD-020**

Level	Factory Floor Life		Soak Requirements (Preconditioning)			Conditions
	Conditions	Time	Time		Conditions	
1	≤30°C / 90% RH	Unlimited	168 hours		85°C / 85% RH	
2	≤30°C / 60% RH	1 year	168 hours		85°C / 60% RH	
			Time (hours)			
			X +	Y =	Z	
3	≤30°C / 60% RH	168 hours	24	168	192	30°C / 60% RH
4	≤30°C / 60% RH	72 hours	24	72	96	30°C / 60% RH
5	≤30°C / 60% RH	24/28 hours	24	24/48	48/72	30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	30°C / 60% RH

Notes: X = Default value of semiconductor manufacturer's time between bake and bag. If the semiconductor manufacturer's actual time between bake and bag is different from the default value, use the actual time.

Y = Floor life of package after it is removed from dry pack bag.

Z = Total soak time for evaluation.

## Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in [Table 4](#). If factory floor conditions are outside the stated environmental conditions (30°C/90% RH for level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

## Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C., in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor

the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

## Handling Parts in Sealed Bags

### Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

### Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in part appearance can verify moisture levels.

### Expiration Date

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated

bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

### **Other Conditions**

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This

## **Tape and Reel**

Xilinx offers a tape & reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive Polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape & reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

### **Benefits**

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape & reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Anti-static reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape & reel shipments include desiccant pouches and humidity indicators to insure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481.

provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, if the factory floor life has not been exceeded. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

## **Material and Construction**

### **Carrier Tape**

- The pocketed carrier Tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded 'live bug' or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into an automated board assembly equipment.

### **Cover Tape**

- An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.
- Surface resistivity on both sides is less than 1011 ohms per square inch.

### **Reel**

- The reel is made of anti-static Polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.
- A protective strip made of conductive Polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.
- Surface resistivity is less than 1011 ohms per square inch.
- Device loading orientation is in compliance with EIA Standard 481.

### **Bar Code Label**

- The bar code label on each reel provides customer identification, device part number, date code of the

product and quantity in the reel.

- Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.
- The label is an alphanumeric, medium density Code 39 labels.
- This machine-readable label enhances inventory

management and data input accuracy.

#### **Shipping Box**

- The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, # 3 white 'pizza' box, rated to 200 lb test.

**Table 5: Tape & Reel Packaging**

Package Type	Pin Count	Carrier Width	Cover Width	Pitch	Reel Size	Qty per Reel
PLCC (Plastic Leaded Chip Carrier)	20	16 mm	13.3 mm	12 mm	7 inch	250
	20	16 mm	13.3 mm	12 mm	13 inch	750
	44	32 mm	25.5 mm	24 mm	13 inch	500
	68	44 mm	37.5 mm	32 mm	13 inch	250
	84	44 mm	37.5 mm	36 mm	13 inch	250
SO (Plastic Small Outline)	8	12 mm	9.2 mm	8 mm	7 inch	750
QFP (Plastic Quad Flat Pack) PQ, VQ, TQ, HA	100	44 mm	37.5 mm	32 mm	13 inch	250
	160	44 mm	37.5 mm	40 mm	13 inch	200
BGA (Plastic Ball Grid Array)	225/256	44 mm	37.5 mm	32 mm	13 inch	500

Notes:

- 1.A minimum of 230mm of empty pockets are provided at the beginning (leader) of each reel.

2.A minimum of 160mm of empty pockets are provided at the end (trailer) of each reel.

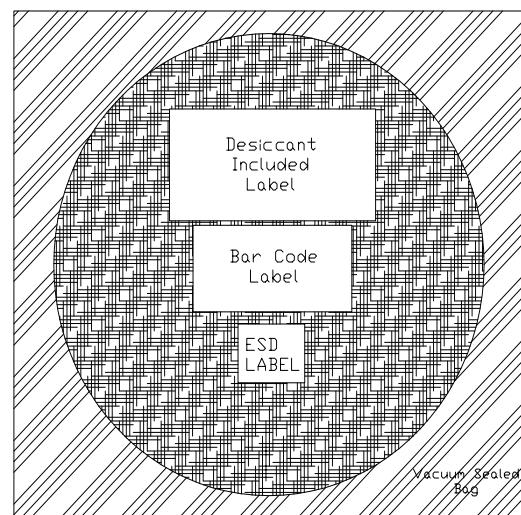
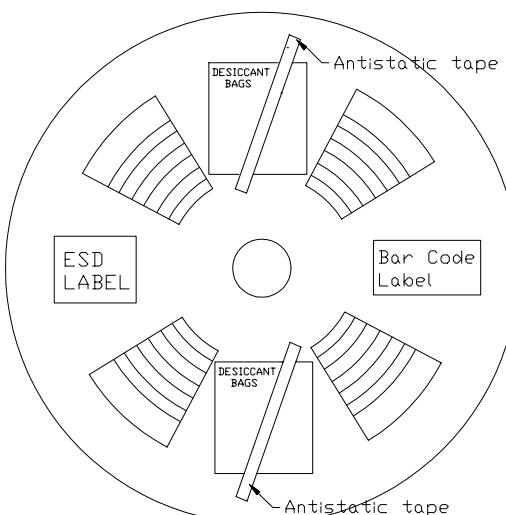
3.Tape Leader/Trailer requirements are in compliance to EIA Standards 481.

4.Peel Strength between 20 and 120 grams ensures consistency during de-reeling operations and is compliant to EIA Standard 481.

5.Each reel is subject to peel back strength tests.

6.For packages not listed above, please contact your Xilinx sales representative for updated information.

## Standard Bar Code Label Locations



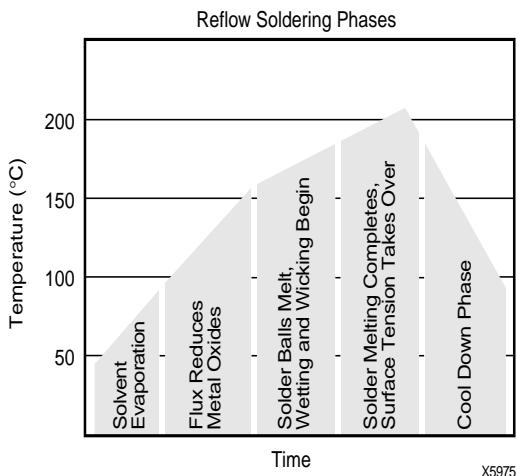
## Reflow Soldering Process Guidelines

In order to implement and control the production of surface mount assemblies, the dynamics of the solder reflow process, and how each element of the process is related to the end result, must be thoroughly understood.

The primary phases of the reflow process are as follows:

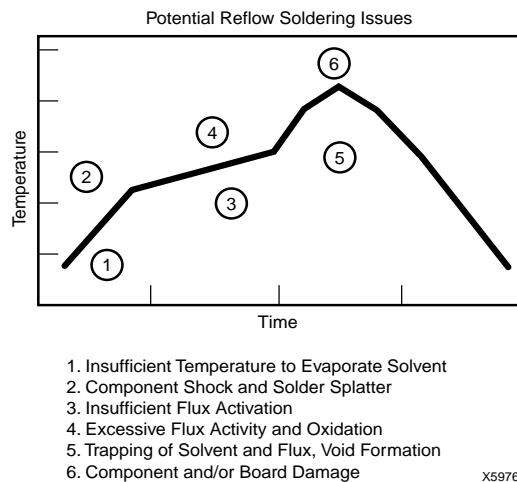
1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in [Figure 2](#).



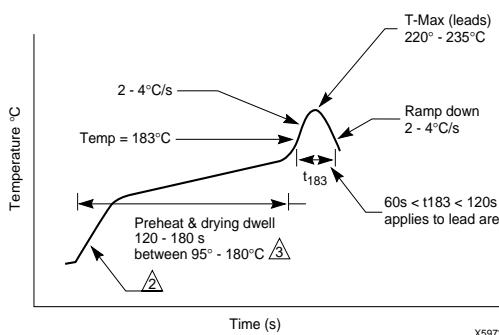
**Figure 2: Soldering Sequence**

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in [Figure 3](#).



**Figure 3: Soldering Problems Summary**

**Figure 4** and **Figure 5** show typical conditions for solder reflow processing using Vapor Phase or IR Reflow. The moisture sensitivity of Plastic Surface Mount Components



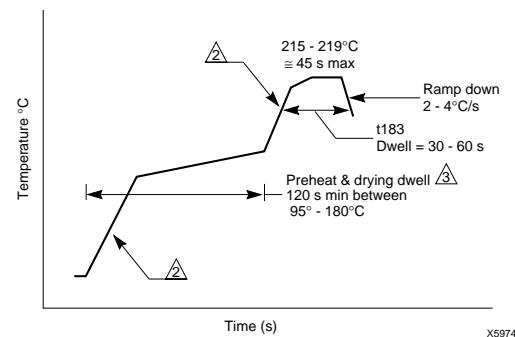
**Figure 4:** Typical conditions for IR reflow soldering

Notes:

1. Max temperature range = 220°C-235°C (leads)  
Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.

(PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.



**Figure 5:** Typical conditions for vapor phase reflow soldering

Notes:

1. Solvent - FC5312 or equivalent - ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

## Sockets

**Table 6** lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorse-

ment by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

**Table 6: Socket Manufacturers**

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	

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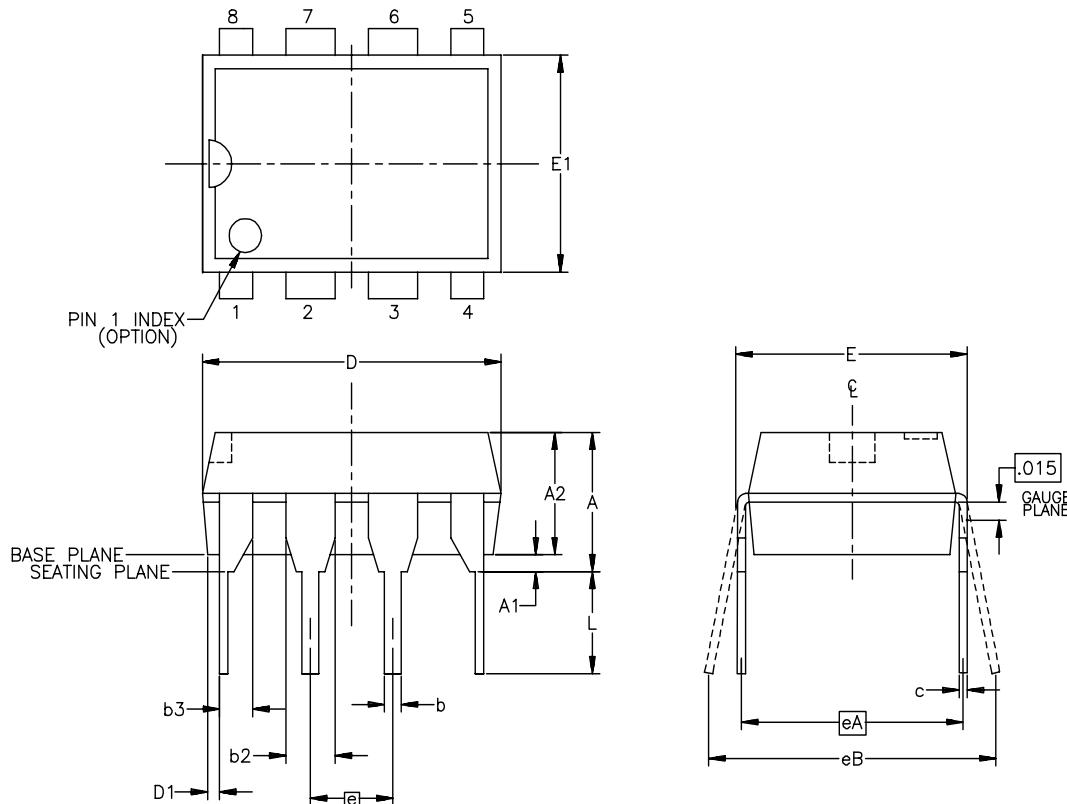
November 13, 1997 (Version 1.2)

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## Package Drawings

Ceramic DIP Package - DD8 .....	10-22
Plastic DIP Package - PD8 .....	10-23
SOIC and TSOP Packages - SO8, VO8 .....	10-24
SOIC Package - SO20 .....	10-25
PLCC Packages - PC20, PC28, PC44, PC68, PC84 .....	10-26
VQFP Packages - VQ44, VQ64, VQ100 .....	10-27
TQFP/HTQFP Packages - TQ100, TQ144, TQ176, HT100, HT144, HT176 .....	10-28
PQ/HQFP Packages - PQ100, HQ100 .....	10-29
PQ/HQFP Packages - PQ44, PQ160, PQ208, PQ240, HQ160, HQ208, HQ240 .....	10-30
PQ/HQFP Packages - PQ304, HQ304 .....	10-31
BGA Packages - BG225 .....	10-32
BGA Packages - BG256 .....	10-33
BGA Packages - BG352, BG432 .....	10-34
BGA Packages - BG560 .....	10-35
Ceramic PGA Packages - PG68, PG84 .....	10-36
Ceramic PGA Packages - PG120, PG132, PG156 .....	10-37
Ceramic PGA Packages - PG175 .....	10-38
Ceramic PGA Packages - PG191 .....	10-39
Ceramic PGA Packages - PG223, PG299 .....	10-40
Ceramic PGA Packages - PG411 .....	10-41
Ceramic PGA Packages - PG475 .....	10-42
Ceramic PGA Packages - PG559 .....	10-42
Chip Scale Packages - CS48, CS144 .....	
 Ceramic Brazed QFP Packages - CB100, CB164, CB196 (XC4000 Version) .....	10-45
Ceramic Brazed QFP Packages - CB228 .....	10-46

## Plastic DIP Package - PD8



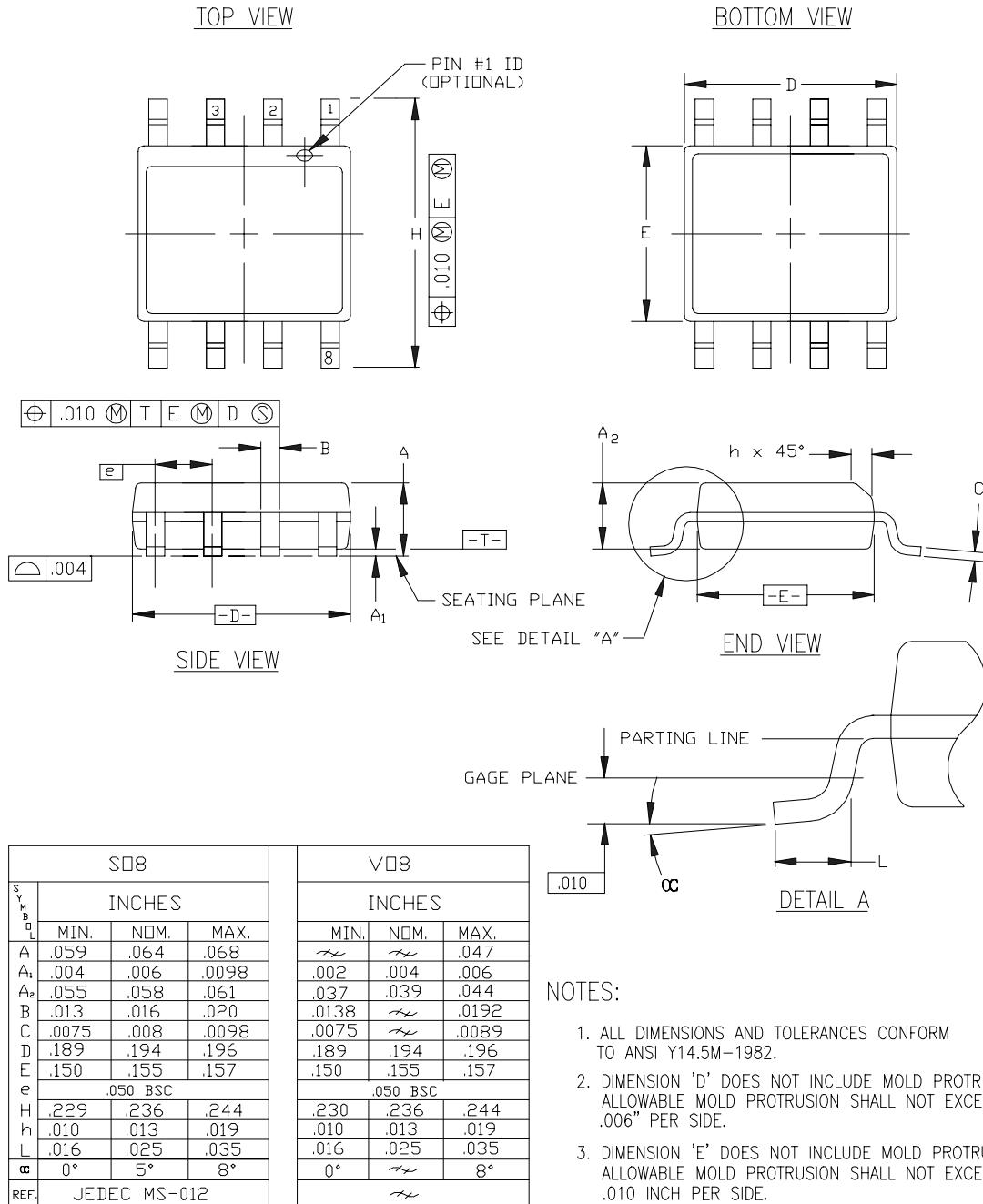
S Y M B L	INCHES		N O T E
	MIN.	MAX.	
A	~	0.181	
A <sub>1</sub>	0.019	~	
A <sub>2</sub>	0.122	0.161	
b	0.014	0.022	
b <sub>2</sub>	0.045	~	
b <sub>3</sub>	~	0.045	
c	0.009	0.012	
D	0.355	0.382	
D <sub>1</sub>	0.005	~	
E	0.303	0.323	
E <sub>1</sub>	0.240	0.272	
e	0.100	BSC	
e <sub>A</sub>	0.300	BSC	
e <sub>B</sub>	~	0.430	
L	0.115	0.150	
N	8		

### NOTES:

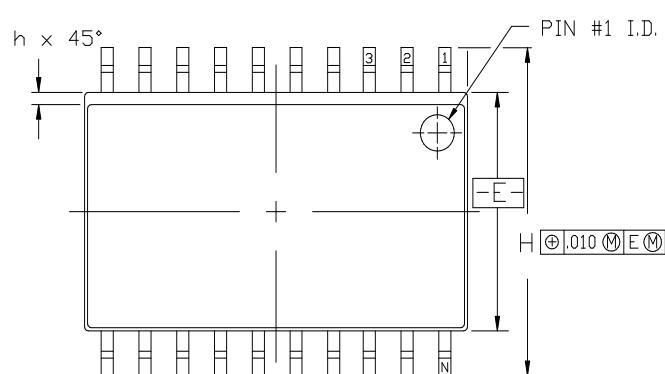
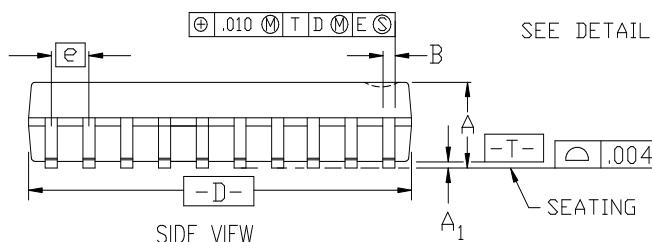
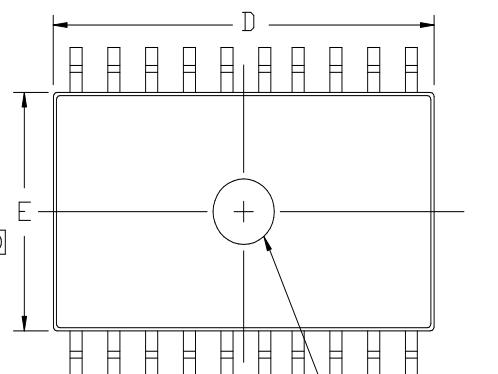
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
3. LEAD FINISH: (85±5%)Sn-Pb SOLDER PLATE
4. CONFORMS TO JEDEC MS-001-BA

8-PIN PLASTIC DIP (PD8)

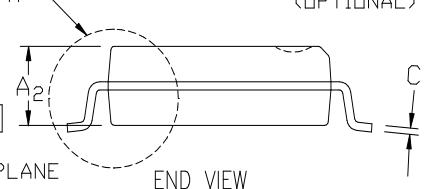
## SOIC and TSOP Packages - SO8, VO8



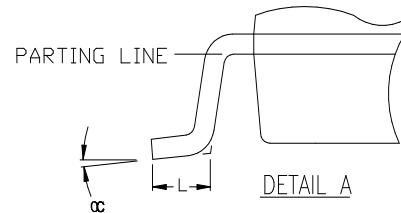
8 LEAD SOIC/TSOP (SO8, VO8)

**SOIC Package - SO20**
TOP VIEW

BOTTOM VIEW


SEE DETAIL A



S Y M B L	INCHES		
	MIN.	NOM.	MAX.
A	.097	.101	.104
A <sub>1</sub>	.005	.009	.0115
A <sub>2</sub>	.090	.092	.094
B	.014	.016	.019
C	.0091	.010	.0125
D	.500	.505	.510
E	.292	.296	.299
e	.050 BSC		
H	.400	.406	.410
h	.010	--	.029
L	.024	.032	.040
$\alpha$	0°	5°	8°

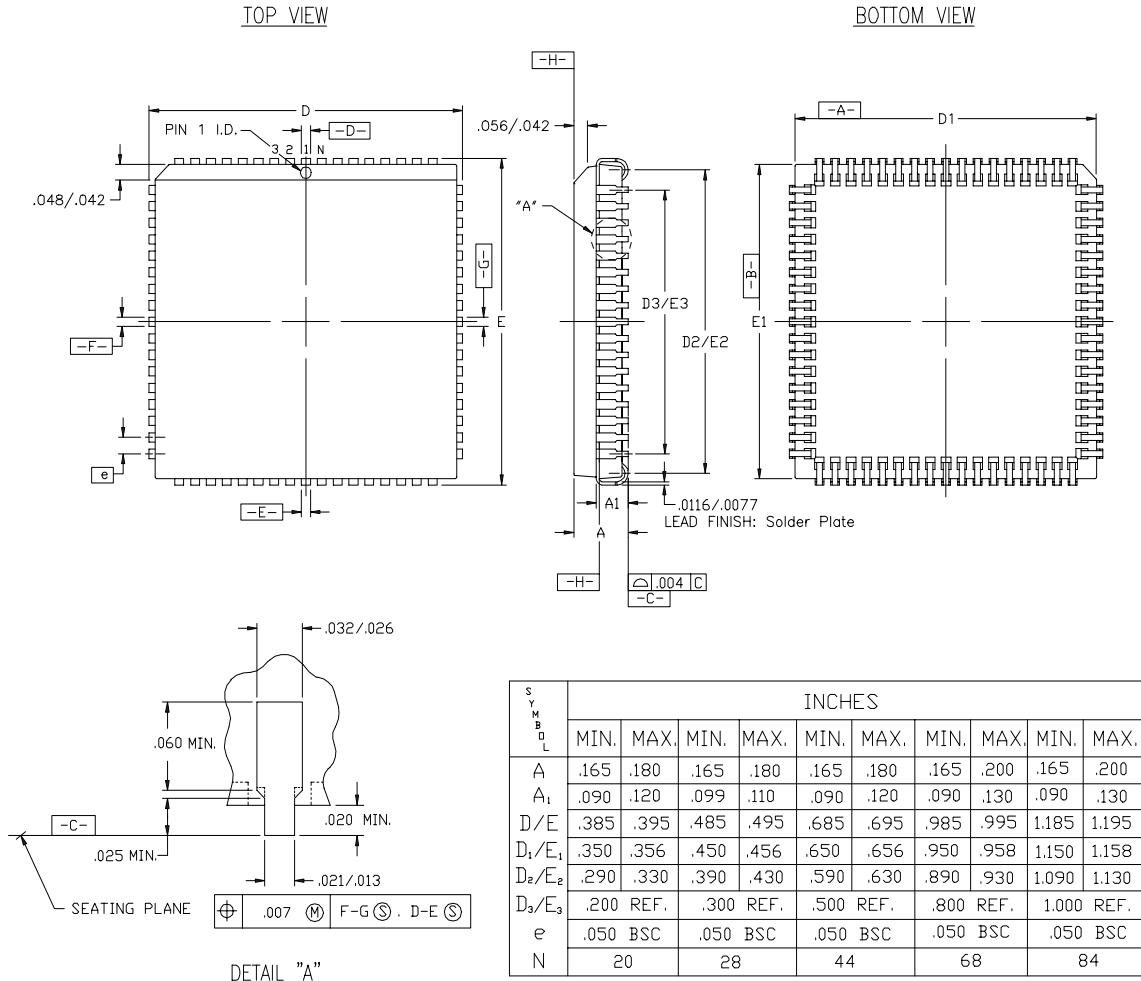


## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "D" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .006" PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED .010" PER SIDE.
4. LEAD FINISH: SOLDER PLATE
5. CONFORMS TO JEDEC MS-013-AC

20 LEAD SOIC (SO20)

## PLCC Packages - PC20, PC28, PC44, PC68, PC84

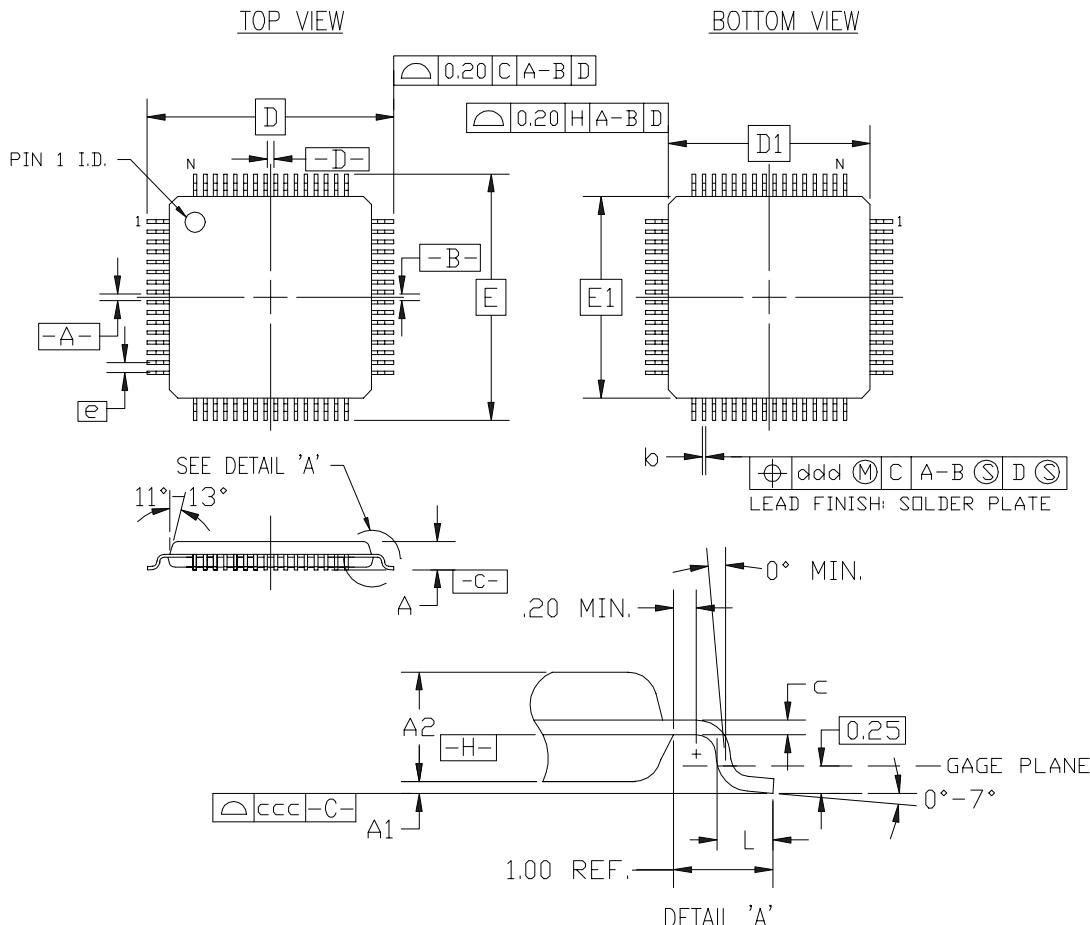


## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSIONS 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE.
3. 'N' IS NUMBER OF TERMINALS.
4. CONFORM TO JEDEC MO-047
5. TOP OF PACKAGE MAY BE SMALLER THAN BOTTOM BY .010".

20, 28, 44, 68 and 84-PIN PLCC (PC20 THRU PC84)

## VQFP Packages - VQ44, VQ64, VQ100



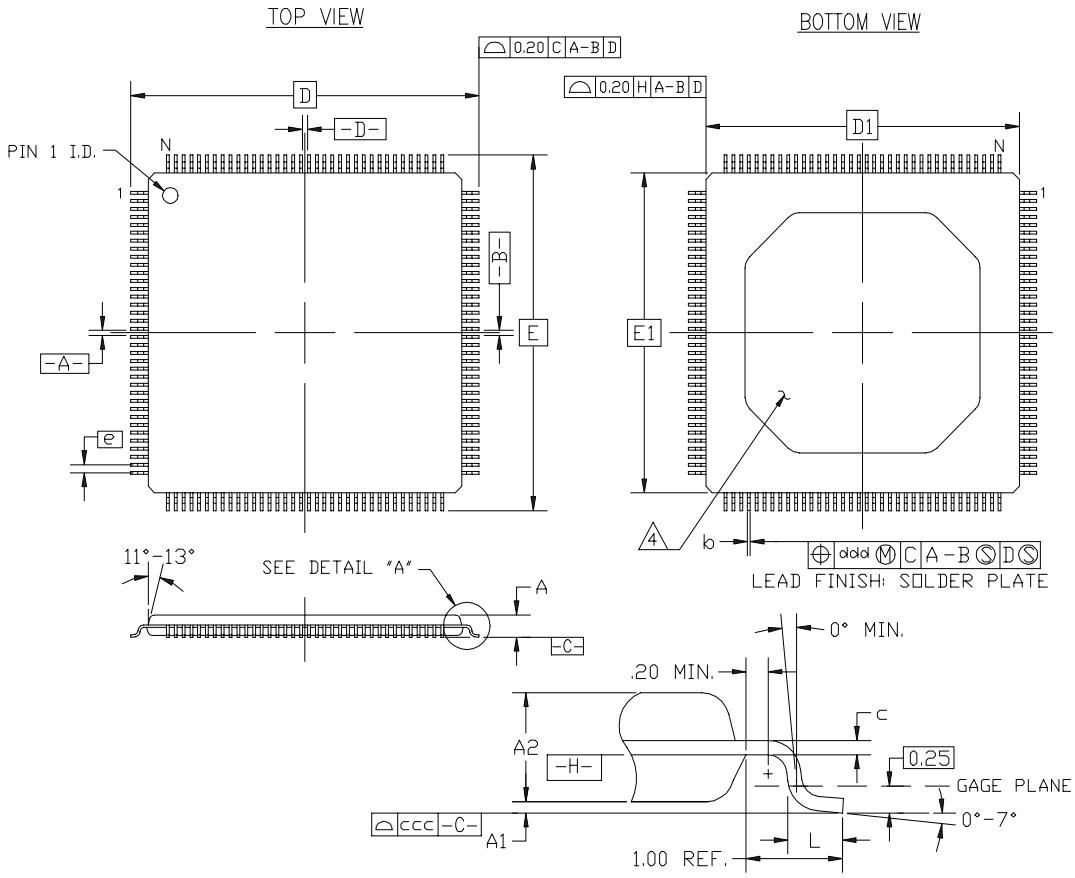
VQ44			VQ64			VQ100		
S Y M B O L	MILLIMETERS		MILLIMETERS		MILLIMETERS		MILLIMETERS	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.
A	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
A <sub>1</sub>	0.05	0.15	0.15	0.05	0.10	0.15	0.05	0.10
A <sub>2</sub>	1.00	1.05	1.05	1.00	1.05	1.05	1.00	1.05
D/E	12.00	BSC		12.00	BSC		16.00	BSC
D <sub>1</sub> /E <sub>1</sub>	10.00	BSC		10.00	BSC		14.00	BSC
b	0.30	0.37	0.45	0.17	0.22	0.27	0.17	0.22
c	0.09	0.20	0.20	0.09	0.20	0.20	0.09	0.20
e	0.80	BSC		0.50	BSC		0.50	BSC
L	0.45	0.60	0.75	0.45	0.60	0.75	0.45	0.60
ccc	0.10			0.08			0.08	
ddd	0.20			0.08			0.08	
N	44			64			100	
REF.	JEDEC MS-026-ACB		JEDEC MS-026-ACD		JEDEC MS-026-AED			

### NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
- DIMENSIONS D<sub>1</sub> AND E<sub>1</sub> DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
- THE TOP OF PACKAGE MAY BE SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.

44, 64, 100-PIN PLASTIC VERY THIN QFP (VQ44, VQ64, VQ100)

## TQFP/HTQFP Packages - TQ100, TQ144, TQ176, HT100, HT144, HT176



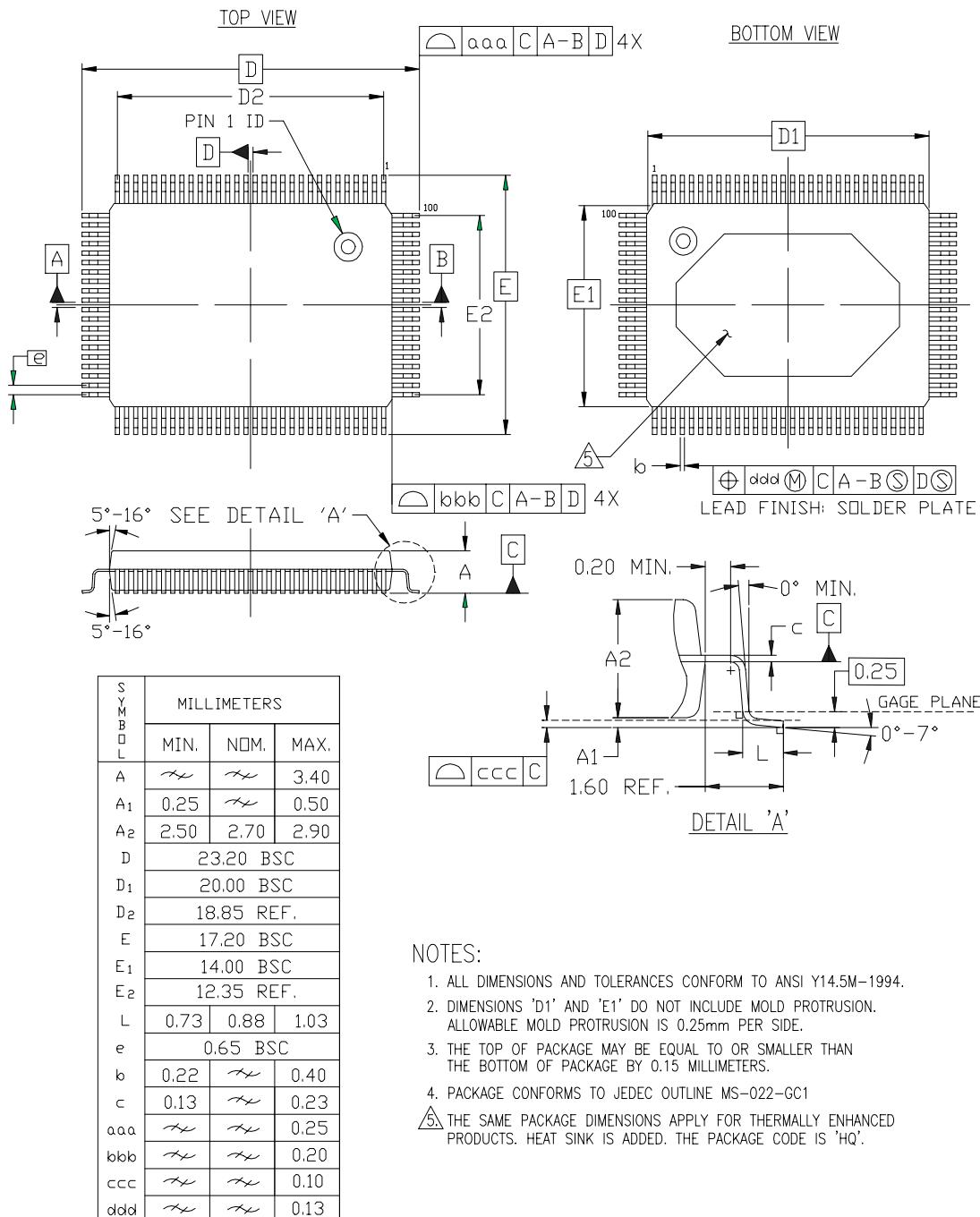
TQ/HT100			TQ/HT144			TQ/HT176			
S	MILLIMETERS		S	MILLIMETERS		S	MILLIMETERS		
	MIN.	NOM.		MIN.	NOM.		MIN.	NOM.	MAX.
A	1.60		A	1.60		A	1.60		
A <sub>1</sub>	0.05	0.15	A <sub>1</sub>	0.05	0.10	A <sub>1</sub>	0.05	0.10	0.15
A <sub>2</sub>	1.35	1.40	A <sub>2</sub>	1.35	1.40	A <sub>2</sub>	1.35	1.40	1.45
D/E	16.00	BSC	D/E	22.00	BSC	D/E	26.00	BSC	
D <sub>1</sub> /E <sub>1</sub>	14.00	BSC	D <sub>1</sub> /E <sub>1</sub>	20.00	BSC	D <sub>1</sub> /E <sub>1</sub>	24.00	BSC	
L	0.45	0.60	L	0.45	0.60	L	0.45	0.60	0.75
e	0.50	BSC	e	0.50	BSC	e	0.50	BSC	
b	0.17	0.22	b	0.17	0.22	b	0.17	0.22	0.27
c	0.09	0.20	c	0.09	0.20	c	0.09	0.20	
ccc	0.08		ccc	0.08		ccc	0.08		
ddd	0.08		ddd	0.08		ddd	0.08		
N	100			144			176		
REF.	JEDEC MS-026-BED		JEDEC MS-026-BFB		JEDEC MS-026-BGA				

## NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5-1982
  2. DIMENSION D<sub>1</sub> AND E<sub>1</sub> DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
  3. PACKAGE TOP DIMENSION MAY BE SMALLER THAN THE BOTTOM DIMENSION BY 0.15mm.
- ⚠** THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HT".

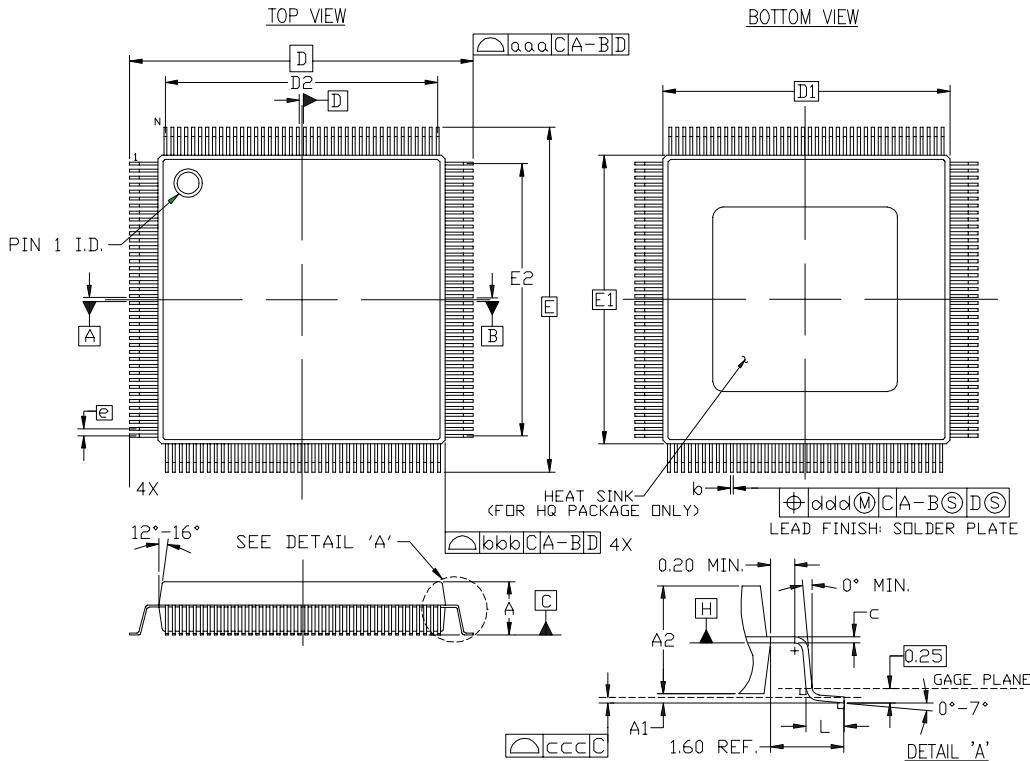
100, 144, 176-PIN TQFP/HEAT SINK TQFP (TQ/HT100, 144, 176)

## PQ/HQFP Packages - PQ100, HQ100



100-PIN PQFP (PQ100)  
100-PIN HEAT SINK PQFP (HQ100)

## PQ/HQFP Packages - PQ44, PQ160, PQ208, PQ240, HQ160, HQ208, HQ240



PQ44			
S Y M L	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.15	2.35	
A <sub>1</sub>	0.05	0.25	
A <sub>2</sub>	1.95	2.00	2.10
D/E	13.20	BSC	
D <sub>1</sub> /E <sub>1</sub>	10.00	BSC	
D <sub>2</sub> /E <sub>2</sub>	8.00	REF.	
L	0.73	0.88	1.03
e	0.80	BSC.	
b	0.30	0.45	
c	0.13	0.23	
aaa	0.25		
bbb	0.20		
ccc	0.10		
ddd	0.20		
N	44		
REF.	JEDEC MS-022-AB		

PQ/HQ160			
S Y M L	MILLIMETERS		
	MIN.	NOM.	MAX.
	3.70	4.10	
	0.25	0.33	0.50
	3.20	3.40	3.60
	31.20	BSC	
	28.00	BSC	
	25.35	REF.	
	0.73	0.88	1.03
	0.65	BSC.	
	0.22	0.40	
	0.13	0.23	
	0.25		
	0.20		
	0.10		
	0.13		
	160		
REF.	JEDEC MS-022-DD1		

PQ/HQ208			
S Y M L	MILLIMETERS		
	MIN.	NOM.	MAX.
	3.70	4.10	
	0.25	0.33	0.50
	3.20	3.40	3.60
	30.60	BSC	
	28.00	BSC	
	25.50	REF.	
	0.50	0.60	0.75
	0.50	BSC.	
	0.17	0.22	0.27
	0.09	0.20	
	0.25		
	0.20		
	0.10		
	0.08		
	0.08		
	208		
REF.	JEDEC MD-143-FA-1		

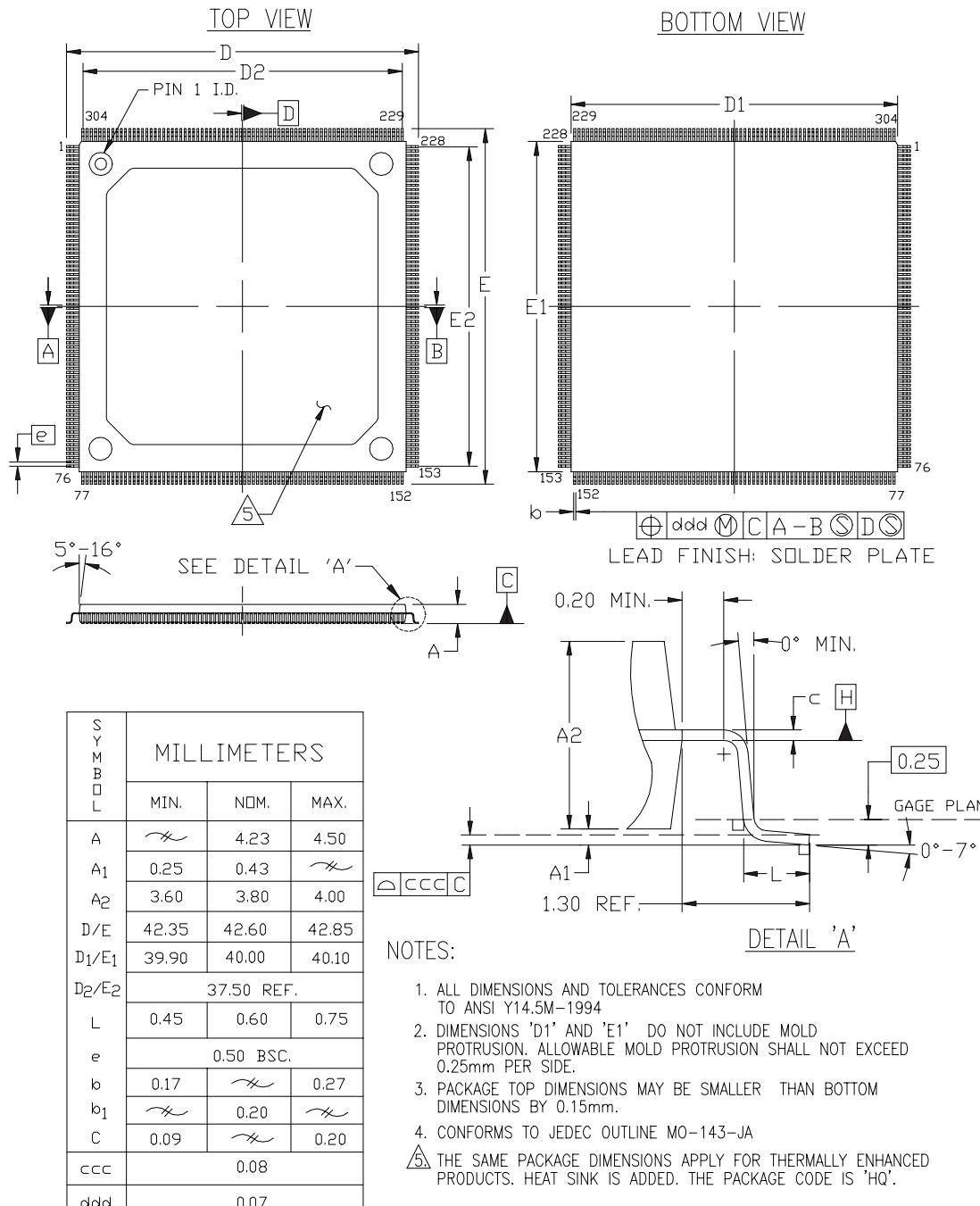
PQ/HQ240			
S Y M L	MILLIMETERS		
	MIN.	NOM.	MAX.
	3.78	4.10	
	0.25	0.38	0.50
	3.20	3.40	3.60
	34.60	BSC	
	32.00	BSC	
	29.50	REF.	
	0.50	0.60	0.75
	0.50	BSC.	
	0.17	0.27	
	0.09	0.20	
	0.25		
	0.20		
	0.08		
	0.08		
	240		
REF.	JEDEC MD-143-GA		

## NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.  
ALLOWABLE MOLD PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
- PACKAGE TOP DIMENSIONS MAY BE SMALLER THAN THE BOTTOM DIMENSIONS BY 0.20mm.
- THE SAME PACKAGE DIMENSIONS APPLY FOR THERMALLY ENHANCED PRODUCTS. HEAT SINK IS ADDED. THE PACKAGE CODE IS "HQ".

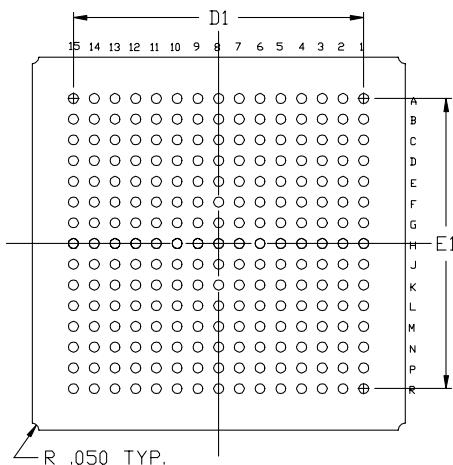
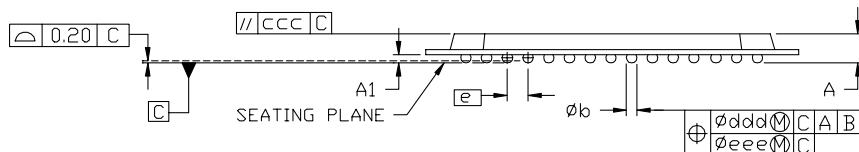
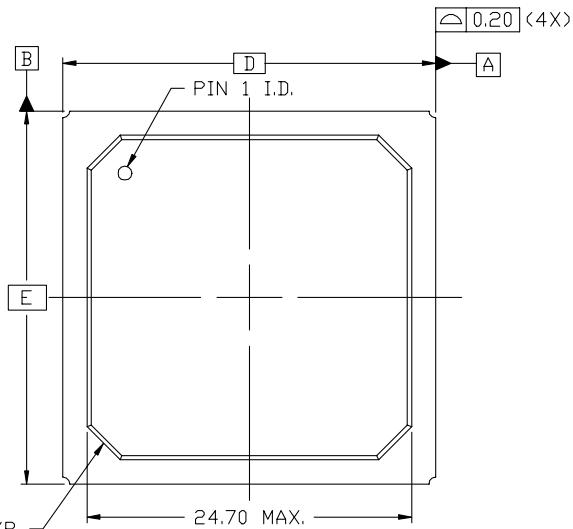
44, 160, 208, 240-PIN PQFP/HEAT SINK PQFP (PQ44, PQ/HQ160, 208, 240)

## PQ/HQFP Packages - PQ304, HQ304



304-PIN PQFP (PQ304)  
304-PIN HEAT SINK PQFP (HQ304)

## BGA Packages - BG225

BOTTOM VIEWTOP VIEW

S Y M B □ L	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.15	3.50	
A <sub>1</sub>	0.50	0.60	0.70
D/E	27.00 BSC		
D <sub>1</sub> /E <sub>1</sub>	21.00 REF.		
e	1.50 BSC		
øb	0.60	0.75	0.90
ccc	0.35	0.35	
ddd	0.30	0.30	
eee	0.15	0.15	
M	15		

## NOTES:

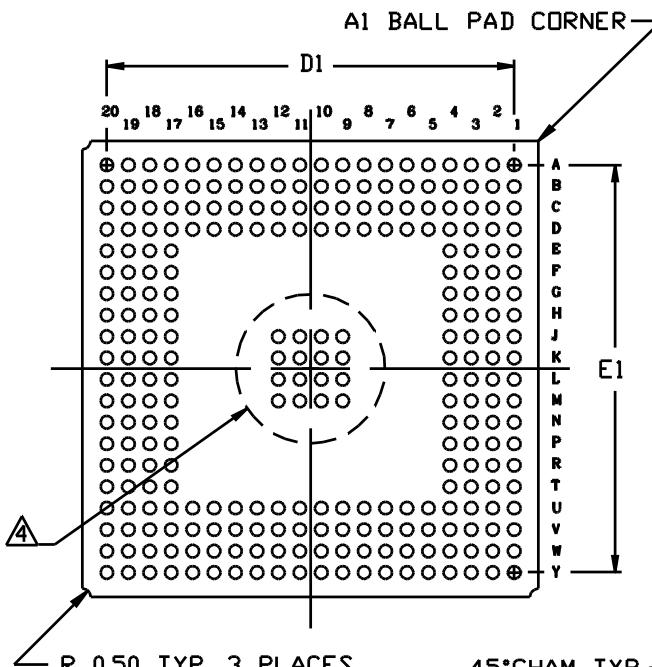
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-151-CAL (DEPOPULATED)

225-BALL PLASTIC BGA (BG225)

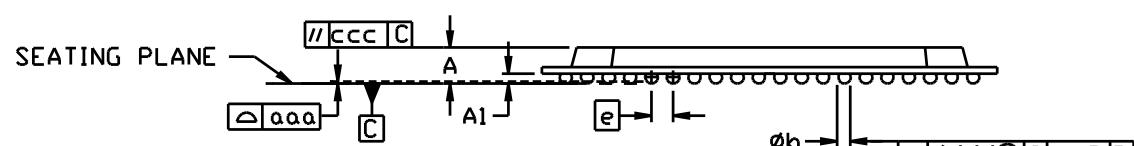
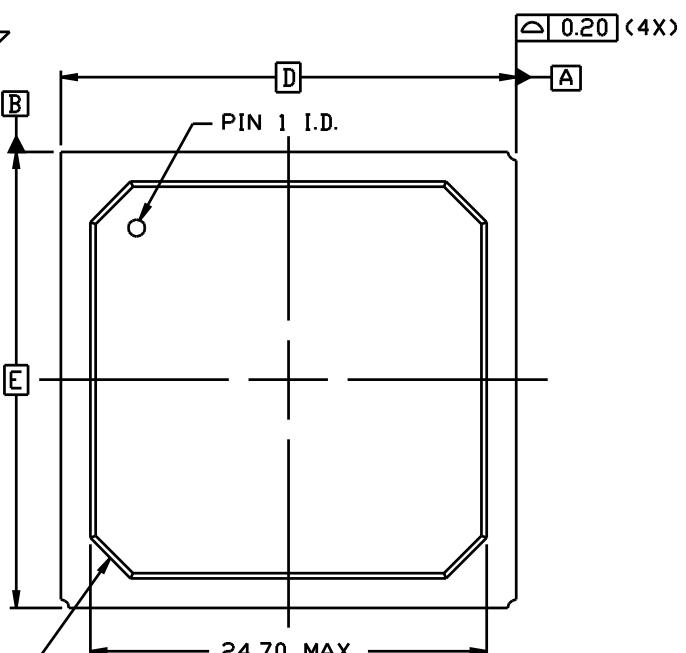
## BGA Packages - BG256

# BG256

BOTTOM VIEW



TOP VIEW

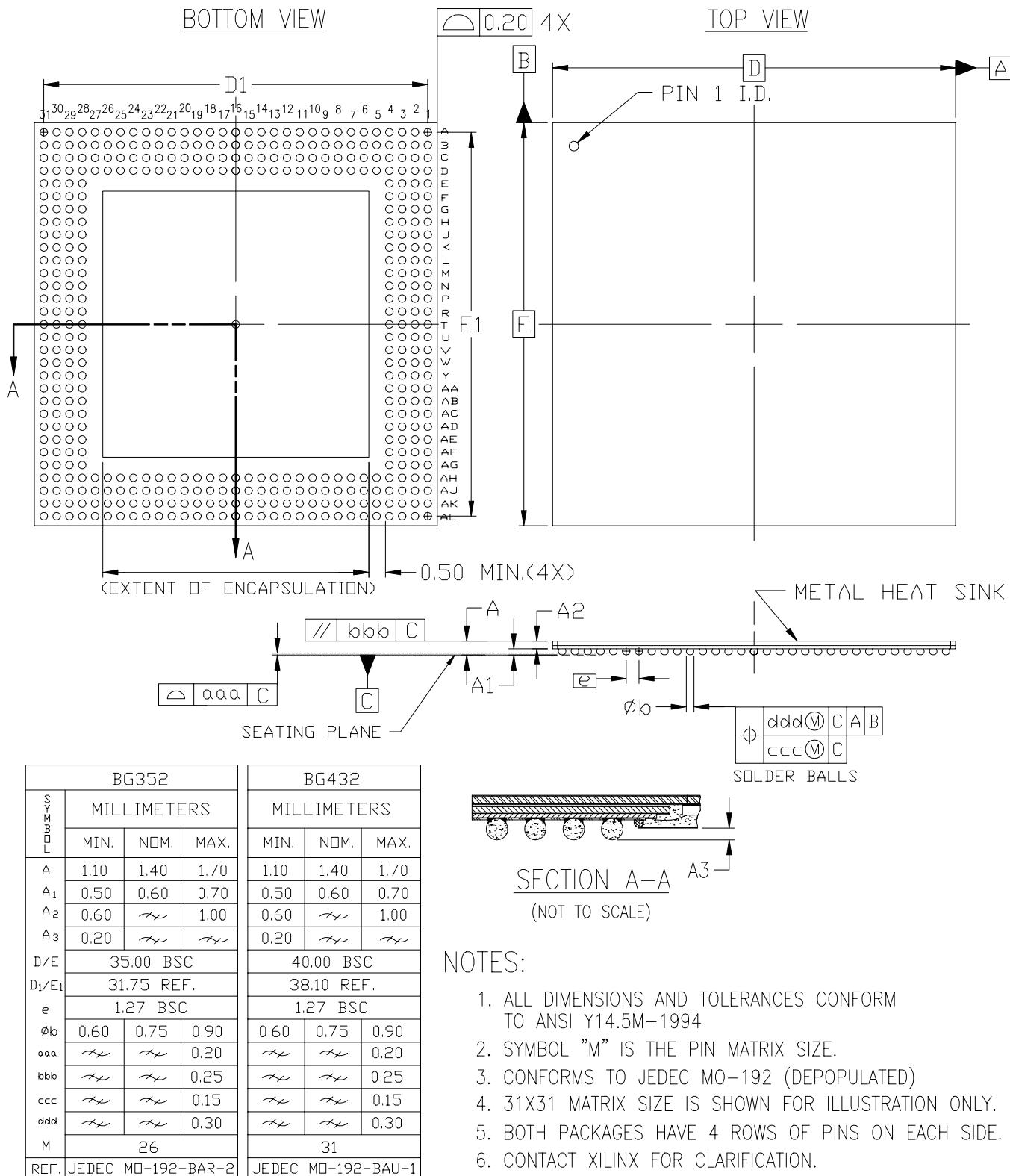


S Y M B O L	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	2.33	3.50
A <sub>1</sub>	0.50	0.60	0.70
D/E 27.00 BSC			
D <sub>1</sub> /E <sub>1</sub> 24.14 REF			
e	1.27 BSC		
φb	0.60	0.75	0.90
aaa	~	~	0.20
ccc	~	~	0.35
ddd	~	~	0.30
eee	~	~	0.15
M	20		

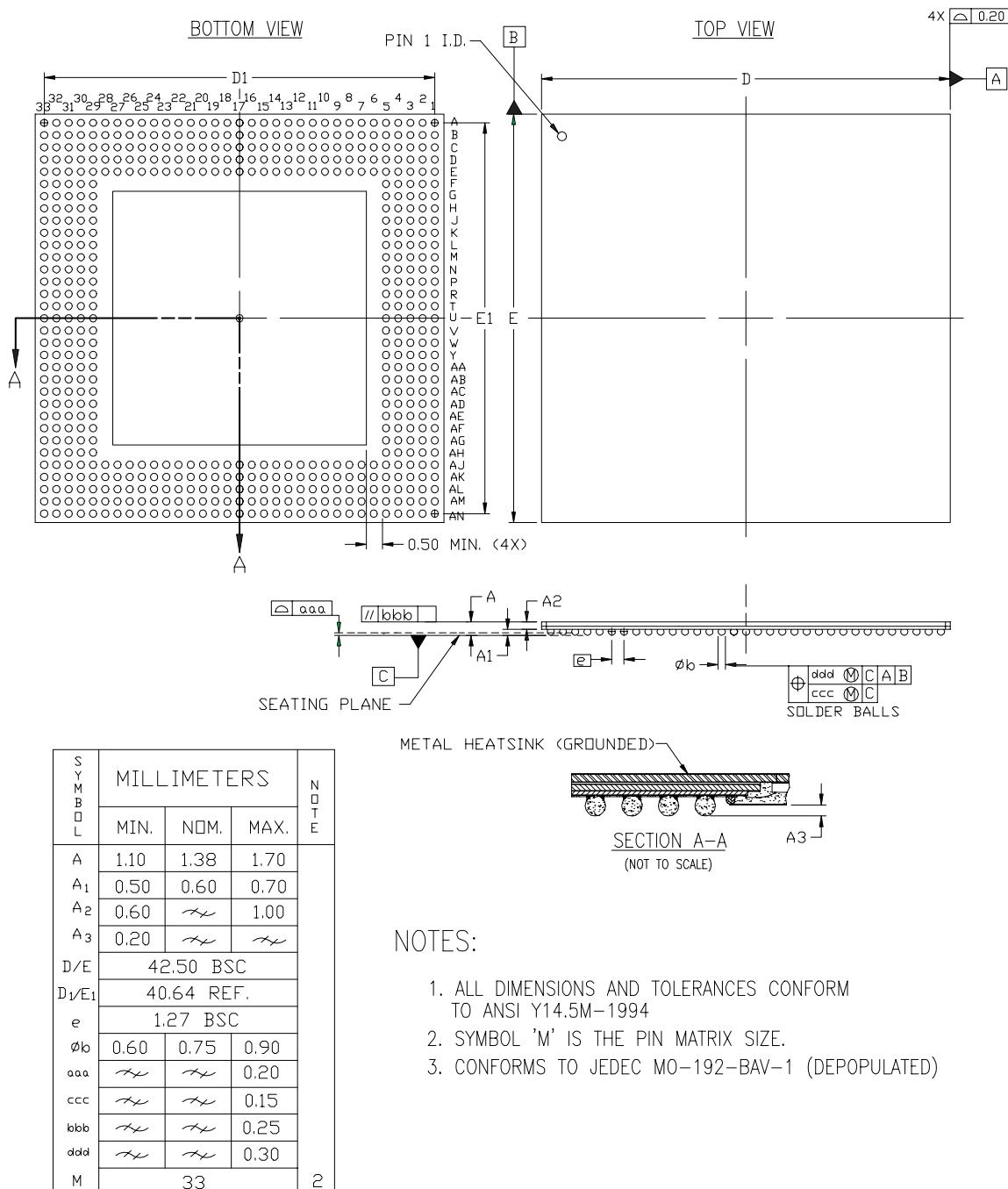
### NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
  2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
  3. CONFORMS TO JEDEC MO-151-BAL-2
- ▲ 16 EXTRA BALLS (GROUNDED) – APPLICABLE TO DEVICES WITH 28K LOGIC GATES OR MORE.

## BGA Packages - BG352, BG432



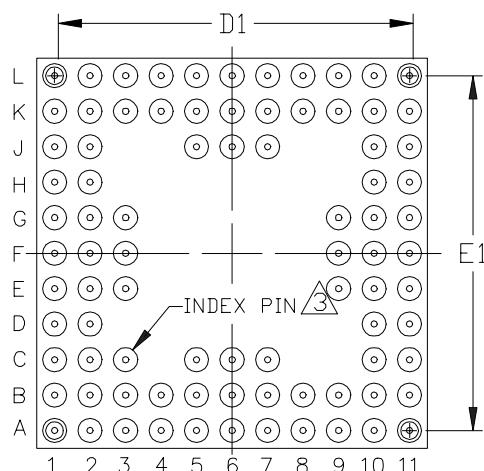
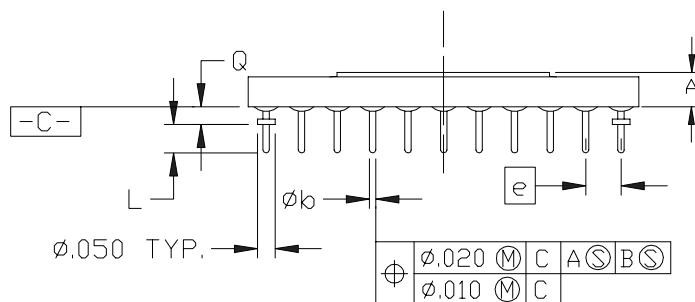
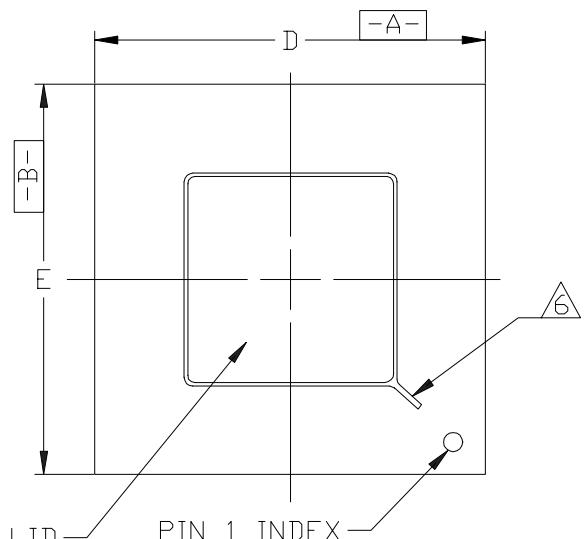
352, 432-BALL PLASTIC BGA (BG352, BG432)  
CAVITY DOWN

**BGA Packages - BG560****NOTES:**

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-192-BAV-1 (DEPOPULATED)

560 BALL PLASTIC BGA (BG560)

## Ceramic PGA Packages - PG68, PG84

BOTTOM VIEWTOP VIEW

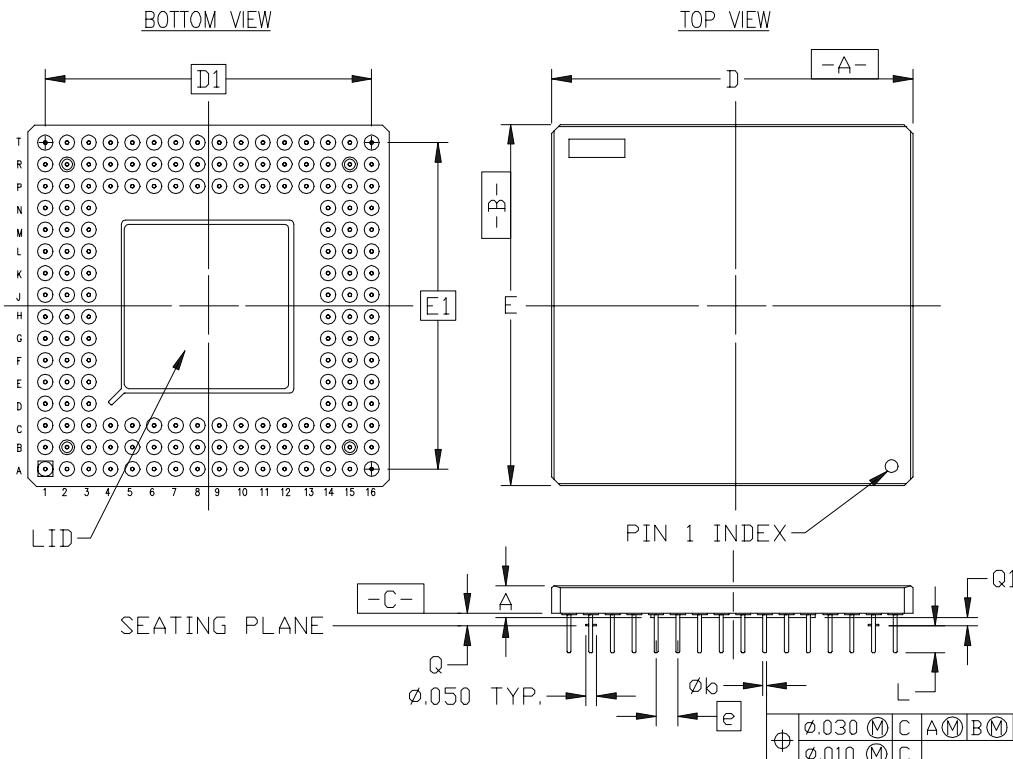
PG68 OR PG84		
S Y M B L	INCHES	
	MIN.	NOM.
A	xx	xx
D/E	1.090	1.100
D <sub>1</sub> /E <sub>1</sub>	1.000	REF.
L	.120	.130
Q	.045	xx
e	.100 BSC	
øb	.016	.018
M	11	
REF.	JEDEC M0-66 AC	

## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL 'M' IS THE PIN MATRIX SIZE.
3. PIN C3 MAY OR MAY NOT BE ELECTRICALLY CONNECTED.
4. PG68 DOES NOT HAVE THIRD ROW ON EACH SIDE EXCEPT THE INDEX PIN.
5. LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)
6. THIS FEATURE IS OPTIONAL, MAYBE AT DIFFERENT LOCATION.

68, 84-PIN CERAMIC PGA (PG68, PG84)

## Ceramic PGA Packages - PG120, PG132, PG156



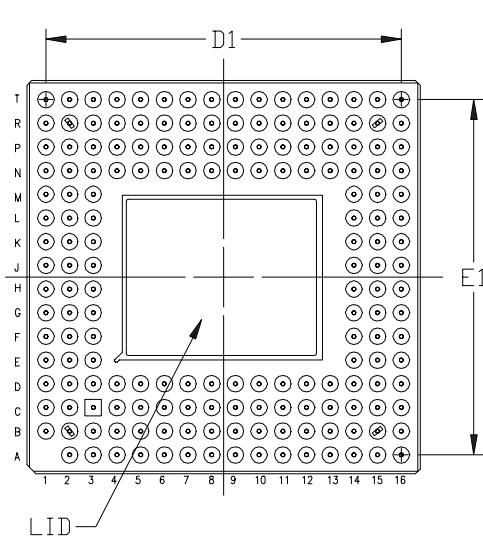
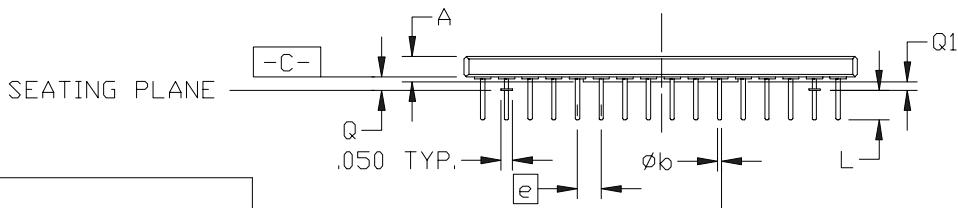
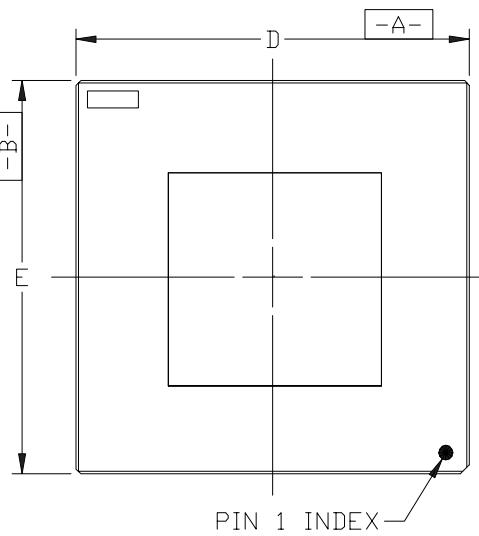
PG120			PG132			PG156				
\$ S Y M B O L	INCHES		INCHES		INCHES		INCHES		INCHES	
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	.120	.130	.140	.120	.130	.140	.120	.130	.140	
D/E	1.340	1.360	1.380	1.440	1.460	1.480	1.640	1.660	1.680	
D <sub>1</sub> /E <sub>1</sub>	1.200 BSC			1.300 BSC			1.500 BSC			
L	.120	.130	.140	.120	.130	.140	.120	.130	.140	
Q	.045	.050	.060	.045	.050	.060	.045	.050	.060	
Q <sub>1</sub>	.025	.030	.035	.025	.030	.035	.025	.030	.035	
e	.100 BSC			.100 BSC			.100 BSC			
øb	.016	.018	.020	.016	.018	.020	.016	.018	.020	
M	13			14			16			
REF.	JEDEC MO-067-AE			JEDEC MO-067-AF			JEDEC MO-067-AH			

### NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
- SYMBOL 'M' IS THE PIN MATRIX SIZE.
- LEAD FINISH: GOLD PLATED
  - COMMERCIAL (.35 MICROINCHES MIN.)
  - MILITARY (.50 MICROINCHES MIN.)

120, 132, 156-PIN CERAMIC PGA (PG120, PG132, PG156)

## Ceramic PGA Packages - PG175

BOTTOM VIEWTOP VIEW

S Y M B Ø L	INCHES		
	MIN.	NOM.	MAX.
A	$\infty$	$\infty$	.145
D/E	1.640	1.660	1.680
D <sub>1</sub> /E <sub>1</sub> 1.500 BSC			
L	.120	.130	.140
Q	.045	$\infty$	.060
Q <sub>1</sub>	.025	$\infty$	$\infty$
e	.100 BSC		
$\phi$ b	.016	.018	.020
M	16		

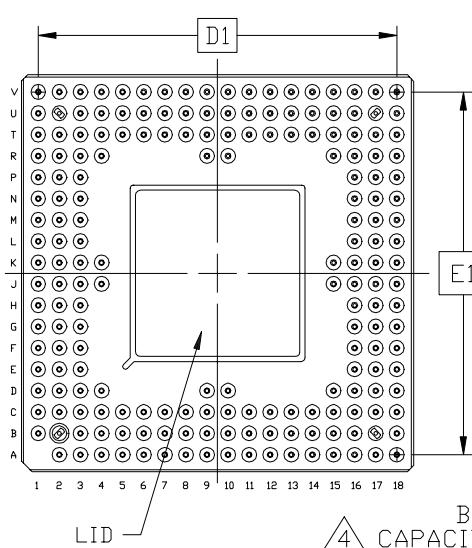
## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL 'M' IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-067-AH
4. LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)

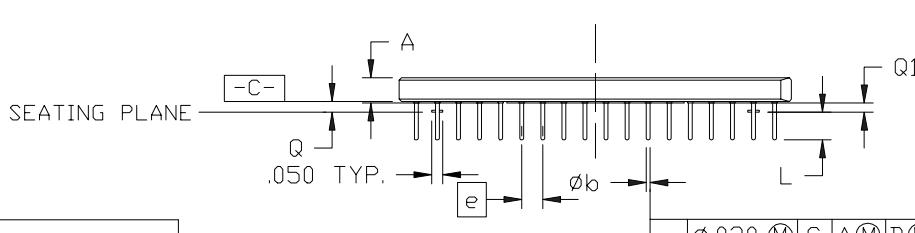
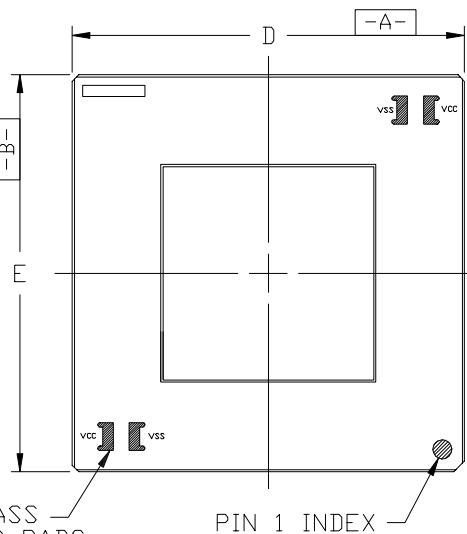
175-PIN CERAMIC PGA (PG175)

## Ceramic PGA Packages - PG191

BOTTOM VIEW



TOP VIEW



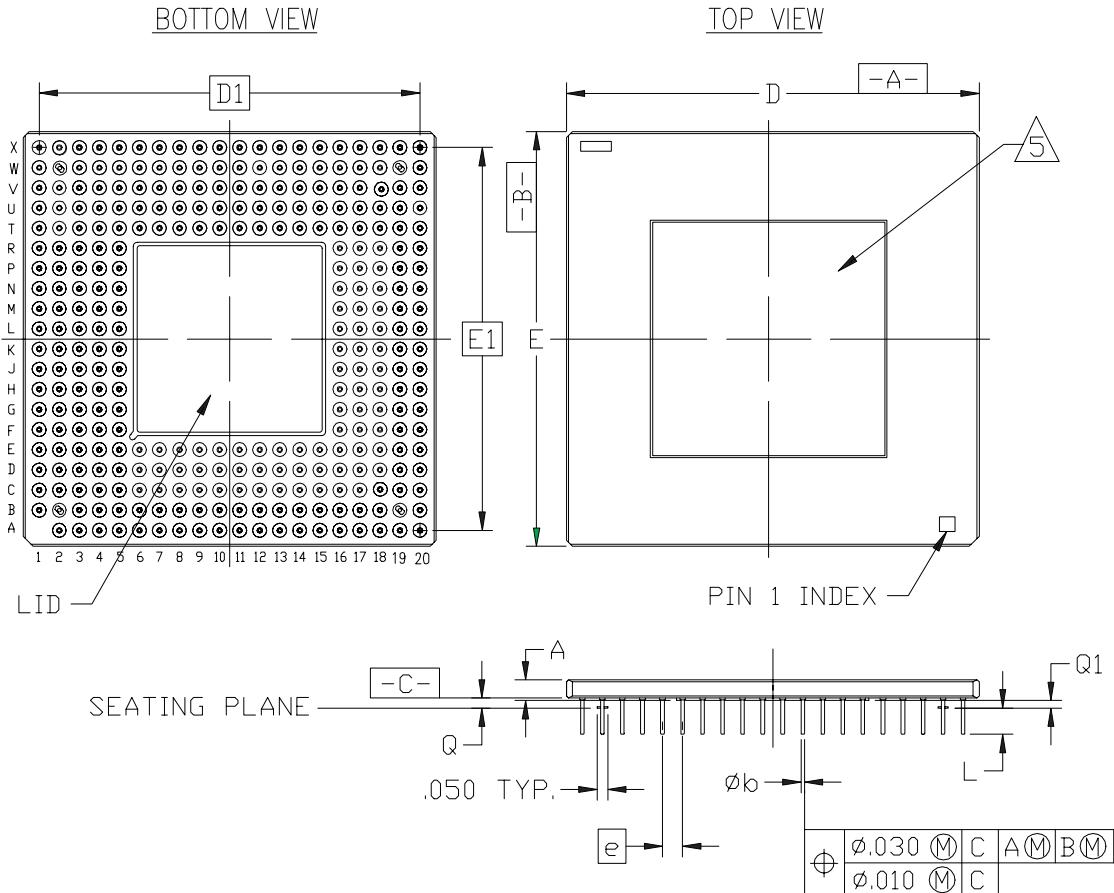
S Y M B L	INCHES		
	MIN.	NOM.	MAX.
A	.115	.145	
D/E	1.840	1.860	1.880
D <sub>1</sub> /E <sub>1</sub>	1.700	BSC	
L	.120	.130	.140
Q	.045	.060	
Q <sub>1</sub>	.025	.025	
e	.100	BSC	
Øb	.016	.018	.020
M	18		

### NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. SYMBOL 'M' IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO-067-AK
4. BYPASS CAPACITOR PADS - GOLD PLATED. MAY OR MAY NOT BE PRESENT ON ALL PACKAGES.
5. LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)

191-PIN CERAMIC PGA (PG191)

## Ceramic PGA Packages - PG223, PG299



PG223			
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	xx	.115	.145
D/E	1.840	1.860	1.880
D <sub>1</sub> /E <sub>1</sub>	1.700 BSC		
L	.120	.130	.140
Q	.045	xx	.060
Q <sub>1</sub>	.025	xx	xx
e	.100 BSC		
øb	.016	.018	.020
M	18		
REF.	JEDEC MO-067-AK		

PG299			
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	xx	xx	.145
D	2.040	2.060	2.080
E	1.900 BSC		
L	.120	.130	.140
Q	.045	xx	.060
Q <sub>1</sub>	.025	xx	xx
e	.100 BSC		
øb	.016	.018	.020
M	20		
REF.	JEDEC MO-067-AM		

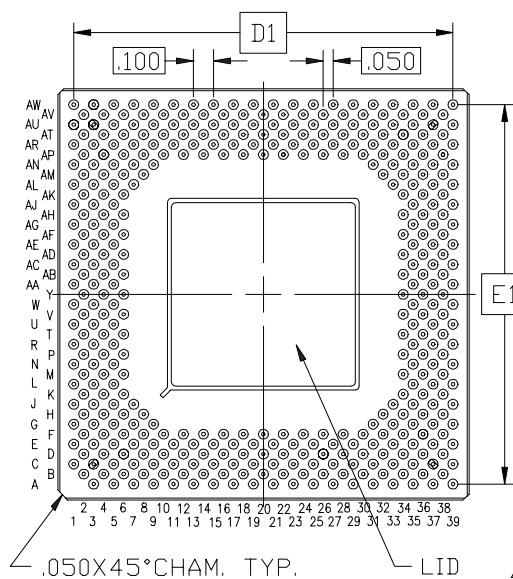
## NOTES:

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
- SYMBOL 'M' IS THE PIN MATRIX SIZE.
- FOR PG223, ONLY 4 ROWS OF PINS ON EACH SIDE.
- LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)
- OPTION - HEAT SINK MAY BE ADDED FOR HIGH POWER DEVICES BUT DIMENSION 'A' REMAINS .145" MAX.
- PG299 20X20 MATRIX SHOWN FOR ILLUSTRATION ONLY.
- CONTACT XILINX FOR CLARIFICATION.

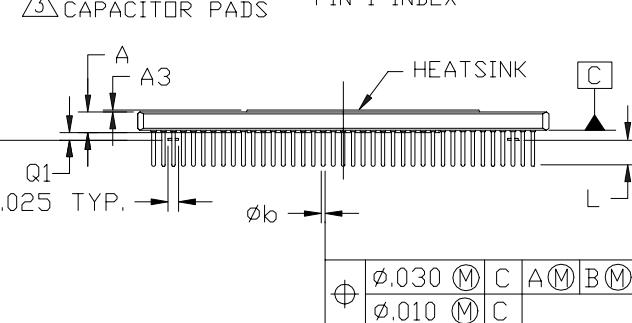
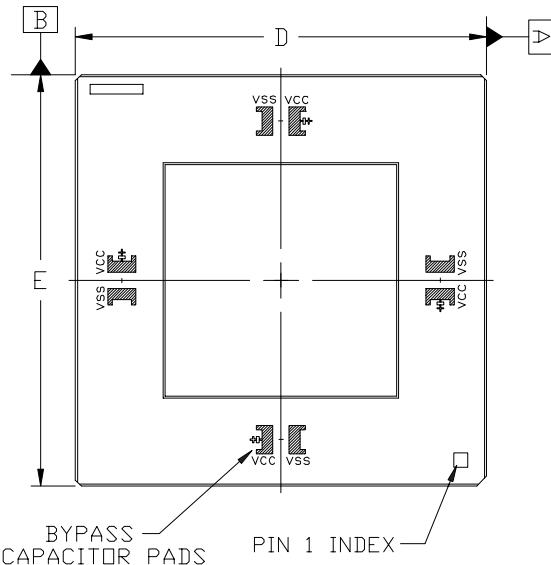
223, 299-PIN CERAMIC PGA (PG223, PG299)

## Ceramic PGA Packages - PG411

BOTTOM VIEW



TOP VIEW



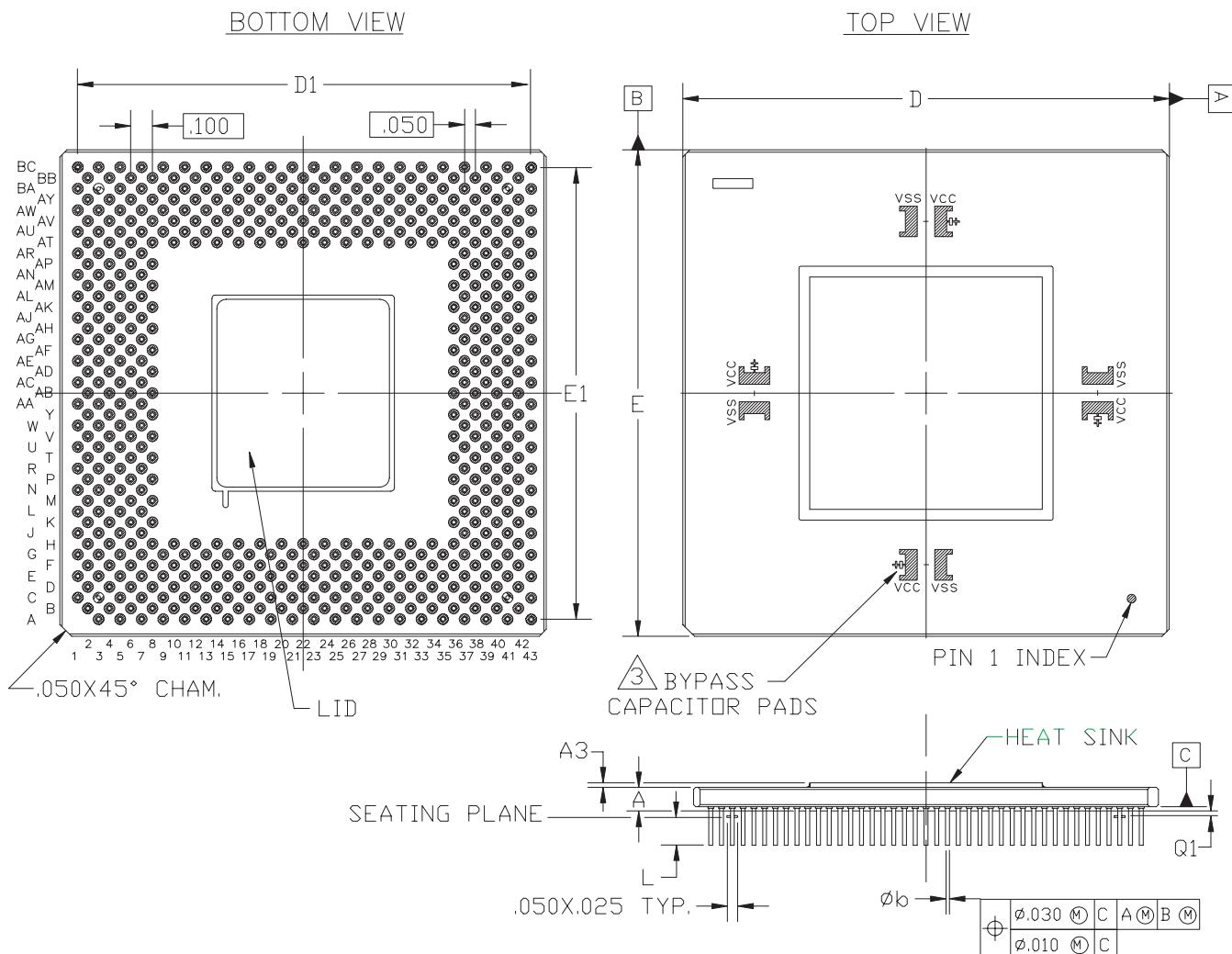
SYMBOL	INCHES		
	MIN.	NOM.	MAX.
A	∞	∞	.165
A3	.015	.020	.025
D/E	2.040	2.060	2.080
D <sub>1</sub> /E <sub>1</sub>	1.900 BSC		
L	.110	∞	.150
Q <sub>1</sub>	.015	∞	.045
M <sub>1</sub>	39		
Ø <sub>b</sub>	.016	.018	.020

### NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE PIN MATRIX SIZE.
3. BYPASS CAPACITOR PADS – GOLD PLATED MAY OR MAY NOT BE PRESENT ON ALL PACKAGES.
4. CONFORMS TO JEDEC MO-128- AM.
5. LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)

411-PIN CERAMIC PGA (PG411)

## Ceramic PGA Packages - PG475, PG559



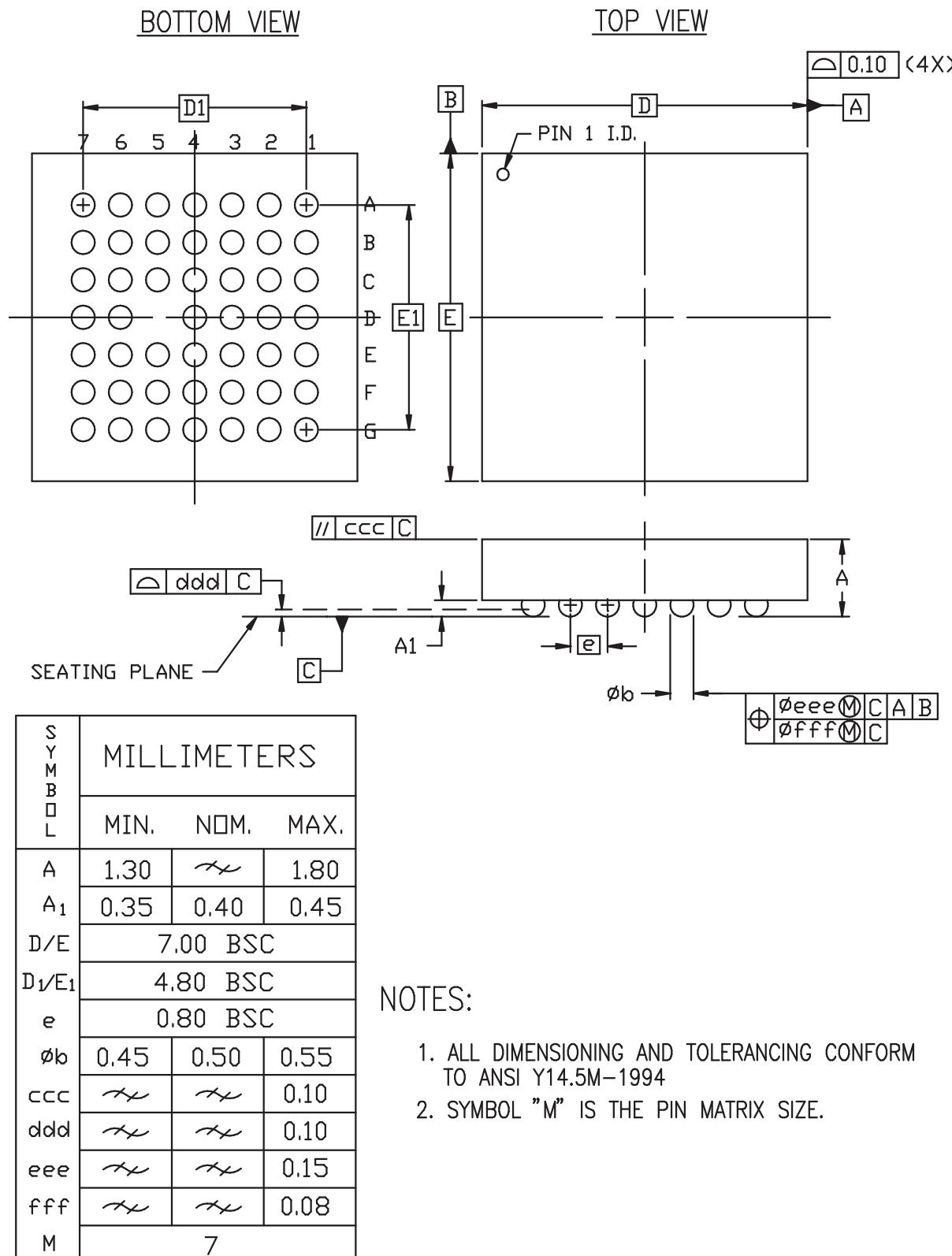
PG475			PG559			
SYMBOL	INCHES		INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	
A	.110	.110	.165	.110	.110	.165
A3	.015	.020	.025	.015	.020	.025
D/E	2.140	2.160	2.180	2.240	2.260	2.280
D <sub>1</sub> /E <sub>1</sub>	2.000 BSC		2.100 BSC			
L	.110	.110	.150	.110	.110	.150
Q <sub>1</sub>	.015	.015	.045	.015	.015	.045
M	41		43			
Øb	.016	.018	.020	.016	.018	.020
REF.	JEDEC M0-128-AN					

## NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994.
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. BYPASS CAPACITOR PADS - GOLD PLATED MAY OR MAY NOT BE PRESENT ON ALL PACKAGES.
4. LEAD FINISH: GOLD PLATED
  - COMMERCIAL (35 MICROINCHES MIN.)
  - MILITARY (50 MICROINCHES MIN.)
5. 43 X 43 MATRIX SHOWN FOR ILLUSTRATION.
6. PG475 - 7 ROWS OF PINS ON EACH SIDE.  
PG559 - 8 ROWS OF PINS ON EACH SIDE.
7. CONTACT XILINX FOR CLARIFICATION.

475, 559-PIN CERAMIC PGA (PG475, PG559)

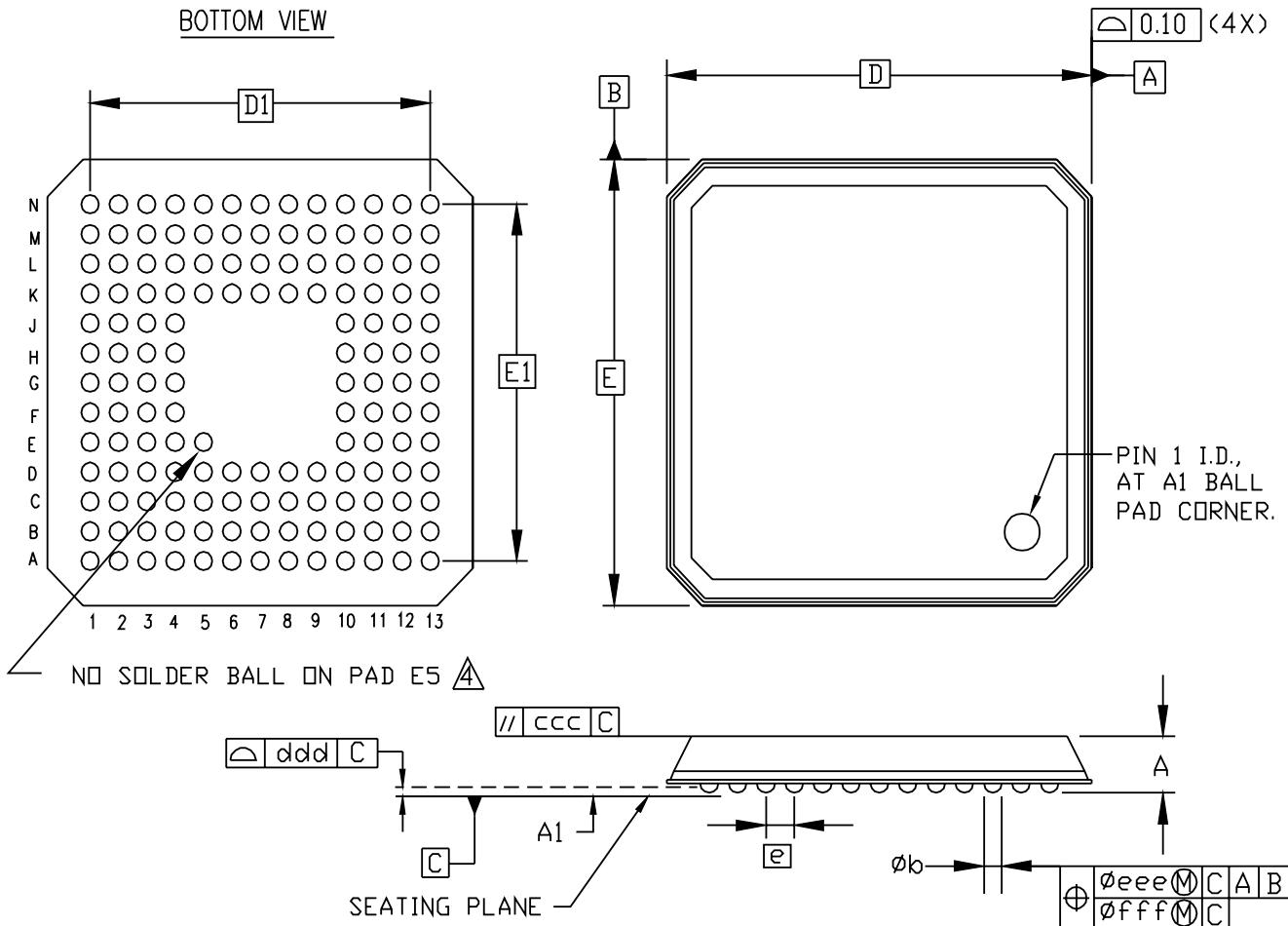
## Chip Scale Package - CS48



48-BALL CHIP SCALE BGA (CS48)

## Chip Scale Package - CS144

BOTTOM VIEW



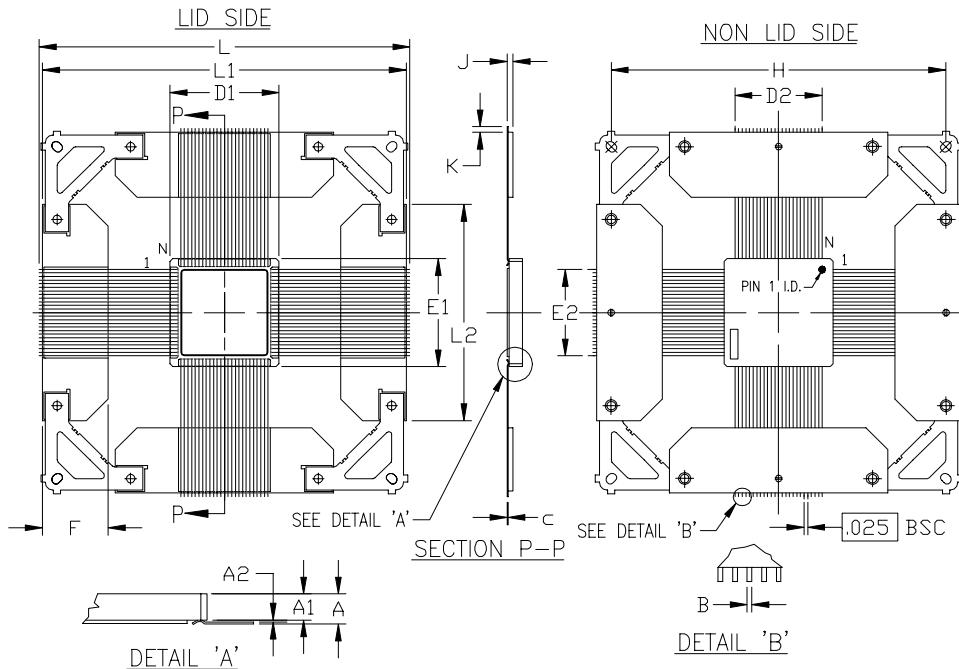
S Y M B D L	MILLIMETERS		
	MIN.	NOM.	MAX.
A	~	~	1.20
A <sub>1</sub>	0.35	0.40	0.45
D/E	12.00 BSC		
D <sub>1</sub> /E <sub>1</sub>	9.60 BSC		
e	0.80 BSC		
b	0.45	0.50	0.55
ccc	~	~	0.10
ddd	~	~	0.12
eee	~	~	0.15
fff	~	~	0.08
M	13		

### NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
  2. SYMBOL "M" IS THE PIN MATRIX SIZE.
  3. CONFORMS TO JEDEC MO-205-BE (DEPOPULATED).
- ④ PAD 'E5' IS FOR PAD 'A1' CORNER INDICATION.

144-BALL CHIP SCALE BGA (CS144)

## Ceramic Braze QFP Packages - CB100, CB164, CB196 (XC4000 Version)



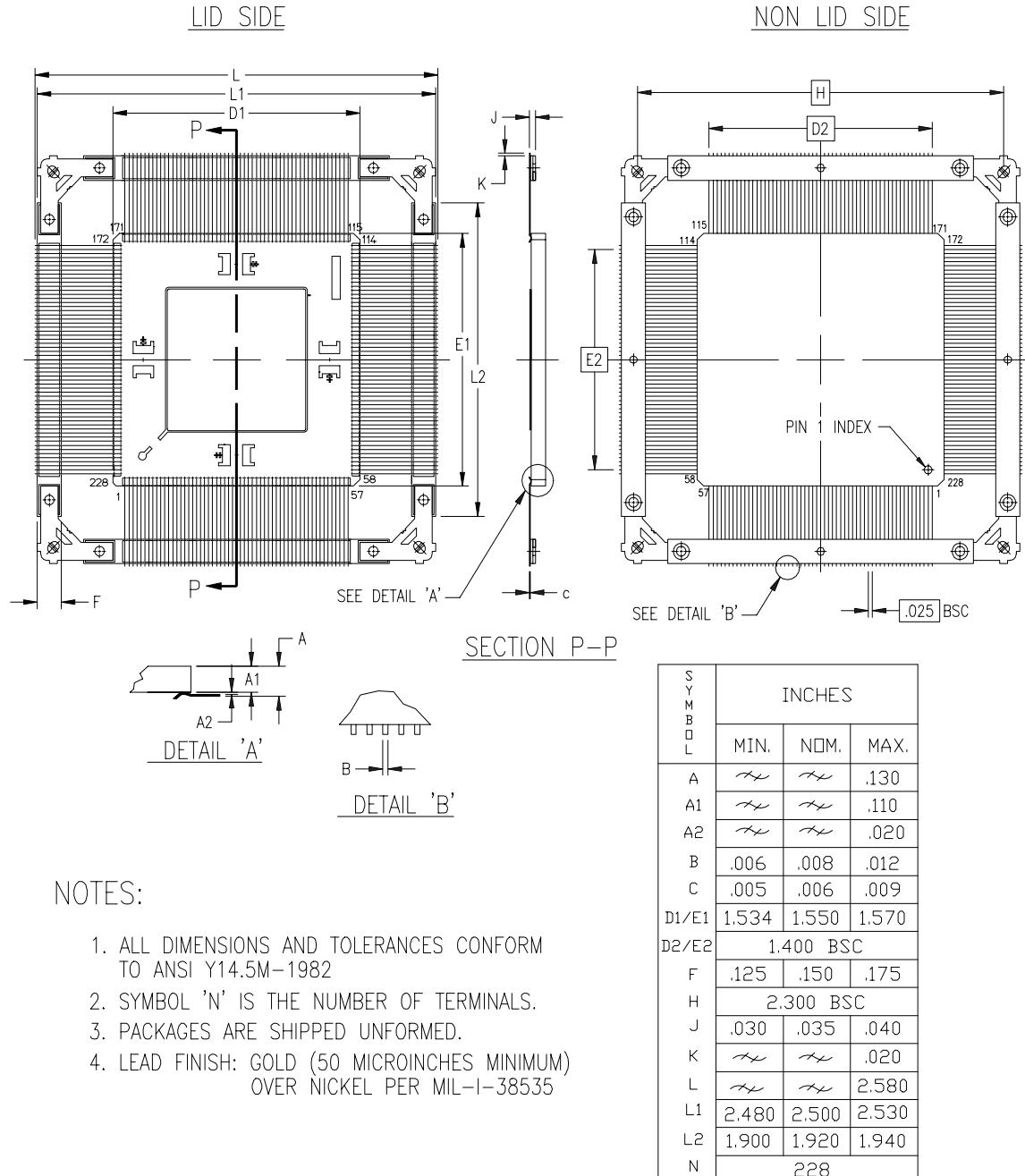
CB100			CB164			CB196			
SYMBOL	INCHES		INCHES		INCHES		INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.130		.135	.130		.130	.130		.130
A1	.115			.110			.081	.090	.105
A2	.020			.020			.020		.020
B	.006	.008	.012	.006	.008	.012	.006	.008	.012
C	.005	.006	.009	.005	.006	.009	.005	.006	.009
D1/E1	.740	.750	.765	1.120	1.130	1.145	1.336	1.130	1.364
D2/E2	.600 BSC			1.000 BSC			1.200 BSC		
F	.425	.450	.475	.175	.200	.225	.175	.200	.225
H	2.300 BSC			2.300 BSC			2.300 BSC		
J	.030	.035	.040	.030	.035	.040	.030	.035	.040
K	.020			.020			.020		
L	.2580			.2580			.2580		
L1	2.490	2.500	2.510	2.485	2.500	2.505	2.470	2.500	2.530
L2	1.480	1.500	1.520	1.480	1.500	1.520	1.700	1.720	1.740
N	100			164			196		

### NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982
2. SYMBOL 'N' IS THE NUMBER OF TERMINALS.
3. PACKAGES ARE SHIPPED UNFORMED.
4. LEAD FINISH: GOLD (50 MICROINCHES MINIMUM)  
OVER NICKEL PER MIL-I-38535

100, 164, 196-PIN CERAMIC BRAZED CQFP (CB100, 164, 196)  
(XC4000 VERSION)

## Ceramic Brazed QFP Packages - CB228



228-PIN CERAMIC BRAZED CQFP (CB228)

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November 21, 1997 (Version 2.0)

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## Quality Assurance Program

All aspects of the Quality Assurance Program at Xilinx have been designed to eliminate the root cause of defects, rather than to try to remove them by inspection. A quality system was put in place which is in full compliance with the requirements of ISO9002. Xilinx was found to be in full compliance of the requirements of ISO9002:1994 by an independent auditor in October, 1995. At that time Xilinx was registered for "the manufacturing and testing of programmable logic devices". Last November, Xilinx was audited by DSCC and found in full compliance with the requirements of MIL 38535 for a QML supplier. In January 1997 Xilinx was formally granted transitional QML approval by DSCC.

The aspects of ISO compliance in place at Xilinx include the following seventeen points:

- **Management Review:** a comprehensive system of management attention and direction for all aspects of company performance that directly affect our customers. These include (among others) Xilinx performance in the areas of Quality, Reliability and On-Time Delivery. Management assures that this quality policy is understood, implemented and maintained at all levels in the organization.
- **Quality Systems:** are in place to ensure that product conforms to customer specifications. These systems facilitate, measure and continuously improve Xilinx performance in those areas that affect customer satisfaction. Xilinx remains committed to achieving 100% customer satisfaction.
- **Contract Review:** is conducted to ensure each contract adequately defines and documents requirements, that differences between customer and Xilinx standard specifications are mutually satisfactorily resolved, and that Xilinx has the capability to meet contract requirements.
- **Document Control:** procedures are established and maintained to control all documents and data that relate to the performance of Xilinx business and processing requirements. All organizations who need access to such documentation during the performance of their functions are assured availability of the latest, controlled versions of that documentation.
- **Purchasing:** procedures are in place to ensure that all purchased products conform to the specified requirements. As Xilinx is a "fabless" manufacturing company, special attention is paid to our subcontract partners. They are required to demonstrate the type of control and capabilities that our customers require. All key Xilinx subcontract partners are ISO certified.
- **Product Identification & Traceability:** is maintained throughout the manufacturing process. Traceability back to the starting materials is available through unique product identification techniques and markings throughout the manufacturing process.
- **Process Control:** is assured by identifying and controlling those processes that directly affect the quality of our products, whether those processes are performed directly by Xilinx, or by our subcontract partners.
- **Inspection & Test:** is performed to ensure that incoming product is not used or processed until it has been verified as conforming to required specifications. This inspection is done jointly by Xilinx and by its subcontract partners.
- **Inspection, Measuring and Test Equipment:** is calibrated in conformance with the requirements of Mil Ref 45662 and/or other international standards. Equipment is maintained in such a manner to ensure that measurement uncertainty is known and is consistent with specification requirements.
- **Inspection & Test Status:** of product is uniquely identified throughout the manufacturing process both at Xilinx and at our subcontract partners. Records are kept to identify the authority responsible for the release of conforming production.
- **Control of Non-Conforming Product:** is assured through disposition procedures that are defined in such a manner as to prevent the shipping of non-conforming products. The responsibility and authority for the disposition of such products are well defined.
- **Corrective Action:** processes are documented and implemented to prevent the recurrence of nonconforming product. These processes are the key to implementing the Xilinx strategy of eliminating the root causes of nonconformity, rather than to apply inspection to try to remove nonconformity.
- **Handling, Storage, Packing & Delivery:** procedures are defined and implemented to prevent damage or deterioration of product once the manufacturing process is complete.
- **Quality Records:** procedures are established and maintained for the identification, collection, indexing, filing, storage, maintenance and disposition of quality records.
- **Internal Quality Audits:** are carried out to verify whether quality activities comply with planned

- arrangements and to determine the effectiveness of the quality system. These audits are regularly supplemented by quality audits performed by our customers, and by our independent ISO auditors.
- **Training:** procedures have been established and are maintained to identify the training needs of all personnel affecting quality during the production of Xilinx products. Personnel performing such activities are qualified based upon appropriate education, training and/or experience.
  - **Statistical Techniques:** are in place at Xilinx and at our subcontract partners for verifying the acceptability of process capabilities and product characteristics.

These key requirements are in place at Xilinx and at our subcontract partners to ensure our ability to achieve customer satisfaction through the **on-time delivery of quality products that meet customer requirements** and are **reliable**.

## Device Reliability

Device reliability is often expressed in a measurement called *Failures in Time* (FITs). In this measure one FIT equals one failure per billion ( $10^9$ ) device operating hours. A failure rate in FITS must include the operating temperature to be meaningful. Hence failure rates are often expressed in FITS at 70°C (or some other temperature in excess of the application).

Since one billion hours is well in excess of 100,000 years, the FIT rate of modern ICs can only be measured by accelerating the failure rate by testing at a higher junction temperature (usually 125°C or 145°C). Extensive testing of Xilinx devices (performed on actual production devices taken directly from finished goods) has been accomplished continuously since 1989 and reported quarterly. Quarterly reports on the reliability of Xilinx products are available through your Xilinx sales representative and at the WebLINX web site ([www.xilinx.com](http://www.xilinx.com)). During the last two years, over 20,000 devices have accumulated a total of over 36,000,000 hours of both static and dynamic operation

at 125°C (equivalent) to yield the FIT rates shown in Figure 1.

## Description of Tests

### Die Qualification

1. **High Temperature Life:** This test is performed to evaluate the long-term reliability and life characteristics of the die. It is defined by the Military Standard from which it is derived as a "Die-Related Test" and is contained in the Group C Quality Conformance Tests. Because of the acceleration factor induced by higher temperatures, (typically 125°C and/or 145°C) data representing a large number of equivalent hours at a normal temperature of 25°C can be accumulated in a reasonable period of time.
2. **Biased Moisture Life:** This test is performed to evaluate the reliability of the die under conditions of long-term exposure to severe, high-moisture environments that could cause corrosion. Although it clearly stresses the package as well, this test is typically grouped under the die-related tests. The device is operated at maximum-rated voltage, 5.5 Vdc, and is exposed to a temperature of 85°C and a relative humidity of 85% throughout the test.

### Package Integrity and Assembly Qualification

1. **Unbiased Pressure Pot:** This test is performed at a temperature of 121°C and a pressure of 2 atm of saturated steam to evaluate the ability of the plastic encapsulating material to resist water vapor. Moisture penetrating the package could induce corrosion of the bonding wires and nonglassivated metal areas of the die (bonding pads only for FPGA devices). Under extreme conditions, moisture could cause drive-in and corrosion under the glassivation. Although it is difficult to correlate this test to actual field conditions, it provides a well-established method for relative comparison of plastic

### Xilinx Historical Reliability

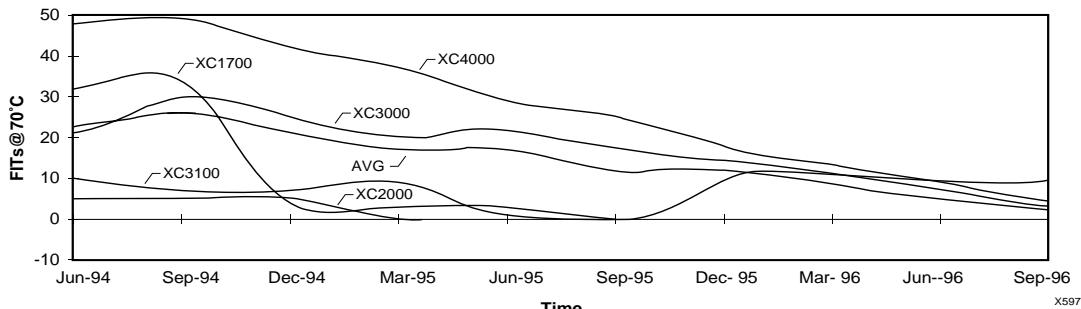


Figure 1: Failure Rates in FITs

- packaging materials and assembly and molding techniques.
2. **Thermal Shock:** This test is performed to evaluate the resistance of the package to cracking and resistance of the bonding wires and lead frame to separation or damage. It involves nearly instantaneous change in temperature from -65°C to +150°C (condition "C").
  3. **Temperature Cycling:** This test is performed to evaluate the long-term resistance of the package to damage from alternating exposure to temperature extremes. The range of temperatures is -65°C to +150°C (condition "C"). The transition time is longer than that in the Thermal Shock test but the test is conducted for many more cycles.
  4. **Salt Atmosphere:** This test was originally designed by the US Navy to evaluate resistance of military-grade ship-board electronics to corrosion from sea water. It is used more generally for non-hermetic industrial and commercial products as a test of corrosion resistance of the package marking and finish.
  5. **Resistance to Solvents:** This test is performed to evaluate the integrity of the package marking during exposure to a variety of solvents. This is an especially important test, since an increasing number of board-level assemblies are subjected to severe conditions of automated cleaning before system assembly. This test is performed according to the methods specified by MIL-STD-883.
  6. **Solderability:** This test is performed to evaluate the solderability of the leads under conditions of low soldering temperature following exposure to the aging effects of water vapor.
  7. **Lead Fatigue:** This test is performed to evaluate the resistance of the completed assembly to vibrations during storage, shipping, and operation.

## Testing Facilities

Xilinx has complete capability to perform High Temperature Life Testing, Thermal Shock, Temperature Cycling, Biased Moisture Life Test, Unbiased Pressure Pot, Solderability and Hermeticity, as well as complete Failure Analysis in house. [Table 1](#) and [Table 2](#) show typical qualification requirements for new and/or changed process flows. [Table 3](#) is a list of current failure analysis capabilities. These laboratories are dedicated exclusively to increasing customer satisfaction through continuous improvements in our processes and technologies.

**Table 1: Plastic Package/Product Qualification Requirements**

Test Seq	Test Description (note 1)								New Assy Techniques (Mat'l/Process/Method)						New Device Mask (note6)	New Fab Proc	Full Qual
		Acc# S.Size (note 2)	New Assy Plant	New Pkg Type I (note3)	New Pkg Type II (note4)	New Pkg Type III LF Design (note5)	Lead Frame	Die Attach	Die Coat	Wire Bond	Mold CLP	Lead Finish					
B1	* Phy. Dimension	0/5	X	X	X									X			X
B2	* Resist. to Solvents	0/3	X										X	X			X
B3	* Solderability Test (note 7)	0/5	X				X						X				X
B4	Solder Heat Test (Optn'l)	0/15				X	X						X				X
B5	Auto Clave (SPP)(Optn'l) 0/76	0/76	X	X	X	X	X		X		X		X				X
B6	* Ball Shear/Bond Pull (note 7)	0/5	X	X					X	X	X			X	X	X	X
B7	** X-Ray (note 7)	0/5	X	X	X	X			X	X	X			X			X
B8	* S.A.T/Dye Pen Test (note 7)	0/10	X	X	X	X	X						X	X			X
B9	* Adhesion of L/Finish (Optn'l)	0/3	X				X							X			X
B10	* External Visual (note 7)	0/25	X	X	X	X	X						X				X
B11	Internal Visual (note 7)	0/5	X	X	X		X	X	X	X				X	X	X	
B12	* Die Shear (note 7)	0/5	X					X						X	X	X	
B13	Flammability Test (note 7)	Per lot											X				X
C1-A	High Temp Life Test	0/76							X					X	X	X	
C1-B	Low Temp Life Test (note 7)	0/22												X	X	X	
C2	C2-A:HAST (0/22) or C2-B: 85/85	0/76	X	X		X	X	X	X				X			X	X
C3	ESD (HBM)	0/3												X	X	X	
C4	High Temp Storage (Optn'l)	0/77											X		X	X	X
D1	* Lead Integrity	0/3	X	X	X									X			X
D2	Thermal Shock (Optn'l)	0/76															X
D3	Temp Cycle	0/76	X	X	X	X	X	X	X	X	X	X			X	X	
E1	Electrical Test & Data Log	0/30													X	X	X
E2	Electrical Characterization	0/30												X	X	X	
E3	T.D.D.B (note 7)	—												X	X	X	
E4	Latch-up	0/9												X	X	X	
E5	Electromigration (note 7)	—												X	X	X	
E6	Photosensitivity (Optn'l)	0/11												X	X	X	
E7	Data Retention Bake EPLD & EPR	0/22												X	X	X	
E8	Input/Output Capacitance	0/5												X	X	X	
E9	Power Cycling (Optn'l)	0/22												X	X	X	
Qty required per lot	E.Good	239	238	162	248	248	157	314	86	325	0	393	464	636			
	E.Reject	63	48	43	35	43	5	5	5	43	29	10	10	64			
	Total	302	286	205	283	291	162	319	91	368	29	403	474	700			

- Notes:
- 1) Test method and stress conditions available upon request.
  - 2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
  - 3) Any new package which has not been qualified in the qualified assembly facility.
  - 4) Any new package where the same body size with different lead pitch has been qualified.
  - 5) New leadframe design whereby the paddle size is larger than the existing leadframe paddle size used in the same qualified package.
  - 6) For new mask from same device family, only high temp life test, ESD, Latch & Capacitance are required.
  - 7) In-process monitor data may be used to satisfy this requirement.
  - \*) Electrical rejects can be used as test sample.
  - \*\*) This is a non-destructive test, sample can be re-used.

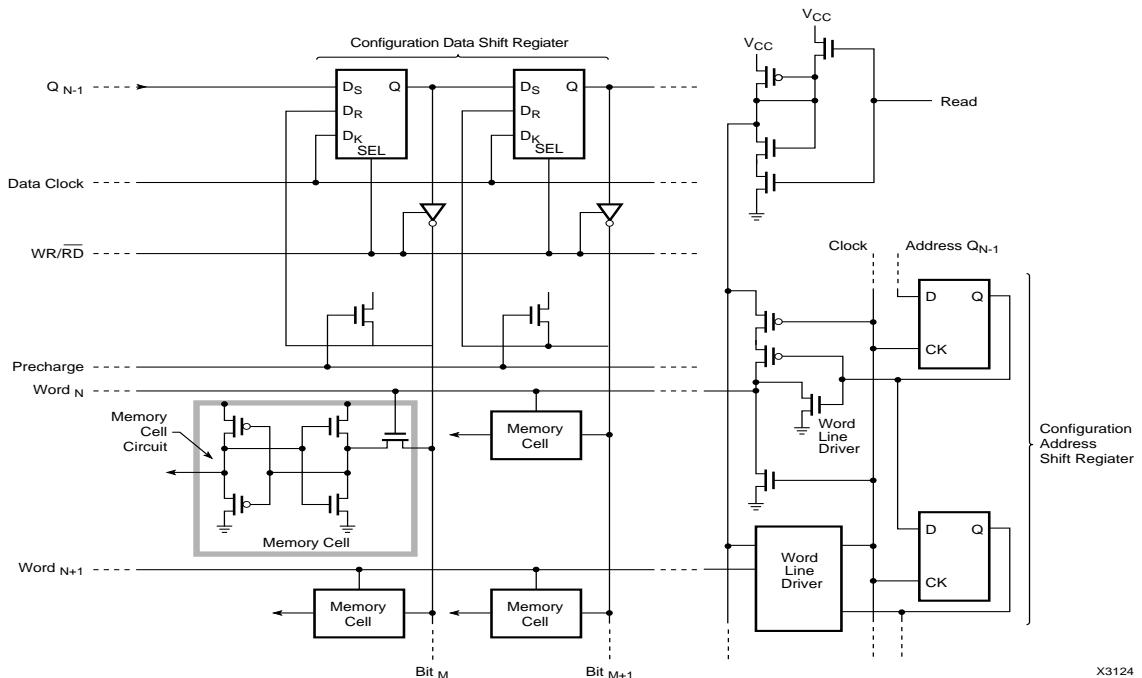
**Table 2: Hermetic Package/Product Qualification Requirements (Commercial)**

Test Seq	Test Description (note 1)	New Assy Techniques (Mat'l/Process/Method)											New Cavity Size (note6)	New Device (note6)	New Fab Proc	Full Qual
		Acc# S.Size (note 2)	New Assy Plant	New Pkg Family (note3)	New Pkg Qual Family (note4)	Lead Frame	Die Attach	Die Coat	Wire Bond	Type of Seal	Lead Finish					
B1	Solder Heat Test (Optn'l)	0/15	X	X						X		X				X
B2	* Resist. to Solvents (note 7)	0/3	X	X								X				X
B3	* Solderability Test (note 7)	0/3	X	X		X						X				X
B4	* Die Shear/Stud Pull (note 7)	0/5	X	X	X		X							X	X	X
B5	* Bond Pull (note 7)	0/2	X	X	X	X		X	X				X	X	X	X
B6	* External Visual (note 7)	0/25	X	X	X	X			X			X				X
B7	Internal Visual (note 7)	0/5	X	X	X	X	X	X	X				X	X	X	X
C1-A	High Temp Life Test	0/76	X	X				X	X				X	X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X	X
C2	High Temp Storage (Optn'l)	0/77						X					X	X	X	X
C3	ESD (HBM)	0/3											X	X	X	X
D1	* Phy. Dimension	0/15	X	X	X							X	X		X	X
D2	* Lead Integrity	0/3	X	X	X	X						X			X	X
D3	Thermal Shock + Temp Cycl + Moisture Resistance	0/32	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D4	Mech. Shock + Vibration + Constant Acceleration	0/32	X	X	X	X	X		X	X			X	X	X	X
D5	* Salt Atmosphere	0/15	X	X	X							X			X	X
D6	* Internal Vapor Content (note 7)	0/3	X	X	X		X	X		X			X		X	X
D7	* Adhesion of L/Finish (Optn'l)	0/2	X	X	X	X						X			X	X
D8	* Lid Torque	0/5	X	X	X					X			X		X	X
D9	Temp Cycle	0/45	X	X	X		X	X	X	X			X	X	X	X
E1	Electrical Test & Data Log	0/30											X	X	X	X
E2	Electrical Characterization	0/30											X	X	X	X
E3	T.D.D.B (note 7)	—											X	X	X	X
E4	Latch-up	0/9											X	X	X	X
E5	Electromigration (note 7)	—											X	X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X	X
E7	Data Retention Bake	0/22											X	X	X	X
E8	Input/Output Capacitance	0/5											X	X	X	X
Qty required per lot		E.Good	190	205	129	69	114	235	190	124	32	124	399	399	414	
		E.Reject	81	81	75	50	8	5	2	33	41	48	7	50	81	
		Total	271	286	204	119	122	240	192	157	73	172	406	449	495	

- Notes:
- 1) Test method and stress conditions available upon request.
  - 2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
  - 3) Package Family - A set of package type with the same package, material, Package construction techniques, terminal pitch, lead shape, row spacing and with identical package assembly tech.
  - 4) Package Type - A package with a unique case outline, configuration, material, piece parts and assembly process.
  - 5) Application to new piece parts or leadframe where cavity size is larger than the largest cavity size for the same package.
  - 6) For new mask from same device family, only high temp life test, ESP, Latch & Capacitance are required.
  - 7) In-process monitor data may be used to satisfy this requirement, for Qual data, data from Assy. lot traveler maybe used.
  - \*) Electrical rejects can be used as test samples

**Table 3: Failure Analysis Equipment List**

Item	Equipment	Vendor	Model Number	Item	Equipment	Vendor	Model Number
1	Scanning Electron Microscope	JEOL	JMS-6401F	17	Die-Shear Tester	KELLER	see #7
2	Gold Sputter (SEM Sample Prep)	ANATECH	Hummer VIII	18	Steam Aging System	Robotic Systems	ST2D
3	Energy Dispersive X-Ray	OXFORD INST.	LINK ISIS-L200C	19	Solder Wave/Pot	Robotic Systems	RPS-202
4	F.I.B. - Focused Ion Beam Workstation	F.E.I.	FIB-600	20	Lead Fatigue Tester	B & G	004-012-00
5	Real-Time X-Ray Imaging System	FEIN FOCUS	FXS-100.10	21	Conventional Oven (C.D.A.)	BID Services	
6	Scanning Acoustic Microscopy	Sonix	Micro-Scan 4HF-200	22	Drill-bit to open MQUADS + Decapping vise		
7	Ball Shear Strength Tester	KELLER	MBS-200	23	Color Printer	Tektronic	Tektronic Phaser IISD
8	XRF Lead Finish/Composition Measurement System	Twin City, Inc.	XRF-5500	24	Stud Pull Tester	B & G	003-010-00
9	Liquid Crystal Hot Spot Detection System/Kit, with 3 temp.	Technology Associates	P/N 4330	25	Work Benches		
10	Emission Microscope for Multilayer Inspection (EMMI)	Hypervision	Visionary 2000	26	Cabinets		
11	Curve Tracer	BID Services		27	Facilities (Lab Area and Equipment Installation Costs)		
12	Metallurgical High Power Microscope	Scientific Instrument Company	see quote (various)	28	Tool Maker Microscope		
13	Stereozoom Low Power Microscope - video camera + monitor	Scientific Instrument Company	see quote (various)	29	Flowhood & Rinse Station		
14	Micro-Etcher System	TM Associates		30	Precision X-Sectioning Equipment		
15	Viseco Camera Interface with High Power Microscope	Computer Modules		31	Plasma Etcher	March Instruments	CS-1701
16	Hermeticity Test System - Fine Leak - Gross Leak	BID Services	-Trio-tech 486 - Veeco MS-170	32	E-Beam IDS-3000		



**Figure 2:** Configuration Memory Cell

## Data Integrity

### Memory Cell Design in the FPGA Device

An important aspect of SRAM-based FPGA device reliability is the robustness of the static memory cells used to store the configuration program.

The basic cell is a single-ended 5-transistor memory element (Figure 2). By eliminating a sixth transistor, which would have been used as a pass transistor for the complementary bit line, a higher circuit density is achieved. During normal operation, the outputs of these cells are fixed, since they determine the user configuration. Write and readback times, which have no relation to the device performance during normal operation, will be slower without the extra transistor. In return, the user receives more functionality per unit area.

This explains the basic cell, but how is the FPGA user assured of high data integrity in a noisy environment? Consider three different situations: normal operation, a Write operation and a Read operation. In the normal operation, the data in the basic memory element is not changed. Since the two circularly linked inverters that hold the data

are physically adjacent, supply transients result in only small relative differences in voltages. Each inverter is truly a complementary pair of transistors. Therefore, whether the output is High or Low, a low-impedance path exists to the supply rail, resulting in extremely high noise immunity. Power supply or ground transients of several volts have no effect on stored data.

The transistor driving the bit line has been carefully designed so that whenever the data to be written is opposite the data stored, it can easily override the output of the feedback inverter. The reliability of the Write operation is guaranteed within the tolerances of the manufacturing process.

In the Read mode, the bit line, which has a significant amount of parasitic capacitance, is precharged to a logic one. The pass transistor is then enabled by driving the word line High. If the stored value is a zero, the line is then discharged to ground. Reliable reading of the memory cell is achieved by reducing the word line High level during reading to a level that insures that the cell will not be disturbed.

## Electrostatic Discharge

Electrostatic-discharge (ESD) protection for each pad is provided by circuitry that uses distributed transistors and/or diodes, represented by the circles in Figure 3. In older devices, these protection circuits are conventional diffused structures. In newer designs, Xilinx utilizes proprietary device structures which exhibit substantially enhanced ESD performance (see Table 4).

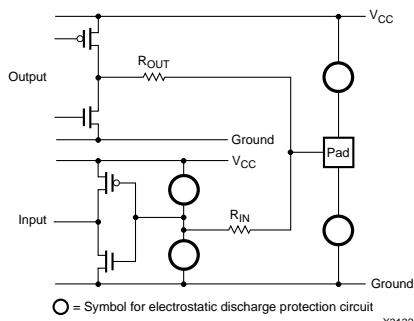


Figure 3: Input/Output Protection Circuitry

Table 4: ESD Performance of Xilinx Components

Circuit Family	Human Body Model	Machine Model	Charged Device
Method 3015	EIAJ 20	Model CDM	
XC1700D	>6,000v	500– 900v	>2,000v
XC2000	1,500–2,500v	250–325v	pend
XC3000A	4,500–7,000v	325–600v	>2,000v
XC3100A	1,750–5,000v	700–800v	>2,000v
XC4000	4,000–8,000v	800–900v	>1,000v
XC4000E	4,000–8,000v	pend	>2,000v
XC4000E	4,000–6,000v	pend	>2,000v
XC5200	3,000–5,000v	pend	>2,000v
XC7000	2,000–4,000v	250–300v	>2,000v
XC9000	2,000–5,000v	pend	>2,000v

Whenever the voltage on a pad approaches a dangerous level, current flows through the protective structures to or from a power supply rail ( $V_{CC}$  or ground). In addition, the capacitances in these structures integrate the pulse to provide sufficient time for the protection networks to clamp the input, avoiding damage to the circuit being protected. Geometries and doping levels are chosen to provide ESD protection on all pads for both positive and negative voltages.

## Latchup

Latchup is a condition in which parasitic bipolar transistors form a positive feedback loop (Figure 4), which quickly reaches current levels that permanently damage the device. Xilinx uses techniques based on doping levels and circuit placement to avoid this phenomenon. The beta of each parasitic transistor is minimized by increasing the base width. This is achieved with large physical spacings. The butting contacts effectively short the n+ and p+ regions for both wells, which makes the  $V_{BE}$  of each parasitic very close to zero. This also makes the parasitic transistors very hard to forward bias. Finally, each well is surrounded by a dummy collector, which forces the  $V_{CE}$  of each parasitic almost to zero and creates a structure in which the base width of each parasitic is large, thus making latchup extremely difficult to induce.

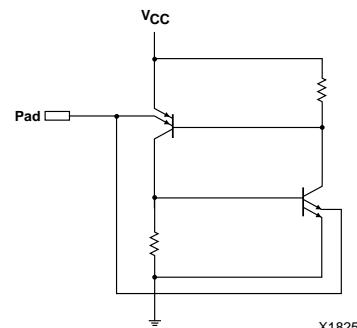


Figure 4: SCR Model

At elevated temperatures, 100 mA will not cause latchup. At room temperature, the FPGA can withstand more than 300 mA without latchup; the EPLD device can withstand more than 200 mA without latchup. However, to avoid metal-migration problems, continuous currents in excess of 10 mA are not recommended.

## High Temperature Performance

Although Xilinx guarantees parts to perform only within the specifications of the data sheet, extensive high temperature life testing has been done at 145°C with excellent results.

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A complete and uniquely accessible offering of worldwide technical support services is available to Xilinx users.

Xilinx Field Application Engineers, located at sales offices and technical support centers worldwide, provide local engineering support, including design evaluation of new projects, close consultation throughout the design process, special training assignments, and new product presentations. Because their role as advisors and troubleshooters keeps them constantly on the go, they are best used not for general questions, but for more targeted queries such as those related to architectural recommendations. The worldwide network of Xilinx sales representatives and distributors also provide local technical support for Xilinx users.

Technical and applications queries can be directed to WebLINX, the Xilinx world wide web site, or the telephone "hotlines". Xilinx provides 24-hour access to the expert Answers database, product and applications information, and a variety of files and utilities via WebLINX and the file download areas. Hotline telephone support provides access to permanent teams of expert Application Engineers located in the United States, United Kingdom, France, Germany, and Japan. These engineers can handle

problems and answer questions right on the spot, and are contributors to, as well as, users of the *Answers* database, accessible at WebLINX ([www.xilinx.com](http://www.xilinx.com)).

Many different publications assist users in completing designs quickly and efficiently, including technical manuals, data sheets, application notes, the AppLINX CD-ROM (a regularly-updated collection of the latest application notes and design hints), and the quarterly XCell newsletter. Most of these publications are available on the WebLINX web site.

For more in-depth support and instruction, a dedicated training organization conducts technical training classes worldwide. Courses geared for both novice and experienced users are available.

The following Technical Support Services are discussed in more detail in this chapter:

- WebLINX World Wide Web site
- Internet File Download area
- Hotline telephone support
- Technical literature
- Training Courses



The screenshot shows the SmartSearch search interface. At the top, there's a navigation bar with links for "Smart Search", "Agents", "Answers", "Ask Xilinx", and "Index". Below the navigation bar, the title "Search the Industry Sites" is displayed. On the left, there's a "Search for:" input field and a "Powered by Verity" logo. In the center, there are several search parameters:

- "Search Page": "Switch to Xilinx Site Search".
- "Find out": Radio buttons for "Applications" (selected) and "Is Title Only".
- "Show results as": Radio buttons for "Titles and Summaries" (selected) and "Titles Only".
- "Search for": An input field containing the text "Focus Search".
- "Search Tips": A link to search tips.
- "Select Where To Search": A section where users can check boxes to search specific sites like Cadence, Data V/O, Mentor, OrCAD, Synopsis, Symplicity, ViewLogic, and Others. There are also checkboxes for Adaptec, EDA Today Newsletter, EE Times, Electronic News, IEEE Spectrum, Int'l Sys Design, RTC, Test & Measurement World, and various organizations like CSC, PREP, IEEE, EDAC, PCI SIG, DAC, Xilinx, Hamilton, Insight, Marvell, and No Horizons.

WebLINX - The Homepage for Programmable Logic ([www.xilinx.com](http://www.xilinx.com))

## WebLINX Web Site ([www.xilinx.com](http://www.xilinx.com))

WebLINX, the Xilinx World Wide Web site, provides instant access to the latest information, ranging from Product Overviews, Application Notes, and Data Sheets to investor information and employment opportunities. Designed to provide users with quick, easy, and intuitive access to the desired information.

WebLINX holds a wealth of Xilinx information, readily available at your fingertips. What's more, *SmartSearch*, our industry-wide search engine, is the definitive resource for all Programmable Logic information on the web. *SmartSearch* searches over 50 different web sites rich in Programmable Logic content, providing central access to a vast amount of data. *SmartSearch* Agents will watch the Web for you and inform you via e-mail when new or updated information is added to any of the sites served by *SmartSearch*. *SmartSearch* Agents allow you to stay up-to-date in the rapidly changing world of Programmable Logic.

New information is constantly being added to the Xilinx site. The following is a list of some of the technical information now available on WebLINX (as of July, 1997):

- Over 60 Application Notes organized by system type (e.g., PCI, DSP, and PCMCIA), function (e.g., memory functions, arithmetic functions, and busses), component product family, and application.
- Complete and detailed data sheets on all Xilinx products.
- Over 1900 records in our Technical Answers database that contains answers to frequently-asked technical questions.
- Xilinx Product Change Notices and Xilinx Customer Updates
- Access to XCell, our quarterly journal for programmable logic users.
- Software updates and patches.
- Links to technical Xilinx presentations via Marshall Electronics' NetSeminar™ archives.

## Technical and Applications Information

The Answers area of WebLINX provides access to technical and applications information that assists design engineers in solving problems. The Answers area is accessible from the Xilinx home page either through the "Answers" icon or by selecting the "Support" topic. Further, this collection of technical and applications information is immediately accessible through the button bar that is located at the bottom of every Web page.

The Answers area provides access to a variety of technical and applications resources including:

- Over 1900 technical solutions and frequently asked questions.
- The File Download Area for access to patches, utilities, and updates.

- Expert Journals that provide flow-specific collections of information including FAQs, Tips, and Hot Topics.
- Documents and applications material.
- Information about Worldwide Hotline access and training course availability.

## File Access and Transfer

Through the file download areas, users have on-line access to a variety of useful files, including user manuals, automated tutorials, design examples, and utilities. Data files can be exchanged with Application Engineers through a secure area of the file download area.

## Hotline Telephone Support

A network of Technical Support Hotlines provides Xilinx users with direct telephone access to Xilinx Application Engineers dedicated to providing resolutions to problems that may arise during the design process. Xilinx Application Engineers use many of the same resources and databases that are now directly available to users via the WebLINX web site. Technical questions also can be submitted via fax or E-mail.

### All regions of the world (WebLINX):

web site: [www.xilinx.com](http://www.xilinx.com)

### North American support:

Hours:	Mon. - Wed., Fri. 6:30 AM - 5:00 PM
	Thur. 6:30 AM - 4:00 PM Pacific Time
Hotline:	800-255-7778 or 408-879-5199
Fax:	408-879-4442
E-mail:	<a href="mailto:hotline@xilinx.com">hotline@xilinx.com</a>

### United Kingdom support:

Hours:	Mon. - Thur.
	9:00 AM - 12:00 PM, 1:00 PM - 5:30 PM
	Fri.
	9:00 AM - 12:00 PM, 1:00 PM - 3:30 PM
Hotline:	(44) 1932-820821
Fax:	(44) 1932-828522
E-mail:	<a href="mailto:ukhelp@xilinx.com">ukhelp@xilinx.com</a>

### France support:

Hours:	Mon. - Fri.
	9:30 AM - 12:30 PM, 2:00 PM - 5:30 PM
Hotline:	(33) 1-3463-0100
Fax:	(33) 1-3463-0959
E-mail:	<a href="mailto:frhelp@xilinx.com">frhelp@xilinx.com</a>

**Germany support:**

Hours: Mon. - Thur.  
8:00 AM - 12:00 PM, 1:00PM - 5:00 PM  
Fri.  
8:00 AM - 12:00 PM, 1:00 PM - 3:00 PM  
Hotline: (49) 89-93088-130  
Fax: (49) 89-93088-188  
E-mail: dlhelp@xilinx.com

**Japan support:**

Hours: Mon., Tue., Thur., Fri.  
9:00 AM - 5:00 PM  
Wed.  
9:00 AM - 4:00 PM  
Hotline: (81) 3-3297-9163  
Fax: (81) 3-3297-0067  
E-mail: jhotline@xilinx.com

**Korea support:**

Hotline: (82) 2-761-4277  
Fax: (82) 2-761-4278  
E-mail: korea@xilinx.com

**Hong Kong support:**

Hotline: (85) 2-2424-5200  
Fax: (85) 2-2424-7159  
E-mail: hongkong@xilinx.com

## Technical Literature

Xilinx offers many different publications to assist users in completing designs quickly and efficiently. These include technical manuals, Data Books, data sheets, application notes, the AppLNX CD, the XCell newsletter, and The Answers Database. Most of these publications are available on-line at the WebLNX web site.

As part of the development system products, Xilinx provides manuals and supporting documents for the development system tools, libraries, CAE tool interfaces, and related software tools. Many of these manuals are available on the CD that holds the software as well as in hardcopy format. On-line help facilities also are an integral part of the development system products.

## AppLNX

AppLNX is a collection of current application notes and other new technical documentation provided on a CD-ROM for easy reference by the design engineer. All the material on the CD is provided in Adobe Acrobat format for easy viewing and printing. The AppLNX CD is updated regularly as new material becomes available.

**XCell Newsletter**

XCell, the quarterly journal for Xilinx programmable logic users, is dedicated to supplying up-to-date information for system designers. A typical issue includes descriptions of new products, updates on component and software availability and revision levels, application ideas, design hints and techniques, and answers to frequently-asked questions.

To add your name to the XCell subscription list, please send your name, company affiliation, and mailing address to XCell editor, via FAX at 408-879-4676.

## Programmable Logic Training Courses

All users of Xilinx products should attend one of our training courses. Attending a Xilinx training course is one of the fastest and most efficient ways to learn how to design with FPGA devices from Xilinx. Hands-on expert instruction with the latest information and software will allow you to implement your own designs in less time with more effective use of the devices. Not only design engineers, but also test engineers, component engineers, CAD engineers, technicians, and engineering managers may want to attend the course in order to understand the Xilinx products.

A variety of courses are offered to meet your specific needs. Courses are held regularly in centers around the world, and can even be brought to your own facility.

## What You Will Learn

Not only will you learn about our products, but we will recommend the best ways to use the software based on our years of experience with thousands of designs. You will learn how to efficiently enter, implement, and verify your design. You can use the Xilinx automatic mode, or take a power-user approach and guide the automatic tools to the best implementation of your design.

## Prerequisites

Students need only have a background in digital logic design. Basic familiarity with the PC or workstation is helpful, but not required. It will benefit you to learn your design entry tool of choice before attending the Xilinx course.

If you would like to prepare for the training course to maximize your learning, you should complete the tutorials available in the development system.

## Benefits

### ***Start or Complete Your Design During the Training Course***

Bring your design to the course and consult with the instructor. Course size is limited to allow more interaction. You can spend extra time getting your design completed before returning home. Call to see if your design entry tool will be available at the course.

### ***Reduce Your Learning Time***

Extensive Xilinx documentation and tutorials provide the information you need to complete your design. But attending the training course for focused, interactive learning is faster than a question-and-answer approach on your own. Instead of interruptions and piecemeal self-education, you will quickly become your company's expert in Xilinx designs.

### ***Make Fewer Design Iterations***

By learning the proper approach, you will save time and expense in prototyping and debugging designs. However, if you do need to make changes to your design, you will learn how to do this quickly and efficiently.

### ***Get to Market Faster***

Getting your product to market faster is probably one of the key reasons you are using Xilinx products. Studies have shown that time-to-market often has a greater effect on profits than development costs. Training will allow you to get your product to market on schedule, allowing your company to reap the rewards that follow.

### ***Lower Production Costs***

By learning how to use the device effectively, you may be able to get more logic into a smaller device, or operate at a higher speed. As a result, you may be able to save on the cost of the device itself, and the surrounding logic on your board.

### ***Increase Quality***

Effective verification techniques will prove the quality of your Xilinx-based design. Higher quality leads to less main-

tenance and repair costs, and improved customer satisfaction.

## Time and Cost Savings

Attending a Xilinx training course is an investment that will pay for itself with the first Xilinx design that you begin. The courses are fast-paced, each providing as much information as possible in the short time available. Hands-on experiences throughout the courses make sure that the information is retained and applied to practical applications. Just as Xilinx products reduce your development time, attending a training course can reduce your design time. The person attending the course will be an in-house expert who can be utilized by other members of your company.

You can reduce your travel costs by attending a course scheduled in your area, or having the class brought right to your facility. The tuition pays for the course notes and expert, in-person instruction, which can be priceless when trying to meet a schedule.

## Course Descriptions

### ***Hands-On Experience***

Each course includes over two hours each day for hands-on labs. There is at least one computer for every two people in the course.

### ***Platforms***

PC systems using Win95 and NT operational systems.

### ***Instructors***

Xilinx training courses have been successfully held worldwide for over seven years. The instructors are Xilinx experts who are skilled at passing that knowledge on to fellow engineers. A dedicated Education organization at Xilinx works closely with the Applications and Engineering groups to keep the courses up-to-date with the latest improvements to Xilinx and third-party tools.

### ***Course Materials***

All course materials are supplied by Xilinx. The course notes are bound for easy use and include additional reference material beyond what is covered in the course.

Most courses include a full lunch, with morning and afternoon snacks. Let the education registrar know if you have any special dietary needs when registering for a course.

### ***Product Coverage***

Xilinx courses cover the latest released versions of our devices and development systems. New products are added to the class as they become available. If you have any questions on coverage of a particular product, please call Xilinx Customer Education.

## FPGA Tools Course Outline

This Xilinx training course is two and one-half days in length. All North American training sites, and most international locations, teach the same course.

This course is heavily focused on the labs, which feature Xilinx' Foundation Software.

- Introduction
- Basic XC4000X Architecture
- CPLD Design
  - 9500 Architecture/Features
- Design Entry
  - Design Flow
  - Xilinx Libraries/ LogiBLOX Components
- Design Manager
  - Implementing the design
  - Design Flow
- Simulation
  - Xilinx Simulation/Verification
  - LogiBLOX Simulation
- Configuration
  - Options/Methods/Debugging
- FPGA Combinatorial Logic Resources
- Designing for FPGA Registers
- Designing for FPGA Memory
- Designing for FPGA I/O
- Low Cost FPGA Families
- Constraining the Design
  - Location/Implementation
  - Timing
- Flow Engine Overview
  - New Terminology
- Custom Options
  - MAP, PAR, and Timing Report Options
  - Flow Options
  - Advanced Operations

## M1 Update Course

The one day course is focused on the latest released products from Xilinx. An update course is available describing the new features of the M1 release. The course will be offered for a limited time at regional sites, or can be brought to your facility. Those customers who have already attended a Xilinx course or have experience using Xilinx products should consider attending the one-day M1 Update training session. These sessions will be most useful if you have the latest software. Browse the Xilinx Web site for scheduled courses, or contact the Xilinx Education Registrar to hold an Update training session at your site.

## M1 Update Course Outline

- Introduction
- M1 Release
  - Changes
  - Future Updates
- FPGA Architecture
  - Features
  - Size
  - Power
- Tool Usage
  - Design Flow
  - Options
  - Software Strategies
- New Features
  - Checkpoint Verification
  - Constraints
- LogiBLOX
- LogiCORE/AllianceCORE
- Conversion Guidelines

## VHDL Seminar (Esperan-Based)

This one day seminar consists of one-half day of presentation and one-half day of hands-on training using the Foundation tools. The seminar is designed to be an introduction, providing the students with enough training so that they are conversant with the language and can write simple VHDL functions.

This course is presented on an as needed basis. Please contact your local Xilinx or distributor sales office for additional course and schedule information.

**The one-day VHDL seminar includes the following topics:**

- VHDL Application Introduction
- VHDL Language Introduction
- Signals and Data Types
- VHDL Operators
- Concurrent and Sequential Statements
- Writing VHDL for Synthesis

**The lab exercises presented during the one-day VHDL seminar consist of:**

- Familiarization with Xilinx Foundation Series
- Synthesis Tool
- Familiarization with the Decoder Design
- Writing Your First VHDL Code
- Adding the Alarm Signal
- Adding a Seven Segment Display Driver
- The Alarm Register
- A Counter
- The Alarm Clock Controller (a State Machine)

## Future Foundation and Synopsys Courses

With the release of the XACTstep version M1 software, the Xilinx education organization is poised to provide additional training courses to our customers. A Foundation schematic-entry course and a Synopsys synthesis course will be offered in the winter 1997 time period. Customers should call the Xilinx Education Registrar for up-to-date course schedules and locations.

## Training Locations

### Xilinx Headquarters

Courses are held regularly at Xilinx headquarters in San Jose, California. During the class, you may elect to meet one-on-one with Xilinx Applications engineers to discuss specific issues not covered in the course. Topics may include using a specific third-party tool, optimizing your particular design, or more advanced issues beyond the coverage of the course.

### North American Distributor Locations

Xilinx distributors sponsor training courses jointly with Xilinx, using the same material as the headquarters courses. Since the distributor sponsors the course, the tuition cost is often reduced for customers of the sponsoring distributor. Check with the distributor when registering. Locations include over seventy cities across North America. Contact your local distributor or Xilinx headquarters for information on courses in your area.

### International Locations

Xilinx courses are held throughout Europe, Japan, Asia, India, Israel, South Africa, South America, and other international locations. Courses vary in length and tuition, but are based on the same material used in North America. Contact your local Xilinx sales office or representative for information about courses in your area.

## On-Site Courses

Xilinx can bring the training course to your own facility for the greatest convenience to your company. To schedule a training course at your facility and determine pricing, call the Xilinx sales office nearest you, or your local Xilinx sales representative. On-site training courses are popular, so the more advanced notice we have, the better our ability to schedule your course exactly when you want it.

## On-Site Courses Provide Additional Benefits:

### No Travel Costs

On-site Xilinx training courses eliminate travel time and expenses:

- No airfare
- No hotel bills
- No car rental

### Courses Tailored To Your Needs

On-site courses can be tailored to meet the specific needs of your company:

- Convenient course time and location
- Projects of a proprietary nature can be discussed openly
- Students can use their own equipment and begin an actual design right in course

### Costs: North America

Prices start at \$4,500 for a minimum course size of six students. (Prices are subject to change without notice.)

### Costs: International

- Prices vary; contact your local Xilinx sales representative. (prices are subject to change without notice.)

### Included in class fees:

- A Xilinx-certified instructor
- Training materials for each student
- PC for every two students (or if you prefer, the training labs can be performed on your PCs or workstations)

## Registration

### Tuition

Course tuition in North America is \$1,000 per student for the two and one-half day courses at Xilinx headquarters. The distributor-sponsored courses are offered at a reduced rate of \$495 for customers of the sponsoring distributor. Check with the distributor when registering. On-site courses start at \$4,500 per class, and vary according to the course and the number of students. For specific pricing of on-site courses, call the Xilinx Education Registrar or your local sales office. For international locations, call the local registrar for pricing. (Prices and course schedules are subject to change without notice.)

Location		Course Title	Tuition	Benefits
North America	Xilinx Headquarters	FPGA Tools M1 Update	\$1,000 \$99	<ul style="list-style-type: none"> <li>• Can meet with applications engineers</li> <li>• Courses held frequently</li> <li>• All class types available</li> </ul>
	Xilinx Sales Office	VHDL Course	\$99	<ul style="list-style-type: none"> <li>• One-day introduction to VHDL</li> </ul>
	Distributor Locations	FPGA Tools M1 Update	\$495 \$99	<ul style="list-style-type: none"> <li>• Courses held frequently; locally available</li> <li>• Lower cost for Distributor's customers</li> <li>• One-day focus on M1 software release</li> </ul>
	On-Site		Starts at \$4,500	<ul style="list-style-type: none"> <li>• Convenience; focus on specific issues</li> </ul>
International	International Locations		Varies	<ul style="list-style-type: none"> <li>• Offered in over 21 countries</li> <li>• Native language</li> </ul>
	On-Site		Varies	<ul style="list-style-type: none"> <li>• Convenience</li> <li>• Can focus on specific issues</li> </ul>

## Money-back Guarantee

We are so confident you will be satisfied with the benefits of a Xilinx training course that we offer the following guarantee:

Full refund of the course cost if you are not completely satisfied.

## Enrollment

To enroll in a Xilinx training course, several enrollment methods are available. The fastest and easiest enrollment mechanism is the on-line registration via the Xilinx web site at "www.xilinx.com". An alternate method for enrollment is to contact the registrar at the course location, or for Xilinx headquarters courses, call (408) 879-5090 or FAX (408) 879-4676 the Education Registrar for additional course information.

Course size is limited, so early enrollment is recommended. **Students are considered enrolled only after a check, money order, or purchase order for the course tuition has been received.** Please mail your payment to the registrar of the location of your training class. For Xilinx-sponsored courses, make checks/P.O. payable to Xilinx, Inc.

Enrollments will be acknowledged with a confirmation letter. We encourage you to sign up early, as courses may fill up quickly.

## Cancellations

Course tuition is fully refundable up to two weeks before the scheduled course starts. Cancellations within two weeks of the scheduled course will incur a 25% cancellation fee. Cancellations within one week of the scheduled course date may only be applied toward a future course date. Rescheduling is allowed until three working days before the start of class. Student substitutions may be made at any time.

## Xilinx Customer Education Registrar

Customer Education Registrar  
 Xilinx, Inc.  
 2100 Logic Drive  
 San Jose, CA 95124  
 Phone: (408) 879-5090  
 Fax: (408) 879-4676,  
 - attn: Customer Education Registrar  
 E-mail: customer.training@xilinx.com  
 Register on-line: <http://www.xilinx.com>



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## Introduction

In the Spartan™, XC3000, XC4000, and XC5200 device families, Xilinx offers several evolutionary and compatible generations of Field Programmable Gate Arrays (FPGAs). Here is a short description of their common features.

Every Xilinx FPGA performs the function of a custom LSI circuit, such as a gate array, but the FPGA is user-programmable and even reprogrammable in the system. Xilinx sells standard off-the-shelf devices in multiple families, and many different sizes, speeds, operating-temperature ranges, and packages. The user selects the appropriate device and then converts the schematic or High-Level-Language description into a configuration data file, using the Xilinx development system software running on a PC or workstation, and then loads this file into the Xilinx FPGA.

This overview describes two aspects of Xilinx FPGAs:

- what logic resources are available to the user
- how the devices are programmed.

## User Logic

Different in structure from traditional logic circuits, or PALs, EPLDs and even gate arrays, the Xilinx FPGAs implement combinatorial logic in small look-up tables (16 x 1 ROMs); each such table either feeds the D-input of a flip-flop or drives other logic or I/O. Each FPGA contains a matrix of identical logic blocks, usually square, from 8 x 8 in the XC4002XL to 68 x 68 in the XC40125XV. Metal lines of various lengths run horizontally and vertically in-between these logic blocks, selectively interconnecting them or connecting them to the input/output blocks.

## Logic Blocks

This modular architecture is rich in registers and powerful function generators that can implement any function of up to five variables. For wider inputs, function generators are easily concatenated. Generous on-chip buffering makes logic block delays insensitive to loading by the interconnect structure, but interconnect delays are layout-dependent and must be analyzed if they are performance-critical.

## Clocks

Clock lines are well-buffered and can drive all flip-flops with < 2 ns skew from chip corner to corner, even throughout the biggest device. The user need not worry about clock loading or clock-delay balancing, or about hold-time issues on the chip, if the designated global clock lines are used.

## Xilinx FPGAs: A Technical Overview for the First-Time User

Application Note by Peter Alfke

There are eight such global low-skew clock lines in XC4000 and Spartan devices, four in XC5200 devices, and two in XC3000 devices.

## Special Features

All devices can implement internal bidirectional busses. The Spartan, XC4000- and XC5200-family devices have dedicated fast carry circuits that improve the efficiency and speed of adders, subtractors, comparators, accumulators and synchronous counters. These families also support boundary scan on every pin.

Spartan and XC4000-series devices can use any of their logic-block look-up tables as distributed RAM, with synchronous write and dual-port options. This makes FIFOs, shift registers and DSP distributed multipliers very fast and efficient.

## Inputs/Outputs

All device pins are available as bidirectional user I/O, with the exception of the supply connections and a few dedicated configuration pins. All inputs and outputs within each family have identical electrical characteristics, but output current capability varies among families. The outputs on XC3000 and XC5200 devices always swing rail-to-rail. Spartan and XC4000E/EX outputs have a global choice between "TTL = totem pole" or "CMOS = rail-to-rail" output swing.

The original families operate from a 5-V supply, but have added 3.3-V variants. These 3.3-V devices, designated by an "L" in their product name, have rail-to-rail outputs.

Inputs of all 5-V devices can be globally configured for either TTL-like input thresholds or mid-rail CMOS thresholds. All 3.3-V devices have CMOS input thresholds (50% of Vcc). All inputs have hysteresis (Schmitt-trigger action) of 100 to 200 mV. SpartanXL and XC4000XL inputs are unconditionally 5-V tolerant, even while their supply voltage is as low as 0 V. This eliminates all power-supply sequencing problems.

## Global Reset

All Xilinx FPGAs have a global asynchronous reset input affecting all device flip-flops. In the Spartan, XC4000- and XC5200-family devices, any pin can be configured as a reset input; in XC3000-families, RESET is a dedicated pin.

## Power Consumption

Since all Xilinx FPGAs use CMOS-SRAM technology, their quiescent or stand-by power consumption is very low, micro-watts for XC3000 devices, max 25 mW to 75 mW for the other 5-V families. The operational power consumption is totally dynamic, proportional to the transition frequency of inputs, outputs, and internal nodes. Typical power consumption is between 100 mW and 5 W, depending on device size, clock rate, and the internal logic structure.

All devices monitor  $V_{CC}$  continuously and shut down when  $V_{CC}$  drops to 3 V (2 V for 3.3-V devices). The device then 3-states all outputs and prepares for reconfiguration.

## Programming or Configuring

### Design Entry

A design usually starts as a schematic, drawn with one of the popular CAE tools, or as a High-Level Language textual description. Most CAE tools have an interface to the Xilinx development system, running on PCs or workstations.

### Design Implementation

After schematic- or HLL design entry, the logic is automatically converted to EDIF. The Xilinx software first partitions the design into logic blocks, then finds a near-optimal placement for each block, and finally selects the interconnect routing. This process of partitioning the logic, placing it on the chip, and routing the interconnects runs automatically, but the user may also affect the outcome by imposing specific timing constraints, or selectively editing critical portions of the design, using the graphic design editor. The user thus has a wide range of choices between a fully automatic implementation and detailed involvement in the layout process. Once the design is complete, a detailed timing report is generated and a serial bitstream can be downloaded into the FPGA, into a PROM programmer, or made available as a computer file.

## Configuring the FPGA

The user then exercises one of several options to load this file into the Xilinx FPGA device, where it is stored in latches, arranged to resemble one long shift register. The data content of these latches customizes the FPGA to perform the intended digital function. The number of configuration bits varies with device type, from 14,819 bits for the smallest device (XC3020) to 2,797,040 bits for the largest device (XC40125XV). Multiple FPGA devices can be daisy-chained and configured with a common concatenated bit-stream. Device utilization does not change the number of configuration bits. Inside the device, these configuration bits control or define the combinatorial circuitry, flip-flops, interconnect structure, and the I/O buffers, as well as their

pull-up or pull-down resistors, input threshold and output slew rate.

### Power-up Sequence

Upon power-up, the device waits for  $V_{CC}$  to reach an acceptable level, then clears the configuration memory, holds all internal flip-flops reset, and 3-states the outputs but activates their weak pull-up resistors. The device then initiates configuration, either as a master, (clocking a serial PROM to receive the serial bitstream or addressing a byte-parallel EPROM), or as a slave, (accepting a clock and bit-serial or 8-bit parallel data from an external source).

### Bit-Serial Configuration

The Xilinx serial PROM is the simplest way to configure the FPGA, using only three or four device pins. Typical configuration time is around one microsecond per bit, but this can be reduced by a factor of eight. Configuration thus takes from a few milliseconds to a several hundred milliseconds. Xilinx serial PROMs come in sizes from 36K to 4M bits. Serial PROMs can also be daisy-chained to store a longer bitstream.

### Byte-Parallel Configuration

Xilinx XC3000, XC4000, and XC5200 FPGA devices can also be configured with byte-wide data, either from an industry-standard PROM or from a microprocessor. The FPGA drives the PROM addresses directly, or it hand-shakes with the microprocessor like a typical peripheral. The byte-wide data is immediately converted into an internal serial bitstream, clocked by the internal Configuration Clock (CCLK). Parallel configuration modes are, therefore, not faster than serial modes.

### Reconfiguration

The user can reconfigure the device at any time by pulling the PROGRAM pin Low, to initiate a new configuration sequence. During this process, outputs not used for configuration are 3-stated. Partial reconfiguration is not possible. For high-volume high-density applications, Xilinx offers lower-cost, fixed-programmed HardWire versions.

### Readback of Configuration Data

After the device has been programmed, the content of the configuration "shift register" can be read back serially, without interfering with device operation. Spartan, XC4000- and XC5200-family devices include a synchronized simultaneous transfer of all user-register information into the configuration registers.

### Quality and Reliability

Since 1985, Xilinx has shipped over 70 million FPGA devices. Industry-leading quality and reliability (ESD protection, AQL and FIT) and aggressive price reductions have undoubtedly contributed to this success.



## Choosing a Xilinx Product Family

XAPP 100 July 10, 1998 (Version 1.3)

Application Note by Peter Alfke

### Summary

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application.

### Xilinx Families

Spartan™, XC3000, XC4000, XC5000, XC9000

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## Introduction

Xilinx offers Field-Programmable Logic circuits, mass-produced standard integrated circuits that the user can customize for the specific application.

Xilinx products offer the following advantages:

- High integration (less space, lower power, higher reliability, lower cost) than solutions based on existing standard devices like MSI and PALs.
- No non-recurring engineering charges and associated risk, typically required for mask-programmed gate array solutions.
- Fast design time and easy design modification, important for early time-to-market.
- Designs can be upgraded in the field for added functionality.

Some potential users might be confused by the wide diversity of Xilinx product offerings. This application note provides a broad overview from the user's perspective.

Xilinx offers programmable logic circuits in two distinctly different technologies.

- SRAM-based FPGAs, the original Xilinx offering, now encompassing the Spartan, XC3000, XC4000, and XC5200 series and their sub-families, like the XC3000A, XC3000L, XC3100A, XC4000E, XC4000EX, and XC4000XL.
- Flash-based complex PLDs, the XC9500 family.

## SRAM-Based FPGAs

These families represent an ongoing evolution of the original Xilinx FPGA architecture, characterized by structural flexibility and an abundance of flip-flops. Logic is implemented in look-up tables, and is interconnected by a hierarchy of metal lines controlled by pass transistors.

Attractive systems features include on-chip bidirectional busses and individual output 3-state and slew-rate control, common reset for all flip-flops, and multiple global low-skew clock networks.

The configuration can be loaded while the devices are connected into a system, and can be changed an unlimited number of times by reloading the "bitstream," the series of bits used to program the device. Configuration must be reloaded whenever Vcc is re-applied. Reconfiguration takes 20 to 200 ms, during which time all outputs are inactive.

Static power consumption is very low, down to microwatts for some of the families. Dynamic power consumption is proportional to the clock frequency, and depends on the logic activity inside the device and on the outputs.

The description "SRAM-based" refers primarily to the standard high-volume manufacturing process, and secondarily to the fact that configuration data is stored in latches. Different from typical SRAMs, these latches use low-impedance active pull-up and pull-down transistors. An on-chip voltage monitor 3-states the outputs and initiates reconfiguration when Vcc drops significantly (to 3.2 V in a 5V system).

These FPGAs are available in different sizes and many different packages. Usually each device type is available in many package types. Any package can accommodate different sized devices with compatible pinouts, so the user can migrate to a larger or smaller device without changing the PC-board layout.

### Overview of SRAM-Based FPGA Families

**XC2000:** Obsolete, do not use for new designs.

The Spartan FPGA families or the XC9500 CPLD family, may be an alternative.

**XC2000L:** 3.3V version of XC2000; obsolete, do not use for new designs. Use the SpartanXL family instead.

**XC3000:** Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible, XC3000A family.

**XC3000A:** Newest version of the XC3000 family

Five device types cover a complexity range from 1,300 to 7,500 gates, with 256 to 928 flip-flops. Logic is implemented in 4-input look-up tables; two tables can be combined to implement any logic function of five variables with only one combinatorial delay of 4 or 5 ns. Flip-flop toggle rate is over 110 MHz.

Global choice of input thresholds (1.2 V or 2.5V), output slew-rate control, and an on-chip crystal oscillator circuit are attractive system features.

- Use for medium-speed, medium-complexity applications.
- Accept lack of dedicated carry circuits, resulting in less efficient and slower arithmetic and counters than in XC4000 families. No on-chip RAM; data storage is thus limited to the available 256 to 928 flip flops.

**XC3000L:** 3.3V version of XC3000A

- Use for battery-operated applications.
- Accept significantly slower speed at 3.3V, compared to XC3000A at 5V.

**XC3100:** Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC3100A family.

**XC3100A:** Newest version of the high-speed XC3100 family.

XC3100A devices are functionally and bitstream identical with the XC3000A, and are available in the same packages

with the same pinouts. The only difference is the higher speed of the XC3100A, with a look-up table delay of 1.5 to 4 ns, and the slightly higher standby current of 8 to 14 mA. One additional high-end family member, the XC3195A, can implement up to 9,000 gates and 1,320 flip-flops.

- Use for high performance design with system clock rates up to 100 MHz.
- Accept lack of dedicated carry circuits, resulting in less efficient and possibly slower arithmetic and counters than in XC4000. No on-chip RAM; data storage is thus limited to the available 256 to 1,320 flip-flops.

**XC3100L:** 3.3V version of XC3100A

- Use for 3.3V applications.
- Accept significantly slower speed at 3.3V, compared to XC3100A at 5V, as well as higher quiescent power and much higher powerdown current than XC3000L at 3.3V.

**XC4000:** Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC4000E family.

**XC4000A:** Superseded

Don't use this family for new designs, since it has been superseded by the improved, faster, less expensive, and pinout-compatible – but not bitstream-compatible – XC4000E family.

**XC4000H:** High I/O - count version of XC4000; obsolete, do not use for new designs.

**XC4000E:** Enhanced superset of the XC4000 family

The XC4000E family is recommended for new designs.

The ten devices in this family stretch from 2,000 to 25,000 logic gate complexity. The emphasis is on systems features and speed. The function generators are more versatile than in the XC3000-Series parts, and there is a dedicated carry network to speed up arithmetic and counters and make them more efficient. Most importantly, the function generators can be used as user RAM with asynchronous or synchronous write addressing, even as dual-port RAMs. This capability makes register files, shift registers and especially FIFOs faster and much more efficient than in any other FPGA. Dedicated carry logic can speed up wide arithmetic and long counters.

- Use for general-purpose logic and data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Use for on-chip distributed RAMs, e.g. >50-MHz FIFOs up to 64 deep, 32 bits wide.

**XC4000EX:** Larger version of the XC4000E family.

Extension of the XC4000E family from 28k to 36k logic gates, with greatly increased routing resources, faster clocking options and more versatile output logic.

- Use for designs beyond 20,000 gate complexity.

**XC4000XL:** 3.3V FPGA

Complete family stretching from 5000 gates to >100,000 gates. Basic features are identical to the XC4000EX but with 5V tolerant input, even when Vcc is <3.0V.

- Use for 3.3V designs, and highest performance.

**XC4000XLT:** 3.3V FPGA, 5V PCI compatible

The XC4000XLT adds 5V VTT pins to the XC4000XL to enable the positive input signal clamping function required by 5V PCI specifications.

**XC4000XV:** 2.5V FPGA

Similar architecture to XC4000EX (5V) and XC4000XL/T (3.3V). Together, these families are referred to as "XC4000X". The XC4000XV extends the family to the largest FPGAs available, in the 250,000-500,000 system gate range. The XC4000XV family uses 0.25 micron technology, with a 2.5V core supply and a 3.3V I/O supply for 5V compatibility.

**Spartan:** 5V low-cost FPGA based on XC4000

The Spartan Series of FPGAs is the best high volume FPGA solution for ASIC replacement. Derived from the highly successful XC4000 architecture and spanning up to 40,000 system gates, the Spartan Series combines high performance, on-chip RAM, software cores, and low prices. The Spartan Series is the first FPGA that meets all the key requirements of ASIC designs for high volume production, and delivers unmatched benefits over competing PLDs.

**SpartanXL™:** 3.3 V version of Spartan FPGA

Similar architecture to 5V Spartan family, but providing higher speed, lower power, and lower cost using smaller process technology. The 5V and 3.3V families are together referred to as the Spartan Series.

**XC5200:** Low-cost FPGA

Architecture optimized for low cost, good routability, and the ability to lock pinout while internal logic is being modified. Dedicated carry structure similar to XC4000, but no RAM. Four-input function generators avoid the XC3000 input constraints. IOBs are less rigidly coupled to the internal matrix

of CLBs and interconnects, which greatly improves the flexibility of pin-locked designs. IOBs have no flip-flops.

Performance is similar to XC3000A, but dedicated carry logic can speed up wide arithmetic and long counters.

- Use for medium-speed general-purpose logic, and for data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Alternative to XC3000A at lower cost, and with additional benefits, such as dedicated carry for arithmetic and counters, improved routing, and ability to cope with locked pinout. High I/O count. Package pinout compatible with XC4000.
- Accept lack of internal RAM.

## FLASH-Based CPLDs (XC9500)

These devices are extensions of the popular PAL architecture, implementing logic as wide AND gates, ORed together, driving either a flip-flop or an output directly. The simple logic structure makes these devices easy to understand, and results in both fast design compilation and short pin-to-pin delays. Wide input gating and fast system clock rates up to 150 MHz are attractive features for state machines and complex synchronous counters.

The XC9500 in-system programmable family, based on FLASH technology, eliminates the need for a separate programmer. These new devices also offer boundary scan (JTAG) to simplify board testing.

## Overview of CPLD Families

**XC7300:** Superseded

Do not use for new designs. Use XC9500 instead.

**XC9500:** FLASH-Based CPLD

Six devices cover the range from 36 to 288 macrocells.

The new XC9500 family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration.

- Delays are deterministic, and compile times are very short.
- Use for high-speed logic, short pin-to-pin delays, for state machines and flexible address decoding, and as PAL replacement.
- Accept higher power consumption and fewer available flip-flops compared to SRAM FPGA.

## Selecting the Appropriate Xilinx Family

It is not always obvious which Xilinx family is the "right" choice for a particular application. To make a decision, start with the known data, the target application. Then address the following questions:

- What type of logic is used in the application?
- What special features are required?

### Type of Logic

All Xilinx devices are general-purpose. Any family can implement any type of logic. There are, however, some features that make certain families more appropriate than others. The following items should be interpreted as "soft" suggestions, not as absolute, unequivocal choices.

#### 1. For shortest pin-to-pin delays and fastest flip-flops:

Use XC9500, or, if fan-in is sufficient, XC3100A, XC4000E/X, or Spartan families.

XC9500 CPLDs have a PAL-like AND/OR structure that is inherently very fast. XC3100A has extremely fast logic blocks, but the single-level fan-in is limited to five.

XC4000E/X/Spartan families have a wider fan-in of nine. XC4000X FPGAs offer a very fast pin-to-pin path using a fast buffer and a 2-input function generator in the IOB.

#### 2. For fastest state machines:

For encoded state machines, use XC9500.

For "one-hot" state machines, use XC3100A, XC4000E/X, XC5200, or Spartan families.

#### 3. For fast counters/adders/subtractors/accumulators/comparators:

Use XC4000E/X, XC5200, Spartan or XC9500 families for wide functions.

Use XC3100A for fast, but short or simple counters.

Spartan, XC4000E/X, and XC5200 devices have dedicated carry-logic that is most effective over the range of 8 to 32 bits.

XC3100A achieves high speed for short word-length and simple operations (such as non-loadable counters) through its fast logic blocks.

#### 4. For shortest design compilation time:

Use XC9500.

XC9500 achieves fast compilation through the simplicity of its PAL-like architecture.

#### 5. For lowest cost per gate:

Use Spartan families.

#### 6. For pinout compatibility within and between families:

Use XC4000E/X, XC5200.

These families are carefully designed to fit the same pinout in any given available package. This allows easy migration to different device sizes or families in the same package. The user can add logic or streamline the design or even use a less costly or faster family without any need to change the existing PC-board layout.

#### 7. For Digital Signal Processing (multiply-accumulate) applications:

Use XC4000E/X or Spartan families.

The look-up-table architecture and the dedicated carry structure are very efficient for distributed arithmetic, a fast and effective way to implement fixed-point multiplication in digital filters.

### Special Features Required

The fourteen items below describe specific features and characteristics available only in the listed families. These are, therefore, "hard" selection criteria.

#### 8. For on-chip RAM:

Use XC4000E/X or Spartan families.

Has many 16x1 or 32x1 RAMs with synchronous write and dual-port capability.

#### 9. For on-chip (bidirectional) bussing:

Use XC3000A, XC3100A, XC4000E/X, XC5200, XC9500, or Spartan families.

XC3000A, XC3100A, XC4000, Spartan and XC5200 families have horizontal Longlines that can be driven by internal 3-state drivers.

XC9500 devices implement busses indirectly using the wired-AND capability in the switch matrix.

#### 10. For non-volatile single-chip solutions:

Use XC9500 or any HardWire device.

The SRAM-based devices require an external configuration source, which may be contained in the microprocessor's memory. XC3000A and XC3000L devices can be used with a battery-backed-up supply, thus eliminating the need for external configuration storage.

#### 11. For lowest possible static power consumption at 5V:

Use XC3000A and, to a lesser extent, Spartan, XC5200, XC4000E, XC4000EX families.

For Icc down to a few microamps, use XC3000A/L in powerdown. The other families consume a few milliamps.

Configurations for CMOS input thresholds on all inputs reduce supply current significantly.

**12. For avoiding pin-locking problems with routing-intensive designs:**

Use XC9500, XC4000EX, XC4000XL, XC5200.

XC9500 devices have special architectural features to enable pin locking.

XC4000EX, XC4000XL, and XC5200 provide additional routing channels, called VersaRing, between the core logic and the I/O.

**13. For Boundary-Scan support:**

Use Spartan, XC4000E, XC4000X, XC5200, or XC9500 families.

**14. For rail-to-rail output voltage swing at 5V Vcc:**

Use Spartan, XC3000A, XC3100A, XC4000E, XC4000EX, or XC5200 families.

(In XC4000E/EX, rail-to-rail is a user-option.)

XC9500 devices have a “totem-pole” output structure with lower Voh.

Spartan/XC4000E/EX devices can be configured with a global choice of either totem-pole or rail-to-rail outputs.

**15. For 3.3V operation:**

Use XC3000L, XC4000XL, or SpartanXL families.

**16. For 5V operation Interfacing with 3.3V devices:**

Use XC9500, Spartan or XC4000E/EX families.

Any Spartan/XC4000E/EX “totem-pole” output drives 3.3V inputs safely, and the TTL-like input threshold can be driven from 3.3V logic.

**17. For In-system programmability:**

Use all Xilinx families.

**18. For PCI compatibility:**

Use Spartan/XC4000E/XL and XC9500 families.

Target and Initiator designs are available for the XC4000E, XC4000XL, and Spartan families.

**19. For Hi-Rel, military, or mil temperature-range applications:**

Use XC4000E/X.

**20. For battery-operated applications requiring low stand-by current:**

Use XC3000A/L, Spartan, XC4000E/EX, XC5200 families.

XC3000L devices have inherently very low static power consumption.

XC3000A devices can use powerdown to ignore all input activity and tolerate Vcc down to 2.3V, while maintaining configuration.

Spartan/XC4000E/EX devices must be configured for CMOS input thresholds, and the user must shut down clock and logic activities externally.

**21. For best protection against Illegal copying of a design (design security):**

Use XC9500 with security bit activated.

Use XC3000A or XC3000L with powerdown battery-back-up configuration.

## Further Information

For further information on any of the Xilinx products discussed in this application note, see the Xilinx WEBLINX at <http://www.xilinx.com>, or call your local sales office.

**Table 1: Selecting a Xilinx Family**

Feature	XC3000A	XC3000L	XC3100A	XC3100L	XC4000E	XC4000EX	XC4000XL	XC4000XV	XC5200	Spartan	SpartanXL	XC9500
1. Shortest pin-to-pin			X		X	X	X			X	X	X
2. Fastest state machines			X		X	X	X	X	X	X	X	X
3. Fastest arithmetic counters			X		X		X	X	X	X	X	
4. Fastest compilation												X
5. Lowest cost										X	X	
6. Footprint compatible families					X	X	X	X	X			
7. DSP (multiply/accumulate)					X	X	X	X		X	X	
8. RAM					X	X	X	X		X	X	
9. Bidirectional busses	X	X	X	X	X	X	X	X	X	X	X	X
10. Non-volatile/single chip												X
11. Low power @ 5V	X				X	X			X	X		
12. Tolerates pin-locking						X	X	X	X			X
13. Boundary scan					X	X	X	X	X	X	X	X
14. Full-swing 5V output	X		X		option	option			X	option		
15. 3.3V operation		X		X			X	X			X	
16. 5V out drives 3.3V					option	option				option		X
17. In-system programmable	X	X	X	X	X	X	X	X	X	X	X	X
18. PCI-compatible					X		X			X	X	X
19. Hi-rel, mil, mil-temp					X	X	X					
20. Low standby current	X	X			X	X	X	X		X	X	
21. Design security	X	X										X



## I/O Characteristics of the 'XL FPGAs

XAPP 088 November 24, 1997 (Version 1.0)

Application Note by PETER ALFKE and BOB CONN

### Summary

Data sheets describe I/O parameters in digital terms, providing tested and guaranteed worst-case values. This application note describes I/O parameters in analog terms, giving the designer a better understanding of the circuit behavior. Such parameters are, however, not production-tested and are, therefore, not guaranteed.

### Xilinx Families

XC4000XL, XC4000XV, and Spartan-XL

### Inputs

Input threshold, the voltage where a 0 changes to a 1 and vice versa, is stable over temperature, but proportional to  $V_{CC}$ :

37 to 38% of  $V_{CC}$  for the falling threshold, 39 to 42% for the rising threshold. There is 50 mV to 150 mV of hysteresis, smallest at hot and high  $V_{CC}$ , largest at cold and low  $V_{CC}$ .

### 5-V Tolerant Inputs

Currently, many systems use a mixture of older 5-V devices and newer 3.3-V devices. This can pose a problem when a 5-V logic High drives a 3.3-V input. See Figure 1.

On most CMOS ICs each signal pin has a clamp diode to  $V_{CC}$ , to protect the circuit against electrostatic discharge (ESD). This diode starts conducting when the pin is driven more than 0.7 V positive with respect to its  $V_{CC}$ . In mixed-voltage systems, this diode presents a problem since it might conduct tens of millamps whenever a 5-V logic High is connected to a 3.3-V input.

In the XC4000XL/XV and SpartanXL devices, Xilinx has overcome this difficulty by eliminating the clamp diode between the device pins and  $V_{CC}$ . The pins can thus be driven as High as 5.5 V, irrespective of the actual supply voltage on the receiving input. These devices are, therefore, unconditionally 5-V tolerant.

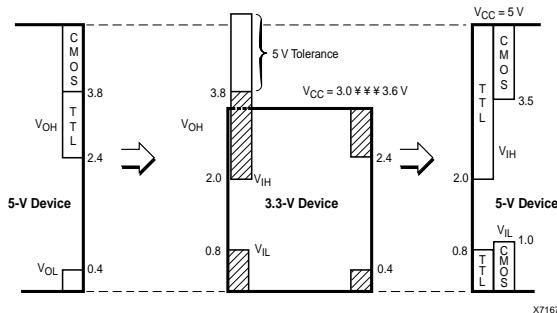


Figure 2: Interface Levels

ant, and the user can ignore all interface precautions, and need not worry about power sequencing.

Excellent ESD protection (up to several thousand volts) is achieved by means of a patented diode-transistor structure that connects to ground, and not to  $V_{CC}$ . The structure behaves like a Zener diode; it becomes conductive at >6 V and diverts the charge or current directly to ground. It can handle current spikes of several hundred millamps, but continuous current must be kept below 20 mA to avoid reliability problems caused by on-chip metal migration.

See also the application note "Supply-Voltage Migration, 5 V to 3.3 V", XAPP080, available at [www.xilinx.com](http://www.xilinx.com).

### PCI-Compliance

The 'XL-I/O is designed to be PCI compliant and also to be 5-V tolerant.

- 3.3-V PCI compliance requires a clamping diode to  $V_{CC}$ .
- 5-V PCI compliance does not explicitly require such a diode, but requires passing the specified PCI overshoot test.
- 5-V tolerance does not permit such a diode.

To satisfy these conflicting requirements, an internal diode is added to each output, with its cathode connected to an internal  $V_{TT}$  rail. See Figure 2.

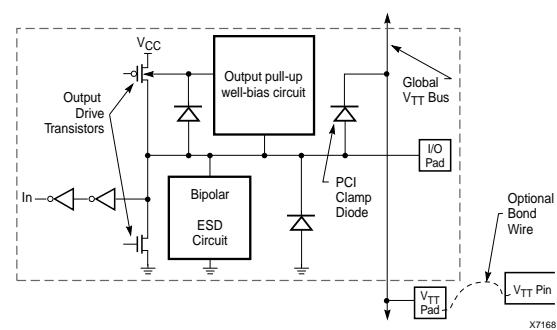


Figure 3: Simplified 'XL-I/O Structure

In the PCI-compliant XC4000XLT devices, this rail is internally bonded to eight device pins which externally must be connected to the appropriate V<sub>CC</sub> supply (5 V or 3.3 V).

In all other 'XL devices, the V<sub>TT</sub> rail is internally left unconnected, thus assuring 5-V tolerance.

## Outputs

### Sink and Source Capability

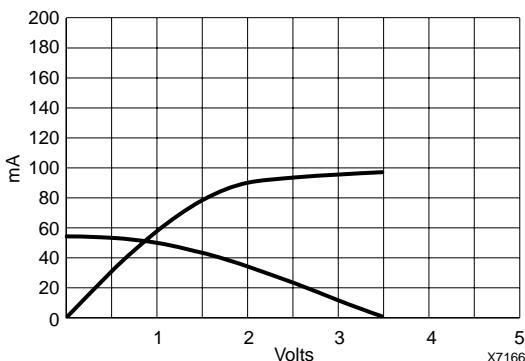
The IBIS files describe the strength of the CMOS output drivers as black boxes, giving only voltage/current values without revealing proprietary circuit details. IBIS gives an unnecessarily large set of numbers, when most users just want to know the strength of the pull-down transistor (sink capability) and the pull-up transistor (source capability). Close to either rail, the outputs are resistive, i.e. voltage is proportional to current.

Table 1 condenses the information and expresses it as output resistance in Ohm for a sink voltage less than 1 V above ground, and a source voltage less than 1 V below V<sub>CC</sub>. (Data based on SPICE simulation).

**Table 2: Sink and Source Capability**

Device Family	Sink Resistance to GND	Source Resistance to VCC	
XC4000E	22.1 - 27.7	53.3 - 90.5	Ohm
XC4000EX	14.4 - 18.8	48.0 - 58.7	Ohm
XC4000XL/XV Spartan-XL	14.4 - 20.5	28.0 - 41.0	Ohm
Optional on all XC4000XV*	8.0 - 12.0*	20.0 - 30.0*	Ohm

\* This per-pin option will also be available on all XC4000XL and Spartan-XL devices later in 1998.



**Figure 4: Output Voltage/  
Current Characteristics (default for XC4000XL,**

## Effect of Additional Capacitive Load

### Transition Time

At the specified 50 pF external load, the rise time is 2.4 ns, and the fall time is 2.0 ns. For additional capacitive loads, add 60 ps/pF to the rise time, and 40 ps/pF to the fall time.

### Delay

Add 30 ps/pF to the rising-edge delay at 3.0 V.

Add 23 ps/pF to the rising-edge delay at 3.6 V.

Add 25 ps/pF to the falling-edge delay at any voltage.

The values were derived from XC4028XL measurements using the fast output option, but the slew-rate limited output option behaves almost identically.

These results are consistent with the IBIS-derived output impedance, since the delay increases with approximately one RC time constant, and the rise and fall times increase each with approximately two time constants.

These are not guaranteed and tested parameters; they are established by measuring a few devices. Xilinx, therefore, suggests that the user add a 20% guardband (multiply by 1.20) when calculating additional delay due to capacitive load above the guaranteed test limit of 50 pF.

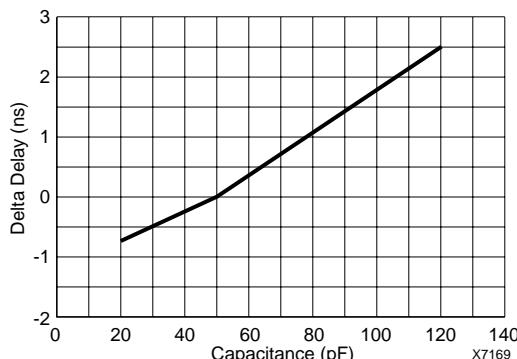
For the same reason, subtract 20% (multiply by 0.80) when calculating the delay reduction due to a capacitive load that is less than 50 pF external. See Figure 4.

When comparing Xilinx numbers to those from other vendors who use 35 pF as a standard load, reduce the Xilinx-specified delay by 0.4 ns. Reduce the Xilinx-specified rise time by 1.0 ns and the fall time by 0.6 ns, thus changing both to 1.4 ns.

### Example:

For an external lumped capacitive load of 200 pF, the rising-edge delay at 3.0 V increases by  $1.2 \cdot 150 \cdot 30 = 5.4$  ns over the guaranteed data sheet value.

The rising-edge transition time increases by an amount of  $1.2 \cdot 150 \text{ pF} \cdot 60 \text{ ps/pF} = 10.8$  ns over the 50-pF transition time of 2.4 ns. The rise time is thus 13.2 ns.



**Figure 5: Additional Delay at Various Capacitive Loads**



## XC4000 Series Technical Information

XAPP 045 November 24, 1997 (Version 1.1)

Application Note

### Summary

This Application Note contains additional information that may be of use when designing with XC4000 Series devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

### Xilinx Family

XC4000/XC4000E/XC4000EX/XC4000L

## Introduction

This application note describes the electrical characteristics of the output drivers, their static output characteristics or I/V curves, the additional delay caused by capacitive loading, and the ground bounce created when many outputs switch simultaneously.

## Voltage/Current Characteristics of XC4000-Family Outputs

Figures 1 and 2 show the output source and sink currents, both drawn as absolute values. Note that the XC4000E/EX families offer a configuration choice between an n-channel only, totem-pole like output structure that pulls a High output to a voltage level that is one threshold drop lower than  $V_{CC}$ , and a conventional complementary output with a p-channel transistor pulling to the positive supply rail. When driving inputs that have a 1.4-V threshold, the lower  $V_{OH}$  of the totem-pole ("TTL") output offers faster speed and more symmetrical switching delays.

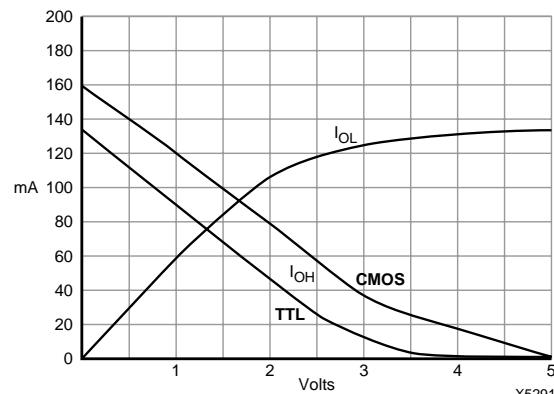


Figure 1: Output Voltage/Current Characteristics for XC4000E

These curves represent typical devices. Measurements were taken at nominal  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$ . These characteristics vary by manufacturing lot, and will be affected by future changes in minimum device geometries. These characteristics are not production-tested as part of the normal device test procedure; they can, therefore, not be guaranteed. Although these measurements show that the output sink and source capability far exceeds the guaranteed data sheet limits, continuous high-current operation beyond the data sheet limits can cause metal migration of the on-chip metal traces, permanently damaging the device. Output currents in excess of the data-sheet limits are, therefore, not recommended for continuous operation. These output characteristics can, however, be used to calculate or model output transient behavior, especially when driving transmission lines or large capacitive loads.

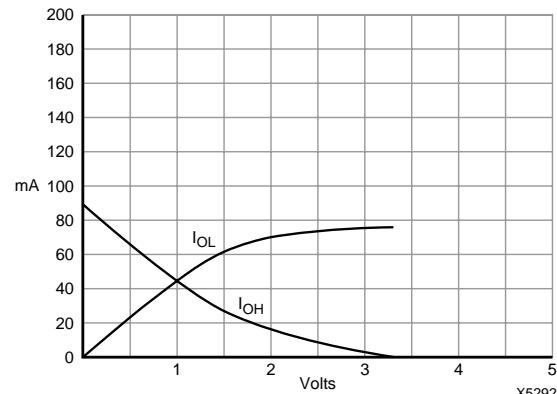


Figure 2: Output Voltage/Current Characteristics for XC4000XL

## Additional Output Delays When Driving Capacitive Load

Xilinx Product Specifications in chapter 4 give guaranteed worst-case output delays with a 50-pF load.

The values below are based on actual measurements on a small number of mid-93 production XC4005-5, all in PQ208 packages, measured at room temperature and  $V_{CC} = 5.5$  V. Listed is the additional output delay, measured crossing 1.5 V, relative to the delays specified in this Data Book.

These parameters are not part of the normal production test flow, and can, therefore, not be guaranteed.

**Table 1: Increase in Output Delay When Driving Light Capacitive Loads (<150 pF)**

		High-to-Low			Low-to-High			
	Slew Mode	10	50	100	10	50	100	pF
XC4000	Slow	-1.6	0*	1.4	-1.4	0*	1.4	ns
	Fast	-1.6	0*	1.2	-1.2	0*	1.1	ns

Note: \*Zero by definition

**Table 2: Increase in Output Delay When Driving Heavy Capacitive Loads (>150 pF)**

	Slew Mode	High-to-Low	Low-to-High	
XC4000	Slow	1.7	1.2	ns/100 pF
	Fast	1.5	1.2	ns/100 pF

Example:

$\Delta t$  High-to-Low for XC4005-5 with Fast-mode output driving 250 pF:

$$1.2 \text{ ns (from Table 1)} + (250-100) \text{ pF} \cdot 1.5 \text{ ns/100 pF} \\ = 1.2 \text{ ns} + 2.25 \text{ ns} = 3.45 \text{ ns}$$

Total propagation delay, clock to pad:

$$T_{OKPOF} + 3.45 \text{ ns} = 7.0 \text{ ns} + 3.45 \text{ ns} = 10.45 \text{ ns}$$

## Ground Bounce in XC4000 Devices

Ground-bounce is a problem with high-speed digital ICs, when multiple outputs change state simultaneously causing undesired transient behavior on an output, or in the internal logic. This is also referred to as the Simultaneous Switching Output (SSO) problem. Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC-internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously. Ground bounce affects outputs that are supposed to be stable Low, and it also affects all inputs since they interpret the incoming level by referencing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input will be interpreted as a short pulse with a polarity opposite to the ground bounce.

$V_{CC}$  bounce is not as important as ground bounce, because it is of lower magnitude due to the weaker pull-up transistors. Also, the noise immunity in the High state is usually better than in the Low state, and input levels are referenced to ground, not  $V_{CC}$ . All this is the result of our industry's TTL heritage.

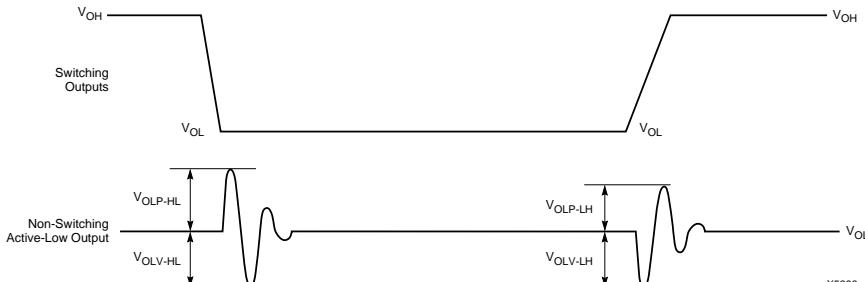
### Test Method

Data was taken on XC4005-5, devices in the PQ208 package, soldered to the Xilinx Ground Bounce Test Board. Pin 82, two pins away from the nearest ground pin, was configured as a permanently Low output driver, effectively monitoring the internal ground level. The simultaneously switching outputs were on pins 80 and 83, for two outputs switching; additionally, pins 80 and 86 were used for four outputs switching. The closest ground pins are 79 and 90.

Four ground-bounce parameters were measured at room temperature, with  $V_{CC}$  set at 5.5 V as shown in Figure 3.

- $V_{OLP-HL}$  Peak ground noise when switching High-to-Low
- $V_{OLV-HL}$  Valley ground noise when switching High-to-Low
- $V_{OLP-LH}$  Peak ground noise switching Low-to-High
- $V_{OLV-LH}$  Valley ground noise switching Low-to-High

All four parameters can affect system reliability.



X5299

**Figure 3: Ground Bounce**

The two positive peak values can cause problems with a signal leaving the ground bounce chip, driving another chip. The positive ground bounce voltage is added to the  $V_{OL}$ , and may exceed the receiving input's noise margin. A continuously logic Low input may thus be interpreted as a short-duration High pulse.

The two negative valley parameters can cause problems with a signal arriving at the ground-bounce chip, reducing the Low-level noise immunity. The incoming voltage may not be Low enough, and may, therefore, be interpreted as a short-duration High input pulse.

**Table 3: Ground Bounce, 16 Outputs Switching, Each With 50 or 150 pF Load,  $V_{CC} = 5.5$  V**

Load	Slew Rate	High-to-Low		Low-to-High		Unit
		$V_{OLP}$	$V_{OLV}$	$V_{OLP}$	$V_{OLV}$	
16 x 50 pF	Slow	670	480	240	240	mV
	Fast	1,170	710	480	660	mV
16 x 150 pF	Slow	740	330	210	280	mV
	Fast	1,180	420	350	710	mV

## Interpretation of the Results

Ground bounce is a linear phenomenon. When multiple outputs switch, the total ground bounce is the sum of the ground-bounce values caused by individual outputs switching. Since the actual switching of multiple outputs is usually not quite simultaneous, small timing differences between the switching outputs, caused by routing delays, can indirectly affect the amplitude. With low capacitive loading, < 50 pF, the peaks and valleys might even partially cancel each other. With larger capacitive loads, the tendency is for valleys to combine with valleys and peaks to combine with peaks.

In most devices tested, the load capacitance does not directly affect the ground-bounce **amplitude**, but it does affect the **duration** of the ground-bounce signals.

On the fastest outputs, minimal load capacitance created a ground-bounce resonant frequency of 340 MHz, with a half-cycle time of 1.5 ns. Such a signal exceeds 90% of its peak amplitude for about 0.4 ns.

With a 50 pF load on the switching outputs, the ground bounce resonant frequency is 90 MHz, with a half-cycle time of 5 ns, staying 1.7 ns above 90% of peak amplitude.

With a 150 pF load on the switching outputs, the ground bounce resonant frequency is 40 to 60 MHz, with a half-cycle time of 8 to 12 ns, staying 3 ns above 90% of peak amplitude.

The main problem with large load capacitances is not an increase in amplitude, but rather an increase in duration of the ground-bounce signal. The amplitude is mainly affected by the number of outputs switching simultaneously, and by

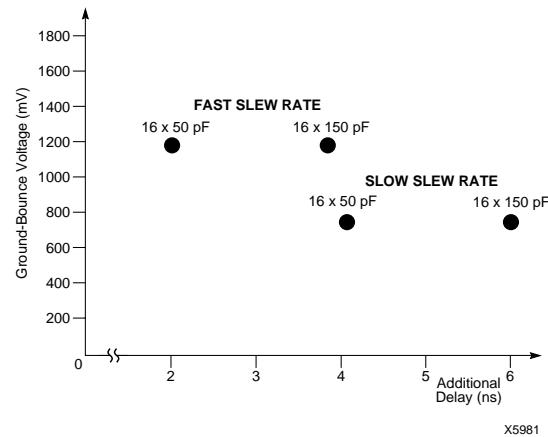
the slew-rate mode of these outputs. Switching outputs closer to the monitoring output also cause larger peaks and valleys than outputs further away.

## Guidelines for Reducing Ground-Bounce Effects

- Minimize the impedance of the system ground distribution network and its connection to the IC pins. PQFPs are best suited, PGAs are worst, and PLCCs are in-between.
- Use PC-boards with ground- and  $V_{CC}$ -planes, connected directly to the ICs' supply pins. Place decoupling capacitors very close to these ground and  $V_{CC}$  pins.
- Keep the ground plane as undisturbed as possible. A row of vias can easily cause a dynamic ground-voltage drop.
- Keep the clock inputs physically away from the outputs that create ground bounce, and connect clocks to input pins that are close to a ground pin. Make sure that all clock and asynchronous inputs have ample noise margin, especially in the Low state.
- If possible, avoid simultaneous switching by staggering output delays, e.g. through additional local routing of signals or clocks.
- Spread simultaneously switching outputs around the IC periphery. For a 16-bit bus, use two outputs each on either side of four ground pins.

## Ground-Bounce vs Delay Trade-Off

After the external sources of ground bounce have been reduced or eliminated, the designer can trade reduced ground bounce for additional delay by selecting between families and slew-rate options. Figure 4 shows the trade-off for 16 outputs switching simultaneously High-to-Low.



**Figure 4: Ground-Bounce vs. Delay Trade-off for 16 Outputs Switching 50 and 150 pF Each**

## XC4000 and XC4000E Power Consumption

Below are the dynamic power consumption values for typical design elements in XC4000 and XC4000E.

The differences between XC4000 and XC4000E are too small to be statistically relevant:

Global clocks in XC4000E are 3% higher, and Longlines and unloaded outputs in XC4000E are 5 to 10% lower than in XC4000.

Power consumption is given at nominal 5.0-V supply and 25°C.

Power is proportional to the square of the supply voltage, but is almost constant over temperature changes. Power is given as "mW per million transitions per second", since the more commonly used "MHz" can be ambiguous. When a 10-MHz clock toggles a flip-flop, the clock line obviously makes 20 MTps, the flip-flop output only 10 MTps.

The first six elements are device-size independent, i.e. they are applicable to all XC4000 or XC4000E devices operating at 5-V Vcc.

- One CLB flip-flop driving nothing but a neighboring flip-flop in the same or adjacent CLB (a typical shift register design):  
0.1 mW per million transitions per second =  
0.1 mW/MTps
- One CLB flip-flop driving its neighbor plus 9 lines of interconnect:  
0.2 mW per million transitions per second =  
0.2 mW/MTps
- One unloaded or unbonded TTL-level output:  
0.25 mW per million transitions per second =  
0.25 mW/MTps
- 50 pF on a TTL-level output: add 0.5 mW/MTps = 1.0 mW/MHz
- One unloaded or unbonded XC4000E CMOS-level output:  
0.31 mW per million transitions per second =  
0.31 mW/MTps
- 50 pF on a CMOS-level output: add 0.625 mW/MTps =  
1.25 mW/MHz

The following elements are obviously device-size dependent:

- One Global Clock driving all CLB flip-flops, but no flip-flop changing:  
in XC4005: 4 mW/MTps = 8 mW/MHz  
in XC4010: 8 mW/MTps = 16 mW/MHz  
in XC4013: 12 mW/MTps = 24 mW/MHz  
in XC4020: 16 mW/MTps = 32 mW/MHz  
in XC4025: 20 mW/MTps = 40 mW/MHz
- One full-length horizontal or vertical Longline with one driving CLB source and one driven CLB load:  
in XC4005: 0.10 mW/MHz = 0.20 mW/MTps  
in XC4010: 0.15 mW/MTps = 0.30 mW/MHz  
in XC4013: 0.18 mW/MTps = 0.36 mW/MHz  
in XC4020: 0.20 mW/MTps = 0.40 mW/MHz  
in XC4025: 0.24 mW/MTps = 0.48 mW/MHz

These numbers do not account for the 10 mA of static power consumption when all device inputs are configured in TTL mode, which is always the default mode, and in XC4000 is actually the only user-accessible mode.

These numbers assume short rise and fall times on all inputs, avoiding the cross-current when both the n-channel pull-down and the p-channel pull-up transistor in the input buffer might conduct simultaneously.

### Tutorial Comments:

In its pure form, a CMOS output driving a capacitive load has a power consumption that is independent of drive impedance or rise and fall time. For a full-swing signal, the power consumed when charging the capacitor is  $C \times V^2 \times f$  where  $f$  is the frequency of charge operations. In each charge operation, half the total energy consumed ends up on the capacitor, and the other half of the energy is dissipated in the current-limiting resistor or transistor, whatever its value may be.

The subsequent discharge cycle does not take any new energy from the power supply, but dissipates in the current-limiting resistor/transistor all the energy that was formerly stored in the capacitor.

It is assumed here that the frequency is low enough so that the capacitors are completely charged and discharged in each half-cycle.



## XC3000 Series Technical Information

XAPP 024 November 24, 1997 (Version 1.0)

Application Note By Peter Alfke and Bernie New

### Summary

This Application Note contains additional information that may be of use when designing with the XC3000 series of FPGA devices. This information supplements the data sheets, and is provided for guidance only.

### Xilinx Family

XC3000/XC3000A/XC3000L/XC3100/XC3100A/XC3100L

## Contents

### CLBs

Function Generators

Flip-flops

Longline Access

### IOBs

Inputs

Outputs

### Routing

Horizontal Longlines

Bus contention

Vertical Longlines

Vertical Longlines

Clock Buffers

Vertical Longlines

Clock Buffers

### Power Dissipation

### Crystal Oscillator

### CCLK Frequency Stability and Low-time restriction

### Powerdown and Battery-Backup

### Configuration and Start-Up

### Reset

Beware of slow rise-time

## Introduction

The background information provided in this Application Note supplements the XC3000, XC3000A, XC3000L, XC3100A and XC3100L data sheets. It covers a wide range of topics, including a number of electrical parameters not specified in the data sheets, and unless otherwise noted, applies to all six families. These additional parameters are sufficiently accurate for most design purposes; unlike the parameters specified in the data sheets, however, they are not worst-case values over temperature and voltage, and are not 100% production tested. They can, therefore, not be guaranteed.

## Configurable Logic Blocks

The XC3000/XC3100 CLB, shown in [Figure 1](#), contains a combinatorial function generator and two D-type flip-flops. Two output pins may be driven by either the function generators or the flip-flops. The flip-flop outputs may be routed directly back to the function generator inputs without going outside of the CLB.

The function generator consists of two 4-input look-up tables that may be used separately or combined into a single function. [Figure 2](#) shows the three available options. Since the CLB only has five inputs to the function generator, inputs must be shared between the two look-up tables.

In the FG mode, the function generator provides any two 4-input functions of A, B and C plus D or E; the choice between D and E is made separately for each function. In the F mode, all five inputs are combined into a single 5-input function of A, B, C, D and E. Any 5-input function may be emulated. The FGM mode is a superset of the F mode, where two 4-input functions of A, B, C and D are multiplexed together according to the fifth variable, E.

In all modes, either of the B and C inputs may be selectively replaced by QX and QY, the flip-flop outputs. In the FG mode, this selection is made separately for the two look-up tables, extending the functionality to any two functions of four variables chosen from seven, provided two of the variables are stored in the flip-flops. This is particularly useful in state-machine-like applications.

In the F mode, the function generators implement a single function of five variables that may be chosen from seven, as described above. The selection of QX and QY is constrained to be the same for both look-up tables. The FGM mode differs from the F mode in that QX and QY may be selected separately for the two look-up tables, as in the FG mode. This added flexibility permits the emulation of selected functions that can include all seven possible inputs.

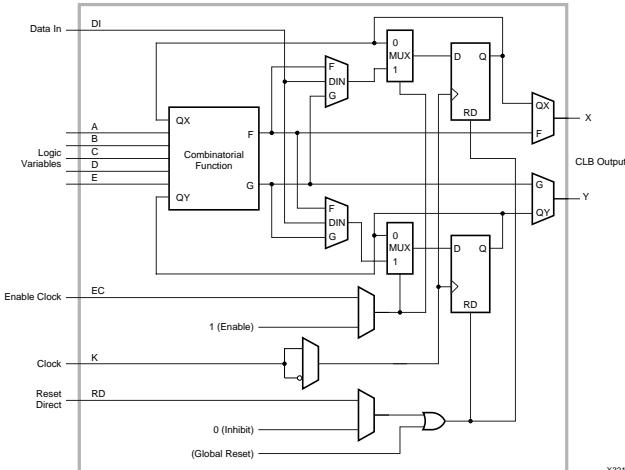


Figure 1: Configurable Logic Block (CLB)

X3217

## Function Generator Avoids Glitches

The combinatorial logic in all CLBs is implemented as a function generator in the form of a multiplexer, built out of transfer gates. The logic inputs form the select inputs to this multiplexer, while the configuration bits drive the data inputs to the multiplexer.

The Xilinx circuit designers were very careful to achieve a balanced design with similar (almost equal) propagation delays from the various select inputs to the data output.

The delay from the data inputs to the output is, of course, immaterial, since the data inputs do not change dynamically. They are only affected by configuration.

This balanced design minimizes the duration of possible decoding glitches when more than one select input changes. Note that there can never be a decoding glitch when only one select input changes. Even a non-overlapping decoder cannot generate a glitch problem, since the node capacitance will retain the previous logic level until the new transfer gate is activated about a nanosecond later.

When more than one input changes "simultaneously," the user should analyze the logic output for any possible intermediate code. If any such code permutation produces a different result, the user must assume that such a glitch might occur and must make the system design immune to it. The glitch might be only a few nanoseconds long, but that is long enough to upset an asynchronous design.

If none of the possible address sequences produces a different result, the user can be sure that there will be no glitch.

The designer of synchronous systems generally doesn't worry about such glitches, since synchronous designs are fundamentally immune to glitches on all signals except clocks or direct SET/RESET inputs.

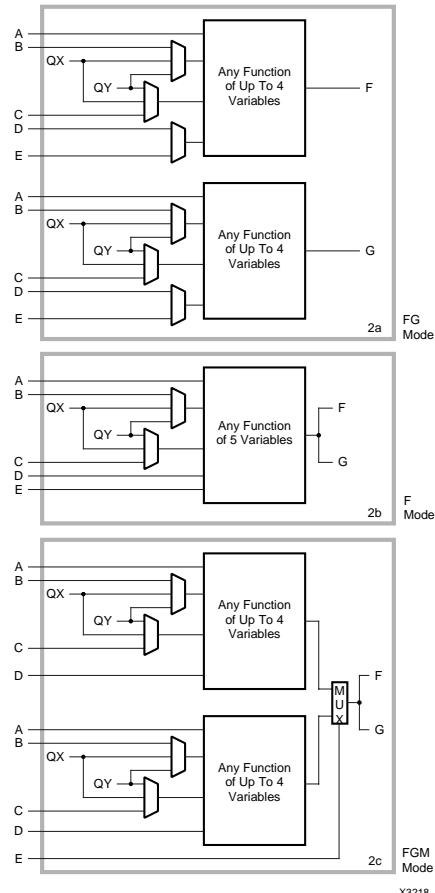


Figure 2: CLB Logic Options

X3218

The automatic logic-partitioning software in the XACT step development system only uses the FG and F modes. However, all three modes are available with manual partitioning, which may be performed in the schematic. If FG or F modes are required, it is simply a matter of including in the schematic CLBMAP symbols that define the inputs and outputs of the CLB.

The FGM mode is only slightly more complicated. Again, a CLBMAP must be used, with the signal that multiplexes between the two 4-input functions locked onto the E pin. The CLB will be configured in the FGM mode if the logic is drawn such that the gates forming the multiplexer are shown explicitly with no additional logic merged into them.

The two D-type flip-flops share a common clock, a common clock enable, and a common asynchronous reset signal. An asynchronous preset can be achieved using the asynchronous reset if data is stored in active-low form; the Low created by reset corresponds to the bit being asserted. The flip-flops cannot be used as latches.

If input data to a CLB flip-flop is derived directly from an input pad, without an intervening flip-flop, the data-pad-to-clock-pad hold time will typically be non-zero. This hold time is equal the delay from the clock pad to the CLB, but may be reduced according to the 70% rule, described later in the IOB Input section of this Application Note. Under this rule, the hold time is reduced by 70% of the delay from the data pad to the CLB, excluding the CLB set-up time. The minimum hold time is zero, even when applying the 70% rule results in a negative number.

The CLB pins to which Longlines have direct access are shown in [Table 1](#). Note that the clock enable pin (EC) and the TBUF control pin are both driven from the same vertical Long Line. Consequently, EC cannot easily be used to enable a register that must be 3-stated onto a bus. Similarly, EC cannot easily be used in a register that uses the Reset Direct pin (RD).

**Table 1: Longline to CLB Direct Access**

Longline	CLB							TBUF
	A	B	C	D	E	K	EC	
Left Most Vertical (GCLK)					X			
Left Middle Vertical	X					X	X	X
Right Middle Vertical		X	X					
Right Most Vertical (ACLK)				X				
Upper Horizontal			X					
Lower Horizontal	X						X	

## Input/Output Blocks

The XC3000/XC3100 IOB, shown in Figure 3, includes a 3-state output driver that may be driven directly or registered. The polarities of both the output data and the 3-state control are determined by configuration bits. Each output buffer may be configured to have either a fast or a slow slew rate.

The IOB input may also be direct or registered. Additionally, the input flip-flop may be configured as a latch. When an IOB is used exclusively as an input, an optional pull-up resistor is available, the value of which is 40-150 kΩ. This resistor cannot be used when the IOB is configured as an output or as a bidirectional pin.

Unused IOBs should be left unconfigured. They default to inputs pulled High with the internal resistor.

## Inputs

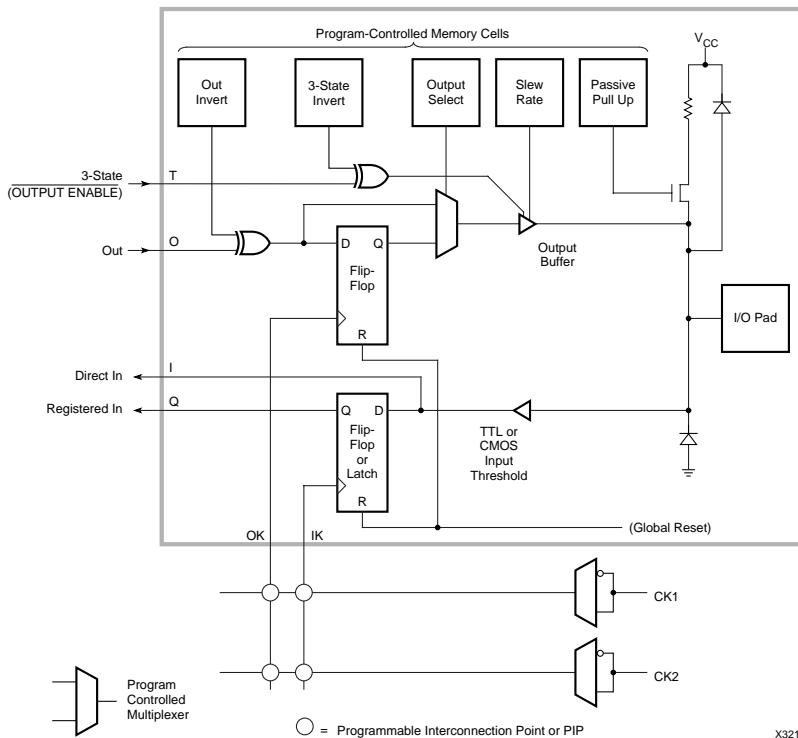
All inputs have limited hysteresis, typically in excess of 200 mV for TTL input thresholds and in excess of 100 mV for CMOS thresholds. Exceptions to this are the PWRDWN pin, and the XTL2 pin when it is configured as the crystal oscillator input.

Experiments show that the input rise and fall times should not exceed 250 ns. This value was established through a worst-case test using internal ring oscillators to drive all I/O pins except two, thus generating a maximum of on-chip noise. One of the remaining I/O pins was configured as an input, and tested for single-edge response; the other I/O was used as an output to monitor the response.

These test conditions are, perhaps, overly demanding, although it was assumed that the PC board had negligible ground noise and good power-supply decoupling. While conservative, the resulting specification is, in most instances, easily satisfied.

IOB input flip-flops are guaranteed to operate correctly without data hold times (with respect to the device clock-input pad) provided that the dedicated CMOS clock input pad and the GCLK buffer are used. The use of a TTL clock or a different clock pad will result in a data-hold-time requirement. The length of this hold time is equal to the delay from the actual clock pad to the GCLK buffer minus the delay from the dedicated CMOS clock pad to the GCLK buffer.

To ensure that the input flip-flop has a zero hold time, delay is incorporated in the D input of the flip-flop, causing it to have a relatively long set-up time. However, the set-up time specified in the data sheet is with respect to the clock reaching the IOB. Since there is an unavoidable delay between the clock pad and the IOB, the input-pad-to-clock-pad set-up time is actually less than the data sheet number.



X3216

**Figure 3: Input/Output Block (IOB)**

Part of the clock delay can be subtracted from the internal set-up time. Ideally, all of the clock delay could be subtracted, but it is possible for the clock delay to be less than its maximum while the internal set-up time is at its maximum value. Consequently, it is recommended that, in a worst-case design, only 70% of the clock delay is subtracted.

The clock delay can only be less than 70% of its maximum if the internal set-up time requirement is also less than its maximum. In this case, the pad-to-pad set-up time actually required will be less than that calculated.

For example, in the XC3000-125, the input set-up time with respect to the clock reaching the IOB is 16 ns. If the delay from the clock pad to the IOB is 6 ns, then 70% of this delay, 4.2 ns, can be subtracted to arrive at a maximum pad-to-pad set-up time of ~12 ns.

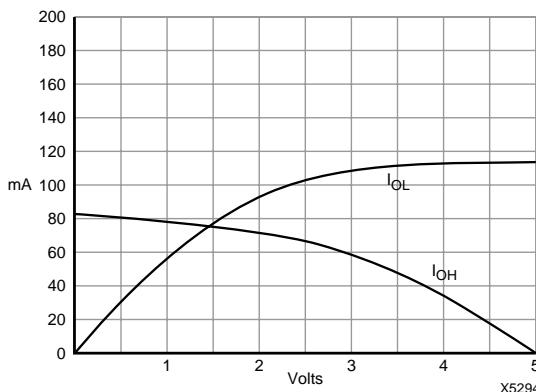
The 70% rule must be applied whenever one delay is subtracted from another. However, it is recommended that delay compensation only be used routinely in connection with input hold times. *Delay compensation in asynchronous circuits is specifically not recommended.* In any case, the compensated delay must not become negative. If 70% of the compensating delay is greater than the delay from which it is deducted, the resulting delay is zero.

*The 70% rule in no way defines the absolute minimum values delays that might be encountered from chip to chip, and with temperature and power-supply variations. It simply indicates the relative variations that might be found within a specific chip over the range of operating conditions.*

Typically, all delays will be less than their maximum, with some delays being disproportionately faster than others. The 70% rule describes the spread in the scaling factors; the delay that decreases the most will be no less than 70% of what it would have been if it had scaled in proportion to the delay that decreased the least. In particular, in a worst-case design where it is assumed that any delay might not have scaled at all, and remains at its maximum value, other delays will be no less than 70% of their maximum.

## Outputs

All XC3000/XC3100 FPGA outputs are true CMOS with n-channel transistors pulling down and p-channel transistors pulling up. Unloaded, these outputs pull rail-to-rail. Some additional ac characteristics of the output are listed in **Table 2**. **Figure 4** and **Figure 5** show output current/voltage curves for typical XC3000 and XC3100 devices.



**Figure 4: Output Current/Voltage Characteristics for XC3000, XC3000A, XC3100 and XC3100A Devices**

Output-short-circuit-current values are given only to indicate the capability to charge and discharge capacitive loads. In accordance with common industry practice for other logic devices, only one output at a time may be short circuited, and the duration of this short circuit to  $V_{CC}$  or ground may not exceed one second. Xilinx does not recommend a continuous output or clamp current in excess of 20 mA on any one output pin. The data sheet guarantees the outputs for no more than 4 mA at 320 mV to avoid problems when many outputs are sinking current simultaneously.

The active-High 3-state control (T) is the same as an active-Low output enable ( $\overline{OE}$ ). In other words, a High on the T-pin of an OBUFZ places the output in a high impedance state, and a Low enables the output. The same naming convention is used for TBUFs within the FPGA device.

## I/O Clocks

Internally, up to eight distinct I/O clocks can be used, two on each of the four edges of the die. While the IOB does not provide programmable clock polarity, the two clock lines serving an IOB can be used for true and inverted clock, and the appropriate polarity connected to the IOB. This does, however, limit all IOBs on that edge of the die to using only the two edges of the one clock.

**Table 2: Additional AC Output Characteristics**

AC Parameters	Fast*	Slow*
Unloaded Output Slew Rate	2.8 V/ns	0.5 V/ns
Unloaded Transition Time	1.45 ns	7.9 ns
Additional rise time for 812 pF	100 ns	100 ns
normalized	0.12 ns/pF	0.12 ns/pF
Additional fall time for 812 pF	50 ns	64 ns
normalized	0.06 ns/pF	0.08 ns/pF

\* Fast and Slow refer to the output programming option.

IOB latches have active-Low Latch Enables; they are transparent when the clock input is Low and are closed when it is High. The latch captures data on what would otherwise be the active clock edge, and is transparent in the half clock period before the active clock edge.

## Routing

### Horizontal Longlines

As shown in [Table 3](#), there are two horizontal Longlines (HLLs) per row of CLBs. Each HLL is driven by one TBUF for each column of CLBs, plus an additional TBUF at the left end of the Longline. This additional TBUF is convenient for driving IOB data onto the Longline. In general, the routing resources to the T and I pins of TBUFs are somewhat limited.

**Table 3: Number of Horizontal Longlines**

Part Name	Rows x Columns	CLBs	Horizontal Longlines	TBUFs per HLL
XC3020	8 x 8	64	16	9
XC3030	10 x 10	100	20	11
XC3042	12 x 12	144	24	13
XC3064	16 x 14	224	32	15
XC3090	20 x 16	320	40	17
XC3195	22 x 22	484	44	23

Optionally, HLLs can be pulled up at either end, or at both ends. The value of each pull-up resistor is 3-10 k $\Omega$ .

In addition, HLLs are permanently driven by low-powered latches that are easily overridden by active outputs or pull-up resistors. These latches maintain the logic levels on HLLs that are not pulled up and temporarily are not driven. The logic level maintained is the last level actively driven onto the line.

When using 3-state HLLs for multiplexing, the use of fewer than four TBUFs can waste resources. Multiplexers with four or fewer inputs can be implemented more efficiently using CLBs.

### Internal Bus Contention

XC3000 and XC4000 Series devices have internal 3-state bus drivers (TBUFs). As in any other bus design, such bus drivers must be enabled carefully in order to avoid, or at least minimize, bus contention. (Bus contention means that one driver tries to drive the bus High while a second driver tries to drive it Low).

Since the potential overlap of the enable signals is layout dependent, bus contention is the responsibility of the FPGA user. We can only supply the following information:

While two internal buffers drive conflicting data, they create a current path of typically 6 mA. This current is tolerable, but should not last indefinitely, since it exceeds our (conser-

vative) current density rules. A continuous contention could, after thousands of hours, lead to metal migration problems.

In a typical system, 10 ns of internal bus contention at 5 MHz would just result in a slight increase in  $I_{cc}$ .

$$16 \text{ bits} \times 6 \text{ mA} \times 10 \text{ ns} \times 5 \text{ MHz} \times 50\% \text{ probability} = 2.5 \text{ mA.}$$

There is a special use of the 3-state control input: When it is directly driven by the same signal that drives the data input of the buffer, i.e. when D and T are effectively tied together, the 3-state buffer becomes an “open collector” driver. Multiple drivers of this type can be used to implement the “wired-AND” function, using resistive pull-up.

In this situation there cannot be any contention, since the 3-state control input is designed to be slow in activating and fast in deactivating the driver. Connecting D to ground is an obvious alternative, but may be more difficult to route.

## Vertical Longlines

There are four vertical Longlines per routing channel: two general purpose, one for the global clock net and one for the alternate clock net.

## Clock Buffers

XC3000/XC3100 devices each contain two high-fan-out, low-skew clock-distribution networks. The global-clock net originates from the GCLK buffer in the upper left corner of the die, while the alternate clock net originates from the ACLK buffer in the lower right corner of the die.

The global and alternate clock networks each have optional fast CMOS inputs, called TCLKIN and BCLKIN, respectively. Using these inputs provides the fastest path from the PC board to the internal flip-flops and latches. Since the signal bypasses the input buffer, well-defined CMOS levels must be guaranteed on these clock pins.

To specify the use of TCLKIN or BCLKIN in a schematic, connect an IPAD symbol directly to the GCLK or ACLK symbol. Placing an IBUF between the IPAD and the clock buffer will prevent TCLKIN or BCLKIN from being used.

The clock buffer output nets only drive CLB and IOB clock pins. *They do not drive any other CLB inputs.* In rare cases where a clock needs to be connected to a logic input or a device output, a signal should be tapped off the clock buffer input, and routed to the logic input. This is not possible with clocks using TCLKIN or BCLKIN.

The clock skew created by routing clocks through local interconnect makes safe designs very difficult to achieve, and this practice is not recommended. In general, the fewer clocks that are used, the safer the design. High fan-out clocks should always use GCLK or ACLK. If more than two clocks are required, the ACLK net can be segmented into individual vertical lines that can be driven by PIPs at the top and bottom of each column. Clock signals routed through

local interconnect should only be considered for individual flip-flops.

## Power Dissipation

As in most CMOS ICs, almost all FPGA power dissipation is dynamic, and is caused by the charging and discharging of internal capacitances. Each node in the device dissipates power according to the capacitance in the node, which is fixed for each type of node, and the frequency at which the particular node is switching, which can be different from the clock frequency. The total dynamic power is the sum of the power dissipated in the individual nodes.

While the clock line frequency is easy to specify, it is usually more difficult to estimate the average frequency of other nodes. Two extreme cases are binary counters, where half the total power is dissipated in the first flip-flop, and shift registers with alternating zeros and ones, where the whole circuit is exercised at the clocking speed.

A popular assumption is that, on average, each node is exercised at 20% of the clock rate; a major EPLD vendor uses a 16-bit counter as a model, where the effective percentage is only 12%. Undoubtedly, there are extreme cases, where the ratio is much lower or much higher, but 15 to 20% may be a valid approximation for most normal designs. Note that global clock lines must always be entered with their real, and obviously well-known, frequency.

Consequently, most power consumption estimates only serve as guidelines based on gross approximations. Table 4 shows the dynamic power dissipation, in mW per MHz, for different types of XC3000 nodes. While not precise, these numbers are sufficiently accurate for the calculations in which they are used, and may be used for any XC3000/XC3100 device. Table 5 shows a sample power calculation.

**Table 4: Dynamic Power Dissipation**

	XC3020	XC3090	
One CLB driving three local interconnects	0.25	0.25	mW/MHz
One device output with a pF load	50	1.25	mW/MHz
One Global Clock Buffer and line	2.00	3.50	mW/MHz
One Longline without driver	0.10	0.15	mW/MHz

**Table 5: Sample Power Calculation for XC3020**

Quantity	Node	MHz	mW/MHz	mW
1	Clock Buffer	40	2.00	80
5	CLBs	40	0.25	50
10	CLBs	20	0.25	50
40	CLBs	10	0.25	100
8	Longlines	20	0.10	16
20	Outputs	20	1.25	500
				Total Power ~800

## Crystal Oscillator

XC3000 and XC3100 devices contain an on-chip crystal oscillator circuit that connects to the ACLK buffer. This circuit, Figure 5, comprises a high-speed, high-gain inverting amplifier with its input connected to the dedicated XTL2 pin, and its output connected to the XTL1 pin. An external biasing resistor, R1, with a value of 0.5 to 1 MΩ is required.

A crystal, Y1, and additional phase-shifting components, R2, C1 and C2, complete the circuit. The capacitors, C1 and C2, in series form the load on the crystal. This load is specified by the crystal manufacturer, and is typically 20 pF. The capacitors should be approximately equal: 40 pF each for a 20 pF crystal.

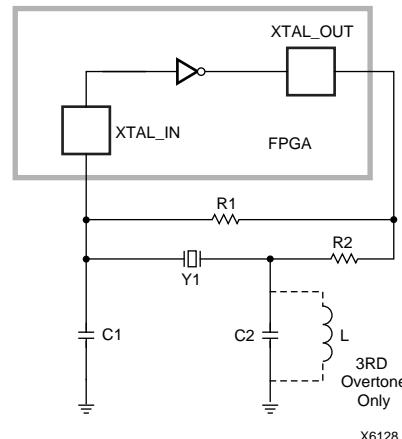
Either series- or parallel-resonant crystals may be used, since they differ only in their specification. Crystals constrain oscillation to a narrow band of frequencies, the width of which is <<1% of the oscillating frequency; the exact frequency of oscillation within this band depends on the components surrounding the crystal. Series-resonant crystals are specified by their manufacturers according to the lower edge of the frequency band, parallel-resonant crystals according to the upper edge.

The resistor R2 controls the loop gain and its value must be established by experimentation. If it is too small, the oscillation will be distorted; if it is too large, the oscillation will fail to start, or only start slowly. In most cases, the value of R2 is non-critical, and typically is 0 to 1 kΩ.

Once the component values have been chosen, it is good practice to test the oscillator with a resistor (~1 kΩ) in series with the crystal. If the oscillator still starts reliably, independent of whether the power supply turns on quickly or slowly, it will always work without the resistor.

For operation above 20 to 25 MHz, the crystal must be operated at its third harmonic. The capacitor C2 is replaced by a parallel-resonant LC tank circuit tuned to ~2/3 of the desired frequency, i.e., twice the fundamental frequency of the crystal. Table 6 shows typical component values for the tank circuit.

Crystal operation below 1 MHz is not supported. Low-frequency crystals have a high resonant impedance and require more gain than provided by the single stage inverter in the XC3000 devices. Low-frequency applications are usually also more power-conscious and would not accept the power consumption of the fast general-purpose Xilinx oscillator circuit. Inexpensive complete oscillator packages are often a better choice.



**Figure 5: Crystal Oscillator**

**Table 6: Third-Harmonic Crystal Oscillator Tank-Circuit**

Frequency (MHz)	LC Tank			R2 (Ω)	C1 (pF)
	L (μH)	C2 (pF)	Freq (MHz)		
32	1	60	20.6	430	23
35	1	44	24.0	310	23
49	1	31	28.6	190	23
72	1	18	37.5	150	12

### Crystal-Oscillator Considerations

There is nothing Xilinx-specific about the oscillator circuit. It's a wide-band inverting amplifier, as used in all popular microcontrollers. When a crystal and some passive components close the feedback path, this circuit becomes a reliable and stable clock source.

The path from XTAL2 to XTAL1 inside the LCA device is a single-stage inverting amplifier, which means it has a low-frequency phase response of 180°, increasing by 45° at the 3-dB frequency.

Input impedance is 10-15 pF, input threshold is CMOS, but dc bias must be supplied externally through a megohm resistor from XTAL1 to XTAL2.

Low-frequency gain is about 10, rolling off 3dB at 125 MHz.

Output impedance is between 50 and 100 Ω and the capacitance on the output pin is 10 to 15 pF.

Pulse response is a delay of about 1.5 ns and a rise/fall time of about 1.5 ns.

For stable oscillation,

- the loop gain must be exactly one, i.e., the internal gain must be matched by external attenuation, and
- the phase shift around the loop must be  $360^\circ$  or an integer multiple thereof. The external network must, therefore, provide  $180^\circ$  of phase shift.

A crystal is a piezoelectric mechanical resonator that can be modeled by a very high-Q series LC circuit with a small resistor representing the energy loss. In parallel with this series-resonant circuit is unavoidable parasitic capacitance inside and outside the crystal package, and usually also discrete capacitors on the board.

The impedance as a function of frequency of this whole array starts as a small capacitor at low frequencies (Figure 6). As the frequency increases, this capacitive reactance decreases rapidly, until it reaches zero at the series resonant frequency.

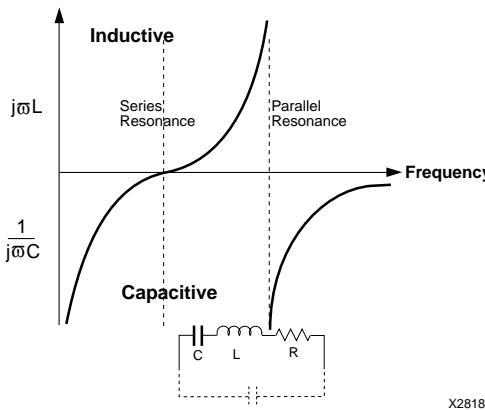


Figure 6: Reactance as a Function of Frequency

At slightly higher frequencies, the reactance is inductive, starting with a zero at series resonance, and increasing very rapidly with frequency. It reaches infinity when the effective inductive impedance of the series LC circuit equals the reactance of the parallel capacitor. The parallel resonance frequency is a fraction of a percent above the series-resonance frequency.

Over this very narrow frequency range between series and parallel resonance, the crystal impedance is inductive and changes all the way from zero to infinity. The energy loss represented by the series resistor prevents the impedance from actually reaching zero and infinity, but it comes very close.

Microprocessor- and FPGA-based crystal oscillators all operate in this narrow frequency band, where the crystal impedance can be any inductive value. The circuit oscillates at a frequency where the attenuation in the external

circuit equals the gain in the FPGA device, and where the total phase shift, internal plus external, equals  $360^\circ$ .

**Figure 7** explains the function. At the frequency of oscillation, the series-resonant circuit is effectively an inductor, and the two capacitors act as a capacitive voltage divider, with the center-point grounded. This puts a virtual ground somewhere along the inductor and causes the non-driven end of the crystal to be  $180^\circ$  out of phase with the driven end, which is the external phase shift required for oscillation. This circuit is commonly known as a Pierce oscillator.

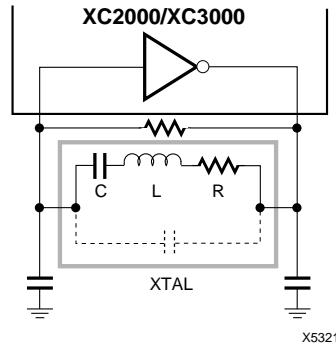


Figure 7: Pierce Oscillator

### Practical Considerations

- The series resonance resistor is a critical parameter. To assure reliable operation with worst-case crystals, the user should experiment with a discrete series resistor roughly equal to the max internal resistance specified by the crystal vendor. If the circuit tolerates this additional loss, it should operate reliably with a worst-case crystal without the additional resistor.
- The two capacitors affect the frequency of oscillation and the start-up conditions. The series connection of the two capacitors is the effective capacitive load seen by the crystal, usually specified by the crystal vendor.
- The two capacitors also determine the minimum gain required for oscillation. If the capacitors are too small, more gain is needed, and the oscillator may be unstable. If the capacitors are too large, oscillation is stable but the required gain may again be higher. There is an optimum capacitor value, where oscillation is stable, and the required gain is at a minimum. For most crystals, this capacitive load is around 20 pF, i.e., each of the two capacitors should be around 40 pF.
- Crystal dissipation is usually around 1 mW, and thus of no concern. Beware of crystals with “drive-level dependence” of the series resistor. They may not start up. Proper drive level can be checked by varying Vcc. The frequency should increase slightly with an increase in Vcc. A decreasing frequency or unstable amplitude indicate an over-driven crystal. Excessive swing at the

XTAL2 input results in clipping near Vcc and ground. An additional 1 to 2 k $\Omega$  series resistor at the XTAL1 output usually cures that distortion problem. It increases the amplifier output impedance and assures additional phase margin, but results in slower start-up.

- Be especially careful when designing an oscillator that must operate near the specified max frequency. The circuit needs excess gain at small signal amplitudes to supply enough energy into the crystal for rapid start-up. High-frequency gain may be marginal, and start-up may be impaired.
- Keep the whole oscillator circuit physically as compact as possible, and provide a single ground connection. Grounding the crystal can is not mandatory but may improve stability.

### **Series Resonant or Parallel Resonant?**

Crystal manufacturers label some crystals as series-resonant, others as parallel-resonant, but there really is no difference between these two types of crystals, they all operate in the same way. Every crystal has a series resonance, where the impedance of the crystal is extremely low, much lower than at any other frequency. At a slightly higher frequency, the crystal is inductive and in parallel resonance with the unavoidable stray capacitance or the deliberate capacitance between its pins.

The only difference between the two types of crystal is the manufacturer's choice of specifying either of the two frequencies. If series resonance is specified, the actual frequency of oscillation is a little higher than the specified value. If parallel resonance is specified, the frequency of oscillation is a little lower. In most cases, these small deviations are irrelevant.

## **CCLK Frequency Variation**

The on-chip R-C oscillator that is brought out as CCLK also performs several other internal functions. It generates the power-on delay,  $2^{16} = 65,536$  periods for a master,  $2^{14} = 16,384$  periods for a slave or peripheral device. It generates the shift pulses for clearing the configuration array, using one clock period per frame, and it is the clock source for several small shift registers acting as low-pass filters for a variety of input signals.

The nominal frequency of this oscillator is 1 MHz with a max deviation of +25% to -10%. The clock frequency, therefore, is between 1.25 MHz and 0.5 MHz. In the XC4000 family, the 1-MHz clock is derived from an internal 8-MHz clock that also can be used as CCLK source.

Xilinx circuit designers make sure that the internal clock frequency does not get faster as devices are migrated to smaller geometries and faster processes. Even the newest

and fastest Xilinx FPGA is compatible with the oldest and slowest device ever manufactured. The CCLK frequency is fairly insensitive to changes in V<sub>CC</sub>, varying only 0.6% for a 10% change in V<sub>CC</sub>. It is, however, very temperature dependent, increasing 40% as the temperature drops from 25°C to -30°C, (Table 7.)

**Table 7: Typical CCLK Frequency Variation**

V <sub>CC</sub>	Temp	Frequency
4.5 V	25°C	687 kHz
5.0 V	25°C	691 kHz
5.5 V	25°C	695 kHz
4.5 V	-30°C	966 kHz
4.5 V	+130°C	457 kHz

## **CCLK Low-Time Restriction**

When used as an input in Slave Serial and Readback modes, CCLK does not tolerate a Low time in excess of 5  $\mu$ s. For very low speed operation, the CCLK High time can be stretched to any value, but the Low time must be kept short. XC4000 and XC5200 devices do not have this restriction.

## **Battery Back-up**

Since SRAM-based FPGAs are manufactured using a high-performance low-power CMOS process, they can preserve the configuration data stored in the internal static memory cells even during a loss of primary power. This is accomplished by forcing the device into a low-power non-operational state, while supplying the minimal current requirement of V<sub>CC</sub> from a battery.

Circuit techniques used in XC3100, XC4000 and XC5200 devices prevent I<sub>CC</sub> from being reduced to the level need for battery back-up. Consequently, battery back-up should only be used for XC2000, XC2000L, XC3000, XC3000A and XC3000L devices.

There are two primary considerations for battery backup which must be accomplished by external circuits.

- Control of the Power-Down (PWRDWN) pin
- Switching between the primary V<sub>CC</sub> supply and the battery.

Important considerations include the following.

- Insure that PWRDWN is asserted logic Low prior to V<sub>CC</sub> falling, is held Low while the primary V<sub>CC</sub> is absent, and returned High after V<sub>CC</sub> has returned to a normal level. PWRDWN edges must not rise or fall slowly.
- Insure "glitch-free" switching of the power connections to the FPGA device from the primary V<sub>CC</sub> to the battery and back.
- Insure that, during normal operation, the FPGA V<sub>CC</sub> is maintained at an acceptable level, 5.0 V  $\pm$  5% ( $\pm$ 10% for Industrial and Military).

Figure 8 shows a power-down circuit developed by Shel Epstein of Epstein Associates, Wilmette, IL. Two Schottky diodes power the FPGA from either the 5.2 V primary supply or a 3 V Lithium battery. A Seiko S8054 3-terminal power

monitor circuit monitors  $V_{CC}$  and pulls  $\overline{PWRDWN}$  Low whenever  $V_{CC}$  falls below 4 V.

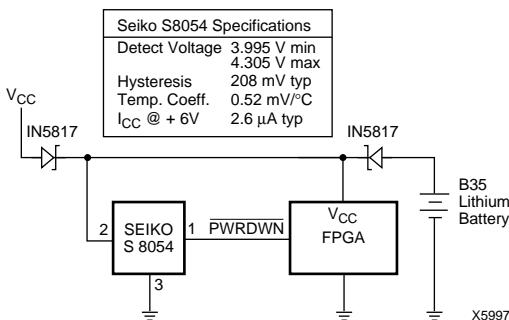


Figure 8: Battery Back-up Circuit

## Powerdown Operation

A Low level on the PWRDWN input, while  $V_{CC}$  remains higher than 2.3 V, stops all internal activity, thus reducing  $I_{CC}$  to a very low level:

- All internal pull-ups (on Long lines as well as on the I/O pads) are turned off.
- The crystal oscillator is turned off.
- All package outputs are three-stated.
- All package inputs ignore the actual input level, and present a High to the internal logic.
- All internal flip-flops or latches are permanently reset.
- The internal configuration is retained.
- When PWRDWN is returned High, after  $V_{CC}$  is at its nominal value, the device returns to operation with the same sequence of buffer enable and D/P as at the completion of configuration.

## Things to Remember

Powerdown retains the configuration, but loses all data stored in the device. Powerdown three-states all outputs and ignores all inputs. No clock signal will be recognized, and the crystal oscillator is stopped. All internal flip-flops and latches are permanently reset and all inputs are interpreted as High, but the internal combinatorial logic is fully functional.

## Things to Watch Out For

Make sure that the combination of all inputs High and all internal flip-flop outputs Low in your design will not generate internal oscillations or create permanent bus contention

by activating internal bus drivers with conflicting data onto the same Longline. These two situations are farfetched, but they are possible and will result in considerable power consumption. It is quite easy to simulate these conditions since all inputs are stable and the internal logic is entirely combinatorial, unless latches have been made out of function generators.

During powerdown, the  $V_{CC}$  monitoring circuit is disabled. It is then up to the user to prevent  $V_{CC}$  dips below 2.3 V, which would corrupt the stored configuration.

During configuration, the PWRDWN pin must be High, since configuration uses the internal oscillator. Whenever  $V_{CC}$  goes below 4 V, PWRDWN must already be Low in order to prevent automatic reconfiguration at low  $V_{CC}$ . For the same reason,  $V_{CC}$  must first be restored to 4 V or more, before PWRDWN can be made High.

PWRDWN has no pull-up resistor. A pull-up resistor would draw supply current when the pin is Low, which would defeat the idea of powerdown, where  $I_{CC}$  is only microamperes.

## Configuration and Start-up

### Start-Up

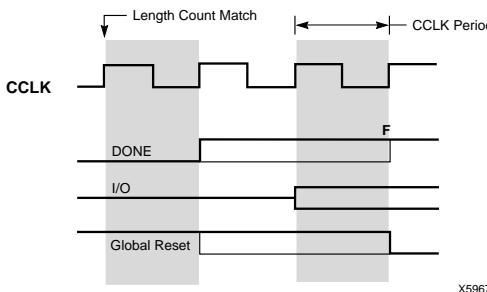
Start-up is the transition from the configuration process to the intended user operation. This means a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic "wakes up" gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 10 describes Start-up timing for the XC3000 families in detail.

DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 11, but the designer can modify it to meet particular requirements.

Until the chip goes active after configuration, all I/O pins not involved in the configuration process remain in a high-impedance state with weak pull-up resistors; all internal flip-flops and latches are held reset. Multiple FPGA devices hooked up in a daisy chain will all go active simultaneously



**Figure 9: Start-up Timing**

on the same CCLK edge. This is well documented in the data sheets.

Not documented, however, is how the internal combinatorial logic comes alive during configuration: As configuration data is shifted in and reaches its destination, it activates the logic and also "looks at" the IOB inputs. Even the crystal oscillator starts operating as soon as it receives its configuration data. Since all flip-flops and latches are being held reset, and all outputs are being held in their high-impedance state, there is no danger in this "staggered awakening" of the internal logic. The operation of the logic prior to the end of configuration is even useful; it ensures that clock enables and output enables are correctly defined before the elements they control become active.

Once configuration is complete, the FPGA device is activated. This occurs on a rising edge of CCLK, when all outputs and clocks that are enabled become active simultaneously. Since the activation is triggered by CCLK, it is an asynchronous event with respect to the system clock. To avoid start-up problems caused by this asynchronism, some designs might require a reset pulse that is synchronized to the system clock.

The circuit shown in Figure 10 generates a short Global Reset pulse in response to the first system clock after the end of configuration. It uses one CLB and one IOB, and also precludes the use of the LDC pin as I/O.

During Configuration, LDC is asserted Low and holds the D-input of the flip-flop High, while Q is held Low by the internal reset, and RESET is kept High by internal and external pull-up resistors. At the end of configuration, the LDC pin is

unasserted, but D remains High since the function generator acts as an R-S latch; Q stays Low, and  $\overline{\text{RESET}}$  is still pulled High by the external resistor. On the first system clock after configuration ends, Q is clocked High, resetting the latch and enabling the output driver, which forces  $\overline{\text{RESET}}$  Low. This resets the whole chip until the Low on Q permits  $\overline{\text{RESET}}$  to be pulled High again.

The whole chip has thus been reset by a short pulse instigated by the system clock. No further pulses are generated, since the High on  $\overline{LDC}$  prevents the R-S latch from becoming set.

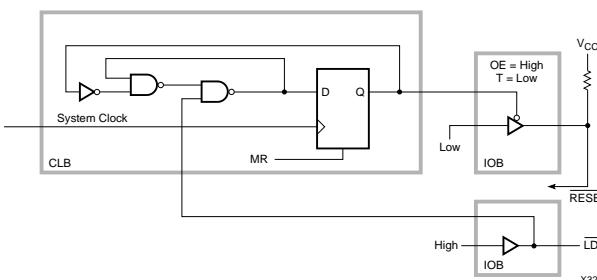
## Beware of a Slow-Rising XC3000 Series RESET Input

It is a wide-spread habit to drive asynchronous `RESET` inputs with a resistor-capacitor network to lengthen the reset time after power-on. This can also be done with Xilinx FPGAs, but the user should question the need, and should beware of certain avoidable problems.

Xilinx FPGAs contain an internal voltage-monitoring circuit, and start their internal housekeeping operation only after  $V_{CC}$  has reached  $\sim 3.5$  V. The internal housekeeping and configuration memory clearing operation then takes between about 10 and 100 ms, depending on configuration mode and processing variations. Any RC delay shorter than 40 ms for a device in master configuration mode, or shorter than 10 ms for a device in slave configuration mode, is clearly redundant.

A significantly longer RC delay can be used to hold off configuration. Without the use of an external Schmitt trigger circuit, the rise time on the **RESET** input will be very slow, and is likely to cross the threshold of ~1.4 V several times, due to external or internal noise. This can cause the FPGA to start configuration, then immediately abort it, then start it again, after having automatically cleared the configuration memory once more.

This is no problem for the FPGA, but it requires that the source of configuration data, especially an XC1700 serial PROM, be reset accordingly. This is another reason to use the INIT output of the lead FPGA, instead of LDC, to drive the RESET input of the XC1700 serial PROMs.



**Figure 10: Synchronous Reset**





## FPGA Configuration Guidelines

XAPP 090 November 24, 1997 (Version 1.1)

Application Note By Peter Alfke

### Summary

These guidelines describe the configuration process for all members of the XC2000, XC3000, XC4000 and XC5200 FPGA devices and their derivatives. The average user need not understand or remember all these details, but should refer to the debugging hints when problems occur.

The XC2000-, XC3000-, XC4000- and XC5200-family FPGAs share a basic configuration concept, and can be combined in a common configuration bitstream, but there are also small differences among the four families as described below.

Following their initial power-on configuration-memory initialization, these Xilinx FPGAs are configured by a serial configuration bitstream. The byte-parallel configuration modes just activate an internal parallel-to-serial converter, and then use the serial bitstream internally. (Express mode in the XC5200 configures eight bits in parallel, but this mode is not covered in this application note.) The software generates a bitstream that starts with a 40-bit header (48-bit header for XC5200), see Figure 1.

Each device uses a few of the leading “ones” to prepare for configuration, then detects the 0010 pattern and stores the following 24 bits as a length-count value in an internal register. The content of this register is continuously compared against a running counter that increments on every rising CCLK edge. CCLK is either an output (in Master and Asynchronous Peripheral modes) or an input (in Slave Serial and Synchronous Peripheral modes). In all modes, even in Master Serial, it is the externally observable Low-to-High transition on the CCLK pin that causes the internal action. Every CCLK rising edge that occurs while INIT and RESET are High is counted, even during the preamble. Note that XC2000 and XC3000 use quasi-static circuitry which imposes a 5 ms max limit on the CCLK Low time, while XC4000 and XC5200 are completely static and have no max CCLK time limit. This is, of course, only of interest in XC2000 and XC3000 Slave Serial mode, where CCLK is generated by the user.

While it is permissible, although not meaningful, to modify the number of leading ones by adding additional ones, or subtracting up to four ones, this would inevitably affect the number of CCLK pulses received by the counter, and thus change the moment when the internal counter is equal to the value stored in the length-count register. ***Don't add or delete preamble-leading ones!***

Each device passes the incoming header, including the length-count value, on to the DOUT pin, delayed by half a CCLK period, i.e. the bits are clocked out on a falling CCLK edge. In this way, the header is passed on to all devices that might be connected in a daisy-chain. After the length-count data has been passed on, DOUT goes active High and stays High until the device has been filled with the appropriate number of configuration frames. After that, DOUT again passes all incoming configuration data on to other devices that might be part of the daisy chain.

DOUT is thus the best observation point to see whether the configuration process has started properly.

Immediately following the header, configuration data is received, formatted in a device-specific sequence of frames. Each frame starts with a single “zero” as start bit (XC5200 starts with a byte of seven leading “ones” and a single trailing “zero”), followed by a device-specific number of configuration bits per frame, followed by three “ones” as stop bits (XC2000, XC3000) or, in XC4000 and XC5200, by four bits that are either 0110, or four bits of a running 16-bit CRC error-checking code. The choice is made in the bit-stream generator, where the default is “CRC disabled”. The header is excluded from the CRC calculation.

Each frame is physically shifted into a serial shift register that had been preset to all ones. When the zero start bit hits the far end of this shift register, the data frame is transferred in parallel into the configuration memory, as addressed by the position of an internal token or pointer. The three stop or four error-check bits provide ample time for this transfer, even at a 10 MHz CCLK rate. After this transfer, the shift-in procedure continues with the following frame. Note that there is no counter for the number of bits in the frame nor for the number of frames. The operation is self-synchronized by detecting the presence of a start bit at the far end of the shift register, and by moving the frame pointer.

11111111	0010	(MSB) 24-Bit Length Count (LSB)	1111	Data
X5553				

Figure 1: 40-Bit Header

Each Xilinx FPGA requires a number of configuration bits that is device-dependent, but independent of the configuration content, and independent of the configuration mode. The number of configuration bits per device ranges from 12,038 for the XC2064 to 1,924,992 for the XC4085XL, approximately 20 bits per available user gate. Exact values are listed in the specific family data sheets.

## Protection Against Data or Format Errors

The serial configuration scheme has proven reliable in thousands of designs and millions of devices, but there have been cases where an erroneous bitstream was loaded accidentally. The original XC2000 and XC3000 devices provide no effective protection against this type of error. If long enough, any random sequence of 0s and 1s will configure such a device. This inevitably takes additional CCLK pulses, more than specified in the length-count value. This means that the CCLK counter already matches the length-count value before the last FPGA in the chain is filled. This comparison is, therefore, ignored, and an additional ~16 million CCLK pulses are required to roll the 24-bit length counter and finish the configuration. Such a configuration will, of course, be wrong and might result in excessive power consumption due to contentions.

XC3000A, XC3100A, XC3000L and XC3100L devices use a simple and effective method to protect against erroneous configuration files or against loss (or gain) of CCLK pulses:

All Xilinx FPGA devices recognize a new frame when its leading zero reaches the end of the shift register. XC2000, XC3000, and XC3100 devices do not check for the presence of valid stop bits, but XC3000A/XC3100A/XC3000L/XC3100L devices always check whether the three bits at the end of the defined frame length are 111. If this check fails, INIT is pulled Low and the internal configuration is stopped, although a master CCLK keeps running. The user must recognize this state and start a new configuration by applying a >6 µs Low level on RESET.

This simple check does not protect against single-bit random errors, but it offers almost 100% protection against erroneous configuration files, defective configuration data sources, synchronization errors between configuration source and FPGA, as well as PC-board defects, such as broken lines or solder bridges.

The XC4000 and XC5200 devices use, optionally, four bits of a running 16-bit cyclic redundancy check code at the end of each frame, combined with additional CRC bits at the end of the bit stream. These error-detecting CRC codes provide excellent protection against errors, even those that do not change the frame structure. When an error is detected, INIT goes Low and stays Low until the user initiates a reconfiguration. A master device does, however, continue generating CCLK pulses and even incrementing or decrementing the parallel PROM address.

## Daisy-Chain Operation

Multiple FPGAs can be configured by a single concatenated bitstream. The device daisy chain is formed by connecting DOUT to the next device's DIN, and connecting all CCLK pins in parallel. DOUT goes active on a falling clock edge, and DIN accepts data on the subsequent rising clock edge. Each DOUT-to-DIN connection adds one extra bit of delay to the bitstream. Since the header is passed through all devices, they all receive the same header information delayed by one bit per device, but all devices maintain perfect synchronism between their CCLK counters, since all receive the same CCLK.

Xilinx recognizes the need for all devices in a daisy chain to finish configuration and begin user operation simultaneously, as a result of one common CCLK edge. Therefore, all devices in a daisy-chain need a common timing reference. They cannot rely on the start pattern received through the pipelined chain, but must all count the common CCLK pulses exactly the same way. This explains the importance of precise configuration clocking, and the danger of reflections and ringing on the CCLK line.

## Start-Up Procedure

During configuration, all outputs that are not involved in the configuration process are 3-stated, although the crystal oscillator circuit is activated as soon as possible. All internal flip-flops and latches are held reset (set or reset in XC4000), and the DONE output is held Low.

At the end of configuration, these three conditions must change: As shown in detail in Figure 2, the various families offer different options:

**XC2000** has no options; the I/Os go active one CCLK period after length-count match. One CCLK period later, DONE goes active and the global reset is released.

**XC3000** makes the I/Os go active two CCLK periods after length-count match; but DONE and the release of the global reset can each occur either one CCLK period before or after the I/Os go active. The default is "early DONE and late release of the global reset". This makes the outputs go active while the internal logic is still held reset. The other option, "early release of global reset", lets the internal logic be clocked out of its reset state before the outputs go active.

Normally, there is no defined timing relationship between the last configuration events triggered by the rising edge of CCLK, and the subsequent events that are controlled by the system clock. The user must be aware of the potential timing problems of this asynchronous relationship between the two clocks. See the XC4000/XC5200 solution described below.

**XC4000** and **XC5200** have more options for the relative timing of I/Os, DONE and GSR, the release of the global set or reset.

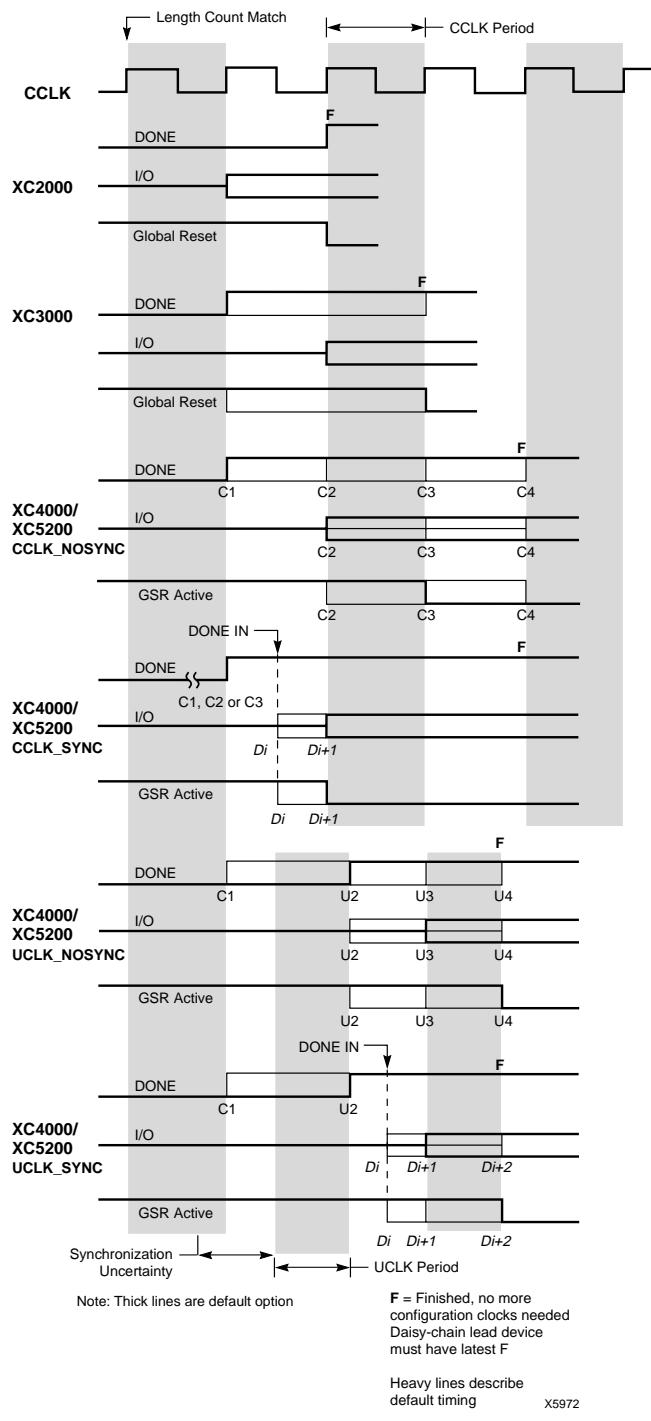


Figure 2: Start-up Timing

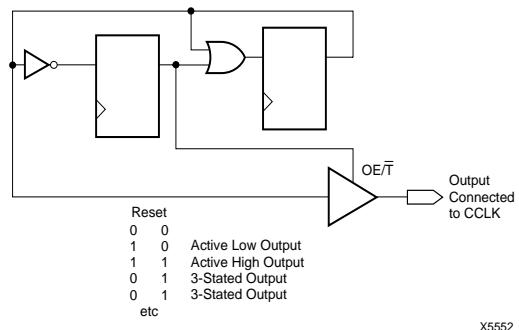
These families can also use DONE as an input to hold off the activation of the I/Os and the release of GSR, until DONE is no longer pulled Low. The change then takes place either immediately upon the release of DONE, or as a result of the next CCLK rising edge. When all DONE pins in a daisy chain are interconnected, this start-up mode guarantees that all devices in the chain go active only when all of them have reached the DONE state, an additional protection against potential configuration errors.

XC4000 and XC5200 can also be configured to employ the system (user) clock instead of CCLK, again either using DONE as an output, or as a bidirectional pin.

The user clock provides a properly synchronized and race-free transition from the end of configuration to the beginning of user operation. The unspecified on-chip delay in the release of GSR (about 100 ns in XC4013E) requires some caution, however, when using a high clock frequency for configuration.

While devices from different families can be arbitrarily interspersed in a daisy-chain, there is one restriction: the lead device must belong to the highest-numbered family in the chain. If the chain contains XC5200 devices, the lead device cannot be XC4000, XC3000 or XC2000; if the chain contains XC4000 devices, the lead device cannot be XC3000 or XC2000; if the chain contains XC3000, then the lead device cannot be XC2000. The reason is shown in Figure 2. Since all devices in the chain store the same length-count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge. The master device then generates additional CCLK pulses until it reaches its finish point F. As shown in Figure 2, the different families generate and require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device has not really finished its configuration process, although DONE may have gone High, the outputs have become active, and the internal reset has been released. For XC4000 and XC5200, not reaching F means that READBACK cannot be initiated, and most boundary scan instructions cannot be used. The limitation in daisy-chain order has been criticized by designers who want to use an inexpensive lead device in Peripheral Mode, and save the more precious XC4000 I/O pins. Here is a solution for that case (Figure 3):

One CLB and one IOB in the lead XC3000 device are used to generate the additional CCLK pulse required by the XC4000 devices. When the lead device releases its internal reset signal, the 2-bit shift register starts responding to its clock input, and it generates an active Low output signal for the duration of one clock period. An external connection between this IOB pin and the CCLK pin thus creates the extra CCLK pulse. This solution requires one CLB, one IOB and pin, and an internal clock source with a frequency of up to 5 MHz. Obviously, the XC3000 lead device must be con-



**Figure 3: Additional CCLK-Pulse Generator**

figured with late internal reset, which happens to be the default option.

## Configuration Modes

There are six different configuration modes, hardware-selected by applying logic levels to the three mode inputs, M0, M1, and M2. The six modes are: Master Serial, Master Parallel Up, Master Parallel Down, Synchronous Peripheral (XC4000 and XC5200 only), Asynchronous Peripheral, and Slave Serial. A seventh mode, Express Mode, is only available in XC5200 devices, and is not described here.

In **Master** modes, the FPGA addresses an external PROM or EPROM storage device, and reads data from it. No additional timing or control signals are used.

In **Peripheral** mode, the FPGA accepts byte-wide data (bit-serial in XC2000), and interacts with the source of data, usually a microprocessor, with a Ready/Busy handshake.

In **Slave** mode, the FPGA receives bit-serial data and a clock from an external data and timing source, either from a microprocessor, or from the lead device in an FPGA-daisy chain.

The modes are selected by putting the appropriate logic levels on the three mode inputs, M0, M1, and M2 prior to the beginning of configuration. These three pins can be hardwired to V<sub>CC</sub> or Ground, but they can then never be used as user I/O. It is better to force a mode pin Low with a 3 kΩ pull-down resistor to ground, acting against the 20 to 100 kΩ internal pull-up resistor, and to rely on the built-in pull-up resistor to establish a High level on the M1, M2 mode pins, but use a 50 kΩ external pull-up resistor on M0. This eliminates the restrictions on using mode pins for user logic or readback.

When mode pin levels are driven by external logic, these levels must be established very soon after power-up. Establishing a mode level too late might eliminate the extra master power-on delay that makes a master wait for slave devices to be ready after power-on. Delaying mode levels until the beginning of configuration will obviously cause the

configuration to fail. Note that some CPLD devices have surprisingly long power-up delays. Be very careful when controlling mode levels in any creative way.

## Selecting the Best Configuration Mode

The selection of the most appropriate configuration mode is influenced by many factors, like

- the need for interface simplicity,
- the need for rapid configuration,
- the need for multiple configuration sources,
- the availability of a microprocessor-based configuration driver.

The simplest interface is Master Serial, using only two FPGA pins, CCLK and DIN, and no external timing or control signals.

The fastest configuration mode is Slave Serial or XC4000/XC5200 Synchronous Peripheral. In these modes, the user can supply a well-defined CCLK frequency of up to 10 MHz for 5-Volt devices. Only Express mode can be faster than that. For prototyping and rapid configuration change, the PC can configure the FPGA directly in Slave Serial mode, using the Xilinx-provided Download Cable or XChecker.

Multiple configuration codes are most conveniently stored in a microprocessor memory, using Peripheral mode to configure the FPGA. Peripheral mode also offers the greatest flexibility for field upgrades. New files can be supplied via diskette or modem, and can be downloaded by the microprocessor.

## When Configuration Fails

### General Debugging Hints for all Families

If the DONE output does not go High, there are several things to check.

- Checking all supply and configuration-related pins with an oscilloscope or logic analyzer can reveal wiring errors, bad socket pins, noisy ground, noisy CCLK, a serial configuration PROM's V<sub>PP</sub> pin not connected to V<sub>CC</sub>, PWRDWN not pulled High, poor or noisy RESET, missing pull-up resistors on DONE (or INIT in the XC3000), bad levels on mode pins, etc. Check all pins: Any dc voltage between 0.5 V and 3.0 V is a sign of serious trouble.
- Monitor the DOUT pin of the lead device, i.e. the FPGA that is either configured alone, or forms the beginning of a daisy chain. At the start of configuration, you should see the 40 (or 48)-bit header shown in Figure 1. After this sequence, the DOUT pin remains High until the device has received all its data. Then, the device becomes transparent and passes additional data (provided there is a daisy chain) through the DOUT pin to the Slave devices. If you don't see this pattern, you have a gross error somewhere. Check the following items:

- If INIT going Low again after configuration start indicates a configuration bitstream or framing error.
- If RESET is used to delay configuration, make sure it has a rise time of <100 ns and that it is glitch-free.
- Ringing on the CCLK line, caused by pc-board reflections, can result in spurious double-clocking and loss of frame synchronization in the FPGA.
- Configuration functions can be disrupted by signal contention between configuration inputs and the FPGA user outputs which become active at the end of configuration. This change is indicated by I/O pins going active and HDC/LDC no longer at their configuration levels. Contention can be avoided by rearranging pin-outs, maintaining additional 3-state control of user-I/O outputs, or matching start-up output levels to the configuration input levels on inputs other than chip-select. As a last resort, it is also possible to use a series resistor (1-10 kΩ) to provide isolation between conflicting signal sources that could occur after configuration is complete.
- If an FPGA heats up significantly, this is usually the result of applying the wrong bitstream, e.g. the bitstream for a different device, causing contention. Legitimate bitstreams have been screened by the Design Rule Checker software, and are guaranteed free of inherent contention problems, provided the configuration is loaded into the designated device. The user can obviously still cause contention on internal Longlines and on connections outside the device.
- During reprogramming, user logic must generate a time-out that insures all devices have completed the Clear cycle before any configuration data is sent.
- Removing the FPGA supply voltage while externally powered signals continue to drive input pins, might keep the FPGA V<sub>CC</sub> pins at a 0.5-to-2.0 V level, which can leave the FPGA in an invalid state. The FPGA input-protection diodes are there to clamp input-voltage excursions to the two supply connections. When the FPGA supply voltage falls more than 0.5 V below an active input signal, this input signal will supply degenerate V<sub>CC</sub> levels. If the input signals are not current-limited, the FPGA inputs can even be damaged by the excessive input current.
- If extraneous CCLK pulses are applied after Clear but before the beginning of the header, they are counted internally, and the internal clock count will then become equal to the stored length-count value before the configuration data is completely loaded. In this case, the DONE output does not become active until the clock counter equals length count a second time. This requires 2<sup>24</sup> extra clocks, about 20 s at the typical rate of 0.7 MHz, or about 2 seconds at the nominally 8-MHz fastest CCLK rate. Whenever configuration takes several or many seconds, this is due to a mismatch between length count and the number of CCLK pulses

- received.
- XChecker or the XACT Download Cable provide an alternate method of configuration to verify configuration data and to isolate wiring errors, such as interchanged or inverted configuration data or control signals.
- Try a different device. Although the chips are 100% factory-tested, an individual device might have been damaged after the test.

## General Debugging Hints for the XC2000 and XC3000 Families

- An undefined (floating) or active Low PWRDWN during configuration can disturb the operation. A Low level on PWRDWN immediately before the start of configuration causes problems in XC2000, forces XC3000 into Slave mode, but is acceptable in XC3000A and L.
- In the XC2000 and XC3000 families, the configuration-clock input signal drives quasi-static circuitry that does not function correctly with a Low time of more than 5 ms.
- At power-up, make sure  $V_{CC}$  rises in 25 ms or less. If this cannot be guaranteed, hold RESET active on the FPGAs and on the serial PROMs until  $V_{CC}$  has reached 4.5 V.
- A slowly rising or noisy RESET can cause multiple FPGAs to get out of synchronization. Always debounce reset switches.

## General Debugging Hints for the XC4000 and XC5000 Families

- At power-up, make sure  $V_{CC}$  rises in 25 ms or less. If this cannot be guaranteed, hold PROGRAM or INIT active Low on the FPGAs and hold the serial PROMs reset until  $V_{CC}$  has reached 4.5 V.
- The boundary scan input pins are active during configuration, even if boundary scan is not used in the design. Toggling TCK, TMS and TDI during configuration might send the device into EXTEST mode, which interferes with configuration. Keeping at least one of these three inputs continuously High during configuration avoids this problem.

## Additional Mode-Specific Debugging Hints for All Families

### Master Parallel Up and Down Mode

- Review the general debugging hints.
- Check that the PROM data pins are connected to the FPGA input pins D0-D7. Check that the PROM address pins are connected to the FPGA output pins A0-A15. Verify that all these connections are in the right order. Monitor the FPGA pins, not the socket pins. Make sure the socket is good.
- If the PROM is dedicated to the FPGA, the CS and OE PROM inputs should be driven from the DONE or LDC

FPGA output.

- Verify that the FPGA is sending addresses to the PROM. If it is not, check the FPGA mode pins.

M0 = 0, M1 = 0, M2 = 1 for Master Parallel Up  
M0 = 0, M1 = 1, M2 = 1 for Master Parallel Down

Make sure  $V_{CC}$ , RESET and PWRDWN are close to  $V_{CC}$  and all ground pins are at 0 V.

- Check that the PROM is receiving addresses and is sending out data. If it is not, check that the PROM is enabled and has  $V_{CC}$  and ground connected, and verify that the PROM is programmed with the correct data.
- Check for contention between the PROM address or data pins and other signals on the board.
- Check that the FPGA is addressing the correct memory segment. In Master Parallel Up mode, the FPGA starts at address 0000 hex and counts up; in Master Parallel Down mode it starts at address FFFF hex (3FFFF hex in XC4000) and counts down. If the PROM requires different addressing, that must be taken care of by external hardware.
- Check for ringing and noise on address and data lines.
- Make sure the data in the PROM is correct. You can check it against the Rawbits file.

### Master Serial Mode

- Review the general debugging hints.
- Verify that the FPGA is generating a clock signal on its CCLK pin and that this signal is reaching the CLK pin of the XC1700-series Serial-Configuration PROM. If it is not, check the mode pins.

M0 = 0, M1 = 0, M2 = 0 for Master Serial mode

- Verify that the XC1700-series Serial Configuration PROM is sending data. If it is not, check that power and ground are applied to the Serial PROM, and  $V_{PP}$  is connected to  $V_{CC}$ .

### Do Not Let the $V_{PP}$ Pin Float

A floating  $V_{PP}$  pin results in temperature-dependent operation, the most notorious cause of unreliable configuration.

- Check that the DATA pin of the Serial PROM is connected to the DIN pin of the FPGA, and that the PROM is enabled with CE Low and OE active. Note that the OE/RESET pin is programmable for either polarity. Check whether this pin is driven from the INIT output. This is the preferred method of guaranteeing SPROM reset.
- Verify that the PROM is programmed with the correct data.
- At power-up, make sure  $V_{CC}$  rises from 2.0 V to 4.5 V in

- less than 25 ms. If it does not, hold the FPGA RESET and the PROM RESET active until  $V_{CC}$  reaches 4.5 V. A typical result of a slow  $V_{CC}$  rise time is that the FPGA sends out CCLK continuously, the CEO pin on the PROM(s) goes Low, but the DONE pin never goes High.
- If you abort configuration by asserting XC3000 RESET or by pulling XC4000/XC5000 PROGRAM Low, you must also reset the serial PROM by asserting its RESET. This occurs automatically if the SROM is reset from INIT.

### **Asynchronous Peripheral Mode**

- Review the general debugging hints.
- Check the mode pin levels.

$M0 = 1, M1 = 0, M2 = 1$  for Peripheral mode

- Use an external 1 kilohm resistor from READY/BUSY pin to ground. On power-up, before the FPGA has interrogated the mode lines, this prevents the pin from being pulled High by its internal pull-up, which would give an early erroneous READY signal.
- Verify that the FPGA is receiving data at its input pin(s) and that it is receiving valid Write-Strobe and Chip-Select signals. If not, check the device driving the FPGA. Make sure that these signals meet the timing requirements listed in the product family documentation. XC3000 Family: Check that the minimum Write-Strobe active time ( $T_{CA}$  min = 100 ns) is met and observe the RDY/BUSY signal. XC2000 Family: Be sure maximum and minimum Write-Strobe active times ( $T_{CA}$  max = 5.0 ms, min = 0.25 ms) are met.
- Make sure that the FPGA is ready to receive data. XC3000 Family: On power up, make sure that the INIT pin has gone High, or wait at least 34 ms before you begin sending data to the FPGA. Make sure that the RDY/BUSY signal is High before sending each data byte. XC2000 Family: On power up, make sure that the FPGA has had time to "wake up," at least 34 ms, before sending it data.
- Check for contention between the Chip Select and Write Strobe signals and monitor the levels on those pins after configuration. It is safest to use the Chip Select pins only as inputs after configuration. Avoid contention if they are used as outputs. With XC2000 family devices, the I/Os become active before the FPGA receives its final data bits and clocks, and also before the DONE pin goes High. In other families, this relative timing is programmable. If the user function for any of the Chip Selects or the Write Strobe become outputs after configuration, they might contend and, in effect, de-select the FPGA so that it never receives its final data bits. Beware of contention!
- Check for contention between the FPGA pins and other

signals on the board. Except in XC2000, data is received as eight bits in parallel. Make sure bit 0 is connected to the D0 pin, bit 1 to D1 pin, etc. (In XC2000 family, data is received serially. If a PROM file is used as a data source, check that data is properly serialized LSB first. Data must be LSB first, although length count is MSB first. This is not intuitively obvious.)

### **Slave Serial Mode**

- Review the general debugging hints.
- Check the mode pin levels.

$M0 = 1, M1 = 1, M2 = 1$  for Slave Serial mode

- See schematics in the data sheet for the FPGA family.
  - Make sure  $V_{CC}$ , RESET, and PWRDWN are at 5 V, and ground pins are at 0 V.
  - Verify that the FPGA is receiving data on DIN and that it is receiving a valid clock signal on CCLK. Check the device sending the data. Check the device sending the clock signal, and make sure the clock meets the timing requirements specified in the product family documentation. Don't violate the XC3000 and XC2000 CCLK Low time specification of 5.0  $\mu$ s. A CCLK generated by a Master FPGA automatically meets the timing requirements.
  - Make sure the FPGA is ready to receive data.
- XC3000 Family:** On power up, make sure the INIT pin is High or wait at least 34 ms before you begin sending data to the FPGA.
- XC2000 Family:** On power up, make sure that the FPGA has had time to "wake up" at least 34 ms, before sending it data.
- At power up, make sure  $V_{CC}$  rises from 2.0 V to 4.5 V in less than 25 ms. If it does not, hold RESET Low until the  $V_{CC}$  pins reach 4.5 V.

### **Daisy Chain Debugging Hints**

- The key to debugging daisy-chain configurations is to isolate the problem and attempt to configure a single FPGA. Remove all but the first device from the board and configure it. Then insert the second device and configure both. Repeat as you add one device at a time until they all configure.
- The first device in the chain can be in any of the configuration modes. Debug it first, using the hints provided for the appropriate mode.
- All devices after the first one are in Slave Serial mode, so refer to the Slave Serial mode debugging hints above to solve any problems with Slave device.
- Monitor the DOUT pin of each device in the chain and verify that the 40-bit header (48-bit with XC5200 as the lead device) appears at the beginning of configuration, staggered by one CCLK period per device.
- If the Master device in the chain is an XC2000-family device and the Slaves are XC3000-family, make sure

the XC3000-family devices are configured with early DONE.

## Potential Length-Count Problem in Parallel or Peripheral Modes

It is highly desirable that the complete change from configuration to user operation occur as the result of one single byte-wide input. The activation of outputs and DONE, the de-activation of the global reset (set/reset in XC4000), and the progression to the “finished” state F (see Figure 2) should all occur as a result of one common byte input. Under normal circumstances, the software achieves this by manipulating the length-count value appropriately, taking into account the additional bits between devices, and adjusting for the fact that byte-wide interfaces always leave the last bit sitting in the P-S converter, shifting it out at the beginning of the next byte. These complexities, combined with the many possible daisy-chain arrangements have occasionally led to problems, where the device outputs go active before the last required byte had been received. This has sometimes lead to contention on the address outputs or data inputs and might prevent the device from going DONE, or reaching the real end of its configuration sequence. Not reaching this “finished” state limits the use of readback and boundary scan. A new option solves this problem:

The default option is “Length-Count aligned” which adjusts the length-count value such that length-count match occurs during the first bit in the last configuration byte. This assures sufficient CCLK pulses to complete any selected type of start-up sequence. The other option is “DONE-aligned”, which adjusts the length count value to make DONE go active at the end of a configuration data byte, which can cause problems in Peripheral mode.

**Only Peripheral modes seem to be sensitive to the difference between these two options.**

## Miscellaneous Notes

**CCLK** is the most important configuration signal. Once the INIT output is High, each device counts every Low-to-High transition of this configuration clock. In all modes except Slave Serial and Synchronous Peripheral, CCLK is a very fast output that cannot be made slew-rate limited. (it is now slew-rate limited in the newest XC4000X and XC5200 devices). When distributing this clock, the user should pay special attention to glitches, overshoots, and undershoots. In severe cases, a  $33\ \Omega$  resistor in series with the CCLK output might improve the signal integrity. In other cases, it might be better to provide a pull-up resistor at the far end of the CCLK net. Since the clock net has a transmission-line characteristic impedance of always less than  $100\ \Omega$ , the limited output drive capability of the CCLK output precludes proper parallel termination.

**DOUT** is an excellent observation point, since every device must output the preamble on this pin, irrespective of the selected configuration mode, and irrespective of the position in, or the existence of, a daisy chain.

**INIT** of all devices in a daisy chain should be interconnected to prevent the configuration from starting before all devices are ready. A  $10\ k\Omega$  pull-up resistor is recommended. The parallel INIT of the daisy-chained devices must be connected to the INIT of the lead XC4000/XC5200 device, or to the RESET input of the lead XC3000 device. This is especially important for re-configuration, where the master does not have a four-times longer wait period.

The **DONE** output indicates the end of the configuration process. In XC2000 and XC3000 systems, it makes sense to ground DONE permanently. The RESET input then becomes the reconfiguration input, and cannot be used as the dedicated asynchronous user RESET input. **LDC** can be used to indicate end of configuration.

**PWRDWN** (on XC2000 and XC3000 devices) must be High before and during the configuration process.

Don't let **PWRDWN** float!



## Configuring Mixed FPGA Daisy Chains

XAPP 091 November 24, 1997 (Version 1.0)

Application Note by Peter Alfke

### Overview

Xilinx FPGAs can be configured in a common daisy-chain structure, where the lead device generates CCLK pulses and feeds serial configuration information into the next downstream device, which in turn feeds data into the next downstream device, etc. There is no limit to the number of devices in a daisy chain, and XC2000, XC3000, XC4000, and XC5200 series devices can be mixed freely with only one constraint: the lead device must be a member of the highest-order family used in the chain. (For the purposes of this discussion, there is no difference between the XC4000 series and the XC5200 family, when XC5200 is used in any configuration mode except Express Mode). The lead device must generate a sufficient number of CCLK pulses after length-count-match was achieved, but XC3000-series devices generate fewer CCLK pulses than XC4000-series or XC5200-family devices require, and XC2000 devices generate even fewer CCLK pulses after length-count match. See Figure 1.

In a daisy-chain, all CCLK pins are interconnected, and DOUT of any upstream device feeds the DIN input of its downstream neighbor. Those are the basic connections. For control purposes, it is advisable to interconnect all the slave INIT pins (the XC2000 does not have this pin) and connect them to the INIT pin of the lead XC4000/XC5200 device or the RESET input of the lead XC3000 device.

Interconnected INIT pins prevent the master from starting the configuration process until all slaves are ready. For power-up this is assured automatically, since the master uses four times as many internal clocks for the power-up as any slave does, but, when re-configuring, master and slave devices consume the same number of clocks to clear a frame, and a fast master might be ready before a slow slave is. Interconnecting INITs solves this problem.

The DONE/PROG (D/P) and RESET pins (XC2000, XC3000) and the XC4000/XC5200 PROGRAM pins can be used in different ways, depending on the designer's preferences regarding reconfiguration, pin utilization, and need for a global RESET input.

If there is no need for a global logic RESET input, then it is best to permanently ground the XC2000/3000 D/P pin, which means that the RESET input functions as the Reconfigure input, and should be connected to all XC4000/XC5200 PROGRAM inputs.

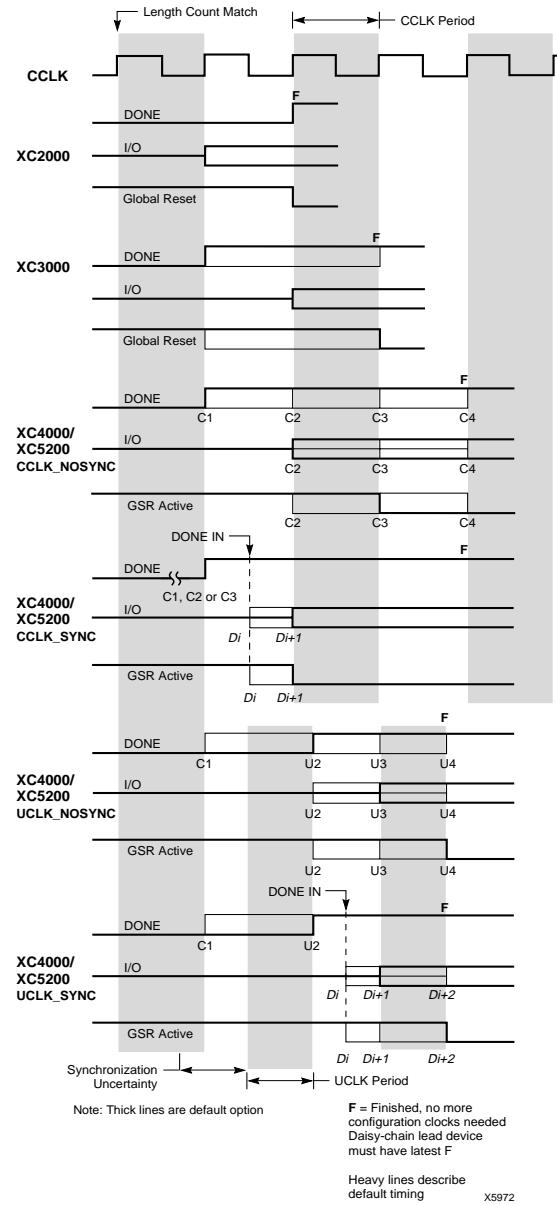
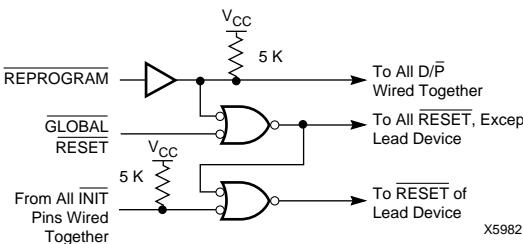


Figure 1: Start-up Timing

**Figure 2:**

If there is a need for a global logic RESET input that can reset all flip-flops in the user logic without causing reconfiguration, then external logic must combine RESET and D/P in such a way, that pulling Low RESET does not affect D/P, but pulling Low D/P also pulls down RESET. See Figure 2.

The following simple recommendations guarantee a well-defined beginning for any FPGA configuration or reconfiguration process, after the initialization and clearing of the configuration memory in all FPGAs has been completed, and the address counter in the serial PROM(s) has been reset.

The connections described below guarantee reliable operation even under adverse operating conditions such as  $V_{CC}$  glitches.

The lead device can use any configuration mode available. In all modes except Slave Serial, its CCLK pin is the output that clocks all other devices.

Obviously, all CCLK and XC1700 CLK pins must be interconnected, the DATA outputs from multiple XC1700 serial PROMs must be interconnected and connected to the DIN input of the lead device, and the daisy-chain must be established by connecting each DOUT output to the downstream DIN input.

#### **Configuration control pins are:**

##### **XC3000A, XC3000L, XC3100, XC3100A:**

- DONE/PROGRAM (open-drain output/input)
- RESET (input)
- INIT (open-drain output)

##### **XC4000 Series (XC4000E, XC4000X) and XC5200 family:**

- DONE (open-drain output / input)
- PROGRAM (input)
- INIT (open-drain output / input)

##### **XC1700:**

- RESET (input with programmable polarity)

The following recommendations assume that there are no XC2000 devices in the daisy chain (they lack the INIT out-

put) and that, if Serial mode is chosen for the lead device, the XC1700 device(s) store only one configuration for the whole daisy chain. The serial PROM(s) must, therefore, be reset before the daisy chain is to be (re)programmed.

There are three possible types of daisy chains using XC3000 and XC4000/XC5200 devices. Here are the recommended connections for the configuration control pins.

#### **Case 1:**

##### **Daisy chain consists of nothing but XC3000-series devices:**

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all slave INITs and connect them to the lead RESET input.

Interconnect all DONE pins.

Interconnect all slave RESET inputs

Instigate Reprogram by pulling the slave RESET net Low for at least 6  $\mu$ s while all DONE pins are Low.

(DONE can be permanently wired Low, but that sacrifices the use of RESET as a global reset of the user logic. If DONE is not wired Low, reprogram must pull DONE Low with an open-collector or open-drain driver).

#### **Case 2:**

##### **Lead device is XC4000-series or XC5200 family, driving any mixture of XC3000, XC4000 and XC5200 devices:**

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all INIT pins.

Interconnect all DONE pins.

Interconnect all XC4000/XC5200 PROGRAM inputs.

Interconnect all XC3000 RESET inputs.

Combine these two nets into one PROGRAM/RESET net

Instigate Reprogram by pulling the combined PROGRAM/RESET Low.

#### **Case 3:**

##### **Daisy chain consists of nothing but XC4000/ and XC5200-type devices:**

Use lead device's LDC to drive XC1700 CE.

Use lead device's INIT to drive XC1700 RESET.

Interconnect all INIT pins.

Interconnect all DONE pins (only required for UCLK-SYNC option).

Interconnect all XC4000/XC5200 PROGRAM inputs.

Instigate Reprogram by pulling PROGRAM Low.



## Configuration Issues: Power-up, Volatility, Security, Battery Back-up

XAPP 092 November 24, 1997 (Version 1.1)

Application Note by Peter Alfke

### Summary

This application note covers several related subjects: How does a Xilinx FPGA power up, and how does it react to power-supply glitches? Is there any danger of picking up erroneous data and configuration? What can be done to maintain configuration during loss of primary power? What can be done to secure a design against illegal reverse-engineering?

### Xilinx Families

XC2000, XC3000, XC4000, XC5200

## Power-Up

Here is a detailed description of XC3000 Series, XC4000 Series and XC5200 device behavior during supply ramp-up and ramp-down.

When  $V_{CC}$  is first applied and is still below about 3 V, the device wakes up in the pre-initialization mode.  $\overline{HDC}$  is High;  $\overline{INIT}$ ,  $\overline{LDC}$  and  $\overline{DONE}$  or  $\overline{DONE}/\overline{PROG}$  ( $D/\overline{P}$ ) are Low, and all other outputs are 3-stated with a weak pull-up resistor.

When  $V_{CC}$  has risen to a value above ~3 V, and a 1 and a 0 have been successfully written into two special cells in the configuration memory, the initialization power-on time delay is started. This delay compensates for differences in  $V_{CC}$  detect threshold and internal CCLK oscillator frequency between different devices in a daisy chain. The initialization delay counts clock periods of an on-chip oscillator (CCLK) which has a 3:1 frequency uncertainty depending on processing, voltage and temperature. Time-out, therefore, takes between 11 and 33 ms for a slave device, four times longer for a master device.

This factor of four makes sure that even the fastest master will always take longer than any slave. We assume that the worst-case difference between 33 ms and  $4 \times 11$  ms is enough to compensate for the  $V_{CC}$  rise time spent between threshold differences (max 2 V) of devices in a daisy chain. Only in cases of very slow  $V_{CC}$  rise time (>25 ms), must the user hold  $\overline{RESET}$  Low until  $V_{CC}$  has reached a proper level. Interconnecting the  $\overline{INIT}$  pins of all devices in a daisy-chain is a better method of synchronizing start-up, but cannot be used with XC2000 devices, since they lack an INIT pin.

After the end of the initialization time-out, each device clears its configuration memory in a fraction of a millisecond, then tests for inactive  $\overline{RESET}$  or  $\overline{PROGRAM}$ , stores the MODE value and starts the configuration process, as described in the Data Sheet. After the device is configured, the 5-V  $V_{CC}$  may dip to about 3.5 V without any significant consequences beyond an increase in delays (circuit speed

is proportional to  $V_{CC}$ ), and a reduction in output drive. If  $V_{CC}$  drops into the 3-V range, it triggers a sensor that forces the device back to the pre-initialization mode described above. All flip-flops are reset,  $\overline{HDC}$  goes High;  $\overline{INIT}$ ,  $\overline{LDC}$  and  $D/\overline{P}$  or  $\overline{DONE}$  go Low, and all other outputs are 3-stated with a weak resistive pull-up. If  $V_{CC}$  dips substantially lower, the active outputs become weaker, but the device stays in this preinitialization mode. When  $V_{CC}$  rises again, a normal configuration process is initiated, as described above.

## Sensitivity to $V_{CC}$ Glitches

The user need not be concerned about power supply dips: The XC3000/XC4000/XC5200 devices stay configured for small dips and they are "smart enough" to reconfigure themselves (if a master) or to ask for reconfiguration by pulling  $\overline{INIT}$  and  $D/\overline{P}$  or  $\overline{DONE}$  Low (if a slave). The devices will not lock up; the user can initiate re-configuration at any time just by pulling  $D/\overline{P}$  or  $PROGRAM$  Low or, if  $D/\overline{P}$  is Low, by forcing a High-to-Low transition on RESET.

Any digital logic device with internal data storage in latches or flip-flops is sensitive to power glitches. This includes every RAM, microprocessor, microcontroller, and peripheral circuit. Only purely combinatorial circuits can be guaranteed to survive a severe power glitch without any problem.

Xilinx SRAM-based FPGAs store their configuration in latches that lose their data when the supply voltage drops below a critical value (which is substantially below 3 V for the 5-V devices), but configuration data is extremely robust and reliable while  $V_{CC}$  stays above 3 V. All Xilinx configuration latches are implemented as cross-coupled complementary inverters with active pull-down n-channel transistors and active pull-up p-channel transistors. Both High and Low logic levels have an impedance of less than 5k $\Omega$  with respect to their respective supply rail.

Typical SRAM memory devices use passive poly-silicon pull-up resistors with an impedance of about 5,000 M $\Omega$ . A

current of one nanoamp (!) is sufficient to upset the typical SRAM cell, whereas it takes a million times more current to upset the Xilinx configuration latch.

This does not mean that SRAMs are unreliable, it just shows that the levels in Xilinx configuration latches are six orders of magnitude more resistant to upsets caused by external events, like cosmic rays or alpha particles. Xilinx has never heard about any occurrence of a spontaneous change in the configuration store in any of its ~50 million FPGA devices sold over the past twelve years.

Whereas most digital circuits rely on  $V_{CC}$  staying within specification, Xilinx FPGAs have an internal voltage monitoring circuit. For example, in the 5-Volt devices, whenever the supply voltage dips below 3 V, the internal monitoring circuit causes the Xilinx FPGA to stop normal operation. All outputs go 3-state, and the device waits for the supply voltage to rise closer to 4 V, when it either demands (slave or peripheral mode) or initiates (master mode) a reconfiguration. In the range between 5.5 and 3 V, all typical CMOS devices maintain their functionality and their data storage, they just get slower as the voltage goes down.

Xilinx has made sure that the FPGA cannot be corrupted by a power glitch. The most sensitive circuit is the low-voltage detector. It kicks in while all other configuration storage and user logic is still guaranteed to be functional. The voltage-monitoring feature in the Xilinx device can even be used to protect other circuitry, or it can be coordinated with external monitoring circuits.

There is no possibility of a  $V_{CC}$  dip causing the device to malfunction, i.e., to operate with erroneous configuration information.

- If  $V_{CC}$  stays above the trip point, the device functions normally, albeit at reduced speed, like any other CMOS device.
- If  $V_{CC}$  dips below the trip point, the device 3-states all outputs and waits for reconfiguration.

Xilinx production-tests the  $V_{CC}$ -dip tolerance of all XC3000 devices in the following way.

After the device is configured,  $V_{CC}$  is reduced to 3.5 V, and then raised back to 5.0 V. Configuration data is then read back and compared against the original configuration bit stream. Any discrepancy results in rejection of the device.

Subsequently,  $V_{CC}$  is reduced to 1.5 V and then raised to 5.0 V. The device must first go 3-state, then respond with a request for reconfiguration.

Both these tests are performed at high temperature ( $>85^{\circ}\text{C}$  for commercial parts,  $>100^{\circ}\text{C}$  for military). Any part failing any of these tests is rejected as a functional failure.

As a result of these careful precautions, we contend that Xilinx FPGAs are safer than all other types of circuitry (except purely combinatorial circuits). A microprocessor can loose the content of its address register, its accumula-

tor or other control register due to an undetected power glitch, with disastrous consequences to the subsequent operation. A Xilinx FPGA detects the power glitch and always plays it safe by flagging the problem.

No complex system of any kind can function reliably when  $V_{CC}$  is unreliable. Xilinx FPGAs do the safest thing possible, whenever such problems occur.

## Design Security

Some Xilinx customers are concerned about the security of their designs. How can they protect their designs against unauthorized copying or reverse-engineering?

We must distinguish between two very different situations:

- Configuration data is accessible from a serial or parallel EPROM or in a microprocessor's memory. This is the normal case.
- Configuration data is hidden from the user, since the design does not permanently store a source of configuration data. After the FPGA was configured, the EPROM or other source was removed from the system, and configuration is kept alive in the FPGA through battery-back-up.

## Design Security when Configuration Data is Accessible

In the first case, it is obviously very easy to make an identical replica of the design by copying the configuration data and the pc-board interconnect pattern of the standard devices, but it is virtually impossible to interpret the bit-stream in order to understand the design or make intelligent modifications to it. Xilinx keeps the interpretation of the bitstream a closely guarded secret. Reverse-engineering an FPGA would require an enormously tedious analysis of each individual configuration bit, which would still only generate an XACT view of the FPGA, not a usable schematic.

The best protection against a mindless copy is legal. The bitstream is easily protected by copyright laws that have proven to be more successfully enforced than the intellectual property rights of circuit designs.

The combination of copyright protection, and the almost insurmountable difficulty of creating any design variation for the intended function, provides good design security. The recent successes of small companies in reverse-engineering microprocessors and microprocessor support circuits show that a non-programmable device can actually be more vulnerable than an FPGA. For advice on legal protection of the configuration bitstream, see the following paragraphs.

### Legal Protection of Configuration Bit-Stream Programs

The bit-stream program loaded into the FPGA may qualify as a "computer program" as defined in Section 101, Title 17 of the United States Code, and as such may be protectable under the copyright law. It may also be protectable as a trade secret if it is identified as such. We suggest that a user wishing to claim copyright and/or trade secret protection in the bit stream program consider taking the following steps.

Place an appropriate copyright notice on the FPGA device or adjacent to it on the PC board to give notice to third parties of the copyright. For example, because of space limitations, this notice on the FPGA device could read "©1996 XYZ Company" or, if on the PC board, could read "Bit Stream ©1996 XYZ Company".

File an application to register the copyright claim for the bit-stream program with the U.S. Copyright Office.

If practicable, given the size of the PC board, notice should also be given that the user is claiming that the bit-stream program is the user's trade secret. A statement could be added to the PC board such as: "Bit-stream proprietary to XYZ Company. Copying or other use of the bitstream program except as expressly authorized by XYZ Company is prohibited."

To the extent that documentation, data books, or other literature accompanies the FPGA-based design, appropriate wording should be added to this literature providing third parties with notice of the user's claim of copyright and trade secret in the bit-stream program. For example, this notice could read: "Bit-Stream©1996 XYZ Company. All rights reserved. The bit-stream program is proprietary to XYZ Company and copying or other use of the bit-stream program except as expressly authorized by XYZ Company is expressly prohibited."

To help prove unauthorized copying by a third party, additional nonfunctional code should be included at the end of the bit-stream program. Therefore, should a third party copy the bit-stream program without proper authorization, if the non-functional code is present in the copy, the copier cannot claim that the bit-stream program was independently developed.

These are only suggestions, and Xilinx makes no representations or warranties with respect to the legal effect or consequences of the above suggestions. Each user is advised to consult legal counsel with respect to seeking protection of a bit-stream program and to determine the applicability of these suggestions to the specific circumstances.

If the user has any questions, contact the Xilinx legal department at 408-879-4984.

### Design Security by Hiding the Configuration Data

If the design does not contain the source of configuration data, but relies on battery-back-up of the FPGA configuration, then there is no conceivable way of copying this design. Opening up the package and probing thousands of latches in undocumented positions to read out their data without ever disturbing the configuration is impossible.

This mode of operation offers the ultimate design security. It is being used by several Xilinx customers who have reason to be concerned about illegal pirating of their designs.

### Battery Back-up and Powerdown

Since SRAM-based FPGAs are manufactured using a high-performance low-power CMOS process, they can preserve the configuration data stored in the internal static memory cells even during a loss of primary power. This is accomplished by forcing the device into a low-power non-operational state, while supplying the minimal current requirement of  $V_{CC}$  from a battery.

Circuit techniques used in XC3100, XC4000 and XC5200 devices prevent  $I_{CC}$  from being reduced to the level needed for battery back-up. Consequently, battery back-up should only be used for XC2000, XC2000L, XC3000, XC3000A and XC3000L devices.

There are two primary considerations for battery backup which must be accomplished by external circuits.

- Control of the Power-Down (PWRDWN) pin
- Switching between the primary  $V_{CC}$  supply and the battery.

Important considerations include the following.

- Insure that PWRDWN is asserted logic Low prior to  $V_{CC}$  falling, is held Low while the primary  $V_{CC}$  is absent, and returned High after  $V_{CC}$  has returned to a normal level. PWRDWN edges must not rise or fall slowly.
- Insure "glitch-free" switching of the power connections to the FPGA device from the primary  $V_{CC}$  to the battery and back.
- Insure that, during normal operation, the FPGA  $V_{CC}$  is maintained at an acceptable level,  $5.0\text{ V} \pm 5\%$  ( $\pm 10\%$  for Industrial and Military).

Figure 1 shows a power-down circuit developed by Shel Epstein of Epstein Associates, Wilmette, IL. Two Schottky diodes power the FPGA from either the 5.2 V primary supply or a 3 V Lithium battery. A Seiko S8054 3-terminal power monitor circuit monitors  $V_{CC}$  and pulls PWRDWN Low whenever  $V_{CC}$  falls below 4 V.

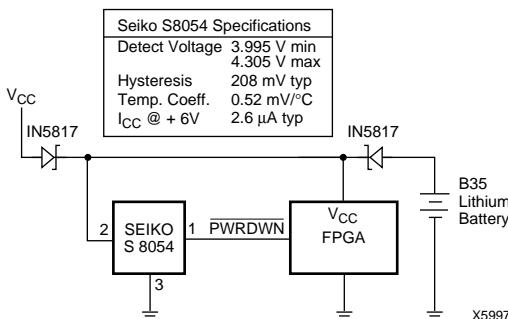


Figure 1: Battery Back-up Circuit

## Powerdown Operation

A Low level on the PWRDWN input, while  $V_{CC}$  remains higher than 2.3 V, stops all internal activity, thus reducing  $I_{CC}$  to a very low level:

- All internal pull-ups (on Long lines as well as on the I/O pads) are turned off.
- The crystal oscillator is turned off
- All package outputs are three-stated.
- All package inputs ignore the actual input level, and present a High to the internal logic.
- All internal flip-flops or latches are permanently reset.
- The internal configuration is retained.
- When PWRDWN is returned High, after  $V_{CC}$  is at its nominal value, the device returns to operation with the same sequence of buffer enable and D/P as at the completion of configuration.

## Things to Remember:

Powerdown retains the configuration, but loses all data stored in the device. Powerdown three-states all outputs and ignores all inputs. No clock signal will be recognized, and the crystal oscillator is stopped. All internal flip-flops and latches are permanently reset and all inputs are interpreted as High, but the internal combinatorial logic is fully functional.

## Things to Watch Out for:

Make sure that the combination of all inputs High and all internal flip-flop outputs Low in your design will not generate internal oscillations or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line. These two situations are farfetched, but they are possible and will result in considerable power consumption. It is quite easy to simulate these conditions since all inputs are stable and the internal logic is entirely combinatorial, unless latches have been made out of function generators.

During powerdown, the  $V_{CC}$  monitoring circuit is disabled. It is then up to the user to prevent  $V_{CC}$  dips below 2.3 V, which might corrupt the stored configuration.

During configuration, the PWRDWN pin must be High, since configuration uses the internal oscillator. Whenever  $V_{CC}$  goes below 4 V, PWRDWN must already be Low in order to prevent automatic reconfiguration at low  $V_{CC}$ . For the same reason,  $V_{CC}$  must first be restored to 4 V or more, before PWRDWN can be made High.

PWRDWN has no pull-up resistor. A pull-up resistor would draw supply current when the pin is Low, which would defeat the idea of powerdown, where  $I_{CC}$  is only microamperes.



## Dynamic Reconfiguration

XAPP 093 November 10, 1997 (Version 1.1)

Application Note by Peter Alfke

### Introduction

All Xilinx SRAM-based FPGAs can be in-system configured and re-configured an unlimited number of times. The XC6200 family has additional features that allow partial and very fast (re-)configuration from a microprocessor bus. See the XC62000 product documentation for details.

This application note describes the procedures for reconfiguring the more traditional Xilinx FPGAs of the XC3000, XC4000, and XC5200 families.

All configuration information is stored in latches that are loaded serially, conceptually like a shift register. There are several different bit-serial or byte-parallel configuration data interfaces, selected by logic levels on three mode inputs, but – with the exception of the XC5200 Express mode – they all result in the bit-serial loading of the configuration latches. The byte-parallel interfaces in Master Parallel and Peripheral modes act just as an 8-bit parallel-to-serial converter. Between devices in a daisy-chain, the configuration information is transmitted bit-serially with a common Configuration Clock (CCLK). In Master and Peripheral modes, CCLK is generated by the lead FPGA device, in Slave Serial mode, CCLK comes from an external source.

Reconfiguration of an operational device, or a daisy-chain of devices, goes through the following sequence of events:

- Reconfiguration is initiated by pulling a specific device pin Low.
- First, all outputs are 3-stated, except **HDC** = High, **LDC** and **DONE** = Low
- Then, all internal registers, flip-flops and latches, as well as the configuration storage latches are cleared. During this time, the **INIT** output is being pulled Low.
- Then, the Mode inputs and **RESET** or **PROGRAM** inputs are sampled to determine the selected configuration mode and whether to start the new configuration process, or to wait.
- Then configuration data is accepted and loaded into the internal latches and distributed through the daisy-chain.
- When all configuration information has been entered, the user outputs are activated, **DONE** goes High and the internal reset is released, all in the order specified in the configuration bitstream. All devices in a daisy-chain perform each of these operations in synchronism.

### Important Considerations

- Reconfiguration is “all or nothing”. There is no way to restrict reconfiguration to a part of the chip (Note that XC6200 devices do not have this limitation).
- Reconfiguration takes a specific time, determined only by device type, size and clock speed, independent of the particular configuration pattern. Configuration takes from tens to hundreds of milliseconds. During that time, all user-outputs of the device, or the whole daisy-chain of devices, are 3-stated with weak internal pull-ups, except for **HDC** and **LDC**, which are active High or Low respectively.
- All user-data stored in registers, flip-flops or latches is erased. There is no way to retain data inside the device from one configuration to the next.

These limitations are absolute. If they are not acceptable, the user must resort to creative solutions, like piggy-backing multiple devices.

The designer of reconfigurable applications should be familiar with the normal configuration process of each device, as described in the individual product descriptions. There is also pertinent information about daisy-chain operation, especially about mixed daisy chains, in other application notes.

Interconnecting the **INIT** pins of all devices in a daisy-chain is mandatory for reconfiguration, since this is the only way to guarantee that the master device does wait for the rest of the daisy-chain to be cleared, before starting the reconfiguration. Only the first configuration after power-up makes the master device spend four times as many clock periods as any slave during the initial clear operation, so that the master cannot possibly get ahead of the slaves. Reconfiguration, however, does not slow down the master this way, so the interconnection of all **INIT** pins must serve that same purpose.

In Master Serial mode, it is highly recommended that the active Low level of **INIT** be used to reset the XC1700-family Serial PROM.

## Reconfiguration Time

Reconfiguration time is usually more critical than the original power-on configuration time, which is often masked by the general power-on delays.

Here are some suggestions to reduce reconfiguration time.

- A daisy-chain is obviously not conducive to fast configuration, it should be broken up into shorter blocks, perhaps single devices. Multiple devices can be configured in parallel, but can still use a common CCLK, and can also be made to start up together. If the devices differ in size or family, they should all be given the same length count as the largest device in the group.
- Configuration Mode  
Parallel and Peripheral modes are not any faster than Master Serial mode, since all modes (with the exception of XC5200 Express mode) internally operate on serial data. The internally generated CCLK frequency is guard-banded to never approach the upper limit of what the device can tolerate. Therefore, the fastest possible configuration mode for XC3000 and XC4000-series devices is Slave Serial, with an external well-controlled source for CCLK. Its frequency can be up to 10 MHz for all 5-V devices, and there are ways to increase the average clock rate well beyond that, but they require dynamic clock frequency changes and an intimate understanding of the configuration frame structure.  
At 10 MHz, configuration time per device ranges from 1.5 ms for the XC3020A to 42 ms for the XC4025E and 192 ms for the XC4085XL.
- Possible Contention Problems:  
Certain user outputs become active during the configuration process:  
Address outputs during Master Parallel mode, Chip Select and Ready/Busy during Peripheral modes.  
The designer must make sure that these active outputs do not cause contention with other logic that might use the same pins as device inputs.

## Initiating Reconfiguration in Different Xilinx Device Families

### XC3000 Series

There are three alternatives:

1. Pull  $\overline{\text{RESET}}$  Low while DONE is permanently grounded externally.

This is the simplest scheme, but it precludes the use of  $\overline{\text{RESET}}$  to clear the flip-flops and latches in the operating user-design.  $\overline{\text{RESET}}$  must be pulled Low for more than six microseconds to overcome its internal low-pass filtering. Configuration starts when  $\overline{\text{RESET}}$  has gone High again.

2. Pull DONE Low with an open-drain ("open-collector") output. This assumes that DONE was High, i.e. that the previous configuration was successful. Reconfiguration starts as soon as the internal memory has been cleared. DONE can be released anytime.
3. Pull DONE Low with an open-drain ("open-collector") output and pull  $\overline{\text{RESET}}$  Low. Keep  $\overline{\text{RESET}}$  Low for at least six microseconds while DONE is Low. DONE can be released anytime after that, or not released at all. See alternative 1.

### XC4000 Series and XC5200 Family

Pull the PROGRAM input Low for at least 0.3 microseconds to initiate clearing the configuration memory, then pull PROGRAM up to start the new configuration process.

While PROGRAM is held Low, a Low level on INIT indicates that the device is continuously clearing the configuration memory. When PROGRAM has been pulled up, INIT stays Low during one more clear operation, then goes High.

All device families, except the original XC4000, have a continuously active pull-up resistor on the PROGRAM pin.

## FPGAs Can Control Their Own Reconfiguration

Pulling PROGRAM, RESET or DONE low can trigger a reconfiguration, as described above. When a user output is connected to drive the reconfiguration pin, the FPGA can trigger its own reconfiguration. Although the triggering output will go 3-state once reconfiguration is initiated, this trigger operation is reliable.

Such auto-reconfiguration offers interesting opportunities for small systems using a single FPGA in Master Parallel configuration mode. A manually operated switch selects the most significant address bits of the PROM, and the FPGA compares the switch settings against a stored value. Upon detecting a difference, it can trigger reconfiguration that is loaded from the newly selected PROM address range. Or an external CMOS register can be loaded with the intended reconfiguration address range and then control the upper bits of the PROM address



## Metastable Recovery

XAPP 094 November 24, 1997 (Version 2.1)

Application Note By Peter Alfke and Brian Philofsky

### Introduction

Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. This happens when the input transition not only violates the setup and hold-time specifications, but actually occurs within the tiny timing window where the flip-flop accepts the new input. Under these circumstances, the flip-flop can enter a symmetrically balanced transitory state, called metastable (meta = between).

While the slightest deviation from perfect balance will cause the output to revert to one of its two stable states, the delay in doing so depends not only on the gain-bandwidth product of the circuit, but also on how perfect the balance is, and on the noise level within the circuit; the delay can, therefore, only be described in statistical terms.

The problem for the system designer is not the illegal logic level in the balanced state (it's easy enough to translate that to either a 0 or a 1), but the unpredictable timing of the final change to a valid logic state. If the metastable flip-flop drives two destinations with differing path delays, one des-

tination might clock in the final data state while the other does not.

With the help of a self-contained circuit, Xilinx evaluated the XC4000 and XC3000-series flip-flops. The result of this evaluation shows the Xilinx flip-flop to be superior in metastable performance to many popular MSI and PLD devices.

Since metastability can only be measured statistically, this data was obtained by configuring several different Xilinx FPGAs with a detector circuit shown in Figure 1. The flip-flop under test receives the asynchronous ~1-MHz signal on its D input, and is clocked by a much higher manually adjustable frequency. The output QA feeds two flip-flops in parallel, one (QB) being clocked by the same clock edge, the other (QC) being clocked by the opposite clock edge. When clocked at a low frequency, each input change gets captured by the rising clock edge and appears first on QA, then, after the falling clock edge, on QC, and finally, after the subsequent rising clock edge, on QB.

If a metastable event in the first flip-flop increases the settling time on QA so much that QC misses the change, but QB still captures it on the next rising clock edge, this error

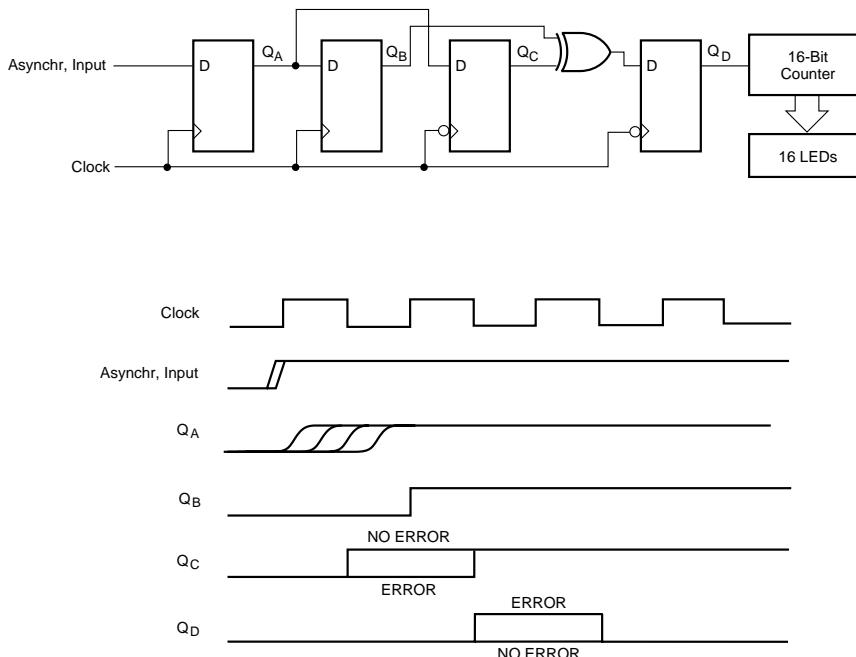


Figure 1: Test Circuit and Timing Diagram

can be detected by feeding the XOR of QB and QC into a falling-edge triggered flip-flop. Its output (QD) is normally Low, but goes High for one clock period each time the asynchronous input transition caused such a metastable delay in QA. The frequency of metastable events can be observed with a 16-bit counter driven by QD.

By changing the clock frequency, and thus the clock half-period, the amount of acceptable metastable delay on the QA output can be varied, and the resulting frequency of metastable events can be observed on the counter outputs.

As expected, no metastable events were observed at clock rates below 70 MHz for the XC4005-6, or below 100 MHz for the XC4005E-3, since a half clock period at those frequencies is adequate for almost any metastability-resolution delay. Increasing the clock rate slightly brought a sudden burst of metastable events. Careful adjustment of the clock frequency gave repeatable, reliable measurements.

## Metastability Measurements

The circuit of [Figure 1](#) was implemented in five different Xilinx devices: two cutting-edge devices using 0.5 micron, 3-layer-metal technology, the XC4005E-3 and the XC3142A-09, one device, the XC5206 using 0.6 micron, 3-layer-metal, and, for comparison purposes, also in two older-technology devices, the XC4005-6 and the XC3042-70.

In each device two different implementations put QA, the flip-flop under test, into an IOB and a CLB (Except for the XC5200 family which has no flip-flops in the IOB). The XC4000-series devices showed little difference between IOB and CLB behavior, but in the XC3000-series devices, the IOB flip-flops showed dramatically better metastable performance than the CLB flip-flops. This difference can be traced to subtle differences in circuit design and layout, and will guide us to further improvements in metastable performance in future designs.

Metastable measurement results are listed in [Table 1](#), and are plotted in [Figure 2](#). The results for XC4000E-3 (IOB and CLB) and for XC3100A-09 IOB flip-flops are outstanding, far superior to most metastable data published anywhere else. When granted 2 or 3 ns of extra settling delay, these devices come close to eliminating the problems caused by metastability, since their MTBF exceeds millions of years.

The older-technology devices are obviously less impressive, but they still show acceptable performance, especially in the IOB input flip-flops that are normally used to synchronize asynchronous input signals.

[Table 1](#) lists the experimental results from which the exponential factor K2 was derived. The clock frequency was adjusted manually, while observing the LSB and the MSB of the 16-bit error counter.  $F_L$  is the clock frequency that generated a ~1 Hz error rate,  $F_H$  generated a ~64,000 Hz error rate.

K2 is derived by dividing  $\ln 64,000$  by the half-period difference.

**Table 1: Metastable Measurement Results**

Device	$F_L$ (MHz)	$F_H$ (MHz)	Half-period Difference (ns)	K2 (1/ns)
XC4005E-3 IOB	111.5	131.6	0.685	16.1
XC4005E-3 CLB	109.0	124.4	0.568	19.4
XC4005-6 IOB	73.0	90.0	1.294	8.5
XC4005-6 CLB	71.2	88.8	1.392	7.9
XC5206-5 CLB	70.8	79.8	0.80	13.7
XC3142A-09 IOB	152.2	206.6	0.87	12.7
XC3142A-09 CLB	107.4	211.3	2.29	4.8
XC3042-70 IOB	46.6	61.5	2.60	4.2
XC3042-70 CLB	41.9	64.8	4.22	2.6

## Metastability Calculations

The Mean Time Between Failures (MTBF) can only be defined statistically. It is inversely proportional to the product of the two frequencies involved, the clock frequency and the average frequency of the asynchronous data changes, provided that these two frequencies are independent and have no correlation.

The generally accepted equation for MTBF is

$$\text{MTBF} = \frac{e^{K2 * t}}{F1 * F2 * K1}$$

K1 represents the metastability-catching set-up time window, which describes the likelihood of going metastable.

K2 is an exponent that describes the speed with which the metastable condition is being resolved. K2 is an indication of the gain-bandwidth product in the feedback path of the master latch of the master-slave flip-flop. A small increase in K2 results in an enormous improvement in MTBF.

With  $F1 = 1$  MHz,  $F2 = 10$  MHz and  $K1 = 0.1$  ns =  $10^{-10}$  s:

$$\text{MTBF (in seconds)} = 10^{-3} * e^{K2*t}$$

Experimentally derived (see [Table 1](#)):

$K2 = 16.1$  per ns, for the XC4005E-3 IOB flip-flops

$K2 = 19.4$  per ns, for the XC4005E-3 CLB flip-flops

$K2 = 8.5$  per ns, for the XC4005-6 IOB flip-flops

$K2 = 7.9$  per ns, for the XC4005-6 CLB flip-flops

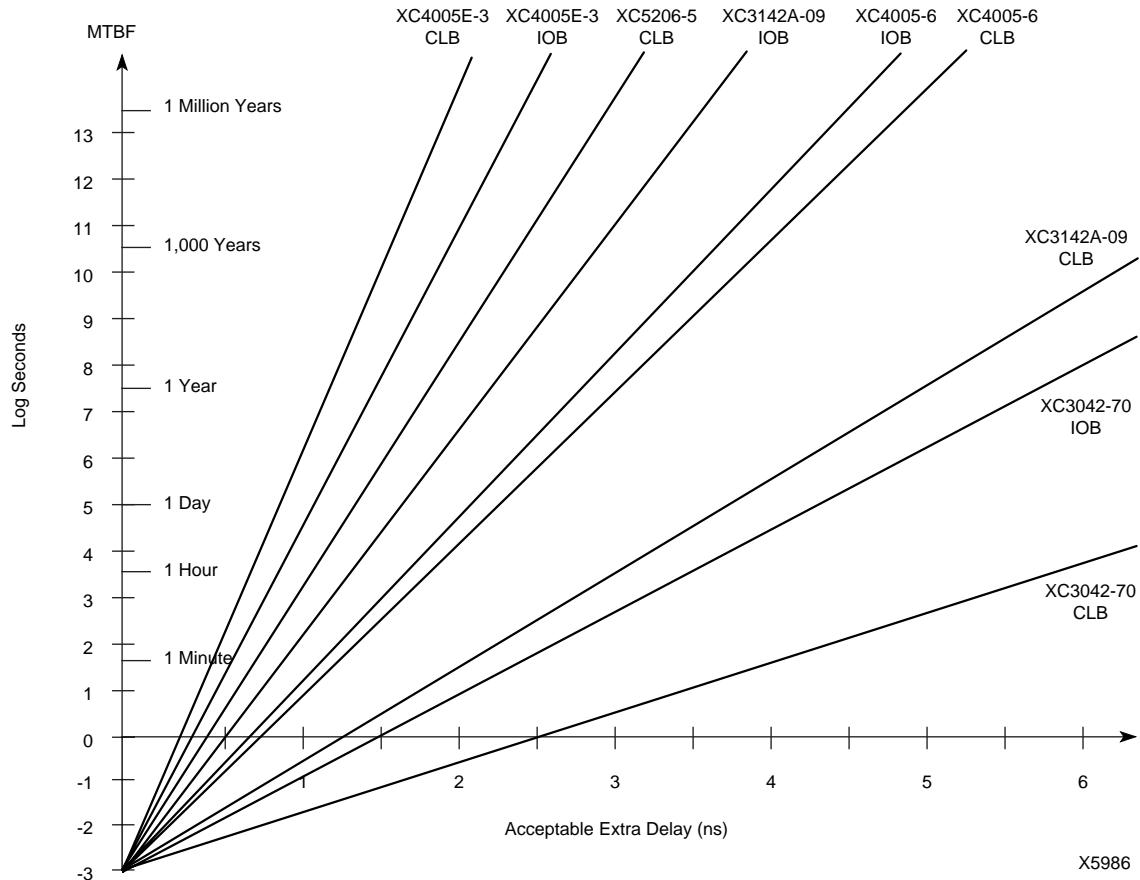
$K2 = 13.7$  per ns, for the XC5206-5 CLB flip-flops

$K2 = 12.7$  per ns, for the XC3142A-09 IOB flip-flops

$K2 = 4.8$  per ns, for the XC3142A-09 CLB flip-flops

$K2 = 4.2$  per ns, for the XC3042-70 IOB flip-flops

$K2 = 2.6$  per ns, for the XC3042-70 CLB flip-flops



**Figure 2: Mean Time Between Failure for various IOB and CLB flip-flop outputs when synchronizing a ~1 MHz asynchronous input with a 10 MHz clock.**

For other operating conditions, divide MTBF by the product of the two frequencies. For a ~10 MHz asynchronous input synchronized by a 40 MHz clock, the MTBF is 40 times

shorter than plotted; for a ~50 kHz signal synchronized by a 1 MHz clock, the MTBF is 200 times longer than plotted here.



## Set-up and Hold Times

XAPP 095 November 24, 1997 (Version 1.0)

Application Brief by Peter Alfke

### Introduction

Beware of hold-time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

“Set-up time” and “hold time” describe the timing requirements on the data input of a flip-flop or register with respect to the clock input. The set-up and hold times describe a window of time during which data must be stable in order to guarantee predictable performance over the full range of operating conditions and manufacturing tolerances.

A positive set-up time describes the length of time that the data must be available and stable before the active clock edge. A positive hold time, on the other hand, describes the length of time that the data to be clocked into the flip-flop must remain available and stable after the active clock edge. A positive set-up time limits the maximum clock rate of a system, but a positive hold time can cause malfunction at any clock rate. Thus, chip designers and system designers strive to eliminate hold-time requirements.

The IC design usually guarantees that any individual flip-flop does not require a positive hold time with respect to the clock signal at this flip-flop.

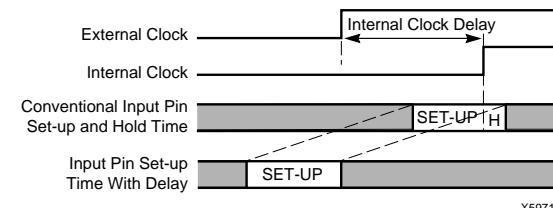
Hold-time requirements between flip-flops or registers on the same chip can be avoided by careful design of the on-chip clock distribution network. If the worst-case clock-skew value is shorter than the sum of minimum clock-to-Q plus minimum interconnect delays, there is never any on-chip hold-time problem.

It is, however, far more difficult to avoid a hold time problem in the device input flip-flops, with respect to the device clock input pin. When specifying the data pin-to-clock pin set-up and hold times, the chip-internal clock distribution delay must be taken into consideration. It effectively moves the timing window to the right (see figure), thus subtracting from the specified internal set-up time (which is good), but adding to the hold time (which is very bad). If the clock distribution delay is any longer than the data input delay – and it easily might be – the device data input has a hold-time requirement with respect to the clock input.

This means that the data source, usually another IC driven by the same clock, must guarantee to maintain data beyond the clock edge. In other words, the data source is not allowed to be very fast. If it is, the receiver might erroneously input the new data instead of the data created by the previous clock, as it should. This is called a race condition, and can be a fatal system failure.

If the receiving device has a hold time requirement, the source of data must guarantee an equivalent minimum value for its clock-to-output delay. Almost no IC manufacturer is willing to do this, and in the few cases where it is done, the minimum value is usually a token 1 ns. Any input hold time requirement is, therefore, an invitation to system failure. Any clock distribution skew on the PC-board can compound this issue and wipe out even the specified short minimum delay.

Xilinx has addressed this problem by adding a deliberate delay to every FPGA data input. In XC3000, and XC3100 FPGAs, this delay is fixed and always present; in XC4000 and XC5200 FPGAs, this delay is optional, and its value is tailored to the clock distribution delay (i.e. it is larger for bigger devices). As a result we can claim that no Xilinx FPGA Data input has a hold-time problem (i.e., none has a positive hold time with respect to the externally applied clock), when the design uses the internal global clock distribution network (and, in XC4000 and XC5200, uses the delayed input option). Most competitive devices do not offer this feature.



X5971



## Overshoot and Undershoot

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XAPP 096 September 9, 1997 (Version 1.0)

Application Note By Peter Alfke

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### Introduction

The "Absolute Maximum Ratings" table in the Xilinx Data Book restricts the signal-pin voltage to a maximum 500 mV excursion above  $V_{CC}$  and below ground. The reason for this tight specification is to prevent uncontrolled current in the input-clamping ESD-protection diodes. Such tight specifications are common in the industry; some manufacturers limit the excursion to 300 mV.

This specification seems to be clean and simple, but it is violated in almost every practical design. When users put modern CMOS devices on PC boards, and interconnect them with unterminated traces, there are reflections, commonly called "ringing", that cause overshoots and undershoots of substantial amplitude (2 V and more). The recent migration to smaller device geometries has made the IC outputs even faster and increased the slew-rate, causing more reflections even on short PC-board traces.

Fortunately, this problem has an easy solution:

The concern is not the input voltage, but rather the current through the input protection diode and other input structures. Excessive current can cause latch-up if it exceeds hundreds of millamps AND if it lasts for microseconds (shorter duration current spikes do not activate the SCR-like latch-up mechanism).

PC-board reflections, on the other hand, usually have a short duration of just a few nanoseconds, and have an impedance of 40 to 100  $\Omega$ , which makes them incapable of causing latch-up. They don't drive enough current and they don't last long enough to cause any harm.

Here is the new Xilinx specification:

"Maximum DC overshoot or undershoot above  $V_{CC}$  or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to  $V_{CC} + 2.0$  V, provided this over- or undershoot lasts less than 20 ns".



## Boundary Scan in XC4000 and XC5200 Series Devices

XAPP017 April 9, 1998 (Version 2.1)

Application Note

### Summary

XC4000 and XC5200 Series FPGA devices contain boundary-scan facilities that are compatible with IEEE Standard 1149.1. This Application Note describes those facilities in detail, and explains how boundary scan is incorporated into an FPGA design.

### Xilinx Family

XC4000 Series, XC5200

## Introduction

In production, boards must be tested to assure the integrity of the components and the interconnections. However, as integrated circuits have become more complex and multi-layer PC-boards have become more dense, it has become increasingly difficult to test assembled boards.

Originally, manufacturers used functional tests, applying input stimuli to the input connectors of the board, and observing the results at the output. Later, "bed-of-nails" testing became popular, where a customized fixture presses sharp, nail-like stimulus- and test-probes into the exposed traces on the board. These probes were used to force signals onto the traces and observe the response.

However, increasingly dense multi-layer PC boards with ICs surface-mounted on both sides have stretched the capability of bed-of-nail testing to its limit, and the industry is forced to look for a better solution. Boundary-scan techniques provide that solution.

The inclusion of boundary-scan registers in ICs greatly improves the testability of boards. Boundary scan provides a mechanism for testing component I/Os and interconnections, while requiring as few as four additional pins and a minimum of additional logic in each IC. Component testing may also be supported in ICs with self-test capability.

Devices containing boundary scan have the capability of driving or observing the logic levels on I/O pins. To test the external interconnect, devices drive values onto their outputs and observe input values received from other devices. A central test controller compares the received data with expected results. Data to be driven onto outputs is distributed through a chain of shift registers, and observed input data is returned through the same shift-register path.

Data is passed serially from one device to the next, thus forming a boundary-scan path or loop that originates at the test controller and returns there. Any device can be temporarily removed from the boundary-scan path by bypassing

its internal shift registers, and passing the serial data directly to the next device.

XC4000/XC5200 FPGA devices contain boundary-scan registers that are compatible with the IEEE Standard 1149.1, that was derived from a proposal by the Joint Test Action Group (JTAG). External (I/O and interconnect) testing is supported; there is also limited support for internal self-test.

## Overview of XC4000/XC5200 Boundary-Scan Features

XC4000/XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE Standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD and BYPASS instructions. The TAP can also support two USERCODE instructions.

**Note:** If boundary scan is not used after the device is configured, the user can use the special boundary scan pads as input or output pins. During configuration, be sure not to toggle the TAP pins, since inadvertent toggling of the TAP pins can turn the boundary scan circuitry 'on.' The TDI, TMS, and TCK pads can be used as unrestricted I/O. The TDO pad can be used as an output pad. In the XC5200 family, all four pins have full I/O capability. And like the regular IOBs, these input and output pins have pullups and pulldowns available.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability even after configuration affords tremendous flexibility for interconnect testing.

Additionally, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This partially compensates for the lack of INTEST support.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USER1/USER2 instructions are only available if boundary scan specified in the schematic/HDL code. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can also be used to configure the FPGA device, and read back the configuration data.

The following description assumes that the reader is familiar with boundary-scan testing and the IEEE Standard. Only issues specific to the XC4000/XC5200 implementation are discussed in detail. For general information on boundary scan, please refer to the bibliography.

## Deviations from the IEEE Standard

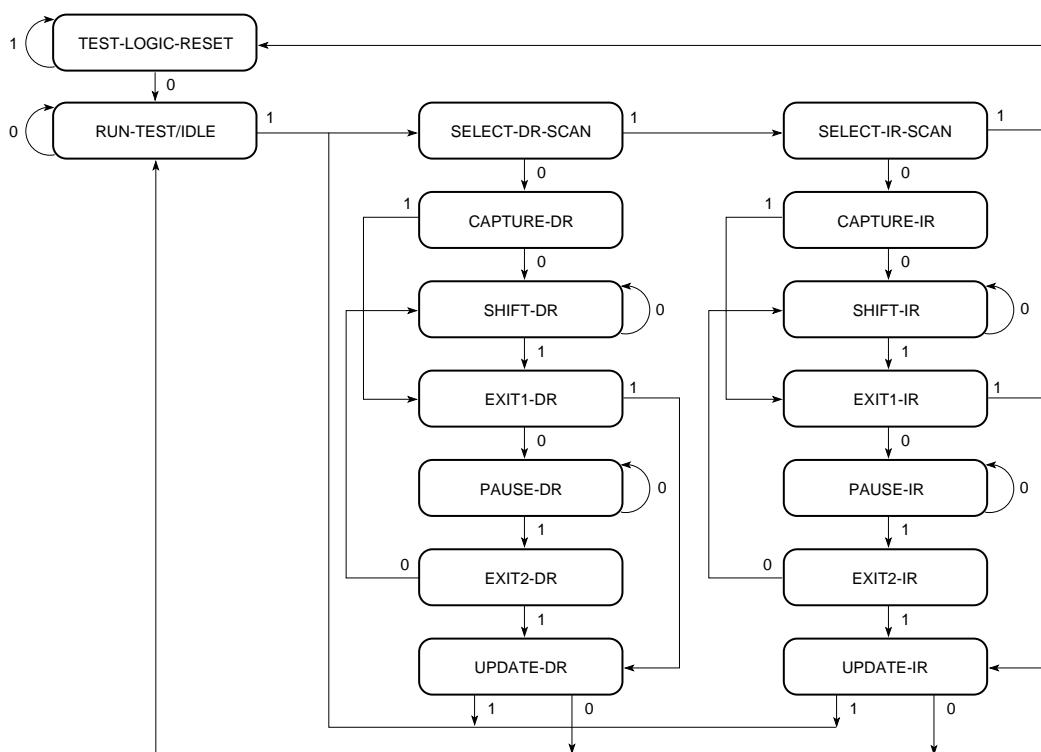
The XC4000/XC5200 boundary scan implementation deviates from the IEEE standard in that three dedicated pins (CCLK, PROGRAM and DONE) are not scanned.

It should also be noted that the Test Data Register contains three Xilinx test bits (BSCANT.UPD, TDO.O and TDO.T) and that bits of the register may correspond to unbonded or unused pins.

Additionally, the EXTEST instruction incorporates INTEST-like functionality that is not specified in the standard, and system clock inputs are not disabled during EXTEST, as recommended in the standard.

The TAP pins (TMS, TCK, TDI and TDO) are scanned, but connections to the TAP controller are made before the boundary-scan logic. Consequently, the operation of the TAP controller cannot be affected by boundary-scan test data.

When the TAP is in the shift-DR state the contents of all data registers are shifted; if you are in the middle of shifting out data from the data register, complete shifting out of all data first, before switching to the instruction or bypass register.



NOTE: The value shown adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.

X2680

**Figure 1: State Diagram for the TAP Controller**

## Boundary-Scan Hardware

### Test Access Port

The boundary-scan logic is accessed through the Test Access Port (TAP), which comprises four semi-dedicated pins: Test Mode Select (TMS), Test Clock (TCK), Test Data Input (TDI) and Test Data Output (TDO), as defined in the IEEE specification.

The TAP pins are permanently connected to the boundary-scan circuitry. However, once the device is configured, the connections may be ignored unless the use of boundary scan is specified in the design. See “[Using Boundary Scan](#)” on page 13-57.

If the use of boundary scan is specified, the TAP input pins (TMS, TCK and TDI) may still be shared with other logic, subject to limitations imposed by external connections and the operation of the TAP Controller. In designs that do not use boundary scan after configuration, the TAP pins can be used as inputs or outputs from the user logic in the FPGA device. TMS, TCK and TDI are available as unrestricted I/Os, while TDO only provides a 3-state output. In the XC5200 family, all four pins are available as I/O.

Before the FPGA is configured, it is important not to toggle the TAP pins (TDI, TMS, TCK), since these pins ‘turn-on’ boundary scan. Before an FPGA is configured, at a minimum, do not toggle TCK. Similarly, if boundary scan is enabled in a design after the FPGA is configured, care must be taken not to toggle the TAP pins (TDI, TMS, TCK) to prevent turning ‘on’ boundary scan by accident.

### TAP Controller

The TAP Controller is a 16-state machine that controls the operation of the boundary-scan circuitry in response to TMS. This state machine implements the state diagram specified by the IEEE standard ([Figure 1](#)) and is clocked by TCK.

Upon power-on, or if the boundary scan logic is not used in the application, the TAP controller is forced into the Test-Logic-Reset state. After configuration, the controller remains disabled, unless its use is explicitly specified in the user design. PROGRAM resets the latched decodes for EXTEST, CONFIGURE, and READBACK instructions.

Loading a 3-bit instruction into the Instruction Register (IR) determines the subsequent operation of the boundary-scan logic, [Table 1](#). The instruction selects the source of the TDO pin, and selects the source of device input and output data (boundary-scan register or input pin/user logic).

**Table 1: Boundary Scan Instructions**

Instruction	Test Selected	TDO Source	I/O Data Source
$I_2$	$I_1$	$I_0$	
0 0 0	EXTEST	DR	DR
0 0 1	SAMPLE/ PRELOAD	DR	Pin/Logic
0 1 0	USER 1	BSCAN.TDO1	User Logic
0 1 1	USER 2	BSCAN.TDO2	User Logic
1 0 0	READBACK	Readback Data	Pin/Logic
1 0 1	CONFIGURE	DOUT	Disabled
1 1 0	RESERVED	—	—
1 1 1	BYPASS	Bypass Register	—

$I_0$  is closest to TDO

Note: Whenever the TAP Controller is in the Shift-DR state, all data registers are shifted, regardless of the instruction. DR data is modified even if a BYPASS instruction is executed.

The instruction register is used not only to hold the current instruction. If the TAP is in the capture-IR state and TCK goes high, the instruction register captures the current boundary-scan state of the device.  $I_0$  is 1 by default.  $I_1$  is 0 by default.  $I_2$  is 0 if the device is in configure by boundary scan mode. Before and after configure by boundary scan mode,  $I_2$  will capture 1. Note that  $I_0$  is shifted out of TDO first, then  $I_1$ , and then  $I_2$ .

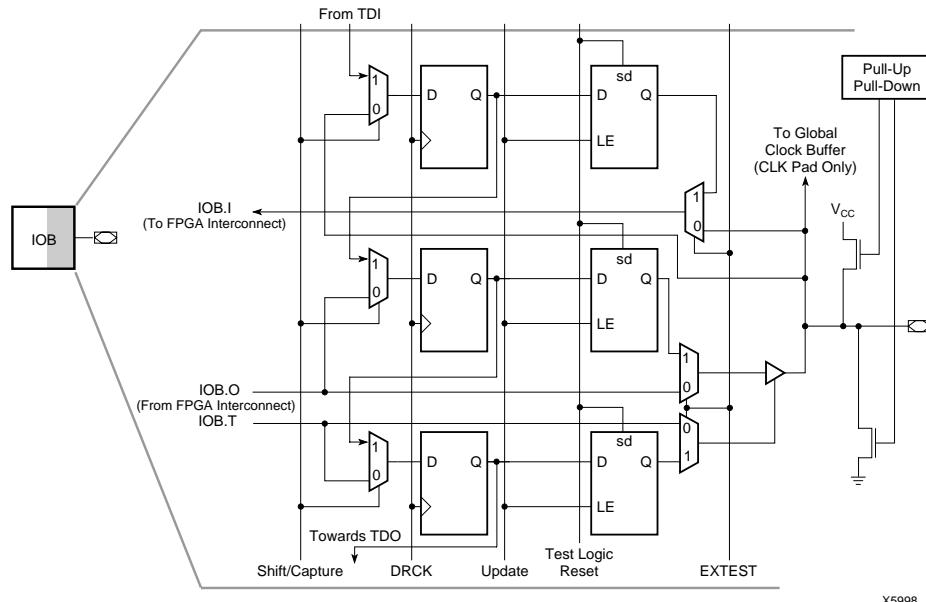
### The Boundary-Scan Data Register

The Data Register (DR) is a serial shift register implemented in the IOBs of the FPGA device, ([Figure 2](#)). Potentially, each IOB can be configured as an independently controlled bidirectional pin. Therefore, three data register bits are provided per IOB: for input data, output data and 3-state control. In practice, many of these bits are redundant, but they are not removed from the scan chain.

An update latch accompanies each bit of the DR, and is used to hold injected test data stable during shifting. The update latch is opened during the Update-DR state of the TAP Controller when TCK is Low.

In a typical DR instruction, the DR captures data during the Capture-DR state (on the rising edge of TCK). This data is then shifted out and replaced with new test data. Subsequently, the update latch opens, and the new test data becomes available for injection into the logic or the interconnect. The injection of data occurs only if an EXTEST instruction is in progress.

Note: The update latch is opened whenever the TAP Controller is in the Update-DR state, regardless of the instruction. Care must be exercised to ensure that appropriate data is contained in the update latch prior to initiating an EXTEST. Any DR instruction, including BYPASS, that is executed after the test data is loaded, but before the EXTEST commences, changes the test data.



X5998

**Figure 2: Boundary Scan Logic in a Typical IOB**

The IEEE Standard does not require the ability to inject data into the on-chip system logic and observe the results during EXTEST. However, this capability helps compensate for the lack of INTEST. Logic inputs may be set to specific levels by a SAMPLE/PRELOAD or EXTEST instruction and the resulting logic outputs captured during a subsequent EXTEST. It must be recognized, however, that all DR bits are captured during an EXTEST and, therefore, may change.

Pull-up and pull-down resistors remain active during boundary scan. Before and during configuration, all pins are pulled up. After configuration, the IOB can be configured with a pull-up resistor, a pull-down resistor or neither.

Note: Internal pull-up/pull-down resistors must be taken into account when designing test vectors to detect open circuit PC traces.

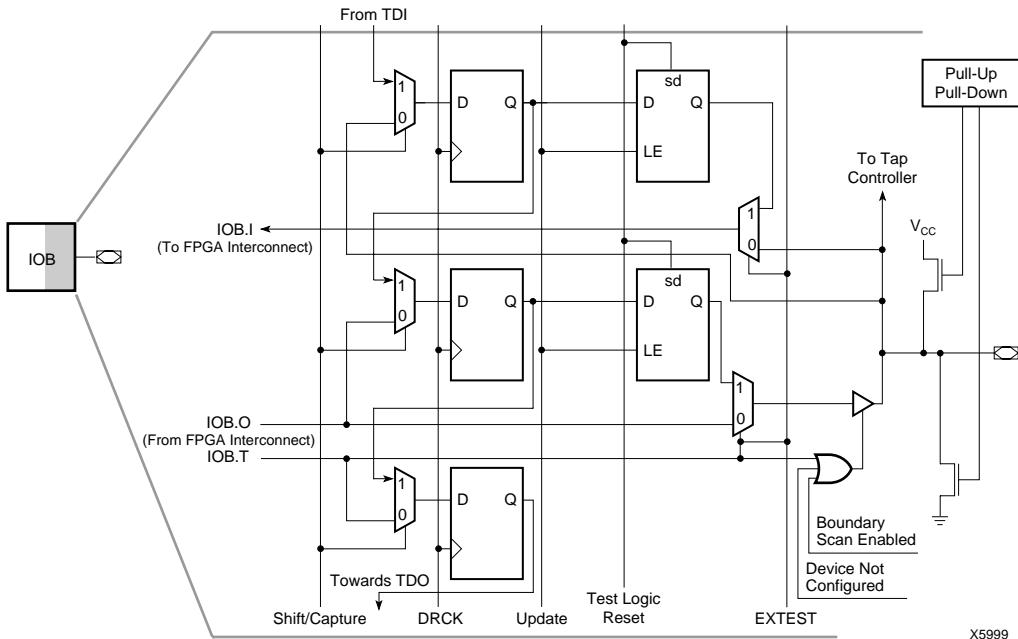
The primary and secondary global clock inputs (PGCK1-4 and SGCK1-4 in XC4000, GCK1-4 in XC5200) are taken directly from the pins, and cannot be overwritten with

boundary-scan data. However, if necessary, it is possible to drive the clock input from boundary scan. The external clock source is 3-stated, and the clock net is driven with boundary scan data through the output driver in the clock-pad IOB. If the clock-pad IOBs are used for non-clock signals, the data may be overwritten normally.

**Figure 3** shows the data-register cell for a TAP pin. An OR-gate permanently disables the output buffer if boundary-scan operation is selected. Consequently, it is impossible for the outputs in IOBs used by TAP inputs to conflict with TAP operation. TAP data is taken directly from the pin, and cannot be overwritten by injected boundary-scan data.

## Bit Sequence

**Table 2** lists, in data-stream order, the boundary-scan cells that make up the DR for the XC4000 Series. The cell closest to TDO corresponds to the first bit of the data-stream, and is at the top of the table. This order is consistent with the BSDL description.



X5999

**Figure 3: Boundary Scan Logic in a TAP Input (TMS, TCK, and TDI Only)**

Each IOB corresponds to three bits in the DR. The 3-state control is first (closest to TDO), the output is next, and the input is last. Other signals correspond to individual register bits. IOB locations assume that the die is viewed from the top, as in the device-level editors KDE or EPIC. In the XC4000, the input-only M0 and M2 mode pins contribute only the In bit to the boundary scan I/O register.

**Table 2: XC4000 Boundary Scan Order**

Bit 0 ( TDO end) Bit 1 Bit 2	TDO.T TDO.O  { Top-edge IOBs (Right to Left) { Left-edge IOBs (Top to Bottom) MD1.T MD1.O MD1.I MDO.I MD2.I { Bottom-edge IOBs (Left to Right) { Right-edge IOBs (Bottom to Top) B SCANT.UPD
(TDI end)	

X2674

Note: All IOBs remain in the DR, independent of whether they are actually used, or even bonded. Three bits, BSCANT.UPD, TDO.O and TDO.T, are included for Xilinx test purposes, and may be ignored by other users. CCLK, PROGRAM and DONE are not included in the boundary scan.

Tables in the data sheets show the DR order for all XC4000/XC5200 family devices. The DR also includes the following non-pin bits: TDO.T and TDO.I, which are always bits 0 and 1 of the DR, respectively, and BSCANT.UPD which is always the last bit of the DR.

## The Bypass Register

This is a 1-bit shift register that passes the serial data directly to TDO when a BYPASS instruction is executed.

## User Registers

The XC4000 and XC5200 boundary-scan instruction set includes two USERCODE instructions, USER1 and USER2. Connections are provided to the TAP and TAP controller that, together with direct connections to the TAP pins, permit the user to include boundary-scan self-test features in the design.

The XC4000 boundary scan symbol has six connections for user registers: SEL1, SEL2, TDO1, TDO2, DRCK and IDLE. TDI is available directly from the IOB that provides the TDI pin. The XC5200 boundary scan symbol has three

additional pins which make the creation of a user register easier: RESET, UPDATE, and SHIFT.

Note: The TDI signal supplied to user test logic is overwritten by boundary-scan test data during EXTEST. During user tests, it is not altered.

**SEL1, SEL2** – SEL1 and SEL2 enable user logic. They are asserted (High) when the instruction register contains instructions USER1 and USER2, respectively.

**TDO1, TDO2** – TDO1 and TDO2 are inputs to the TDO output multiplexer, permitting user access to the serial boundary-scan output. They are selected when executing the instructions USER1 and USER2, respectively. Input to user data registers can be derived directly from the TDI pin, thus completing the boundary-scan chain.

There is a one flip-flop delay between TDO1/TDO2 and the TDO output. This flip-flop is clocked on the falling edge of TCK.

**DRCK** – Data register clock (DRCK) is a gated and uninverted version of TCK. It is provided to clock user test-data registers. TDI data should be sampled with the falling edge of DRCK (rising edge of TCK). The TDO output flip-flop accepts data on the rising edge of DRCK (falling edge of TCK). DRCK is active only during the Capture-DR and Shift-DR states of the TAP controller. When not active in the XC4000, DRCK is Low. In the XC5200, when DRCK is not active, it is High.

**IDLE** – IDLE is a second gated and inverted version of TCK. It is active during the RUN-TEST/IDLE state of the TAP controller, and may be used to clock user test logic a set number of times, determined through TMS by the central test controller.

**RESET** - This pin is only available on the XC5200 boundary scan symbol. Whenever the TAP is in the TEST-LOGIC-RESET state, the RESET pin is High, in all other cases the RESET pin is Low.

**UPDATE** - This pin is only available in the XC5200 boundary scan symbol. Whenever the USER1 or USER2 instructions are used, UPDATE is an inverted version of TCK. In all other cases, UPDATE is Low.

**SHIFT** - This pin is only available in the XC5200 boundary scan symbol. When the USER1 or USER2 instructions are used, SHIFT is High, in all other cases SHIFT is Low.

## Using Boundary Scan

Full access to the built-in boundary-scan logic is always available between power-up and the start of configuration. Optionally, the built-in logic is fully available after configuration if boundary scan is specified in the design. At this time, user test logic is also available, and may be accessed through the boundary-scan port. During configuration, a reduced boundary-scan capability remains available: the SAMPLE/PRELOAD and BYPASS instructions only.

Figure 4 is a flow chart of the XC4000 FPGA start-up sequence that shows when the boundary-scan instructions are available. Since PROGRAM resets the TAP controller, boundary-scan operations cannot commence until PROGRAM has been taken High.

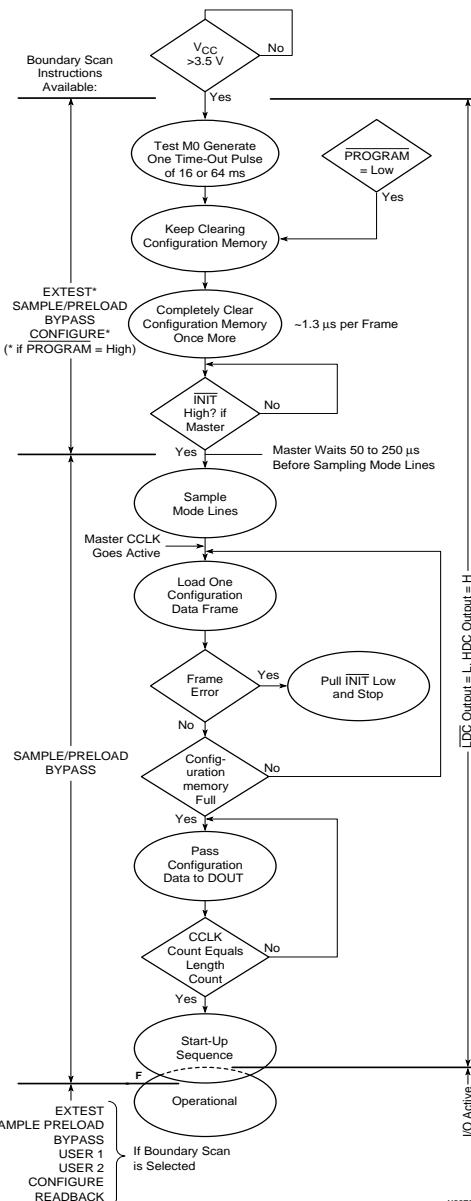


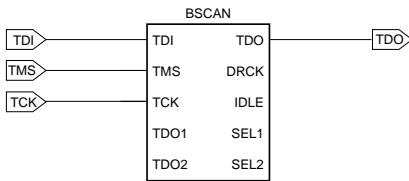
Figure 4: XC4000 Start-up Sequence

Full boundary-scan capabilities are available until INIT is High. Without external intervention, INIT automatically goes High after ~1 ms. If more time is required for boundary-scan testing, INIT may be held Low beyond this period by applying an external Low signal to the INIT pin until testing is complete. Once INIT has gone High, all clocks on the TCK pin are counted as configuration clocks for data and length count. See “**CONFIGURE**” on page 13-59. for more details.

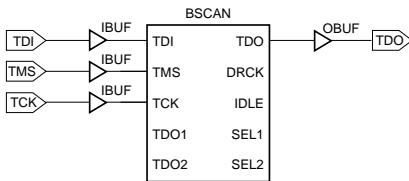
Boundary scan can be accessed before the FPGA is configured and after the FPGA is configured. If you want to access boundary scan before the device is configured, then when you power-up the device, hold the INIT pin Low until  $V_{CC}$  has risen to  $V_{CC}(\min)$ .

If you have already started configuring the device, and data frames are already being sent to the FPGA, then you have two choices. You can either access full-boundary scan mode, or limited boundary scan mode. If you want to access full-boundary scan mode, then both INIT and PROGRAM must be brought Low (Hold INIT and PROGRAM Low for over 300 ns and then release PROGRAM.) After releasing PROGRAM, continue to hold INIT Low while sending signals to the TAP. If you can use the limited boundary scan mode (which means you only can use the SAMPLE/PRELOAD and BYPASS instructions), then just bring INIT Low.

Accessing boundary scan after the device is configured has one requirement. The BSCAN symbol must be instantiated/inserted into your design with the correct syntax (see **Figure 5**). In this case, activating boundary scan after configuration amounts to toggling the TAP pins.



4k BSCAN Syntax for BSCAN after configure symbol



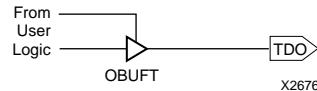
5k BSCAN Syntax for BSCAN after configure symbol

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**Figure 5: Boundary-Scan Schematic Symbols**

If the BSCAN symbol is not included, boundary scan is not selected, and the IOBs used by the TAP input pins are freely available as general purpose IOBs. The TDO output pin may be used as a logic output by explicitly connecting

the TDO pad primitive to an OBUF or OBUTF as required (see **Figure 6**.)



**Figure 6: Typical Non-Boundary-Scan TDO Connection**

## Boundary Scan Instructions

The XC4000/XC5200 boundary scan supports three IEEE-defined instructions (EXTEST, SAMPLE/PRELOAD and BYPASS), two user-definable instructions (USER1 and USER2), and two FPGA-specific instructions (CONFIGURE and READBACK). The instruction codes are shown in See **Table 1 on page 13-54**.

### EXTEST

While the EXTEST instruction is present in the IR, the data presented to the device output buffers is replaced by data previously loaded through the boundary-scan DR and stored in the update latch (**Figure 7**). Similarly, the output 3-state controls are replaced, and the data passed to internal system logic from input pins is replaced.

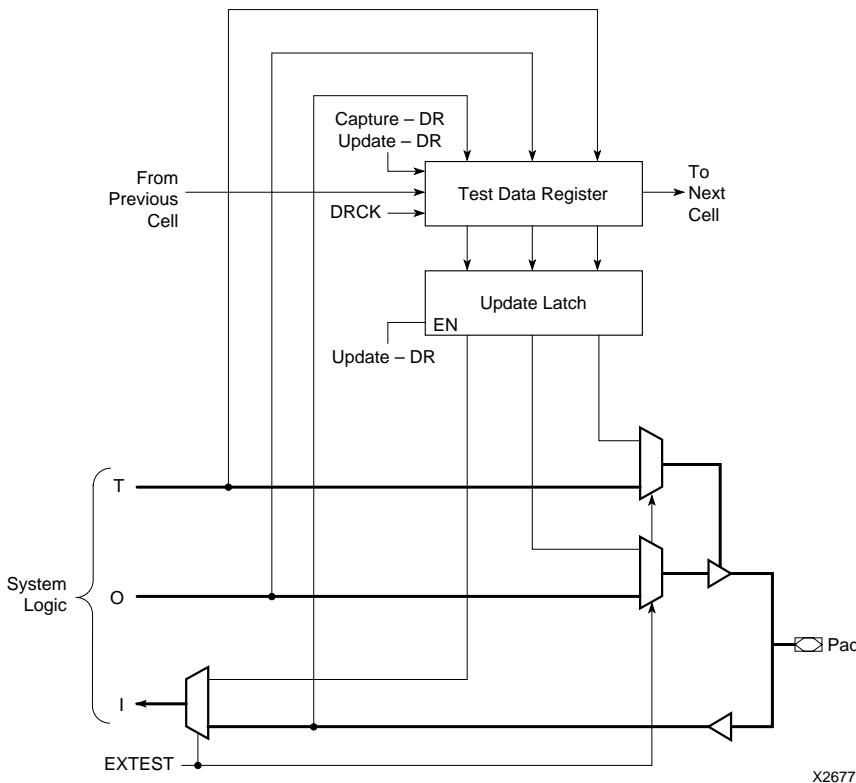
When a DR instruction cycle is executed, data arriving at the device input pins is loaded into the DR. The data from the system logic that drives output buffers and their 3-state controls is also loaded. This action occurs during the CAPTURE-DR state of the TAP controller (**Figure 1 on page 13-53**). Data is serially shifted out of the DR during the SHIFT-DR state; simultaneously, new data is shifted in. In the UPDATE-DR state, the new data is transferred into the update latch for use as replacement data, as described above.

The replacement of system data with update latch data starts as soon as the EXTEST instruction is loaded into the IR. For this data to be valid, it must have been loaded by a previous EXTEST or SAMPLE/PRELOAD operation.

Since the DR and update latch are modified during any DR instruction cycle, including BYPASS, the data in the update latch is only valid if it was loaded in the last DR instruction cycle executed before EXTEST is asserted.

The IEEE definition of EXTEST only requires that test data be driven onto outputs, that 3-state output controls be overridden, and that input data be captured. The capture of output data and 3-state controls and the forcing of test data into the system logic is normally performed during INTEST.

The XC4000/XC5200 effectively performs EXTEST and INTEST simultaneously. This added functionality permits the testing of internal logic, and compensates for the absence of a separate INTEST instruction. However, when performing an EXTEST, care must be taken as to what sig-



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**Figure 7: EXTEST Data Flow**

nals are driven into the system logic. Data captured from internal system logic must be masked out of the test-data stream before performing check-sum analysis.

## SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction permits visibility into system operation by capturing the state of the I/O. It also permits valid data to be loaded into the update register before commencing an EXTEST.

The DR and update latch operate exactly as in EXTEST (see above). However, data flows through the I/O unmodified.

## BYPASS

The BYPASS instruction permits data to be passed synchronously to the next device in the boundary-scan path. There is a 1-bit shift register between the TDI and TDO flip-flop.

## USER1, USER2

These instructions permit test logic, designed by the user and implemented in CLBs, to be accessed through the TAP.

Test clocks and paths to TDO are provided, together with two signals that indicate that user instructions have been loaded. See “User Registers” on page 13-56.

User tests depend upon CLBs and interconnect that must be configured to operate. Consequently, they may only be performed after configuration.

## CONFIGURE

Steps to follow to configure a Xilinx XC4000 or XC5200 device via JTAG:

The bitstream format is identical for all configuration modes. A user can use a *design.BIT* file or a *design.RBT* file, depending on whether the user wants to read a binary file (.BIT) or an ASCII file (.RBT).

1. Enable the boundary scan circuitry.

This can be done one of three ways, either during power-up, or by configuring the device with boundary scan enabled, or by pulling the PROGRAM pin low.

To enable boundary scan during power-up, hold the INIT pin Low when power is turned on. When V<sub>CC</sub> has

reached  $V_{CC(min)}$ , the TAP inputs can be toggled to enter JTAG instructions. The INIT pin can be held Low one of two ways, either manually or with a pulldown. If you choose to manually hold the INIT low, then the INIT pin must be held low until the CONFIGURE instruction is the current instruction. If you choose a pulldown, use a pulldown which pulls the INIT pin down to approximately 0.5V. The pulldown has the merit of holding INIT low whenever the FPGA is powered-up, and letting the user observe the INIT pin during configuration.

After the FPGA has been configured, if you want to reconfigure a configured device that has boundary scan enabled after configuration, then just start toggling the boundary scan TAP pins.

2. Load the Xilinx CONFIGURE instruction into the Instruction Register (IR).

The Xilinx CONFIGURE instruction is  $101(I_2\ I_1\ I_0)$ .  $I_0$  is the bit shifted first into the IR.

3. After shifting in the Xilinx CONFIGURE instruction, make the CONFIGURE instruction the current JTAG instruction by going to the UPDATE-IR state. When TCK goes low in the UPDATE-IR state, the FPGA is now in the JTAG configuration mode and will start clearing the configuration memory. The CONFIGURE instruction is now the current instruction, which must be followed by a rising edge on TCK. If you chose to manually hold the INIT pin Low, then the INIT pin must be held Low until the CONFIGURE instruction is the current instruction.
4. Once the Xilinx CONFIGURE instruction has been made the current instruction, the user must go to the RUN-TEST/IDLE state, and remain in the RUN-TEST/IDLE state until the FPGA has finished clearing its configuration memory.

The approximate time it takes to clear the FPGA configuration memory is:  $2 * 1 \text{ us} * (\text{number of frames per device bitstream})$ .

When the FPGA has finished clearing its configuration memory, the open-collector INIT has gone high impedance. At this point, the user should advance to the SHIFT-DR state. Once the TAP is in the SHIFT-DR state and the INIT pin has been released, clocks on the TCK pin will be considered configuration clocks for data and length count.

5. In the SHIFT-DR state, start shifting in the bitstream. Continue shifting in the bitstream until DONE has gone High and the startup sequence has finished.

During the time you are shifting in the bitstream via the TAP, the configuration pins LDC, HDC, INIT, PROGRAM, DOUT, and DONE all function as they normally do during non-JTAG configuration. These pins can be probed by the user. After completion of configuration, or

if configuration failed, the SAMPLE/PRELOAD instruction can be used to view these IOBs (except PROGRAM and DONE.)

LDC is Low during configuration. HDC is High during configuration. INIT will be high impedance during configuration, but if a CRC error or frame error is detected, INIT will go Low. If a pulldown is present on INIT then the user must probe INIT with a meter or scope. With a pulldown (as in step 1) attached to the INIT pin, the user will see a drop from approximately 0.5V to 0V if INIT drops Low to indicate a data error. PROGRAM can still be used to abort the configuration process. DOUT and TDO will echo TDI until the preamble and length count are shifted into TDI. After the preamble and length count have been shifted into the FPGA, DOUT will remain High. DONE will go High when configuration is finished. Until configuration is finished, DONE will remain Low.

### Additional Notes

(a) It is possible to configure several XC4000/XC5200 devices in a JTAG chain. But unlike non-JTAG daisy-chain configuration, this does not necessarily mean merging all the bitstreams into one bitstream. In the case of JTAG configuration of Xilinx devices in a JTAG chain, all devices, except the one being configured, will be placed in BYPASS mode. The one device in CONFIGURE mode will have its bitstream downloaded to it. After configuring this device it will be placed in BYPASS, and another device will be taken out of BYPASS into CONFIGURE.

(b) If you are configuring a long daisy-chain of JTAG devices (TDI connected to TDO of the previous device), the bitstream for the device with the CONFIGURE instruction may need to have its bitstream modified.

For example, assume that the a user has the following daisy-chain of devices:

```
source -----> device1 -----> device2 -----> device3
```

Device1's TDO pin is connected to device2's TDI pin, and device2's TDO pin is connected to device3's TDI pin.

The way to configure this chain is to place one device in CONFIGURE, and the other two in BYPASS. Further assume that device1 and device2 configure in this way, but device3 never configures. Specifically, device3's DONE pin never goes High. The problem is the bitstream length count. A possible cause, aside from bitstream corruption, is that the final value of the length count computed by the user/software was reached before the loading was complete.

There are two solutions. One solution involves just continually clocking TCK (for about 15 seconds) until DONE goes High. The other solution is to modify the bitstream; increase the length count by the number of devices ahead of the device under configuration.

In the preceding example, the user would increase the length count value by 2. (In a daisy-chain of devices configuring via boundary scan, devices in BYPASS will supply the extra 1s needed at the head of the bitstream.)

(c) In general for the XC4000 and XC5200, if you are configuring these devices via JTAG, finish configuring the device first before executing any other JTAG instructions. Once configuration through boundary scan is started, the configuration operation must be finished.

(d) If boundary scan is not included in the design being configured, then make sure that the release of I/Os is the last event in the startup sequence.

If boundary scan is not available, the FPGA is configured, and the I/Os are released before the startup sequence is finished, the FPGA will not respond to input signals and outputs will not respond at all.

(e) Re-issuing a boundary scan CONFIGURE instruction after the clearing of configuration memory will cancel the CONFIGURE instruction.

The proper method of re-issuing a CONFIGURE instruction after the configuration memory is cleared is to issue another boundary scan instruction, and follow it by the CONFIGURE instruction.

(f) If configuration through boundary scan fails, there are only two boundary scan instructions available: SAMPLE/PRELOAD and BYPASS. If another reconfiguration is to be attempted, then the PROGRAM pin must be pulled Low, or the FPGA must be repowered.

(g) When the CONFIGURE instruction is the current instruction, clocks on the TCK pin are not considered configuration clocks until the INIT pin has gone high impedance, and the TAP is in the SHIFT-DR state.

(h) If the user is attempting to configure a chain of devices, it is recommended that the user only configure the chain in all boundary scan mode, or use the non-boundary scan configuration modes. It is possible to configure a daisy-chain of devices, some in boundary scan and some in non-boundary scan configuration. Configuring in a mixed mode will not necessarily give the user a continuous boundary scan chain, which may or may not be a problem for a particular user's applications.

(j) Currently, there is no software to configure a Xilinx FPGA via the boundary scan pins. The user must provide this.

(k) Configuring a chain of Xilinx FPGAs via boundary scan does not require merging all the bitstreams into one bitstream, as in non-boundary scan configuration daisy-chains. When the FPGA is in boundary scan configuration, the same configuration circuitry used for non-boundary scan configuration is used. So, if a user would like, it is possible to merge all bitstreams into one bitstream, using the PROM File Formatter or MakePROM/promgen. In a case where the user wants to merge the bitstreams into one bit-

stream, the user should configure as in note (a) above. Additionally, the user will have to tie all INIT pins together. All DONE pins will also have to be tied together.

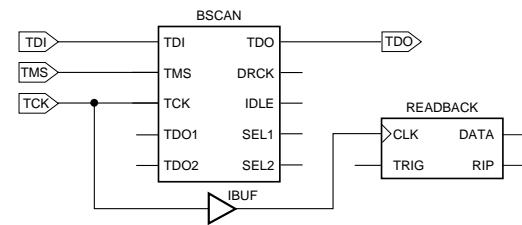
NOTE: The intention of configuration for a daisy-chain was to use either all the devices in boundary scan, or all the devices in non-boundary scan configuration.

## READBACK

Readback through boundary scan allows the user to access the readback features of the device, which would normally need to be accessed through user-specified pins. All limits of 'normal' readback are the same with readback through the TAP. Like regular readback, readback through the TAP is at a minimum of 100 KHz and at a maximum of 2 MHz. Like regular readback, the readback bitstream through boundary scan has the same format.

Unlike regular readback, which can be done repeatedly, readback through the TAP requires the following circuit:

1. In your schematic, or top-level synthesis design, instantiate the BSCAN and READBACK symbols.
2. Connect the BSCAN symbol pins TDI, TMS, TCK, and TDO to the boundary scan pads TDI, TMS, TCK, and TDO, respectively.
3. Next, connect the net between the TCK pad and TCK pin on the BSCAN symbol to an IBUF. Take the output of the IBUF and connect it to the CLK pin of the READBACK symbol. See [Figure 8](#).



- 4k BSCAN Symbol setup for multiple READBACKS through TAP.
- For the 5k, add IBUFs to TDI, TMS, and TCK. For TDO, add an OBUF. (see figure 5)

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**Figure 8: Symbol Setup for Multiple Readbacks**

For the XC5200, the equivalent circuit must be implemented using the XACT Design Editor (XDE) program EditLCA, or EPIC in the M1-based tools. After placing and routing your XC5200 design, load the *design.LCA* file into EditLCA, and follow the procedures below: (<ENTER> means hit the enter key on your keyboard)

(a) Once EditLCA has displayed the *design.LCA* file, type the following:

eb bscan <ENTER>

This will bring up the Editblock window for the XC5200 BSCAN symbol.

(b) In the Editblock window, select the 'used' option, which is in the upper left corner of the screen.

(c) Now type:

```
endb <ENTER>
```

This brings you back to the EditLCA screen.

(d) Next type the following:

```
addnet username tckpin.i rdbk.ck <ENTER>
```

where tckpin is the pin number of the TCK pin of your XC5200 device. 'username' is a net name of your choice. For example, if your design used an XC5202PC84, then the above command line would be:

```
addnet mynet p16.i rdbk.ck <ENTER>
```

(e) At this point you should see a net go from the TCK pin to the CK pin of the Readback symbol.

(f) Save your changes to the LCA file and exit XDE.

4. After entering the above circuit, compile the design to an LCA file.

5. Make the bitstream file for the LCA file by using the following option with makebits, or use the M1 Bitstream Generator:

```
-f readclk:rdbk
```

For example, at a unix prompt:

```
% makebits -f readclk:rdbk design
```

6. Now the FPGA is ready to perform consecutive readbacks.

Readback is performed by loading the IR with the READBACK instruction and then shifting out the captured data from the SHIFT-DR state in the TAP. Readback data is captured when READBACK is made the current instruction in the TAP.

Perform the first readback by loading the IR with the READBACK instruction. This first readback must be finished, which means shifting out the \*entire\* readback bitstream. To be safe, shift out the entire bitstream and then send three additional TCKs.

7. After performing the first readback, another readback can be performed by going to the TEST-LOGIC-RESET state, and re-loading the READBACK instruction and performing the Readback as described in the previous paragraph.

In summary, consecutive readbacks are performed by starting from TEST-LOGIC-RESET, loading the IR with the READBACK instruction, shifting out the readback bitstream plus three additional TCKs, and then going back to the TEST-LOGIC-RESET state.

Alternatively, if you do not want to go back to the TEST-LOGIC-RESET state, realize that after shifting out the readback bitstream, a minimum of three additional clocks are needed on the readback register. So, after doing a readback, instead of going back to TEST-LOGIC-RESET, a user can opt to execute some other JTAG instruction, and then perform another readback.

Also, this procedure is only needed if you intend to do more than one readback. If you intend only do a readback once, then the connection between the BSCAN symbol and the READBACK symbol is not needed. In that case, all that is needed is the BSCAN symbol instantiated with the boundary scan pads (TDI, TMS, TCK, & TDO) on the top level of the design.

## Boundary Scan Description Language Files

Boundary Scan Description Language (BSDL) files describe boundary-scan-capable parts in a standard format used by automated test-generation software. The order and function of bits in the boundary-scan data register are included in this description.

BSDL files are available in the Xilinx File Download area via the Xilinx WebLINX web site ([www.xilinx.com](http://www.xilinx.com)).

## Bibliography

The following publications contain information about the IEEE Standard 1149.1, and should be consulted for general boundary-scan information beyond the scope of this application note.

Colin M. Maunder & Rodham E. Tulloss. *The Test Access Port and Boundary Scan Architecture*. IEEE Computer Society Press, 10662 Los Vaqueros Circle, P.O. Box 3014, Los Alamitos, CA 90720-1264. See [www.computer.org/cspres/catalog/st01096.htm](http://www.computer.org/cspres/catalog/st01096.htm)

John Fluke Mfg. Co. Inc. *The ABC of Boundary Scan Test*. John Fluke Mfg. Co. Inc., P.O. Box 9090, Everett, WA 98206.

GenRad Inc. *Meeting the Challenge of Boundary Scan*. GenRad Inc., 300 Baker Ave., Concord, MA 01742-2174.

Ken Parker. *The Boundary Scan Handbook*. Kluwer Academic Publications, (617) 871-6600.

IEEE Standards, [standards.ieee.org](http://standards.ieee.org)

Texas Instruments, [www.ti.com/sc/docs/jtag/jtaghome.htm](http://www.ti.com/sc/docs/jtag/jtaghome.htm)