California State University, Sacramento
The College of Engineering and Computer Science

CPE 166 Advanced Logic Design

Midterm

Fall 2020

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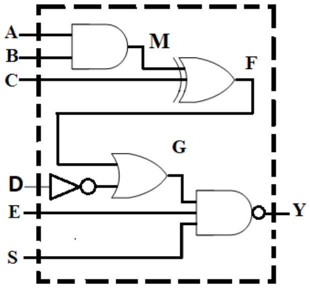
1. [23 points]. (1). Write the Verilog program for the following combinational circuit.



```
module cir1 (A, B, C, D, E, S, Y );

input   ______A,B,C,D,E,S__________________________;

output _______Y_________________________;

wire    ________M,F,G_________________________;

assign   M = _______A & B_____________________ ;

assign   F  =  ______M ^ C______________________;

assign   G = ________F | ~D_____________________;

assign  Y =  ________~ (G & E & S)_____________________;

endmodule
```

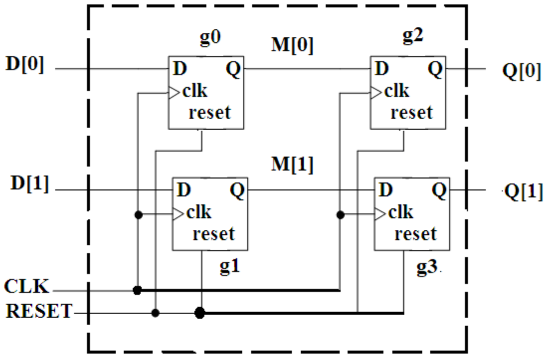
(2). Complete the testbench for the above circuit to generate testing cases for all possible values of A, B, C, D, E, and S.

```
module  tb;

__reg_______    A, B, C, D, E, S;
_wire________     Y;
__integer_______      i;

_ex1 uut( .A(A), .B(B),  .C(C), .E(E), .S(S)) ______________;

initial
begin
        { A, B, C, D, E, S } = __0__________________ ;
         for ( i=0;   i <  ___64________;  i=i+1)
         begin
                 #5      _______A,B,C,D,E,S_________________;
         end
         #5  $stop;
end
endmodule
```

2.[27 points] Use Verilog hierarchical design method to design the following circuit.
1). Design clock rising edge triggered 1-bit D FlipFlop with asynchronous reset.

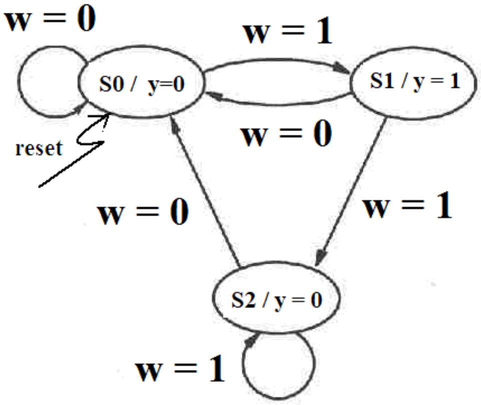
```
module dff (D, clk, reset, Q);
 input        ______D,clk,reset_________________;
 output        ________Q_______________;
 reg           ________Q_______________;

always@(  __posedge_____clk________    or  _________posedge reset___________ )
begin
        if (reset)
                  ___Q <= 1'b0 ______________;
       else
                  ___Q <= D;______________;
end
endmodule
```

2). Use dff above to implement the following circuit and complete the Verilog design.



```
module cir2 (D, CLK, RESET, Q);
input           ___[1:0]D_______________;
input          ___CLK, RESET_______________;
output        ____[1:0]Q_______________;
wire          _____[1:0]M______________ ;

dff      g0(.D(D[0]), .clk(CLK), .reset(RESET), .Q(M[0]));

dff      g1(.D(D[1]), .clk(CLK), .reset(RESET), .Q(M[1]));

dff      g2(.D(M[0]), .clk(CLK), .reset(RESET), .Q(Q[0]));

dff      g3(.D(M[1]), .clk(CLK), .reset(RESET), .Q(Q[1]));

endmodule
```

3. [30 points] A finite state machine is described using a state diagram shown below.



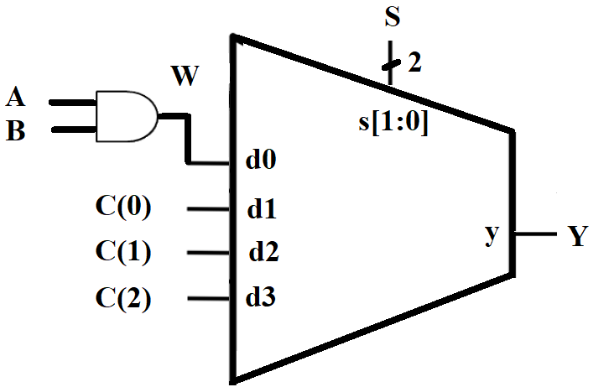
Write the complete Verilog code for the above finite state machine.

```
module fsm(reset, clk, w, y);
    input reset, clk, w;
    output y;
    reg y;

    reg [1:0] cs, ns;
    parameter S0=2b'00, S1=2'b01, S2=2'b10;
    always@(cs)
    begin
        case(cs)
            S0: y=0;
            S1: y=1;
            S2: y=0;
            default y=0;
        endcase
    end

    always@(cs or w)
    begin
        case(cs)
            S0: if(w) ns=S1;
                else ns=S0;
            S1: if(w) ns=S2;
                else ns=S0;
            S2: if(w) ns=S2;
                else ns=S0;
            default: ns=S0;
        endcase
    end
```

```
// continue your code here.
```

always@(posedge clk or posedge reset)
begin
   if(reset) cs <= S0;
   else cs <=ns;
   end
end module	

4. [20 points] Complete the following circuit design in VHDL.



Library __IEEE________________________________;
Use   ____IEE.STD_LOGIC_1164.ALL______________________________;

_entity_________ cir4 is
        Port (A, B: _in std_logic_____________________________;
                C: _in std_logic_vector [2 downto 0]_____________________________;
                S: _in std_logic_vector[1 downto 0]_____________________________;
                Y: _ out std_logic_____________________________);
End cir4;

_ architecture___________ design of ____cir4______ is

_signal_________ W: ___std_logic______________________________;

Begin

W <= ________A and B__________________________;

Y <= ____W_____________ when ____S='00'__________ else

```
                    ________C(0)________  when  ______S=’01’_______  else

                    _______C(1)_________  when  _____S=’10’________  else

                    _____C(2)___________ ;

end design;
```