# California State University, Sacramento The College of Engineering and Computer Science

## **CPE 186 Computer Hardware Design**

Midterm

Fall 2020

Student Name: Shammah Thao

	[36 points] Each of correct answer.	f the following questions onl	y has one correct answer. Please	select the			
rate i	With PCI Bus width s going to be 32 MBps	n of 64 bits and running at m. B. 264 MBps	aximum 33MHz, the maximum d C. 512 MBps	ata transfer			
	/hen IRDY# gets a <mark>itiator</mark>	sserted, it indicates which of B. Target	the following agent is ready for t C. None	transaction?			
<ul> <li>3). What is the functionality of C/BE[3:0]?</li> <li>A. Defines the PCI command during address phase.</li> <li>B. Indicate byte enable during address phase.</li> <li>C. None of the above.</li> </ul>							
<ul> <li>4). For PCI Express (PCIe) Transactions:</li> <li>A. Memory Read is Posted Transaction.</li> <li>B. IO Read is Non-Posted Transaction.</li> <li>C. Configuration Write is Posted Transaction.</li> </ul>							
<ul> <li>5). Sequence Number is first added into the TLP packet by the PCIe transmitter at the</li> <li>A. Transaction Layer</li> <li>B. Data Link Layer</li> <li>C. PHY Layer</li> </ul>							
6). PCIe TLP maximum data payload transfer size is A. 2 DW B. 3 DW C. 1024 DW							
<ul><li>7). FRAME# is used to signal</li><li>A. only start of a transaction B. only end of a transaction</li><li>C. the start and end of a transaction.</li></ul>							
	CIe Type 0 configu Base Address Reg	-	Registers C. 6 Base Address F	Registers			
,	CIe TLP header siz Words or 8 Words		C. 4 DW or 5 DW				
<mark>А. Т</mark> В. І	PCIe replay buffer Transaction Layer Data Link Layer PHY Layer	is located inside the					

- 11). Suppose a legacy device ABC is restricted to the lower 16 bits of PCIe IO address space. This means, the device ABC supports
- A. 64 GB IO address space
- B. 64 MB IO address space
- C. 64 KB IO address space

b=1;

#10; a=1; b=1;

#10 \$stop;

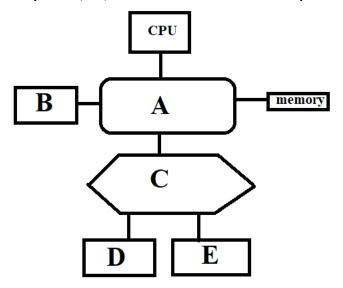
- 12). Which of the following statement about PCIe is correct?
- A. The transmitter uses a 2-bit Replay Number counter, referred to as the REPLAY\_NUM counter, to keep track of the number of replay events.
- B. The transmitter uses a 8-bit Replay Number counter, referred to as the REPLAY\_NUM counter, to keep track of the number of replay events.
- C. The transmitter uses a 12-bit Replay Number counter, referred to as the REPLAY\_NUM counter, to keep track of the number of replay events.
- D. The transmitter uses a 20-bit Replay Number counter, referred to as the REPLAY\_NUM counter, to keep track of the number of replay events.

```
[24 points].
`timescale 1 ns / 1 ns
module cir(a, b, f);
 input a, b;
 output f;
 assign f = \sim (a \& b);
endmodule
(1). Write a general verilog testbench for the above circuit without
using any task. You must include all four testing cases for a and b.
module cir tb;
module cir tb;
reg a,b;
wire f;
cir utt(a,b,f);
initial begin
a=0;
b=0;
#10;
a=1;
b=0;
#10;
a=0;
```

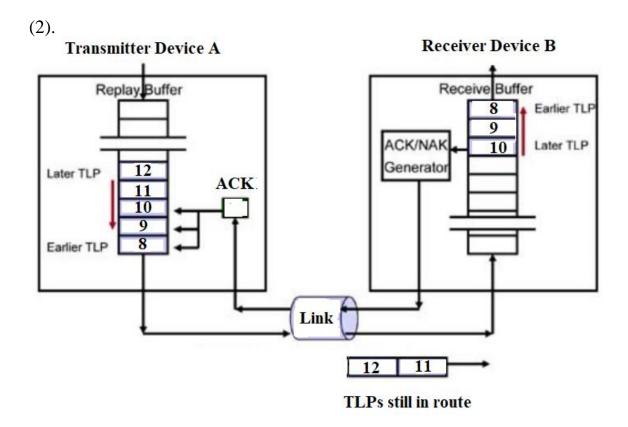
end endmodule

```
(2). Modify the above testbench by using task called "test" below to
rewrite your testbench.
`timescale 1 ns / 1 ns
module cir tb;
 reg __a,b____;
 wire \overline{f};
 cir g1 ( ___a__, __b___, f);
 initial begin
  a = 0; b = 0;
  #10 test( f, 1 );
  a = 0; b = 1;
  #10 test( f, _____0__);
a = 1; b = 0;
  #10 test( f, ____0__);
a = 1; b = 1;
  #10 test( f, ____1__);
  #10 $stop;
 end
task test;
// Write a task in Verilog of "test" which compares two input data
// values, one is from generated testing output result and another
// one is from expected testing result and find out if they are equal.
// If the two values are not equal, display the simulation time,
// the error massage, as well as the testing values of a and b.
Task check res;
input data;
input res;
begin
       if(data!=res)
               $display($time, "ns, Error: a=%b, b=%b, Expected value =
%d, Actual value = %d n", a, b, res, data);
end
endtask
endmodule
```

- 3. [40 points]
- (1). Fill out 5 blanks with different PCIe hardware unit names of Endpoint (EP), Switch, and Root Complex in the diagram below.



	Root ComplexSwitch	 B:Legacy EndPoint,
D :	PCI-XP Endpoint	E: PCI-XP Bridge to PCI



Device A transmits TLPs with Sequence Numbers 8, 9, 10, 11, 12 where TLP 8 is the first TLP sent and TLP 12 is the last TLP sent.

Device B receives TLPs with Sequence Numbers 8, 9, 10 in that order. TLP 11, 12 are still en route.

Device B performs the error checks and collectively acknowledges good receipt of TLPs 8, 9, 10.

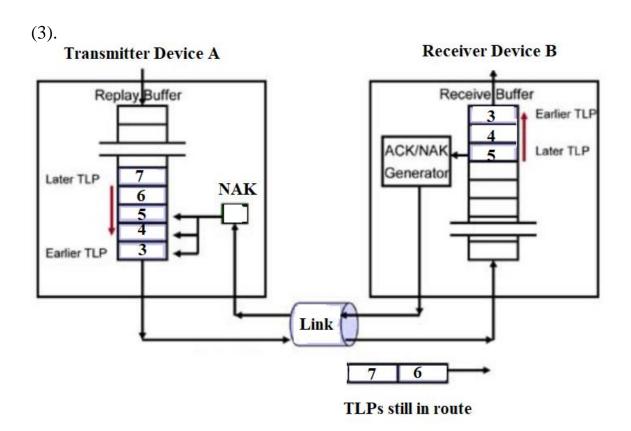
i. What sequence number will Device B return with in its ACK DLLP packet?

Your Answer: sequence number 11.

ii. What will Device A do with the TLP packets in its replay buffer after it receives the above ACK information successfully?

### Your Answer:

A will clear 8,9,10 from its buffer and remain with 11, 12. It will then send sequence number 11 followed by sequence number 12.



Device A transmits TLPs with Sequence Numbers 3, 4, 5, 6, and 7. Device B receives TLP 3 with no error. However, it receives TLP 4 with a CRC error. Device B schedules the return of a NAK DLLP with a Sequence Number.

i. What sequence number will Device B send to Device A in its NAK DLLP packet?

Your Answer: sequence number \_\_\_\_\_4\_\_

ii. What will Device A do with the TLP packets 3, 4, 5, 6, and 7 in its replay buffer after it receives the above NAK information successfully?

### **Your Answer**:

Buffer accepts all the packet which is send after 4 but it sends every time negative acknowledge until it will not get the correct packet of 4. So, Device A has only packet 4 in Replay buffer.

(4). The receiver Device B returns an ACK/NAK DLLP to the Device A, but the remote transmitter Device A detects a CRC error in the DLLP. What will the transmitter Device A do after detecting CRC error in its received ACK/NAK DLLP?

#### **Your Answer**:

If DLLP CRC error is detected, the DLLP is discarded and an error is reported