California State University, Sacramento
The College of Engineering and Computer Science

CPE 186 Computer Hardware Design

Final Exam

Fall 2020

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1. [14 points]

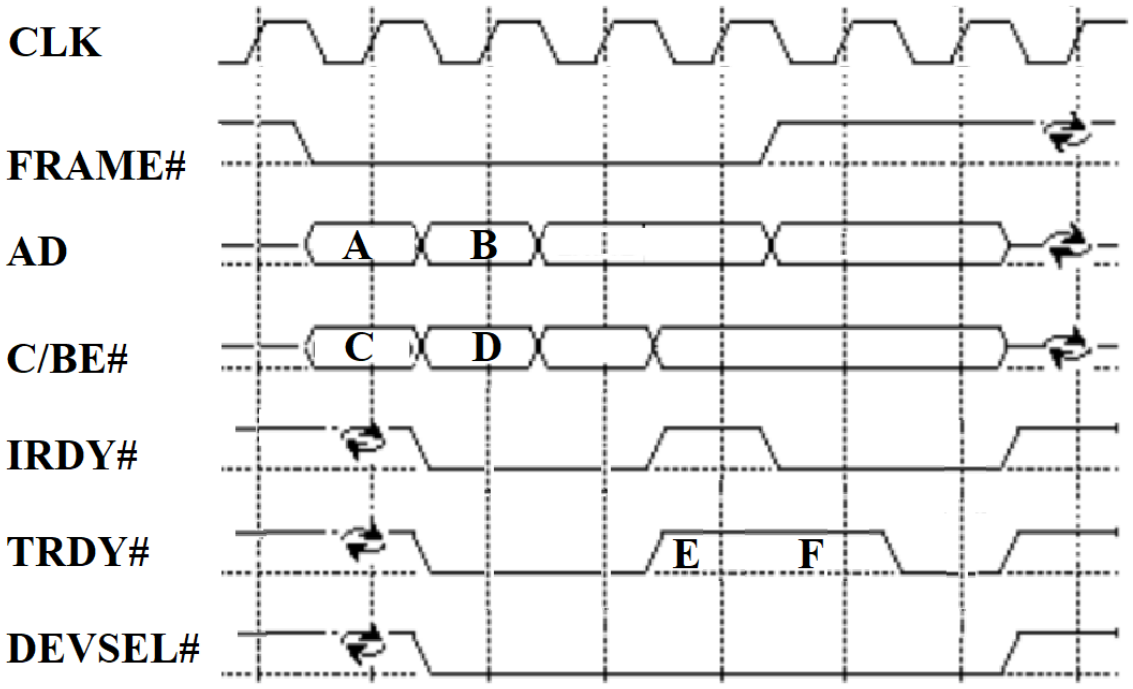
(1). The following waveform is used for PCI bus write transaction. Fill out each of the 5 blocks indicated on the waveform with one of the functionality names below:

WAIT STATE, COMMAND, DATA, ADDRESS, BYTE ENABLE.

A: _____address_____ B:_____data 1_____

C: _____byte COMMAND_____ D: ____byte enable_____

E: _____Wait state_____ F: ___wait state_____



(2). Is the above transfer burst transfer or not?

Your answer: _____yes_____

2. [30 points] Each of the following questions only has one correct answer. Please select the correct answer.

1). Which of the following statements about AD bus is correct?

A. The AD bus is only used as address for PCI transaction.

B. The AD bus is only used as data for PCI transaction

C. The AD bus is used as address during the address phase and it is used as data during the data phase for PCI transaction.

D. None of the above is correct.

2). How many interrupt request signals does the PCI bus supports?

A. 6 (INTA#, INTB#, INTC#, INTD#, INTE#, INTF#)

B. 1 (INTA#)

C. 4 (INTA#, INTB#, INTC#, INTD#)

D. 3 (INTA#, INTB#, INTC#)

3). Which statement about MSI below is correct?

A. A MSI enabled PCI Express device will manage interrupts with a central bus controller to monitor the req# signal, and obtain bus control by using the gnt#, which is in the same way as specified by the PCI bus standard.

B. A MSI enabled PCI Express device will assert INTA# and then deassert INTA# for interrupt.

C. Each MSI interrupt is associated with one IRQ Line Number.

D. None of the above.

4). Which statement about PCIe data transfer below is correct?

A. Data is transmitted in parallel on PCIe physical lane in the same manner as the PCI bus standard.

B. Data is transmitted serially on PCIe physical lane in the same manner as the PCI bus standard.

C. Data is transmitted serially on the PCIe physical lane, which is different from the parallel data transmission used in the PCI bus standard

5). Which statement about flow control below is correct?

A. Flow Control Packet is a type of TLP

B. Flow Control Packet is a type of DLLP.

C. When the transmitter sends data, it will increase the credits based on the amount of data sent.

D. None of the above.

6). Which statement shown below is correct?

A. Control character COM indicates last character in any ordered-set

B. Control character PAD indicates electrical idle ordered-set

C. For PCIe x1 Packet and x4 packet, END Control character must end at lane 3.

D. None of the above

7). Completion Time-Out is

A. Non-Fatal uncorrectable error B. Correctable error C. Fatal uncorrectable error

8). When Bad DLLP Mask in the advanced correctable error mask register is set to 1

A. Bad DLLP error is allowed to be generated

B. Bad DLLP error is not allowed to be generated

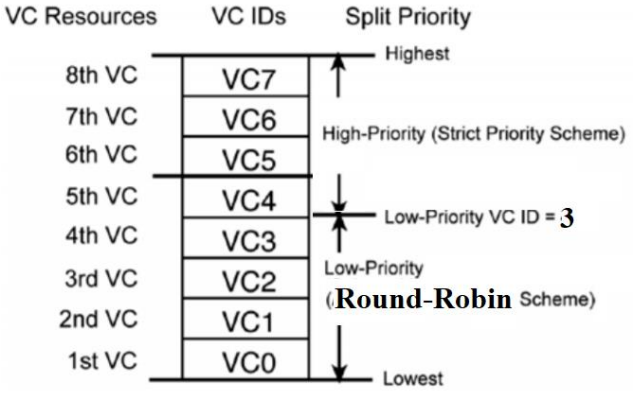
C. Bad DLLP error is allowed to be reported

D. Bad DLLP error is not allowed to be reported

9). Which of the following PCIe error handling mechanisms is correct?
A. Uncorrectable errors-nonfatal are handled by hardware.
B. Uncorrectable errors-fatal are handled by hardware.
C. Correctable errors are handled by hardware.

10). For EMC consideration, we should
A. Increase digital circuit current to be powerful enough to avoid EMI
B. Increase digital circuit loop area to be powerful enough to avoid EMI
C. Decrease digital circuit frequency to reduce EMI
D. None of above

3. [18 points] Suppose PCIe Virtual Channel Arbitration with Low and High-Priority Implementation is shown below.



(1). For VC7, VC6, VC5, and VC4, which VC has the lowest priority? Your Answer:
___VC4_____

(2). For VC6, VC5, VC1, and VC0, which VC has the highest priority? Your Answer:
____VC6_____

(3). Suppose most recently, VC7 was granted by the VC arbiter.
Then if currently, VC7, VC6, VC5, and VC4 send requests at the same time, which VC will be granted by the VC arbiter? Your Answer:
___VC6_____

(4). Suppose most recently, VC3 was granted by the VC arbiter. Then if currently, VC3, VC2, VC1, VC0 send requests at the same time, which VC will be granted by the VC arbiter?
Your Answer: ____VC2_____

(5). Suppose most recently, VC7 was granted by the VC arbiter. Then if currently, VC0, VC2, VC4, VC6 send requests at the same time, which VC will be granted by the VC arbiter?
Your Answer: _____VC6_____

(6). Suppose most recently, VC3 was granted by the VC arbiter. Then if currently, VC0, VC2, VC4, VC6 send requests at the same time, which VC will be granted by the VC arbiter?
Your Answer: _____VC6_____

4. [38 points] Complete blanks and also Verilog design below.

(1). 8b/10b Encoder will translate 32 bits data into _____40_____ bits.

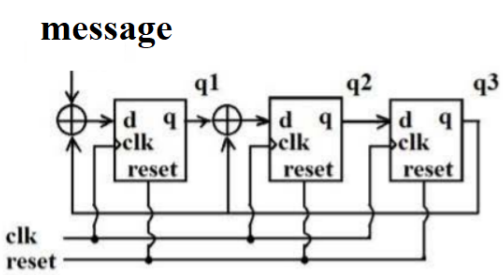
(2). 2.5 Gb/s PCIe transport lane consists of _____2.5_____Gb/s of 8b/10b encoded user data.

(3). Complete Verilog design below to implement the FIFO controller to control 4K (4096) different memory locations.

```
module fifo(clk, rst, wr, rd, full, empty, w_addr, r_addr);
input    clk, rst, wr, rd;
output   full, empty;

output [11:0]  w_addr, r_addr;
reg    [12:0]  w_ptr, r_ptr;

always@(posedge clk or posedge rst)
begin
  if(rst)
  begin
    w_ptr <= 0;
    r_ptr <= 0;
  end
  else
    if(wr && !full)
      w_ptr <= w_ptr + 1;
    if(rd && !empty)
      r_ptr <= r_ptr + 1;
end

assign full = ((r_ptr!=w_ptr) && (r_ptr[11:0]==w_ptr[11:0]))?1:0;
```

```
assign empty = (r_ptr==w_ptr) ? 1 : 0;

assign w_addr = w_ptr[2:0];
assign r_addr = r_ptr[2:0];

endmodule
```

(3). The message data value "11001" is sent to the following circuit through the serial input "message". Assume that the initial values of q1, q2, and q3 are "111".
When reset = 0, please fill in the values of q1, q2 and q3 in the following table on the rising edge of the clk in different clock cycles.

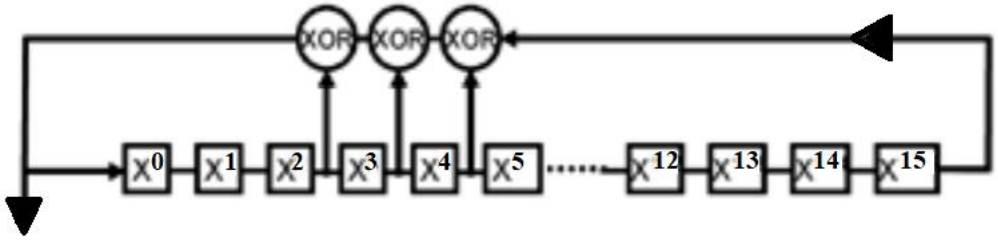


clock cycle	message	q1	q2	q3
0	1	1	1	1
1	1			
2	0			
3	0			
4	1			

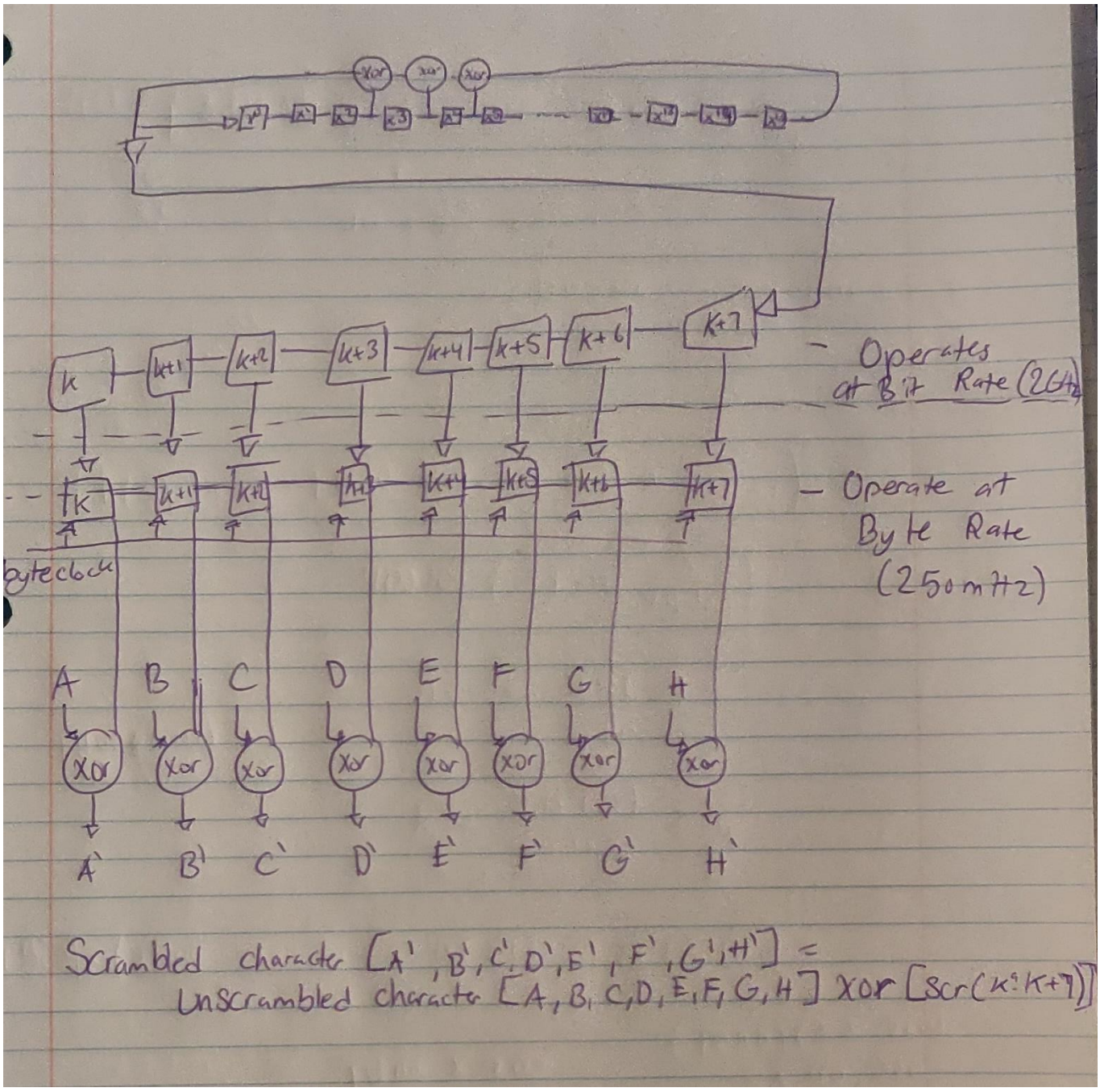
Clock cycle	Message	Q1	Q2	Q3
0	1	1	1	1
1	1	0	1	1
2	0	1	0	0
3	0	0	0	0
4	1	1	1	1

(4). PCIe transmitter scrambles data and generates data outputs of A' B' C' D' E' F' G' H'.
The circuit below shows the LFSR circuit used by the receiver to un-scramble data. Complete the circuit schematic to show how the **receiver** unscramble data from A' B' C' D' E' F' G' H' to get the original data of A B C D E F G H.

Suppose the clock frequency of the LFSR is 2 G Hz.



BELOW



Scrambled character [A', B', C', D', E', F', G', H'] =
UnScrambled character [A, B, C, D, E, F, G, H] XOR [Scr(K:K+7)]