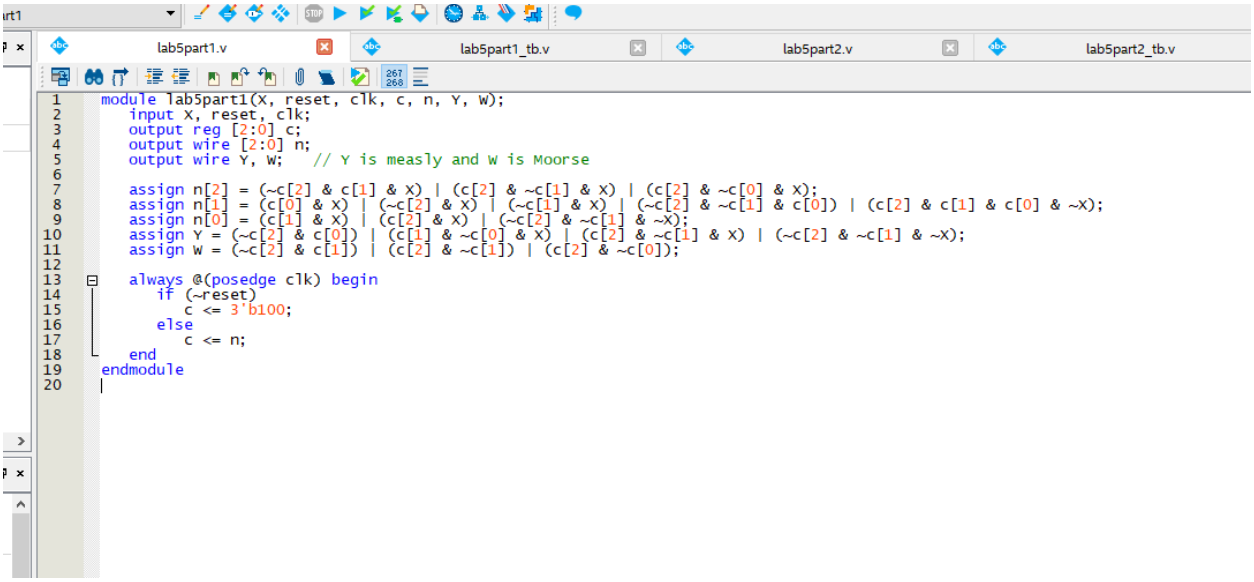
Shammah Thao

Cpe64

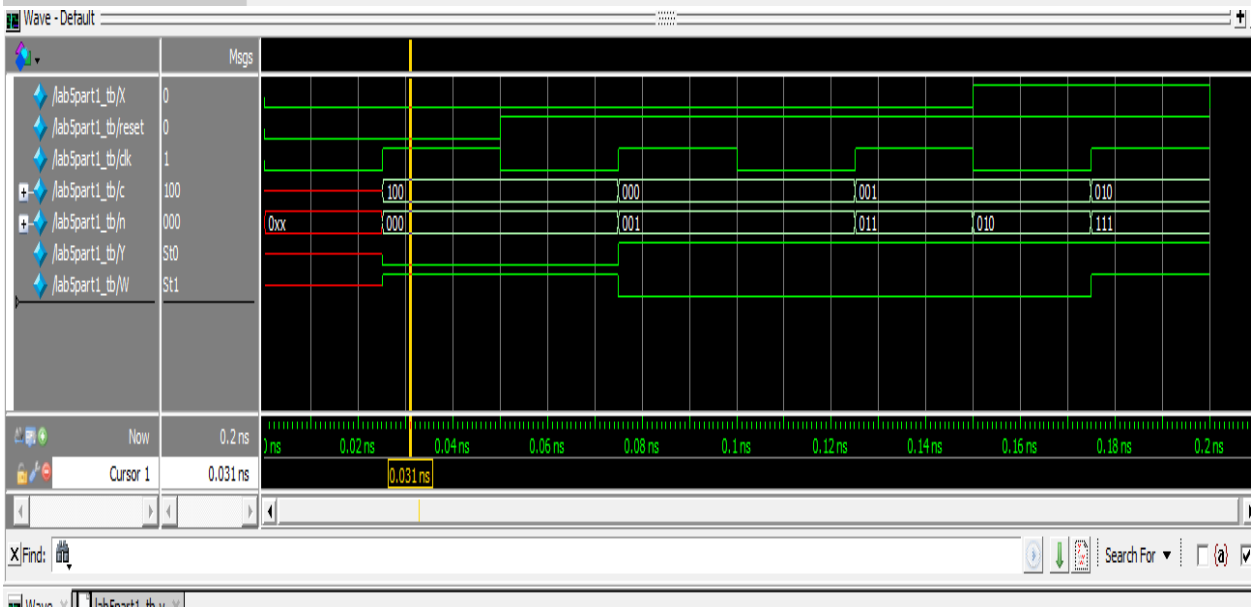
Part 1:



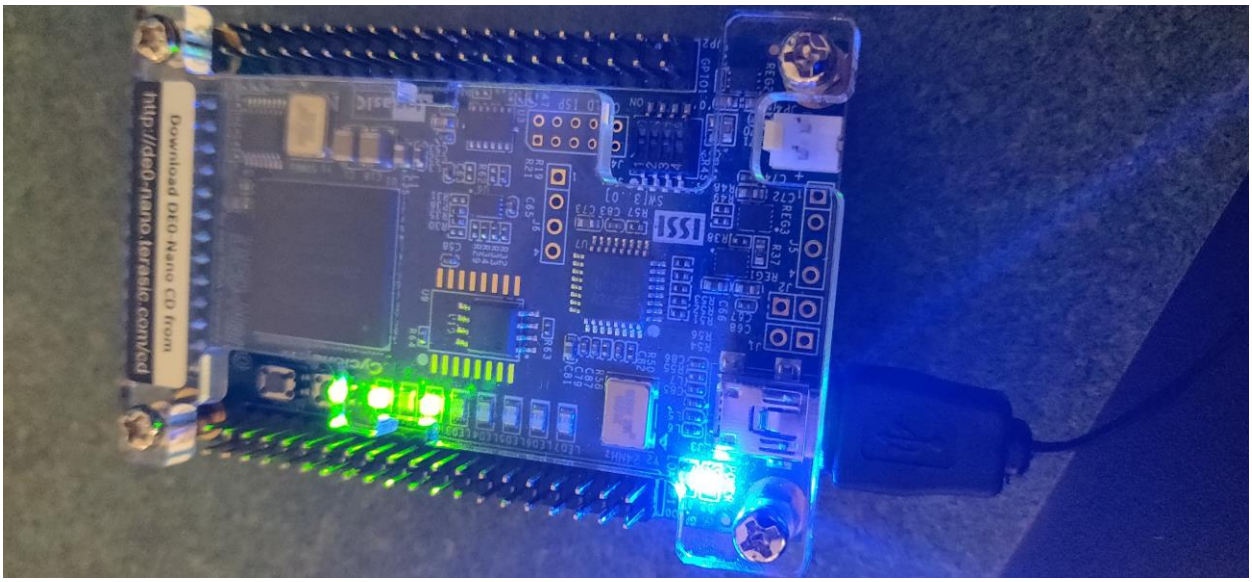

```
module lab5part1(X, reset, clk, c, n, Y, W);
   input X, reset, clk;
   output reg [2:0] c;
   output wire [2:0] n;
   output wire Y, W;   // Y is measly and W is Moorse

   assign n[2] = (~c[2] & c[1] & X) | (c[2] & ~c[1] & X) | (c[2] & ~c[0] & X);
   assign n[1] = (c[0] & X) | (~c[2] & X) | (~c[1] & X) | (~c[2] & ~c[1] & c[0]) | (c[2] & c[1] & c[0] & ~X);
   assign n[0] = (c[1] & X) | (c[2] & X) | (~c[2] & ~c[1] & ~X);
   assign Y = (~c[2] & c[0]) | (c[1] & ~c[0] & X) | (c[2] & ~c[1] & X) | (~c[2] & ~c[1] & ~X);
   assign W = (~c[2] & c[1]) | (c[2] & ~c[1]) | (c[2] & ~c[0]);

   always @(posedge clk) begin
      if (~reset)
         c <= 3'b100;
      else
         c <= n;
   end
endmodule
```

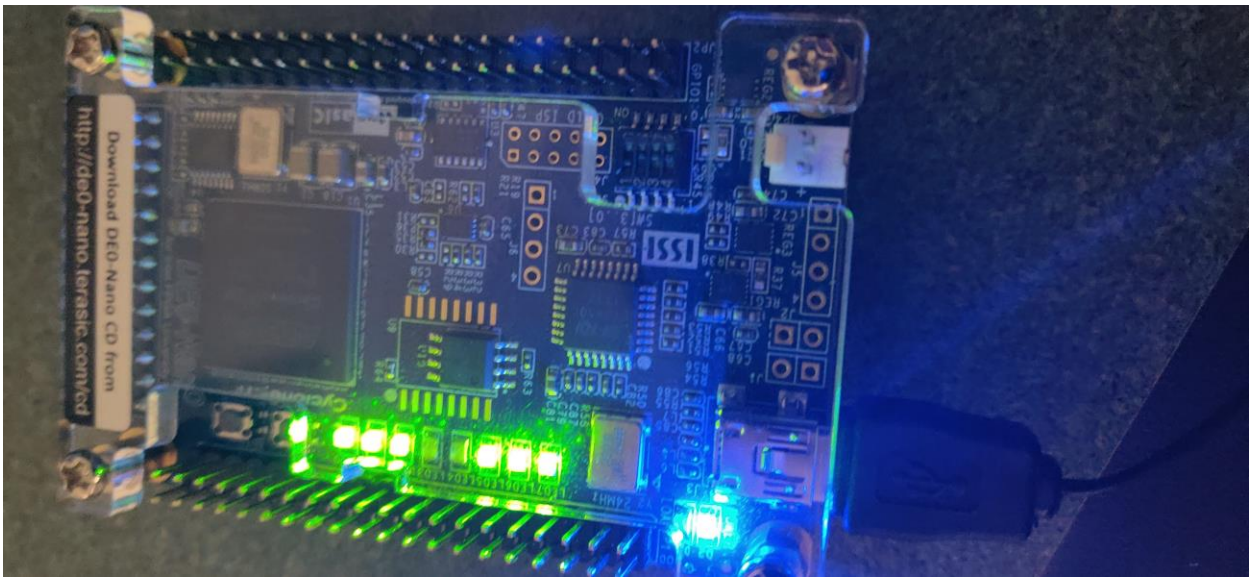
lab5part1.v | lab5part1_tb.v | lab5part2.v

```
module lab5part1_tb();
   reg X, reset, clk;
   wire [2:0] c, n;  //c : curret n: next state
   wire Y, W;

   lab5part1 uut(.X(X), .reset(reset), .clk(clk), .c(c), .n(n), .Y(Y), .W(W));

   initial begin
      clk = 1'b0;
      reset = 1'b0;
      X = 1'b0;

      #50;
      reset = 1'b1;
      X = 1'b0;

      #50;
      X = 1'b0;

      #50;
      X = 1'b1;

      #50;
      X = 1'b0;
      $stop;
   end

   always begin
      #25;
      clk = ~clk;
   end
endmodule
```



Switch 2	block	-	1	0	0
Switch 1	reset	-	0	1	1
Switch 0	X	-	0	0	1
Led 2	c[2]	-	1	1	0
Led 3	c[1]	-	0	0	0
Led 4	c[0]	-	0	0	0
Led 5	n[2]	-	0	0	0
Led 6	n[1]	-	0	0	0
Led 7	n[0]	-	0	0	1
Led 0	W(morse)	-	1	1	0
Led 1	Y(ready)	-	0	0	1

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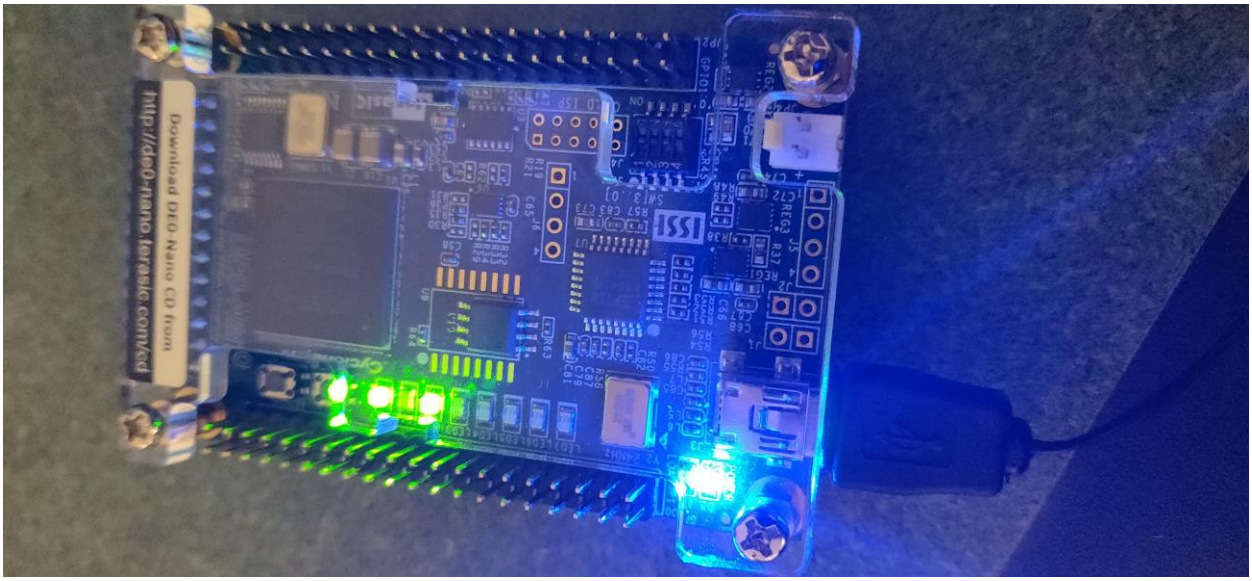
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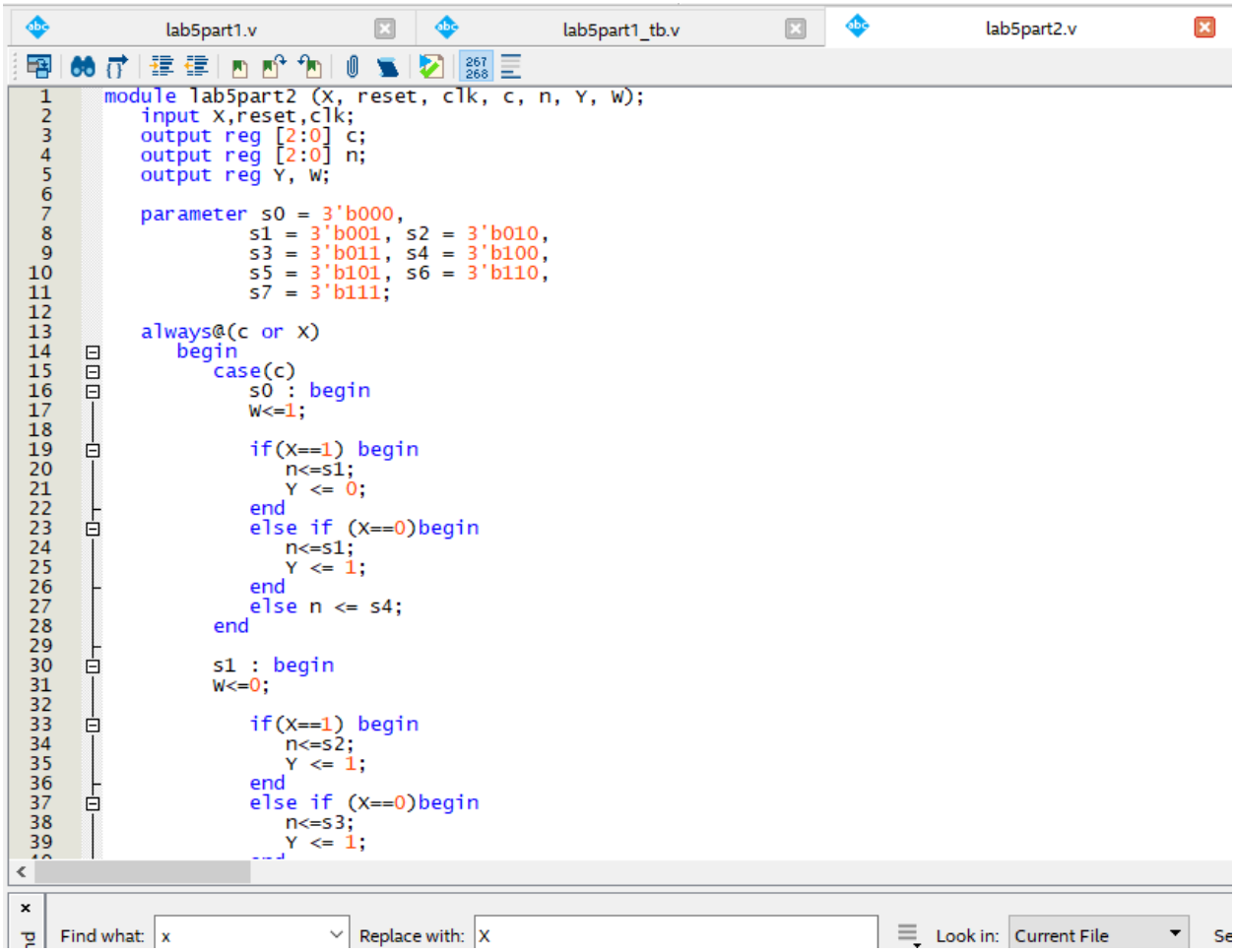
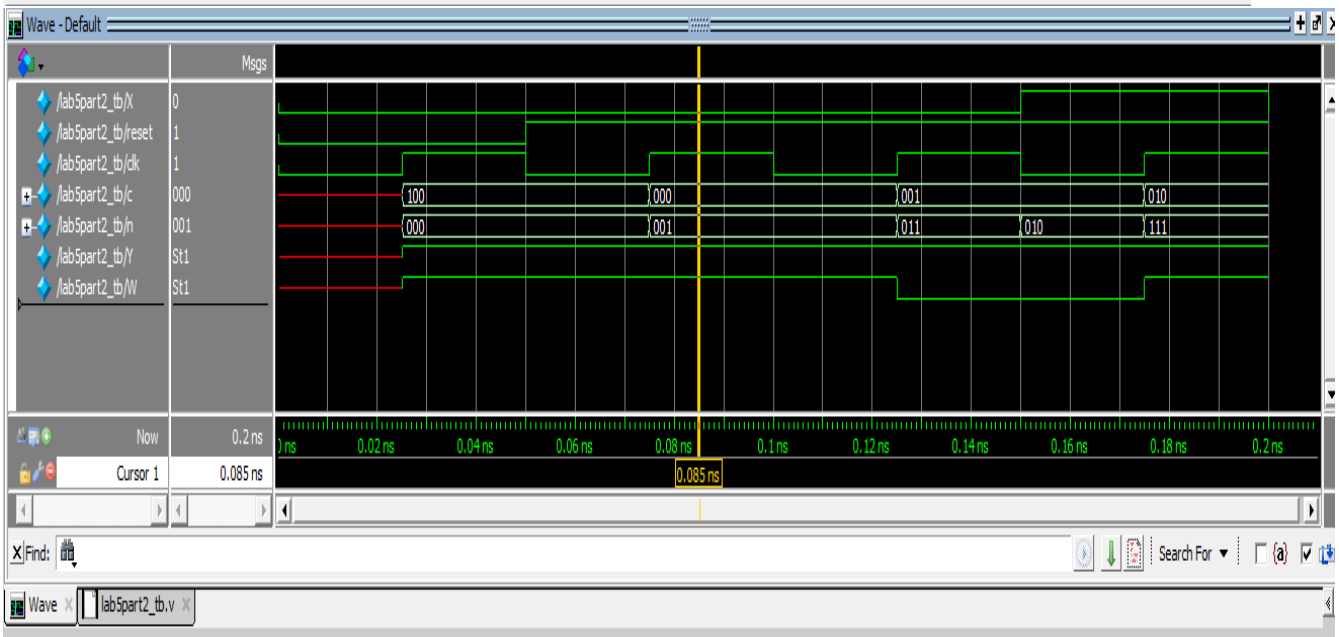
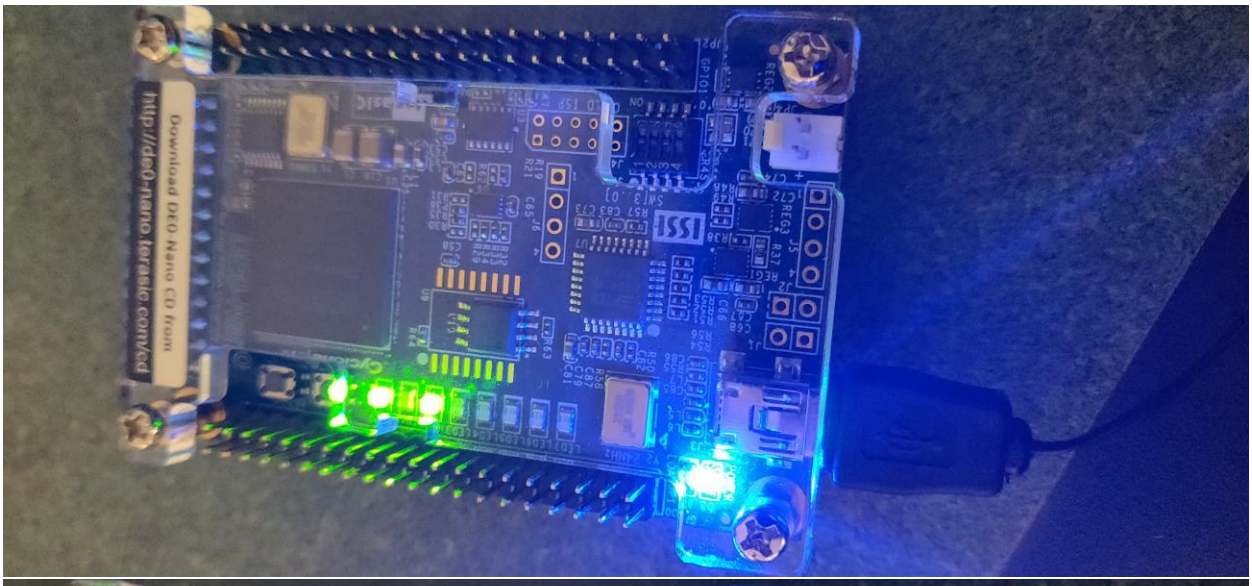
Part 2:


lab5part1.v
lab5part1_tb.v
lab5part2.v
module lab5part2 (X, reset, clk, c, n, Y, W);
input X,reset,clk;
output reg [2:0] c;
output reg [2:0] n;
output reg Y, W;
parameter s0 = 3'b000,
s1 = 3'b001, s2 = 3'b010,
s3 = 3'b011, s4 = 3'b100,
s5 = 3'b101, s6 = 3'b110,
s7 = 3'b111;
always@(c or X)
begin
case(c)
s0 : begin
W<=1;
if(X==1) begin
n<=s1;
Y <= 0;
end
else if (X==0)begin
n<=s1;
Y <= 1;
end
else n <= s4;
end
s1 : begin
W<=0;
if(X==1) begin
n<=s2;
Y <= 1;
end
else if (X==0)begin
n<=s3;
Y <= 1;
Find what: x
Replace with: X
Look in: Current File

lab5part1.v | lab5part1_tb.v | lab5part2.v

```
1  module lab5part2_tb();
2     reg X, reset, clk;
3     wire [2:0] c, n;
4     wire Y, W;  //Y is mealy    W is moorse
5
6     lab5part2 uut(.X(X), .reset(reset), .clk(clk), .c(c), .n(n), .Y(Y), .W(W));
7
8     initial begin
9        clk = 1'b0;
10       reset = 1'b0;
11       X = 1'b0;
12
13       #50;
14       reset = 1'b1;
15       X = 1'b0;
16
17       #50;
18       X = 1'b0;
19
20       #50;
21       X = 1'b1;
22
23       #50;
24       X = 1'b0;
25       $stop;
26    end
27
28    always begin
29       #25;
30       clk = ~clk;
31    end
32 endmodule
33
```

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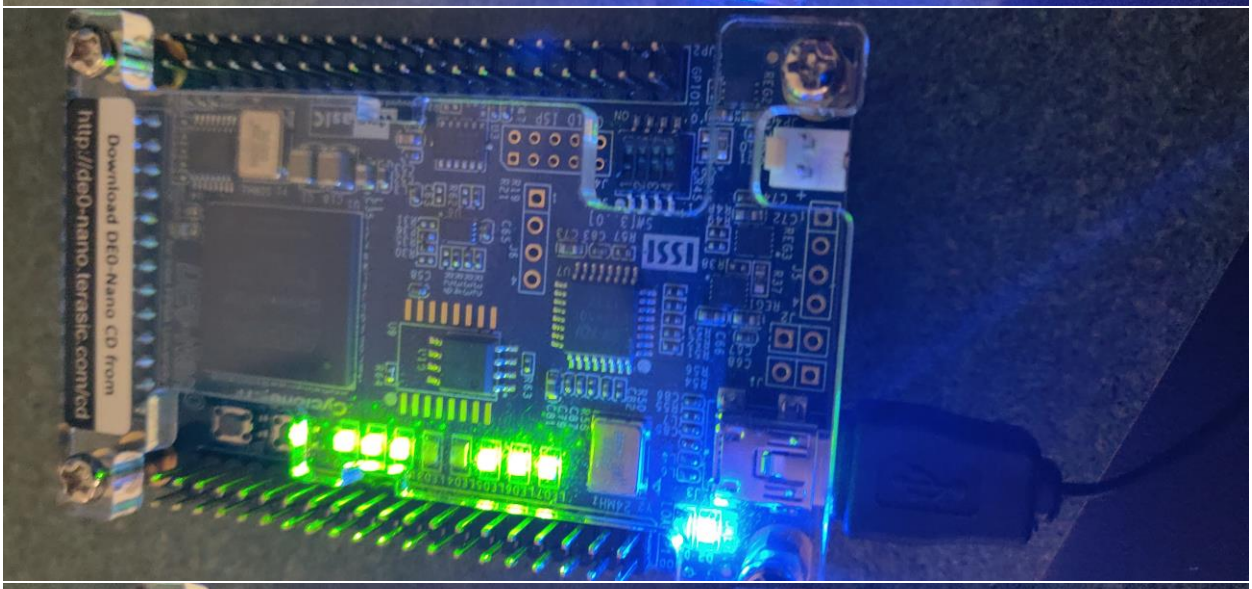
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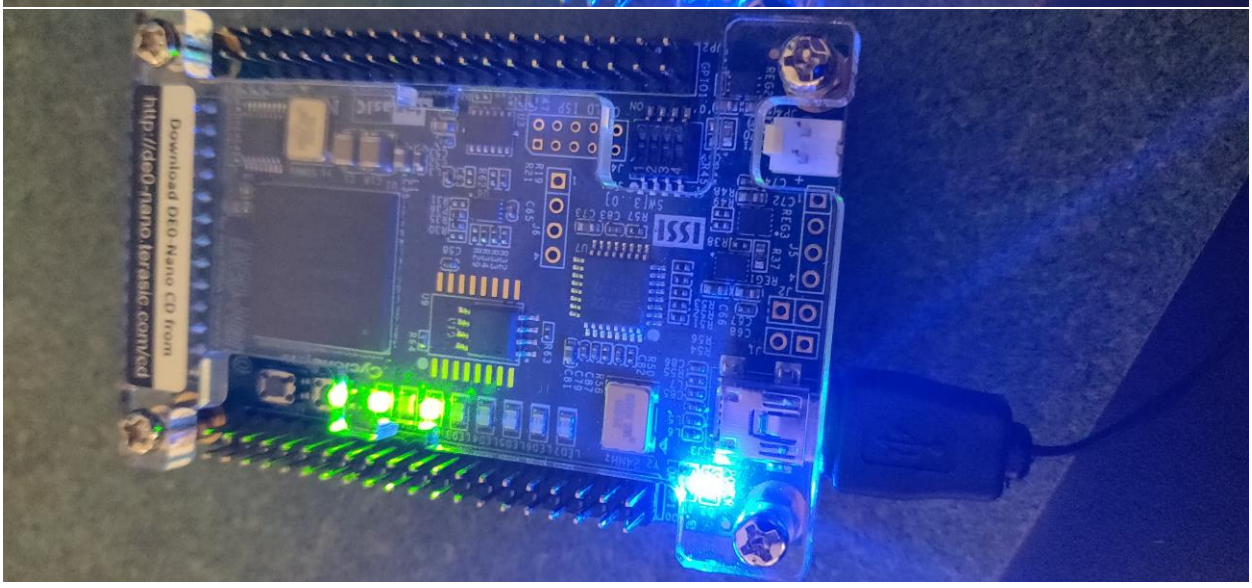
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