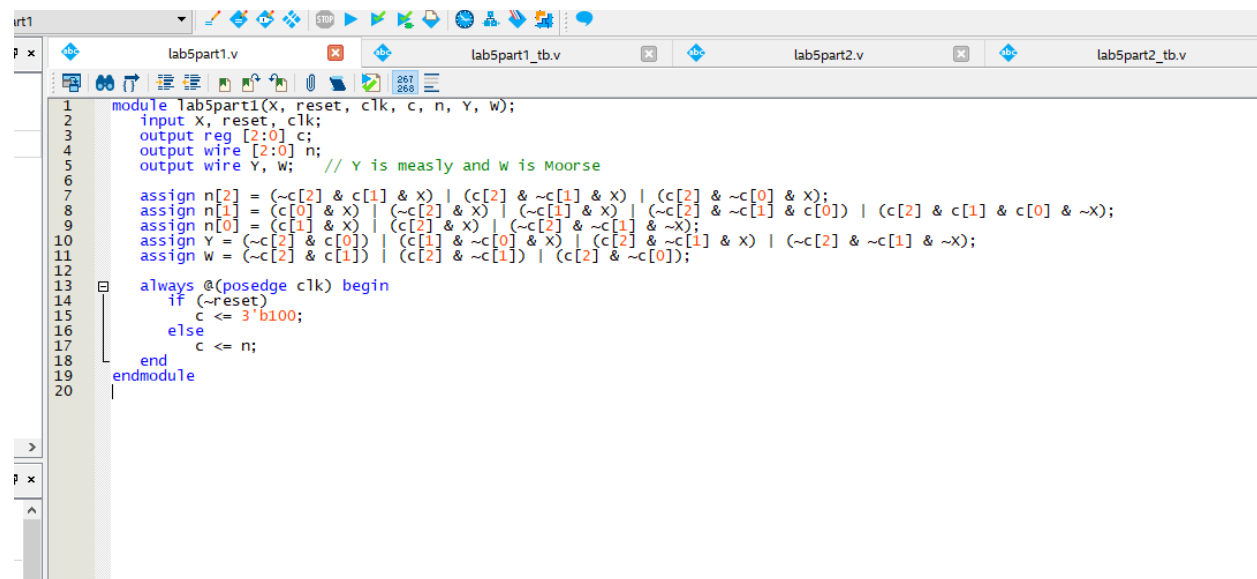


Shammah Thao

Cpe64

Part 1:



```
1 module lab5part1(X, reset, clk, c, n, Y, W);
2   input X, reset, clk;
3   output reg [2:0] c;
4   output wire [2:0] n;
5   output wire Y, W; // Y is measly and W is Moorese
6
7   assign n[2] = (~c[2] & c[1] & X) | (c[2] & ~c[1] & X) | (c[2] & ~c[0] & X);
8   assign n[1] = (c[0] & X) | (~c[2] & X) | (~c[1] & X) | (~c[2] & ~c[1] & c[0]) | (c[2] & c[1] & c[0] & ~X);
9   assign n[0] = (c[1] & X) | (c[2] & X) | (~c[2] & ~c[1] & ~X);
10  assign Y = (~c[2] & c[0]) | (c[1] & ~c[0] & X) | (c[2] & ~c[1] & X) | (~c[2] & ~c[1] & ~X);
11  assign W = (~c[2] & c[1]) | (c[2] & ~c[1]) | (c[2] & ~c[0]);
12
13  always @(posedge clk) begin
14    if (~reset)
15      c <= 3'b100;
16    else
17      c <= n;
18  end
19 endmodule
20
```

lab5part1.v
lab5part1_tb.v
lab5part2.v

```

module lab5part1_tb();
    reg x, reset, clk;
    wire [2:0] c, n; //c : curret n: next state
    wire Y, W;

    lab5part1 uut(.x(x), .reset(reset), .clk(clk), .c(c), .n(n), .Y(Y), .W(W));

    initial begin
        clk = 1'b0;
        reset = 1'b0;
        x = 1'b0;

        #50;
        reset = 1'b1;
        x = 1'b0;

        #50;
        x = 1'b0;

        #50;
        x = 1'b1;

        #50;
        x = 1'b0;
        $stop;
    end

    always begin
        #25;
        clk = ~clk;
    end
endmodule

```

Wave - Default

Signal	Value	Hex
/lab5part1_tb/x	0	
/lab5part1_tb/reset	0	
/lab5part1_tb/clk	1	
/lab5part1_tb/c	100	000
/lab5part1_tb/n	000	000
/lab5part1_tb/Y	S10	
/lab5part1_tb/W	S11	

Timing diagram showing signals x, reset, clk, c, n, Y, and W over time. A cursor is positioned at 0.031 ns.

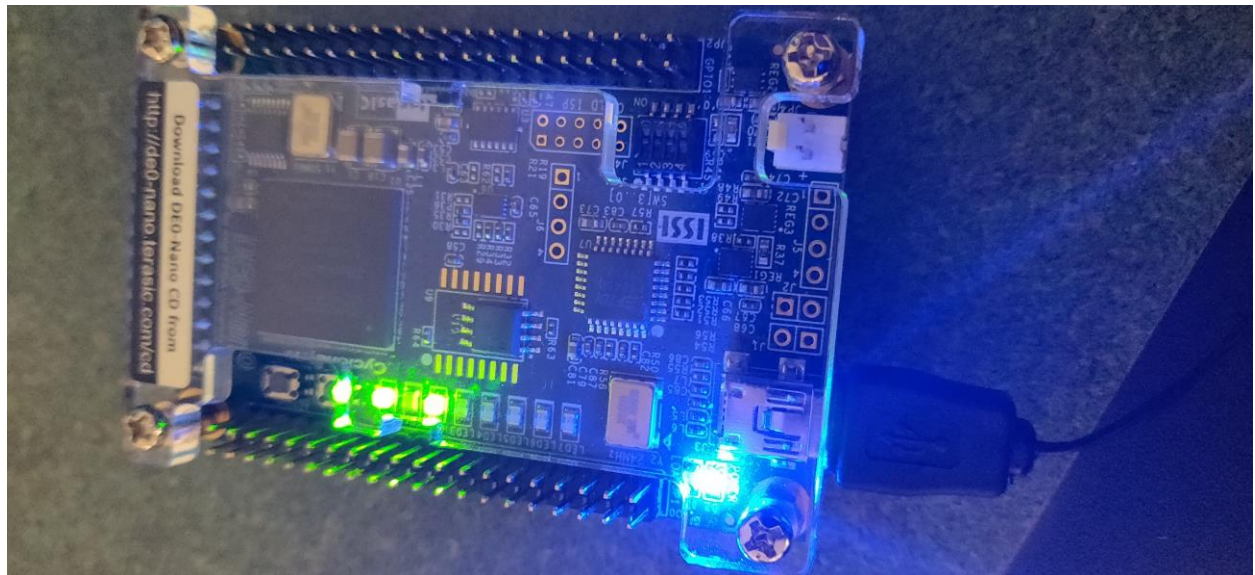
Now: 0.2 ns

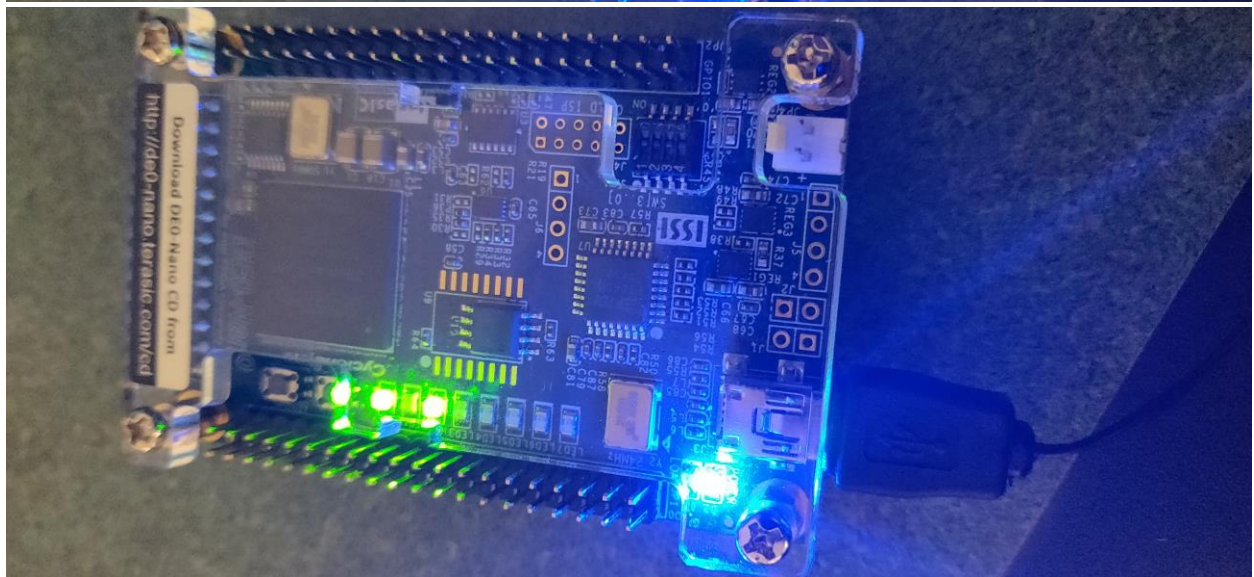
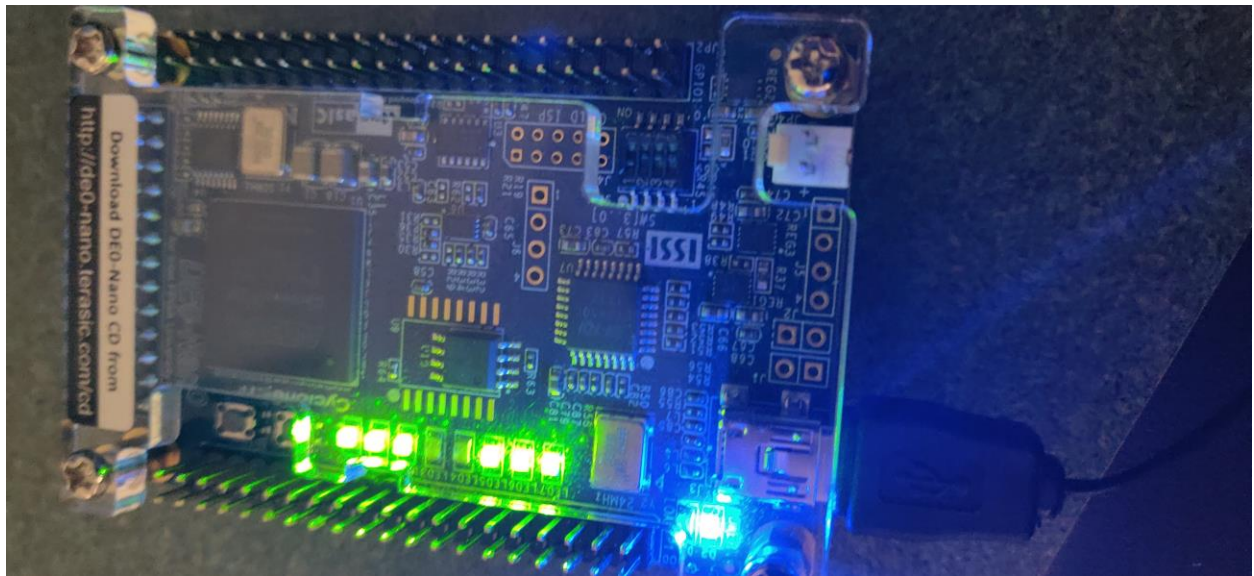
Cursor 1: 0.031 ns

Find:

Search For: (a) ✓

Switch 2	kl0cu	-	1	0	E1	0
Switch 1	reset	-	0	1		1
Switch 0	X	-	0	0	J15	1
Led 2	c[2]	-	1	1		0
Led 3	c[1]	-	0	0		0
Led 4	c[0]	-	0	0		0
Led 5	n[2]	-	0	0		0
Led 6	n[1]	-	0	0		0
Led 7	n[0]	-	0	0		1
Led 0	w(mooroc)	-	1	1		0
Led 1	Y(mealy)	-	0	0		1





Part 2:

lab5part1.vlab5part1_tb.vlab5part2.v

267268

```
1 module lab5part2 (x, reset, clk, c, n, Y, w);
2   input x,reset,clk;
3   output reg [2:0] c;
4   output reg [2:0] n;
5   output reg Y, w;
6
7   parameter s0 = 3'b000,
8             s1 = 3'b001, s2 = 3'b010,
9             s3 = 3'b011, s4 = 3'b100,
10            s5 = 3'b101, s6 = 3'b110,
11            s7 = 3'b111;
12
13   always@(c or x)
14   begin
15     case(c)
16     s0 : begin
17       w<=1;
18
19       if(x==1) begin
20         n<=s1;
21         Y <= 0;
22       end
23       else if (X==0)begin
24         n<=s1;
25         Y <= 1;
26       end
27       else n <= s4;
28     end
29
30     s1 : begin
31       w<=0;
32
33       if(x==1) begin
34         n<=s2;
35         Y <= 1;
36       end
37       else if (X==0)begin
38         n<=s3;
39         Y <= 1;
40       end
41     end
42   end
```

Find what: x

Replace with: X

Look in: Current File

Se

```

1 module lab5part2_tb();
2     reg x, reset, clk;
3     wire [2:0] c, n;
4     wire Y, w; //Y is mealy    w is moorse
5
6     lab5part2 uut(.x(x), .reset(reset), .clk(clk), .c(c), .n(n), .Y(Y), .w(w));
7
8     initial begin
9         clk = 1'b0;
10        reset = 1'b0;
11        x = 1'b0;
12
13        #50;
14        reset = 1'b1;
15        x = 1'b0;
16
17        #50;
18        x = 1'b0;
19
20        #50;
21        x = 1'b1;
22
23        #50;
24        x = 1'b0;
25        $stop;
26    end
27
28    always begin
29        #25;
30        clk = ~clk;
31    end
32 endmodule
33

```

