Lab 6: State Machine application

CpE Section 1

Instructor: Telles, Eric

Friday: 4:30 pm – 6:50pm

Thao, Shammah

Part 2: Display decoder 7-segment

Description:

For this lab, we are to display a 7-segment decoder using an fpga

Procedure:

Study the 7-segment display on the circuit board in lab. Are the signals to activate (turn on) individual segments on the circuit board active high or active low? If segments ‘a’ through ‘f’ are ON and ‘g’ is OFF, the number "0" will appear on the 7- segment display because the ‘g’ segment will NOT be turned ON. Do the Verilog code, compile and assign pins for the seven-segment display on breadboard or demo board. Download and test your design.

Engineering Data:

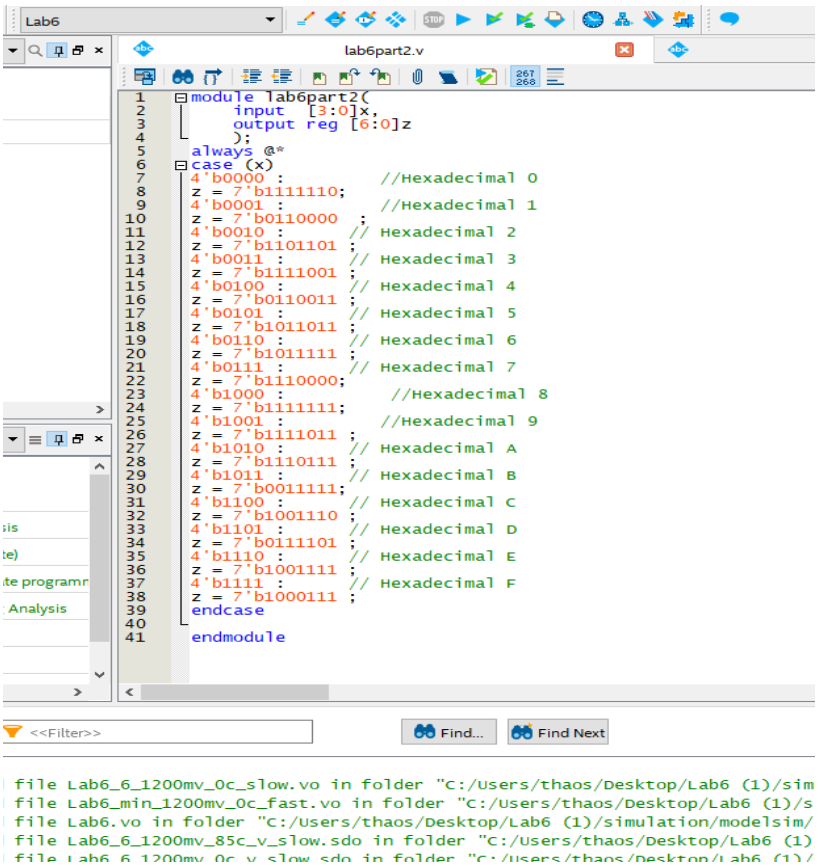

Figure 1:Verilog

For figure one, we used cased statement to set each bit as its own hexa decimal. This allows us to use the pin easily, since we are setting each z output as its own position making the correct led lit up. Using figure 2, we were able to design a testbench for all 16 hex.

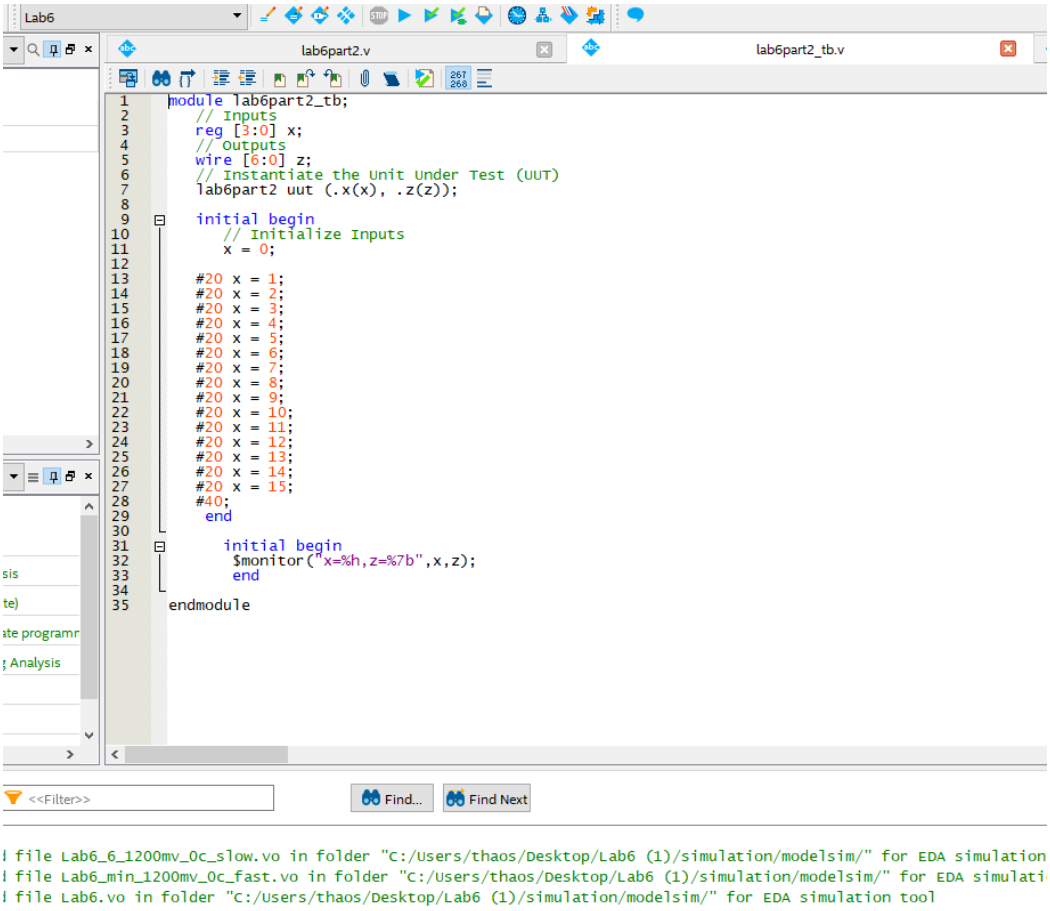

Figure 2:Testbench

VID_20190503_220024.mp4

Figure 3:video

For figure 3, it is the video of all the parts being display from 0 to F.

Conclusion:

In conclusion this lab was a good lab for the ending. Coming from multipart lab to doing only one part was a great relief. This lab put our knowledge of Verilog coding to the test and seeing if you can come up with code that will help you complete this lab.