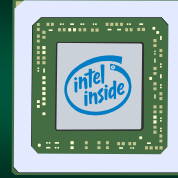




## Introduction to the Intel x64

Part 2

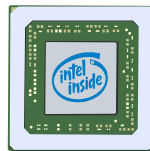


## The Intel x64

It was simple at first...

## The Intel x64

- The Intel x64 is the main processor used by servers, laptops, and desktops
- It has evolved continuously over a 40 year period
- The term "x86" refers to the 32-bit and 16



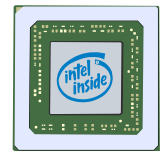
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## What to call the processor

- The classic term "x86" refers to the 32-bit and 16-bit processor family
- With move to 64-bit, the term "x64" is used to differentiate the newest design from the previous



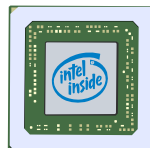
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## The Original x86

- First "x86" was the Intel 8086 released in 1978
- Attributes:
  - 16-bit processor (registers were 16-bit)
  - 16 registers
  - can access 1MB of RAM



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## Original x86 Registers

- The x86 processor has evolved continuously over the last 4 decades
- It jumped to 32-bit, and then, finally, to 64-bit
- The result is many of the registers have strange names

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## Original x86 Registers

It was simple at first...

## Original x86 Registers

- The original x86 contained 16 registers
- 8 can be used by your programs
- The other 8 are used for memory management



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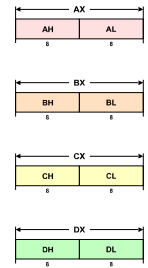
## Original x86 Registers

- 8 Registers can be used by your programs
  - Four General Purpose: **AX, BX, CX, DX**
  - Four pointer index: **SI, DI, BP, SP**
- The remaining 8 are restricted
  - Six segment: CS, DS, ES, FS, GS, SS
  - One instruction pointer: IP
  - One status register – used in computations

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## Original General Purpose Registers

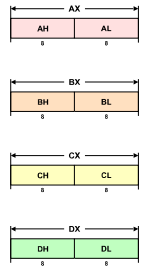
- However, back then (and now too) it is very useful to store 8-bit values
- So, Intel chopped 4 of the registers in half
- These registers have generic names of A, B, C, D



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## Original General Purpose Registers

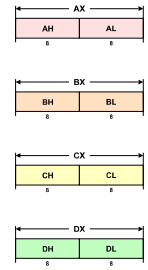
- The first and second byte can be used separately or used together
- Naming convention
  - high byte has the suffix "H"
  - low byte has the suffix "L"
  - for both bytes, the suffix is "X"



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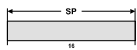
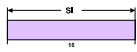
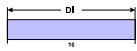
## Original General Purpose Registers

- This essentially doubled the number of registers
- So, there are:
  - four 16-bit registers or
  - eight 8-bit registers
  - (and any combination you can think off)



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## Last the 4 Registers



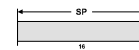
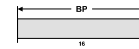
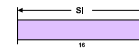
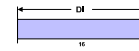
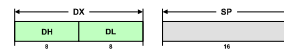
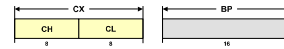
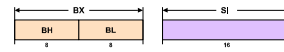
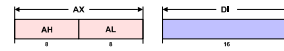
- The remaining 4 registers were not cut in half
- Used for storing indexes (for arrays) and pointers
- Their purpose
  - DI – destination index
  - SI – source index
  - BP – base pointer
  - SP – stack pointer

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## Original 16-Bit Registers



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## Evolution to 64 Bit Registers

This is going to hurt...

## Evolution to 32-bit

- When the x86 moved into the 32-bit era, Intel expanded the registers to 32-bit
  - the 16-bit ones still exist
  - they have the prefix "e" for extended
- New instructions were added (to use them)

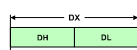
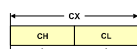
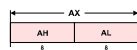


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## Original Registers

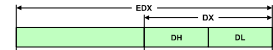
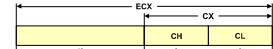
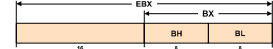
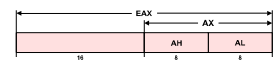


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## Expansion to 32-bit

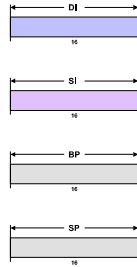


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## Original Registers

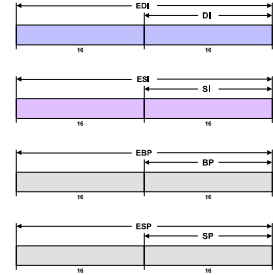


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## Expansion to 32-bit



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## Evolution to 64-bit

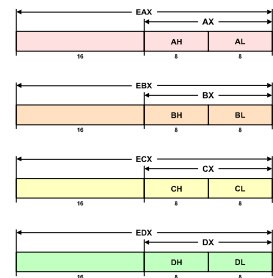
- The processor then evolved to 64-bit
- The registers were extended again
  - the 64-bit have the prefix "*r*" for *register*
  - 8 additional registers were added
  - also, it is now possible to get 8-bit values from all registers (hardware is more consistent!)

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## Expansion to 64-bit

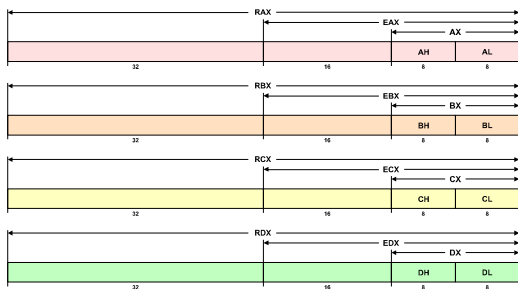


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## Expansion to 64-bit

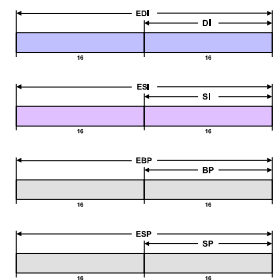


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## Expansion to 64-bit

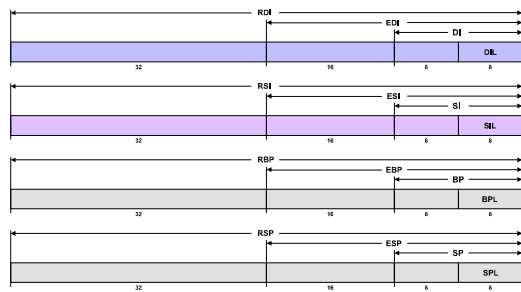


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## Expansion to 64-bit

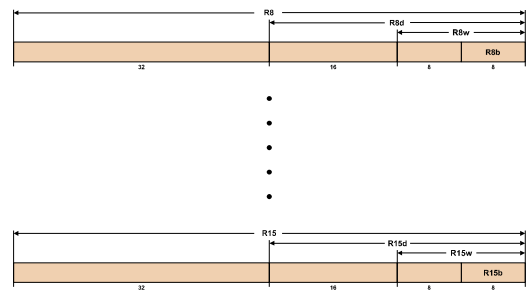


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## New 64-bit Registers: R8...R15



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## 64-Bit Register Table

Register	32-bit	16-bit	8-bit High	8-bit Low
<b>rax</b>	<b>eax</b>	<b>ax</b>	<b>ah</b>	<b>al</b>
<b>rbx</b>	<b>ebx</b>	<b>bx</b>	<b>bh</b>	<b>bl</b>
<b>rcx</b>	<b>ecx</b>	<b>cx</b>	<b>ch</b>	<b>cl</b>
<b>rdx</b>	<b>edx</b>	<b>dx</b>	<b>dh</b>	<b>dl</b>
<b>rsi</b>	<b>esi</b>	<b>si</b>		<b>sil</b>
<b>rdi</b>	<b>edi</b>	<b>di</b>		<b>dil</b>
<b>rbp</b>	<b>ebp</b>	<b>bp</b>		<b>bpl</b>
<b>rsp</b>	<b>esp</b>	<b>sp</b>		<b>spl</b>

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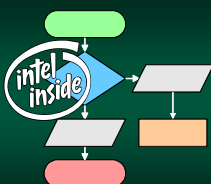
## 64-Bit Register Table

Register	32-bit	16-bit	8-bit High	8-bit Low
<b>r8</b>	<b>r8d</b>	<b>r8w</b>		<b>r8b</b>
<b>r9</b>	<b>r9d</b>	<b>r9w</b>		<b>r9b</b>
<b>r10</b>	<b>r10d</b>	<b>r10w</b>		<b>r10b</b>
<b>r11</b>	<b>r11d</b>	<b>r11w</b>		<b>r11b</b>
<b>r12</b>	<b>r12d</b>	<b>r12w</b>		<b>r12b</b>
<b>r13</b>	<b>r13d</b>	<b>r13w</b>		<b>r13b</b>
<b>r14</b>	<b>r14d</b>	<b>r14w</b>		<b>r14b</b>
<b>r15</b>	<b>r15d</b>	<b>r15w</b>		<b>r15b</b>

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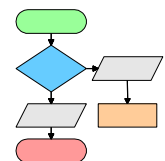


## Basic Intel x86 Instructions

Feel the pow-wah of the x86!

## Basic Intel x86 Instructions

- Each x86 instruction can have up to 2 operands
- Operands in x86 instructions are very versatile
- Often each argument can be either a memory address, register or an immediate value



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## Types of Operands

- Registers
- Memory address
- Register pointing to memory
- A constant stored with the instruction – this is called an *immediate*

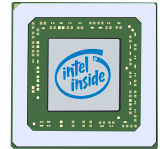
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## Intel x86 Instruction Limits

- There are some limitations...
- Some instructions must use an immediate
- Some instructions require a *specific* register to perform calculations



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## Intel x86 Instruction Limits

- A register must *always* be involved
  - processors use registers for all activity
  - both operands cannot access memory at the same time
  - *the processor has to have it at some point!*
- Also, obviously, the receiving field cannot be an immediate value

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## Instruction: Move

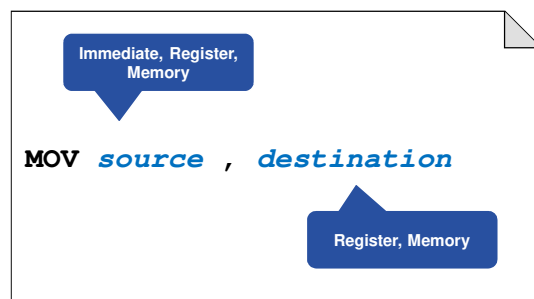
- The x86 Move Instruction combines load, store, and register transfer logic
- It is one of the most common instructions used in programs (true of all processors)
- Remember how often you use the assignment statement in C / Java?

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## Instruction: Move

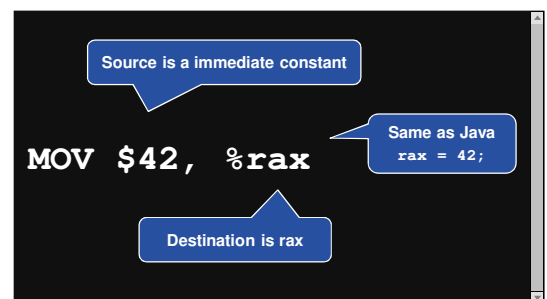


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## Example: Move immediate



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## Example: "A" Register

# So many options!

```
mov $42, %al    #low byte
mov $13, %ah    #high byte
mov $47, %ax    #both bytes
```

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## Example: Move register to register

MOV %rax, %rbx

Source is rax

Same as Java  
rbx = rax;

Destination is rbx

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## Example: Move register to memory

MOV %rax, counter

Source is rax

Memory location  
named 'Counter'

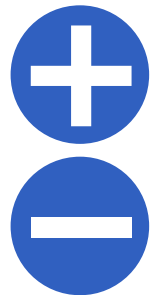
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## Instruction: Add & Subtract

- The Add and Subtract instructions take two operands and store the result in the second operand
- This is the same as the += and -= operators used in Visual Basic .NET, C, C++, Java, etc...



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## Instruction: Add

ADD value, target

Immediate, Register,  
Memory

Register, Memory

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## Example: Move register to memory

MOV counter, %rax  
ADD \$2, %rax

Move memory into rax

Same as Java  
rax += 2;

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## Instruction: And & Or

- The Logical And and Logical Or instructions take two operands and stores the result in the second operand
- This is the same as the  $\wedge$  and  $\vee$  operators used in C, C++, Java, etc...



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## Instruction: Logical And

**AND** *value* , *target*

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## Example: Logical Or

```
#Convert 5 to ASCII '5'
MOV $5, %rax
OR $0x30, %rax
```

0011 0000

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## Instruction: Call

- The Call Instruction transfers control to a memory location (a subroutine)
- Subroutines are analogous to the functions you wrote in Java
- Once it completes, execution continues after the call

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## Instruction: Call

**CALL** *address*

Usually a label – a constant that holds an address

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## Example: Print an integer

```
#This is using the CSC35 library
```

```
MOV $42, %rcx
CALL PrintInt
```

This name is an address

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