CFS2300: General Sensor Conditioner with Digital Temperature Calibration

DatasheetV1.9

Product Overview

The CFS2300 is a highly integrated, low power high precision sensor conditioner for general resistive bridge sensors, which features a low noise instrument amplifier, a low power 24 bit Σ-Δ ADC, a digital sensor calibration DSP and a 12-bit DAC. The CFS2300 can provide an on-chip digital compeCFStion of sensor offset, gain, temperature drift and non-linearity based on the internal fuse banks (OTP), which is fast, precise, without the cost overhead with trimming by laser or external components. Multiple temperature sensing methods are supported by CFS2300 for sensor's temperature calibrating. Once calibrated, the pin VOUT can provide a selectable fixed level or ratio-metric analog output, and I2C, SPI and one wire (OWI) interfaces are supported for chip configuration, sensor calibrating and digital output.

Key Features

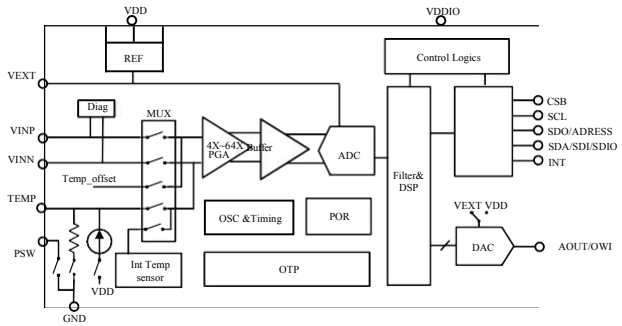
- Support both digital and analog output modes.
- Input referred RMS noise: 600nV @ OSR=1024X, GAIN=32X
- OTP based digital calibration of sensor offset, sensitivity, temperature drift and non-linearity with a calibration precision up to 0.05% full scale.
- 1X~128X programmable gain for sensors with different input spans up to rail-to-rail.
- Full set of diagnostic features
- Low power instrument amplifier and 24-bit Σ-Δ ADC
- Multiple temperature sensing methods
- 8-level resolution settings for conversion time and accuracy trade off
- SPI / I2C serial interface
- One Wire Interface (OWI) Supported
- Ultra low power-down current (< 0.2uA@25℃)
- Supply voltage 1.8V to 5.5V
- Operation temperature from -40℃ to 125℃

Available Supports

- Evaluation kit with calibration procedure for fast user design
- Support for mass calibration
- Quick circuit customization possible

Applications

- Pressure sensor conditioner
- Magnetic sensor conditioner
- Strain Gauge interface
- Industry process control



1.0 ABSOLUTE MAXIMUM RATING

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	**Comments**
Supply Voltage	VDD	-0.3		6.5	V	
	VDDIO	-0.3		6.5	V	
Analog pin voltage		-0.3		VDD+0.3	V	
Analog output current				40mA		
Digital output voltage		-0;3		VDDIO+0.3	V	25°C
ESD Susceptibility			4		kV	HBM
Storage temperature		-60		150	**°C**	

2.0 ELECTRICAL CHARACTERISITICS

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Comments**
Supply/Regulation						
Supply Voltage	VDD	1.8		5.5	V	
	VDDIO	1.2V		5.5	V	
Operation temp	T_A	-40		125	°C	
Supply Current@25°C on during conversion	I_{DD_pgaoff}		900		uA	PGA off (Gain<=2), DAC off
	I_{DD_pgaon}		1500		uA	PGA on (Gain>=4), DAC off
	Idd_dac		1700		uA	PGA on and DAC on
Standby current	I_{sd}		100		nA	25°C
Regulator output		1.62	1.8	1.98	V	'regulator_sel' = 0
		3.24	3.6	3.96	V	'regulaor_sel' = 1
Regulator PSRR			60		dB	
Current load on Regulator	I_{load}			5mA		
Signal Chain (MUX+PGA+BUFFER+ADC) CHARACTERISTICS						
Resolution	*N*		*24*		*Bits*	
Conversation time	Tcnv	Depend on OSR setting, refer to Table 4.1			Ms	
Output Data Resolution		24			Bit	LSB = (1/2^23)*(VEXT-PSW) ('raw_data_on'=1)
Effective Resolution	ENOB	refer to Table 4.1			Bits	Depends on Gain & OSR
Gain setting	GAIN	1		128		

Integral Nonlinearity	INL			15	ppm of FS	
Input Common Mode Rejection	CMRR	80	110		dB	
Power Supply Rejection	PSRR	90	110		dB	
TEMPERATURE SENSOR						
Output Data Resolution		16			Bit	LSB = (1/256) ℃
Abs Accuracy of built-in temp sensor (temp_sel = 11b)				±0.5	℃	@25℃
				±1	℃	-40 to 85 ℃
Internal Resistance for temperature sensor (temp_sel = 01b)	$R_{T\text{-}RES}$	4.5	5	5.5	Kohm	
Internal offset voltage for temp sensor (temp_sel = 00/01/11b)	$V_{T\text{-}OFF}$	0		1	VEXT	Configured by 'T_ref_trim'
ANALOG PINS						
Absolute Voltage of Input Pins	VINP, VINN	GND+0.1		VDD -0.1	V	PGA off
		GND+0.4		VDD -0.8	V	PGA on
Differential Input Ranges (V_{offset}+V_{sp})	V_{range}		+- 1/GAIN		V/V	
Input Pin Leakage	Iin			+-1	nA	PGA off
Low-side Power Switch Resistance	Rsw			8	Ohm	
DAC						
Resolution			12		Bit	
DNL				0.5	LSB	
INL				1	LSB	
Rload of DAC buffer	Rload	1k			Ohm	
Cload of DAC	Cload			15	nF	
Short Current Limit		15	20	25	mA	
Upper output limit		3/4		1	VDD	
Lower output limit		0		1/4	VDD	
SERIAL INTERFACE						
Serial Clock Frequency	Fsclk			10	MHz	SPI Interface
				400	KHz	I2C Interface

3.0 REGISTERS

All the CFS2300 registers can be departed into normal registers and OTP registers. The normal registers are used to send a conversion command to the CFS2300, read back the conversion data and perform the OTP blowing. The OTP registers are used to store the configurations and calibration coefficients for the CFS2300, whose default values can be programmed by the inside OTP banks.

3.1. NORMAL REGISTERS

Table3.1 normal registers

Addr	Description	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	SPI _Ctrl	RW	SDO_active	LSB_first	Softreset			Softreset	LSB_first	SDO_active	0x00
0x01	Part_ID	R	PartID<7:0>								0x00
0x02	Status	R	Error_code<3:0>						1'b0	DRDY	
0x06	DATA_MSB	R	Data out<23:16>								0x00
0x07	DATA_CSB	R	Data out<15:8>								0x00
0x08	DATA_LSB	R	Data out<7:0>								0x00
0x09	TEMP_MSB	R	Temp out<15:8>								0x00
0x0A	TEMP_LSB	R	Temp out<7:0>								0x00
0x30	CMD	RW	Sleep_time<3:0>				Sco	Measurement_ctrl<2:0>			0x00
0x6C	OTP_CMD	RW	Blow start<6:0>							margin	0x00

Reg0x00

SDO_active: 1: 4-wire SPI, 0: 3-wire SPI

LSB_first: 1: LSB first for SPI interface, 0: MSB first for SPI interface

Soft_reset: 1: Reset all the CFS2300 registers (except 'margin'), automatically come back to 0 after reset complete.

Reg0x01

PartID: OTP programmed 8 bits Part ID, corresponding to OTP register Reg0xA4. Read only from the address 0x01.

Reg0x02

DRDY： 1, indicates once conversion complete, and the output data is ready for reading.

Error_code: When diagnostic function enabled, These bits stores the error information.

Error_code[3]: VINP short to VDD

Error_code[2]: VINP short to GND

Error_code[1]: VINN short to VDD

Error_code[0]: VINN short to GND

Reg0x06-Reg0x08

Data_out: 24 bits ADC output data when 'raw_data_on' = 0 with an LSB equals to (1/2^23)*(VEXT-PSW). 24 bits calibrated data when 'raw_data_on' = 1.

Reg0x09-Reg0x0a

Temp_out: Temperature output with an LSB equals to (1/256) °C

Reg0x30

Sleep_time<3:0>: 0000:0ms, 0001:62.5ms, 0010:125ms ... 1111: 1s, only active during sleep mode conversion.

Measurement_control<1:0>: 000b, indicate a single shot temperature signal conversion. 001b, indicate a single shot sensor signal conversion. 010b: indicate a combined conversion (once temperature conversion immediately followed by once sensor signal conversion). 011b: indicate a sleep mode conversion (periodically perform once combined conversion with an interval time of 'sleep_time'), 100b: OTP programming mode, enter this mode to when programming OTP banks.

Sco: 1, Start of conversion, automatically come back to 0 after conversion ends (except sleep mode conversion).

Reg0x6C

Blow_start<6:0>: Write these bits into 0110101b to start the OTP blowing. The whole OTP banks would be automatically programmed as what stored in the corresponding OTP registers. The OTP banks can only be programmed once.

Margin: Provides a critical read condition to filter out "weak programmed" bits when OTP reloading during soft reset. It is recommended to set this bit after OTP programmed in factory to check if the OTP banks are reliably programmed.

3.2. OTP REGISTERS

Table3.2 OTP registers

Addr	Description	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0xA4	PartID	RW	PartID<7:0>								OTP
0xA5	Sys_config	RW	DAC_on	P_T_ration <1:0>		Vout_sel	Regulator_sel	Unipolar	Raw_data_on	DIAG_on	OTP
0xA6	P_config	RW	1'b0	Input_swap	Gain_P<2:0>			OSR_P<2:0>			OTP
0xA7	T_config_1	RW	Temp_sel<1:0>		Gain_T<2:0>			OSR_T<2:0>			OTP
0xA8	T_config_2	RW	4'b0000				T_offset_trim<3:0>				OTP
0xA9	DAC_limit	RW	DAC_limit_h<3:0>				DAC_limit_l<3:0>				OTP
0xAA	Cal_OTP_1	RW	Cal_coff_1<7:0>								OTP
…	…	RW	…								OTP
0xBB	Cal_OTP_18	RW	Cal_coff_19<7:0>								OTP
0xBC	Redundancy	RW	Redundancy<7:0>								OTP

Reg0xA4

PartID: OTP programmed 8 bits Part ID, also can be read from address 0x01.

Reg0xA5

DAC_on: 1, enable analog output. When analog output enabled, CFS2300 continuously performs once temperature conversion after 64/32/16/1 (configured by 'P_T_ratio') times sensor signal conversions, no matter what 'CMD' (reg0x30) register settings.

P_T_ratio: set how many sensor signal conversions performed after once temperature conversion during analog output mode. 00: 64 times, 01: 32 times, 10: 16 times, 11: once.

Vout_sel: 0: set the DAC output voltage to be rail to rail, that is goes with the voltage on VDD pin, 1: set the DAC output fixed at a voltage range of 0-1.5*VEXT.

Regulator_sel: 0: set the VEXT voltage to be 1.8V, 1: set the VEXT voltage to be 3.6V.

Unipolar: 0: ADC output in bipolar format, 1: ADC output in unipolar format. (Only take effect when 'raw_data_on' = 1)

Raw_data_on: 0: output calibrated data, 1: output ADC raw data. (Only take effect in single shot sensor signal conversion and single shot temperature conversion)

Diag_on: 1, Enable diagnosis function.

Reg0xA6

Input Swap: Swap VINP and VINN inside the CFS2300

Gain_P: set the gain of the sensor signal conversion channel. 000: gain=1, 001: gain=2, 010: gain=4, 011: gain=8, 100: gain=16, 101: gain=32, 110: gain=64, 111: gain=128.

OSR_P: set the over sampling ratio of the sensor signal conversion channel. 000:1024X, 001:2048X, 010:4096X, 011:8192X, 100:256X, 101:512X, 110:16384X, 111:32768X.

Reg0xA7

Temp_sel: select different temperature sensing methods. 00: external temp sensor with a resistance connected between TEMP and GND inside chip, 01: external temperature sensor with a current source output via TEMP pin, 10: external temperature sensor, 11: internal temperature sensor.

Gain_T: set the gain of the temperature conversion channel. 000: gain=1, 001: gain=2, 010: gain=4, 011: gain=8, 100: gain=16, 101: gain=32, 110: gain=64, 111: gain=128.

OSR_T: set the over sampling ratio of the temperature conversion channel. 000:1024X, 001:2048X, 010:4096X, 011:8192X, 100:256X, 101:512X, 110:16384X, 111:32768X.

Reg0xA8

T_offset_trim: set the offset voltage for external temperature conversion from 0V to VEXT.

Reg0xA9

DAC_limit_h: set an upper clipping limit for the analog output from 3/4Vfs (0000b) to Vfs(1111b)

DAC_limit_l: set a lower clipping limit for the analog output from 0(0000b) to 1/4Vfs(1111b)

Reg0xAA-Reg0xBB

Cal_coff: Coefficients used for sensor calibrating.

Reg0xBC

Redundancy: A pointer, make the OTP bit it pointed functioning as programmed even if it is programming failed. This is a method to improve the yield of OTP blowing.

4.0 FUNCTIONAL DESCRIPTIONS

The CFS2300 is a highly integrated 24-bit sensor conditioner for applications of high precision low frequency measurement such as pressure transducer, weight scale. It can provide fully calibration for the sensor inherent temperature drift and non-linearity with multiple temperature sensing methods supported. The chip incorporates an in-amp, a buffer and a 24-bit sigma delta modulator followed by a calibration DSP and a 12-bit DAC for the analog output. With wide gain and OSR range, the CFS2300 could be suitable for variance sensors. One-time-programmable fuses are used to store the calibration coefficients for on-chip calibration calculations. SPI, I2C and OWI interfaces are supported for serial communication.

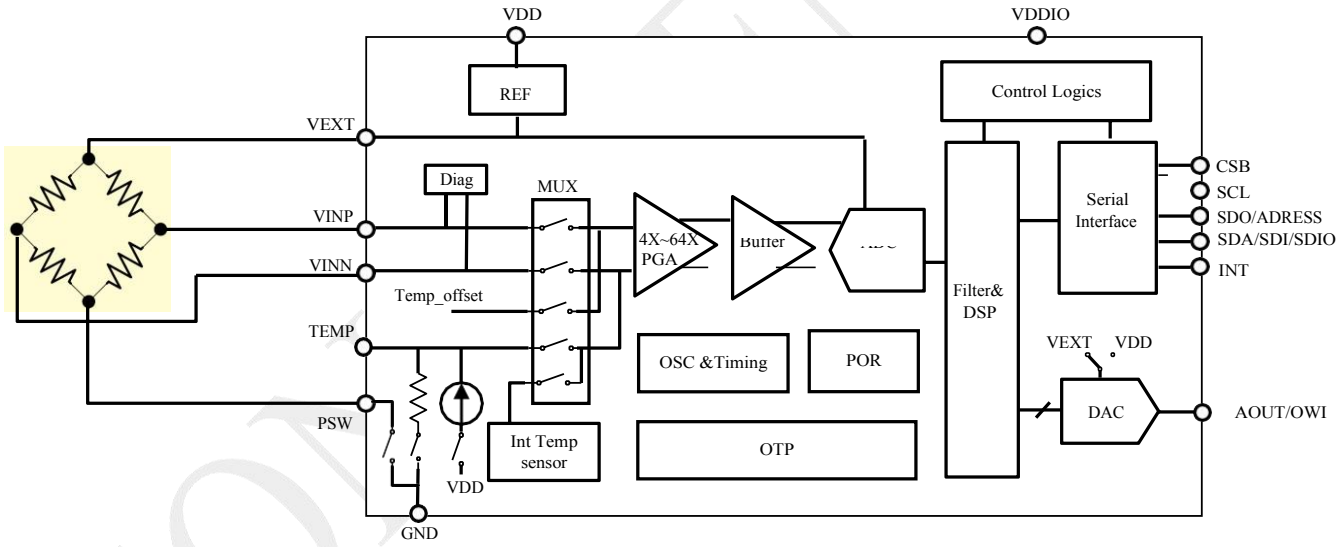


Figure4.1 Basic Application Diagram

4.1. SIGNAL PATH

4.1.1. Analog Inputs and Reference

The reference voltage VREF is defined as the voltage difference between VEXT pin and PSW pin. VEXT pin is powered by the internal 1.8V/3.6V regulator for higher PSRR on a noisy system. The user could also bias this pin externally at a higher voltage, for example, short to VDD, to increase the dynamic range.

A low side switch on the PSW pin connected the low-side of the sensor. Sensor current could be automatically turned off when not in measurement mode.

TEMP pin is used for the external temperature sensor input. With an optional low drift 5Kohm pulled down resistance and an optional low drift excitation current source connected, TEMP pin can support multiple external temperature sensing methods.

4.1.2. PGA, Buffer and Modulator

The total gain of the analog path can be separately set for sensor signal channel and temperature channel as 1X, 4X, 8X, 16X, 32X and 64X by bits 'Gain_P' and 'Gain_T'. The allowed input range is +-VREF/GAIN where VREF is the voltage difference between VEXT and PSW.

4.1.3. Digital Filter with Programmable Over-Sampling Factor

The CFS2300 has a digital decimation filter followed the modulator. The output data rate could be separately programmable for sensor signal channel and temperature channel from 256X to 32768X by setting bits 'OSR_P' and 'OSR_T'.Table4.1 shows the effective number of bit (ENOB) and Conversion time (Tss) under different gain, OSR settings. Table4.2 shows the input referred RMS noise.

Table 4.1 ENOB (bits) under different ODR and Gain settings (VEXT=1.8V)

OSR_P	Tss(ms)	ADC ENOB							
		gain=1	gain=2	gain=4	gain=8	gain=16	gain=32	gain=64	gain=128
256X	1.54	17.7	17.6	17.1	17	17.1	16.8	16.4	16
512X	1.86	18	18	17.4	17.3	17.3	17.1	16.8	16.1
1024X	2.5	18.4	18.3	17.8	17.8	17.7	17.5	17	16.3
2048X	3.78	18.9	18.8	18.2	18.2	18.2	17.9	17.4	16.5
4096X	6.34	19.2	19.2	18.6	18.7	18.5	18.3	17.9	17.2
8192X	11.46	19.8	19.8	19	19.1	19.1	18.8	18.4	17.5
16384X	21.7	20.3	20.2	19.5	19.4	19.5	19.3	19	18.1
32768X	42.18	20.8	20.7	20.1	19.7	20.1	19.7	19.4	18.5

Table 4.2 Input Referred RMS noise (nV) under different ODR and Gain settings (VEXT=1.8V)

OSR_P	Tss(ms)	Input RMS noise(nV)							
		gain=1	gain=2	gain=4	gain=8	gain=16	gain=32	gain=64	gain=128
256X	1.54	16907.2	9060.3	6406.6	3433.2	1601.7	985.9	650.5	429.2
512X	1.86	13732.9	6866.5	5203.8	2788.6	1394.3	800.8	493.0	400.4
1024X	2.5	10407.6	5577.3	3943.7	1971.9	1056.7	606.9	429.2	348.6
2048X	3.78	7359.3	3943.7	2988.8	1494.4	747.2	460.0	325.2	303.5
4096X	6.34	5977.6	2988.8	2265.1	1056.7	606.9	348.6	230.0	186.8
8192X	11.46	3943.7	1971.9	1716.6	800.8	400.4	246.5	162.6	151.7
16384X	21.7	2788.6	1494.4	1213.8	650.5	303.5	174.3	107.3	100.1
32768X	42.18	1971.9	1056.7	800.8	528.3	200.2	132.1	81.3	75.9

4.1.4. Work Mode

4.1.4.1. Single-shot Sensor Signal Conversion

Setting 'measurement_control' = 01 and 'sco' = 1 to initiate once single-shot sensor signal conversion, the chip powers up, performs once sensor signal conversion, and returns back to standby mode with automatically changing 'sco' to 0. INT goes high when data is ready and returns low after the data value (0x06-0x08) has been read out from the 'data_out' registers. The 'data_out' registers can be read several times if required, even when the INT pin is low, but care must be taken not to read data when the 'data_out' registers are just in refreshing.

The gain of the sensor signal conversion channel can be configured by the bits 'Gain_P' from 1X to 64X and the OSR for the sensor conversion is configured by the 'OSR_P' bits from 256X to 32768X, the tradeoff of the conversion time and the output RMS noise under different OSR settings is shown in table 4.1/4.2.

A following calibration DSP is optional during the single-shot sensor signal conversion. When the DSP is enabled ('raw_data_on'=0), a 24-bit calibrated sensor data will be stored in the 'data_out' registers after conversion ends,

and else, the raw 24-bit ADC output is stored there. The relationship between the raw ADC data and the input signals for the sensor signal conversion is shown below:

$$CNT_{ADC\_raw\_P} = (\frac{VINP - VINN}{VREF}) * 2^{23} * Gain\_P \quad (\text{'unipolar'} = 0)$$

$$CNT_{ADC\_raw\_P} = (\frac{VINP - VINN}{VREF}) * 2^{23} * Gain\_P + 2^{23} \quad (\text{'unipolar'} = 1)$$

4.1.4.2. Single-shot Temperature Conversion

Different temperature sensing methods are supported by the CFS2300, either internally or externally. The 'temp_sel' bits support four configures for the temperature measurement. Set 'temp_sel' = 11 to choose the internal temperature sensor.

For the external temperature sensing methods, the pin 'TEMP' is used as the temperature signal input and the other end of the differential temperature signal pair is generated inside and can be configured by 'T_offset_trim' bits from 0 to VEXT with an minimum step of 1/15VEXT (Table 4.3).

Table 4.3 Temp offset voltage under different 'T_offset_trim' settings

T_offset_trim	T_offset_voltage
0000	0/15 VEXT
0001	1/15 VEXT
0010	2/15VEXT
0011	3/15 VEXT
0100	4/15 VEXT
0101	5/15 VEXT
0110	6/15 VEXT
0111	7/15VEXT
1000	8/15 VEXT
1001	9/15 VEXT
1010	10/15 VEXT
1011	11/15 VEXT
1100	12/15 VEXT
1101	13/15 VEXT
1110	14/15 VEXT
1111	VEXT

During external temperature sensing, a low temperature drift 5Kohm pulled down resistance or a low temperature drift excitation current source can be optional connected to the 'TEMP' pin to support multiple temperature sensing methods. Typical applications for these temperature measurement methods are shown below. Rt could be either the sensor bridge itself or a extra temperature sensing element close to the senor.

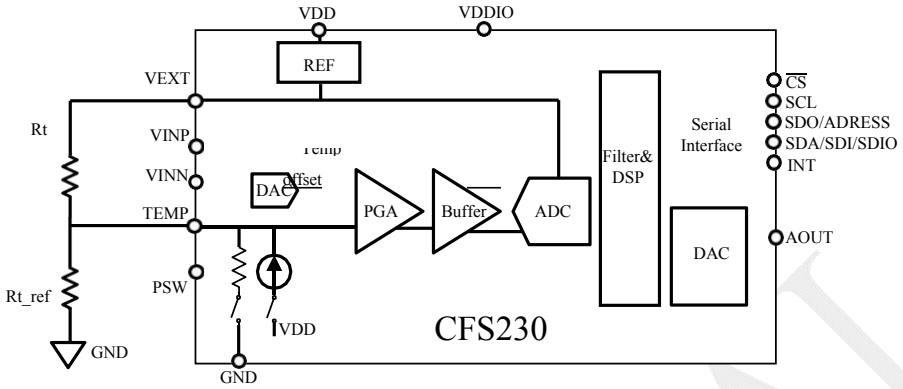


Figure4.2 External Temperature sensing ('temp_sel'== 10b)

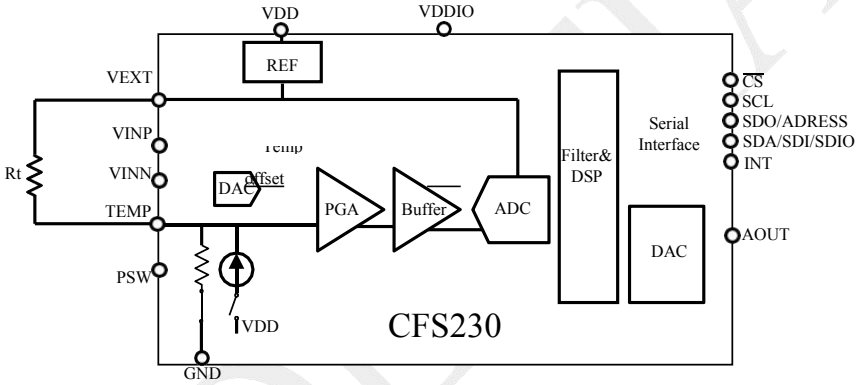


Figure4.3 External temperature sensing with pull-down resistance connected ('temp_sel'== 00b)

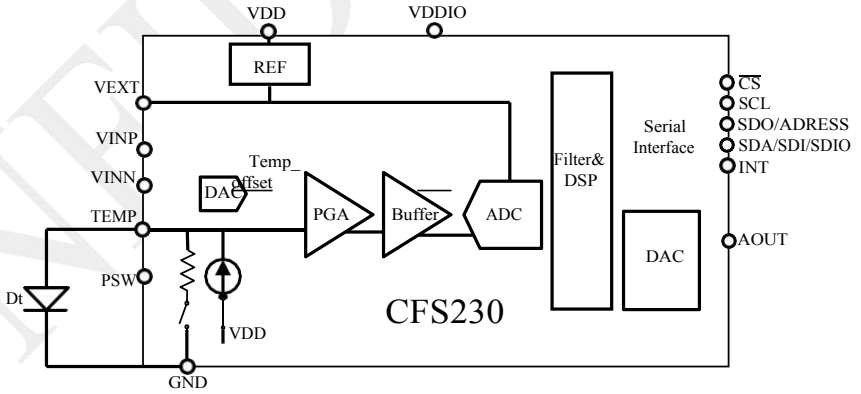


Figure4.4 External temperature sensing with a 20uA current source connected ('temp_sel'== 01b)

Setting 'measurement_control' = 00 and 'sco' = 1 to initiate once single-shot temperature conversion, the chip powers up, performs once temperature conversion, and returns back to standby mode with automatically changing 'sco' to 0. When setting 'raw_data_on' = 0, the calibrated temperature data is stored in "temp_out" registers and else, the raw ADC data of the temperature channel conversion would be stored in the "data_out" registers. INT pin also goes high when the conversion ends and will return low after a reading of the "temp_out" or "data_out" registers.

The gain of the external temperature conversion channel can be configured by the bits 'Gain_T' from 1X to 64X and the gain of the internal temperature conversion channel is fixed. The OSR for the sensor conversion is configured by the 'OSR_T' bits from 256X to 32768X.

4.1.4.3. Combined conversion

Setting 'measurement_control' = 10 and 'sco' = 1 to initiate once combined conversion, the chip powers up, successively performs once temperature conversion and once sensor signal conversion, then returns back to standby mode with automatically changing 'sco' to 0. The 'raw_data_on' bit should be set 0 during combined conversion and the calibrated temperature data and sensor signal data are separately stored in 'temp_out' and 'data_out' registers. INT pin will go high when the sensor signal conversion ends and will return low after a reading of the "data_out" registers.

The gain and OSR of the temperature channel and sensor signal channel are separately configured by the bits 'Gain_P', 'OSR_P', 'Gain_T' and 'OSR_T' just as the single shot conversions.

4.1.4.4. Sleep conversion

Setting 'measurement_control' = 11 and 'sco' = 1 to get into sleep conversion mode, the chip powers up and periodically performs once temperature conversion, once sensor signal conversion and a period of sleep phase. The duration of the sleep phase is configured by the 'sleep_time' bits from 64ms to 1s. The chip will not get back to standby mode until manually setting 'sco' bit to '0'. The 'raw_data_on' bit will be forced to 0 during sleep conversion and the calibrated temperature data and sensor signal are separately stored in 'temp_out' and 'data_out' registers. INT pin will go high when the sensor signal conversion ends and will automatically return low before next temperature conversion starting or after a reading of the "data_out" registers.

The gain and OSR of the temperature channel and sensor signal channel are separately configured by the bits 'Gain_P', 'OSR_P', 'Gain_T' and 'OSR_T' just as the single shot conversions.

4.1.4.5. Analog Output Mode

Set 'dac_on' =1 to get into the analog output mode (no matter what 'CMD' registers contents). During analog output mode, the CFS2300 alternately performs 64/32/16/1 times pressure conversions and once temperature conversion automatically. The higher 12 bits (without the sign bit) of the calibrated pressure data will be mapped to the VOUT pin with the equations below and all negative data_out values will be mapped to the lower limit voltage. Calibration coefficients must be carefully set in this mode to make the full span of the pressure data occupies the full span of the output voltage.

$$AOUT = \frac{data\_out[22:11]}{4096} * VDD(Aout\_sel = 0)$$

$$AOUT = \frac{data\_out[22:11]}{4096} * 1.5 * VEXT(Aout\_sel = 1)$$

The DAC allows programming a lower and upper clipping limit for the output signal. The internal 12-bit calculated bridge value is compared against the 12-bit value formed by {11, DAC_limit_h[3:0],111111} for the upper limit and {00,DAC_limit_l[3:0],000000} for the lower limit. If the calculated pressure value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this value; otherwise it is output as is

4.1.4.6. Diagnostic features

A suite of diagnostic features are provided on CFS2300 through six fault monitor comparators, refer to figure 4.5.

When diagnostics are enabled by set 'diag_on' to 1, two branches of 100nA current sources are added on the input pair from sensor. This will add some voltage shift to the input signal but mostly common mode drift and any error introduced could be minimized during sensor calibration. Four comparators are used to monitor if the voltage is in 100mV range of VEXT or ground. User could use this information to find out sensor faults like loss of bridge positive, loss of bridge negative, open sensor connection and sensor input short.

The outputs of all the comparators are locked into the 'Error_code<3:0>' register at the end of every data conversion. When either of the fault comparator outputs is asserted, indicating a fault, CFS2300 analog output VOUT will be forced to a fault indicating voltage level of 2.5% of AVDD. Together with the lower or upper clip limit function, system diagnostic can be performed to determine if the sensor is detective or the process being monitored by the sensor is out of range.

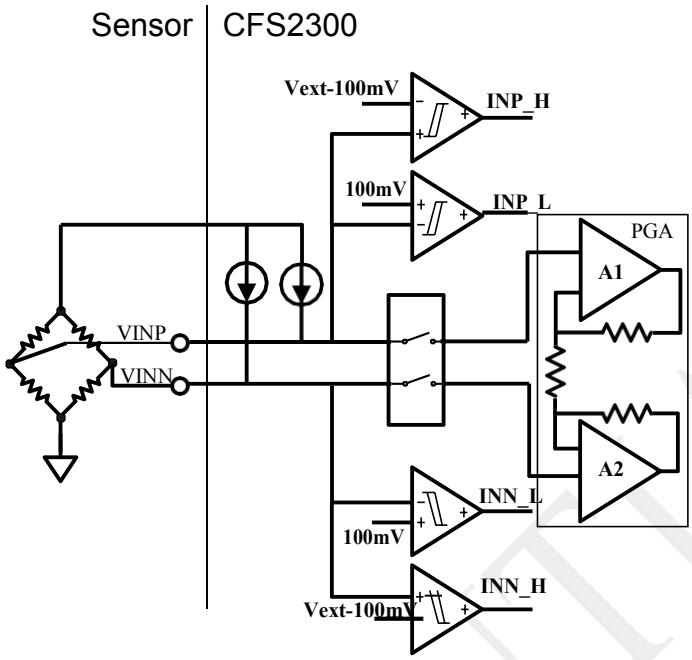


Figure4.5 CFS2300 Fault Monitoring System

4.2. OTP

The CFS2300 contains 224 OTP bits. The lower 200 bits are released to customer to program the default configurations and the sensor calibration coefficients, and the higher 24bits are reserved for internal trimming and will be pre-programmed in factory. The reg0xbc and its corresponding OTP bits are used as OTP redundancy pointer, which can write one OTP bit address and make this OTP bit functioning as programmed even if it has not been programmed or programming failed. E.g. Writing Reg0xbc to 0x1a can make the 26 t OTP bit functioning as being programmed even if this OTP bit is not actually programmed.

To program the OTP bits, please follow steps below:

1. Write all OTP registers what you want toprogram.
2. Switch the supply voltage on the VDD pin to 6.5V
3. Write Reg0x30 with 0x0C to enter OTP program mode
4. Write Reg0x6C with 01101010b to start OTP programming.
5. Waiting 10ms
6. Switch the supply voltage on the VDD back to 2.5V
7. Write Reg0x6C with 00000001b to set the OTP read out margin.
8. Write Reg0x00 with 0x24 to soft reset the CFS2300
9. Read the OTP banks back to check if program succeeded.

4.3. SENSOR CALIBRATION

CFS2300 offers an on-chip calibration for sensor offset, sensitivity, temperature drift and non-linearity with the quotations below and the maximum range for sensors that can be calibrated by CFS2300 is shown in table 4.4. To get the calibration coefficient for a particular sensor, please contact Novosense customer support for coefficient calculating kits.

$$P' - P_0 = (CNT_{sense} - (CNT_{off} + CTC_1 (T - T_0) + CTC_2 (T - T_0)^2)) * (S_0 + STC_1 (T - T_0) + STC_2 (T - T_0)^2)$$

$$P - P_0 = (P' - P_0) + K_s \cdot (P' - P_0)^2 + K_s \cdot (P' - P_0)^3$$

Table4.4 Maximum range of sensors allowed for CFS2300

Symbol	Description	Min	Max	Unit
Vfs	Full Span	+/-0.001	+/-1	V/V
STC1	1st temp drift for sensitivity	-0.0078	0.0078	Vfs/℃
STC2	2nd temp drift for sensitivity	-1.5e-5	1.5e-5	Vfs/℃2
Voff	Sensor offset	-1/GAIN < Voff+Vfs < 1/GAIN		V/V
CTC1	1st temp drift for Offset	-0.0078	0.0078	V/V/℃
CTC2	2nd temp drift for Offset	-1.5e-5	1.5e-5	V/V/℃2
Ks	2nd order non-linearity	-0.25	0.25	1/Vfs
Kss	2nd order non-linearity	-0.25	0.25	1/Vfs

Also, CFS2300 offers an on-chip calibration for both external and internal temperature sensing methods. After calibration, the CFS2300 can offer an real time temperature value of +/- 1℃ accuracy with the built-in temperature sensor during -40℃ and 85℃. Please contact Novosense customer support for coefficient calculating kits.

5.0 SPI INTERFACE

CFS2300 provides both SPI and I2C interface for serial communication and 'CSB' pin is used to switch between these two protocols. Pulling 'CSB' pin low selects the SPI interface, leaving 'CSB' pin float or puling it high selects the I2C interface.

5.1. INTERFACE SPECIFICATION

Table 5.1 SPI interface specifications

Symbol	Parameter	Condition	Min	Max	Unit
f_{sclk}	Clock frequency	Max load on SDIO or SDO = 25pF		10	MHz
t_{sclk_l}	SLCK low pulse		20		Ns
t_{sclk_h}	SLCK high pulse		20		
T_{sdi_setup}	SDI setup time		20		ns
T_{sdi_hold}	SDI hold time		20		ns
T_{sdo_od}	SDO/SDI output delay	Load = 25pF		30	ns
		Load = 250pF		40	ns
T_{csb_setup}	CSB setup time		20		ns
T_{csb_hold}	CSB hold time		40		ns

The figure below shows the definition of the SPI timing given in table 5.1

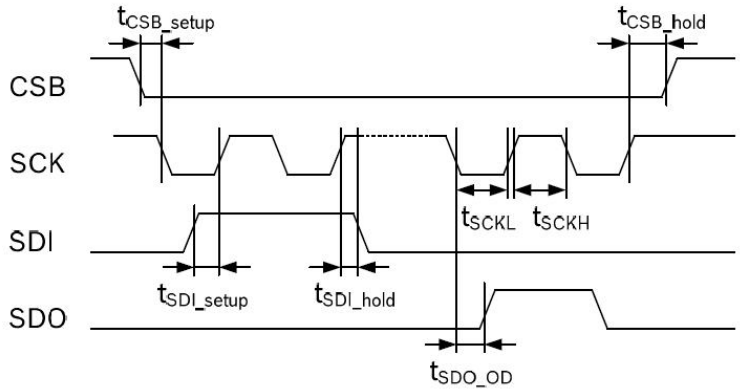


Figure 5.1 SPI timing diagram

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of framing. Once the beginning of the frame has been determined, timing is straightforward. The first phase of the transfer is the instruction phase, which consists of 16 bits followed by data that can be of variable lengths in multiples of 8 bits. If the device is configured with CSB tied low, framing begins with the first rising edge of SCLK.

The instruction phase is the first 16 bits transmitted. As shown in Figure 5.2, the instruction phase is divided into a number of bit fields.

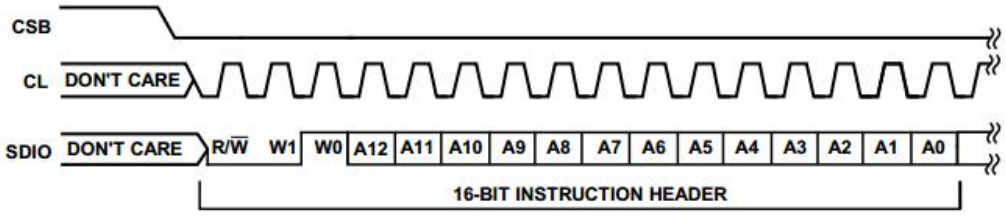


Figure 5.2 Instruction Phase Bit Field

The first bit in the stream is the read/write indicator bit (R/W). When this bit is high, a read is being requested, otherwise indicates it is a write operation.

W1 and W0 represent the number of data bytes to transfer for either read or write (Table 5.2). If the number of bytes to transfer is three or less (00, 01, or 10), CSB can stall high on byte boundaries. Stalling on a nonbyte boundary terminates the communications cycle. If these bits are 11, data can be transferred until CSB transitions high. CSB is not allowed to stall during the streaming process.

The remaining 13 bits represent the starting address of the data sent. If more than one word is being sent, sequential addressing is used, starting with the one specified, and it either increments (LSB first) or decrements (MSB first) based on the mode setting.

Table5.2. W1 and W0 settings

W1:W0	Action	CSB stalling
00	1 byte of data can be transferred.	Optional
01	2 bytes of data can be transferred.	Optional
10	3 bytes of data can be transferred.	Optional
11	4 or more bytes of data can be transferred. CSB must be held low for entire sequence; otherwise, the cycle is terminated.	No

Data follows the instruction phase. The amount of data sent is determined by the word length (Bit W0 and Bit W1). This can be one or more bytes of data. All data is composed of 8-bit words.

Data can be sent in either MSB-first mode or LSB-first mode (by setting 'LSB_first' bit). On power up, MSB-first mode is the default. This can be changed by programming the configuration register. In MSB-first mode, the serial exchange starts with the highest-order bit and ends with the LSB. In LSB-first mode, the order is reversed. (Figure 5.3)

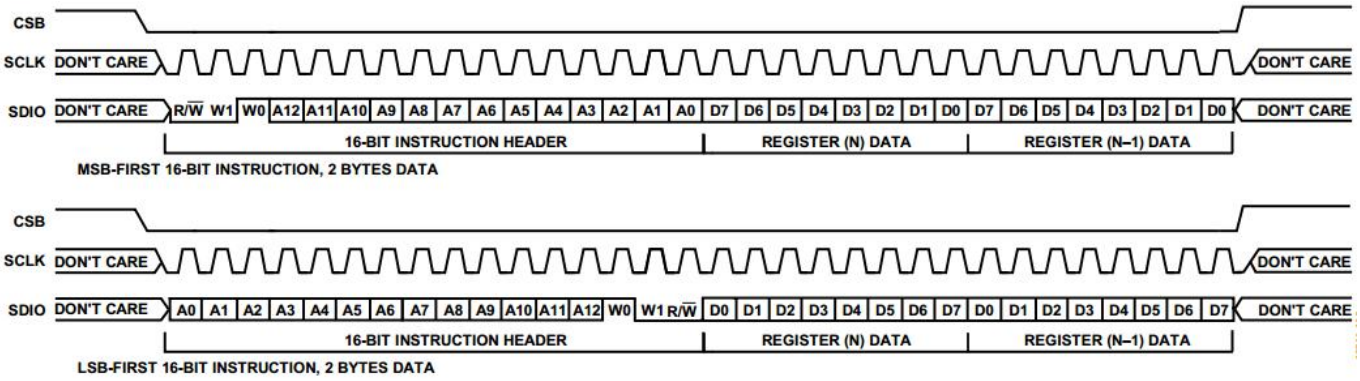


Figure5.3: MSB First and LSB First Instruction and Data Phases

Register bit 'SDO_active' is responsible for activating SDO on devices. If this bit is cleared, then SDO is inactive and read data is routed to the SDIO pin. If this bit is set, read data is placed on the SDO pin. The default for this bit is low, making SDO inactive.

6.0 I2C INTERFACE

I2C bus uses SCL and SDA as signal lines. Both lines are connected to VDDIO externally via pull-up resistors so that they are pulled high when the bus is free. The I2C device address of CFS2300 is shown below. The LSB bit of the 7bits device address is configured via SDO/ADDR pin.

Table6.1 I2C Address.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	0	1	1	0	SDO/ADDR	0/1

Table 6.2 Electrical specification of the I2C interface pins

Symbol	Parameter	Condition	Min	Max	Unit
f_{scl}	Clock frequency			400	kHz
t_{LOW}	SCL low pulse		1.3		us
t_{HIGH}	SCL high pulse		0.6		us
t_{SUDAT}	SDA setup time		0.1		us
t_{HDDAT}	SDA hold time		0.0		us
t_{SUSTA}	Setup Time for a repeated start condition		0.6		us
t_{HDSTA}	Hold time for a start condition		0.6		Us
t_{SUSTO}	Setup Time for a stop condition		0.6		Us
t_{BUF}	Time before a new transmission can start		1.3		Us

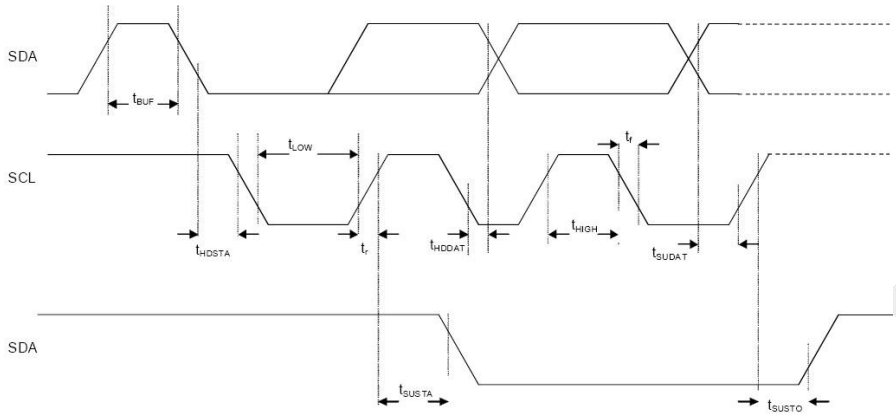


Figure 6.1 I2C Timing Diagram

The I2C interface protocol has special bus signal conditions. Start (S), stop (P) and binary data conditions are shown below. At start condition, SCL is high and SDA has a falling edge. Then the slave address is sent. After the 7 address bits, the direction control bit R/W selects the read or write operation. When a slave device recognizes that it is being addressed, it should acknowledge by pulling SDA low in the ninth SCL (ACK) cycle.

At stop condition, SCL is also high, but SDA has a rising edge. Data must be held stable at SDA when SCL is high. Data can change value at SDA only when SCL is low.

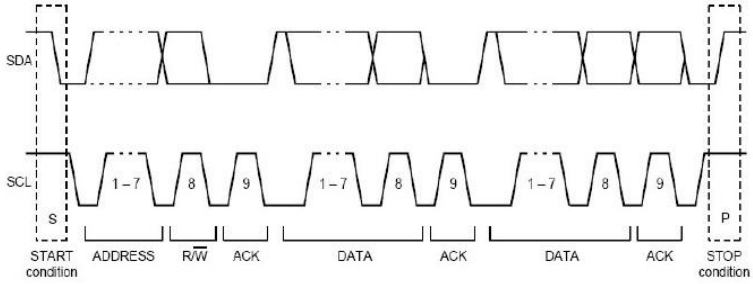


Figure 6.2 I2C Protocol

7.0 ONE WIRE INTERFACE

Besides the serial interfaces, the BMA230 also employs a one wire digital interface (OWI), which combines a simple and easy protocol with a cost saving pin sharing. Both the analog voltage output and this digital interface occur over the same pin. An advantage of this OWI interface is that it enables “end of line” calibration – no additional pins are required to digitally calibrate a finished assembly. Please contact NOVOSENSE for details.

8.0 PAD ASSIGNMENT

The CFS2300 is offered either via bare die or SOP-8 Package. The pad location and description of bare dies are shown in Fig8.1

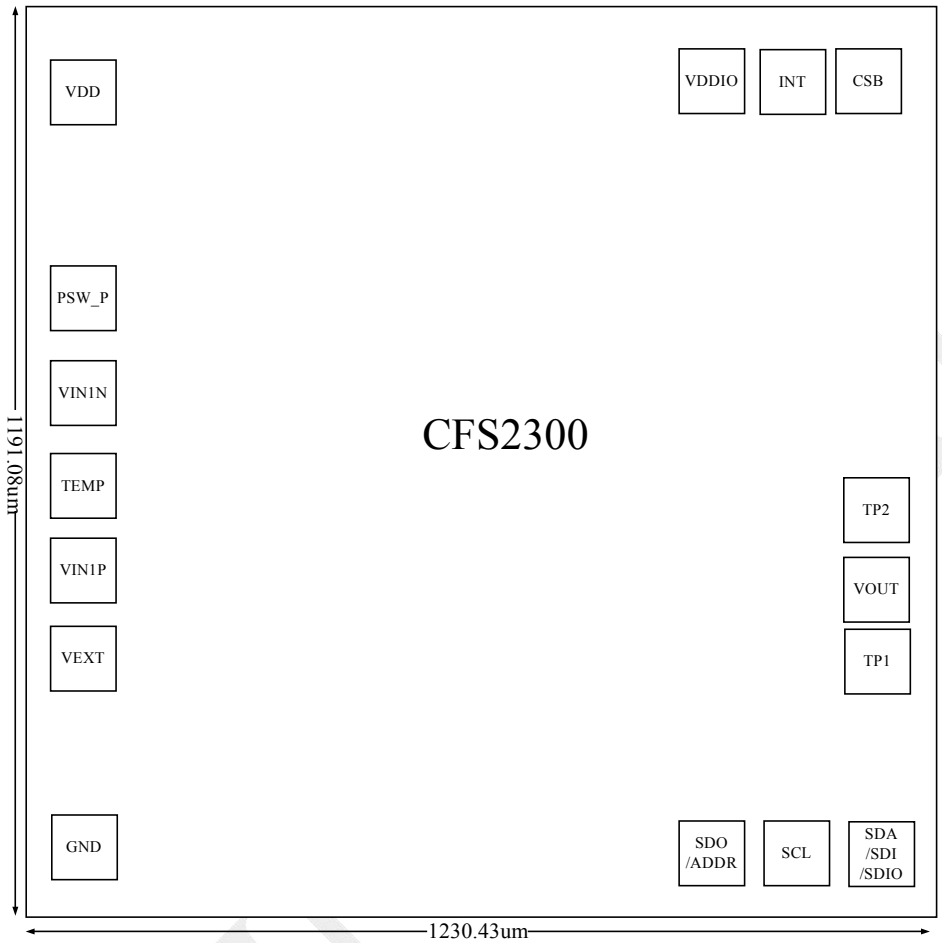


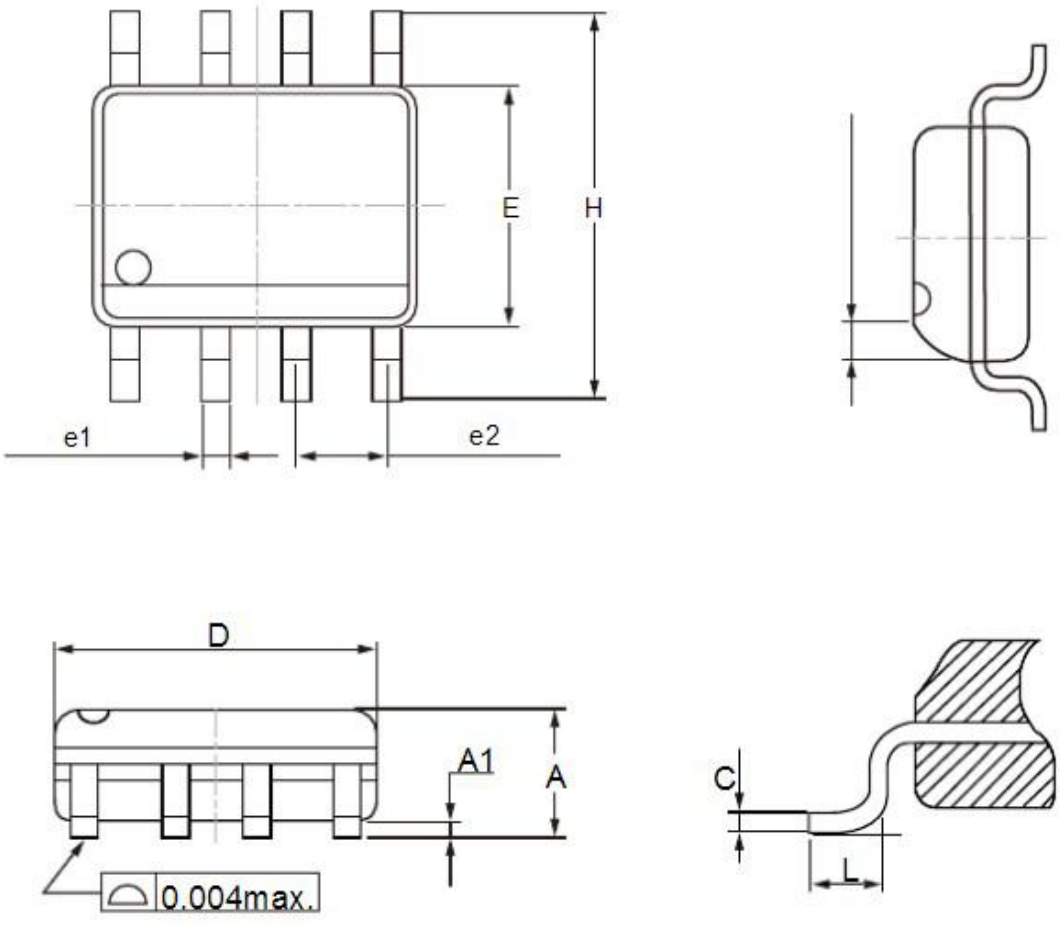
Fig8.1 Pin Assignment

Table 8.1 PAD Description

Pin Name	**Type**	**Description**
VDD	Power supply	Power supply for core circuits
VEXT	Analog output	Excitation voltage for Mass sensor
PSW	Analog output	Low-side Power Switch connection for pressure sensor
TEMP	Analog output	External temperature sensor input
VINP	Analog input	Positive analog Input Pins
VINN	Analog input	Negative analog Input Pins
GND	Power supply	Ground supply
SDO/ADDR	Digital output	Serial data output in 4-wire SPI mode Address select in I2C mode
SCL	Digital input	Serial clock
SDA/SDI/SDIO	Digital input	Serial data input/output in I2C mode (SDA) Serial data input in 4-wire SPI mode (SDI) Serial data input/output in 3-wire SPI mode (SDIO)

INT	Digital output	Interrupt output (data ready)
CSB	Digital input	Chip select
VDDIO	Power supply	Power Supply for I/O Circuit
VOUT/OWI	Analog output / Digital Inout	DAC output / One Wire Interface
TP1	Analog output	Test pad, internal use
TP2	Analog Output	Test Pad, internal use

The CFS2300 is also offered via SOP-8 package, the dimensions are shown in fig8.2 Note that, only SPI serial interface can not be used in the packaged version.



SYMBOLS	Millimeters			Inches		
	MIN.	Nom.	MAX.	MIN.	Nom.	MAX.
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	0.17	0.25	0.004	0.007	0.010
C	0.18	0.22	0.25	0.007	0.009	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.158
H	5.80	6.00	6.20	0.229	0.236	0.244
e1	0.35	0.43	0.56	0.014	0.017	0.022
e2	1.27BSC			0.05BSC		
L	0.40	0.65	1.27	0.016	0.026	0.050

Fig8.2 Dimensions for SOP-8 package

The pin allocations for SOP-8 packaged CFS2300 are shown in Fig8.3.

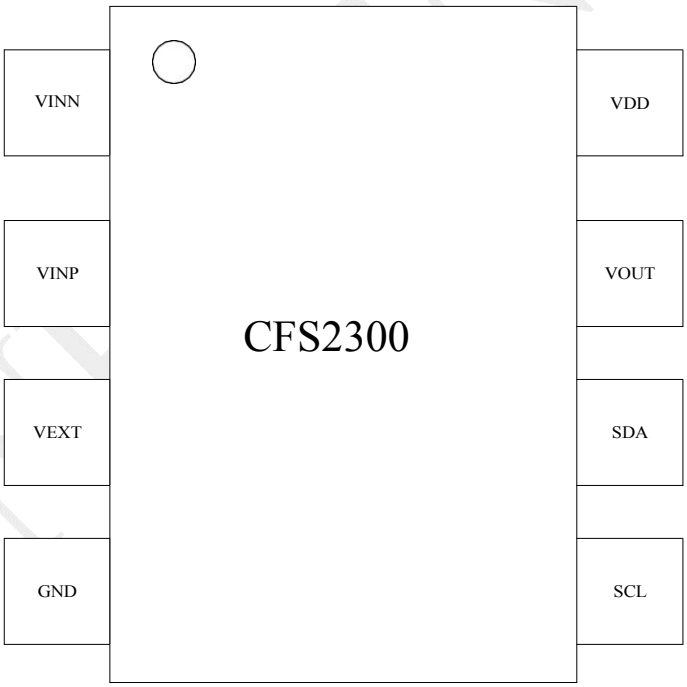


Fig8.3 pin assignment for SOP-8 package(Top View)

The CFS2300 is also offered via MSOP-10 package, the pin assignment shown in fig8.4

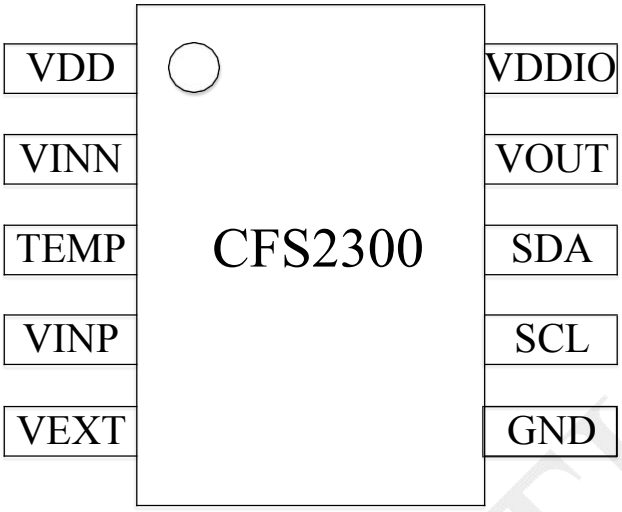


Fig8.4 Pin assignment for MSOP-10 package (Top View)

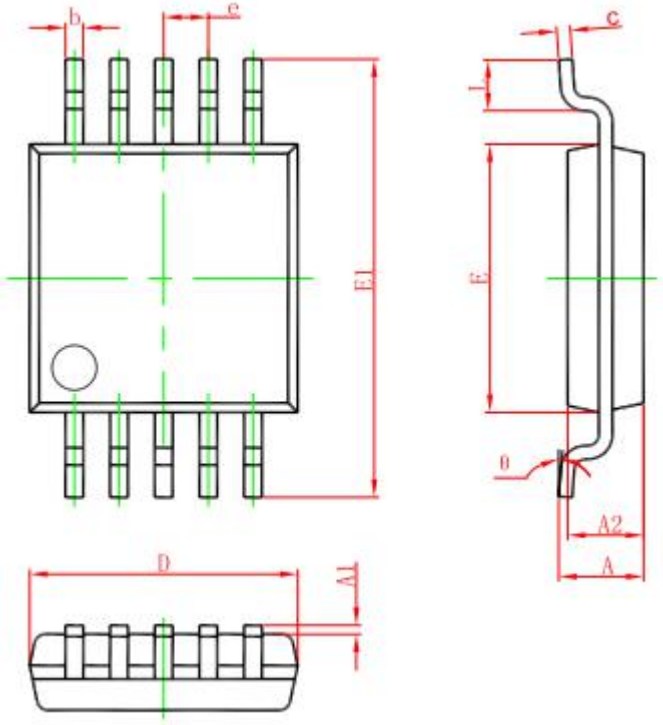


Fig8.5 MSOP-10 package Outline

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Fig8.6 MSOP-10 package Outline Dimensions

Table 8.2 PAD Description for SOP-8&MSOP-10 Packaged

Pin Name	**Type**	**Description**
VINN	Analog input	Negative analog Input Pins
VINP	Analog input	Positive analog Input Pins
VEXT	Analog output	Excitation voltage for Mass sensor
GND	Analog input	Ground supply
SCL	Digital input	Serial clock
SDA	Digital input	Serial data input/output in I2C mode (SDA)
VOUT/OWI	Analog output / Digital Inout	DAC output / One Wire Interface
VDD	Power supply	SOP8:Power supply for both core and IO circuits; MSOP10:Power supply for core
VDDIO	Power supply	MSOP10 only; Power supply for IO circuits
TEMP	Analog input	MSOP10 only; External temperature sensor input

9.0 TYPICAL APPLICATION

9.1. I2C MODE FOR BARE DIE

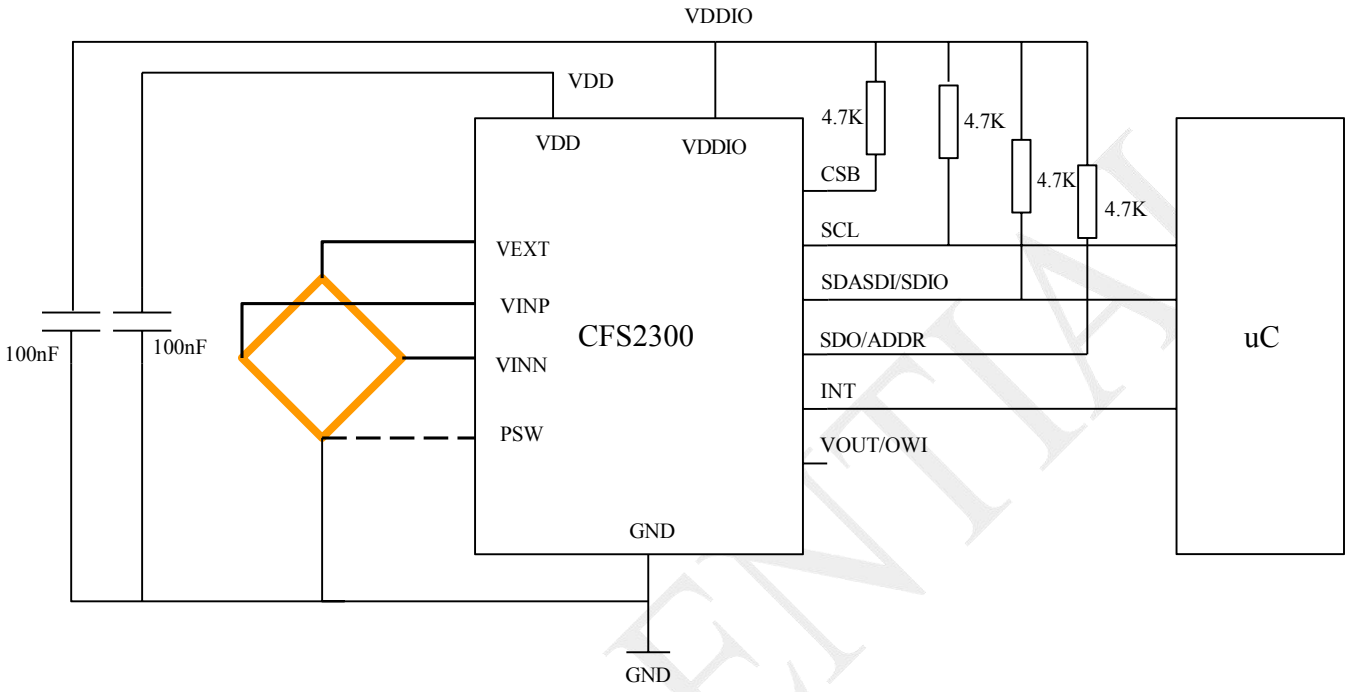


Fig9.1 Typical Application (I2C Mode)

9.2. SPI MODE FOR BARE DIE

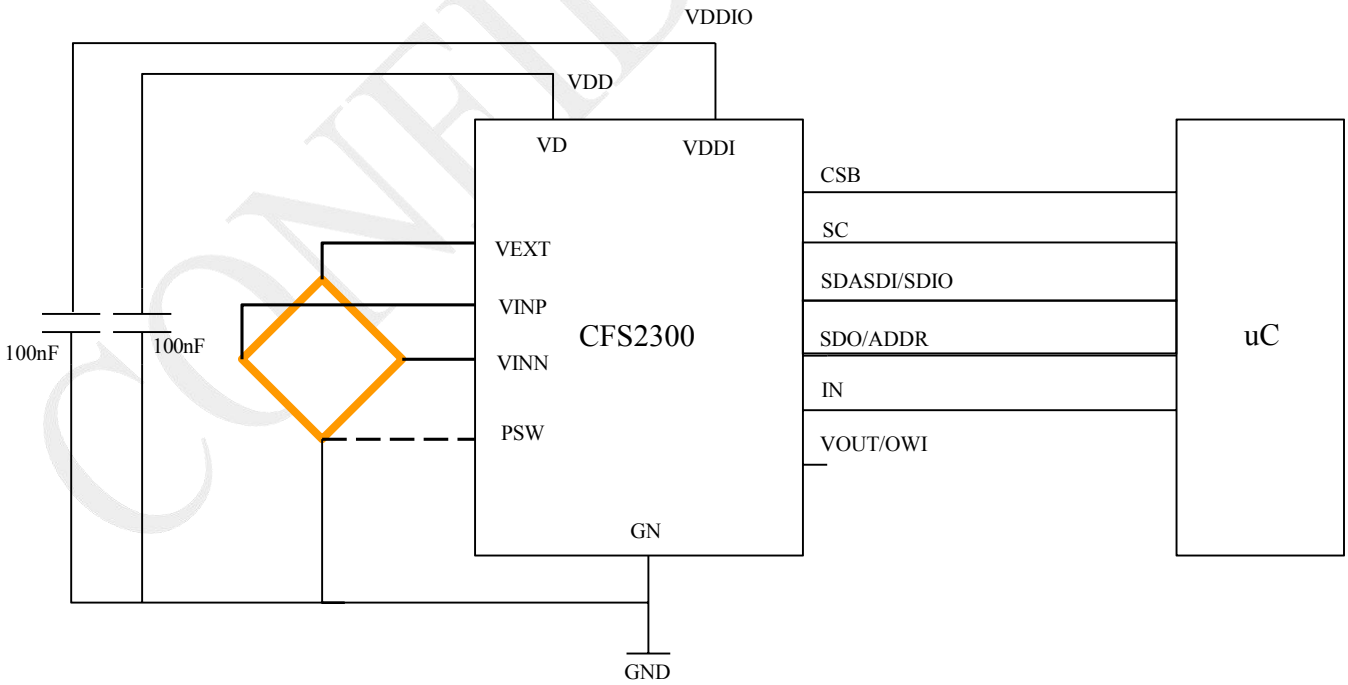


Fig9.2 Typical Application (SPI Mode)

9.3. OWI MODE FOR BARE DIE

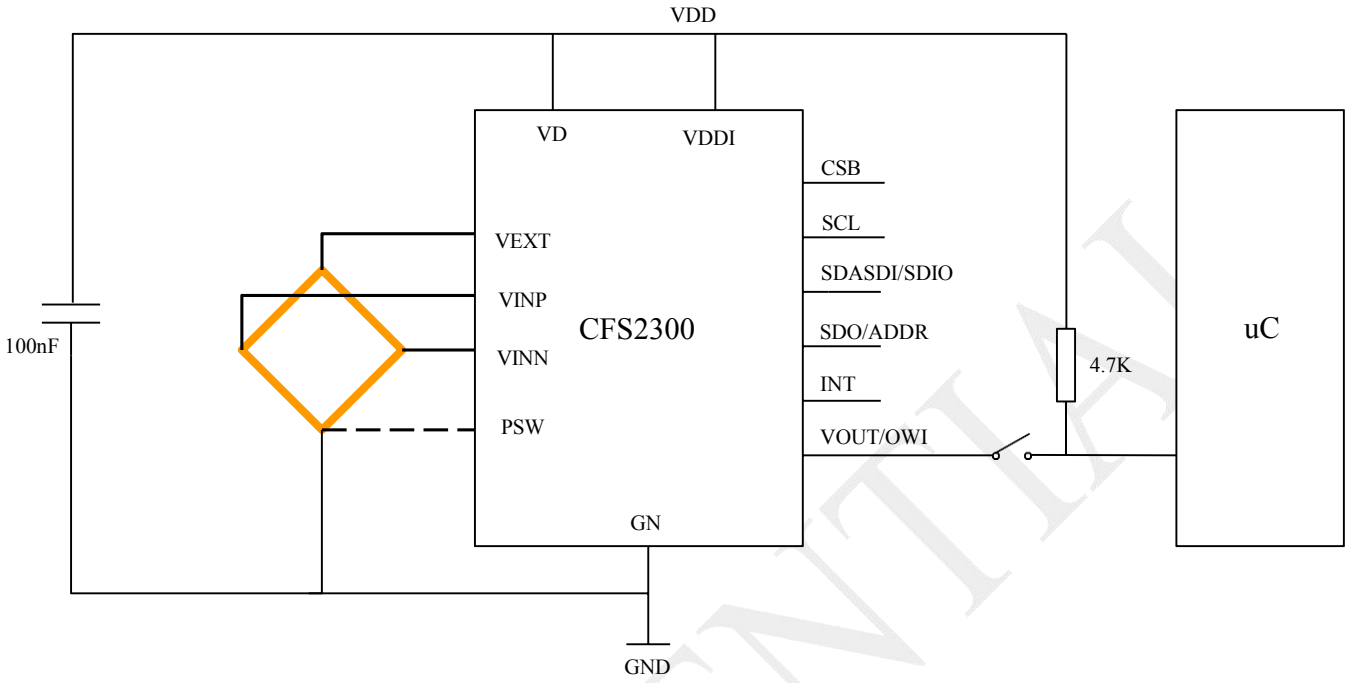


Fig9.3 Typical Application (OWI Mode)

9.4. I2C MODE FOR SOP-8 PACKAGED CHIP

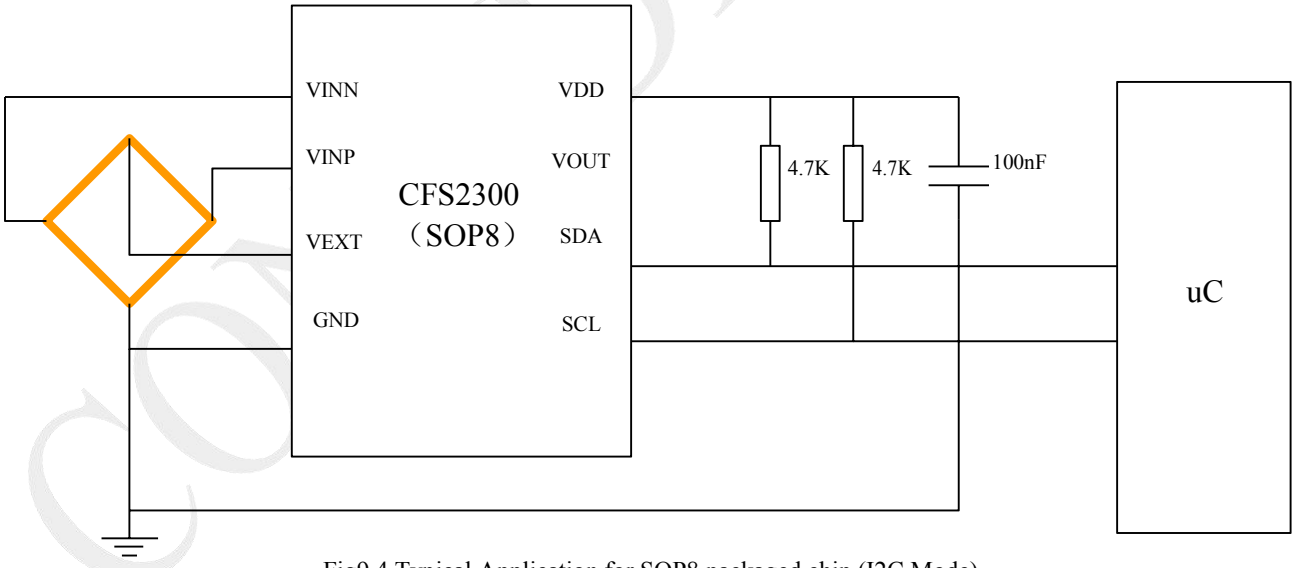


Fig9.4 Typical Application for SOP8 packaged chip (I2C Mode)

9.5. OWI MODE FOR SOP-8 PACKAGED CHIP

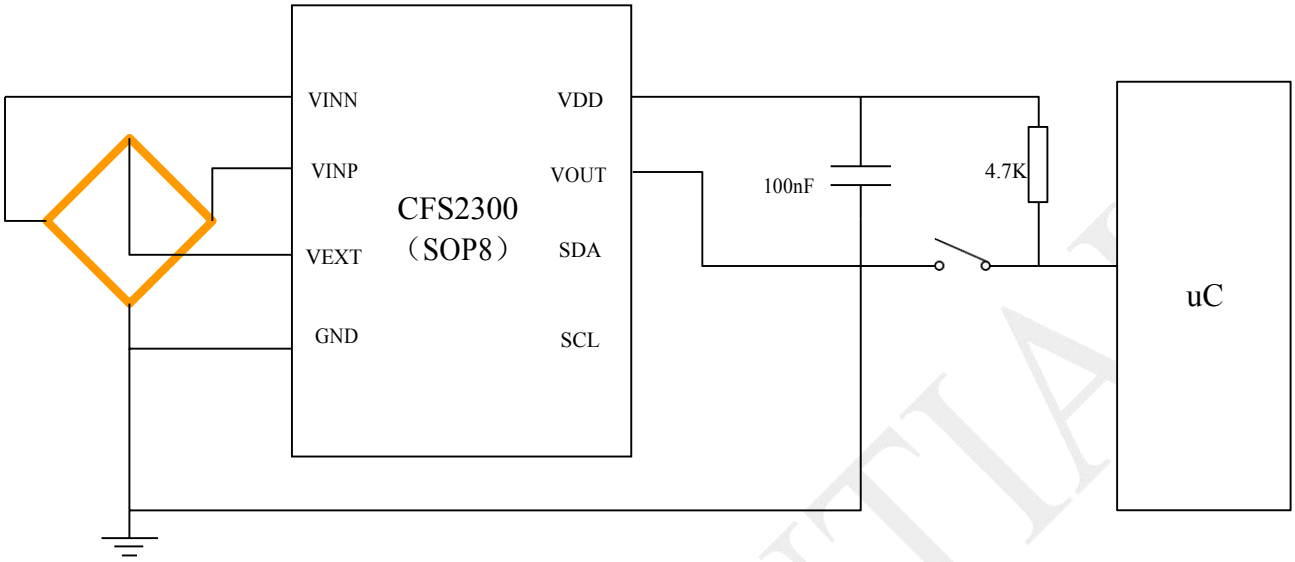


Fig9.5 Typical Application for SOP8 packaged chip (OWI Mode)

10.0 ORDER INFORMATION

Part NO	Unit	Description
CFS2300_B	pcs	Bare die
CFS2300_P	pcs	SOP-8 packaged

11.0 DOCUMENT HISTORY AND MODIFICATION

Revision	Description	Date
1.0	Initial Version	2013-12-20
1.1	Add SOP-8 Package information	2013-3-5
1.2	Add application note for SOP8 package	2014-4-1
1.4	Correct the application Diagram	2014-06-03
1.5	Add gain=2X, 128X	2014-7-22
1.6	Update for CFS2300C. 1) Update Diagnostic features, in both register map and block description 2) Update bare die pad floor plan by rename the original GND pad near AOUT to TP2.	2014/12/05
1.7	TEMP sensor select mode change	2015/6/26
1.8	Update ENOB data, typical application circuit	2015/8/24
1.9	Add MSOP10 Package information	2015/12/11