Cray-1/2/3/4

Vortragsvorbereitung @ VCFE/VCFB

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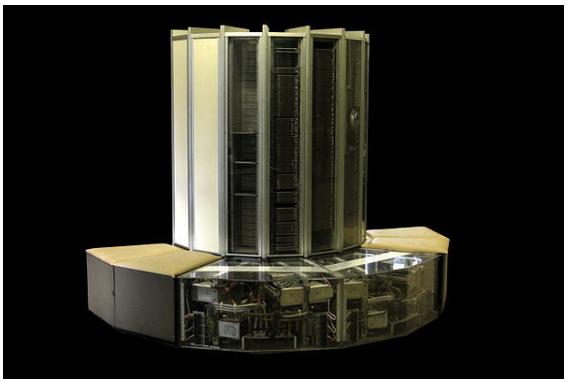
Chapter 1

Cray-1



Cray-1 with internals exposed at EPFL

The **Cray-1** was a supercomputer designed, manufactured and marketed by Cray Research. The first Cray-1 system was installed at Los Alamos National Laboratory in 1976 and it went on to become one of the best known and most successful supercomputers in history. The Cray-1's architect was Seymour Cray; the chief engineer was Cray Research co-founder Lester Davis.[2]

1.1 History

From 1968 to 1972 Seymour Cray of Control Data Corporation (CDC) worked on the CDC 8600, the successor to his earlier CDC 6600 and CDC 7600 designs. The 8600 was essentially made up of four 7600s in a box with an additional special mode that allowed them to operate lock-step in a SIMD fashion.

Jim Thornton, formerly Cray's engineering partner on earlier designs, had started a more radical project known as the CDC STAR-100. Unlike the 8600's brute-force approach to performance, the STAR took an entirely different route. In fact the main processor of the STAR had less performance than the 7600, but added additional hardware and instructions to speed up particularly common supercomputer tasks.

By 1972, the 8600 had reached a dead end; the machine was so incredibly complex that it was impossible to get one working properly. Even a single faulty component would render the machine non-operational. Cray went to William Norris, Control Data's CEO, saying that a redesign from scratch was needed. At the time the company was in serious financial trouble, and with the STAR in the pipeline as well, Norris could not invest the money.

As a result, Cray left CDC and started Cray Research very close to the CDC lab. In the back yard of the land he purchased in Chippewa Falls, Cray and a group of former CDC employees started looking for ideas. At first the concept of building another supercomputer seemed impossible, but after Cray Research's Chief Technology Officer traveled to Wall Street and found a lineup of investors willing to back Cray, all that was needed was a design.

For four years Cray Research designed its first computer.[3] In 1975 the 80 MHz Cray-1 was announced. Excitement was so high that a bidding war for the first machine broke out between Lawrence Livermore National Laboratory and Los Alamos National Laboratory, the latter eventually winning and receiving serial number 001 in 1976 for a six-month trial. The National Center for Atmospheric Research (NCAR) was the first official customer of Cray Research in 1977, paying US$8.86 million ($7.9 million plus $1 million for the disks) for serial number 3. The NCAR machine was decommissioned in 1989.[4] The company expected to sell perhaps a dozen of the machines, and set the selling price accordingly, but ultimately over 80 Cray-1s of all types were sold, priced from $5M to $8M. The machine made Seymour Cray a celebrity and his company a success, lasting until the supercomputer crash in the early 1990s.

Based on a recommendation by William Perry's study, the NSA purchased a Cray-1 for theoretical research in cryptanalysis. According to Budiansky, "Though standard histories of Cray Research would persist for decades in stating that the company's first customer was Los Alamos National Laboratory, in fact it was NSA..."[5]

The 160 MFLOPS Cray-1 was succeeded in 1982 by the 800 MFLOPS Cray X-MP, the first Cray multiprocessing computer. In 1985 the very advanced Cray-2, capable of 1.9 GFLOPS peak performance, succeeded the first two models but met a somewhat limited commercial success because of certain problems at produc-

ing sustained performance in real-world applications. A more conservatively designed evolutionary successor of the Cray-1 and X-MP models was therefore made by the name Cray Y-MP and launched in 1988.

As a comparison standpoint, the processor in a typical 2013 smartphone performs at roughly 1 GFLOPS.[6]

1.2 Background

Typical scientific workloads consist of reading in large data sets, transforming them in some way and then writing them back out again. Normally the transformations being applied are identical across all of the data points in the set. For instance, the program might add 5 to every number in a set of a million numbers.

In traditional computers the program would loop over all million numbers, adding five, thereby executing a million instructions saying a = add b, c. Internally the computer solves this instruction in several steps. First it reads the instruction from memory and decodes it, then it collects any additional information it needs, in this case the numbers b and c, and then finally runs the operation and stores the results. The end result is that the computer requires tens or hundreds of millions of cycles to carry out these operations.

1.2.1 Vector machines

In the STAR, new instructions essentially wrote the loops for the user. The user told the machine where in memory the list of numbers was stored, then fed in a single instruction a(1..1000000) = addv b(1..1000000), c(1..1000000). At first glance it appears the savings are limited; in this case the machine fetches and decodes only a single instruction instead of 1,000,000, thereby saving 1,000,000 fetches and decodes, perhaps one-fourth of the overall time.

The real savings are not so obvious. Internally, the CPU of the computer is built up from a number of separate parts dedicated to a single task, for instance, adding a number, or fetching from memory. Normally, as the instruction flows through the machine, only one part is active at any given time. This means that each sequential step of the entire process must complete before a result can be saved. The addition of an instruction pipeline changes this. In such machines the CPU will "look ahead" and begin fetching succeeding instructions while the current instruction is still being processed. In this assembly line fashion any one instruction still requires as long to complete, but as soon as it finishes executing, the next instruction is right behind it, with most of the steps required for its execution already completed.

Vector processors use this technique with one additional trick. Because the data layout is in a known format — a set of numbers arranged sequentially in memory — the pipelines can be tuned to improve the performance of fetches. On the receipt of a vector instruction, special hardware sets up the memory access for the arrays and stuffs the data into the processor as fast as possible.

CDC's approach in the STAR used what is today known as a *memory-memory architecture*. This referred to the way the machine gathered data. It set up its pipeline to read from and write to memory directly. This allowed the STAR to use vectors of any length, making it highly flexible. Unfortunately, the pipeline had to be very long in order to allow it to have enough instructions in flight to make up for the slow memory. That meant the machine incurred a high cost when switching from processing vectors to performing operations on individual randomly located operands. Additionally, the low scalar performance of the machine meant that after the switch had taken place and the machine was running scalar instructions, the performance was quite poor. The result was rather disappointing real-world performance, something that could, perhaps, have been forecast by Amdahl's law.

1.2.2 Cray's approach

Cray was able to look at the failure of the STAR and learn from it. He decided that in addition to fast vector processing, his design would also require excellent all-around scalar performance. That way when the machine switched modes, it would still provide superior performance. Additionally they noticed that the workloads could be dramatically improved in most cases through the use of registers.

Just as earlier machines had ignored the fact that most operations were being applied to many data points, the STAR ignored the fact that those same data points would be repeatedly operated on. Whereas the STAR would read and process the same memory five times to apply five vector operations on a set of data, it would be much faster to read the data into the CPU's registers once, and then apply the five operations. However, there were limitations with this approach. Registers were significantly more expensive in terms of circuitry, so only a limited number could be provided. This implied that Cray's design would have less flexibility in terms of vector sizes. Instead of reading any sized vector several times as in the STAR, the Cray-1 would have to read only a portion of the vector at a time, but it could then run several operations on that data prior to writing the results back to memory. Given typical workloads, Cray felt that the small cost incurred by being required to break large sequential memory accesses into segments was a cost well worth paying.

Since the typical vector operation would involve loading a small set of data into the vector registers and then running several operations on it, the vector system of the new design had its own separate pipeline. For instance, the multiplication and addition units were implemented as

separate hardware, so the results of one could be internally pipelined into the next, the instruction decode having already been handled in the machine's main pipeline. Cray referred to this concept as *chaining*, as it allowed programmers to "chain together" several instructions and extract higher performance.

1.3 Description

The new machine was the first Cray design to use integrated circuits (ICs). Although ICs had been available since the 1960s, it was only in the early 1970s that they reached the performance necessary for high-speed applications. The Cray-1 used only four different IC types, an ECL dual 5-4 NOR gate (one 5-input, and one 4-input, each with differential output),[7] another slower MECL 10K 5-4 NOR gate used for address fanout, a 16×4-bit high speed (6 ns) static RAM (SRAM) used for registers and a 1,024×1-bit 48 ns SRAM used for the main memory.[8] These integrated circuits were supplied by Fairchild Semiconductor and Motorola. In all, the Cray-1 contained about 200,000 gates.

ICs were mounted on large five-layer printed circuit boards, with up to 144 ICs per board. Boards were then mounted back to back for cooling (see below) and placed in twenty-four 28-inch-high (710 mm) racks containing 72 double-boards. The typical module (distinct processing unit) required one or two boards. In all the machine contained 1,662 modules in 113 varieties.

Each cable between the modules was a twisted pair, cut to a specific length in order to guarantee the signals arrived at precisely the right time and minimize electrical reflection. Each signal produced by the ECL circuitry was a differential pair, so the signals were balanced. This tended to make the demand on the power supply more constant and reduce switching noise. The load on the power supply was so evenly balanced that Cray boasted that the power supply was unregulated. To the power supply, the entire computer system looked like a simple resistor.

The high-performance ECL circuitry generated considerable heat, and Cray's designers spent as much effort on the design of the refrigeration system as they did on the rest of the mechanical design. In this case, each circuit board was paired with a second, placed back to back with a sheet of copper between them. The copper sheet conducted heat to the edges of the cage, where liquid Freon running in stainless steel pipes drew it away to the cooling unit below the machine. The first Cray-1 was delayed six months due to problems in the cooling system; lubricant that is normally mixed with the Freon to keep the compressor running would leak through the seals and eventually coat the boards with oil until they shorted out. New welding techniques had to be used to properly seal the tubing. The only patents issued for the Cray-1 computer concerned the cooling system design.

In order to bring maximum speed out of the machine, the entire chassis was bent into a large C-shape. Speed-dependent portions of the system were placed on the "inside edge" of the chassis, where the wire-lengths were shorter. This allowed the cycle time to be decreased to 12.5 ns (80 MHz), not as fast as the 8 ns 8600 he had given up on, but fast enough to beat CDC 7600 and the STAR. NCAR estimated that the overall throughput on the system was 4.5 times the CDC 7600.[9]

The Cray-1 was built as a 64-bit system, a departure from the 7600/6600, which were 60-bit machines (a change was also planned for the 8600). Addressing was 24-bit, with a maximum of 1,048,576 64-bit words (1 megaword) of main memory, where each word also had 8 parity bits for a total of 72 bits per word.[10] There were 64 data bits and 8 check bits. Memory was spread across 16 interleaved memory banks, each with a 50 ns cycle time, allowing up to four words to be read per cycle. Smaller configurations could have 0.25 or 0.5 megawords of main memory.

The main register set consisted of eight 64-bit scalar (S) registers and eight 24-bit address (A) registers. These were backed by a set of sixty-four registers each for S and A temporary storage known as T and B respectively, which could not be seen by the functional units. The vector system added another eight 64-element by 64-bit vector (V) registers, as well as a vector length (VL) and vector mask (VM). Finally, the system also included a 64-bit real-time clock register and four 64-bit instruction buffers that held sixty-four 16-bit instructions each. The hardware was set up to allow the vector registers to be fed at one word per cycle, while the address and scalar registers required two cycles. In contrast, the entire 16-word instruction buffer could be filled in four cycles.

The Cray-1 had twelve pipelined functional units. The 24-bit address arithmetic was performed in an add unit and a multiply unit. The scalar portion of the system consisted of an add unit, a logical unit, a population count, a leading zero count unit and a shift unit. The vector portion consisted of add, logical and shift units. The floating point functional units were shared between the scalar and vector portions, and these consisted of add, multiply and reciprocal approximation units.

The system had limited parallelism. It could fetch one instruction per clock cycle, operate on multiple instructions in parallel and retire up to two every cycle. Its theoretical performance was thus 160 MIPS (80 MHz x 2 instructions), although there were a few limitations that made floating point performance generally about 160[11] MFLOPS. However, by using vector instructions carefully and building useful chains, the system could peak at 250 MFLOPS.

Since the machine was designed to operate on large data sets, the design also dedicated considerable circuitry to I/O. Earlier Cray designs at CDC had included separate

computers dedicated to this task, but this was no longer needed. Instead the Cray-1 included four 6-channel controllers, each of which was given access to main memory once every four cycles. The channels were 16 bits wide and included 3 control bits and 4 for error correction, so the maximum transfer speed was 1 word per 100 ns, or 500 thousand words per second for the entire machine.

The initial model, the **Cray-1A**, weighed 5.5 tons including the Freon refrigeration system. Configured with 1 million words of main memory, the machine and its power supplies consumed about 115 kW of power; cooling and storage likely more than doubled this figure. A Data General SuperNova S/200 minicomputer served as the maintenance control unit (MCU), which was used to feed the Cray Operating System into the system at boot time, to monitor the CPU during use, and optionally as a front-end computer. Most, if not all Cray-1As were delivered using the follow-on Data General Eclipse as the MCU.

1.4 Cray-1S

The **Cray-1S**, announced in 1979, was an improved Cray-1 that supported a larger main memory of 1, 2 or 4 million words. The larger main memory was made possible through the use of 4,096 x 1-bit bipolar RAM ICs with a 25 ns access time.[12] The Data General minicomputers were optionally replaced with an in-house 16-bit design running at 80 MIPS. The I/O subsystem was separated from the main machine, connected to the main system via a 6 MB/s control channel and a 100 MB/s High Speed Data Channel. This separation made the 1S look like two "half Crays" separated by a few feet, which allowed the I/O system to be expanded as needed. Systems could be bought in a variety of configurations from the S/500 with no I/O and 0.5 million words of memory to the S/4400 with four I/O processors and 4 million words of memory.

1.5 Cray-1M

The **Cray-1M**, announced in 1982, replaced the Cray-1S.[13] It had a faster 12 ns cycle time and used less expensive MOS RAM in the main memory. The 1M was supplied in only three versions, the M/1200 with 1 million words in 8 banks, or the M/2200 and M/4200 with 2 or 4 million words in 16 banks. All of these machines included two, three or four I/O processors, and the system added an optional second High Speed Data Channel. Users could add a Solid-state Storage Device with 8 to 32 million words of MOS RAM.

1.6 Software

In 1978 the first standard software package for the Cray-1 was released, consisting of three main products:

- Cray Operating System (COS) (later machines would run UNICOS, Cray's UNIX flavor)
- Cray Assembly Language (CAL)
- Cray FORTRAN (CFT), the first automatically vectorizing Fortran compiler

The United States Department of Energy funded sites from Lawrence Livermore Laboratory, Los Alamos Scientific Laboratory, Sandia National Laboratory and the National Science Foundation supercomputer centers (for high-energy physics) represented the second largest block with LLL's Cray Time Sharing System (CTSS). CTSS was written in a dynamic memory Fortran, first named LRLTRAN, which ran on CDC 7600s, renamed CVC (pronounced "Civic") when vectorization for the Cray-1 was added. Cray Research attempted to support these sites accordingly. These software choices had influences on later minisupercomputers, also known as "crayettes".

NCAR has its own operating system (NCAROS).

The National Security Agency developed its own operating system (Folklore) and language (IMP with ports of Cray Pascal and C and Fortran 90 later)[14]

Libraries started with Cray Research's own offerings and Netlib.

Other operating systems existed, but most languages tended to be Fortran or Fortran-based. Bell Laboratories, as proof of both portability concept and circuit design, moved the first C compiler to their Cray-1 (non-vectorizing). This act would later give CRI a six-month head start on the Cray-2 Unix port to ETA Systems' detriment, and Lucasfilm's first computer generated test film, *The Adventures of André and Wally B.*.

Application software generally tends to be either classified (*e.g.* nuclear code, cryptanalytic code) or proprietary (*e.g.* petroleum reservoir modeling). This was because little software was shared between customers and university customers. The few exceptions were climatological and meteorological programs until the NSF responded to the Japanese Fifth Generation Computer Systems project and created its supercomputer centers. Even then, little code was shared.

1.7 Museums

Cray-1s are on display at the following locations:

- Bradbury Science Museum in Los Alamos, New Mexico

- Chippewa Falls Museum of Industry and Technology in Chippewa Falls, Wisconsin
- The Cray Inc. offices at Cray Plaza in St. Paul, Minnesota
- Computer History Museum in Mountain View, California[15]
- DigiBarn Computer Museum[16]
- Deutsches Museum in Munich
- École Polytechnique Fédérale de Lausanne in Lausanne, Switzerland
- ETH Zürich - Eidgenössische Technische Hochschule Zürich, Switzerland
- National Center for Atmospheric Research in Boulder, Colorado[17]
- National Air and Space Museum in Washington, D.C.[18]
- The National Museum of Computing at Bletchley Park[19]
- Science Museum in London[20]
- Swedish National Museum of Science and Technology in Stockholm, Sweden[21]

1.8 Other images of the Cray-1

-  Logic boards
-  Inside of the tower
-  Cooling system
-  Top of the casing
-  Close-up of logic boards
-  Cray-1A power supply detail
-  Cray-1 at Computer History Museum
-  Cray-1 at Computer History Museum
-  Cray-1 at Deutsches Museum

1.9 References

[1] Cray-1 Computer System Hardware Reference Manual 2240004, Rev C, Publication: 1977 November 4, Cray Research, Inc.

[2] C.J. Murray, "The ultimate team player," *Design News*, March 6, 1995.

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[8] RM Russell, "The CRAY-1 Computer System," *Comm. ACM*, January 1978, pp. 63–72.

[9] "SCD Supercomputer Gallery: CRAY1-A". National Center for Atmospheric Research.

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[17] "Cray 1". National Center for Atmospheric Research. Retrieved 2012-05-15.

[18] "National Air and Space Museum". Retrieved 2010-01-21. This object is on display in the Beyond The Limits exhibition at the National Mall building.

[19] "A Cray 1 Arrives". The National Museum of Computing. Retrieved 2014-02-27.

[20] "Cray 1A supercomputer, serial number 11, c 1979". NMSI. Retrieved 2012-05-15.

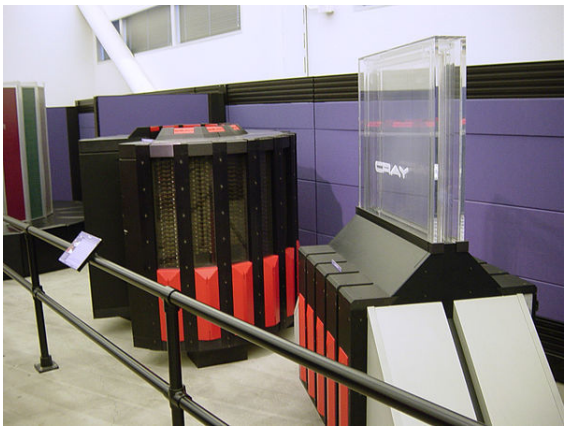
[21] TM44354 Dator Cray Research,Inc.Cray Research, Inc. 1976 SAAB Aerospace, p. 52, Datorföremål+på+TM.pdf. Retrieved 2012-05-15.

1.10 External links

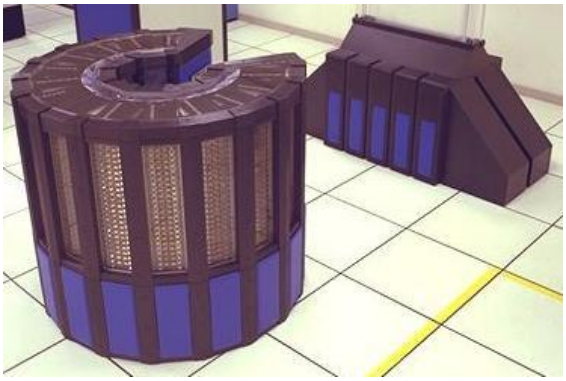
- *CRAY-1 Computer System Hardware Reference Manual*, Publication No. 2240004 Rev.C 11/77 (first three chapters) – From DigiBarn / Ed Thelen
- *CRAY-1 Computer System Hardware Reference Manual*, Publication No. 2240004 Rev.C 11/77 (full, scanned, PDF)
- Collection of on-line Cray manuals & documentation @ Bitsavers
- Cray Channels Magazine @ The Centre for Computing History
- Cray Manuals & Documentation @ The Centre for Computing History
- Cray Users Group Publications @ The Centre for Computing History
- NCAR Supercomputer Gallery
- Verilog definition of Cray-1A CPU logic

Chapter 2

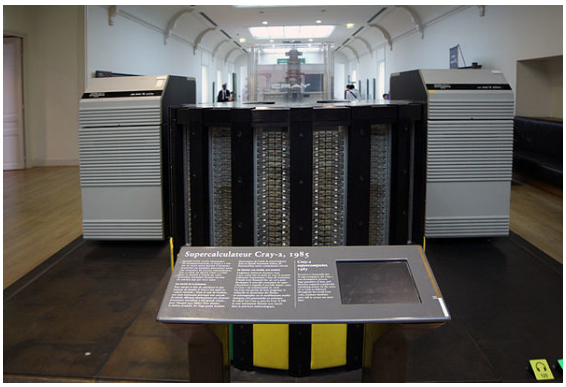
Cray-2



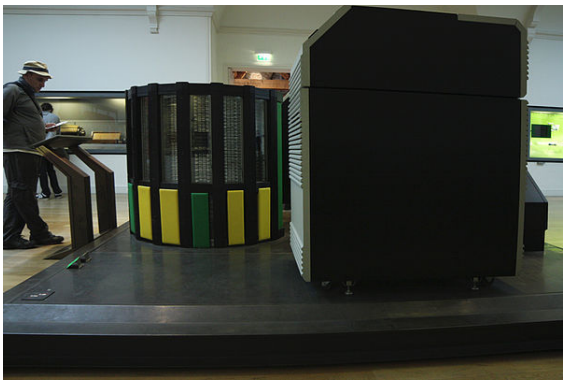
A Cray-2 and its Fluorinert-cooling "waterfall", formerly serial number 2101, the only 8-processor system ever made, for NERSC



A Cray-2 operated by NASA



Front view of 1985 Supercomputer Cray-2, Musée des Arts et Métiers, Paris



Side view of 1985 Supercomputer Cray-2, Musée des Arts et Métiers, Paris

The **Cray-2** is a supercomputer with four vector processors built with emitter-coupled logic and made by Cray Research starting in 1985. At 1.9 GFLOPS peak performance, it was the fastest machine in the world when it was released, replacing the Cray X-MP in that spot. The Cray-2 was replaced as the world's fastest computer by the ETA-10G in 1990.

2.1 Initial design

With the successful launch of his famed Cray-1, Seymour Cray turned to the design of its successor. By 1979 he had become fed up with management interruptions in what was now a large company, and as he had done in the past, decided to resign his management post and move to form a new lab. As with his original move to Chippewa Falls, Wisconsin from Control Data HQ in Minneapolis, Minnesota, Cray management understood his needs and supported his move to a new lab in Boulder, Colorado. Working as an independent consultant at these new Cray Labs, he put together a team and started on a completely new design. This Lab would later close, and a decade later a new facility in Colorado Springs would open.

Cray had previously attacked the problem of increased speed with three simultaneous advances: more functional

Detail of the upper part of the Cray-2

Inside of the Cray-2

units to give the system higher parallelism, tighter packaging to decrease signal delays, and faster components to allow for a higher clock speed. The classic example of this design is the CDC 8600, which packed four CDC 7600-like machines based on ECL logic into a 1 x 1 meter cylinder and ran them at an 8 ns cycle speed (125 MHz). Unfortunately the density needed to achieve this cycle time led to the machine's downfall. The circuit boards inside were densely packed, and since even a single malfunctioning transistor would cause an entire module to fail, packing more of them onto the cards greatly increased the chance of failure.

One solution to this problem, one that most computer vendors had already moved to, was to use integrated circuits (ICs) instead of individual components. Each IC included a selection of components from a module prewired into a circuit by the automated construction process. If an IC did not work, another one would be tried. At the time the 8600 was being designed the simple MOSFET-based technology did not offer the speed Cray needed. Relentless improvements changed things by the mid-1970s, however, and the Cray-1 had been able to use newer ICs and still run at a respectable 12.5 ns (80 MHz). In fact, the Cray-1 was actually somewhat faster than the 8600 because it packed considerably more logic into the system due to the IC's small size.

Although IC design continued to improve, the physical size of the ICs was constrained largely by mechanical limits; the resulting component had to be large enough to solder into a system. Dramatic improvements in density were possible, as the rapid improvement in microprocessor design was showing, but for the type of ICs used by Cray, ones representing a very small part of a complete circuit, the design had plateaued. In order to gain another 10-fold increase in performance over the Cray-1, the goal Cray aimed for, the machine would have to grow more complex. So once again he turned to an 8600-like solution, doubling the clock speed through increased density, adding more of these smaller processors into the basic system, and then attempting to deal with the problem of getting heat out of the machine.

Another design problem was the increasing performance gap between the processor and main memory. In the era of the CDC 6600 memory ran at the same speed as the processor, and the main problem was feeding data into it. Cray solved this by adding ten smaller computers to the system, allowing them to deal with the slower external storage (disks and tapes) and "squirt" data into memory when the main processor was busy. This solution no longer offered any advantages; memory was large enough that entire data sets could be read into it, but the processors ran so much faster than memory that they would often spend long times waiting for data to arrive. Adding four processors simply made this problem worse.

To avoid this problem the new design banked memory and two sets of registers (the B- and T-registers) were replaced with a 16 KWord block of the very fastest memory possible called a *Local Memory,* not a cache, attaching the four *background processors* to it with separate high-speed pipes. This Local Memory was fed data by a dedicated *foreground processor* which was in turn attached to the main memory through a Gbit/s channel per CPU; X-MPs by contrast had 3, for 2 simultaneous loads and a store and Y-MP/C-90s had 5 channels to avoid the von Neumann bottleneck. It was the foreground processor's task to "run" the computer, handling storage and making efficient use of the multiple channels into main memory. It drove the background processors by passing in the instructions they should run via eight 16 word buffers, instead of tying up the existing cache pipes to the background processors. Modern CPUs use a variation of this design as well, although the foreground processor is now referred to as the *load/store unit* and is not a complete machine unto its own.

Main memory banks were arranged in quadrants to be accessed at the same time, allowing programmers to scatter their data across memory to gain higher parallelism. The downside to this approach is that the cost of setting up the *scatter/gather unit* in the foreground processor was fairly high. Stride conflicts corresponding to the number of memory banks suffered a performance penalty (latency)

as occasionally happened in power-of-2 FFT-based algorithms. As the Cray 2 had a much larger memory than Cray 1's or X-MPs, this problem was easily rectified by adding an extra unused element to an array to spread the work out.

2.1.1 Packed circuit boards and new design ideas

Cray-2 models soon settled on a design using large circuit boards packed with ICs. This made them extremely difficult to solder together, and the density was still not enough to reach their performance goals. Teams worked on the design for about two years before even Cray himself "gave up" and decided it would be best if they simply canceled the project and fired everyone working on it. Les Davis, Cray's former design collaborator who had remained at Cray headquarters, decided it should be continued at low priority. After some minor personnel movements the team continued on much as before.

Typical logic module, showing the tight packing. The pogo pins connecting the cards together are the gold-colored rods seen between the ICs.

Six months later Cray had his "eureka" moment. He called the main engineers together for a meeting and presented a new solution to the problem. Instead of making one larger circuit board, each "card" would instead consist of a 3-D stack of eight, connected together in the middle of the boards using pins sticking up from the surface (known as "pogos" or "z-pins"). The cards were packed right on top of each other, so the resulting stack was only about 3 inches high. With this sort of density there was no way any conventional air-cooled system would work; there was too little room for air to flow between the ICs. Instead the system would be immersed in a tank of a new inert liquid from 3M, Fluorinert. The cooling liquid was forced sideways through the modules under pressure, and the flow rate was roughly one inch per second. The heated liquid was cooled using chilled water heat exchangers and returned to the main tank. Work on the new design started in earnest in 1982, several years after the original start date.

While this was going on the Cray X-MP was being developed under the direction of Steve Chen at Cray headquarters, and looked like it would give the Cray-2 a serious run for its money. In order to address this internal threat, as well as a series of newer Japanese Cray-1-like machines, the Cray-2 memory system was dramatically improved, both in size as well as the number of "pipes" into the processors. When the machine was eventually delivered in 1985 the delays had been so long that much of its performance benefits were due to the faster memory. Purchasing the machine really made sense only for users with huge data sets to process.

The first Cray-2 delivered possessed more physical memory (256 MWord) than all previously delivered Cray machines combined. Simulation moved from a 2-D realm or coarse 3-D to a finer 3-D realm because computation did not have to rely on slow virtual memory.

2.2 Uses and successors

The Cray-2 was predominantly developed for the United States Departments of Defense and Energy. Uses tended to be for nuclear weapons research or oceanographic (sonar) development. However, the first Cray-2 (serial number 1) was used at the National Magnetic Fusion Energy Computer Center at Lawrence Livermore National Laboratory for unclassified energy research. It also found its way into civil agencies (such as NASA Ames Research Center), universities, and corporations worldwide. For example, Ford and General Motors both used the Cray-2 for processing complex Finite Element Analysis models of car bodyshells, and for performing virtual crash testing of bodyshell components prior to production.

The Cray-2 would have been superseded by the Cray-3, but due to development problems only a single Cray-3 was built and it was never paid for. The spiritual descendant of the Cray-2 is the Cray X1, offered by Cray.

2.2.1 Comparison to later computers

In 2012, Piotr Luszczek (a former doctoral student of Jack Dongarra), presented results showing that an iPad 2 matched the historical performance of the Cray-2 on an embedded LINPACK benchmark.[1]

2.3 History

Due to the use of liquid cooling, the Cray-2 was given the nickname "Bubbles", and common jokes around the computer made reference to this unique system. Gags included "No Fishing" signs, cardboard depictions of the Loch Ness Monster rising out of the heat exchanger tank, plastic fish inside the exchanger, etc. The power consumption of the Cray-2 was 150 - 200 kW. Each vertical stack of logic modules sat above a stack of power modules which powered 5 volt busbars, each of which delivered about 2200 amps. The Cray-2 was powered by two motor-generators, which took in 480 V three-phase.

2.4 See also

- History of supercomputing

2.5 References

[1] Larabel, Michael (16 September 2012). "Apple iPad 2 As Fast As The Cray-2 Super Computer". Retrieved February 19, 2015.

2.6 External links

- Cray-2 module pictures
- Cray-2 Functional Description Manual
- Cray-2 Brochure

Chapter 3

Cray-3

Seymour Cray poses behind a Cray-3 processor tank.

The **Cray-3** was a vector supercomputer, Seymour Cray's designated successor to the Cray-2. The system was the first major application of gallium arsenide (GaAs) semiconductors in computing, using hundreds of custom built ICs packed into a 1 cubic foot (0.028 m^3) CPU. The design goal was performance around 16 GFLOPS, about 12 times that of the Cray-2.

Work started on the Cray-3 in 1988 at Cray Research's (CRI) development labs in Chippewa Falls, Wisconsin. Other teams at the lab were working on designs with similar performance. To focus the teams, the Cray-3 effort was moved to a new lab in Colorado Springs, Colorado later that year. Shortly thereafter, the corporate headquarters in Minneapolis decided to end work on the Cray-3 in favor of another design, the Cray C90. In 1989 the Cray-3 effort was spun off to a newly formed company, Cray Computer Corporation (CCC).

The launch customer, Lawrence Livermore National Laboratory, cancelled their order in 1991 and a number of company executives left shortly thereafter. The first machine was finally ready in 1993, but with no launch customer, it was instead loaned as a demonstration unit to the nearby National Center for Atmospheric Research in Boulder. The company went bankrupt in May 1995, and the machine was officially decommissioned.

With the delivery of the first Cray-3, Seymour Cray immediately moved on to the similar-but-improved Cray-4 design, but the company went bankrupt before it was completely tested.[1] The Cray-3 was Cray's last completed design; with CCC's bankruptcy he formed SRC Computers to concentrate on parallel designs, but died in a car accident in 1996 before this work was delivered.[2]

3.1 History

3.1.1 Background

Seymour Cray began the design of the Cray-3 in 1985, as soon as the Cray-2 reached production.[3] Cray generally set himself the goal of producing new machines with ten times the performance of the previous models. Although the machines did not always meet this goal, this was a useful technique in defining the project and clarifying what sort of process improvements would be needed to meet it.[4]

Cray had always attacked the problem of increased speed with three simultaneous advances; more execution units to give the system higher parallelism, tighter packaging to decrease signal delays, and faster components to allow for a higher clock speed. Of the three, Cray was normally least aggressive on the last issue, his designs tended to use only components that were already in widespread use, as opposed to leading-edge designs.[4]

For the Cray-3, he decided to set an even higher performance improvement goal, an increase of 12x over the Cray-2.[5] For the Cray-2, he introduced a novel 3D-packaging system for its integrated circuits to allow higher densities,[6] and it appeared that there was some room for improvement in this process. For the new design, he stated that all wires would be limited to a maximum length of 1 foot (0.30 m). This would demand the pro-

cessor be able to fit into a 1 cubic foot (0.028 m^3) block, about $1/3$ that of the Cray-2 CPU. This would not only increase performance, but make the system 27 times smaller.[7]

But for a 12x performance increase, packaging alone would not be enough, the circuits on the chips themselves would also have to speed up. The Cray-2 appeared to be pushing the limits of speed of silicon-based transistors at 4.1 ns (244 MHz), and it did not appear that anything more than another 2x would be possible. If the goal of 12x was to be met, more radical changes would be needed, and a "high tech" approach would have to be used.[8]

Cray had intended to use gallium arsenide circuitry in the Cray-2, which would not only offer much higher switching speeds, but also used less energy and thus ran cooler as well. At the time the Cray-2 was being designed, the state of GaAs manufacturing simply was not up to the task of supplying a supercomputer.[9] By the mid-1980s, things had changed and Cray decided it was the only way forward.[10] Given a lack of investment on the part of large chip makers, Cray decided to invest in a GaAs chip-making startup, GigaBit Logic, and use them as an internal supplier.[11]

Describing the system in November 1988, Cray stated that the 12 times performance increase would be made up of a three times increase due to GaAs circuits, and four times due to the use of more processors. One of the problems with the Cray-2 had been poor multiprocessing performance due to limited bandwidth between the processors, and to address this the Cray-3 would adopt the much faster architecture used in the Cray Y-MP. This would provide a design performance of 8000 MIPS, or 16 GFLOPS.[7]

3.1.2 Development

The Cray-3 was originally slated for delivery in 1991.[12] This was during a time when the supercomputer market was rapidly shrinking from 50% annual growth in 1980, to 10% in 1988.[10] At the same time, Cray Research was also working on the Y-MP, a faster multi-processor version of the system architecture tracing its ancestry to the original Cray-1. In order to focus the Y-MP and Cray-3 groups, and with Cray's personal support,[13] the Cray-3 project moved to a new research center in Colorado Springs.[3]

By 1989 the Y-MP was starting deliveries, and the main CRI lab in Chippewa Falls, Wisconsin, moved on to the C90, a further improvement in the Y-MP series.[14][15] With only 25 Cray-2s sold, management decided that the Cray-3 should be put on "low priority" development. In November 1988, the Colorado Springs lab was spun off as Cray Computer Corporation (CCC), with CRI retaining 10% of the new company's stock and providing a $85 million promissory note to fund development.[3] Cray himself was not a shareholder in the new company, and worked under contract.[16][17] As CRI retained the lease on the original building, the new company had to move once again, introducing further delays.[3][6]

By 1991, development was behind schedule.[18] Development slowed even more when Lawrence Livermore National Laboratory cancelled its order for the first machine,[19] in favor of the C90. Several executives, including the CEO, left the company.[16] The company then announced they would be looking for a customer that needed a smaller version of the machine, with four to eight processors.[20]

The first (and only) production model (serial number S5, named *Graywolf*) was loaned to NCAR as a demonstration system in May 1993. NCAR's version was configured with 4 processors and a 128 MWord (64-bit words, 1 GB) common memory.[21] In service, the static RAM proved to be problematic. It was also discovered that the square root code contained a bug that resulted in 1 in 60 million calculations being wrong. Additionally, one of the four CPUs was not running reliably.[22]

CCC declared bankruptcy in March 1995, after spending about $300 million of financing. NCAR's machine was officially decommissioned the next day.[23] Seven system cabinets, or "tanks", serial numbers S1 to S7, were built for Cray-3 machines. Most were for smaller two-CPU machines. Three of the smaller tanks were used on the Cray-4 project,[24] essentially a Cray-3 with 64 faster CPUs running at 1 ns (1 GHz) and packed into an even smaller space.[25] Another was used for the Cray-3/SSS project.[26]

The failure of the Cray-3 was in large part due to the changing political and technical climate. The machine was being designed during the collapse of the Warsaw Pact and ending of the cold war, which led to a massive downsizing in supercomputer purchases.[20][27] At the same time, the market was increasingly investing in massively parallel (MP or MPP) designs. Cray was critical of this approach, and was quoted by the Wall Street Journal as saying that MPP systems had not yet proven their supremacy over vector computers, noting the difficulty many users have had programming for large parallel machines. "I don't think they'll ever be universally successful, at least not in my lifetime".[27]

3.2 Architecture

3.2.1 Logical design

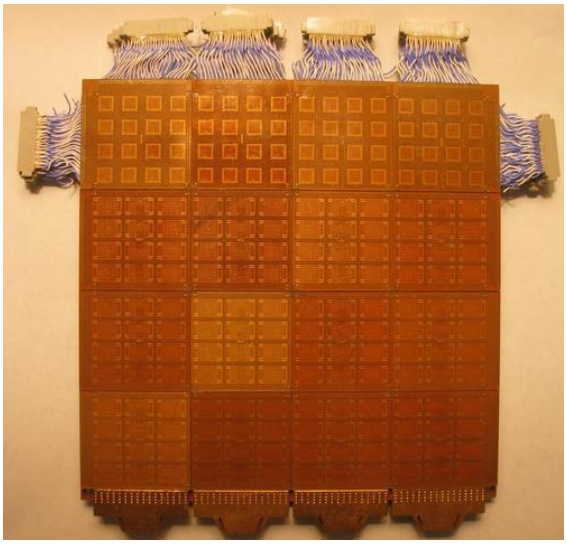
The Cray-3 system architecture comprised a *foreground processing system*, up to 16 *background processors* and up to 2 gigawords (16 GB) of *common memory*. The foreground system was dedicated to input/output and system management. It included a 32-bit processor and four synchronous data channels for mass storage and network de-

vices, primarily via HiPPI channels.[28]

Each background processor consisted of a *computation section*, a *control section* and *local memory*. The computation section performed 64-bit scalar, floating point and vector arithmetic. The control section provided instruction buffers, memory management functions, and a real-time clock. 16 kwords (128 kbytes) of high-speed local memory was incorporated into each background processor for use as temporary scratch memory.[29]

Common memory consisted of silicon CMOS SRAM, organized into *octants* of 64 banks each, with up to eight octants possible. The word size was 64-bits plus eight error-correction bits, and total memory bandwidth was rated at 128 gigabytes per second.[30]

3.2.2 CPU design



Typical module layout, with a 4x4 arrangement of "submodules", stacked 4-deep. The metal connectors on the bottom are power connections.

As with previous designs, the core of the Cray-3 consisted of a number of modules, each containing several circuit boards packed with parts. In order to increase density, the individual GaAs chips were not packaged, and instead several were mounted directly with ultrasonic gold bonding to a board approximately 1 inch square. The boards were then turned over and mated to a second board carrying the electrical wiring, with wires on this card running through holes to the "bottom" (opposite the chips) side of the chip carrier where they were bonded, hence sandwiching the chip between the two layers of board. These *submodules* were then stacked four-deep and, as in the Cray-2, wired to each other to make a 3D circuit.[21]

Unlike the Cray-2, the Cray-3 modules also included edge connectors. Sixteen such submodules were connected together in a 4×4 array to make a single module measuring 121 by 107 by 7 millimetres (4.76 in × 4.21 in × 0.28 in). Even with this advanced packaging the circuit density was low even by 1990s standards, at about 96,000 gates per cubic inch.[31] Modern CPUs offer gate counts of millions per square inch, and the move to 3D circuits was still just being considered as of 2011.[32]

Thirty-two such modules were then stacked and wired together with a mass of twisted-pair wires into a single processor. The basic cycle time was 2.11 ns, or 474 MHz, allowing each processor to reach about 0.948 GFLOPS, and a 16 processor machine a theoretical 15.17 GFLOP. Key to the high performance was the high-speed access to main memory, which allowed each process to burst up to 8 GB/s.[33]

3.2.3 Mechanical design

Complete processor "brick". The modules are visible inside, mounted vertically.

The modules were held together in an aluminum chassis known as a "brick". The bricks were immersed in liquid fluorinert for cooling, as in the Cray-2. A four-processor system with 64 memory modules dissipated about 88 kW of power.[21] The entire four-processor system was about 20 inches (510 mm) tall and front-to-back, and a little over 2 feet (0.61 m) wide.[34]

For systems with up to four processors, the processor assembly sat under a translucent bronzed acrylic cover at the top of a cabinet 42 inches (1.1 m) wide, 28 inches (0.71 m) deep and 50 inches (1.3 m) high,[34] with the memory below it, and then the power supplies and cooling systems on the bottom. Eight and 16-processors system would have been housed in a larger octagonal cabinet. All in all, the Cray-3 was considerably smaller than the Cray-2, itself relatively small compared to other supercomputers.[34]

In addition to the system cabinet, a Cray-3 system also needed one or two (depending on number of processors) *system control pods* (or "C-Pods"), 52.5 inches (1.33 m) square and 55.3 inches (1.40 m) high, containing power

and cooling control equipment.[34]

3.2.4 System configurations

The following possible Cray-3 configurations were officially specified:[35]

3.2.5 Software

The Cray-3 ran the Colorado Springs Operating System (*CSOS*) which was based upon Cray Research's UNICOS operating system version 5.0. A major difference between CSOS and UNICOS was that CSOS was ported to standard C with all PCC extensions that were used in UNICOS removed.[36]

Much of the software available under the Cray-3 was derived from Cray Research and included for instance the X Window System, vectorizing FORTRAN and C compilers, NFS and a TCP/IP stack.[37][36]

3.3 References

3.3.1 Citations

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[2] "Obituary – Seymour Cray, Father of supercomputing". Archived from the original on 2008-05-07.

[3] Trew 2012, p. 245.

[4] MacKenzie 1998, p. 141.

[5] MacKenzie 1998, p. 153.

[6] Readings 2000, p. 10.

[7] Trew 2012, p. 246.

[8] MacKenzie 1998, pp. 153–154.

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[10] MacKenzie 1998, p. 154.

[11] Peltz, James (23 January 1990). "GigaBit Logic Negotiating Sale With Cray Computers". *LA Times*.

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3.4 External links

- Digibarn's Cray-3 Modules
- Cray Research and Cray computers FAQ Part 2
- Cray-2 and −3 instruction sets (archived)

Chapter 4

Cray-4

The **Cray-4** was intended to be Cray Computer Corporation's successor to the failed Cray-3 supercomputer. It was marketed to compete with the T90 from Cray Research.[1] CCC went bankrupt in 1995 before any Cray-4 had been delivered.

4.1 Design

The earlier Cray-3 was the first major application of gallium arsenide (GaAs) semiconductors in computing. It was not considered a success, and only one Cray-3 was delivered. Seymour Cray moved on to the Cray-4 design, announcing the design in 1994.

The Cray-4 was essentially a shrunk and sped-up version of the Cray-3, and it consisted of a number of vector processors attached to a fast memory. The Cray-3 supported from four to sixteen processors running at 474 MHz, while the Cray-4 scaled from four to sixty-four processors running at 1 GHz.[2] The final packaging for the Cray-4 was intended to fit into 1-cubic-foot (0.028 m^3), and was to be tested in the smaller one-CPU "tanks" from the Cray-3. A "midrange" system included 16 processors, 1,024 megawords (8192 MB) of memory and provided 32 gigaflops for $11 million.[3]

The local memory architecture used on the Cray-2 and Cray-3 was dropped, returning to the mass of B- and T-registers on earlier designs, owing to Seymour's lack of success using the local memory effectively.

4.2 1994

"Significant technical progress was made during 1994 on the CRAY-4, which takes advantage of technologies and manufacturing processes developed during the design and manufacture of the CRAY-3. The Company announced introduction of the CRAY-4 to the market on November 10, 1994. Several single processor CRAY-4 prototype systems, each with 64 megawords of memory, were undergoing diagnostic testing prior to the Company filing for bankruptcy. The Company began testing individual CRAY-4 modules at the start of 1994 and planned to be able to deliver a 4-processor CRAY-4 prototype system by approximately the end of the second quarter of 1995. Upon filing of bankruptcy, the Company stopped work on the CRAY-4." [4]

4.3 Legacy

The processor with serial number 001 sold at auction for $37,500 on 22 September 2015. Manufactured in 1995 it is believed to be the only one in existence.[5] Parts of CPU prototypes exist. Marketing brochures also exist.

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4.5 External links

Chapter 5

Cray

This article is about the supercomputer brand. For other uses, see Cray (disambiguation).

Cray Inc. is an American supercomputer manufacturer headquartered in Seattle, Washington.[1] It also manufactures systems for data storage and analytics.[4] Several Cray supercomputer systems are listed in the TOP500, which ranks the most powerful supercomputers in the world.[5] The number of Cray systems on the list varies from year to year.

Cray manufactures its products in Chippewa Falls, Wisconsin, where its founder, Seymour Cray, was born and raised. The company also has offices in St. Paul, Minnesota (the site of its original headquarters under Seymour Cray), and numerous other sales, service, engineering, and R&D locations around the world.[6][7]

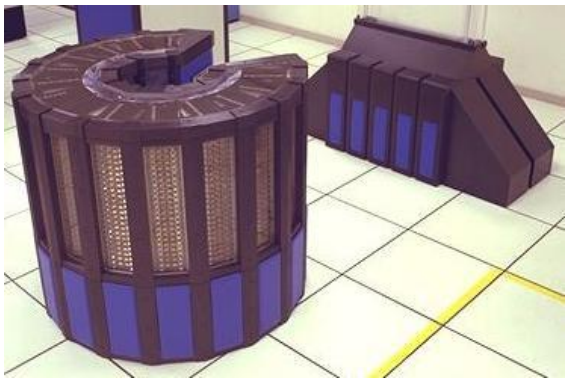
The company's predecessor, **Cray Research**, Inc. (CRI), was founded in 1972 by computer designer Seymour Cray.[8] Seymour Cray went on to form the spin-off **Cray Computer Corporation** (CCC), in 1989, which went bankrupt in 1995, while Cray Research was bought by SGI the next year. Cray Inc. was formed in 2000 when Tera Computer Company purchased the Cray Research Inc. business from SGI and adopted the name of its acquisition.[9]

5.1 Company history

5.1.1 Background: 1950 to 1972

Seymour Cray began working in the computing field in 1950 when he joined Engineering Research Associates (ERA) in Saint Paul, Minnesota. There, he helped to create the ERA 1103. ERA eventually became part of UNIVAC, and began to be phased out. He left the company in 1960, a few years after former ERA employees set up Control Data Corporation (CDC). He initially worked out of the CDC headquarters in Minneapolis, but grew upset by constant interruptions by managers. He eventually set up a lab at his home town in Chippewa Falls, Wisconsin, about 85 miles to the east. Cray had a string of successes at CDC, including the CDC 6600 and CDC 7600.

5.1.2 Cray Research Inc. and Cray Computer Corporation: 1972 to 1996



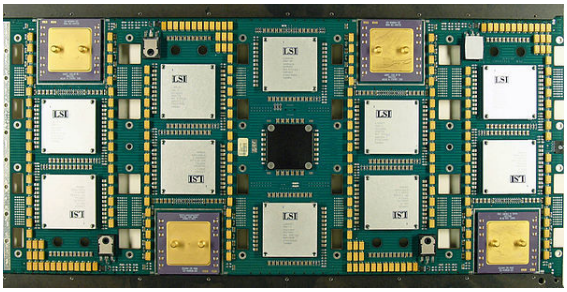
Cray-2 supercomputer

When CDC ran into financial difficulties in the late 1960s, development funds for his follow-on CDC 8600 became scarce, and when he was told the project would have to be put "on hold" in 1972, Cray left to form his own company, **Cray Research Inc.** Copying the previous arrangement, Cray kept the research and development facilities in Chippewa Falls, and the business headquarters in Minneapolis. The company's first product, the Cray-1 supercomputer, was a major success because it was faster than all other computers at the time. The first system was sold within a month for US$8.8 million. Seymour Cray continued working, this time on the Cray-2, though it only ended up being marginally faster than the Cray X-MP, developed by another team at the company.

Cray soon left the CEO position to become an independent contractor. He started a new VLSI technology lab for the Cray-2 in Boulder, Colorado, **Cray Laboratories**, in 1979, which closed in 1982; undaunted, Cray later headed a similar spin-off in 1989, **Cray Computer Corporation** (CCC) in Colorado Springs, where he worked on the Cray-3 project—the first attempt at major use of gallium arsenide (GaAs) semiconductors in computing. However, the changing political climate (collapse of the Warsaw Pact and the end of the Cold War) resulted in

poor sales prospects. Ultimately, only one Cray-3 was delivered, and a number of follow-on designs were never completed. The company filed for bankruptcy in 1995. CCC's remains then began Cray's final corporation, SRC Computers, Inc. which still exists.

Cray Research continued development along a separate line of computers, originally with lead designer Steve Chen and the Cray X-MP. After Chen's departure, the Cray Y-MP, Cray C90 and Cray T90 were developed on the original Cray-1 architecture but achieved much greater performance via multiple additional processors, faster clocks, and wider vector pipes. The uncertainty of the Cray-2 project gave rise to a number of Cray-object-code compatible "Crayette" firms: Scientific Computer Systems (SCS), American Supercomputer, Supertek, and perhaps one other firm. These firms did not mean to compete against Cray and therefore attempted less expensive, slower CMOS versions of the X-MP with the release of the COS operating system (SCS) and the CFT Fortran compiler; they also considered National labs (LANL/LLNL) developed CTSS operating system as well before caving in to the tide of Unixes.



Cray T3E processor board

A series of massively parallel computers from Thinking Machines, Kendall Square Research, Intel Supercomputing Systems Division, nCUBE, MasPar and Meiko Scientific took over the 1980s high performance market. At first, Cray Research denigrated such approaches by complaining that developing software to effectively use the machines was difficult – a true complaint in the era of the ILLIAC IV, but becoming less so each day. Cray eventually realized that the approach was likely the only way forward and started a five-year project to capture the lead in this area: the plan's result was the DEC Alpha-based Cray T3D and Cray T3E series, which left Cray as the only remaining supercomputer vendor in the market besides NEC by 2000.

Most sites with a Cray installation were considered a member of the "exclusive club" of Cray operators. Cray computers were considered quite prestigious because Crays were extremely expensive machines, and the number of units sold was small compared to ordinary mainframes. This perception extended to countries as well: to boost the perception of exclusivity, Cray Research's marketing department had promotional neckties made with a mosaic of tiny national flags illustrating the "club of Cray-operating countries".(Computer History Museum, Cray 1 30th Anniversary recorded presentation, 2006)

New vendors introduced small supercomputers, known as minisupercomputers (as opposed to superminis) during the late 1980s and early 1990s, which out-competed low-end Cray machines in the market. The Convex Computer series, as well as a number of small-scale parallel machines from companies like Pyramid Technology and Alliant Computer Systems were particularly popular. One such vendor was Supertek, whose S-1 machine was an air-cooled CMOS implementation of the X-MP processor. Cray purchased Supertek in 1990 and sold the S-1 as the Cray XMS, but the machine proved problematic; meanwhile, their not-yet-completed S-2, a Y-MP clone, was later offered as the Cray Y-MP EL (later becoming the EL90 series) which started to sell in reasonable numbers in 1991-92—to mostly smaller companies, notably in the oil exploration business. This line evolved into the Cray J90 and eventually the Cray SV1 in 1998.

In December 1991, Cray purchased some of the assets of Floating Point Systems, another minisuper vendor that had moved into the file server market with its SPARC-based Model 500 line.[10] These SMP machines scaled up to 64 processors and ran a modified version of Sun Microsystems' Solaris. Cray set up **Cray Research Superservers, Inc.** (later the **Business Systems Division**) to sell this system as the Cray S-MP, later replacing it with the Cray CS6400. In spite of these machines being some of the most powerful available when applied to appropriate workloads, Cray was never very successful in this market, possibly due to it being so foreign to their existing market niche.

CCC was building the Cray-3/SSS when it went into Chapter 11 in March 1995.

5.1.3 Silicon Graphics: 1996 to 2000

Cray Research merged with Silicon Graphics (SGI) in February 1996. At the time the industry was highly critical of the move, noting that there was little overlap between the two companies, either in markets or technology. Founder Seymour Cray died as a result of a traffic accident later that year.

SGI immediately sold off the Superservers business to Sun, who quickly turned the UltraSPARC-based *Starfire* project then under development into the extremely successful Enterprise 10000 range of servers.

SGI did use a number of Cray technologies in their attempt to move from the graphics workstation market into supercomputing. Key among these was the use of the Cray-developed HIPPI data-bus and details of the interconnects used in the T3 series.

SGI's long-term strategy was to merge their high-end server line with Cray's product lines in two phases, code-

named *SN1* and *SN2* (SN standing for "Scalable Node"). The SN1 was intended to replace the T3E and SGI Origin 2000 systems and later became the *SN-MIPS* or SGI Origin 3000 architecture. The SN2 was originally intended to unify all high-end/supercomputer product lines including the T90 into a single architecture. This goal was never achieved before SGI divested itself of the Cray business, and the SN2 name was later associated with the *SN-IA* or SGI Altix 3000 architecture.

Under SGI ownership, one new Cray model line, the SV1, was launched in 1998. This was a clustered SMP vector processor architecture, developed from J90 technology.

SGI set up a separate Cray Research Business Unit in August 1999 in preparation for detachment. On March 2, 2000, the unit was sold to Tera Computer Company. Tera Computer Company was then renamed Cray Inc. when the deal closed on April 4.

5.1.4 Cray Inc.: 2000 to present

Cray-designed HLRN-III Konrad *at Zuse Institute Berlin, 2014*

After the Tera merger, the Tera MTA system was relaunched as the Cray MTA-2. This was not a commercial success and shipped to only two customers. Cray Inc. also unsuccessfully badged the NEC SX-6 supercomputer as the Cray SX-6 and acquired exclusive rights to sell the SX-6 in the U.S., Canada and Mexico.

In 2002, Cray Inc. announced their first new model, the Cray X1 combined architecture vector / MPP supercomputer. Previously known as the *SV2*, the X1 is the end result of the earlier *SN2* concept originated during the SGI years. In May 2004, Cray was announced to be one of the partners in the U.S. Department of Energy's fastest-computer-in-the-world project to build a 50 teraflops machine for the Oak Ridge National Laboratory. Cray was sued in 2002 by Isothermal Systems Research for patent infringement. The suit claimed that Cray used ISR's patented technology in the development of the Cray X1.[11] The lawsuit was settled in 2003.[12] As of November 2004, the Cray X1 had a maximum measured performance of 5.9 teraflops, being the 29th fastest supercomputer in the world. Since then the X1 has been superseded by the X1E, with faster dual-core processors.

On October 4, 2004, the company announced the Cray XD1 range of entry-level supercomputers which use dual-core 64-bit AMD Opteron CPUs running Linux. This system was previously known as the OctigaBay 12K before Cray's acquisition of that company. The XD1 provided one Xilinx Virtex II Pro field-programmable gate array (FPGA) with each node of four Opteron processors. The FPGAs could be configured to embody various digital hardware designs and could augment the processing or input/output capabilities of the Opteron processors. Furthermore, each FPGA contains a pair of PowerPC 405 processors which can add to the already considerable power of a single node. The Cray XD1, although moderately successful, was eventually discontinued.

In 2004, Cray completed the Red Storm system for Sandia National Laboratories. Red Storm was to become the jumping-off point for a string of successful products that eventually revitalized Cray in supercomputing. Red Storm had processors clustered in 96 unit cabinets, a theoretical maximum of 300 cabinets in a machine, and a design speed of 41.5 teraflops. Red Storm also included an innovative new design for network interconnects, which was dubbed SeaStar and destined to be the centerpiece of succeeding innovations by Cray. The Cray XT3 massively parallel supercomputer became a commercialized version of Red Storm, similar in many respects to the earlier T3E architecture, but, like the XD1, using AMD Opteron processors. The Cray XT4, introduced in 2006 added support for DDR2 memory, newer dual-core and future quad-core Opteron processors and utilized a second generation SeaStar2 communication coprocessor. It also included an option for FPGA chips to be plugged directly into processor sockets, unlike the Cray XD1, which required a dedicated socket for the FPGA coprocessor.[13]

On August 8, 2005, Peter Ungaro was appointed CEO,[14] Ungaro had joined Cray in August 2003 as Vice President of Sales and Marketing[15] and had been made Cray's President in March 2005.

On November 13, 2006, Cray announced a new system, the Cray XMT, based on the MTA series of machines.[16][17] This system combined multi-threaded processors, as used on the original Tera systems, and the SeaStar2 interconnect used by the XT4. By reusing ASICs, boards, cabinets, and system software used by the comparatively higher volume XT4 product, the cost of making the very specialized MTA system can be reduced. A second generation of the XMT is scheduled for release in 2011, with the first system ordered by the Swiss National Supercomputing Center (CSCS).[18]

In 2006, Cray announced a vision of products dubbed 'Adaptive Supercomputing'.[19] The first generation of such systems, dubbed the *Rainier Project*, used a common interconnect network (SeaStar2), programming environment, cabinet design, and I/O subsystem. These systems included the existing XT4 and the XMT. The second generation, launched as the XT5h, allowed a system to combine compute elements of various types into a common system, sharing infrastructure. The XT5h combined Opteron, vector, multithreaded, and FPGA compute processors in a single system.

In April 2008, Cray and Intel announced they would collaborate on future supercomputer systems. This partnership produced the Cray CX1 system, launched in September the same year. This was a deskside blade server system, comprising up to 16 dual- or quad-core Intel Xeon processors, with either Microsoft Windows HPC Server 2008 or Red Hat Enterprise Linux installed. In early 2010, Cray also introduced the Cray CX1000, a rack-mounted system with a choice of compute-based, GPU-based, or SMP-based chassis. The CX1 and CX1000 product lines were sold until late 2011.

By 2009, the largest computer system Cray had delivered was the XT5 system at National Center for Computational Sciences at Oak Ridge National Laboratories.[20] This system, with over 224,000 processing cores, was dubbed *Jaguar* and was the fastest computer in the world as measured by the LINPACK benchmark[21] at the speed of 1.75 petaflops[22] until being surpassed by the Tianhe-1A in October 2010. It was the first system to exceed a sustained performance of 1 petaflops on a 64-bit scientific application.

In May 2010, the Cray XE6 supercomputer was announced. The Cray XE6 system had at its core the new Gemini system interconnect. This new interconnect included a true global-address space represented a return to the T3E feature set that had been so successful with Cray Research. This product was a successful follow-on the XT3,XT4 and XT5 products. The first multi-cabinet XE6 system was shipped in July 2010. The next generation *Cascade*[23] systems were designed make use of future multicore and/or manycore processors from vendors such as Intel and NVIDIA. Cascade was scheduled to be introduced in early 2013 and designed to use the next-generation network chip and follow-on to Gemini, code named *Aries*.

In 2011, Cray announced the Cray XK6 hybrid supercomputer. The Cray XK6 system, capable of scaling to 500,000 processors and 50 petaflops of peak performance, combines Cray's Gemini interconnect, AMD's multi-core scalar processors, and NVIDIA's Tesla GPGPU processors. In October 2012 Cray announced the Cray XK7 which supports the NVIDIA Kepler GPGPU and announced that the ORNL Jaguar system would be upgraded to an XK7 (renamed *Titan*) and capable of over 20 petaflops.[24] Titan was the world's fastest supercomputer as measured by the LINPACK benchmark[25] until the introduction of the Tianhe-2 in 2013, which is substantially faster. In 2011 Cray also announced it had been awarded the $188M US Blue Waters contract with the University of Illinois, after IBM had pulled out of the delivery.[26] This system was delivered in 2012 and was the largest system to date, in terms of cabinets and general-purpose x86 processors, that Cray had ever delivered.

In November 2011, the Cray Sonexion 1300 Data Storage System was introduced and signaled Cray entry into the high performance storage business. This product used modular technology and a Lustre file system.

In April 2012, Cray Inc. announced the sale of its interconnect hardware development program and related intellectual property to Intel Corporation for $140 million.[27][28]

On November 9, 2012, Cray announced the acquisition of Appro International, Inc., a California-based privately held developer of advanced scalable supercomputing solutions.[29] Currently the #3 provider on the Top100 supercomputer list, Appro builds some of the world's most advanced high performance computing (HPC) cluster systems.

On November 1, 2013, Cray announced the acquisition of the Gnodal IP and team in Europe.[30][31]

5.2 References

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5.4 External links

- Official website
- Cray SEC Filings
- Cray Manuals Library @ Computing History
- Cray Manuals at bitsavers.org
- Historic Cray Research Marketing Materials at the Computer History Museum
- Top 500 Supercomputers
- Fred Gannett's Cray Supercomputer FAQ
- DigiBarn Computer Museum: Cray Supercomputers and Memorabilia
- Cray headquarters is at coordinates 47°36′22″N 122°19′55″W / 47.6060°N 122.3320°W

Chapter 6

Seymour Cray

Seymour Roger Cray (September 28, 1925[1] – October 5, 1996[2]) was an American electrical engineer and supercomputer architect who designed a series of computers that were the fastest in the world for decades, and founded Cray Research which built many of these machines. Called "the father of supercomputing,"[2] Cray has been credited with creating the supercomputer industry.[3] Joel S. Birnbaum, then chief technology officer of Hewlett-Packard, said of him: "It seems impossible to exaggerate the effect he had on the industry; many of the things that high performance computers now do routinely were at the farthest edge of credibility when Seymour envisioned them."[4]

6.1 Early life

Cray was born in 1925 in Chippewa Falls, Wisconsin, to Seymour R. and Lillian Cray. His father was a civil engineer who fostered Cray's interest in science and engineering. As early as the age of ten he was able to build a device out of Erector Set components that converted punched paper tape into Morse code signals. The basement of the family home was given over to the young Cray as a "laboratory".[5]

Cray graduated from Chippewa Falls High School in 1943 before being drafted for World War II as a radio operator. He saw action in Europe, and then moved to the Pacific theatre where he worked on breaking Japanese naval codes. On his return to the United States he received a B.Sc. in Electrical Engineering at the University of Minnesota, graduating in 1949, followed by a M.Sc. in applied mathematics in 1951.[6]

6.2 Career

6.2.1 Engineering Research Associates

In 1951, Cray joined Engineering Research Associates (ERA) in Saint Paul, Minnesota.[7] ERA had formed out of a former United States Navy laboratory that had built codebreaking machines, a tradition ERA carried on when such work was available. ERA was introduced to computer technology during one such effort, but in other times had worked on a wide variety of basic engineering as well.

Cray quickly came to be regarded as an expert on digital computer technology, especially following his design work on the ERA 1103, the first commercially successful scientific computer. His work with super computers won him the nickname "The Wizard of Chippewa Falls".[7] He remained at ERA when it was bought by Remington Rand and then Sperry Corporation in the early 1950s. At the newly formed Sperry-Rand, ERA became the "scientific computing" arm of their UNIVAC division.

6.2.2 Control Data Corporation

When the scientific computing division was phased out in 1957, a number of employees left to form Control Data Corporation (CDC). Cray wanted to follow immediately, but CDC's CEO, William Norris, refused, as Cray was in the midst of completing a project for the Navy, with whom Norris was interested in maintaining a good relationship. The project, the Naval Tactical Data System, was completed early the next year, whereupon Cray left for CDC as well.

By 1960 he had completed the design of the CDC 1604, an improved low-cost ERA 1103 that had impressive performance for its price range. Even as the CDC 1604 was starting to ship to customers in 1960, Cray had already moved on to designing other computers. He first worked on the design of an upgraded version (the CDC 3000 series), but company management wanted these machines targeted toward 'business and commercial' data processing for average customers. Cray did not enjoy working on such 'mundane' machines, constrained to design for low-cost construction, so CDC could sell lots of them. His desire was to *"produce the largest [fastest] computer in the world"*. So after some basic design work on the CDC 3000 series, he turned that over to others and went on to work on the CDC 6600. (But several unique features of the 6600 first start to appear in the 3000 series.)

Although in terms of hardware the 6600 was not on the leading edge, Cray invested considerable effort into the

design of the machine in an attempt to enable it to run as fast as possible. Unlike most high-end projects, Cray realized that there was considerably more to performance than simple processor speed, that I/O bandwidth had to be maximized as well in order to avoid "starving" the processor of data to crunch. As he later noted, *Anyone can build a fast CPU. The trick is to build a fast system.*[7]

The 6600 was the first commercial supercomputer, outperforming everything then available by a wide margin. While expensive, for those that needed the absolutely fastest computer available there was nothing else on the market that could compete. When other companies (namely IBM) attempted to create machines with similar performance, they stumbled (Stretch/IBM 7030). Indeed, the 6600 solved a critical design problem — "imprecise interrupts"[8] — that was largely responsible for IBM's failure. He did this by replacing I/O interrupts with a polled request issued by one of 10 so-called peripheral processors, which were built-in mini-computers that did all transfers in and out of the 6600's central memory. He then further increased the challenge in the later release the 5-fold faster CDC 7600.

In 1963, in a *Business Week* article announcing the CDC 6600, Seymour Cray clearly expressed an idea that is often misattributed to Herb Grosch as so-called Grosch's law:

> Computers should obey a square law -- when the price doubles, you should get at least four times as much speed.[9]

CDC's Chippewa Falls laboratory

During this period Cray had become increasingly annoyed at what he saw as interference from CDC management. Cray always demanded an absolutely quiet work environment with a minimum of management overhead, but as the company grew he found himself constantly interrupted by middle managers who — according to Cray — did little but gawk and use him as a sales tool by introducing him to prospective customers.

Cray decided that in order to continue development he would have to move from St. Paul, far enough that it would be too long a drive for a "quick visit" and long distance telephone charges would be just enough to deter most calls, yet close enough that real visits or board meetings could be attended without too much difficulty. After some debate, Norris backed him and set up a new laboratory on land Cray owned in his hometown of Chippewa Falls. Some of the reason for the move may also have to do with Cray's worries about an impending nuclear war, which he felt made Minneapolis a serious safety concern. His house, built a few hundred yards from the new CDC laboratory, included a huge bomb shelter.

The new Chippewa Lab was set up in the middle of the 6600 project, although it does not seem to have delayed the project. After the 6600 shipped, the successor CDC 7600 system was the next product to be developed in Chippewa Falls, offering peak computational speeds of ten times the 6600. The failed follow-on to the 7600, the CDC 8600, was the project that finally ended his run of successes at CDC in 1972.

Although the 6600 and 7600 had been huge successes in the end, both projects had almost bankrupted the company while they were being designed. The 8600 was running into similar difficulties and Cray eventually decided that the only solution was to start over fresh. This time Norris was not willing to take the risk, and another project within the company, the CDC STAR-100 seemed to be progressing more smoothly. Norris said he was willing to keep the project alive at a low level until the STAR was delivered, at which point full funding could be put into the 8600. Cray was unwilling to work under these conditions and left the company.

6.2.3 Cray Research

With a Cray-1

The split was fairly amicable, and when he started Cray Research in a new laboratory on the same Chippewa property a year later, Norris invested $300,000 in start-up money. Like CDC's organization, Cray R&D was based in Chippewa Falls and business headquarters were in Minneapolis. Unlike CDC, Cray's manufacturing was also in Chippewa Falls.

At first there was some question as to what exactly the new company should do. It did not seem that there would be any way for them to afford to develop a new computer, given that the now-large CDC had been unable to support more than one. When the President in charge of financing traveled to Wall Street to look for seed capital, he was surprised to find that Cray's reputation was very well known. Far from struggling for some role to play in the market, the financial world was more than willing to provide Cray with all the money they would need to develop a new machine.

After several years of development, their first product was released in 1976 as the Cray-1. As with earlier Cray de-

signs, the Cray-1 made sure that the *entire* computer was fast, as opposed to just the processor. When it was released it easily beat almost every machine in terms of speed, including the STAR-100 that had beaten the 8600 for funding. The only machine able to perform on the same sort of level was the ILLIAC IV, a specialized one-off machine that rarely operated near its maximum performance, except on very specific tasks. In general, the Cray-1 beat anything on the market by a wide margin.

Serial number 001 was "lent" to Los Alamos in 1976, and that summer the first full system was sold to the National Center for Atmospheric Research for $8.8 million. The company's early estimates had suggested that they might sell a dozen such machines, based on sales of similar machines from the CDC era, so the price was set accordingly. Eventually, well over 80 Cray-1s were sold, and the company was a huge success financially.

Follow-up success was not so easy. While he worked on the Cray-2, other teams delivered the two-processor Cray X-MP, which was another huge success and later the four-processor X-MP. When the Cray-2 was finally released after six years of development it was only marginally faster than the X-MP, largely due to very fast and large main memory, and thus sold in much smaller numbers. The Cray-2 ran at 250 MHz with a very deep pipeline, making it harder to code for than the shorter pipe X-MP.

As the Cray-3 project started, he found himself once again being "bothered" too much with day-to-day tasks. In order to concentrate on design, Cray left the CEO position of Cray Research in 1980 to become an independent contractor. In 1988 he moved the Cray 3 project from Chippewa Falls to a laboratory in Colorado Springs, Colorado.

In 1989, Cray was faced with a repeat of history when the Cray-3 started to run into difficulties. An upgrade of the X-MP using high-speed memory from the Cray-2 was under development and seemed to be making real progress, and once again management was faced with two projects and limited budgets. They eventually decided to take the safer route, releasing the new design as the Cray Y-MP.

6.2.4 Cray Computer Corporation

Cray decided to spin off the Colorado Springs laboratory to form **Cray Computer Corporation**. This new entity took the Cray-3 project with them.

The 500 MHz Cray-3 proved to be Cray's second major failure. In order to provide the tenfold increase in performance that he always demanded of his newest machines, Cray decided that the machine would have to be built using gallium arsenide semiconductors. In the past Cray had always avoided using anything even near the state of the art, preferring to use well-known solutions and designing a fast machine based on them. In this case, Cray was developing every part of the machine, even the chips inside it.

Nevertheless, the team was able to get the machine working and installed their first example at NCAR. The machine was still essentially a prototype, and the company was using the installation to debug the design. By this time a number of massively parallel machines were coming into the market at price/performance ratios the Cray-3 could not touch. Cray responded through "brute force", starting design of the Cray-4 which would run at 1 GHz and outpower these machines, regardless of price.

In 1995 there had been no further sales of the Cray-3, and the ending of the Cold War made it unlikely anyone would buy enough Cray-4s to offer a return on the development funds. The company ran out of money and filed for Chapter 11 bankruptcy March 24, 1995.

6.2.5 SRC Computers

Cray had always resisted the massively parallel solution to high-speed computing, offering a variety of reasons that it would never work as well as one very fast processor. He famously quipped "If you were plowing a field, which would you rather use: Two strong oxen or 1024 chickens?" By the mid-1990s this argument was becoming increasingly difficult to justify, and modern compiler technology made developing programs on such machines not much more difficult than their simpler counterparts.

Cray set up a new company, **SRC Computers**, and started the design of his own massively parallel machine. The new design concentrated on communications and memory performance, the bottleneck that hampered many parallel designs. Design had just started when Cray died suddenly as a result of a car accident. SRC Computers carried on development and now specializes in reconfigurable computing.

6.3 Technical approaches

Cray frequently cited two important aspects to his design philosophy: remove heat, and ensure that all signals that are supposed to arrive somewhere at the same time do indeed arrive at the same time.[10]

His computers were equipped with built-in cooling systems, extending ultimately to coolant channels cast into the mainframes and thermally coupled to metal plates within the circuit boards, and to systems immersed in coolants. In a story he told about himself, he realized early in his career that he should interlock the computers with the cooling systems so that the computers would not operate unless the cooling systems were operational. It did not originally occur to him to interlock in the other direction until a customer reported that localized power outages had shut down their computer, but left the cool-

ing system running — so they arrived in the morning to find the machine encased in ice.

Cray addressed the problem of skew by ensuring that every signal path in his later computers was the same electrical length, so that values that were to be acted upon at a particular time were indeed all valid values. When required, he would run the traces back and forth on the circuit boards until the desired length was achieved, and he employed Maxwell's equations in design of the boards to ensure that any radio frequency effects which altered the signal velocity and hence the electrical path length were accounted for.

When asked what kind of CAD tools he used for the Cray-1, Cray said that he liked #3 pencils with quad paper pads. Cray recommended using the backs of the pages so that the lines were not so dominant. When he was told that Apple Computer had just bought a Cray to help design the next Apple Macintosh, Cray commented that he had just bought a Macintosh to design the next Cray.[11]

6.4 Personal life

Cray avoided publicity, and there are a number of unusual tales about his life away from work (termed "Rollwagenisms", from then-CEO of Cray Research, John A. Rollwagen). He enjoyed skiing, wind surfing, tennis, and other sports. Another favorite pastime was digging a tunnel under his home; he attributed the secret of his success to "visits by elves" while he worked in the tunnel: "While I'm digging in the tunnel, the elves will often come to me with solutions to my problem."[12][13]

Cray died on October 5, 1996, two weeks after his car was struck on the highway and rolled several times.[14][15]

The IEEE Computer Society's Seymour Cray Computer Engineering Award,[16] established in late 1997, recognizes innovative contributions to high performance computing systems exemplifying Cray's creative spirit.

6.5 See also

- Charles Babbage Institute
- Cray-3/SSS
- John Vincent Atanasoff

6.6 Notes

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6.8 External links

- Seymour Cray Oral History
- Quotations related to Seymour Cray at Wikiquote

- An Imaginary Tour of a Biological Computer (Why Computer Professionals and Molecular Biologists Should Start Collaborating): Remarks of Seymour Cray to the Shannon Center for Advanced Studies, University of Virginia, May 30, 1996

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