1. Description

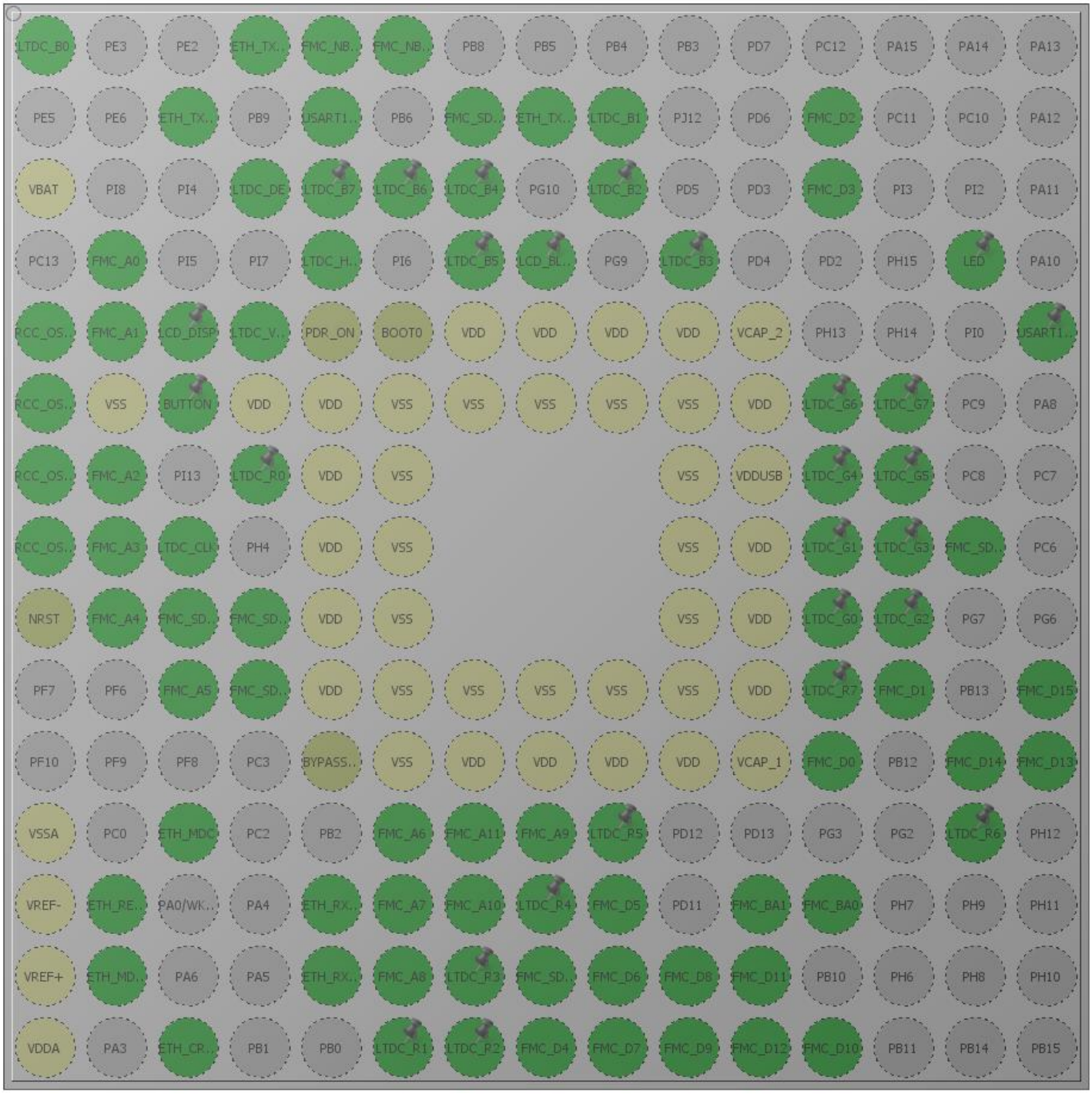
1.1. Project

Project Name	LCD_LwIP
Board Name	STM32F746G-DISCO
Generated with:	STM32CubeMX 4.27.0
Date	12/10/2018

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



STM32F746NGHx
TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	LTDC_B0	
A4	PG14	I/O	ETH_TXD1	
A5	PE1	I/O	FMC_NBL1	
A6	PE0	I/O	FMC_NBL0	
B3	PG13	I/O	ETH_TXD0	
B5	PB7	I/O	USART1_RX	
B7	PG15	I/O	FMC_SDNCAS	
B8	PG11	I/O	ETH_TX_EN	
B9	PJ13	I/O	LTDC_B1	
B12	PD0	I/O	FMC_D2	
C1	VBAT	Power		
C4	PK7	I/O	LTDC_DE	
C5	PK6	I/O	LTDC_B7	
C6	PK5	I/O	LTDC_B6	
C7	PG12	I/O	LTDC_B4	
C9	PJ14	I/O	LTDC_B2	
C12	PD1	I/O	FMC_D3	
D2	PF0	I/O	FMC_A0	
D5	PI10	I/O	LTDC_HSYNC	
D7	PK4	I/O	LTDC_B5	
D8	PK3 *	I/O	GPIO_Output	LCD_BL_CTRL
D10	PJ15	I/O	LTDC_B3	
D14	PI1 *	I/O	GPIO_Output	LED
E1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
E2	PF1	I/O	FMC_A1	
E3	PI12 *	I/O	GPIO_Output	LCD_DISP
E4	PI9	I/O	LTDC_VSYNC	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E15	PA9	I/O	USART1_TX	
F1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	

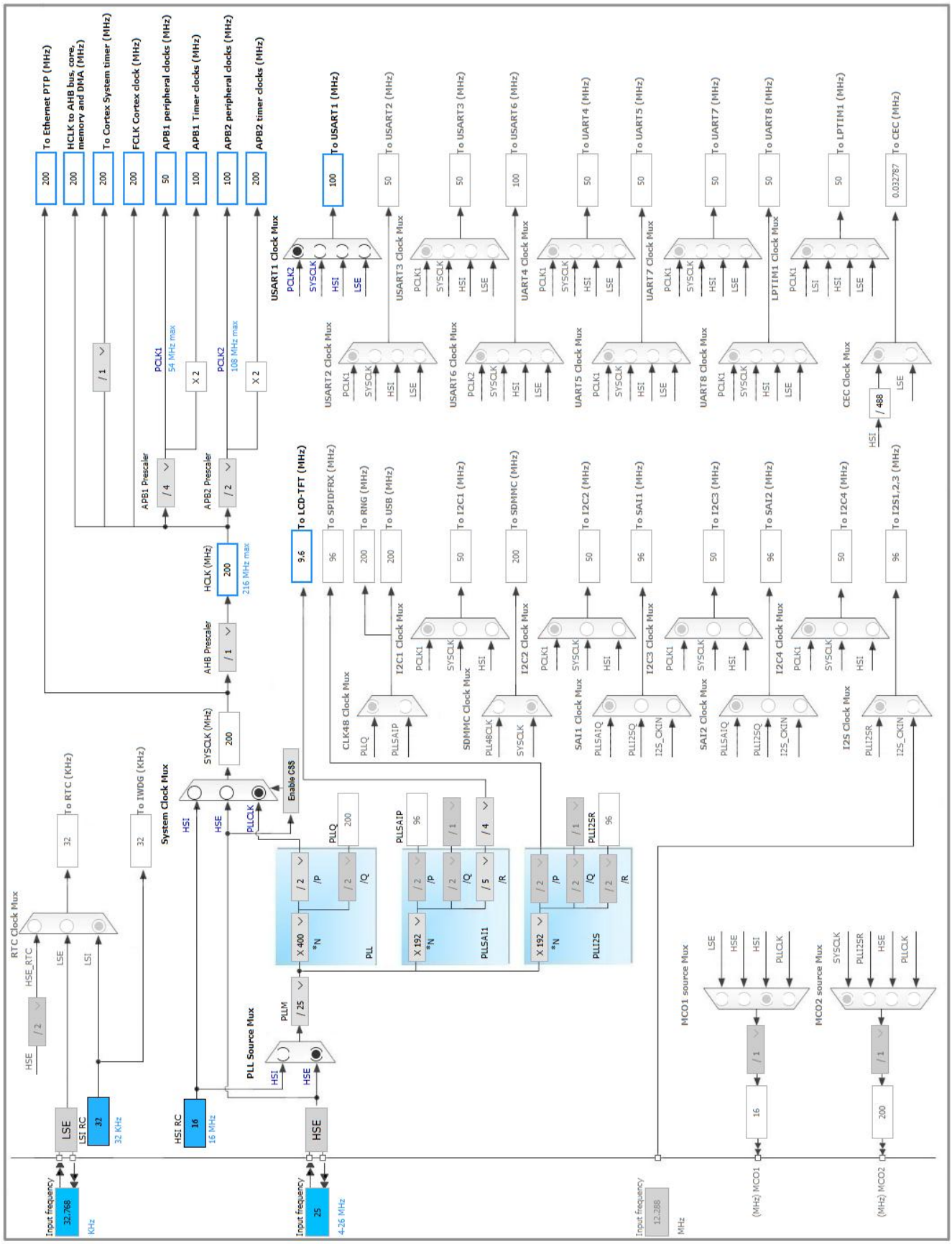
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F2	VSS	Power		
F3	PI11 *	I/O	GPIO_Input	BUTTON
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	PK1	I/O	LTDC_G6	
F13	PK2	I/O	LTDC_G7	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	PF2	I/O	FMC_A2	
G4	PI15	I/O	LTDC_R0	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	PJ11	I/O	LTDC_G4	
G13	PK0	I/O	LTDC_G5	
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	
H3	PI14	I/O	LTDC_CLK	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
H12	PJ8	I/O	LTDC_G1	
H13	PJ10	I/O	LTDC_G3	
H14	PG8	I/O	FMC_SDCLK	
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	
J3	PH5	I/O	FMC_SDNWE	
J4	PH3	I/O	FMC_SDNE0	
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J12	PJ7	I/O	LTDC_G0	
J13	PJ9	I/O	LTDC_G2	
K3	PF5	I/O	FMC_A5	
K4	PH2	I/O	FMC_SDCKE0	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	PJ6	I/O	LTDC_R7	
K13	PD15	I/O	FMC_D1	
K15	PD10	I/O	FMC_D15	
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	
L14	PD9	I/O	FMC_D14	
L15	PD8	I/O	FMC_D13	
M1	VSSA	Power		
M3	PC1	I/O	ETH_MDC	
M6	PF12	I/O	FMC_A6	
M7	PG1	I/O	FMC_A11	
M8	PF15	I/O	FMC_A9	
M9	PJ4	I/O	LTDC_R5	
M14	PJ5	I/O	LTDC_R6	
N1	VREF-	Power		
N2	PA1	I/O	ETH_REF_CLK	
N5	PC4	I/O	ETH_RXD0	
N6	PF13	I/O	FMC_A7	
N7	PG0	I/O	FMC_A10	
N8	PJ3	I/O	LTDC_R4	
N9	PE8	I/O	FMC_D5	
N11	PG5	I/O	FMC_BA1	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N12	PG4	I/O	FMC_BA0	
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	
P5	PC5	I/O	ETH_RXD1	
P6	PF14	I/O	FMC_A8	
P7	PJ2	I/O	LTDC_R3	
P8	PF11	I/O	FMC_SDNRAS	
P9	PE9	I/O	FMC_D6	
P10	PE11	I/O	FMC_D8	
P11	PE14	I/O	FMC_D11	
R1	VDDA	Power		
R3	PA7	I/O	ETH_CRS_DV	
R6	PJ0	I/O	LTDC_R1	
R7	PJ1	I/O	LTDC_R2	
R8	PE7	I/O	FMC_D4	
R9	PE10	I/O	FMC_D7	
R10	PE12	I/O	FMC_D9	
R11	PE15	I/O	FMC_D12	
R12	PE13	I/O	FMC_D10	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. DMA2D

mode: Activated

5.1.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

5.2. ETH

Mode: RMII

5.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	**00:80:E1:00:00:44 ***
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

5.2.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	

	0x0000FFFF *
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Interrupt Source Flag register Offset	**0x000B ***
PHY Link down inturrupt	**0x000B ***

5.3. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

5.3.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

5.4. LTDC

Display Type: RGB888 (24 bits)

5.4.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**41 ***
Horizontal Back Porch	**13 ***
Active Width	**480 ***
Horizontal Front Porch	**32 ***
HSync Width	40
Accumulated Horizontal Back Porch Width	53
Accumulated Active Width	533
Total Width	565

Synchronization for Height:

Vertical Synchronization Height	**10 ***
Vertical Back Porch	2
Active Height	**272 ***
Vertical Front Porch	2
VSync Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283
Total Height	285

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	**255 ***
Blue	0

5.4.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**272 ***
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	**480 ***
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	**272 ***

Pixel Parameters:

Layer 0 - Pixel Format	**ARGB1555 ***
Layer 1 - Pixel Format	**ARGB1555 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 0 - Blending Factor2	**Alpha constant x Pixel Alpha ***
Layer 1 - Alpha constant for blending	**255 ***

Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 1 - Blending Factor2	**Alpha constant x Pixel Alpha ***

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	**480 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**272 ***
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	**480 ***
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	**272 ***

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.6. SYS

Timebase Source: SysTick

5.7. USART1

Mode: Asynchronous

5.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.8. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

5.8.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.3

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**192.168.069.010 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.255.000 ***
GATEWAY_ADDRESS (Gateway Address)	000.000.000.000

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

5.8.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

5.8.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

5.8.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

5.8.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

5.8.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

5.8.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

5.8.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

5.8.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

5.8.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

5.8.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

5.8.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
FMC	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PK3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_CTRL
	PI1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED
	PI12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DISP
	PI11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTTON

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt	unused		
FMC global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	LCD_LwIP
Project Folder	C:\Users\Wim Dams\Documents\tmp\LCD_LwIP
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.12.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report