
STM32
CubeMX

1. Description

1.1. Project

Project Name	Webserver_PlatformIO
Board Name	STM32F746G-DISCO
Generated with:	STM32CubeMX 6.5.0
Date	03/31/2022

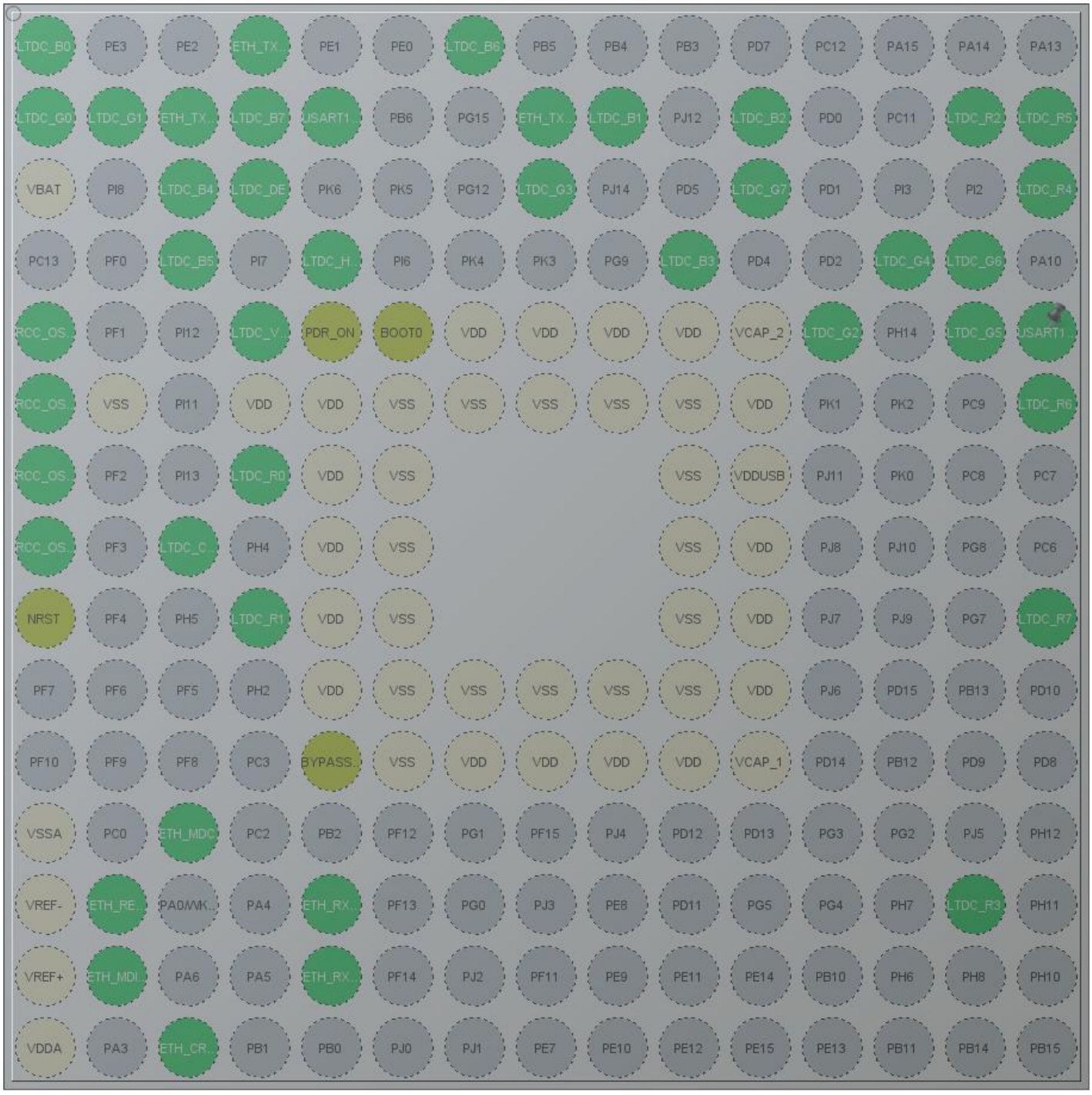
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



TFBGA216 (Top view)

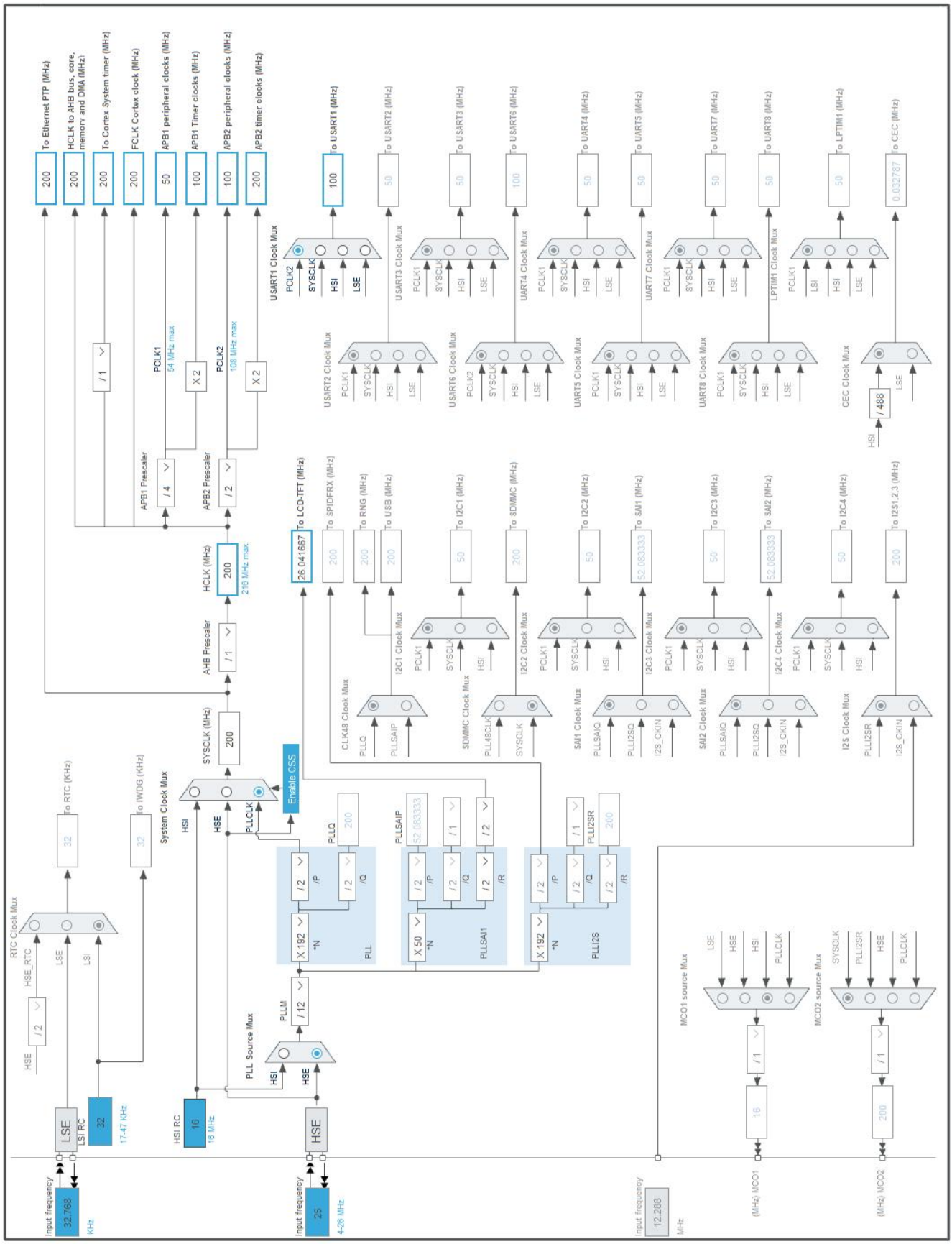
3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4	I/O	LTDC_B0	
A4	PG14	I/O	ETH_TXD1	
A7	PB8	I/O	LTDC_B6	
B1	PE5	I/O	LTDC_G0	
B2	PE6	I/O	LTDC_G1	
B3	PG13	I/O	ETH_TXD0	
B4	PB9	I/O	LTDC_B7	
B5	PB7	I/O	USART1_RX	
B8	PG11	I/O	ETH_TX_EN	
B9	PJ13	I/O	LTDC_B1	
B11	PD6	I/O	LTDC_B2	
B14	PC10	I/O	LTDC_R2	
B15	PA12	I/O	LTDC_R5	
C1	VBAT	Power		
C3	PI4	I/O	LTDC_B4	
C4	PK7	I/O	LTDC_DE	
C8	PG10	I/O	LTDC_G3	
C11	PD3	I/O	LTDC_G7	
C15	PA11	I/O	LTDC_R4	
D3	PI5	I/O	LTDC_B5	
D5	PI10	I/O	LTDC_HSYNC	
D10	PJ15	I/O	LTDC_B3	
D13	PH15	I/O	LTDC_G4	
D14	PI1	I/O	LTDC_G6	
E1	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
E4	PI9	I/O	LTDC_VSYNC	
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E12	PH13	I/O	LTDC_G2	
E14	PI0	I/O	LTDC_G5	
E15	PA9	I/O	USART1_TX	

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F1	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F15	PA8	I/O	LTDC_R6	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G4	PI15	I/O	LTDC_R0	
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H3	PI14	I/O	LTDC_CLK	
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
J1	NRST	Reset		
J4	PH3	I/O	LTDC_R1	
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		
J11	VDD	Power		
J15	PG6	I/O	LTDC_R7	
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
L5	BYPASS_REG	Reset		
L6	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
M1	VSSA	Power		
M3	PC1	I/O	ETH_MDC	
N1	VREF-	Power		
N2	PA1	I/O	ETH_REF_CLK	
N5	PC4	I/O	ETH_RXD0	
N14	PH9	I/O	LTDC_R3	
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	
P5	PC5	I/O	ETH_RXD1	
R1	VDDA	Power		
R3	PA7	I/O	ETH_CRS_DV	

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Webserver_PlatformIO
Project Folder	C:\Bachelorproef\Webserver_PlatformIO
Toolchain / IDE	Other Toolchains (GPDSC)
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LTDC_Init	LTDC
4	MX_USART1_UART_Init	USART1
5	MX_LWIP_Init	LWIP

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	DS10916_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

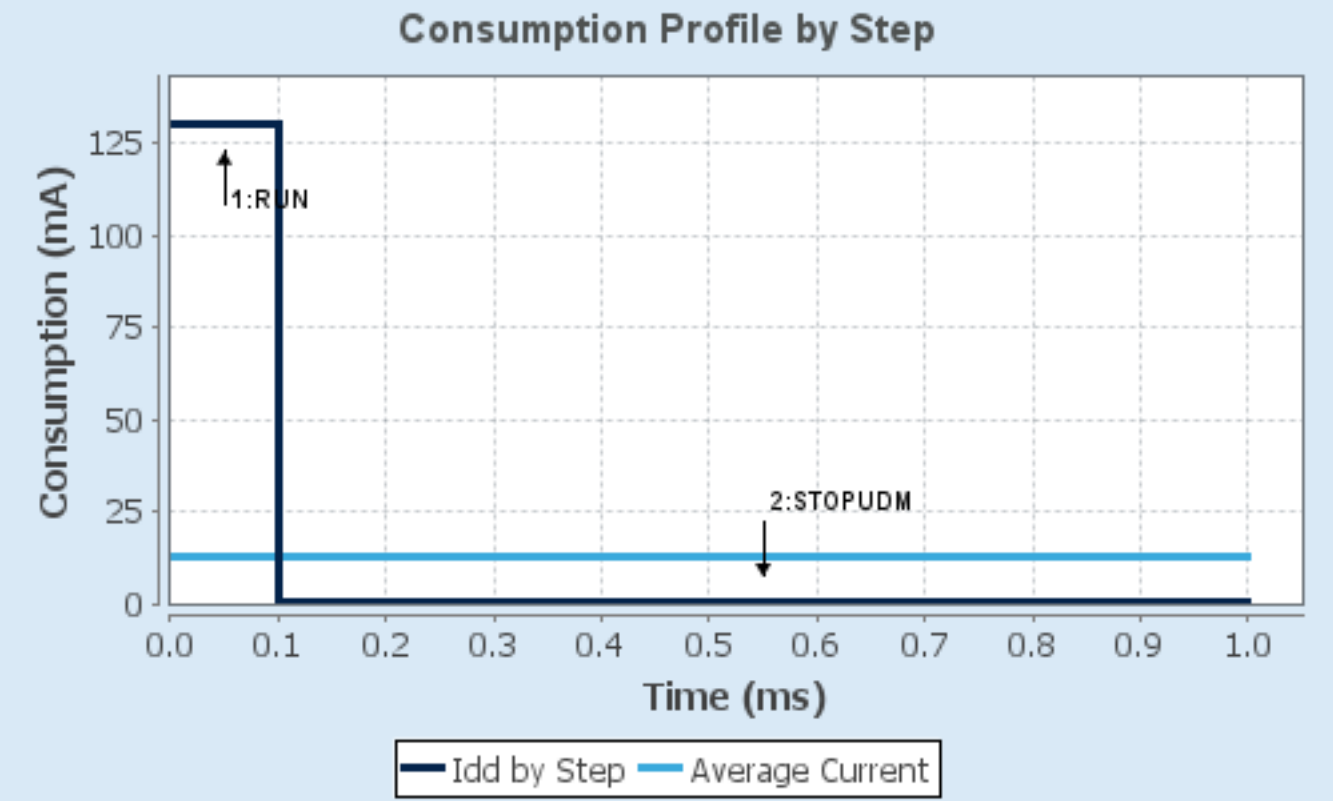
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	92.56	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ETH

Mode: RMII

7.1.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled
Speed	100 MBits/s
Duplex Mode	Full Duplex

General : Ethernet Configuration:

Ethernet MAC Address	**00:80:E1:00:00:69 ***
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.1.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***

Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Interrupt Source Flag register Offset	**0x000B ***
PHY Link down inturrupt	**0x000B ***

7.2. LTDC

Display Type: RGB888 (24 bits)

7.2.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	640
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	654
Total Width	660

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	480
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	485
Total Height	487

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low

Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	**255 ***

7.2.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**600 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**480 ***
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	**600 ***
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	**480 ***

Pixel Parameters:

Layer 0 - Pixel Format	**ARGB1555 ***
Layer 1 - Pixel Format	**ARGB1555 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 0 - Blending Factor2	**Alpha constant x Pixel Alpha ***
Layer 1 - Alpha constant for blending	**255 ***
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	**Alpha constant x Pixel Alpha ***
Layer 1 - Blending Factor2	**Alpha constant x Pixel Alpha ***

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	**600 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**480 ***
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	**600 ***
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	**480 ***

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

Timebase Source: SysTick

7.5. USART1

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.6. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.6.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.6.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

IPv4 - ICMP Options:

LWIP_BROADCAST_PING (Respond to Broadcast Pings)	**Enabled ***
LWIP_MULTICAST_PING (Respond to Multicast Pings)	**Enabled ***

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

7.6.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.6.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.6.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	**Enabled ***
HTTPD_ENABLE_HTTPS (HTTPS Support)	**1 ***

7.6.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.6.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

7.6.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.6.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.6.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.6.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.6.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI4	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI5	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA8	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current

10. Docs & Resources

Type	Link
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Training Material	https://www.st.com/resource/en/sales_guide/sg_sc2154.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32f7.pdf
Flyers	https://www.st.com/resource/en/flyer/flnucleolrwan.pdf
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