Carry-Skip and Carry-Select Adders

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1. Carry Skip Concept.
   (a) The carry skip adder (CSKA) divides the operands to be added into r bit blocks, the average size of which is n/r. Within each block, a ripple carry adder is used to produce the sum bits and a carry out bit for the block.
   (b) Setting the carry-in signal of a block to zero causes the carry out to serve as a block generate signal.
   (c) An r bit AND gate is also used to form the block propagate signal.
   (d) The block generate and block propagate signals are combined using the standard carry equation to produce the input carry to the next block.

2. A 16-bit CSKA adder with 4-bit blocks.
   (a) Draw picture of the 16-bit CSKA adder with 4-bit blocks.
   (b) In order to obtain the carry into bit position 8, we use the equation:

$$c_8 = g_{7:4} + p_{7:4} \cdot c_4$$

   where

$$p_{7:4} = p_7 \cdot p_6 \cdot p_5 \cdot p_4$$

   (c) The first and the fourth blocks are regular ripple carry adders, while the second and the third blocks are ripple carry adders, with three additional gates.
   (d) This adder requires $16 \cdot 9 = 144$ gates to implement the FAs and $2 \cdot 3 = 6$ gates to implement the carry logic, for a total of 150 gates.
   (e) It is assumed that the carry logic would be 2 gates, even though this would require a 5-input AND gate (e.g. $p_7 \cdot p_6 \cdot p_5 \cdot p_4 \cdot c_4$). The equations could easily be changed to handle only 4-input gates or less, but this would increase the gate count.
   (f) The delay for this adder is $2 \cdot 4 + 3 = 11\triangle$ to go through the first ripple carry adder $2 \cdot 2 = 4\triangle$ to go through the next two blocks, and $2 \cdot 4 + 1 = 9\triangle$ to go through the next last block, for a total delay of $24\triangle$.

3. Generalized CSKA Gate Counts
   (a) An n-bit CSKA uses n FAs, each of which requires 9 gates.
   (b) It also uses $\lceil n/r \rceil - 2$ sets of carry skip logic, each of which requires 3 gates.
   (c) Thus, the total number of gates used by an n-bit CSKA is:

$$9 \cdot n + 2 \cdot (\lceil \frac{n}{r} \rceil - 2)$$

4. Generalized CSKA Delay
   (a) The first block has a delay of $(2 \cdot r + 3)\triangle$ before the carry out is ready.
   (b) The next $(\lceil n/r \rceil - 2)$ blocks have a delay of $2\triangle$ for the carry to skip.
   (c) The last block has a delay of $2 \cdot r + 1$ from the carry in to the most significant sum bit.
   (d) Thus, the total delay is for s_{n-1} is:

$$\begin{aligned} & (2 \cdot r + 3) + 2 \cdot (\lceil \frac{n}{r} \rceil - 2) + (2 \cdot r + 1) \\ = \;& 4 \cdot r + 2 \cdot \lceil \frac{n}{r} \rceil \\ \approx \;& 4 \cdot r + 2 \cdot \frac{n}{r} \end{aligned}$$

5. Optimizing the Block Size to Reduce Delay
   (a) The optimum block size is determined by taking the derivative of the delay with respect to r, setting it to zero, and solving for

r.

$$\begin{aligned} 4 - \frac{2 \cdot n}{r^2} &= 0 \\ r &= \sqrt{n/2} \end{aligned}$$

(b) Plugging this into the delay equation gives

$$4\sqrt{n/2} + 2 \cdot \frac{n}{\sqrt{n/2}} = 4\sqrt{2 \cdot n}$$

(c) For example, if $n = 32$, then the delay is minimized by selecting $r = 4$, which gives a worst case delay of $4\sqrt{2 \cdot 32} = 32\triangle$.

(d) For $n = 16$, the delay is minimized by selecting $r = \sqrt{8} \approx 2.82$. Since r must be an integer, we can select $r = 3$ for the first five blocks, and use a full adder for the remaining bit. This adder has a worst case delay of $22\triangle$ and requires 156 gates.

6. Variable Length Blocks.

(a) The delay of the carry skip adder can be reduced even further by varying the block size.

(b) A good strategy is to use smaller blocks on the two ends and larger blocks in the middle.

(c) The design of a 16 bit CSKA with block size of $(1, 2, 3, 4, 3, 2, 1)$ requires 159 gates and has a worst case delay of $19\triangle$.

(d) Speed can also be improved by using faster block adders (e.g., CLAs) on the ends or using more than one level of carry skip logic.

7. Characteristics of CSKAs

(a) In general, CSKAs require slightly more gates than RCAs and fewer gates than CLAs.

(b) The delay for CSKAs is less than the delay for RCAs, but greater than the delay for CLAs.

(c) CSKAs are less regular than RCAs and more regular than CLAs.

8. Carry Select Concept.

(a) The carry select adder (CSEA) divides the operands to be added into r bit blocks, the average size of which is n/r.

(b) For each block, except the first, two r-bit ripple carry adders operate in parallel to form 2 sets of sum bits and carry out signals. One RCA has an initial carry in of zero and the other has an initial carry in of one.

(c) The block with a carry in of zero provides a block generate signal, and the block with a carry in of one provides a block propagate signal. These two signals are used to generate a carry out signal for the block.

(d) The carry out from the previous block controls a multiplexor that selects the appropriate set of sum bits.

9. Multiplexor Logic.

(a) A $2:1$ multiplex, with inputs x and y, select bit t, and output z, can be implemented as

$$z = x \cdot t + y \cdot \bar{t}$$

If $t = 1$, $z = x$; otherwise $z = y$.

(b) An r-bit $2:1$ multiplex requires $3 \cdot r + 1$ gates; 1 to invert t and $3 \cdot r$ to implement the AND and OR gates.

10. A 16-bit CSEA adder with 4-bit blocks.

(a) Draw picture of the 16-bit CSEA adder with 4-bit blocks.

(b) In order to obtain the carry into bit position 8, we use the equation:

$$c_8 = g_{7:4} + p_{7:4} \cdot c_4$$

where $g_{7:4}$, and $p_{7:4}$ come from the ripple carry adders.

(c) The delay for this adder is $2 \cdot 4 + 3 = 11\triangle$ to go through the first ripple carry adder, $2{\cdot}2 = 4\triangle$ to go through the next two blocks, and $3\triangle$ to go through the multiplexor. The total delay is $18\triangle$.

(d) The adder requires $28{\cdot}9 = 252$ gates for full adders, $12 \cdot 3 + 3 = 39$ gates for the multiplexors, and $2 \times 3 = 6$ gates for the carry logic. The total gate count is 297 gates.

11. Generalized CSEA Gate Counts

(a) An n-bit CSEA with r bit blocks uses $2{\cdot}n{-}r$ FAs, each of which requires 9 gates.

(b) It uses $\lceil n/r \rceil - 1$ sets of carry logic blocks, each of which requires 2 gates.

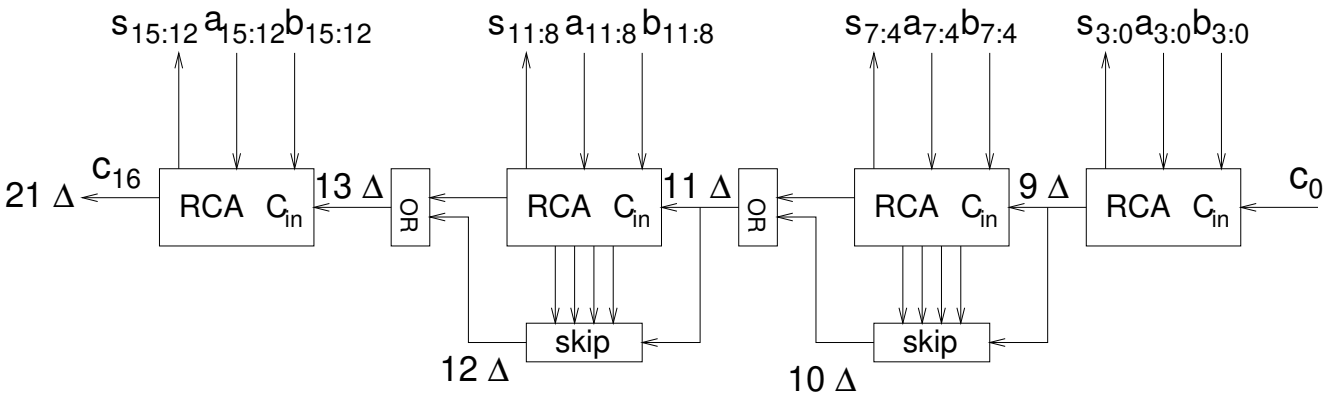

Figure 1: 16-bit Carry Skip Adder (r = 4).

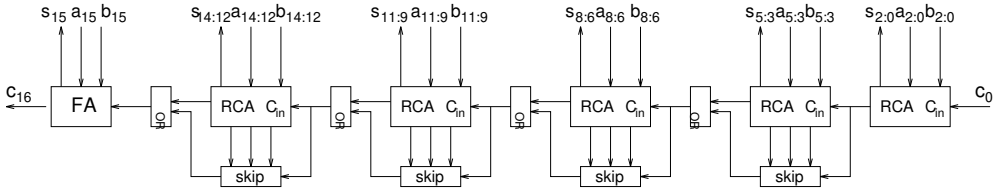

Figure 2: 16-bit Carry Skip Adder (r = 3).

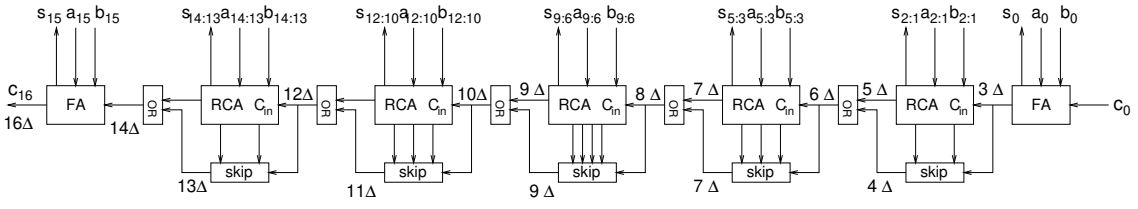

Figure 3: 16-bit Carry Skip Adder with Variable-Size Blocks.

(c) The mux logic requires $\lceil n/r \rceil - 1$ inverters and $3 \cdot (n - r)$ AND/OR gates.

(d) Thus, the total number of gates used by an n-bit CSEA is:

$$\begin{aligned} & 9 \cdot (2 \cdot n - r) + 2 \cdot (\lceil \frac{n}{r} \rceil - 1) + \\ & (\lceil \frac{n}{r} \rceil - 1) + 3 \cdot (n - r) \\ = \quad & 21 \cdot n - 12 \cdot r + 3 \cdot \lceil \frac{n}{r} \rceil - 3 \end{aligned}$$

12. Generalized CSEA Delay

(a) The first block has a delay of $(2 \cdot r + 3)\triangle$ before the carry out is ready.

(b) The next $(\lceil n/r \rceil - 2)$ blocks have a delay of $2\triangle$ for the carry logic.

(c) The last block has a delay of 3 for the multiplexor selection logic.

(d) Thus, the total delay is for s_{n-1} is:

$$\begin{aligned} & 2 \cdot r + 3 + 2 \cdot (\lceil \frac{n}{r} \rceil - 2) + 3 \; = \\ & 2 \cdot r + 2 \cdot \lceil \frac{n}{r} + 1 \rceil \approx \; 2 \cdot r + 2 \cdot \frac{n}{r} + 2 \end{aligned}$$

13. Optimizing the Block Size to Reduce Delay

(a) The optimum block size is determined by taking the derivative of the delay with respect to r, setting it to zero, and solving for r.

$$\begin{aligned} 2 - \frac{2n}{r^2} &= 0 \\ r &= \sqrt{n} \end{aligned}$$

(b) Plugging this into the delay equation gives

$$2\sqrt{n/2} + 2 \cdot \frac{n}{\sqrt{n}} + 2 = 2\sqrt{n} + 2$$

(c) For example, if $n = 16$, then the delay is minimized by selecting $r = 4$, which gives a worst case delay of $4\sqrt{16} + 2 = 18\triangle$.

14. Variable Length Blocks.

(a) The delay of the CSEA can be reduced even further by varying the block size.

(b) A good strategy is have the first two blocks be small and have the same size. Each subsequent block should have one bit larger than the previous block.

(c) For example, a 16 bit CSEA with block size of $(2, 2, 3, 4, 5)$ requires 322 gates and has a worst case delay of $16\triangle$.

(d) Speed can also be improved by using faster block adders (e.g., CLAs) and another CLA to generate the carry bits.

15. Characteristics of CSEAs

(a) In general, CSEAs require even more gates than CLAs.

(b) The delay for CSEAs proportional to $\sqrt{n}$. It is less than the delay for RCAs and CSKAs, but greater than the delay for CLAs.

(c) CSKAs are less regular than RCAs and CSKAs, and slightly more regular than CLAs.

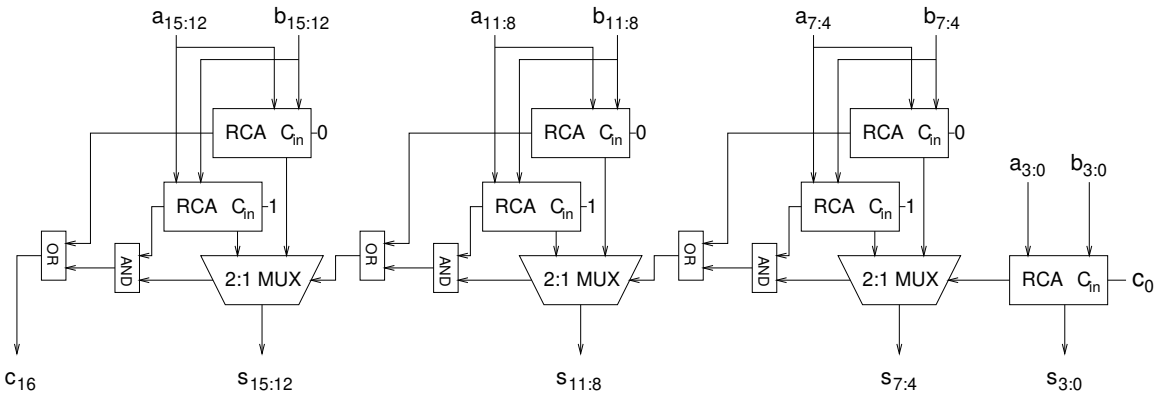

Figure 4: 16-bit Carry Select Adder (r = 4).