OSU ECEN 4233 HSCA, Spring 2024

HW 1: Crash Course Assignment on SV Simulation

Instructor: James E. Stine, Jr.

Assigned: Wednesday, 1/17, 2024
Due **Wednesday 1/31, 2024** (midnight)
Handin: `http://canvas.okstate.edu`

- Using SystemVerilog, design a unit (using RTL) that computes the following:

  1. $Z = A \cdot B + C$. You should treat both A and B as unsigned and two's complement 64-bit values and use behavioral constructs to design your HDL. That is, it should output both unsigned and two's complement results. Make sure you adequately test your design with a testbench.
  2. Write an HDL module for a hexadecimal seven-segment display decoder. The decoder should handle the digits A, B, C, D, E, and F, as well as 0–9.
  3. Write an HDL module for the FSM with the state transition diagram given below. Please make sure you adequately test this design include its reset.
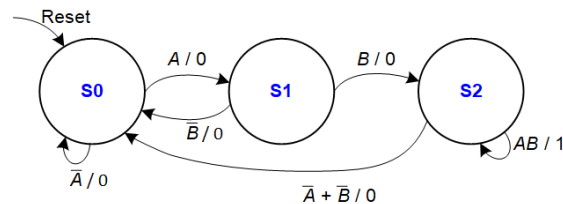
  4. Gray codes have a useful property in that consecutive numbers differ in only a single bit position. Design a 3-bit modulo 8 Gray code counter FSM with no inputs and three outputs. (A modulo N counter counts from 0 to $N - 1$, then repeats. For example, a watch uses a modulo 60 counter for the minutes and seconds that counts from 0 to 59.) When reset, the output should be 000. On each clock edge, the output should advance to the next Gray code. After reaching 100, it should repeat with 000.
  5. Extend your modulo 8 Gray code counter from the previous problem to be an UP/DOWN counter by adding an UP input. If $UP = 1$, the counter advances to the next number. If $UP = 0$, the counter retreats to the previous number. Extra credit: Add a LOAD option.

- What to hand in? (3 things!) Each design should have the following. You are welcome to combine HDLs to produce simpler output waveforms for this assignment.

  – SystemVerilog files (SV and tb)
  – DO Files
  – Simulation Waveform (please try to identify results for grader to determine the correct response easily).

Please use our DLD text [1] as well as notes on Canvas to help you get started. Do not Google anything as it just leads to problems!

References

[1] S. Harris and D. Harris, *Digital Design and Computer Architecture, RISC-V Edition*. Elsevier Science, 2021.