Reduced Area Multiplier Example

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1. Reduced Area Multiplier

This document is meant to show the in-class example of a 6-bit by 6-bit Reduced-Area or Column-Compression Multiplier. Here is a table documenting the area where the final iteration has an 7-bit CPA:

Iteration	Number of $(3,2)$ Counters	Number of $(2,2)$ Counters
1	8	2
2	6	1
3	4	2
Total	18	5

The methodology for creating Reduced-Area trees, or so they are called, can be organized into the following steps listed below.

1. Reorganize matrix into inverted triangle (optional)
2. For each stage, the number of Full Adders (FAs) used in the column i is $\#FAs = \lfloor b_i/3 \rfloor$ where b_i is the number of bits in column i.
3. Half Adders (HAs) are used only if
   (a) when required to reduce the number of bits in a column to the height specified by the Dadda sequence.
   (b) To reduce the rightmost column containing exactly two bits.
4. Repeat step (2) until the final height is 2.

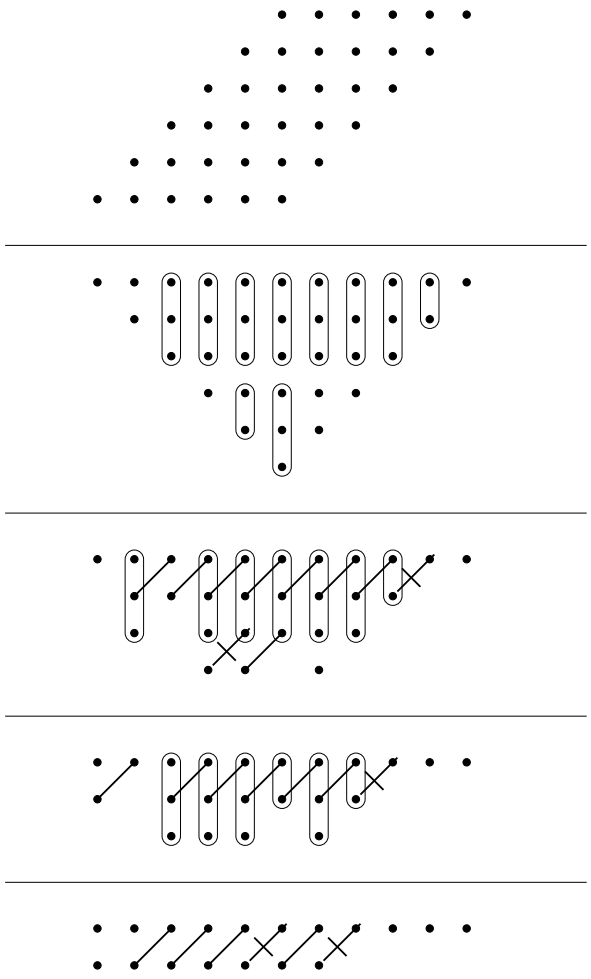

Figure 1: In-class Example of 6×6 Reduced-Area or Column-Compression Multiplier.